RICHTEK®

RTQ9683

Smart Power Stage (SPS) Module with Integrated Current and Temperature Monitors

1 General Description

The RTQ9683 is a monolithic half-bridge that integrates synchronous MOSFETs and gate drivers. It can deliver up to 30A of output current across a wide input voltage range of 4.5V to 22V.

With the integration of gate drivers and MOSFETs in a monolithic structure, the RTQ9683 achieves high-efficiency performance by optimizing driver control delay timings, along with minimizing parasitic inductance and dead time.

The RTQ9683 provides real-time current reporting function with an IMON gain 5μA/A. The RTQ9683 also has the ability to monitor junction temperature through the TMON circuit.

The RTQ9683 is available in a WQFN-21L 3x5 (FC) package. The recommended junction temperature is range −40°C to 125°C.

2 Ordering Information

RTQ9683 □-□□

- Packing
  A: Standard
- Product Grade
  T: Industrial Grade
- Package Type(1)
  N: WQFN-21L 3x5 (FC) (W-Type)

Note 1.

Marked with (1) indicated: Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

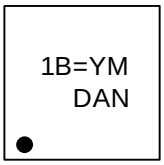
3 Features

- **30A Output Current Capability**
- **Wide VIN Input Range**
- **Switching Frequency up to 2MHz**
- **Standby Mode Quiescent Current**
- **Zero Current Detection with Middle State PWM**
- **Compatible with 3.3 V or 5 V Middle State PWM Input**
- **Current Reporting (IMON) at 5μA/A**
- **Temperature Reporting (TMON) at 8mV/°C**
- **Fault Detection: OTP**
- **Protections**
  - **Current-Limit Protections (POCP and NOCP)**
  - **Over-Temperature Protection (OTP)**
  - **Undervoltage Protection on BST-SW**

4 Applications

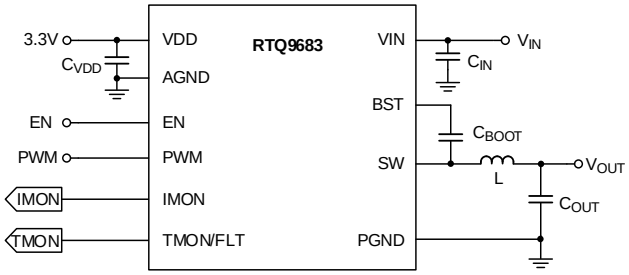
- VR for CPU, GPU, and DDR Memory Powers
- High Frequency and High Efficiency VRM

5 Marking Information



1B=: Product Code
YMDAN: Date Code

6 Simplified Application Circuit



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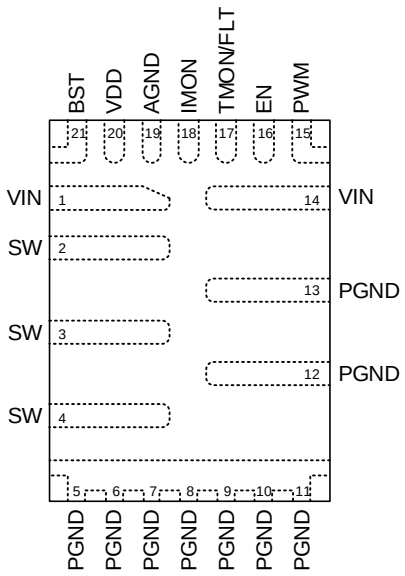
7 Pin Configuration

(TOP VIEW)

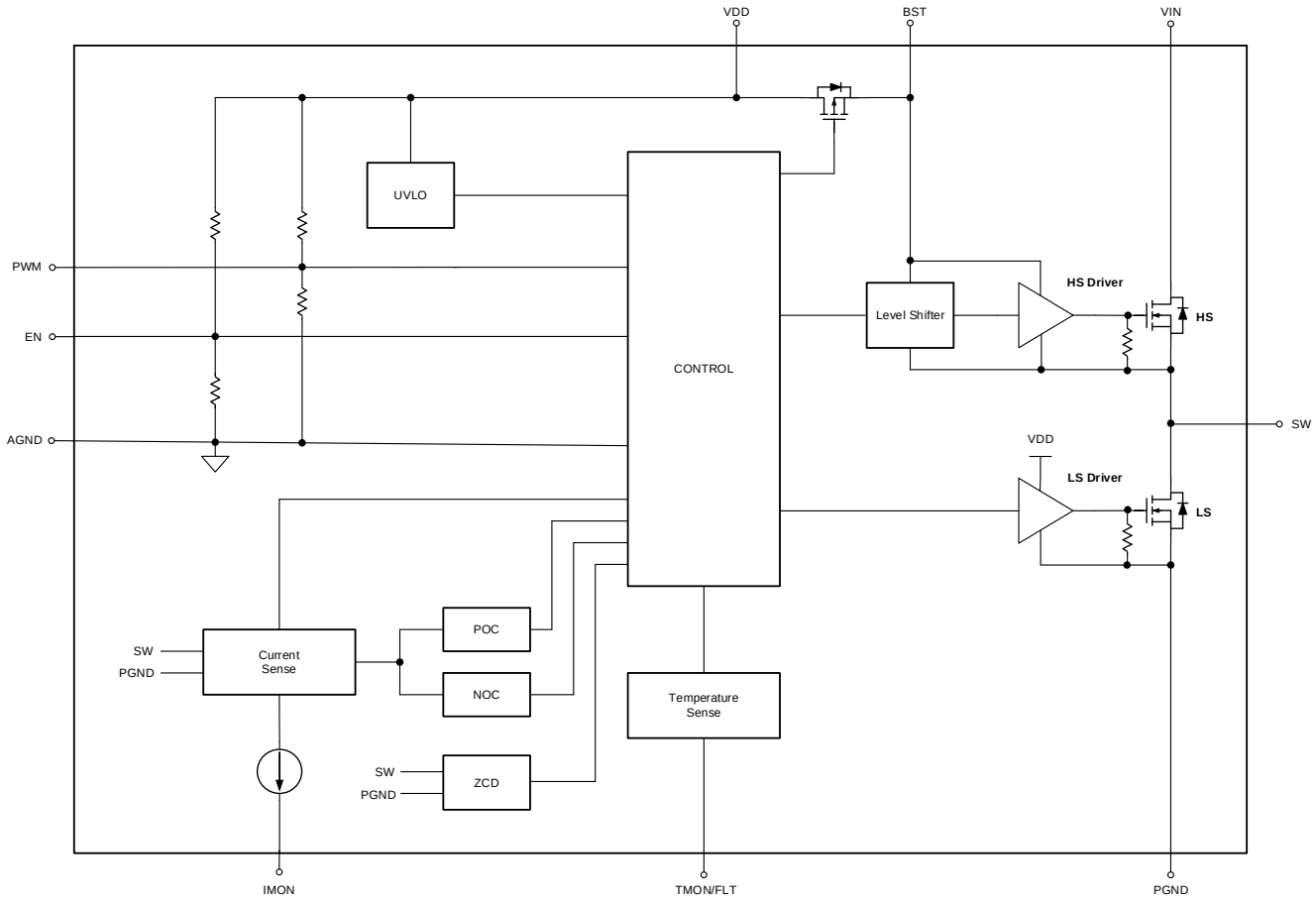


WQFN-21L 3x5 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 14	VIN	Main input power supply.
2, 3, 4	SW	Switching node between high-side and low-side MOSFETs. Connect an external power inductor to SW terminals.
5 to 13	PGND	Power ground. It is also the power ground of the synchronous MOSFET.
15	PWM	PWM signal input. Compatible with 3.3V and 5V PWM middle-state level. PWM input: “High Level” turns the control MOSFET on; “Middle-state” turns both MOSFETs off; “Low Level” turns the synchronous MOSFET on.
16	EN	Enable signal. Pulling EN high enables the driver and enters normal operation. When the EN pin and PWM are in the middle-state, the SPS enters standby mode.
17	TMON/FLT	Output thermal monitor. The voltage at this pin is defined by the equation 8mV x T_J (Celsius Temperature) + 0.6V. It is recommended to place a 100nF ceramic capacitor from TMON to PGND. Pulled high to 3.3V when OTP.
18	IMON	Output current monitor – 5μA/A.
19	AGND	Analog ground. All signals are referenced to this pin.
20	VDD	3.3V supply for control logic and gate driver. Connect this pin to 3.3V with an external RC filter (R = 2.2Ω, C = 1μF).
21	BST	Bootstrap supply for the upper gate driver. Connect a ceramic capacitor with value between 0.1μF to 1μF from BST to SW pins.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 28V
- Supply Driver Voltage, V_{DD} ---------- –0.3V to 4V
- Enable, V_{EN} ---------- –0.3V to 6.8V
- Current Monitor, V_{IMON} ---------- –0.3V to 4V
- Temperature Monitor, V_{TMON_FLT} ---------- –0.3V to 4V
- PWM Input, V_{PWM} ---------- –0.3V to 6.8V
- Phase, SW to PGND, V_{SW}
  - DC ---------- –0.3V to 26V
  - <25ns ---------- –5V to 32V
- Bootstrap, BST to PGND, V_{BST} ---------- –0.3V to V_{SW} + 4V
- Instantaneous Peak Current (20ms) ---------- 50A
- Instantaneous Peak Current (10ms) ---------- 65A
- Instantaneous Peak Current (10μs) ---------- 70A
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  - HBM (Human Body Model) ---------- 2kV
  - CDM (Charged Device Model) ---------- 500V

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, V_{IN} ---------- 4.5V to 22V
- Supply Control Input, V_{DD} ---------- 3V to 3.6V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WQFN-21L 3x5 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	50.1	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	15.27	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	0.72	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	18.4	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10	°C/W

Note 5. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board (Richtek EVB) which is in size of 123mm x 68mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions

14 Electrical Characteristics

(V_{DD} = 3.3V, T_J = –40°C to 125°C, unless otherwise specified.)

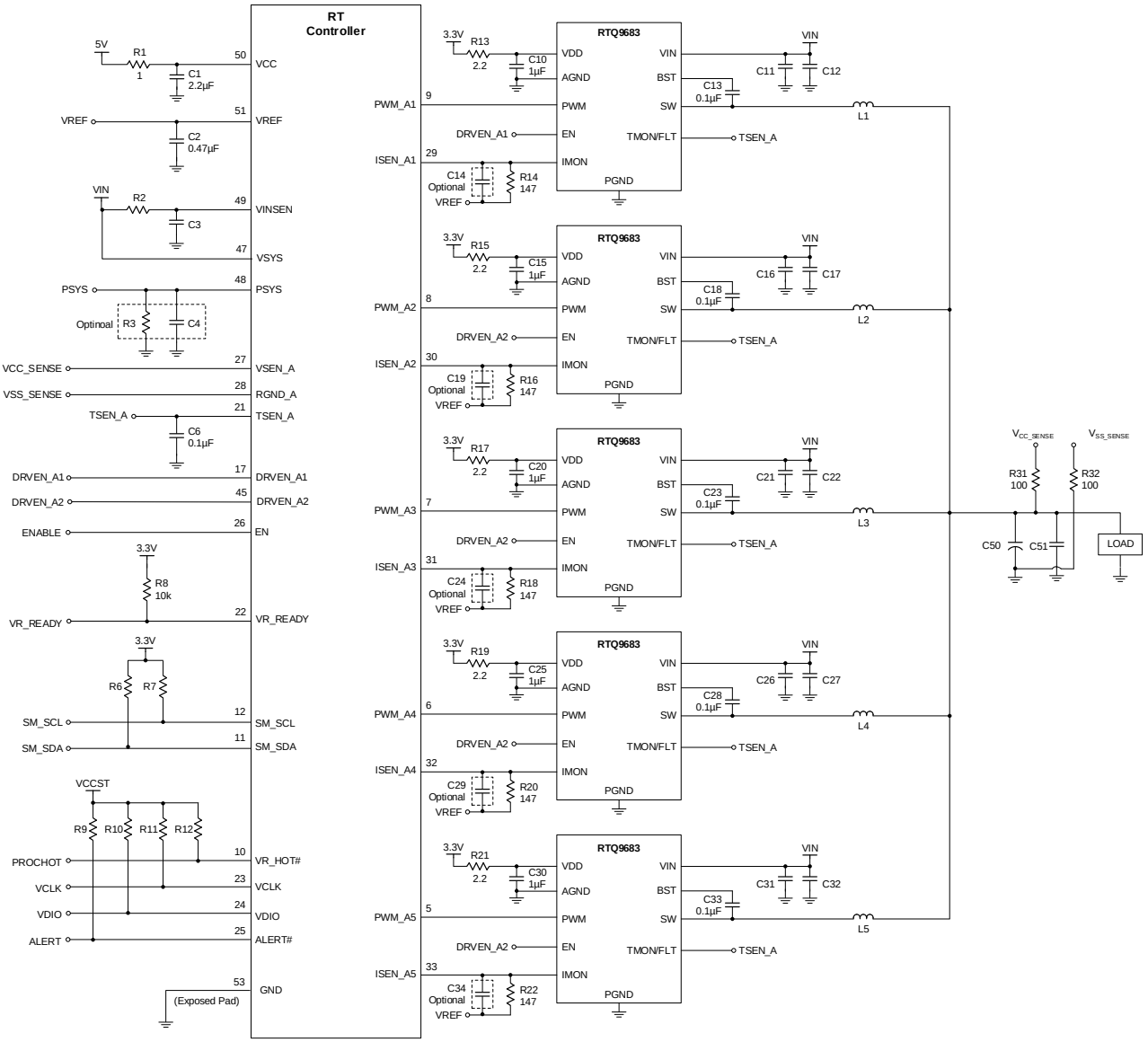
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply Characteristics						
VIN Quiescent Current	$I_{IN\ STBY}$	PWM = Middle State, EN = Middle State, V_{IN} = 4.5V to 22V, T_A = 25°C	--	--	1	μA
VDD Quiescent Current in Standby Operation	$I_{DD\ STBY}$	PWM = Middle State, EN = Middle State, V_{IN} = 4.5V to 22V, T_A = 25°C	--	--	10	μA
VDD Quiescent Current in Normal Operation	I_{DD}	PWM = Middle State, EN = H/L	--	--	1.6	mA
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}		--	2.74	2.95	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		--	0.23	--	V
POR Delay Time	TD_POR		--	--	250	μs
Enable Characteristics						
EN Input Logic-High	V_{EN_H}		2.75	--	--	V
EN Input Middle Threshold	V_{EN_M}		1.1	--	2	V
EN Input Logic-Low	V_{EN_L}		--	--	0.47	V
EN Input Middle State Voltage	V_{EN_FLOAT}	EN= Floating	1.48	1.65	1.82	V
EN Input Pull-Up Resistor (Note 7)	R_{EN_PU}		--	100	--	kΩ
EN Input Pull-Down Resistor (Note 7)	R_{EN_PD}		--	100	--	kΩ
Standby Mode Entry Delay Time	T_{STBY_ENTRY}	EN = H to Middle-state, PWM = Middle-state	--	4	--	μs
Standby Mode Exit Delay Time	T_{STBY_EXIT}	EN = Middle-state to H	--	--	44	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Signal Characteristics						
PWM High to SW Rising Delay (Note 7)	t_R	PWM = H, SW rising to 1V	--	40	--	ns
PWM Low to SW Falling Delay (Note 7)	t_F	PWM = L, SW falling to (V_{IN}-1V)	--	40	--	ns
PWM Middle State to HS Off Delay (Note 7)	t_{H-M}	PWM High to Middle state	--	70	--	ns
PWM Middle State to LS Off Delay (Note 7)	t_{L-M}	PWM Low to Middle state	--	70	--	ns
PWM Middle State to HS On Delay (Note 7)	T_{M-H}	PWM Middle state to High	--	40	--	ns
PWM Middle State to LS On Delay	T_{M-L}	PWM Middle state to Low	--	40	--	ns
PWM Input Pull-Up Resistor (Note 7)	R_{PWM_PU}		--	14	--	kΩ
PWM Input Pull-Down Resistor (Note 7)	R_{PWM_PD}		--	14	--	kΩ
PWM Input Logic-High	V_{PWM_H}		2.65	--	--	V
PWM Input Logic-Low	V_{PWM_L}		--	--	0.48	V
PWM Input Middle State Threshold	V_{PWM_M}		1.1	--	2	V
Minimum HS On-Time (Note 7)	t_{ON_MIN}		--	47	--	ns
Dead-Time Rising (Note 7)	t_{DT_R}		--	4	--	ns
Dead-Time Falling (Note 7)	t_{DT_F}		--	12	--	ns
IMON Characteristics						
IMON Gain (Note 7)	I_{MON_GAIN}		--	5	--	μA/A
IMON Gain Accuracy	I_{MON_ACC}	5A ≤ I_{SW} ≤ 40A	–3	--	3	%
		1A ≤ I_{SW} < 5A	–10	--	10	
IMON Offset	I_{MON_OFFSET}	I_{OUT} = 0A, T_A = 25°C	–2.5	--	2.5	μA
IMON Reference Voltage Range	V_{REF}		0.8	--	2	V
TMON Characteristics						
TMON Gain (Note 7)	T_{MON_GAIN}		--	8	--	mV/°C
TMON Voltage Range (Note 7)	V_{TMON}	T_J = 25°C	--	0.8	--	V
		T_J = 100°C	--	1.4	--	
		T_J= 150°C	--	1.8	--	
Over-Temperature Protection Threshold (Note 7)	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis (Note 7)	T_{OTP_HYS}		--	20	--	°C
TMON Voltage when Fault	V_{TMON_FLT}		--	3.3	--	V
Protections						
Positive Inductor Peak Current Limit (Note 7)	I_{LIM_PEAK}		--	70	--	A

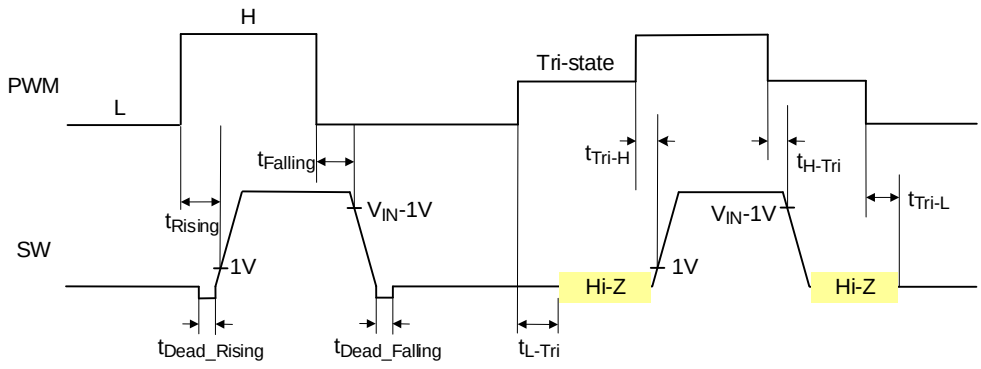
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Inductor Peak Current Limit Hysteresis (Note 7)	$I_{LIM\_PEAK\_HYS}$		--	20	--	A
Negative Inductor Peak Current Limit (Note 7)	$I_{LIM\_PEAK\_NEG}$		--	–20	--	A
Negative Inductor Peak Current Limit Hysteresis (Note 7)	$I_{LIM\_PEAK\_NEG\_HYS}$		--	10	--	A
Boot Low Rising Threshold (Note 7)	V_{BTLOW_R}		--	2.6	--	V
Boot Low Falling Threshold (Note 7)	V_{BTLOW_F}		--	2.4	--	V

Note 7. Guaranteed by design.

15 Typical Application Circuit

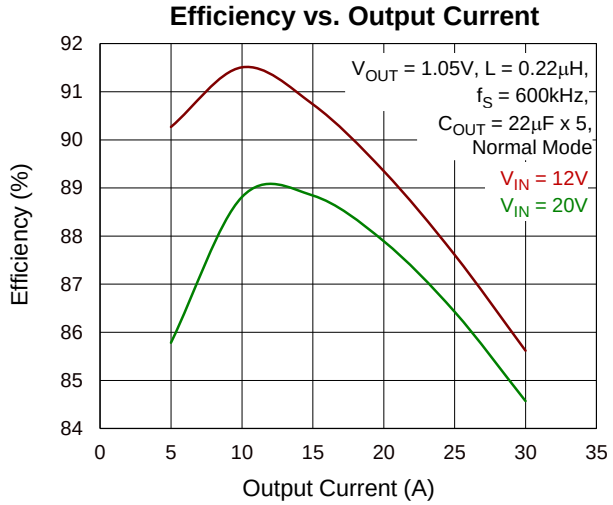


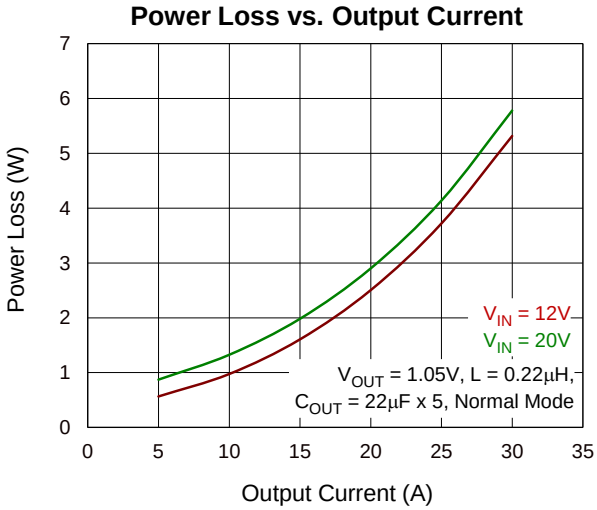
16 Timing Diagram



Note 8. SW is drawn at positive inductor current.

17 Typical Operating Characteristics





18 Operation

The RTQ9683 is a 30A monolithic half-bridge driver with integrated MOSFETs. It is suited for multi-phase buck regulators. When the VDD exceeds the V_{UVLO} rising threshold and VBST is sufficiently high, the device begins operating.

18.1 Pulse-Width Modulation (PWM)

The PWM pin of the RTQ9683 supports a three-level (H, L, and Middle state) PWM signal and is compatible with 3.3V and 5V PWM logic. When the PWM input signal is within the middle state logic level for 70ns (t_{H-M} or t_{L-M}), the high-side MOSFET (HS-FET) turns off instantaneously, and diode emulation is active. The LS-FET remains on until the inductor current is nearly zero, which is detected by the zero-current detection (ZCD) circuit. The PWM signal keeps in the middle state by floating the PWM input. The internal voltage divider will pull the signal to the middle state.

18.2 Enable input (EN)

Enable signal. Pulling EN high enables the driver and enters normal operation. When the EN pin and PWM are in the middle state, the SPS enters standby mode with quiescent current. Table 1 shows the operation mode truth table for EN and PWM inputs.

Table 1

Mode	EN	PWM	HS	LS	TMON/FLT	IMON	NOTE
Standby	MID	MID	OFF	OFF	OFF	OFF	
Normal	H/L	H	ON	OFF	Measured	Measured	
Normal	H/L	L	OFF	ON	Measured	Measured	
Normal	H/L	MID	OFF	Diode Emulation	Measured	Measured	

18.3 Standby Mode

When the EN pin is in a middle state and the PWM signal is forced to a middle state voltage for 4μs, the RTQ9683 enters standby mode. In standby mode, the device shuts down, and the IMON, OTP, and TMON/FLT outputs are disabled.

18.4 Positive and Negative Inductor Current Limit

While the output current exceeds the I_{LIM_PEAK} threshold by detecting on the HS-FET, the HS-FET turns off and the LS-FET remains on. The positive inductor peak current limit (POCP) is automatically disabled until the inductor current is lower than the releasing threshold (I_{LIM_PEAK} - $I_{LIM\_PEAK\_HYS}$).

When the LS-FET detects a current lower than the $I_{LIM\_PEAK\_NEG}$ threshold, the RTQ9683 turns off the LS-FET and immediately turn off LS to limit the negative current. The negative inductor peak current limit (NOCP) is automatically disabled once the current is above the releasing threshold ($I_{LIM\_PEAK\_NEG}$ + $I_{LIM\_PEAK\_NEG\_HYS}$).

18.5 BST-SW Undervoltage Protection

The BST-SW voltage is applied to the HS-FET gate while PWM is high. A low BST-SW voltage weakens the gate drive of the HS-FET, leading to a higher HS RDS (ON) and an increased risk of unreliable operation. To prevent this, the RTQ9683 incorporates undervoltage circuitry for the bootstrap capacitor. When the BST-SW voltage is below the V_{BTLOW_F} voltage, the HS-MOSFET will turn off in the next PWM cycle until the BST-SW voltage recovers to the V_{BTLOW_R} voltage. During BST-SW undervoltage protection, the operation of the low-side MOSFET will continue to follow the PWM pattern.

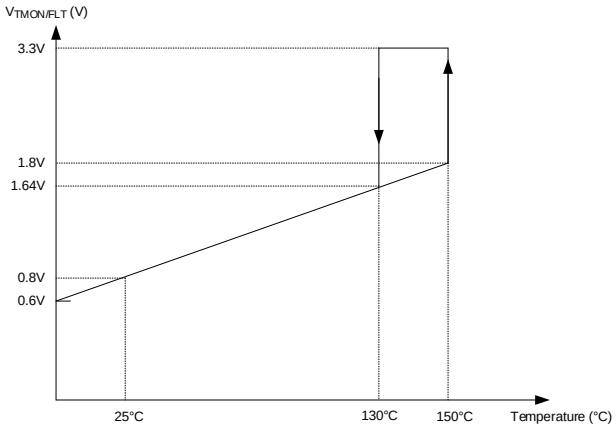
18.6 Over-Temperature Protection (OTP)

Once the junction temperature rises above the over-temperature rising threshold (150°C), the LS-FET turns on and stays on until ZCD. The RTQ9683 will automatically recover when the temperature falls below the falling threshold of 130°C.

18.7 Junction Temperature Sense and Fault Detection

The RTQ9683 features an internal temperature sensing circuit that is proportional to T_J when the RTQ9683 is in normal operation. The sensed temperature is reported at the TMON/FLT pin with a linear voltage slope of 8mV/°C and a 600mV offset at 0°C, as shown in the following equation:

$$V_{TMON\_FLT}\,(V) = 0.6V + 0.008V/^oC \times T_J(^oC)$$



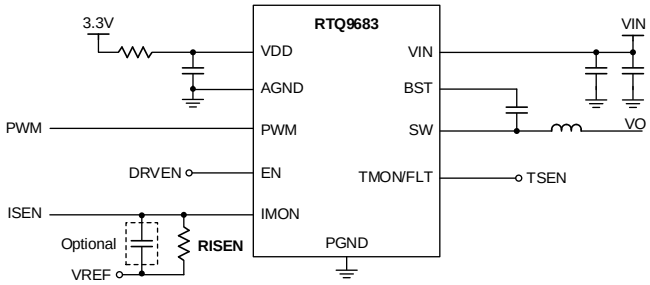
The TMON/FLT pin also provides the OTP fault flag. The TMON/FLT pin will go high to 3.3V when a fault occurs.

18.8 Current-Sense (IMON) Output

The IMON output is a current source that is proportional to the inductor current, with a gain of 5μA/A. The IMON current creates a proportional voltage drop across the R_{ISEN} resistor, terminated to an external voltage reference and differentially sensed by an external controller. The purpose of the IMON feature is to replace DCR current sensing or output current sensing using an external precision resistor. Both techniques are lossy and lead to reduced system efficiency. Inductor DCR sensing is also inaccurate for low-value DCR inductors. The accuracy of the IMON signal is ±3% from 5A to 40A output current.

To display the bidirectional current value on the IMON pin, it is necessary to provide a reference voltage (V_{REF}). The V_{IMON} voltage on the IMON pin must be maintained within the range of 0.8V to 2V. The required V_{REF} is shown in the following equation:

$$V_{IMON}\,(V) = V_{REF} + R_{ISEN} \times IMON$$



19 Application Information

(Note 9)

19.1 Bootstrap Circuit Component Selection

Connect an external capacitor (C_{BOOT}) between BST and SW. For effectively turning the high-side MOSFET on, the stored energy in C_{BOOT} needs to be greater than the total gate charge of the high-side MOSFET. Calculating V_{CBOOT} is essential to ensure MOSFET safe operation in the ohmic region. As a result, V_{CBOOT} must be large enough to avoid the high-side MOSFET from being incompletely turned on. The value of the bootstrap capacitor is defined using the following equation:

$$C_{BOOT} \geq \frac{Q_{gH}}{\Delta V_{CBOOT}}$$

where ΔV_{CBOOT}: Maximum allowable voltage drop on bootstrap capacitor.

Q_{gH}: The gate charge of the HS-FET.

In practice, a low-value capacitor C_{BOOT} will lead to overcharging that can damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on C_{BOOT}, it is recommended to connect a ceramic capacitor with a value of 0.1μF between the BST and SW pins for proper operation.

19.2 Layout Considerations

See Figure 1 for placement recommendations.

- All high−current paths, such as VIN, SW, VO, and PGND coppers traces, should be short and wide for low parasitic inductance and resistance.
- As a primary consideration, the decoupling capacitors for VDD, VBST, and VIN should be placed on the same layer as the SPS.
- It is recommended to route the signal traces (Pin 15 to Pin 21) with a 10mil trace width or greater.
- Minimize the SW copper area and route sensitive traces away from the SW and BST pins, as these high dv/dt nets are prone to capacitive coupling.
- AGND and PGND should only be connected at a single pad.
- Adding a high-frequency bypass capacitor C_{VIN2} (0.1μF/25V/0402) close to pin1 can help reduce switching spikes.
- To achieve better thermal performance and minimize parasitic impedance, additional VIAs can be placed under the VIN and PGND copper planes.
- Keep the IMON signal away from high dv/dt paths and use a ground plane to isolate it from noise signals.
- Implement a low-pass RC filter between the VDD and AGND pins, consisting of the C_{VDD} bypass capacitor and a 0 to 2.2Ω resistor.
- Increase the copper plane size to minimize parasitic impedance on the bootstrap capacitor charging path.
- Ensure to place the C_{BOOT} as close to the BST and SW pins as feasible.
- The C_{BOOT} can be any size. However, keep the effective capacitance larger than 0.1μF under all conditions.
- Place RC snubbers between SW and ground to absorb SW ringing if required.

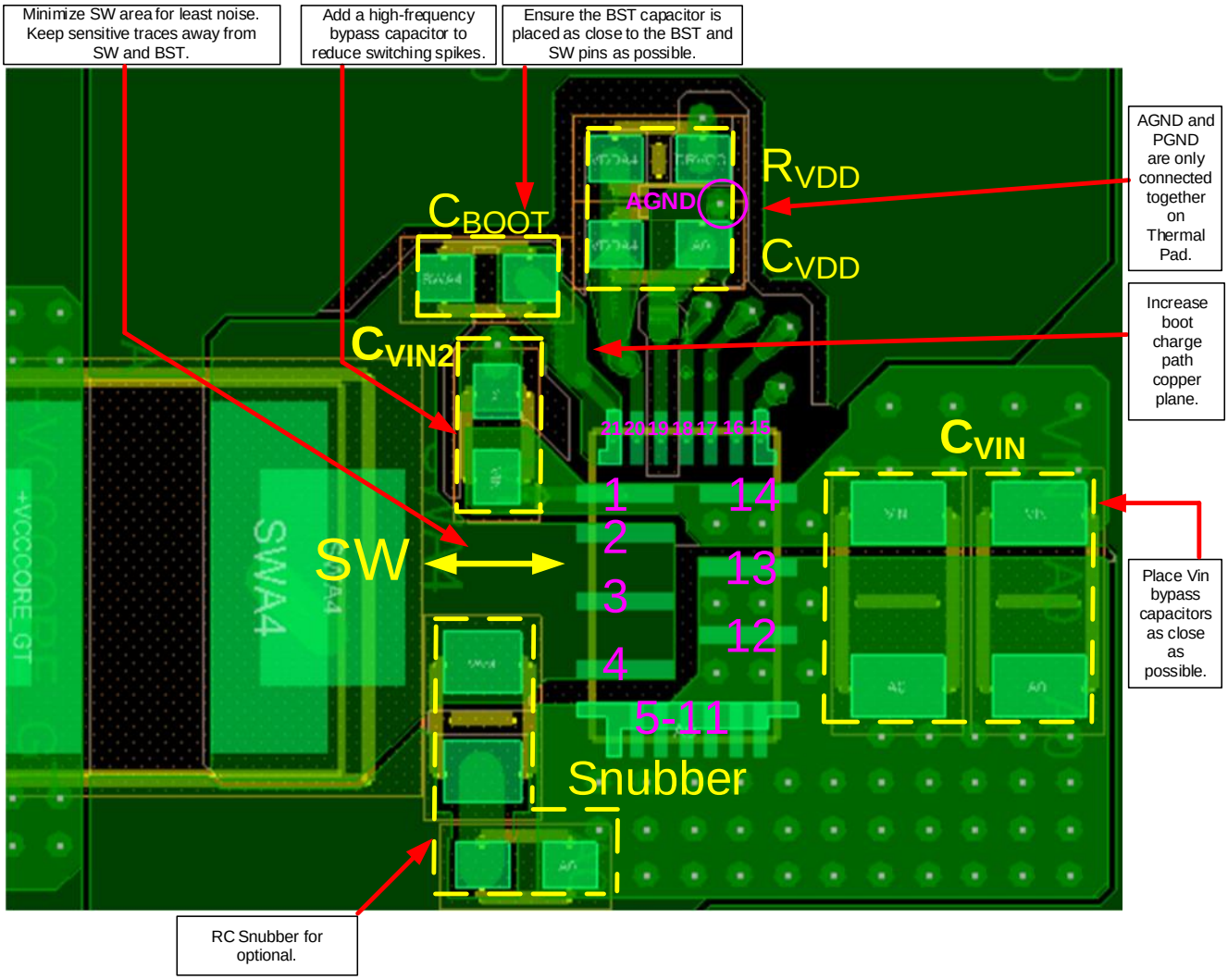
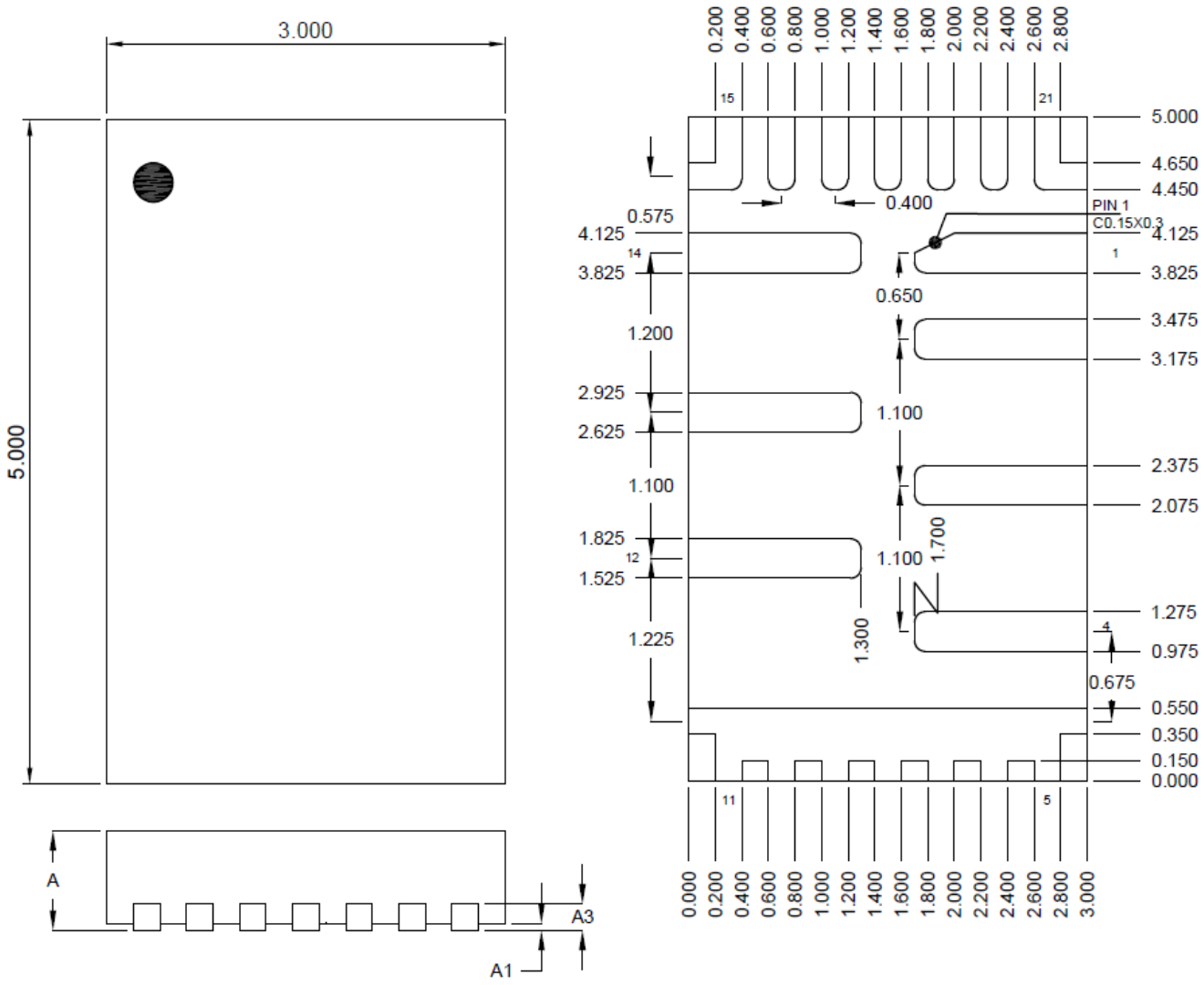


Figure 1. PCB Layout Guide

Note 9. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

20 Outline Dimension

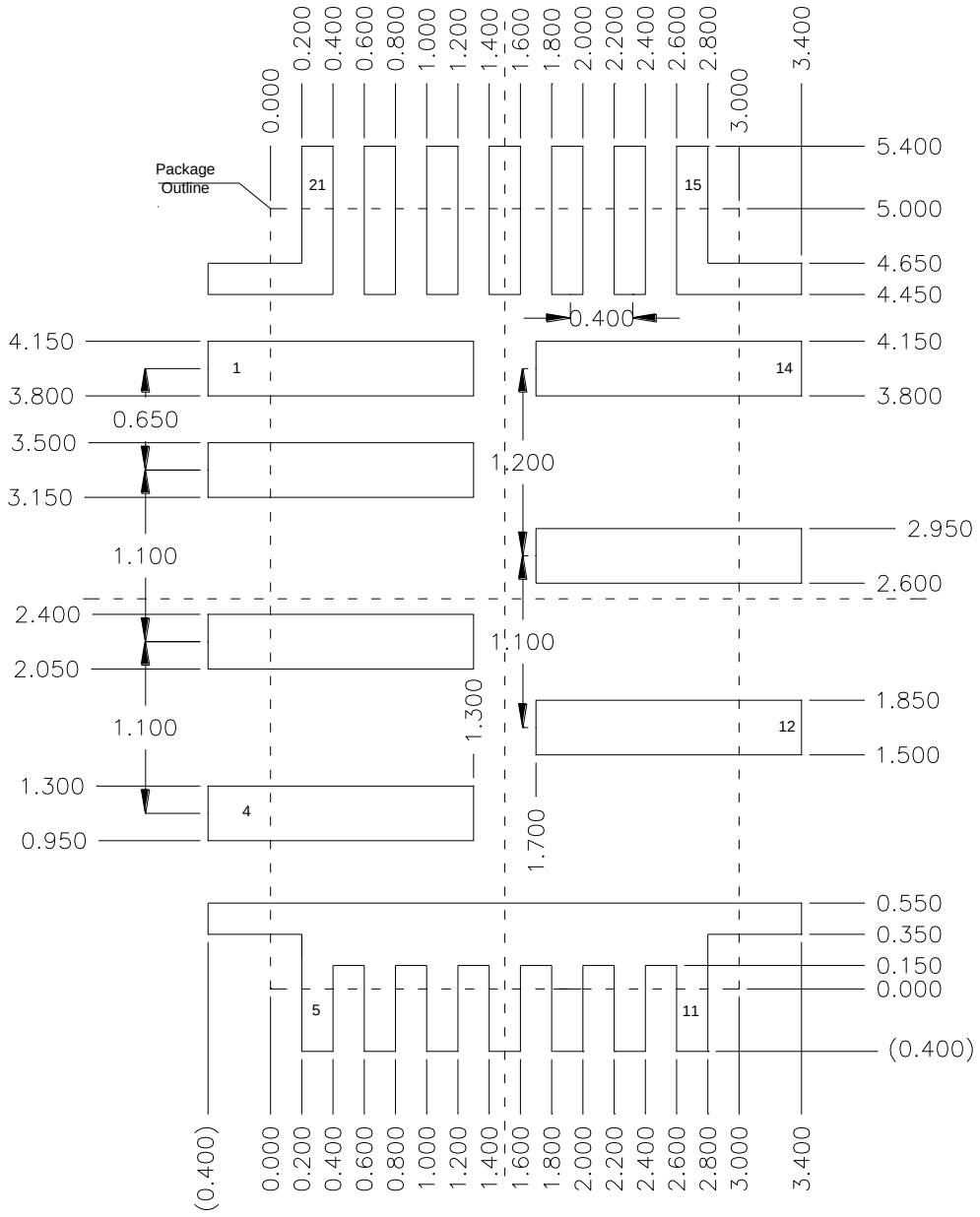


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 21L QFN 3x5 Package (FC)

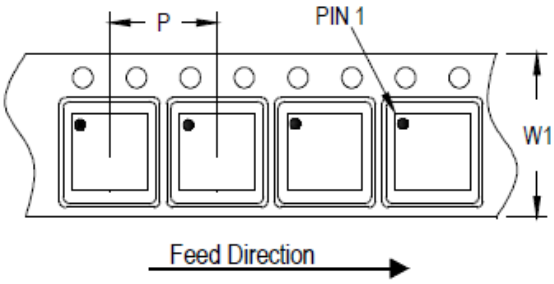
21 Footprint Information

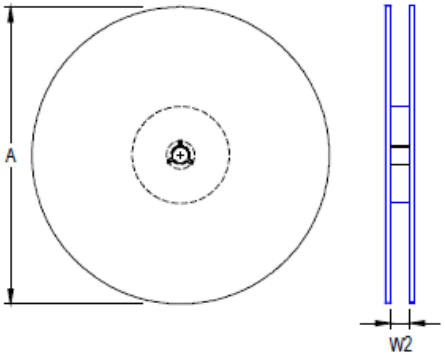


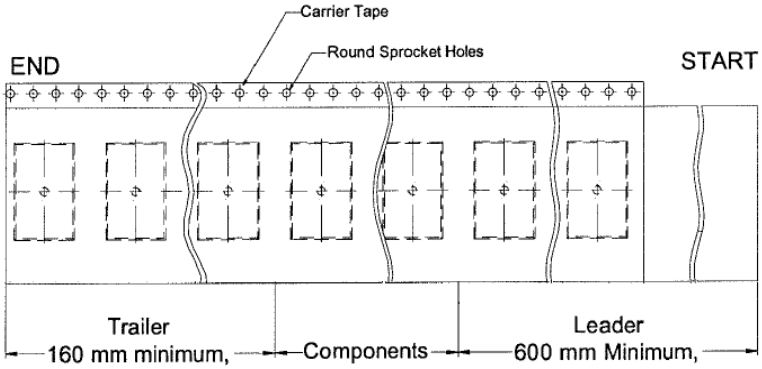
Package	Number of Pin	Tolerance
V/W/U/XQFN3x5-21(FC)	21	±0.05 mm

22 Packing Information

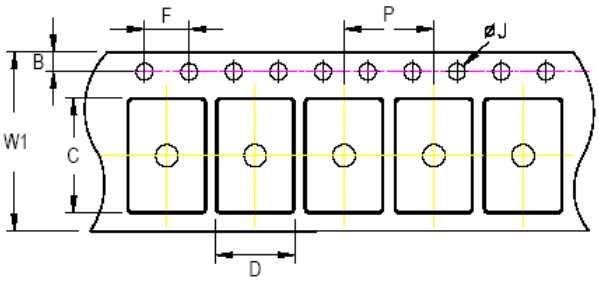
22.1 Tape and Reel Data

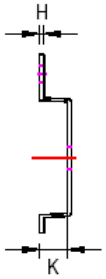






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x5	12	8	180	7	1,500	160	600	12.4/14.4





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description	Item
00	2024/7/8	Final	Functional Pin Description on P3 Absolute Maximum Ratings on P5 Electrical Characteristics on P6 Timing Diagram on P9 Operation on P11, P12