RICHTEK®

RTQ7883A-QT

USB Type-C PD and PWM Buck Converter with AnyPower and PD Safe Features

1 General Description

The RTQ7883A-QT is a highly integrated functions USB Type-C Power Delivery (USBC PD) with internal 2 switch PWM buck converter up to 3A output current and duty cycle 99% for low dropout operation. The IC has an embedded ARM Cortex-M0 MCU, which handles various functions of communication protocol, smart control of the PWM converter, firmware-based protections, and customized functions. The IC features hardware-based protections, such as inductor peak current limit, VBUS overvoltage protection (VBUS OVP) and VO undervoltage protection (VO UVP), so that the protections have faster responses and can still function even when the MCU is not activated. The RTQ7883A-QT can offer an excellent USB PD solution for a USB-PD Provider application with few external components and simple PCB layout.

The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

2 Ordering Information

RTQ7883A□□-QT□

Packing
A: Standard

Grade
QT: AEC-Q100 Qualified

Package Type(1)
N: WQFN-42L 6x6 (W-Type) (Exposed Pad)

Function Code

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

3 Applications

- Automotive USB Type-C Power Delivery Charger

4 Features

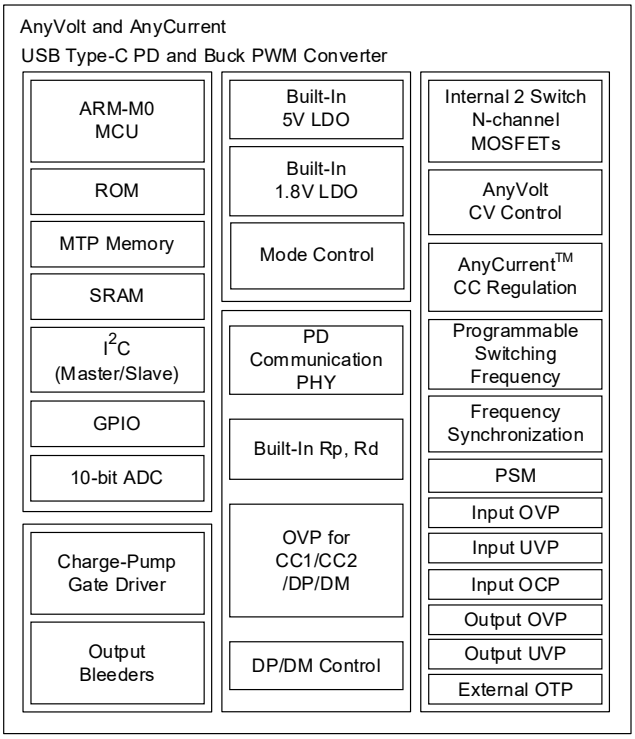
- **AEC-Q100 Grade 1 Qualified**
- **USB PD PD3.1/PPS Certification Passed (TID 10022)**
- **UFCS Certification Passed (UFCS00104)**
- **Operating Ambient Temperature: –40°C to 125°C**
- **Junction Temperature: –40°C to 150°C**
- **Type-C, USB PD, and Communication Protocols**
  - **Compliant with USB PD 3.1 Specification, USB Type-C Cable, and Connector Specification 2.1**
  - **Support Other Proprietary Communication Protocols through Internal MCU, DP, and DM Pins**
- **Integrated PWM Buck Converter**
  - **Wide Input Voltage Range: 4.5V to 30V, 4.5V to 36V (<0.4s)**
  - **Wide Output Voltage Range: 3.3V to V_{IN} (21V Maximum)**
  - **Maximum 3A Output Current**
  - **Internal 2 Switch N-Channel MOSFETs**
  - **Duty 99% for Low Dropout Operation**
  - **Peak-Current Mode PWM Operation**
  - **Internal Compensation for CV, CC**
  - **Programmable PWM Switching Frequency (200kHz to 600kHz)**
  - **Pulse-Skipping Mode for Light-Load Efficiency**
- **AnyPower for Constant Voltage Output (9.93mV/Step, Typ.) and Constant Current Output (in 10-Bit Resolution)**
- **PD Safe**
  - **Adjustable Converter Input Current Limit (INOC)**
  - **Fast Response VIN OVP/UVP Detection**
  - **Programmable VBUS OVP and VO UVP**
  - **Fast Response OVP for CC1/2 and DP/DM**
  - **Adjustable External OTP/Internal OTP**
- **VBUS Cable Voltage Drop Compensation**
- **Switching Frequency Synchronization for Better EMI**

- **Master/Slave I²C Interface**
- **GPIOs for MUX Control or Customized Functions**
- **Built-In Output Bleeders for Quick VBUS Discharge**
- **Built-In Charge Pump for Driving N-Channel MOSFETs**
- **Built-In Internal LDO**
- **Online Firmware Update via Slave I²C or CC1/2 Interface**
- **Available in WQFN-42L 6x6 Package**

5 Marking Information

RTQ7883ALN: Product Code
QT: Automotive Product Grade
YMDAN: Date Code

6 Simplified Functional Block Diagram



7 Simplified Application Circuit

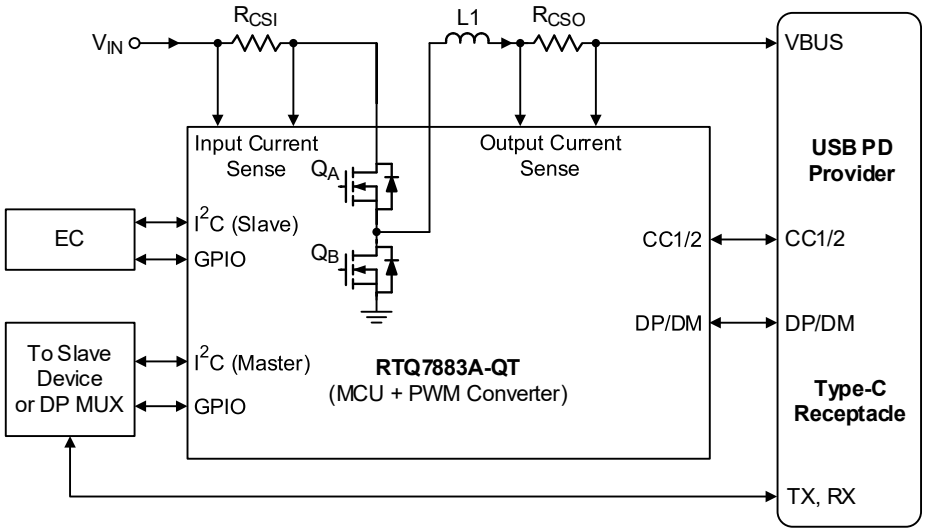
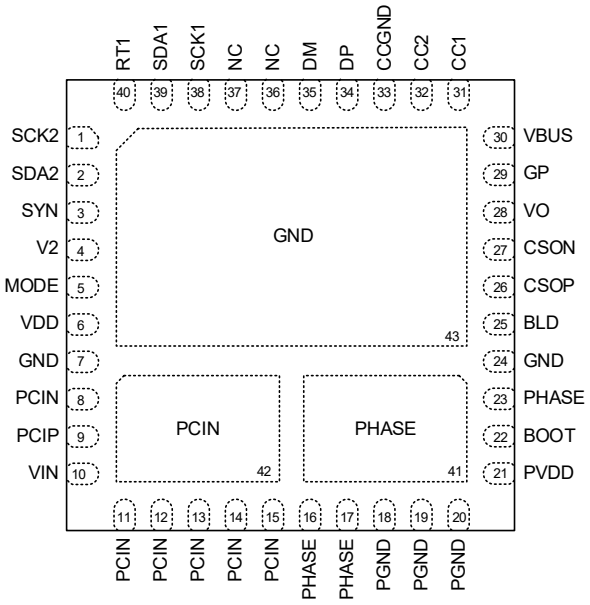


Table of Contents

8 Pin Configuration

(TOP VIEW)



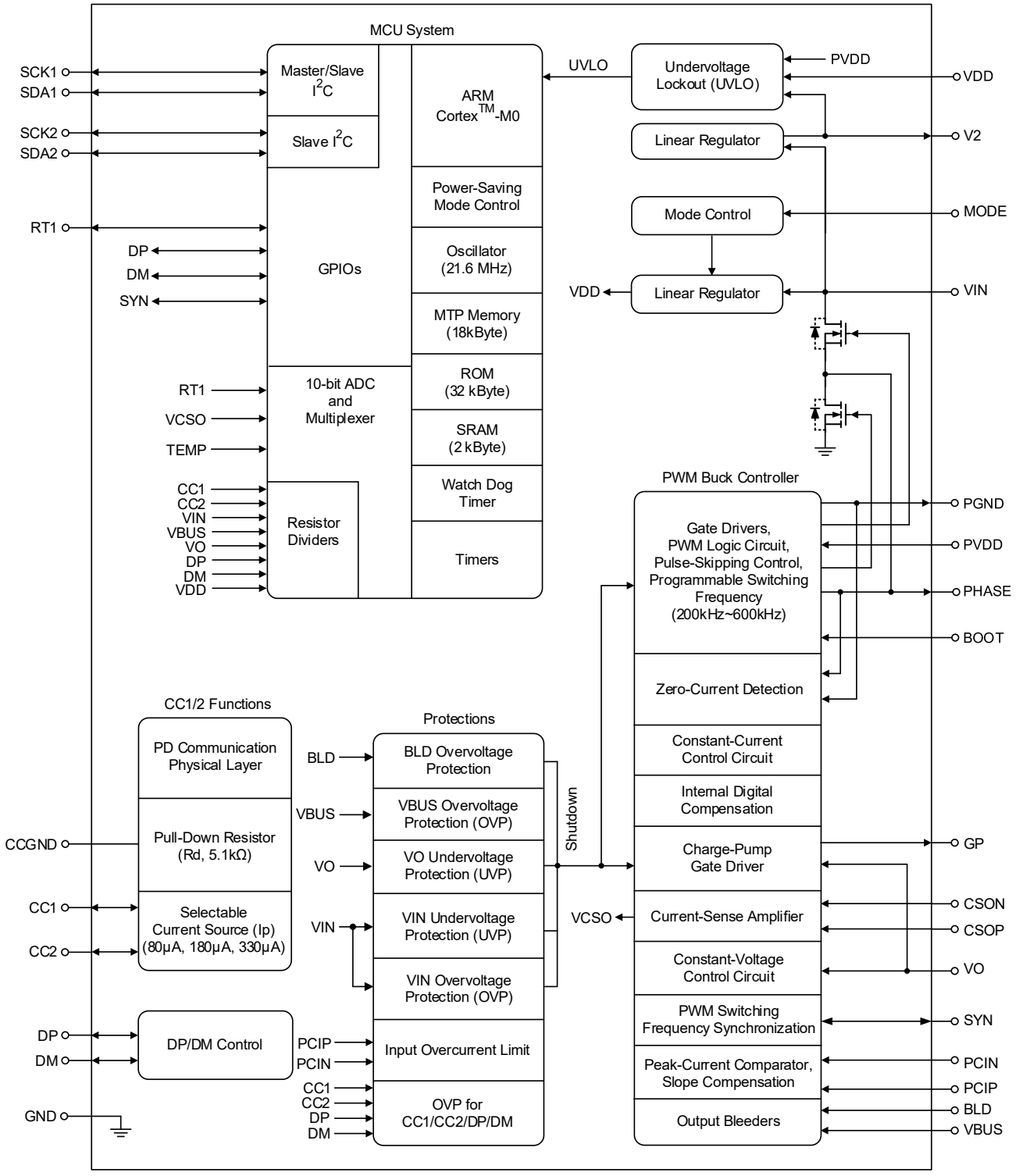
WQFN-42L 6x6

9 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SCK2	Open-drain clock signal input/output pin of the Slave I^2C Interface. This pin can be set as an open-drain or push-pull GPIO pin.
2	SDA2	Open-drain data signal input/output pin of the Slave I^2C Interface. This pin can be set as an open-drain or push-pull GPIO pin.
3	SYN	Switching frequency synchronization in two port application. This pin can be set as an open-drain or push-pull GPIO pin.
4	V2	Internal 1.8V linear regulator output to supply power for internal circuitry. An MLCC (1μF) must be connected from this pin to ground.
5	MODE	Normal operation or firmware update. (Default pin floating, no external connection)
6	VDD	Output pin of the VIN-to-VDD linear regulator. An MLCC (1μF) must be connected from this pin to ground.
7, 24	GND	Analog ground.
8, 11, 12, 13, 14, 15	PCIN	Negative peak-current signal input pin and input current path.
9	PCIP	Positive peak-current signal input pin.
10	VIN	Input voltage for the IC.
16, 17, 23	PHASE	PHASE is the switching node that supplies power to output. Connect the inductor to the PHASE pin.
18, 19, 20	PGND	Power GND.

Pin No.	Pin Name	Pin Function
21	PVDD	Bias voltage (5V typ.) supply for the low-side gate drivers. An MLCC (1μF) must be connected from this pin to ground.
22	BOOT	Bootstrap capacitor connection node. An MLCC (0.1μF) must be connected from this pin and PHASE pin to power the internal high-side gate driver.
25	BLD	A built-in programmable current bleeder to discharge the output capacitor of the PWM converter. Connect this pin to the converter output.
26	CSOP	Positive input of a current-sense amplifier to sense the output current for constant current regulation and also through an ADC to the MCU. Connect this pin to the positive terminal of output current-sense resistor via an RC filter.
27	CSON	Negative input of a current-sense amplifier for output constant-current regulation and output current detection. Connect this pin to the negative terminal of output current-sense resistor via an RC filter.
28	VO	Input of feedback voltage from converter output. The voltage is monitored for output undervoltage protection.
29	GP	Charge-pump gate diver output. It can driver external N-channel MOSFETs to turn on/off the output power path.
30	VBUS	USB-C VBUS voltage input. The voltage at this pin is monitored for USB-C VBUS overvoltage protection with an 8-bit programmable threshold voltage.
31	CC1	Type-C connector Configuration Channel (CC) 1. Generally, this input/output pin is connected to USB Type-C connector CC1 terminal.
32	CC2	Type-C connector Configuration Channel (CC) 2. Generally, this input/output pin is connected to USB Type-C connector CC2 terminal.
33	CCGND	Analog ground.
34	DP	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. This pin can be set as an open-drain or push-pull GPIO pin. Connect this pin to the DP pin of a USB connector.
35	DM	Input/Output pin of built-in DPDM interface for BC1.2 and proprietary protocols. This pin can be set as an open-drain or push-pull GPIO pin. Connect this pin to the DM pin of a USB connector.
36, 37	NC	No connection.
38	SCK1	Open-drain clock signal input/output pin of the Slave/Master I^2C Interface. This pin can be set as an open-drain or push-pull GPIO pin.
39	SDA1	Open-drain data signal input/output pin of the Slave/Master I^2C Interface. This pin can be set as an open-drain or push-pull GPIO pin.
40	RT1	Open-drain/push-pull GPIO, analog input or external over-temperature protection (EOTP) input pin. Connect an NTC from this pin to GND pin for the EOTP.
41 (Exposed Pad)	PHASE	PHASE is the switching node that supplies power to output. Connect the inductor to the PHASE pin.
42 (Exposed Pad)	PCIN	Negative peak-current signal input pin and input current path.
43 (Exposed Pad)	GND	Analog ground.

10 Functional Block Diagram



11 Absolute Maximum Ratings

(Note 2)

- V2 to GND ---------- –0.3V to 2.5V
- VDD, PVDD to GND ---------- –0.3V to 6.5V
- VBUS, CSOP, CSON, VO, BLD to GND ---------- –0.3V to 25V
- CSOP to CSON Voltage ($V_{CSOP-CSON}$) ---------- –5V to 5V
- BLD to CSOP Voltage ($V_{BLD-CSOP}$) ---------- –0.3V to 6.5V
- BLD to CSON Voltage ($V_{BLD-CSON}$) ---------- –0.3V to 6.5V
- GP to GND ---------- –0.3V to 33V
- VIN, PCIN, PCIP to GND (DC) ---------- –0.3V to 32V
  (<0.4s) ---------- –0.3V to 36V
- VIN to PCIP Voltage ($V_{VIN-VPCIP}$) ---------- –0.3V to 6.5V
- VIN to PCIN Voltage ($V_{VIN-VPCIN}$) ---------- –0.3V to 6.5V
- PCIP to PCIN Voltage ($V_{PCIP-PCIN}$) ---------- –5V to 5V
- I^2C Pins (SCK1, SDA1, SCK2, SDA2) to GND ---------- –0.3V to 6.5V
- GPIO Pins (RT1, SYN, MODE) to GND ---------- –0.3V to 6.5V
- DP, DM to GND ---------- –0.3V to 24V
- CC1, CC2 to GND ---------- –0.3V to 24V
- BOOT to PHASE ($V_{BOOT-PHASE}$) ---------- –0.3V to 6.5V
- PHASE to GND (DC) ---------- –0.3V to 30V
  (<20ns) ---------- –5V to 36V
- PGND, CCGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-42L 6x6 ---------- 2.46W
- Package Thermal Resistance (Note 3)
  WQFN-42L 6x6, θ_{JA} ---------- 50.67°C/W
  WQFN-42L 6x6, θ_{JC} ---------- 2.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- PWM Converter Input Voltage, V_{IN} ---------- 4.5V to 30V
- PWM Converter Output Voltage, V_{OUT} ---------- 3V to 21V
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C
- Minimum MTP Memory Write/Erase Cycles ---------- 100cycles at 25°C

Note 5. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(V_{IN} = 12V, V_{DD} = V_{PVDD} = 5V, T_A = T_J = –40°C to 125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD and V2 Linear Regulators (VDD LDO and V2 LDO), Undervoltage Lockout (UVLO) and MODE Control						
VDD Output Voltage (5.0V Normal/4.3V DGM)	V_{REG_VDD}	In normal mode, V_{IN} = 12V, I_{OUT} = 0mA, CVDD = 1μF	4.7	5	5.3	V
		In deep-green mode, V_{IN} = 12V, I_{OUT} = 0mA, CVDD = 1μF	3.9	4.2	4.5	
VDD Load Regulation Drop Voltage (5.0V Normal)	V_{DROP_VDD12}	V_{IN} = 12V, I_{OUT} = 80mA, CVDD = 1μF	--	0.3	--	V
	V_{DROP_VDD5}	V_{IN} = 5V, I_{OUT} = 80mA, CVDD= 1μF	--	0.3	--	V
VDD Short Current	I_{SC_VIN}	V_{IN} = 12V, VDD short to GND	--	70	--	mA
VIN Normal Operating Current	I_{OP_VIN}		--	10	--	mA
VIN Operating Current in Deep Green-Mode (DGM_LQ)	I_{DGM_VIN}		--	120	--	μA
VIN Operating Current in VDD Shutdown Mode	I_{RST_VIN}	V_{IN} = 12V, PWM = MCU = off, digital output pins = open	--	10	50	μA
V2 Output Voltage	V_{REGV2}	In normal mode I_{V2} = 20mA load, C_{V2} = 1μF	1.62	1.8	1.98	V
V2 Short-Circuit Current	I_{SC_V2}	V_{IN} = 12V, V_{DD} = 5V V2 short to GND	--	50	--	mA
VDD POR Voltage Threshold		V_{DD} rising	3.8	4	4.2	V
VDD UVLO Voltage Hysteresis		V_{DD} falling	--	0.225	--	V
PVDD POR Threshold			3.8	4	4.2	V
PVDD UVLO Hysteresis			--	0.2	--	V
PVDD Input Current in PWM Shutdown			--	--	3	μA
MODE Threshold Voltage			1.5	--	VDD	V
			0	--	0.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller – Programmable Oscillator and Maximum On-Time						
PWM Frequency Range		Programmable	200	--	600	kHz
PWM Frequency Accuracy	f_{PWM}		–10	--	10	%
MCU Section						
MCU Clock Frequency	f_{MCU}		19.4	21.6	23.8	MHz
OSC 80k Frequency in Deep Green-Mode	f_{80K}		72	80	88	kHz
PWM Controller – Constant-Voltage (CV) Control Loop						
CV Regulated Voltage Range at the VO Pin	V_{REG_VO}	Programmable (11-bit), 9.93mV/step	3	--	21	V
CV Regulated Voltage Accuracy at the VO Pin (CVDAC_11bit)		V_{IN} = 12V, V_{OUT} = 5V/9V	–120	--	120	mV
		V_{IN} = 24V, V_{OUT} = 20V	–200	--	200	
PWM Controller – Constant-Current (CC) Control Loop and Output						
CSON and CSOP Operating Voltage Range		CC Programmable (10-bit), CSA_gain = 40	3	--	21	V
CC Regulated Voltage Range between the CSOP and CSON Pins (CCDAC_10bit)	V_{REF_CC}	CSAgain = 40, Rsense = 5mΩ, CC_step = 12.5mA, CC_max = 7A	5	--	35	mV
CC Regulated Voltage Accuracy between the CSOP and CSON Pins		CSAgain = 40, Rsense = 5mΩ, nominal V_{REF_CC} = 5mV/15mV/25mV	–1	--	1	mV
CSOP/CSON Input Current		PWM bias = on	--	--	50	µA
		PWM bias = off	--	--	1	
PWM Controller – Input Current Comparison and Slope Compensation						
Maximum Input Overcurrent (INOC) Voltage Threshold Range	V_{TH_CSMAX}		30	--	150	mV
Maximum Input Overcurrent (INOC) Voltage Threshold Accuracy		V_{TH_CSMAX} = 70mV	–8	--	8	mV
		V_{TH_CSMAX} = 120mV	–10	--	10	
Voltage Rate Range of Slope Compensation			0	--	80	mV/µs
PCIP Input Current		In PSM, V_{IN} = V_{PCIP} = 24V	--	--	50	µA
		PWM bias = off, V_{IN} = V_{PCIP} = 24V	--	--	3	
PCIN Input Current		In PSM, V_{IN} = V_{PCIP} = 24V	--	--	30	µA
		PWM bias = off, V_{IN} = V_{PCIP} = 24V	--	--	3	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller – Zero-Current Detection (ZCD) and Gate Drivers						
MOS-B ZCD Voltage Threshold between PGND and PHASE Pins	V_{TH_ZCDB}		--	4	--	mV
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$	PVDD = 5V, BOOT = 5V, PHASE = 0, IDS = 1A, PCIN-to-PHASE	--	25	--	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$	PVDD = 5V, PGND = 0, IDS = 1A, PHASE-to-PGND	--	25	--	mΩ
Dead-Time at UGATE Falling Edge			--	40	--	ns
Dead-Time after LGATE Falling Edge			--	40	--	ns
System Protections – Overvoltage, Undervoltage, and Overcurrent Protections (OVP, UVP, and OCP)						
VIN UVP Voltage Threshold Range	V_{TH_VINUV}	Programmable	4	--	27	V
VIN UVP Voltage Threshold Accuracy			–5	--	5	%
VIN OVP Voltage Threshold Range	V_{TH_VINOV}	Programmable	4	--	27	V
VIN OVP Voltage Threshold Accuracy			–5	--	5	%
VBUS OVP Voltage Threshold Range	V_{TH_VBUSOV}	Programmable	3.3	--	24	V
VBUS OVP Voltage Threshold Accuracy		Setting of $V_{TH\_VBUSOVP}$ = 12V	–5	--	5	%
		Setting of $V_{TH\_VBUSOVP}$ = 5V	–0.3	--	0.3	V
BLD OVP Voltage Threshold	V_{TH_BLDOV}		115	120	125	%
VO UVP Voltage Threshold Range	V_{TH_VOUV}	Programmable	3	--	20	V
VO UVP Voltage Threshold Accuracy		VO_UVP = 5V to 20V	–5	--	5	%
		VO_UVP = 3V	–0.2	--	0.2	V
USB PD Controller – CC1/2 Voltage Detections and BMC Transmitter/Receiver						
CC1/2 Pull-Up Current Source – 1			64	80	96	µA
CC1/2 Pull-Up Current Source – 2			165.6	180	194.4	µA
CC1/2 Pull-Up Current Source – 3			303.6	330	356.4	µA
Transmitter High-Level Output Voltage Range			1.05	1.125	1.2	V
Transmitter Low-Level Output Voltage Range			0	--	75	mV
Rising Time of the Transmitter Output Voltage			300	--	--	ns

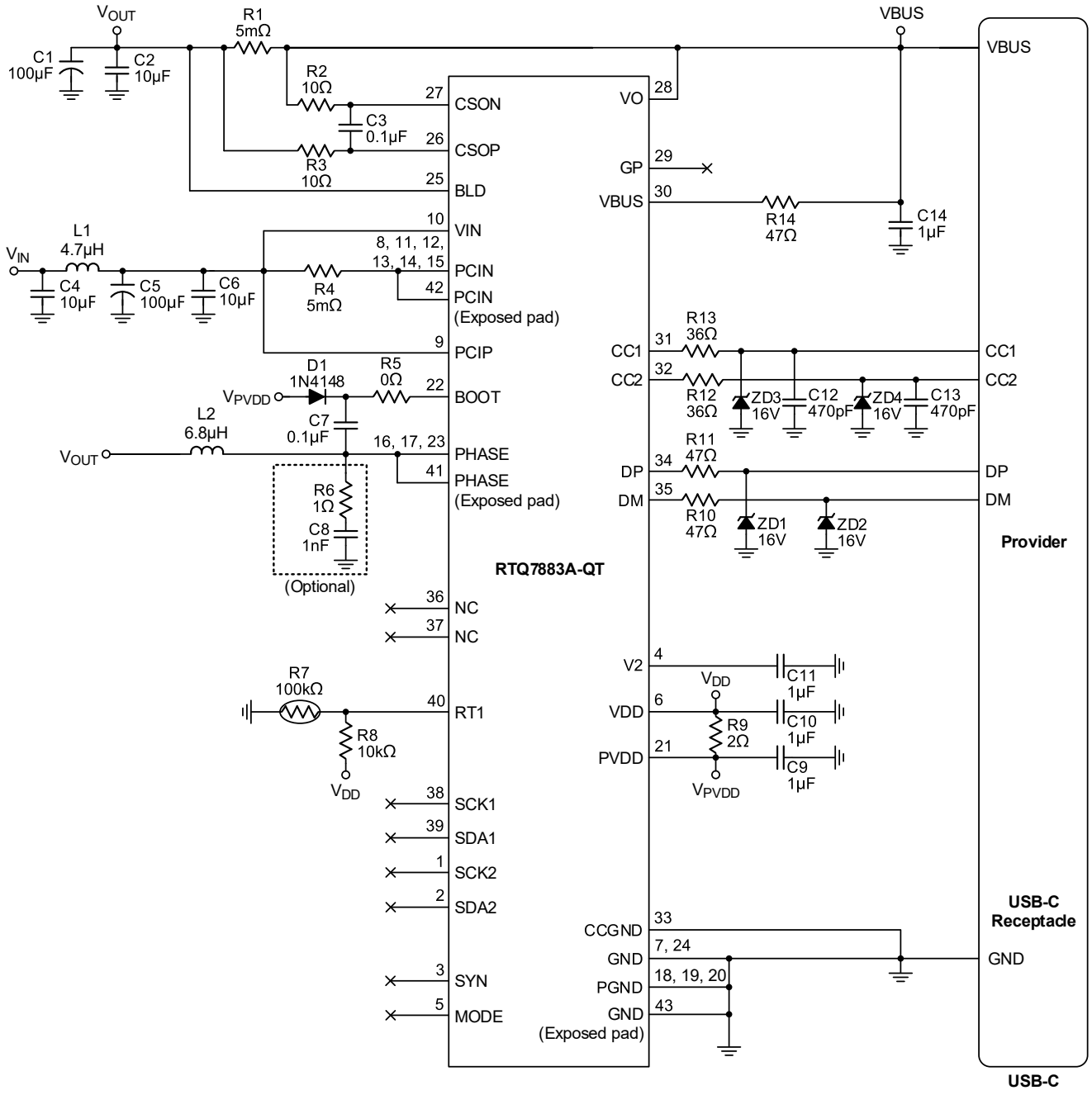
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Falling Time of the Transmitter Output Voltage			300	--	--	ns
Receiver High-Level Input Voltage Range			--	0.8	--	V
			--	0.7	--	
			--	0.6	--	
			--	0.5	--	
Receiver Low-Level Input Voltage Range			--	0.5	--	V
			--	0.4	--	
			--	0.3	--	
			--	0.2	--	
CC1/CC2 Short to VBUS Protection			5.415	5.7	5.985	V
DPDM Interfaces in Source Role Operation						
On-Resistance of DP-to-DM MOSFET			--	40	80	Ω
DP/DM High-Level Output Voltage	V_{OH_DPDM}	Sourcing current = 2mA	--	3.3	--	V
			--	1.8	--	
DP/DM Low-Level Output Voltage	V_{OL_DPDM}	Sinking current = 2mA	--	--	0.3	V
DP/DM Voltage Falling Threshold for Plug-Out Detection	V_{REF1_DPDM}		--	0.3	--	V
			--	0.4	--	
			--	0.5	--	
			--	0.6	--	
Input Voltage Offset Selection VREF2H_DPDM, VREF2L_DPDM	V_{IN_LEV}		--	0	--	V
			--	0.4	--	
RX Upper Input Voltage Threshold	V_{REF2H_DPDM}	V_{IN_LEV} = 0V	--	0.8	--	V
			--	1.3	--	
			--	1.9	--	
			--	2.05	--	
		V_{IN_LEV} = 0.4V	--	1.2	--	
			--	1.7	--	
			--	2.3	--	
			--	2.45	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RX Lower Input Voltage Threshold	V_{REF2L_DPDM}	V_{IN_LEV} = 0V	--	0.6	--	V
			--	1.1	--	
			--	1.8	--	
			--	1.95	--	
		V_{IN_LEV} = 0.4V	--	1	--	
			--	1.5	--	
			--	2.2	--	
			--	2.35	--	
DP/DM Internal Pull-High Resistance	R_{UP_DPDM}		7.5	10	12.5	kΩ
DP/DM Internal Pull-Low Resistance	R_{DWN_DPDM}		16	20	24	kΩ
DP/DM Output Voltage for Divider Mode			–6%	1.2	6%	V
			–6%	2	6%	
			–5%	2.7	5%	
			–5%	3.3	5%	
Output Resistance DP/DM for Divider Mode 2.0/2.7/3.3			--	30	--	kΩ
Output Resistance DP/DM for Divider Mode 1.2			--	100	--	kΩ
DP/DM Output Voltage-1 for SRC	V_{SRC1_DPDM}	Programmable for QC application, 0.6V only	--	0.6	--	V
DP/DM Output Voltage-2 for SRC	V_{SRC2_DPDM}	Programmable for QC application, 3.3V only	--	3.3	--	V
DP/DM Short to VBUS Protection			5.415	5.7	5.985	V
DM CDP Output Voltage			0.5	--	0.7	V
DP Sink Current			50	--	150	μA
Charge-Pump Gate Drivers and Bleeders						
GP On-Resistance of Pull-Low MOSFET			--	--	200	Ω
BLD Discharge Current	I_{BLD_DIS}	Programmable	15	30	45	mA
			30	60	90	
			45	90	135	
			60	120	180	
VBUS Bleeder Resistor			--	1.2	--	kΩ
GP Maximum GP Voltage			V_{VO} + V_{DD}	V_{VO}+ 2xV_{DD} – 3V	V_{VO}+ 2xV_{DD} – 1V	V

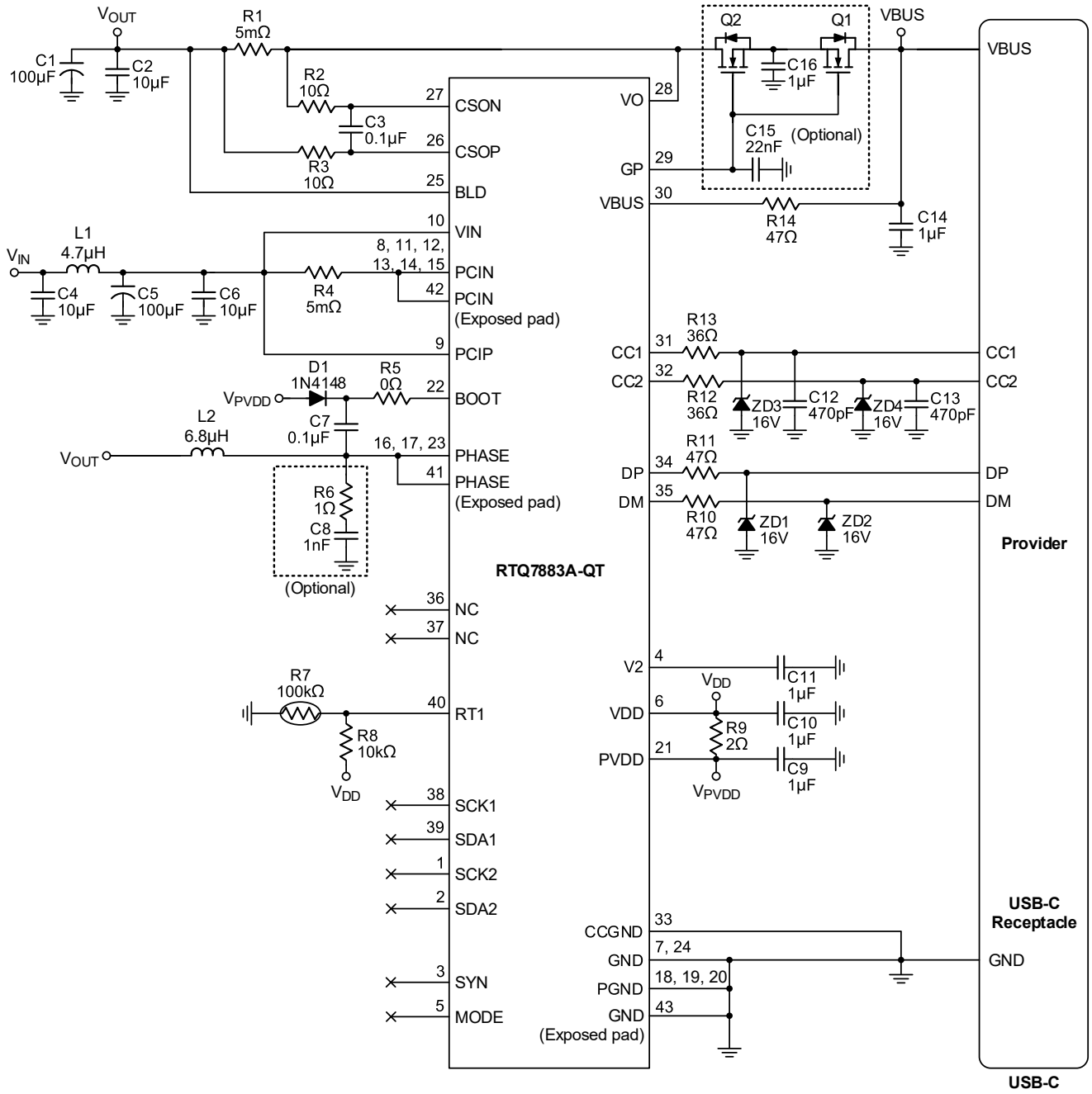
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Input and Output – I^2C Pins (SCK1, SDA1, SCK2, and SDA2) and GPIO Pins (RT1 and SYN)						
I^2C/GPIO High-Level Input Voltage Range	V_{IH}		1.5	--	VDD	V
I^2C/GPIO Low-Level Input Voltage Range	V_{IL}		0	--	0.4	V
I^2C/GPIO High-Level Output Voltage	V_{OH}		VDD – 1.5V	VDD – 0.8V	--	V
I^2C/GPIO Low-Level Output Voltage	V_{OL}		--	--	0.3	V
I^2C/GPIO Leakage Current			--	--	1	μA
RT1 Current Source		V_{RT1} < 2.7V	92	100	108	μA

14 Typical Application Circuit

14.1 Typical Application Circuit



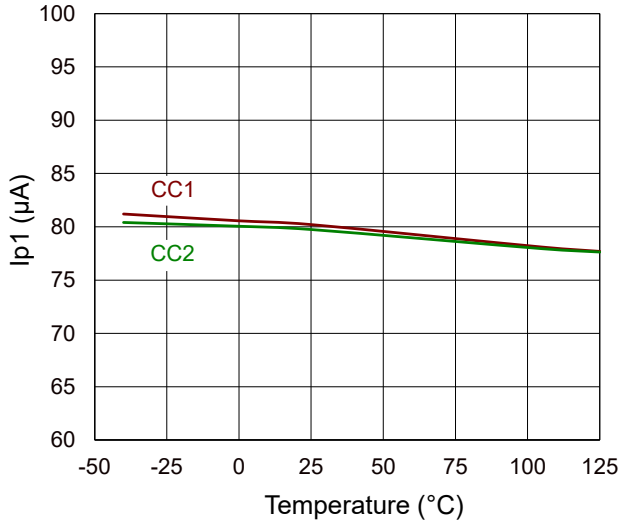
14.2 Typical Application Circuit with VBUS Blocking MOSFET



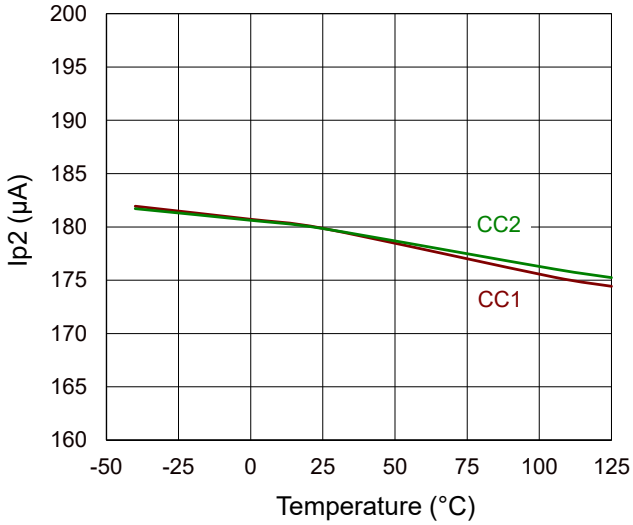
VBUS Blocking MOSFET		
Q2	**Q1**	**Note**
Y	Y	The safest V_{BUS} protection circuit.
Y	N	Prevent current from V_{IN} to V_{BUS}.
N	Y	Prevent current from V_{BUS} to V_{IN}.
N	N	V_{BUS} does not have any protection circuit.

15 Typical Operating Characteristics

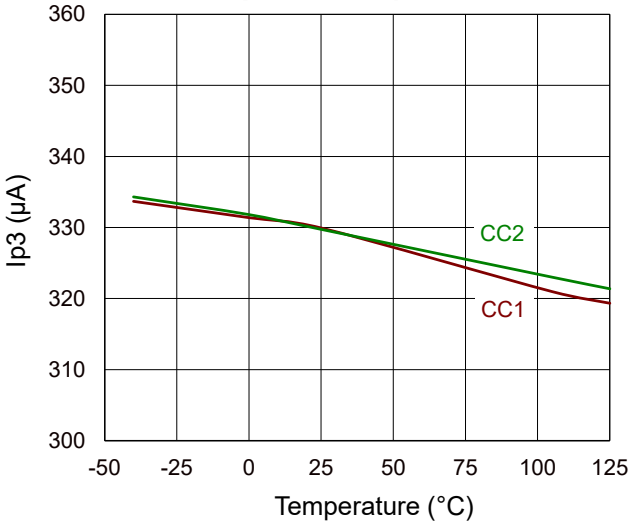
Ip1 vs. Temperature



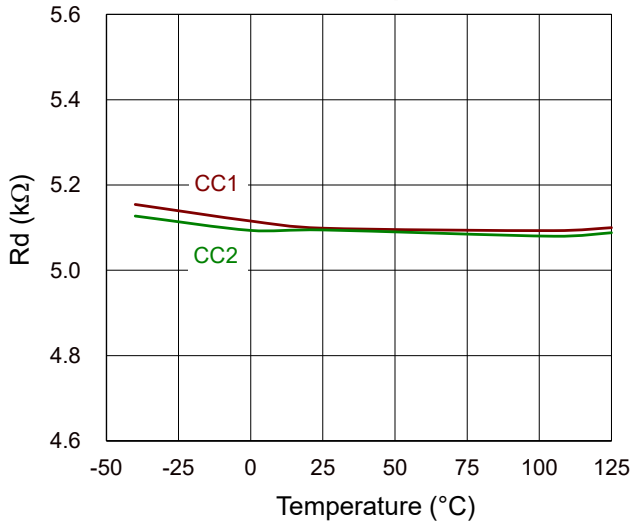
Ip2 vs. Temperature



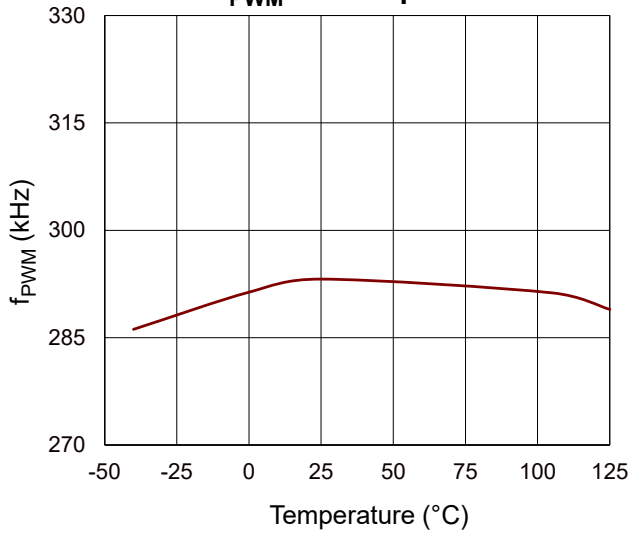
Ip3 vs. Temperature



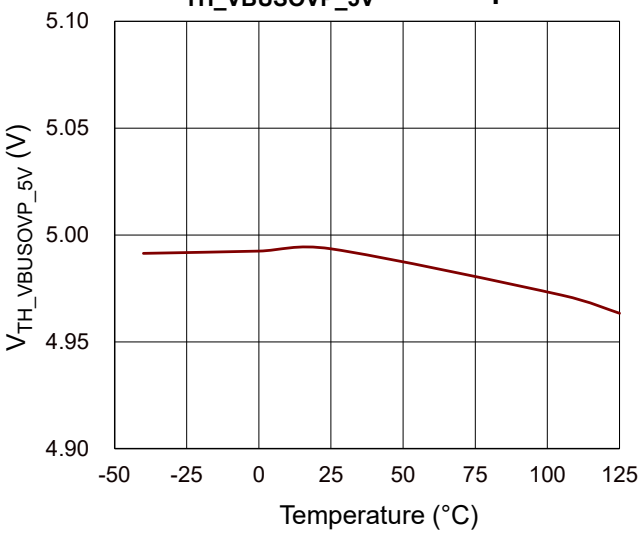
Rd vs. Temperature

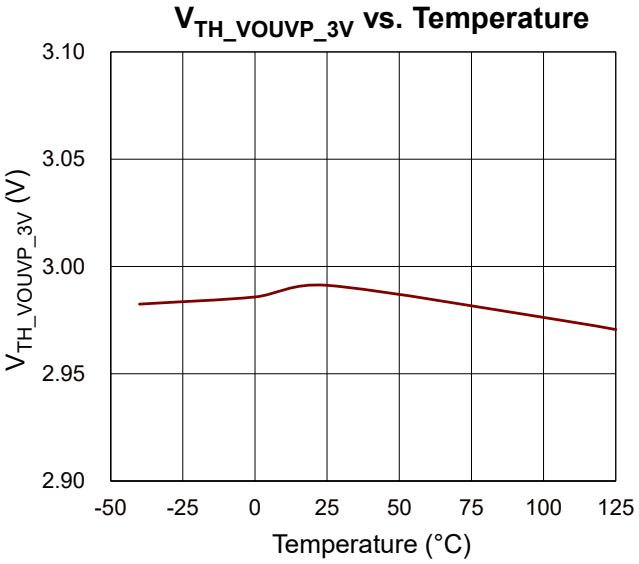


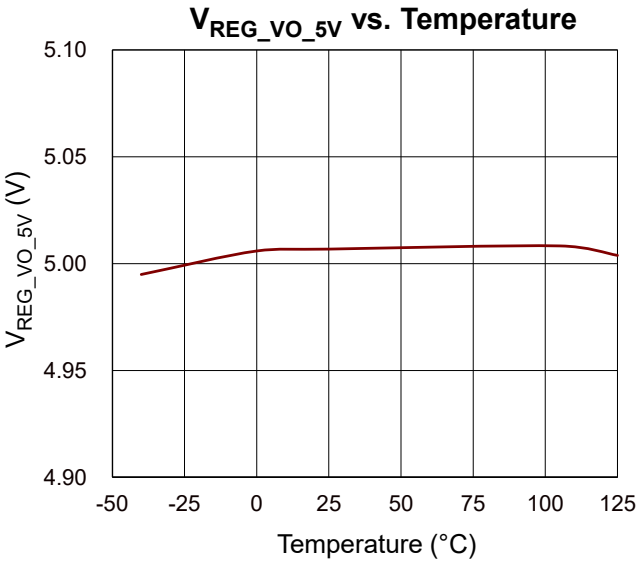
f_{PWM} vs. Temperature

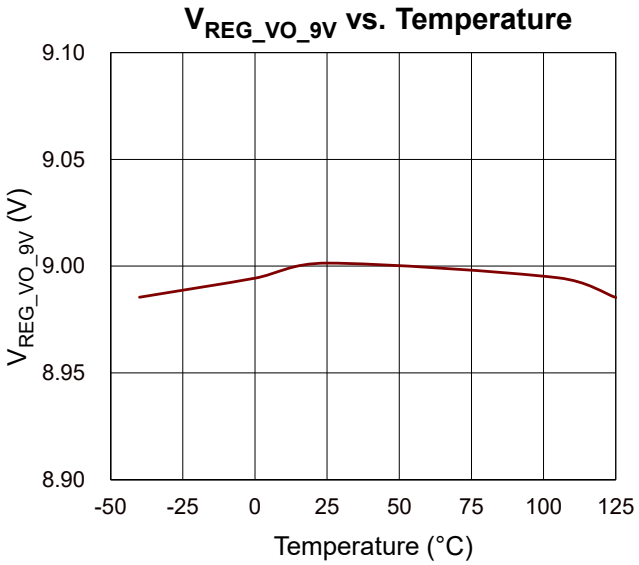


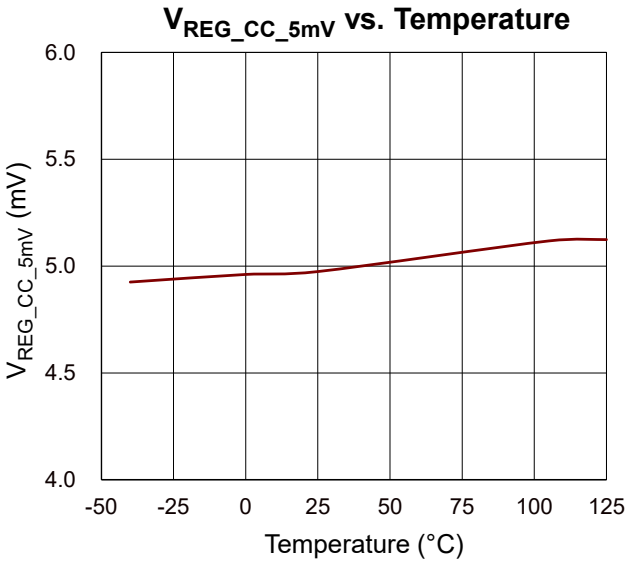
$V_{TH\_VBUSOVP\_5V}$ vs. Temperature

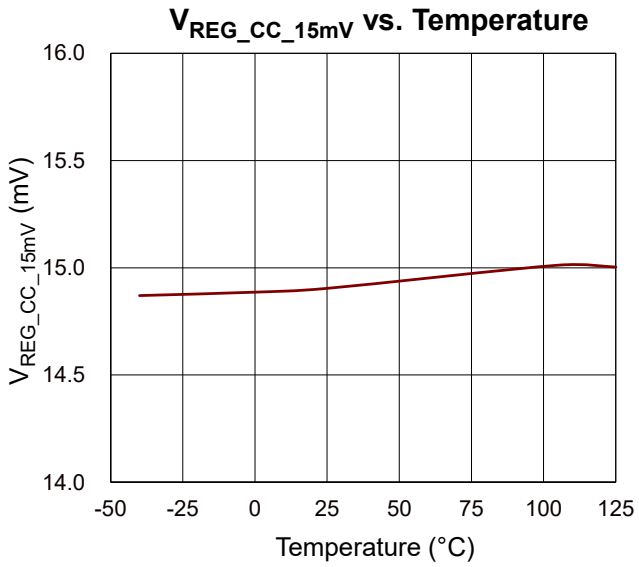












16 Operation

The RTQ7883A-QT is a versatile USB Type-C Power Delivery (USB-C PD) and PWM Buck converter designed especially for applications as providers. It is a highly integrated solution with the following main functional blocks: MCU System, PWM Buck Controller, Protections and CC1/2 Functions as depicted in the “Functional Block Diagram”.

The MCU System embeds an ARM Cortex-M0 MCU, a multi-time programming (MTP) memory, a ROM, an SRAM, a 10-bit ADC (analog to digital converter), two I^2C interfaces (slave and master) and GPIO (general purpose input or output) pins. The MCU System is programmed to perform power controls, customized functions, as a policy engine and a device policy manager. This MCU reports the operating status of PD operation, such as present input/output voltage, output current and external temperature to an EC (embedded controller) or AP (application processor) and receives commands from the EC/AP, as a system policy manager, via the slave I^2C interface. The GPIO pins can be used to control high-speed multiplexers or other customized functions.

The “PWM Buck controller” consists of an AnyVolt constant-voltage (CV) control circuit (9.93mV/step, typ.), an AnyCurrent constant-current (CC) control circuit, an output current-sense amplifier (7.8mA to 12.5mA/step, depending on the current-sense resistor), built-in gate drivers, one charge-pump gate driver and output bleeders (at the BLD and VBUS pins). Generally, either the CV or the CC control circuit regulates the output voltage or current through peak-current mode PWM operation. Diode emulation function and pulse-skipping mode (PSM) are built in to improve power efficiency at light loads. The output current-sense amplifier (OCS-AMP) allows current-sense resistors as low as 5mΩ to 15mΩ for reducing power loss. Moreover, the charge-pump driver adopts N-channel MOSFETs for on/off control of output power-path, instead of P-channel MOSFETs having higher cost. In operation the output bleeders at BLD and VBUS pins can be turned on to discharge output voltage (VBUS) during the VBUS negative transition, in the hard reset process, or after the removal of the USB-C connector.

The PD Safe power delivery operation consists of overvoltage protection (OVP) at the VBUS pin, undervoltage protection at the VO pin and output CC regulation. With the PD Safe feature, trip levels of the OVP and UVP can be set dynamically for each output voltage target. The CC regulation level is also adaptively programmed according to the current level in full load.

The “CC1/2 Functions” block consists of the physical layer, three selectable levels of the pull-up current sources Ip (instead of resistors Rp), a controllable pull-down resistor Rd.

16.1 Undervoltage Lockout (UVLO)

The RTQ7883A-QT UVLO function continuously monitors bias voltages at the VDD and V2 pins. When both of the supply voltages (V_{DD} and V_{V2}) rise above the respective rising UVLO thresholds, the internal UVLO signals will go low to activate the MCU. In addition, the IC also monitors the bias voltage at the PVDD pin for UVLO function. Only when all of the UVLO signals go low, or the PWM Buck controller will not be activated; meanwhile the MCU or PWM controllers will be kept in the “Undervoltage Lockout” state to prevent any undesirable operation.

16.2 Pulse-Skipping Mode (PSM)

When a switch-mode converter operates in light load condition, most power loss is caused by switching losses. To reduce switching loss in light load condition, the switching frequency needs to be reduced by entering the pulse-skipping mode (PSM) and the discontinuous conduction mode (DCM). In this operation, an internal compensation voltage V_{COMP} is compared by a PSM comparator, which has a programmable PSM threshold.

When the internal compensation voltage V_{COMP} is above the PSM threshold, the converter works in normal fixed-frequency PWM mode. As long as the V_{COMP} drops below the PSM threshold, the converter will enter the pulse-skipping mode to reduce switching frequency and thus diminish switching losses. The PSM threshold also defines

the minimum inductor peak current in PSM operation. Setting a larger PSM threshold will give a higher minimum peak current which in turn gives a lower switching frequency at light load for better light load efficiency at the cost of increased output voltage ripple. Conversely, a lower PSM threshold gives lower peak current and lower PSM ripple at the cost of worse light load efficiency.

16.3 Diode Emulation Mode

A Diode Emulation Mode (DEM) is also a necessary function to avoid delivering energy from converter output to converter input during dynamic output voltage control. The DEM function is equipped with zero-current detection (ZCD) circuits for low-side MOSFET. The Source-to-Drain voltage (V_{SDB}, detected via the PGND and PHASE pins) of the low-side MOSFET is compared with a zero-current threshold (V_{TH_ZCDB}). When the V_{SDB} drops below the V_{TH_ZCDB} voltage, the RTQ7883A-QT turns off the low-side MOSFET thereby avoiding reverse inductor current. In DEM operation, the behavior of the low-side MOSFET resembles a diode.

16.4 Cable Voltage Drop Compensation (CDC)

In a power delivery system with both a provider and a consumer, the provider with the RTQ7883A-QT AnyVolt feature can slightly adjust its CV output voltage to compensate voltage drop across the USB cable. A PD controller of the consumer can request higher VBUS voltage from the provider through PD communication to achieve an accurate application voltage.

There is another method to implement the CDC function without PD communication. The RTQ7883A-QT can use the ADC to detect the output current-sense voltage (V_{CSO}) between CSOP and CSON pins and adaptively add a proper output voltage offset (V_{CDC}) to compensate the cable voltage drop. The output voltage offset (V_{CDC}) is gradually added by adjusting the CV regulated output voltage (V_{REG_VO}) and is approximately proportional to the converter output current (I_{OUT}). V_{CDC} is approximately determined by the following equation:

$V_{CDC} = I_{OUT} \times R_{CABLE}$

where:

R_{CABLE} is a preset value of parasitic resistance of USB cable.

16.5 VBUS Overvoltage Protection (VBUS OVP)

In Figure 1, the VBUS OVP function is a hardware-based protection which monitors the voltage at the VBUS pin via a built-in resistor-divider. When the VBUS voltage exceeds its OVP threshold, the output of the OVP comparator goes high and starts the debounce time counting. At the end of the debounce time counting, the signal VBUS OVP goes high to turn off the PWM controller. The OVP trip voltage is programmable from 3.3V to 24V (8-bit, 100mV/step typ.) and its debounce time is also selectable to meet various application requirements.

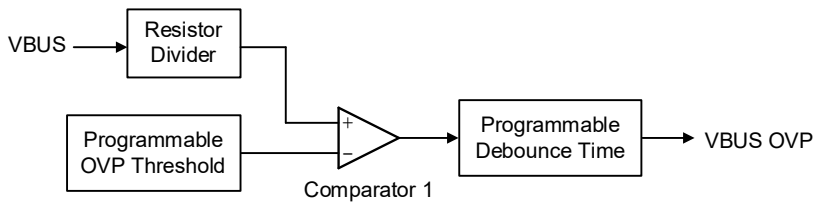


Figure 1. Functional Diagram of VBUS OVP

16.6 VO Undervoltage Protection (VO UVP)

In Figure 2, the VO UVP function is a hardware-based protection which monitors the voltage at the VO pin via a built-in resistor-divider. When the VO voltage falls below its UVP threshold, the output of the UVP comparator goes high and starts the debounce time counting. At end of the debounce time, the signal VO UVP goes high to turn off PWM controller. The UVP trip voltage is programmable from 3V to 20V (8-bit, 100mV/step typ.) and its debounce time is also selectable to avoid false triggering and to meet various application requirements.

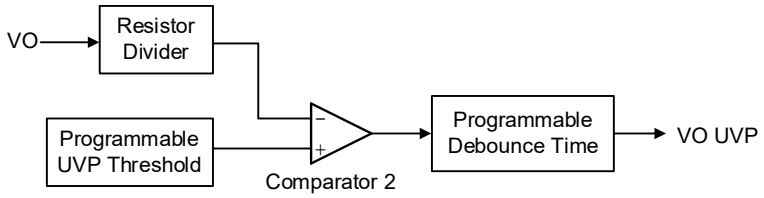


Figure 2. Functional Diagram of VO UVP

16.7 AnyCurrent Constant-Current (CC) Regulation

It is noted that a robust system is very important in USB PD operations, the AnyCurrent CC regulation allows setting the most suitable CC level for a negotiated PD system.

The RTQ7883A-QT integrates a current-sense amplifier to sense output current for CC regulation and also through an ADC to the MCU for the output current to be recorded. The amplifier accurately sense the current-sense voltage (i.e., VCS = output current x current-sense resistor) between the CSOP and CSON pins. The recommended current-sense voltage range for CC regulation is from 5mV to 35mV which is programmed by an internal 10-bit DAC (digital-to analog converter) with 0.0625mV/step resolution.

16.8 Power-Path Gate Driver for Driving N-Channel MOSFETs

The RTQ7883A-QT integrates a power-path gate driver to control external output blocking MOSFETs between the output of the PWM converter and the USB-C VBUS terminal. A built-in charge pump is included to supply the gate driver to turn on the external N-channel power MOSFETs, allowing for more cost-effective power systems compared to the P-channel counterparts.

16.9 Online Firmware Update via Slave I^2C or CC1/CC2 Interface

The embedded MTP memory allows the RTQ7883A-QT's firmware to be updated by an EC (Embedded Controller) or AP (Application Processor) through the I^2C slave interface. The RTQ7883A-QT provides some firmware-programmable design features, which greatly eases the design efforts during product development stage. End users are also allowed to update the firmware through CC1/CC2.

17 Application Information

(Note 6)

17.1 Calculating Output Discharge Time

Figure 3 shows the functional block diagram of two built-in output bleeders at the VBUS and BLD pins. The VBUS bleeder consists of an internal resistor (1.2kΩ typ.) and a pull low MOSFET (Q_{BLD_VBUS}) for discharging the capacitors at VBUS side. The BLD bleeder is a programmable BLD discharge current (I_{BLD_DIS}) for discharging the capacitors at the output of the PWM converter. If the blocking MOSFETs Q2 and Q1 are turn on during discharging, the BLD bleeder with larger current capability dominates the discharge time. If the blocking MOSFETs are turn off, the VBUS discharge time (t_{DIS_CVBUS}) and BLD discharge time (t_{DIS_COUT}) can be calculation with equation.

The VBUS discharge time (t_{DIS_CVBUS}) of the capacitor connected to the VBUS pin is determined by the following equation:

$$t_{DIS\_CVBUS} = R_{BLD\_INT} \times C_{VBUS} \times \ln\left(\frac{V_{BUS\_INI}}{V_{BUS\_FINAL}}\right)$$

where:

- R_{BLD_INT} is total internal resistance during on-state of the internal MOSFET QBLD_VBUS.
- C_{VBUS} is the total capacitance, coupled to the VBUS pin.
- V_{BUS_INI} is the initial bus voltage before the discharging.
- V_{BUS_FINAL} is the final bus voltage at end of the discharging.

The discharge time (t_{DIS_COUT}) of the capacitor connected to the output of the PWM converter is determined by the following equation:

$$t_{DIS\_COUT} = \frac{C_{OUT} \times (V_{OUT\_INI} - V_{OUT\_FINAL})}{I_{BLD}}$$

where:

- I_{BLD} is the internal discharge current.
- C_{OUT} is the total capacitance connected to the output of the PWM converter.
- V_{OUT_INI} is the initial voltage of the PWM converter output before discharging.
- V_{OUT_FINAL} is the final voltage of the PWM converter output at end of discharging.

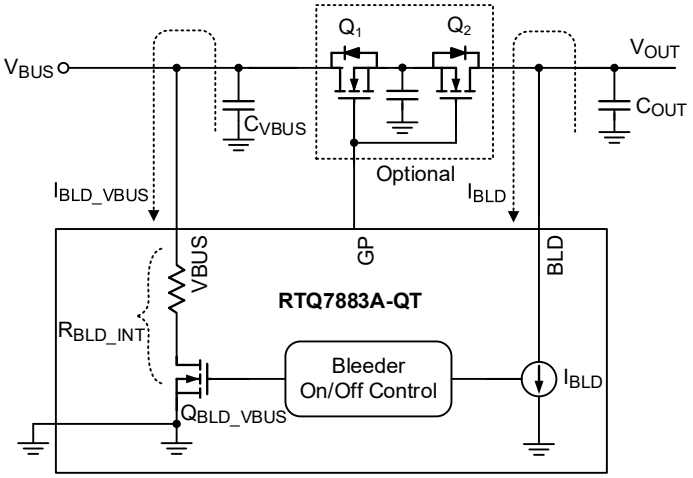


Figure 3. Functional Diagram of the Output Bleeders

17.2 Using Charge-Pump Gate Driver for Power-Path On/Off Control

Figure 4 shows the application schematic of a power-path on/off control. In this schematic, two N-channel MOSFETs of low on-resistance driven by a built-in gate driver, supplied by the charge pump, are employed to turn on or off the power-path between the PWM converter output and the USB-C VBUS terminal. If the internal control signal “ON” goes high, the GP voltage (V_{GP}) will be pulled high to turn on the power MOSFETs (Q_2 and Q_1) and connect the power-path. If “ON” goes low, V_{GP} will be pulled low by a built-in MOSFET to disconnect the power-path.

Power input (VO) is needed for the charge pump, and the VO pin must be connected the PWM converter output to ensure the power MOSFETs can be turned on successfully.

An optional MLCC capacitor (C_{GP}) can be used to reduce the V_{GP} rising rate and surge current in the power-path as the power MOSFETs being switched on.

When the power MOSFETs being switched off, the parasitic inductor and capacitors on the power path may cause voltage ringing at the drain of the Q_2 or Q_1. An optional gate resistor (R_{GP}) can be added to reduce the falling rate of the power-path current and prevent voltage spikes and ringing. A 1μF MLCC capacitor (C_{MID}) between the source terminals to ground is necessary in order to prevent oscillation due to such dual-MOSFET connection.

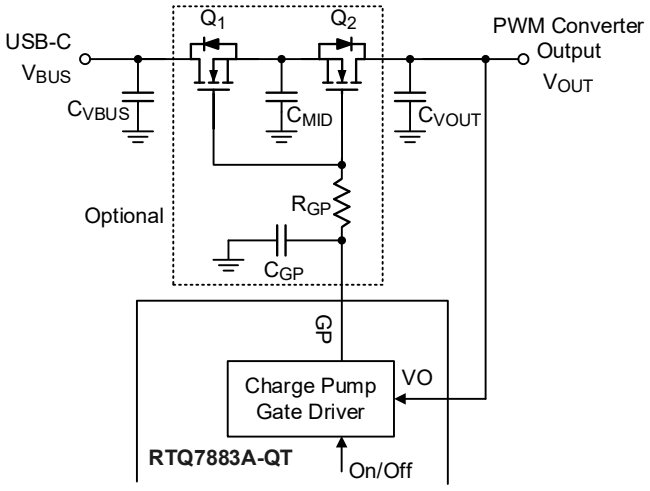


Figure 4. Functional Diagram of the Power-Path Control

17.3 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-42L 6x6 package, the thermal resistance, θ_{JA}, is 50.67°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C - 25°C) / (50.67°C/W) = 2.46W for a WQFN-42L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

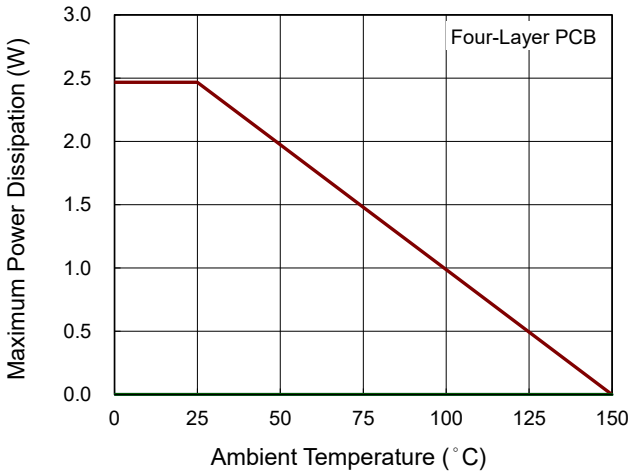


Figure 5. Derating Curve of Maximum Power Dissipation

17.4 Layout Considerations

- Connect the IC GND pin, CCGND pin, and the GND exposed pad to a ground plane (IC-ground), and then connect the IC-ground to the USB GND terminals via a low-impedance path.
- Connect the decoupling MLCCs near the pins of VDD, V2, and PVDD to GND via low impedance paths.
- Connect the boot strap MLCC from the BOOT pin to the PHASE pin via a short and low-impedance path.
- The paths of R_{CSOP} and R_{CSON} must be directly connected to the terminals of current-sense resistor (R_{CSO}) using Kelvin connections as shown in the layout shown in Figure 6.

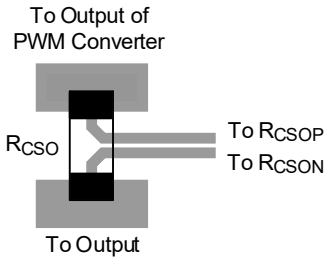


Figure 6. Kelvin Connections for the RCSO

- Figure 7 is a recommended power component placement of the PWM Buck power-stage. For better EMI performance, the power loop "CIN1 → RCSI → Internal Buck MOS → PGND to CIN1" must be as short as possible to minimize the switching noise. It is necessary to place several MLCCs (CIN1, 10 to 0.1μF/50V, X5R/X7R) close to RTQ7883A-QT to absorb high frequency switching EMI noise. For reducing the input and output voltage ripples during heavy load operation, it is recommended to add more MLCCs or solid capacitor for input and output capacitors. Moreover, the RTQ7883A-QT integrated buck power MOSFETs, it needs PCIN and PHASE PCB areas as heat sink for high-side and low-side MOSFETs heat dissipation.

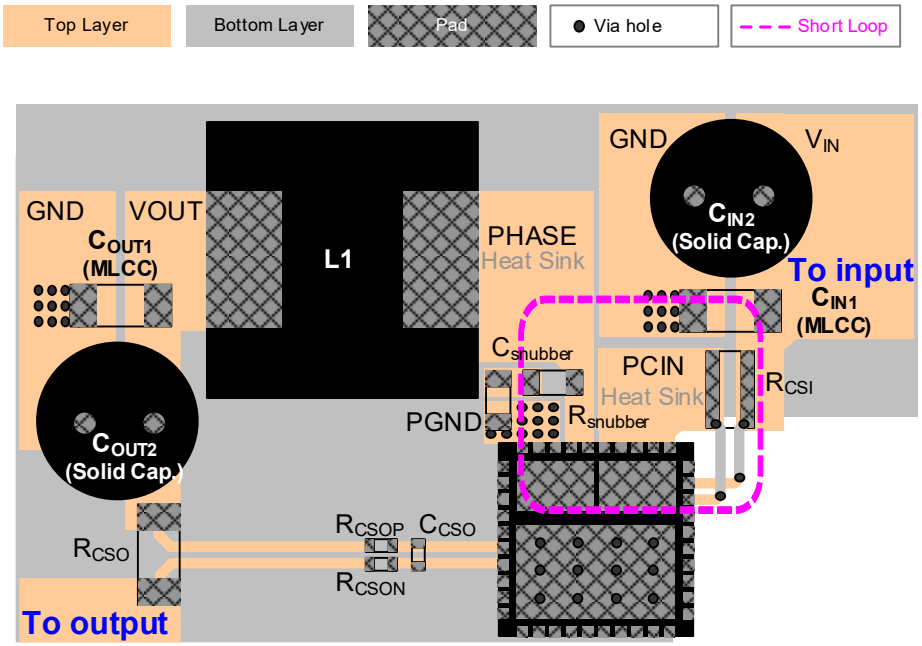


Figure 7. Recommended PCB Layout of the Power Stage

- To prevent the switching noises, keep the following signals far away from switching nodes PHASE pin:
  - Input and output current-sense signals
  - CC1 and CC2 signals
  - DP and DM signals
  - CV-loop and CC-loop feedback signals

- For improving ESD immunity, the Zener and MLCC of CC1/CC2 and DP/DM must place close to USB Type-C connector with low-impedance paths to GND.

17.5 Manual Firmware Update

During product development stage, users might need to download or update the RTQ7883A-QT firmware. This can be done by adding a 5-pin connector (CON1) or five test pads on PCBs for updating the RTQ7883A-QT firmware manually as shown in Figure 8. This connector is then connected to a “Firmware update fixture” by a 5-pin cable. The fixture is also connected to a PC via a Micro USB cable and acts as a bridge between the RTQ7883A-QT and the PC. With this setup, users can download firmware to the RTQ7883A-QT by using the RTQ7883A-QT graphic user interface (GUI) installed in the PC. During the firmware update process, the fixture can supply current (up to 40mA) to the RTQ7883A-QT and the system VIN via the 5V_OUT pin of the 5-pin cable. If the power from the fixture is enough to power the RTQ7883A-QT and the system VIN, it is not necessary to use the auxiliary input voltage for the system V_{IN}. On the other hand, if the system V_{IN} consumes more current than the fixture capability, one needs to use an auxiliary input voltage.

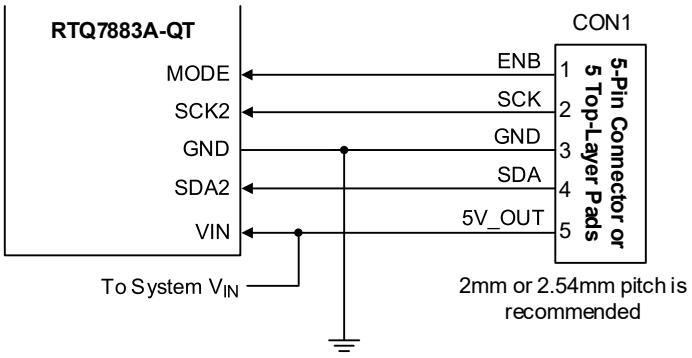
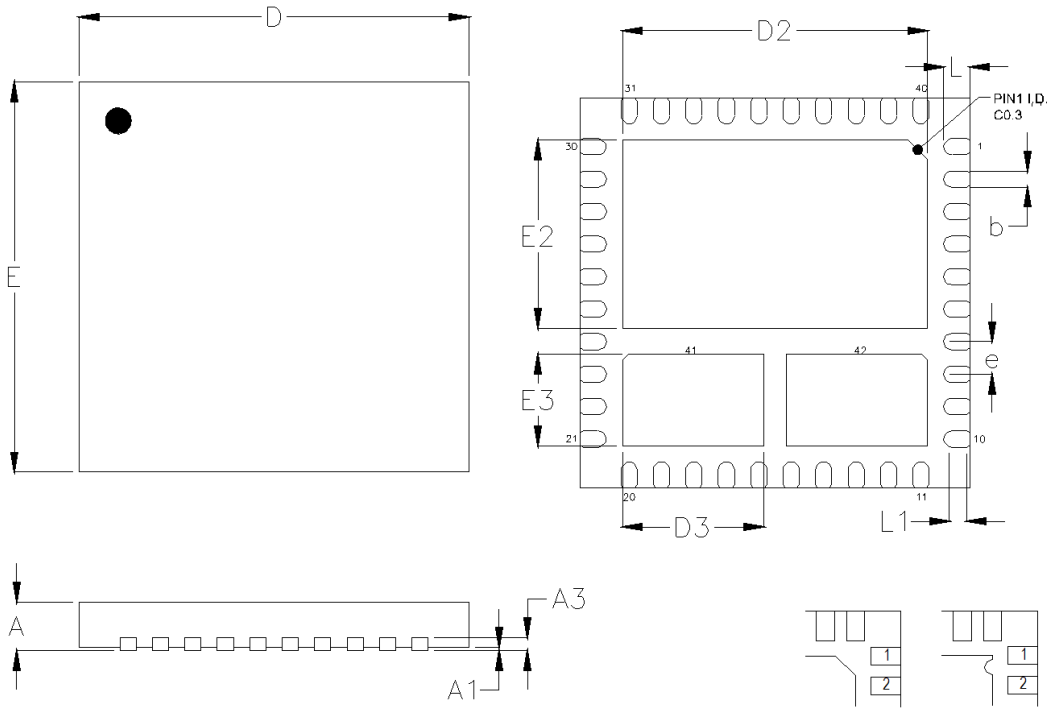


Figure 8. Connections for Manual Firmware Update

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek’s product and ensure such product meets applicable standards and any safety, security, or other requirements.

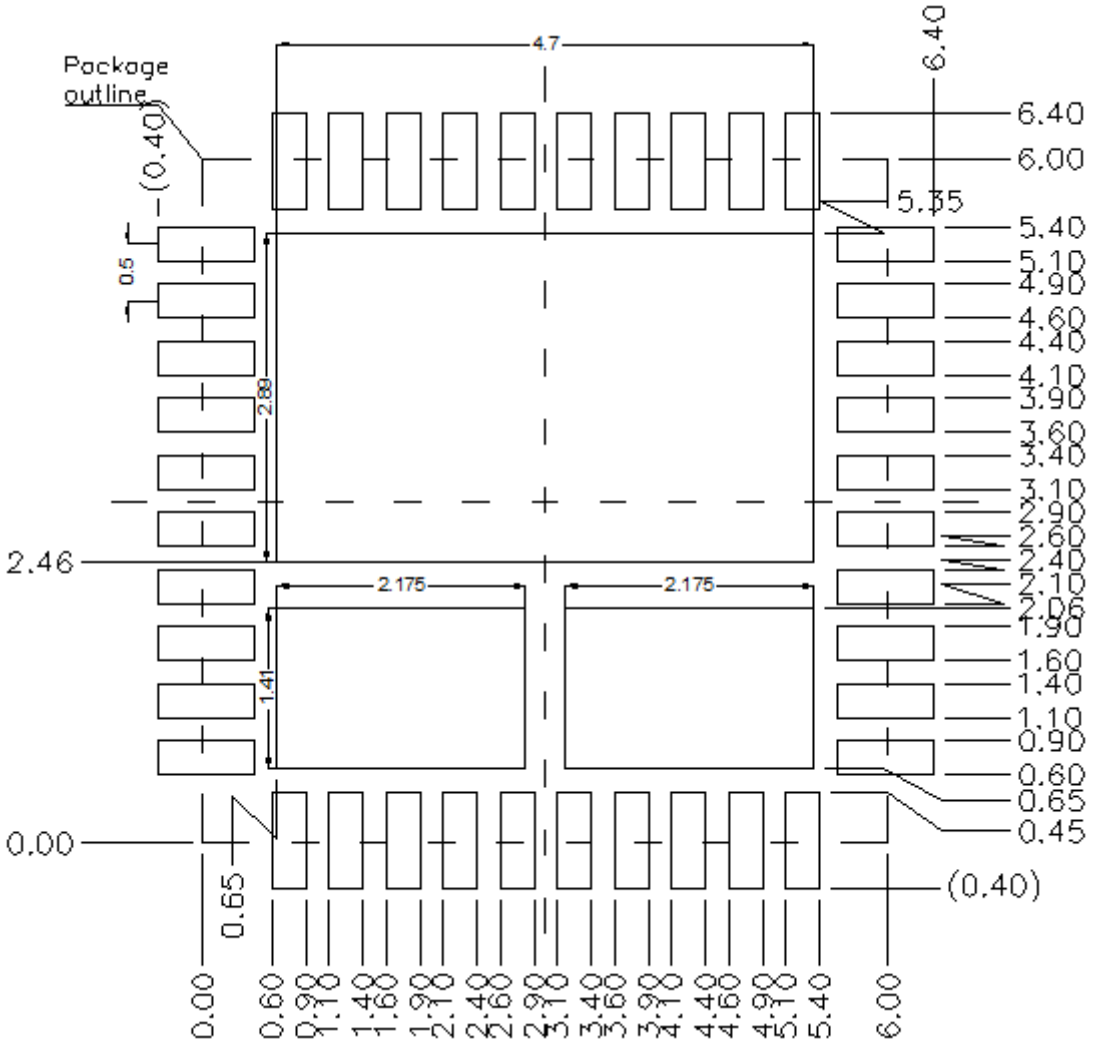
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	5.950	6.050	0.234	0.238
D2	4.650	4.750	0.183	0.187
D3	2.125	2.225	0.084	0.088
E	5.950	6.050	0.234	0.238
E2	2.840	2.940	0.112	0.116
E3	1.360	1.460	0.054	0.057
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.313		0.012	

W-Type 42L QFN 6x6 Package

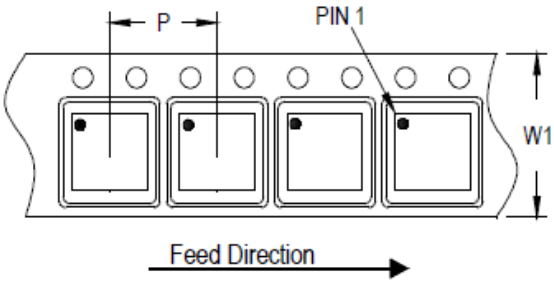
19 Footprint Information

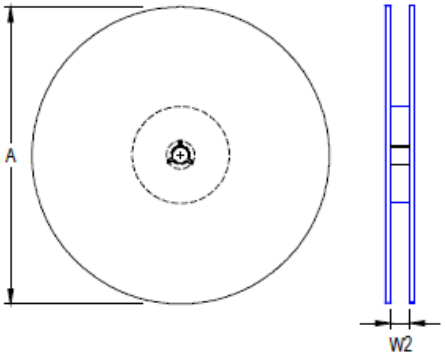


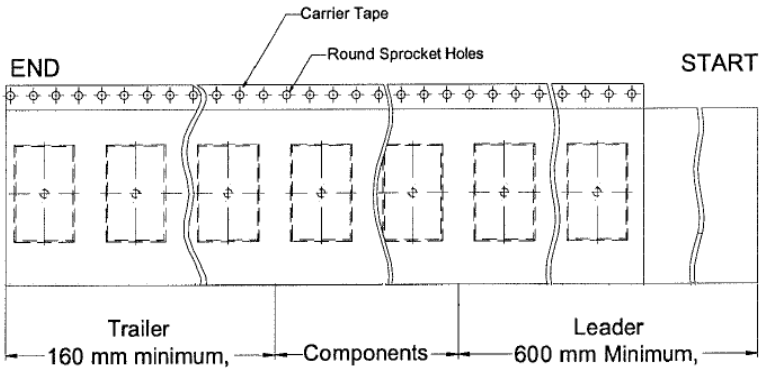
Package	Number of Pins	Tolerance
V/W/U/XQFN6x6-42	42	±0.05

20 Packing Information

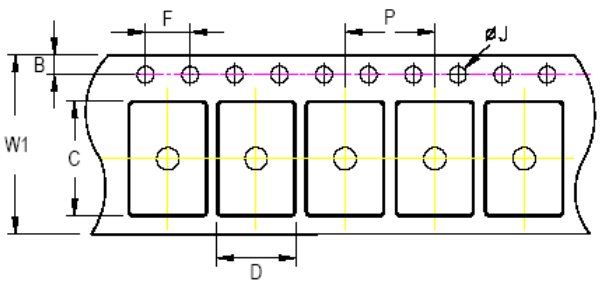
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 6x6	16	12	330	13	2,500	160	600	16.4/18.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 16mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
QFN and DFN 6x6	13”	2,500	Box G	1	2,500	Carton A	6	15,000

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

21 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/27	Final	General Description on P1 Features on P1, 2 Marking Information on P2 Simplified Functional Block Diagram on P2 Simplified Application Circuit on P2 Functional Pin Description on P4, 5 Functional Block Diagram on P6 Electrical Characteristics on P8 to 13 Typical Application Circuit on P14,15 Typical Operating Characteristics on P16, 17 Operation on P18, 19, 20 Application Information on P21 to 25
01	2025/11/24	Modify	*General Description on page 1* *Features on page 1* *Recommended Operating Conditions on page 8* *Electrical Characteristics on page 8* *Thermal Considerations on page 23* - Modified junction temperature range and ambient temperature range *Absolute Maximum Ratings on page 7* *Thermal Considerations on page 23* - Modified power dissipation *Packing Information on page 28* - Added tape size K