RICHTEK®

RTQ5756

3V to 5.5V, 4-Phase, Step-Down Converter with I²C Interface

1 General Description

The RTQ5756 series products are synchronous step-down converters with 4-phase capability, allowing for both multiphase and single-phase operations. These products offer a wide range of configuration options. The RTQ5756A provides triple outputs with 2+1+1 phase, while the RTQ5756B offers quad outputs with 1+1+1+1 phase. The RTQ5756C provides dual outputs with 3+1 phase, and the RTQ5756D offers a single output with 4-phase. Lastly, the RTQ5756E provides dual outputs with 2+2 phase. This flexibility and high integration make the RTQ5756 series suitable for various applications that require high current and compact power management solutions, such as low-power processors, I/O power, the core power of FPGA, DSP, and other ASICs. With an input voltage range of 3V to 5.5V, these converters are compatible with a wide variety of low voltage systems. They can deliver up to 20A peak current and support output voltages ranging from 0.4V to 1.55V.

The RTQ5756 series products also offer programmable functions, including voltage level, voltage change slew rate, and soft-start slew rate, which can be controlled through an I²C interface operating at up to 3.4MHz. Additionally, these products support remote-sense function to ensure accurate output voltage under heavy loads. They are equipped with interrupt and fault-detection functions to report any error status. The RTQ5756 series products are available in a WL-CSP-54B 2.69x3.92 (BSC) package. The recommended junction temperature range is –40°C to 125°C.

See Ordering Information for the key features of each part number.

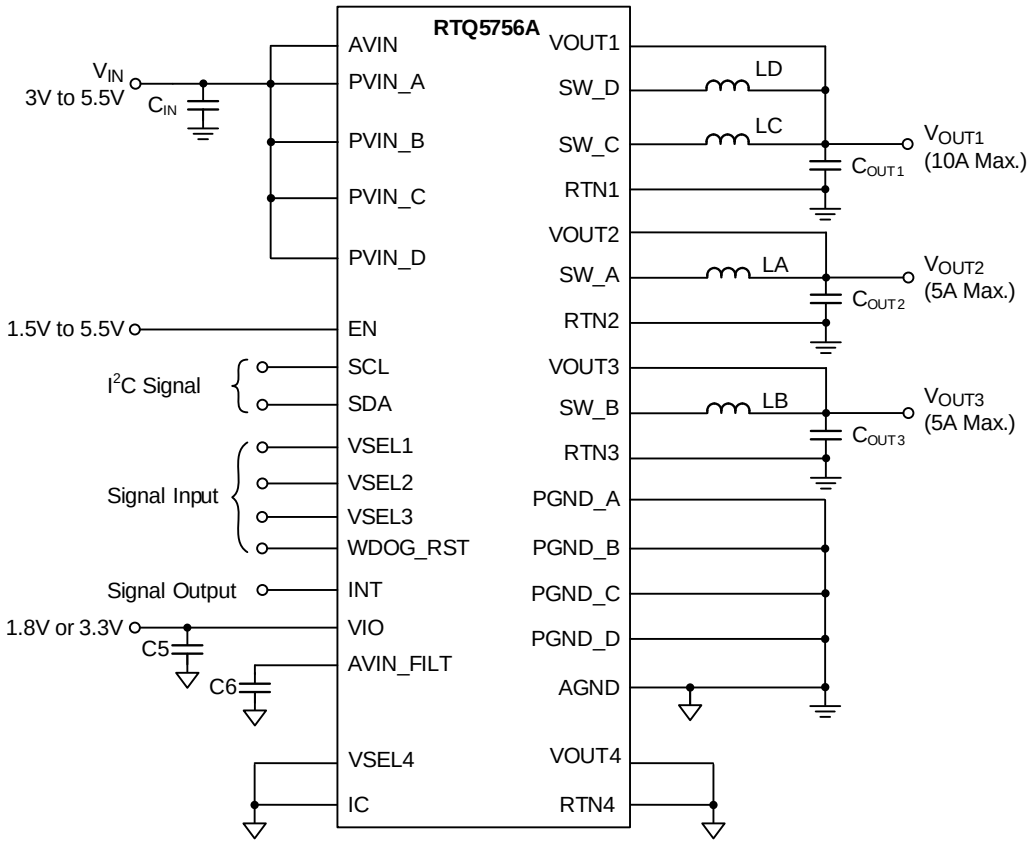
2 Features

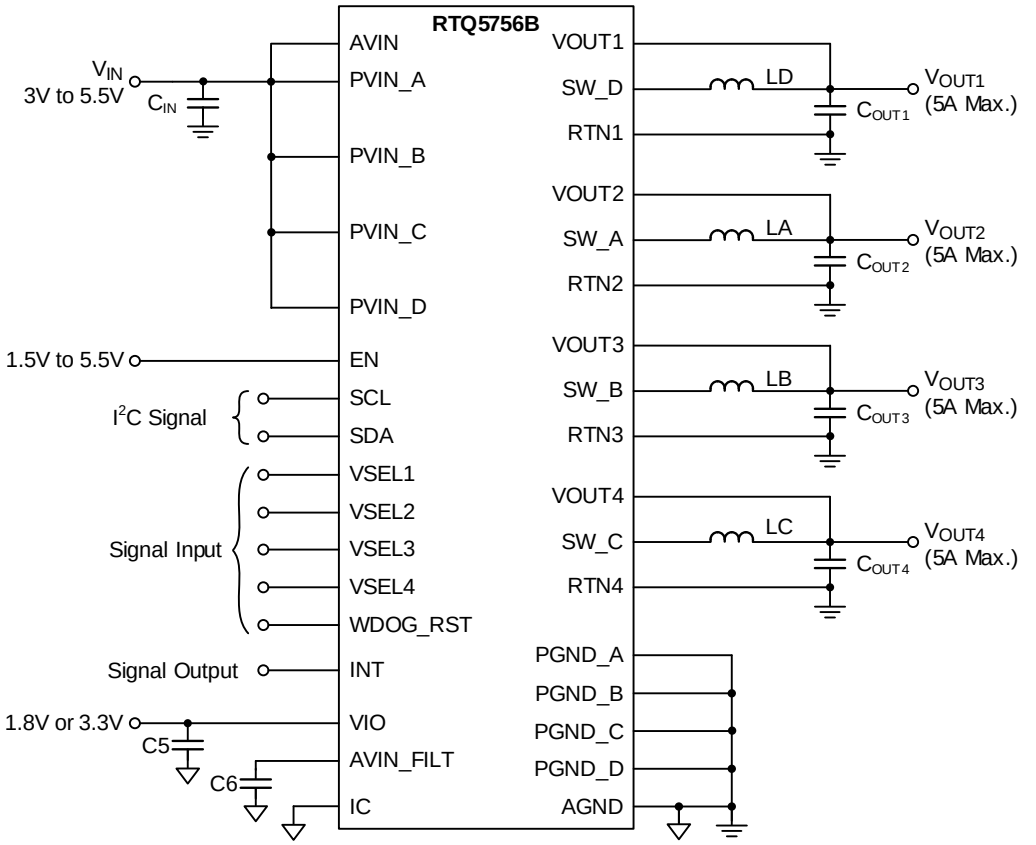
- **Integrated FETs- 4-Phase Buck Converter**
- **Input Supply Voltage Range: 3V to 5.5V**
- **I²C Programmable Output Voltage: 0.4 to 2.05V (0.4 to 1.55V for 3-phase and 4-phase outputs)**
- **Typical Switching Frequency: 2MHz and 2.2MHz**
- **Support 5A Output Current Capability Per Phase**
- **Differential Remote Sense for Each Output with High Accuracy**
- **Fast Transient Response**
- **Power Saving Mode Enables Higher Light Load Efficiency**
- **Output Dynamic Voltage Scaling (DVS) with Programmable Ramp Up/Down Slew Rate**
- **Programmable Soft-Start Function**
- **Programmable Startup/Shutdown Sequence**
- **Interrupt Function and Fault Detection**
- **Watchdog Reset Function Prevents System Hang**
- **Input Undervoltage-Lockout (UVLO)**
- **Cycle-by-Cycle Current Limit for Each Phase**
- **Output Overvoltage/Undervoltage Protection**
- **Over-Temperature Protection**
- **WL-CSP-54B 2.69x3.92 (BSC) Package**

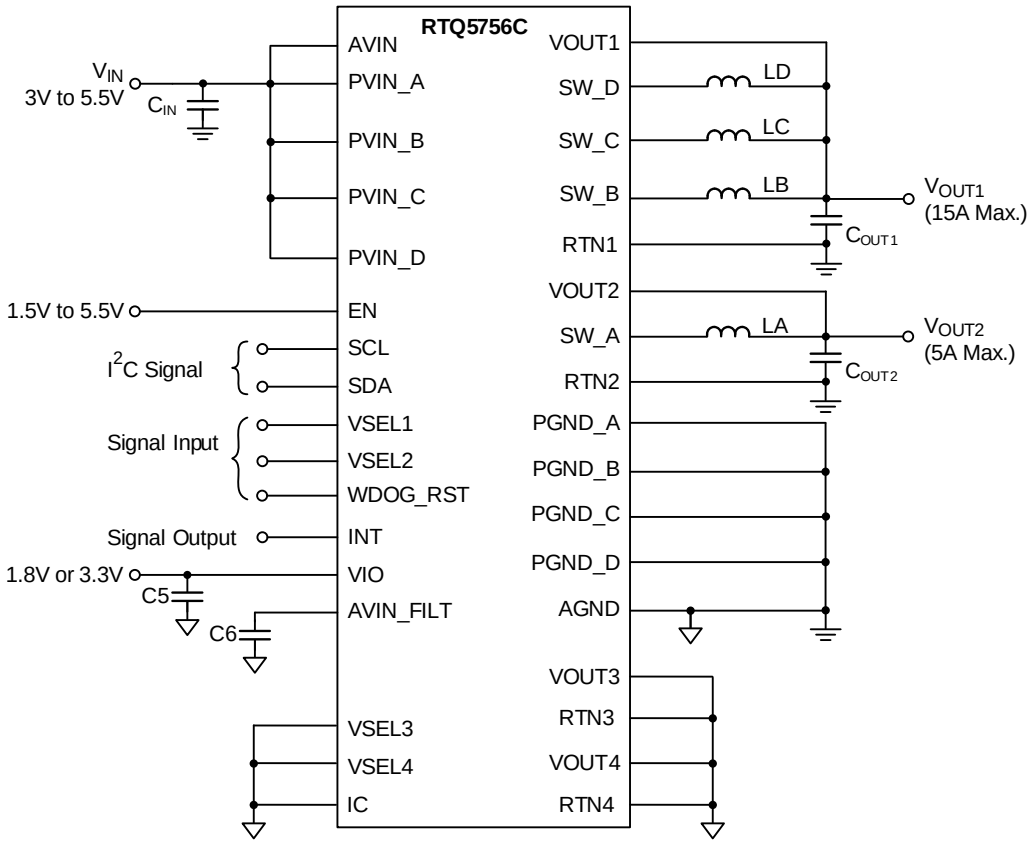
3 Applications

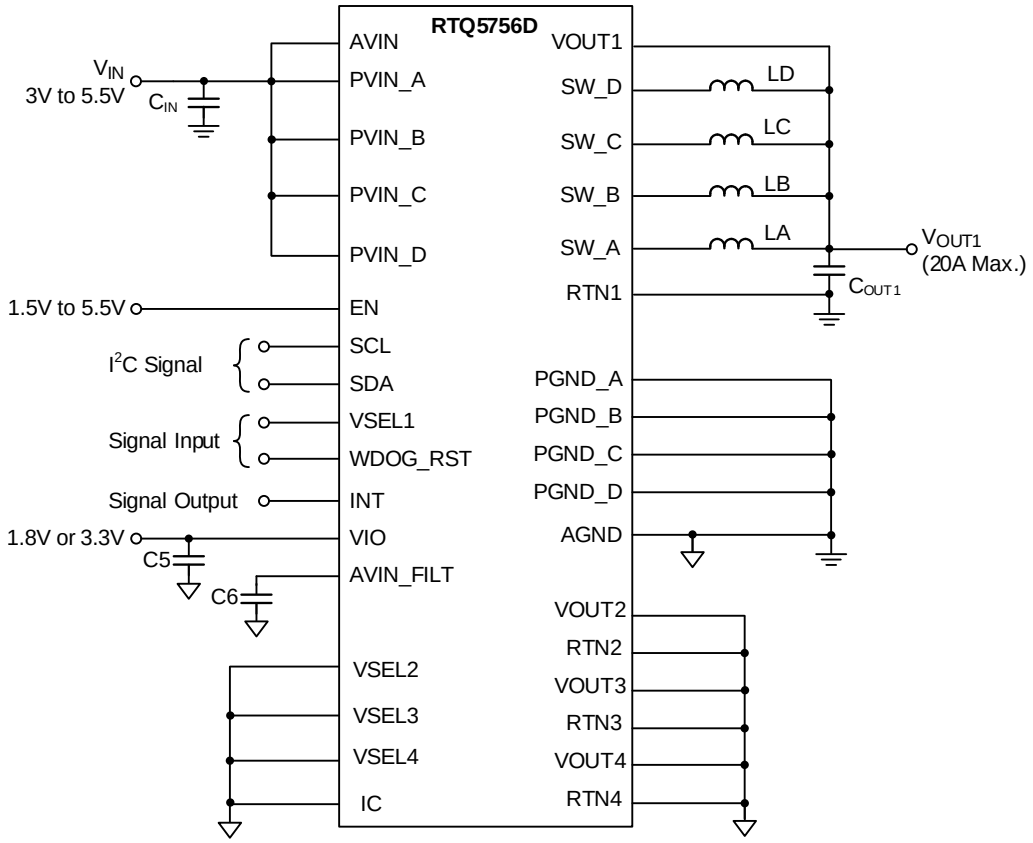
- Home Gateway and Access Point Networks
- Optical Modules
- Set-Top Boxes and OTT Devices
- Storage Systems
- Surveillance Systems

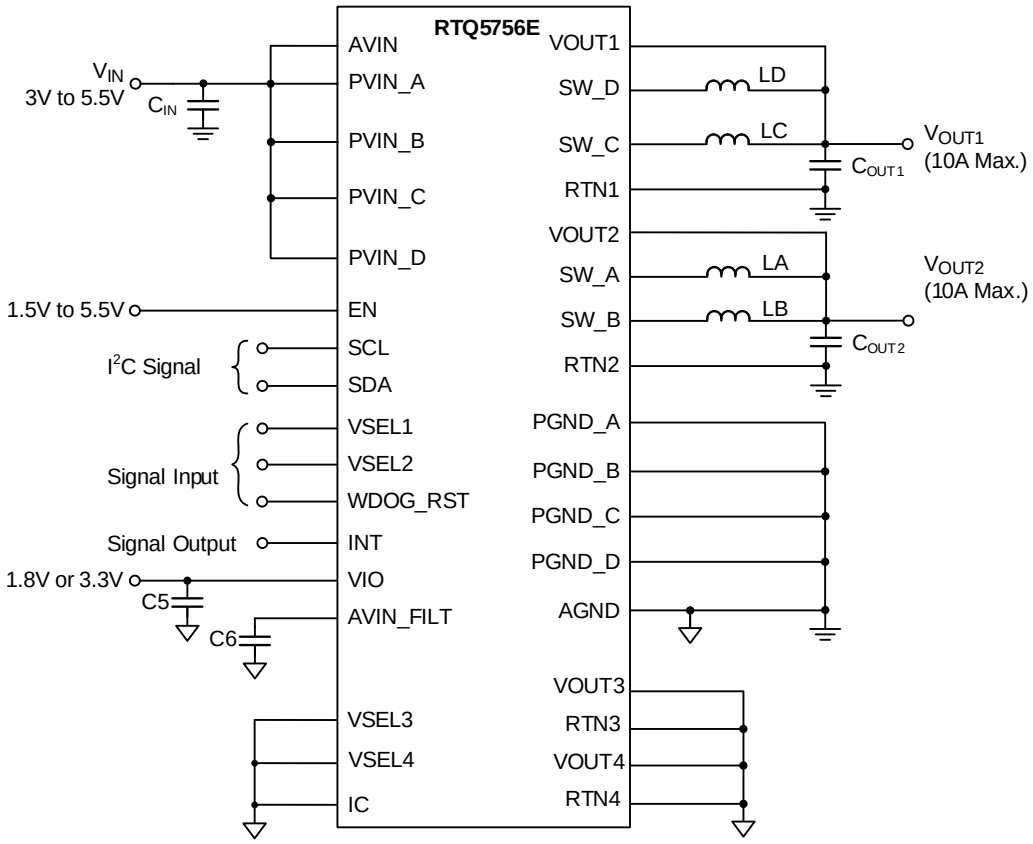
4 Simplified Application Circuit











5 Ordering Information

Product Number(1)	Output Channel	Configuration	Typical Switching Frequency	I²C Programmable Output Voltage	Package Type(2)
RTQ5756AWSC-YY	Vout1~3	2+1+1 phase	2MHz	0.4V to 2.05V	WSC: WL-CSP-54B 2.69x3.92 (BSC)
RTQ5756BWSC-YY	Vout1~4	1+1+1+1 phase			
RTQ5756EWSC-YY	Vout1~2	2+2 phase			
RTQ5756CWSC-YY	Vout1	3+1 phase	2.2MHz	0.4V to 1.55V	
	Vout2			0.4V to 2.05V	
RTQ5756DWSC-YY	Vout1	4+0 phase		0.4V to 1.55V	

Note 1.

- Marked with (1) indicated: The last two bits "YY" represent the trim version. See Product Status for all available devices. For additional trim options, contact our sales representative directly or through a Richtek distributor located in your area.
- Marked with (2) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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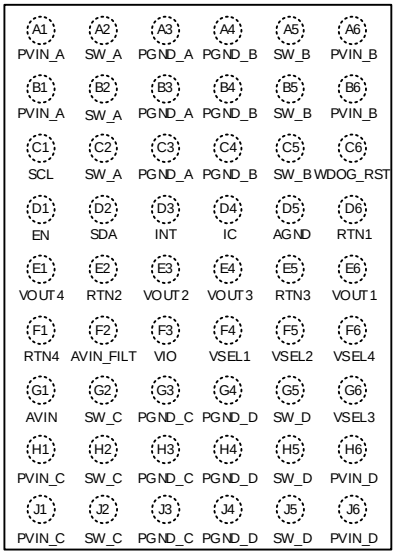
7 Pin Configuration

(TOP VIEW)



WL-CSP-54B 2.69x3.92 (BSC)

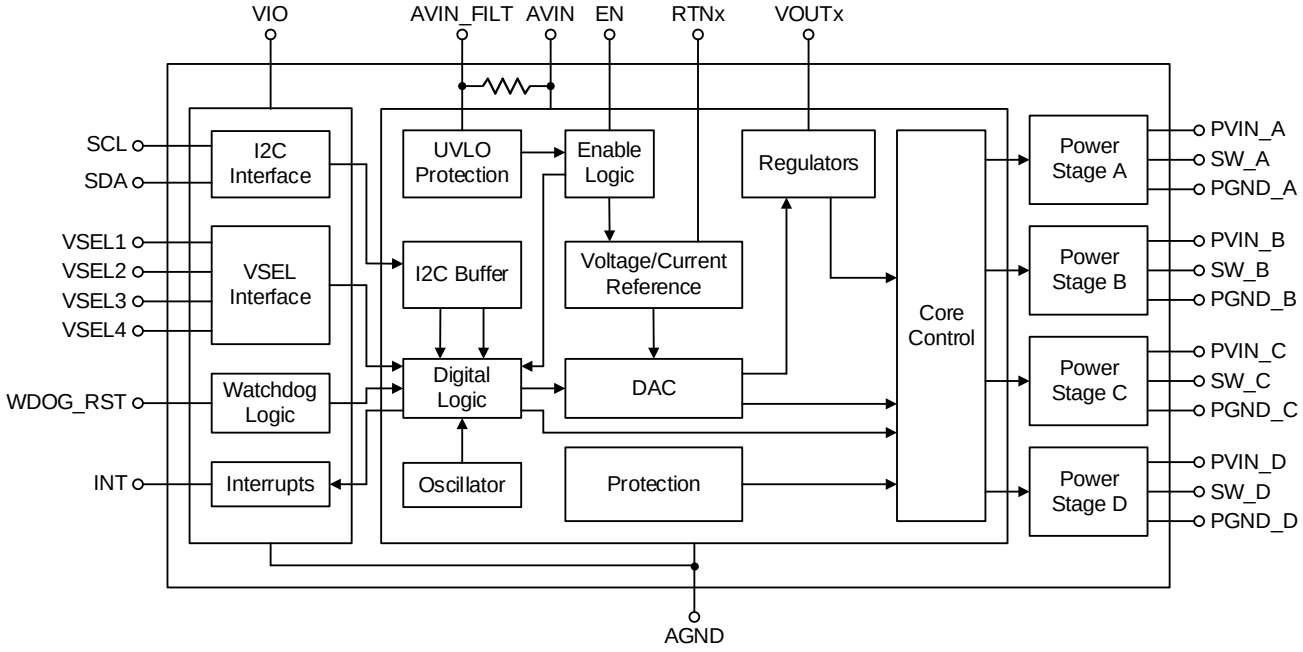
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, B1	PVIN_A	Power input for power stage A. It is recommended to use a 10μF, X7R capacitor.
A2, B2, C2	SW_A	Switch node for power stage A. Connect to the power inductor.
A3, B3, C3	PGND_A	Power ground for power stage A.
A4, B4, C4	PGND_B	Power ground for power stage B.
A5, B5, C5	SW_B	Switch node for power stage B. Connect to the power inductor.
A6, B6	PVIN_B	Power input for power stage B. It is recommended to use a 10μF, X7R capacitor.
C1	SCL	Clock input for the I^2C interface. The pull-up voltage supply must be the same as the VIO voltage for correct operation. Connect this pin to AGND if the I^2C interface is not used. Do not leave this pin floating.
C6	WDOG_RST	Control input for output voltage reset. Resets each buck output voltage, DVSx, and ENDVSx registers to the factory default setting value when this pin is pulled low. Connect this pin to a voltage higher than 70% of the VIO pin voltage if this pin is not used. Do not leave this pin floating. The minimum watchdog debounce time is 100μs.
D1	EN	Master chip enable. A logic-high enables the converter; a logic-low forces the device into shutdown mode. Do not leave this pin floating.
D2	SDA	Data line for the I^2C interface. The pull-up voltage supply must be the same as the VIO voltage for correct operation. Connect this pin to AGND if the I^2C interface is not used. "Do Not" leave this pin floating.
D3	INT	Interrupt indicator.
D4	IC	Internal connection. Connect this pin to AGND.
D5	AGND	Ground for internal analog and digital circuitry.

Pin No.	Pin Name	Pin Function
D6	RTN1	Remote ground sense for Buck1.
E1	VOUT4	Output voltage sense for Buck4. Short to AGND for RTQ5756A/C/D/E.
E2	RTN2	Remote ground sense for Buck2. Short to AGND for RTQ5756D.
E3	VOUT2	Output voltage sense for Buck2. Short to AGND for RTQ5756D
E4	VOUT3	Output voltage sense for Buck3. Short to AGND for RTQ5756C/D/E.
E5	RTN3	Remote ground sense for Buck3. Short to AGND for RTQ5756C/D/E.
E6	VOUT1	Output voltage sense for Buck1.
F1	RTN4	Remote ground sense for Buck4. Short to AGND for RTQ5756A/C/D/E.
F2	AVIN_FILT	Filtered analog supply voltage. It is recommended to connect a 1μF, X7R capacitor from this pin to AGND.
F3	VIO	I/O supply voltage for digital communications. Connect this pin to 1.8V or 3.3V. Do not leave this pin floating.
F4	VSEL1	Buck1 DVS register selection control input. 0x52[1:0] determines the DVS register control input of Buck1. When 0x52[1:0] is set to “10”, Buck1 DVS up or down operation is controlled by the external VSEL1 pin. Then 0x52[2] determines the polarity of the VSEL1 pin: DVS0 is selected if the VSEL1 pin is pulled up to V_{VIO}, but DVS1 is selected if the VSEL1 pin is pulled down to AGND. The factory default setting value of 0x52[1:0] is 00 (DVS0 is selected and ignores the VSEL1 pin). Do not leave this pin floating.
F5	VSEL2	Buck2 DVS register selection control input. 0x6C[1:0] determines the DVS register control input of Buck2. When 0x6C[1:0] is set to “10”, Buck2 DVS up or down operation is controlled by the external VSEL2 pin. Then 0x6C[2] determines the polarity of the VSEL2 pin: DVS0 is selected if the VSEL2 pin is pulled up to V_{VIO}, but DVS1 is selected if the VSEL2 pin is pulled down to AGND. The factory default setting value of 0x6C[1:0] is 00 (DVS0 is selected and ignores the VSEL2 pin). Do not leave this pin floating. Short to AGND for RTQ5756D.
G6	VSEL3	Buck3 DVS register selection control input. 0x86[1:0] determines the DVS register control input of Buck3. When 0x86[1:0] is set to “10”, Buck3 DVS up or down operation is controlled by the external VSEL3 pin. Then 0x86[2] determines the polarity of the VSEL3 pin: DVS0 is selected if the VSEL3 pin is pulled up to V_{VIO}, but DVS1 is selected if the VSEL3 pin is pulled down to AGND. The factory default setting value of 0x86[1:0] is 00 (DVS0 is selected and ignores the VSEL3 pin). Do not leave this pin floating. Short to AGND for RTQ5756C/D/E.
G1	AVIN	Analog supply voltage input.
G2, H2, J2	SW_C	Switch node for power stage C. Connect to the power inductor.
G3, H3, J3	PGND_C	Power ground for power stage C.
G4, H4, J4	PGND_D	Power ground for power stage D.
G5, H5, J5	SW_D	Switch node for power stage D. Connect to the power inductor.

Pin No.	Pin Name	Pin Function
F6	VSEL4	Buck4 DVS register selection control input. 0xA0[1:0] determines the DVS register control input of Buck4. When 0xA0[1:0] is set to “10”, Buck4 DVS up or down operation is controlled by the external VSEL4 pin. Then 0xA0[2] determines the polarity of the VSEL4 pin: DVS0 is selected if the VSEL4 pin is pulled up to V_{VIO}, but DVS1 is selected if the VSEL4 pin is pulled down to AGND. The factory default setting value of 0xA0[1:0] is 00 (DVS0 is selected and ignores the VSEL4 pin). Do not leave this pin floating. Short to AGND for RTQ5756A/C/D/E.
H1, J1	PVIN_C	Power input for power stage C. It is recommended to use a 10μF, X7R capacitor.
H6, J6	PVIN_D	Power input for power stage D. It is recommended to use a 10μF, X7R capacitor.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, PVIN_x ---------- –0.3V to 6V
- SW_x PIN Switch Voltage, SW_x ---------- –0.3V to 7.3V
  < 20ns ---------- –1V to 9.5V
- PVIN_x Pin to SW_x PIN ---------- –0.3V to 6V
  <20ns ---------- –1V to 9.5V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 3V to 5.5V
- Output Voltage Range for 1 and 2 Phase Configuration ---------- 0.4V to 2.05V
- Output Voltage Range for 3 and 4 Phase Configuration ---------- 0.4V to 1.55V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WL-CSP-54B 2.69x3.92 (BSC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	37.9	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	0.8	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	35.2	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.6	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 110mm x 100mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(Note 7)

(V_{IN} = 3.7V, V_{VIO} = 1.8V or 3.3V, T_J = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Analog Input Voltage	V_{AVIN}		3	--	5.5	V
Power Input Voltage	V_{PVIN}		3	--	5.5	V
Shutdown Current	I_{SHDN}	EN = 0V, digital circuit does not work	--	0.1	--	μA
Buck Off Current	I_{SDBO}	EN = VIO = 1.8V, disable all Buck converters by software	--	30	--	μA
1Phase no Switching Current	I_{SLP_1ph}	V_{OUT} = 1.2 x $V_{OUT\_SETTING}$	--	100	--	μA
2Phase no Switching Current	I_{SLP_2ph}	V_{OUT} = 1.2 x $V_{OUT\_SETTING}$	--	130	--	μA
3Phase no Switching Current	I_{SLP_3ph}	V_{OUT} = 1.2 x $V_{OUT\_SETTING}$	--	160	--	μA
4Phase no Switching Current	I_{SLP_4ph}	V_{OUT} = 1.2 x $V_{OUT\_SETTING}$	--	190	--	μA
Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising	2.45	2.7	2.95	V
Undervoltage-Lockout Hysteresis	ΔV_{UVLO}		--	300	--	mV
Switching Frequency	f_{SW}	RTQ5756A/B/E, V_{OUT} = 1V (FCCM)	1.7	2	2.3	MHz
		RTQ5756C/D, V_{OUT} = 1V (FCCM)	1.9	2.2	2.4	
On-Resistance of High-side MOSFET	R_{DSON_H}	V_{IN} = 5V	--	17	--	mΩ
On-Resistance of Low-side MOSFET	R_{DSON_L}	V_{IN} = 5V	--	5	--	mΩ
HSFET Current Limit per Channel	I_{LIM_H}		6.5	8	9	A
LSFET Current Limit per Channel	I_{LIM_L}		5	7	8.5	A
LSFET Negative Current Limit per Channel	I_{LIM_NL}		--	3.5	--	A
SDA, SCL, WDOG_RST, VSEL Input Voltage Logic-High	V_{IH}	3V ≤ V_{IN} ≤ 5.5V	0.7 x VIO	--	--	V
SDA, SCL, WDOG_RST, VSEL Input Voltage Logic-Low	V_{IL}	3V ≤ V_{IN} ≤ 5.5V	--	--	0.3 x VIO	
EN Input Voltage Rising Threshold	V_{EN_R}		1.2	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	
V_{OUT} DC Accuracy	V_{OUT_FPWM}	Forced PWM, 0.6V ≤ V_{OUT} ≤ 2.05V	–1.5	--	1.5	%
Output Undervoltage Protection Rising Threshold	V_{UVP_R}	Trigger level	40	50	60	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Undervoltage Protection Falling Threshold	V_{UVP_F}	Recovery level	47	57	67	%
Output Overvoltage Protection Rising Threshold	V_{OVP_R}	Trigger level	120	133	145	%
Output Overvoltage Protection Falling Threshold	V_{OVP_F}	Recovery level	110	125	140	%
Minimum On-Time	t_{ON_MIN}		--	40	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	90	--	ns
Discharge Resistor	R_{DISCHG}		--	10	--	Ω
Current Balance	$I_{BALANCE}$	RTQ5756A/E, Load = 10A, $\lvert I_{Avg} - I_{SW\_N;\ N = A\ to\ D}\rvert$, T_A = 0 to 85°C	--	--	0.5	A
		Load = 10A, $\lvert I_{Avg} - I_{SW\_N;\ N = A\ to\ D}\rvert$	--	--	1.2	
INT Output Voltage Logic-High	V_{OH}	Push-pull, I_{SINK} = 2mA	1.6	--	VIO	V
INT Output Voltage Logic-Low	V_{OL}	Output low level, I_{SOURCE} = 2mA	--	--	0.4	V

Note 7. The measured switching frequency may not always fall within the declared range due to variations in operation modes and operating points. In auto mode, the switching frequency (f_{SW}) is reduced to enable power-saving functionality during light load conditions. Additionally, in multiphase operation, the f_{SW} varies based on the active phase count in auto mode, meaning that the switching frequency adjusts according to the number of active phases.

14.1 System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. (V_{IN} = 3.7V, V_{VIO} = 1.8V or 3.3V, T_J = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
V_{OUT} DC Accuracy	V_{OUT_AUTO}	Auto Mode, V_{OUT} = 1V	–2.5	--	2.5	%
Load Regulation	V_{LOAD_REG}	$I_{OUT(DC)}$ = 0A to 10A (FCCM)	--	–0.08	--	%/A
Line Regulation	V_{LINE_REG}	3V ≤ V_{IN} ≤ 5V, $I_{OUT(DC)}$ = 0A (FCCM)	--	0.2	--	%/V
Load Transient Response	V_{LOAD_TRAN}	1-phase configuration, 0.01A to 2.5A, t_R = t_F = 100ns, L= 0.22µH, V_{OUT} = 1V, C_{OUT} = 22µF x 2/phase, T_A = 25°C (FCCM)	--	±50	--	mV
		2-phase configuration, 0.01A to 5A, t_R = t_F = 200ns, L= 0.22µH, V_{OUT} = 1V, C_{OUT} = 22µF x 2/phase, T_A = 25°C (FCCM)	--	±50	--	mV
		3-phase configuration, 0.01A to 7.5A, t_R = t_F = 300ns, L= 0.22µH, V_{OUT} = 1V, C_{OUT} = 22µF x 2/phase, T_A = 25°C (FCCM)	--	±50	--	mV
		4-phase configuration, 0.01A to 10A, t_R = t_F = 200ns, L= 0.22µH, V_{OUT} = 1V, C_{OUT} = 22µF x 2/phase, T_A = 25°C (FCCM)	--	±50	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Phase Adding Level	I_{ADD}	From 1-phase to 2-phase, V_{OUT} = 1V	--	3.6	--	A
		From 2-phase to 3-phase, V_{OUT} = 1V	--	5.4	--	
		From 3-phase to 4-phase, V_{OUT} = 1V	--	8.2	--	
Phase Shedding Level	I_{SHED}	From 2-phase to 1-phase, V_{OUT} = 1V	--	2	--	A
		From 3-phase to 2-phase, V_{OUT} = 1V	--	4.5	--	
		From 4-phase to 3-phase, V_{OUT} = 1V	--	6.4	--	
Soft-Start Time	t_{SS}	Slew Rate = 10mV/μs	–20	--	20	%
Dynamic Voltage Scaling Rising Slew Rate	$t_{DVS\_SR\_R}$	VIN = 3.7V, VOUT = 0.6V to 1.2V, Slew Rate = 16mV/μs (default)	–20	--	20	%
Dynamic Voltage Scaling Falling Slew Rate	$t_{DVS\_SR\_F}$	VIN = 3.7V, VOUT = 1.2V to 0.6V, Slew Rate = 4mV/μs (default)	–20	--	20	%
Over-Temperature Protection Threshold	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	40	--	°C
HOT Die Warning	T_{HD}		--	110	--	°C
HOT Die Warning Hysteresis	T_{HD_HYS}		--	15	--	°C
I^2C Interface						
SCL Clock Frequency	f_{SCL}	Standard mode	--	--	100	kHz
		Fast mode	--	--	400	kHz
		Fast mode plus	--	--	1	MHz
		High speed mode, load 100pF max	--	--	3.4	MHz
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
		High speed mode	0.16	--	--	
SCL Clock Low Period	t_{LOW}	Standard mode	4.7	--	--	μs
		Fast mode	1.3	--	--	
		Fast mode plus	0.5	--	--	
		High speed mode	0.16	--	--	
SCL Clock High Period	t_{HIGH}	Standard mode	4	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
		High speed mode	0.09	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard mode	4.7	--	--	μs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
		High speed mode	0.16	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA Data Hold Time	$t_{HD;DAT}$	Standard mode	5	--	--	µs
		Fast mode	0	--	--	
		Fast mode plus	0	--	--	
		High speed mode	0	--	--	
SDA Setup Time	$t_{SU;DAT}$	Standard mode	250	--	--	ns
		Fast mode	100	--	--	
		Fast mode plus	50	--	--	
		High speed mode	10	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard mode	4	--	--	µs
		Fast mode	0.6	--	--	
		Fast mode plus	0.26	--	--	
		High speed mode	0.16	--	--	
Bus Free Time between Stop and Start	t_{BUF}	Standard mode	4.7	--	--	µs
		Fast mode	1.3	--	--	
		Fast mode plus	0.5	--	--	
Rise Time of SDA and SCL Signals	t_R	Standard mode	--	--	1000	ns
		Fast mode	20	--	300	ns
		Fast mode plus	--	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
Fall Time of SDA and SCL Signals	t_F	Standard mode	--	--	300	
		Fast mode	20 x (VDD/ 5.5V)	--	300	ns
		Fast mode plus	20 x (VDD/ 5.5V)	--	120	ns
		High speed mode (SDA) load 100pF max	10	--	80	ns
		High speed mode (SCL) load 100pF max	10	--	40	ns
SDA Output Low Sink Current	I_{OL_I2C}	SDA voltage = 0.4V	2	--	--	mA

15 Typical Application Circuit

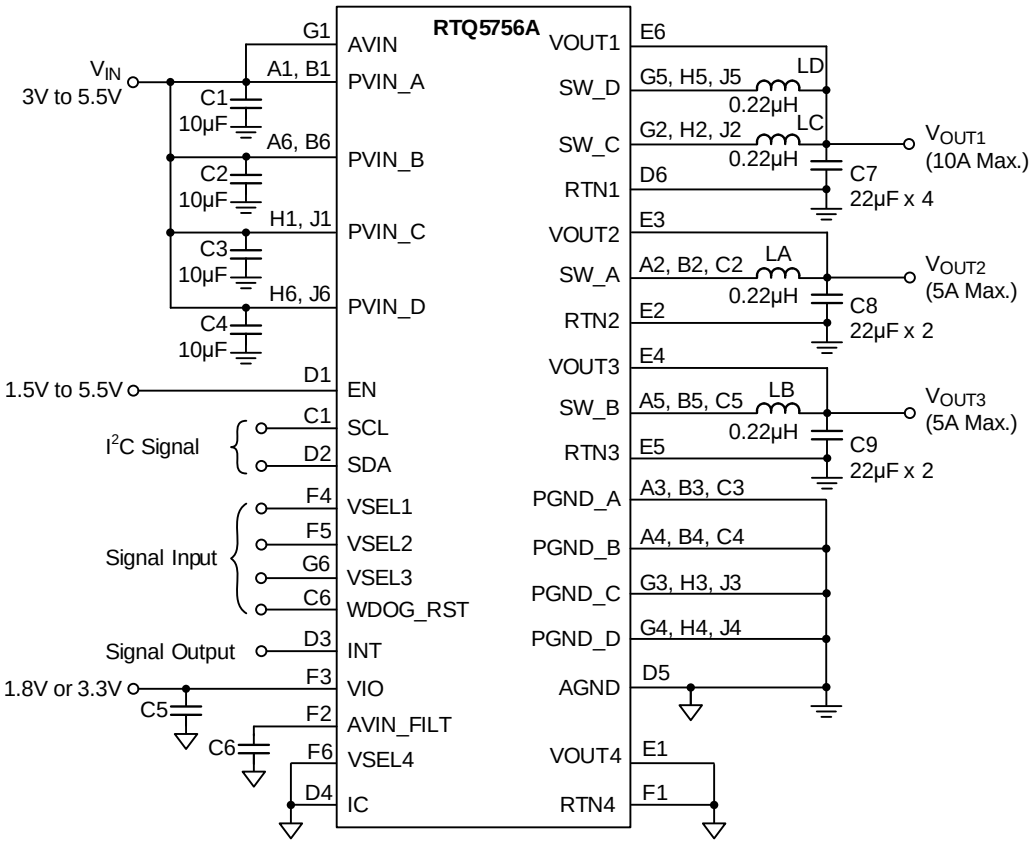


Table 1. Recommended BOM

Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RTQ5756A	DC-DC Converter	WL-CSP-54B 2.69x3.92 (BSC)	Richtek
C1, C2, C3, C4	4	GRM188D70J106MA73	10µF	C-0603	Murata
		GRM188C81A106MA73			
C5, C6	2	GCM188R71C105KA64	1µF	C-0603	Murata
		GRM155C71C105KE11		C-0402	
C7, C8, C9	8	GRM188C80G226ME15	22µF	C-0603	Murata
		GRM188D70J226ME01			
LA, LB, LC, LD	4	DFE201610E-R24M	0.24µH	2016	Murata
		TFM201610ALM-R24MTAA			TDK
		HMMQ25201B-R22MSR-57	0.22µH	2520	Cyntec

Note 8. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias. The effective values of capacitors C1 to C4 must be larger than 4µF, and capacitors C7 to C9 must be larger than 14µF.

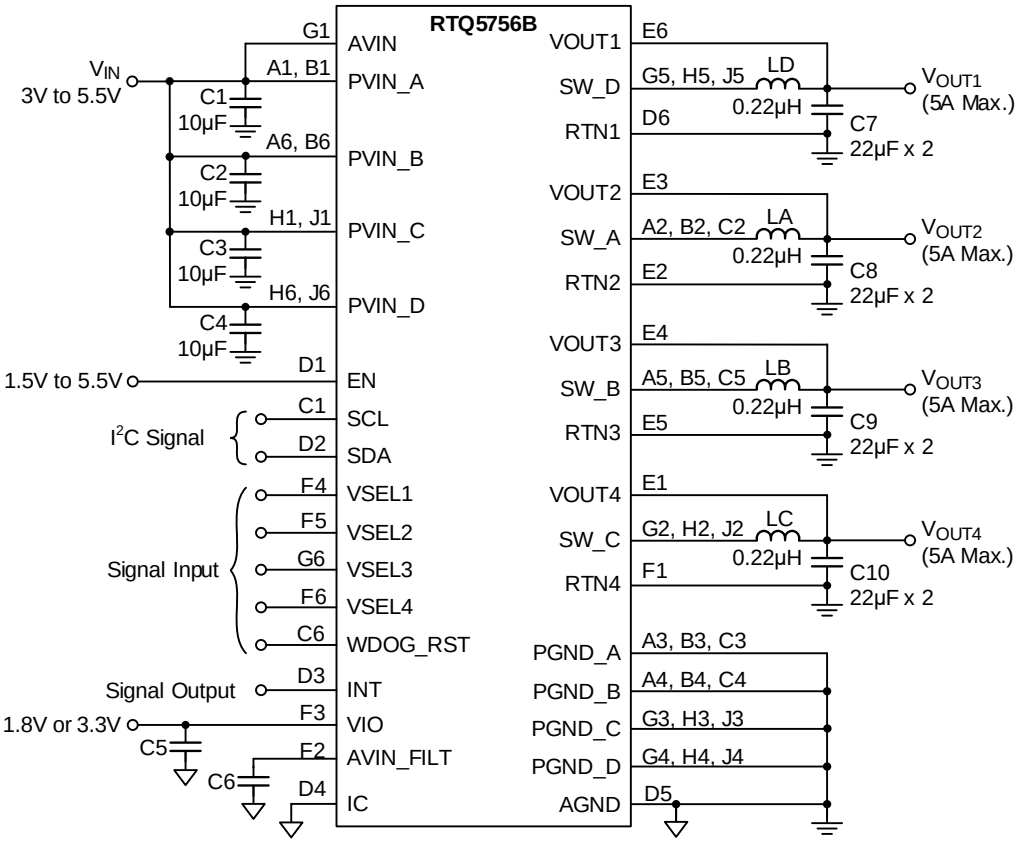


Table 2. Recommended BOM

Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RTQ5756B	DC-DC Converter	WL-CSP-54B 2.69x3.92 (BSC)	Richtek
C1, C2, C3, C4	4	GRM188D70J106MA73	10µF	C-0603	Murata
		GRM188C81A106MA73			
C5, C6	2	GCM188R71C105KA64	1µF	C-0603	Murata
		GRM155C71C105KE11		C-0402	
C7, C8, C9, C10	8	GRM188C80G226ME15	22µF	C-0603	Murata
		GRM188D70J226ME01			
LA, LB, LC, LD	4	DFE201610E-R24M	0.24µH	2016	Murata
		TFM201610ALM-R24MTAA			TDK
		HMMQ25201B-R22MSR-57	0.22µH	2520	Cyntec

Note 9. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias. The effective values capacitors of C1 to C4 must be larger than 4µF, and capacitors C7 to C10 must be larger than 14µF.

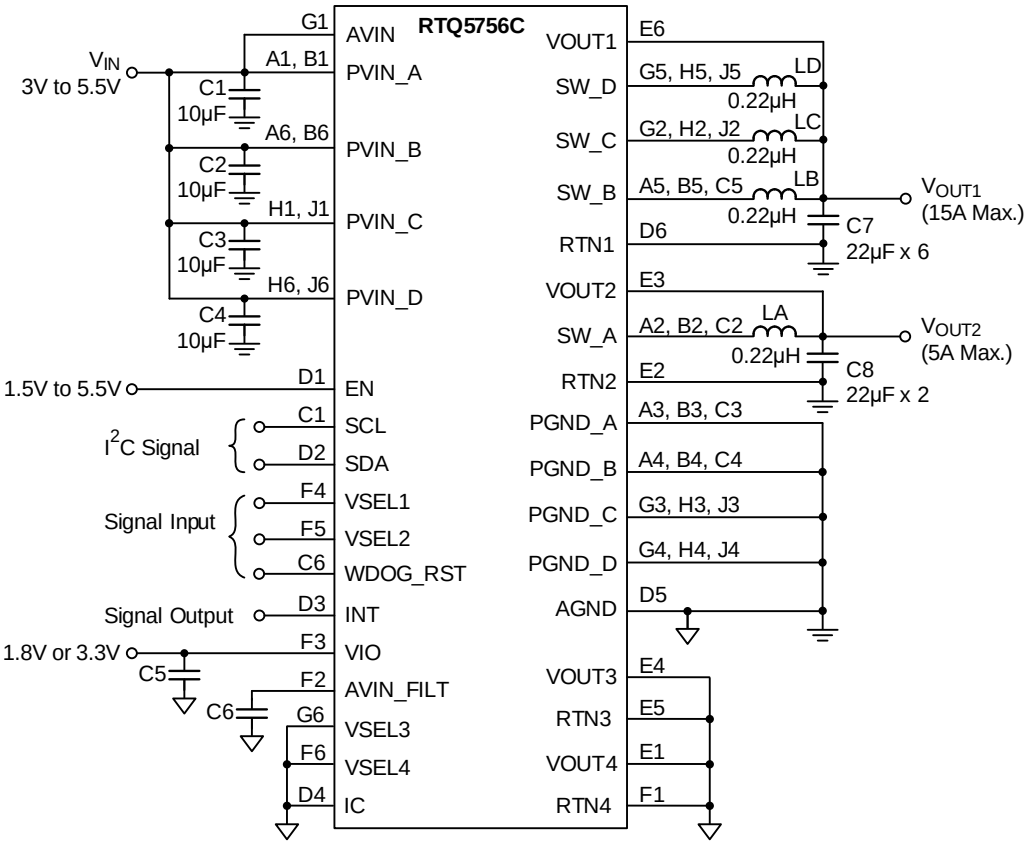


Table 3. Recommended BOM

Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RTQ5756C	DC-DC Converter	WL-CSP-54B 2.69x3.92 (BSC)	Richtek
C1, C2, C3, C4	4	GRM188D70J106MA73	10µF	C-0603	Murata
		GRM188C81A106MA73			
C5, C6	2	GCM188R71C105KA64	1µF	C-0603	Murata
		GRM155C71C105KE11		C-0402	
C7, C8	8	GRM188C80G226ME15	22µF	C-0603	Murata
		GRM188D70J226ME01			
LA, LB, LC, LD	4	DFE201610E-R24M	0.24µH	2016	Murata
		TFM201610ALM-R24MTAA			TDK
		HMMQ25201B-R22MSR-57	0.22µH	2520	Cyntec

Note 10. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias. The effective values of capacitors C1 to C4 must be larger than 4µF, and capacitors C7 and C8 must be larger than 14µF.

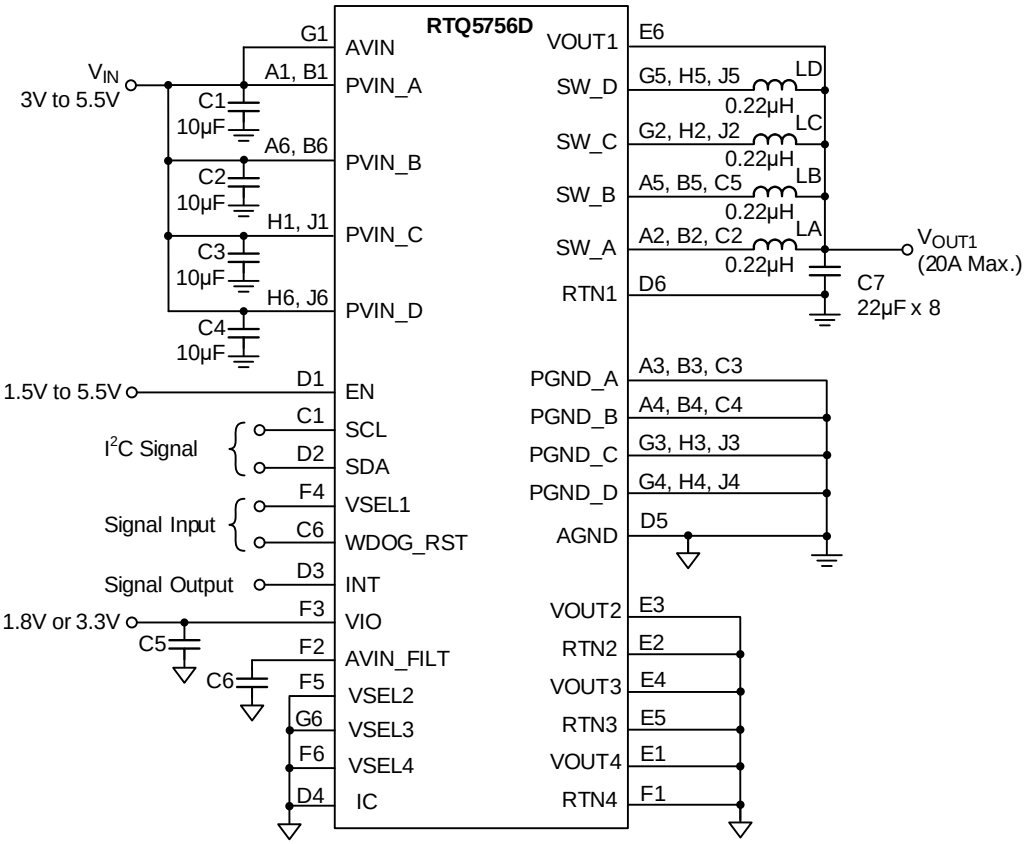


Table 4. Recommended BOM

Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RTQ5756D	DC-DC Converter	WL-CSP-54B 2.69x3.92 (BSC)	Richtek
C1, C2, C3, C4	4	GRM188D70J106MA73	10µF	C-0603	Murata
		GRM188C81A106MA73			
C5, C6	2	GCM188R71C105KA64	1µF	C-0603	Murata
		GRM155C71C105KE11		C-0402	
C7	8	GRM188C80G226ME15	22µF	C-0603	Murata
		GRM188D70J226ME01			
LA, LB, LC, LD	4	DFE201610E-R24M	0.24µH	2016	Murata
		TFM201610ALM-R24MTAA			TDK
		HMMQ25201B-R22MSR-57	0.22µH	2520	Cyntec

Note 11. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias. The effective values of capacitors C1 to C4 must be larger than 4µF, and capacitor C7 must be larger than 14µF.

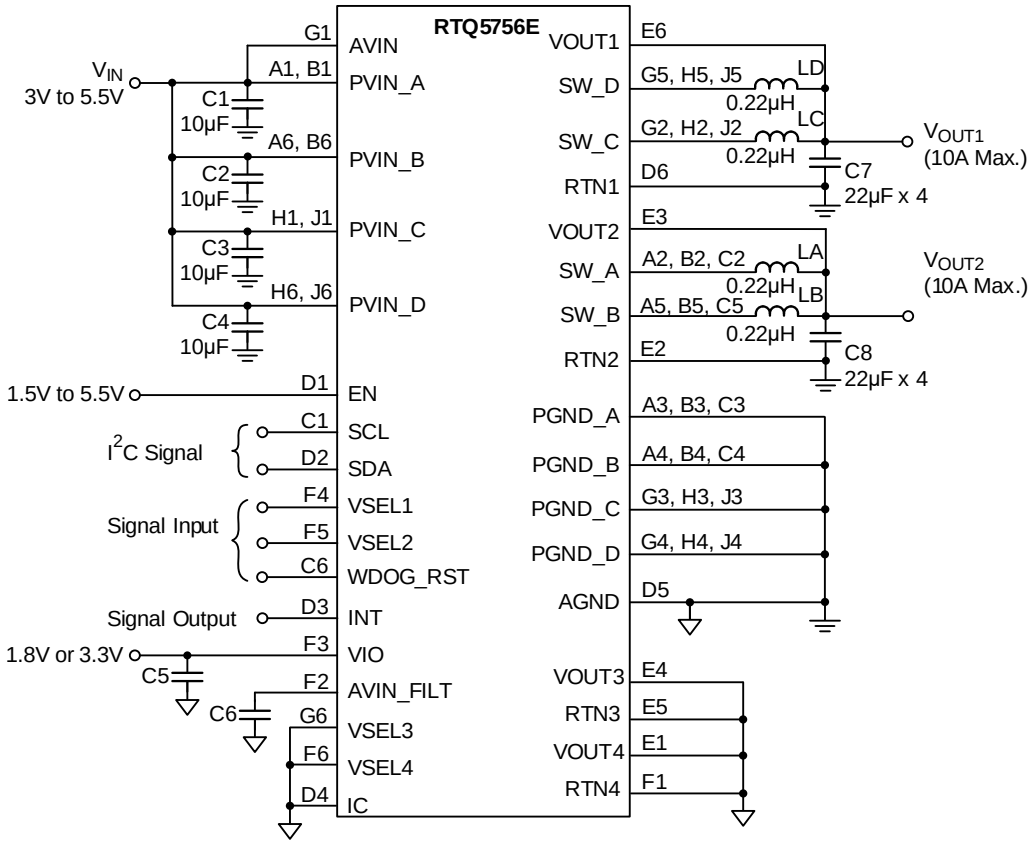


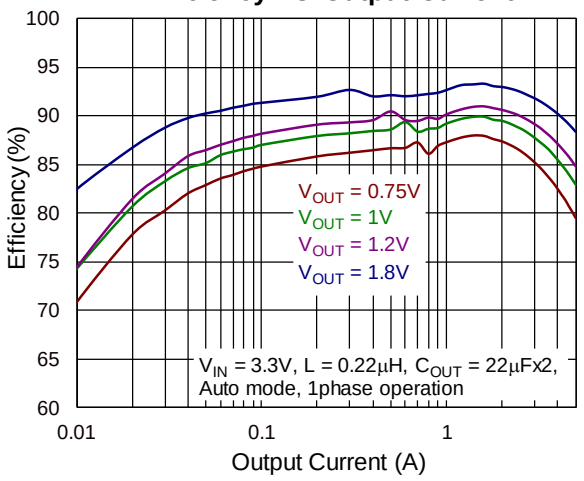
Table 5. Recommended BOM

Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RTQ5756E	DC-DC Converter	WL-CSP-54B 2.69x3.92 (BSC)	Richtek
C1, C2, C3, C4	4	GRM188D70J106MA73	10µF	C-0603	Murata
		GRM188C81A106MA73			
C5, C6	2	GCM188R71C105KA64	1µF	C-0603	Murata
		GRM155C71C105KE11		C-0402	
C7, C8	8	GRM188C80G226ME15	22µF	C-0603	Murata
		GRM188D70J226ME01			
LA, LB, LC, LD	4	DFE201610E-R24M	0.24µH	2016	Murata
		TFM201610ALM-R24MTAA			TDK
		HMMQ25201B-R22MSR-57	0.22µH	2520	Cyntec

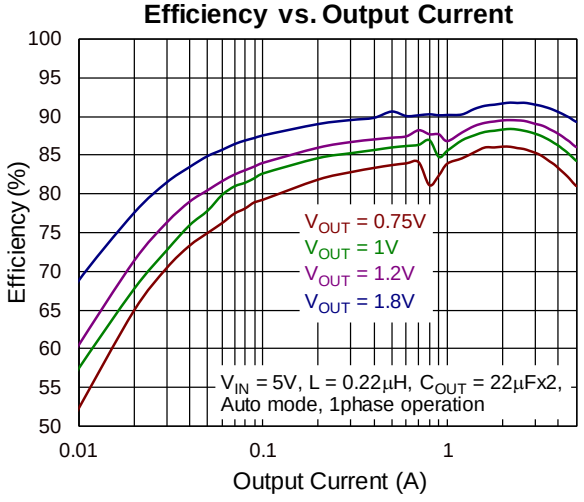
Note 12. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias. The effective values of capacitors C1 to C4 must be larger than 4µF, and capacitors C7 and C8 must be larger than 14µF.

16 Typical Operating Characteristics

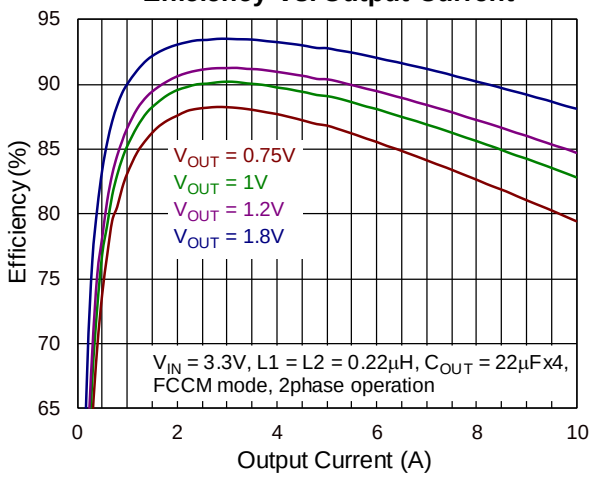
Efficiency vs. Output Current



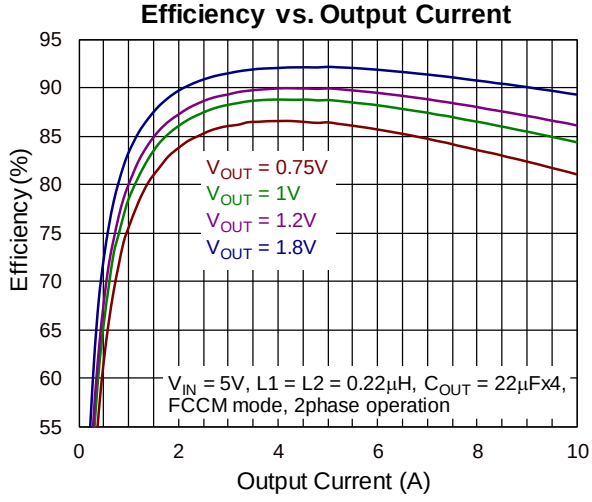
Efficiency vs. Output Current



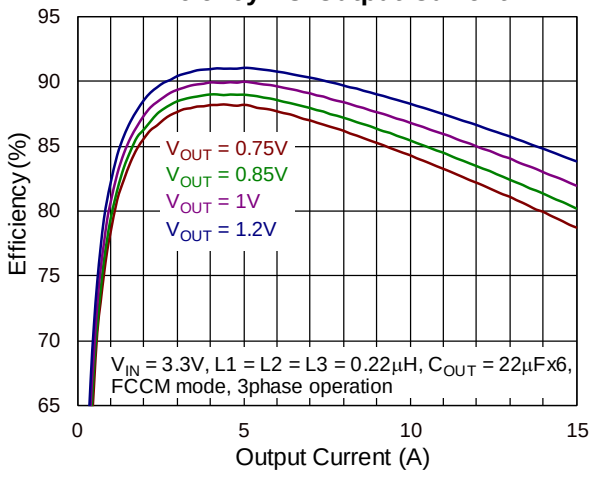
Efficiency vs. Output Current



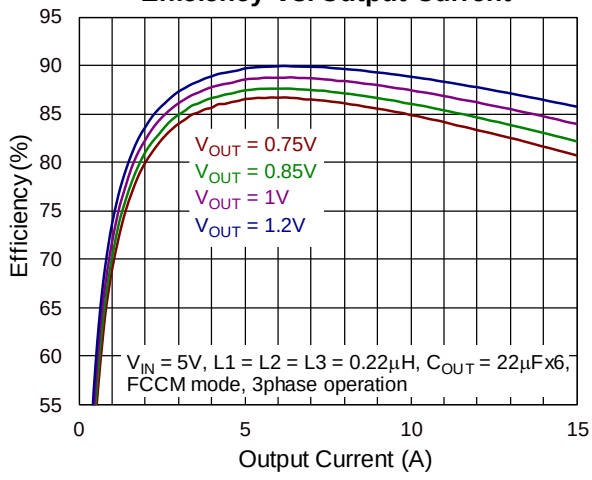
Efficiency vs. Output Current

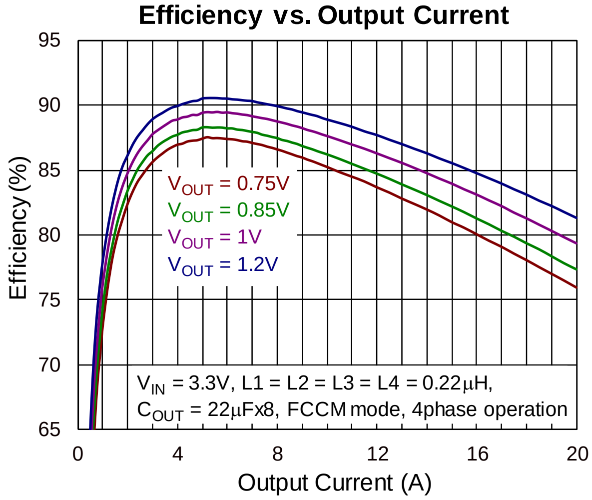


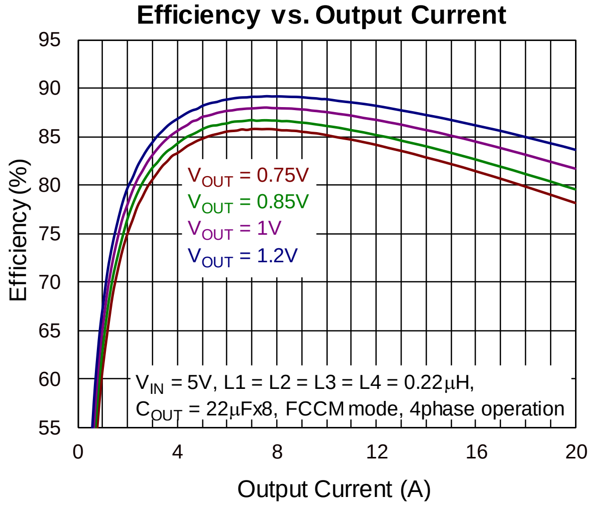
Efficiency vs. Output Current

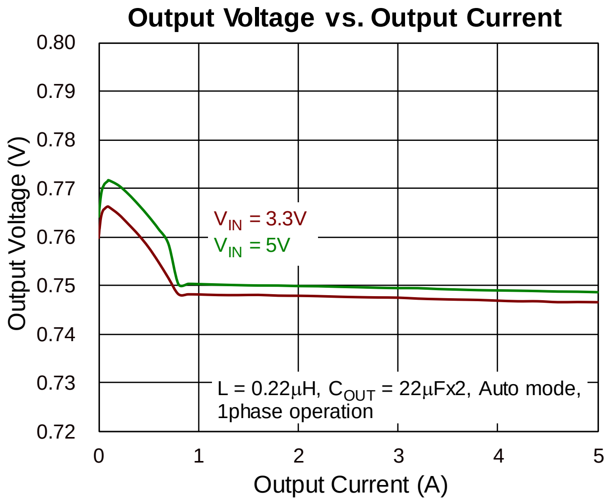


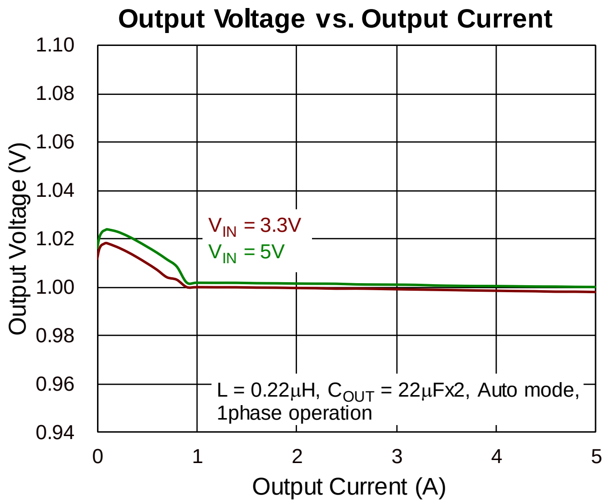
Efficiency vs. Output Current

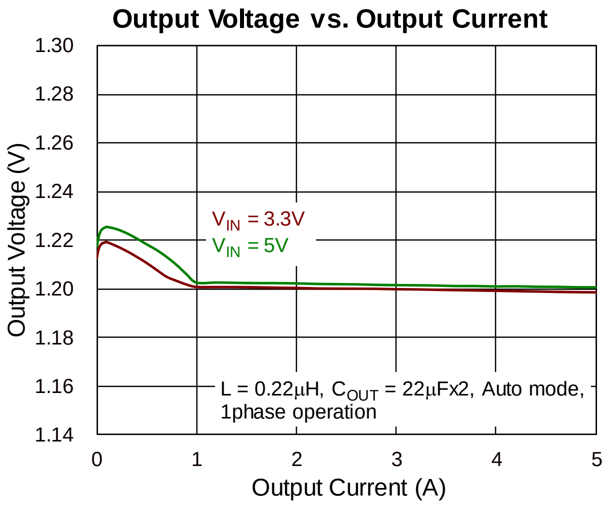


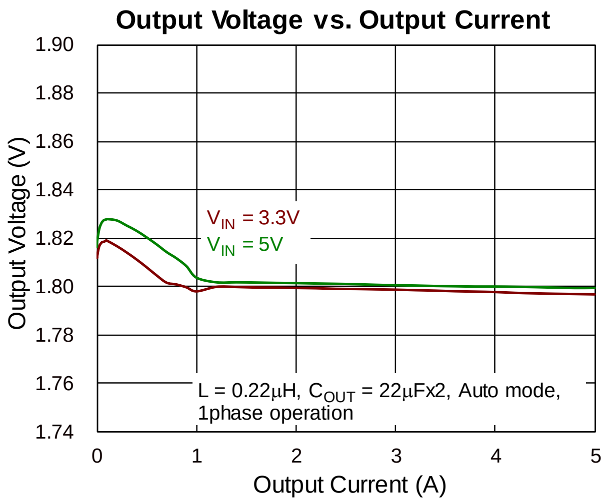




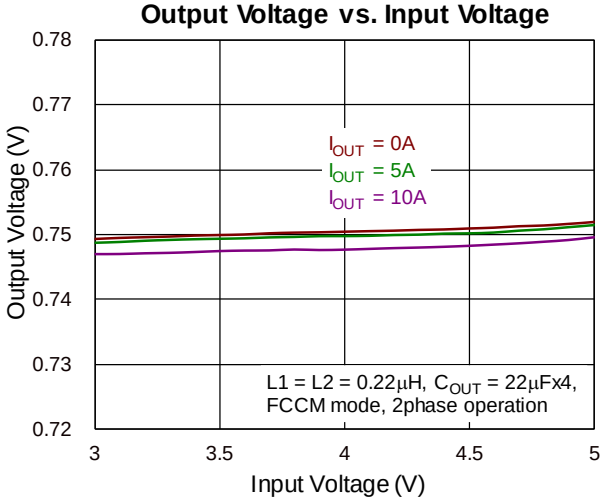




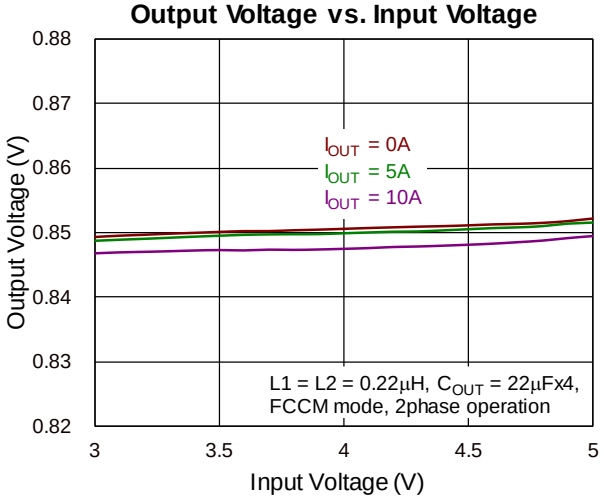




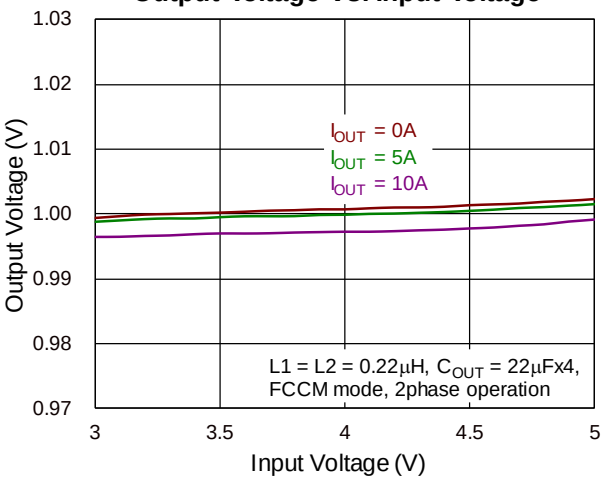
Output Voltage vs. Input Voltage



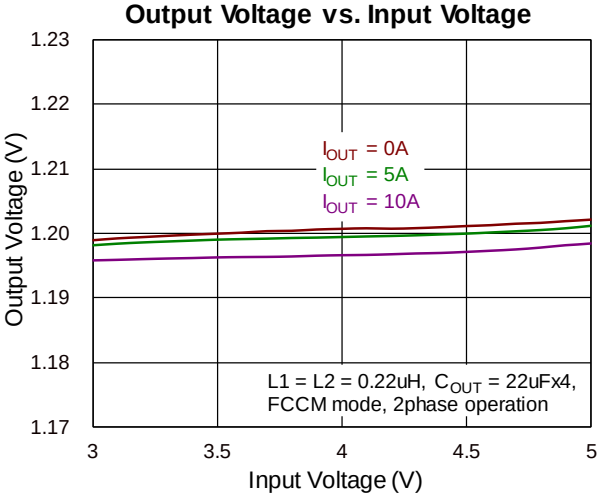
Output Voltage vs. Input Voltage



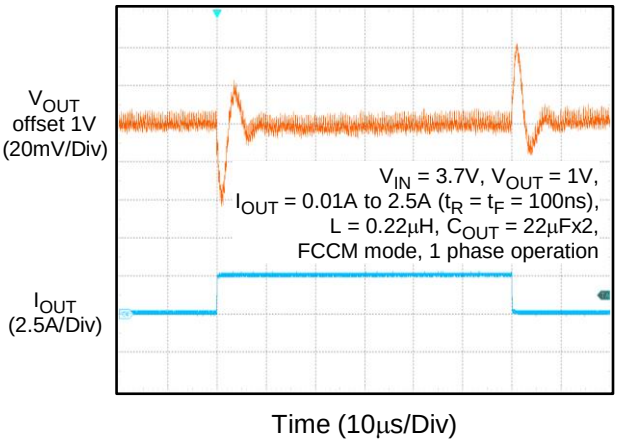
Output Voltage vs. Input Voltage



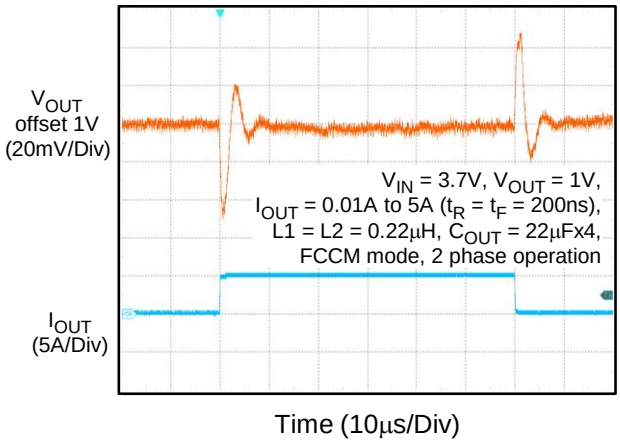
Output Voltage vs. Input Voltage



Load Transient Response



Load Transient Response



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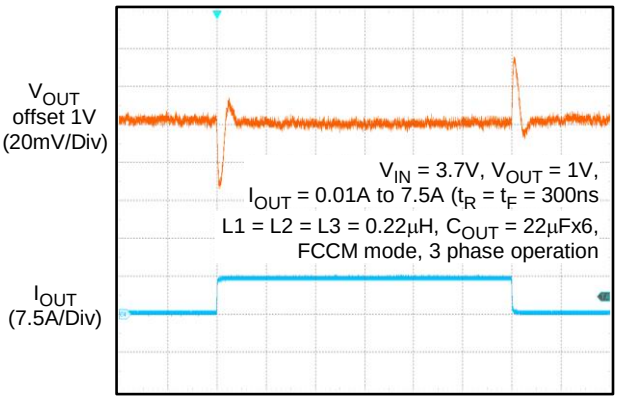
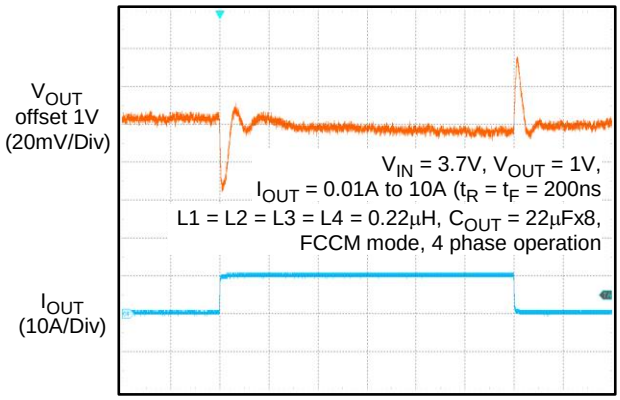


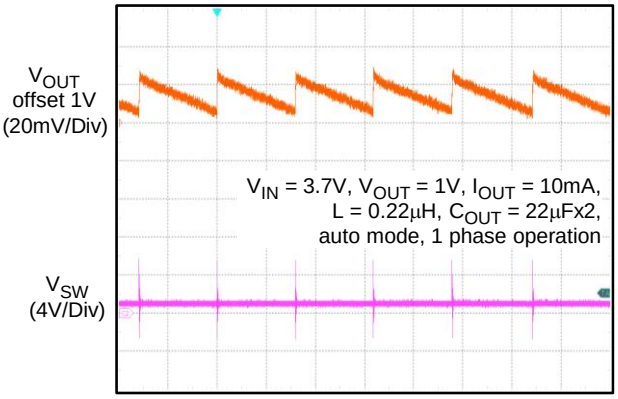
Time (10µs/Div)

Load Transient Response



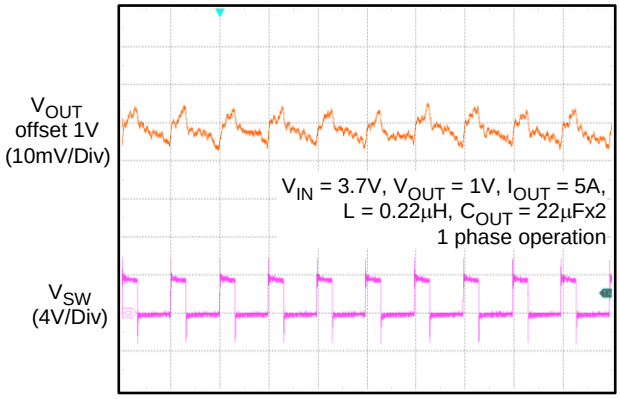
Time (10µs/Div)

Output Ripple Voltage



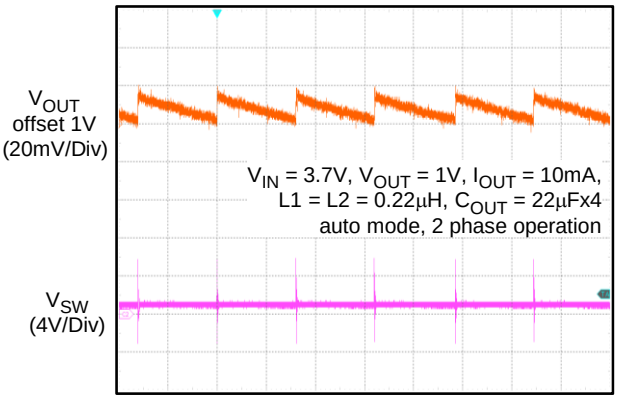
Time (40µs/Div)

Output Ripple Voltage



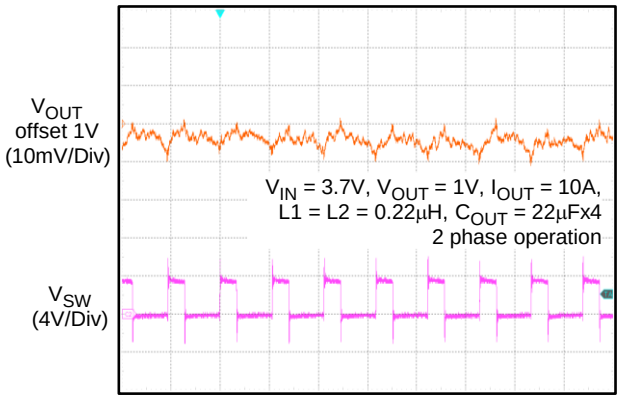
Time (500ns/Div)

Output Ripple Voltage



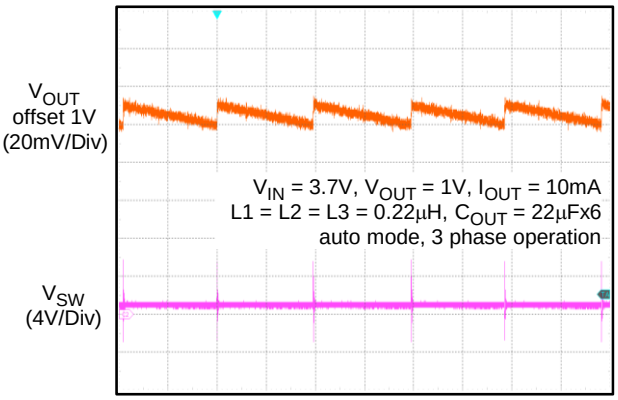
Time (40µs/Div)

Output Ripple Voltage



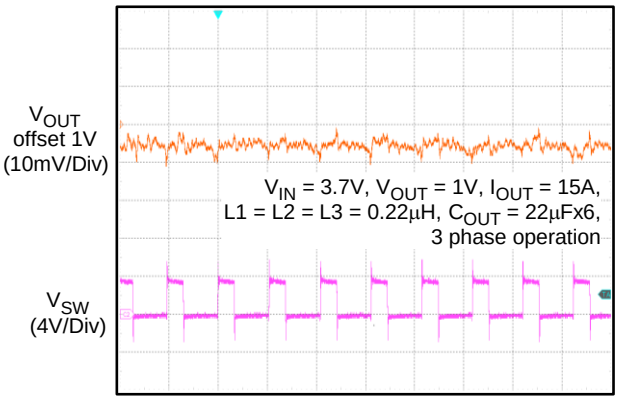
Time (500ns/Div)

Output Ripple Voltage



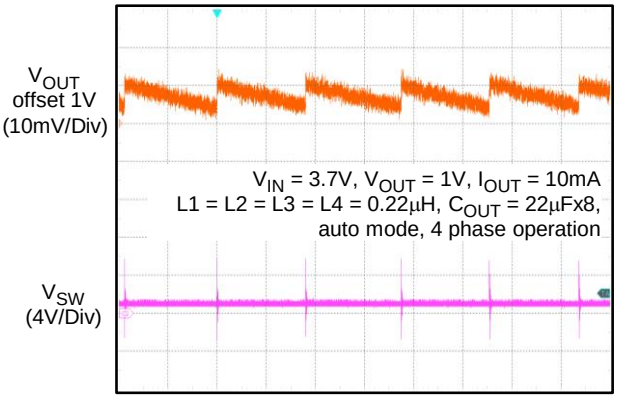
Time (40µs/Div)

Output Ripple Voltage



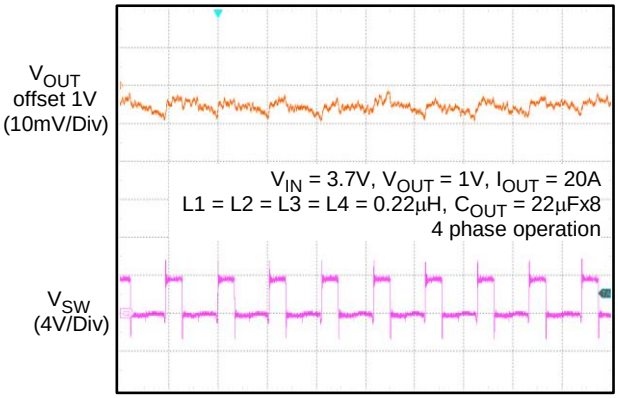
Time (500ns/Div)

Output Ripple Voltage



Time (40µs/Div)

Output Ripple Voltage



Time (500ns/Div)

17 Operation

The RTQ5756 series comprises power management ICs that integrate four high-efficiency buck converters. This series is factory configured as five different part options: RTQ5756A (2+1+1 phase), RTQ5756B (1+1+ 1+1 phase), RTQ5756C (3+1 phase), RTQ5756D (4-phase) and RTQ5756E (2+2 phase) converters. The converter is capable of providing up to 20A peak current with an output voltage range from 0.4V to 1.55V.

The RTQ5756 series utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small ceramic capacitors (MLCC) to save the PCB space.

During normal operation, the internal high-side power switch (HSFET) is activated for a predetermined duration determined by a one-shot timer at the start of each clock cycle. When the HSFET is deactivated, the internal low-side power switch (LSFET) is activated. The output voltage is remotely sensed at the VOUT pin and the RTN pin to ensure high accuracy and is compared to an internal reference voltage. As a result, an error signal is obtained and internally compensated. The compensated error signal is then compared to an internal ramp signal. Once the minimum off-time one-shot has elapsed and the inductor current is below the current-limit threshold, the one-shot is triggered again if the internal ramp signal falls below the compensated error signal. The ACOT® control architecture is characterized by its ultrafast transient response. When there is a sudden increase in load, the output voltage rapidly drops, triggering a new on-time to increase the inductor current once again.

In multiphase operation, phase interleaving control is employed to minimize input and output ripple. This technique activates different phases in a cyclical fashion by applying a sequence of control pulses to the phase transistors. By doing so, the ripple in the input and output currents is reduced, resulting in improved performance and efficiency. Additionally, current balance control is utilized to ensure an equal distribution of stress on each phase. This control mechanism helps maintain balanced current flow among the different phases, preventing any phase from being overloaded or underutilized. The use of both phase interleaving control and current balance control enhances the overall performance and reliability of the multiphase system. The phase spacing of each switching stage in various multiphase configurations is as follows:

- In a 2-phase configuration, the phases are spaced 180º apart.
- In a 3-phase configuration, the phases are spaced 120º apart.
- In a 4-phase configuration, the phases are spaced 90º apart.

The RTQ5756 series features a four-phase buck converter, which is divided into four groups as outlined below:

- Group 1:
    1. Power stage: PVIN_D, SW_D, PGND_D
    2. Feedback and Control Pins: VOUT1, RTN1 and VSEL1
    3. I^2C registers named Buck1: 0x14, 0x25[4], 0x33, 0x37, 0x3E~0x57
- Group 2:
    1. Power stage: PVIN_A, SW_A, PGND_A
    2. Feedback and Control Pins: VOUT2, RTN2 and VSEL2
    3. I^2C registers named Buck2: 0x15, 0x25[5], 0x34, 0x38, 0x5B~0x71
- Group 3:
    1. Power stage: PVIN_B, SW_B, PGND_B
    2. Feedback and Control Pins: VOUT3, RTN3 and VSEL3
    3. I^2C registers named Buck3: 0x16, 0x25[6], 0x35, 0x39, 0x75~0x8B
- Group 4:

1. Power stage: PVIN_C, SW_C, PGND_C
2. Feedback and Control Pins: VOUT4, RTN4 and VSEL4
3. I^2C registers named Buck4: 0x17, 0x25[7], 0x36, 0x3A, 0x8F~0xA5

To ensure the proper operation of the converter, the circuit diagram is defined, and the control register is assigned based on the output configuration. When the RTQ5756 is configured for multiphase output, master and slave control is implemented. In the case where the selected group functions as a slave, the feedback pins (VOUTx and RTNx), VSESW pin, and the corresponding I^2C control registers (Buckx) are not utilized and should be connected to GND.

Taking the RTQ5756C as an example, it consists of two output channels. For V_{OUT1}, the output voltage is sensed from the output capacitor through VOUT1 and RTN1 pins, with the phase nodes employed being SW_D (master), SW_C, and SW_B in the specified multiphase control order. The active control registers for this setup are Buck1. Similarly, for V_{OUT2}, the output voltage is sensed from the output capacitor through VOUT2 and RTN2 pins, with the employed phase node being SW_A, and the active control registers being Buck2.

The output configuration setups based on the RTQ5756 part options are detailed in Table 6.

Table 6. Output Configuration Setup

Part No.	Output Channel	Phase Sequence Assignment	Output Voltage Sense Pin	VSEL Pin Control	Active Control Registers
RTQ5756A	V_{OUT1}	SW_D (master), SW_C	VOUT1, RTN1	VSEL1	Buck1
	V_{OUT2}	SW_A	VOUT2, RTN2	VSEL2	Buck2
	V_{OUT3}	SW_B	VOUT3, RTN3	VSEL3	Buck3
RTQ5756B	V_{OUT1}	SW_D	VOUT1, RTN1	VSEL1	Buck1
	V_{OUT2}	SW_A	VOUT2, RTN2	VSEL2	Buck2
	V_{OUT3}	SW_B	VOUT3, RTN3	VSEL3	Buck3
	V_{OUT4}	SW_C	VOUT4, RTN4	VSEL4	Buck4
RTQ5756C	V_{OUT1}	SW_D (master), SW_C, SW_B	VOUT1, RTN1	VSEL1	Buck1
	V_{OUT2}	SW_A	VOUT2, RTN2	VSEL2	Buck2
RTQ5756D	V_{OUT1}	SW_D (master), SW_C, SW_B, SW_A	VOUT1, RTN1	VSEL1	Buck1
RTQ5756E	V_{OUT1}	SW_D (master), SW_C	VOUT1, RTN1	VSEL1	Buck1
	V_{OUT2}	SW_A (master), SW_B	VOUT2, RTN2	VSEL2	Buck2

17.1 UVLO, Enable Control and Soft-Start

The RTQ5756 series implements undervoltage-lockout protection (UVLO) to prevent operation without fully turning on the internal HSFET and LSFET. The UVLO monitors the voltage of AVIN. When the AVIN voltage is lower than the UVLO threshold, the IC stops switching and resets all digital functions.

The RTQ5756 series provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{ENL}) of the enable input (EN), the converter will enter shutdown mode and reset all digital functions (I^2C). Then the converter is disabled even if the VIN voltage is above the VIN undervoltage-lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (10μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}), the device starts switching. When appropriate voltages are present on the VIN, AVIN, VIO and EN pins, the RTQ5756 series will begin digital functions, switching, and initiate a soft-start ramp of the output voltage. The boot time for the device to implement

soft-start approximately 270μs (typical) when both the input voltage and EN voltage are above UVLO and EN rising threshold. After the device completes the boot process, it takes 500μs (typical) for the I²C interface circuit to settle. It is advisable to enable the device only after the VIO voltage has stabilized, as the VIO voltage serves as the power supply for digital functions. The RTQ5756 series supports enable/shutdown delay time setting (factory setting, default = 0ms) and soft-start slew rate setting. The soft-start function is used to prevent large inrush current while the converter is powered up. The soft-start time of each buck is programmable through registers 0x55[5:4], 0x6F[5:4], 0x89[5:4], and 0xA3[5:4].

Figure 1 and Figure 2 show the start-up and power-off sequence with enable control by software EN. The output voltage is disabled or enabled by setting the following registers: 0x49[0] and 0x4B[0] (Buck1), 0x63[0] and 0x65[0] (Buck2), 0x7D[0] and 0x7F[0] (Buck3), 0x97[0] and 0x99[0] (Buck4). The RTQ5756 series also implements enable control by the external EN pin with enable and shutdown delay time. Note that enable delay time is factory setting only, and the default value of Buck1 to Buck4 can be read from the following registers: 0x56[5:0], 0x70[5:0], 0x8A[5:0] and 0xA4[5:0]. As for shutdown delay time, it can be either factory programmed or set by software, and the default value of Buck1 to Buck4 can be read from the following registers: 0x57[5:0], 0x71[5:0], 0x8B[5:0], and 0xA5[5:0]. The start-up and power-off sequences by external EN pin are shown in Figure 3 and Figure 4.

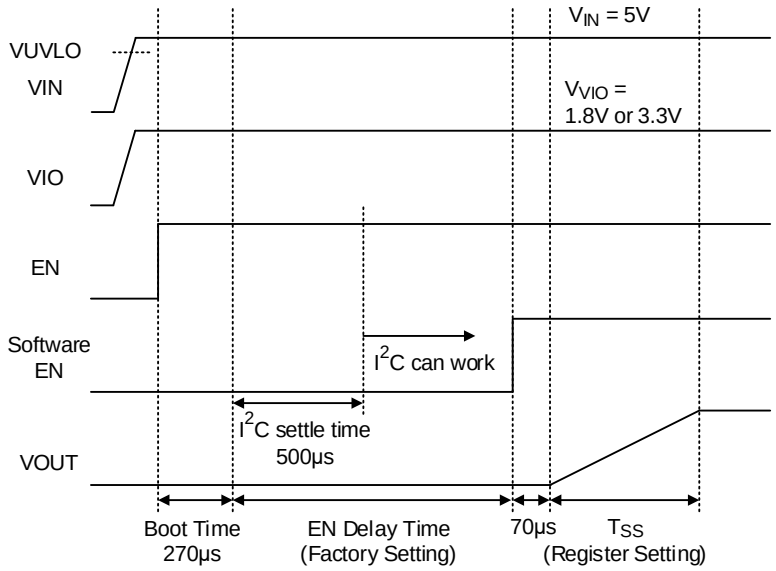


Figure 1. Start-Up Sequence by Software EN

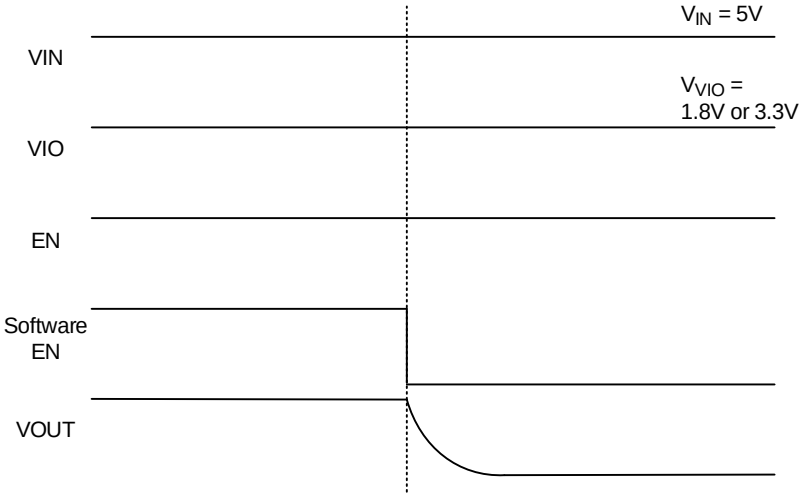


Figure 2. Power-Off Sequence by Software EN

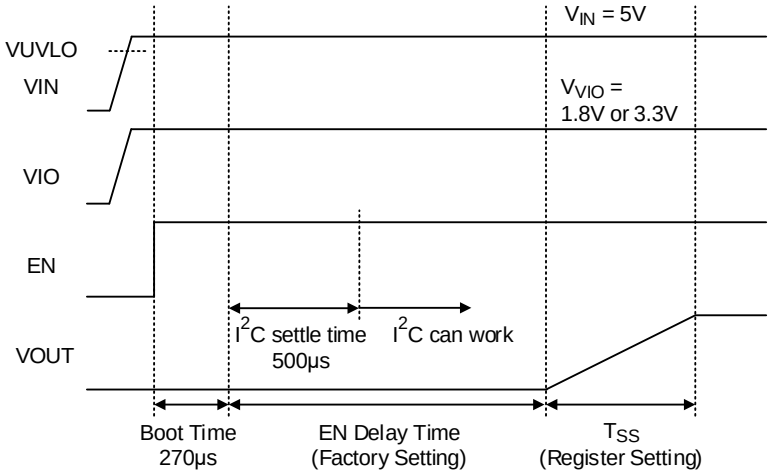


Figure 3. Start-Up Sequence by External EN Pin

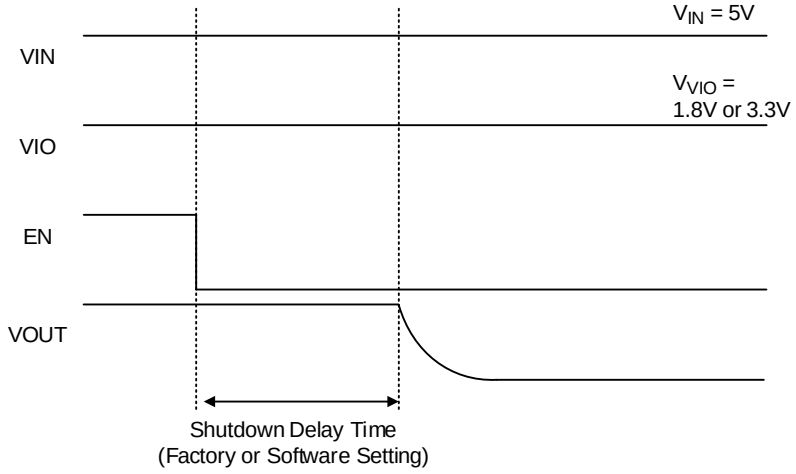


Figure 4. Power-Off Sequence by External EN Pin

17.2 Dynamic Voltage Scaling (DVS)

The RTQ5756 series offers a wide output voltage range with 8-bit resolution, and each buck converter features two independently programmable voltage settings known as DVS0 and DVS1. Taking Buck1 as an example, register 0x48[8:0] is utilized to set the voltage of DVS0, while 0x4A[8:0] is used to set the voltage of DVS1. There are two methods for selecting the DVS.

In the first method, the selection can be changed via software using register 0x52[1:0]. DVS0 can be controlled by setting 0x52[1:0] = 00, and DVS1 can be controlled by setting 0x52[1:0] = 01.

In the second method, the selection of the DVS can be controlled by an external hardware pin when setting 0x52[1:0] = 10. The VSEL pin plays this role, and its polarity is defined by 0x52[2]. When setting 0x52[2] = 0, pulling VSEL high uses DVS0, and pulling VSEL low uses DVS1. Conversely, when setting 0x52[2] = 1, pulling VSEL high uses DVS1, and pulling VSEL low uses DVS0. The output setting diagram is shown in Figure 5.

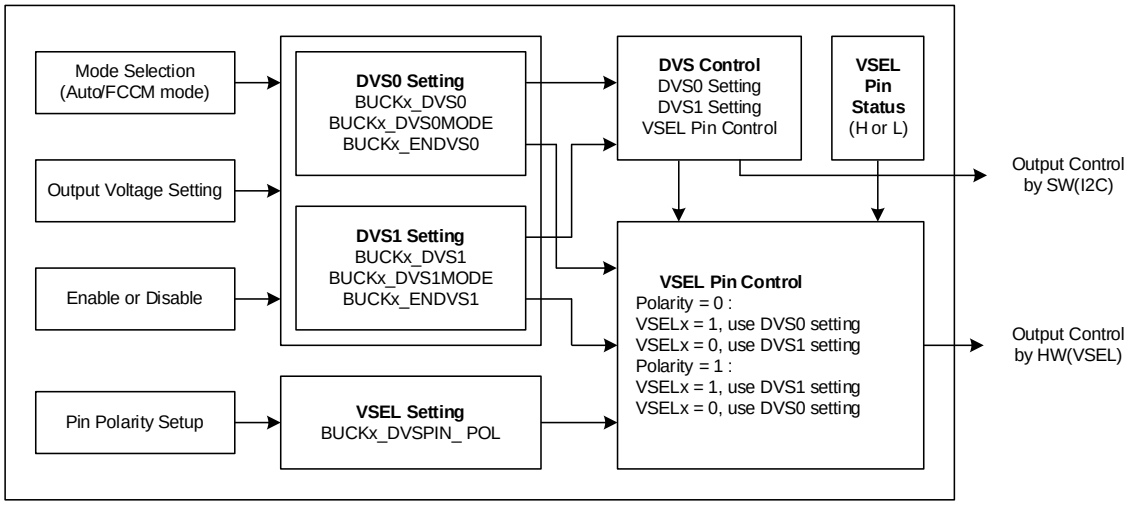


Figure 5. Output Setting Diagram

The RTQ5756 series also supports DVS speed configuration, regardless of the slew rate of voltage changes within the same DVSx or between DVS0 and DVS1. Take Buck1 for an example, when the output voltage is set from low to high or high to low, register 0x54[6:4] defines the slew rate of DVS up, while 0x54[2:0] is used to define the slew rate of DVS down. In order to have better performance during voltage changes operations, the master/slave enters PWM operation and maintains it for 100μs after the voltage achieves the target, even if the IC is set to Auto mode. Besides, set the output voltage down to the target voltage within 123% of the internal reference voltage to avoid OVP triggered when DVS down with decay mode. Figure 6 and Figure 7 show the DVS up and down operations.

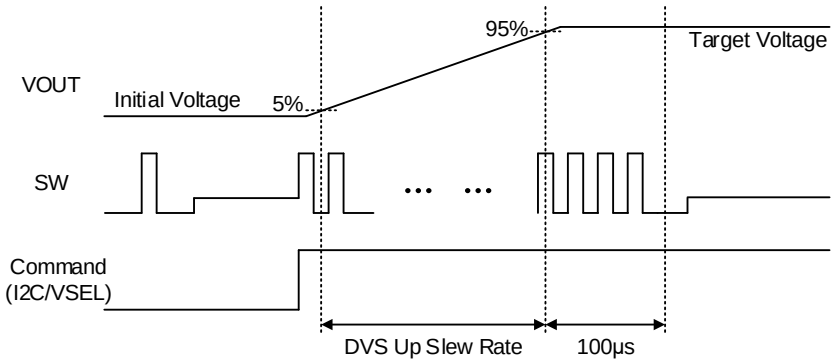


Figure 6. DVS Up Operation

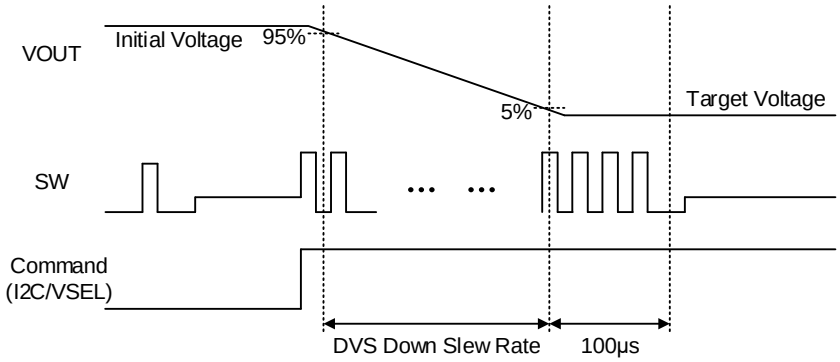


Figure 7. DVS Down Operation

17.3 MODE Selection

The operation modes, whether DVS0 or DVS1, encompass two distinct configurations: forced continuous conduction mode (FCCM) and automatic power saving mode (Auto mode). These modes are configured using specific registers as follows: 0x49[5] and 0x4B[5] for Buck1, 0x63[5] and 0x65[5] for Buck2, 0x7D[5] and 0x7F[5] for Buck3, and 0x97[5] and 0x99[5] for Buck4. For instance, to set Buck1 to FCCM, a value of "1" should be written at 0x49[5].

When Auto mode operation is selected, the RTQ5756 series automatically adjusts the switching frequency at light-load conditions to maintain high efficiency. This is achieved by enabling the internal zero current detection circuitry to sense the inductor current using the LSFET $R_{DS(ON)}$. As the inductor current decreases to zero and becomes negative, both HSFET and LSFET are turned off, and the output capacitor supplies the load current until the feedback voltage falls below the internal reference voltage. Moreover, the switching frequency increases to 2MHz/2.2MHz as the inductor current reaches the continuous conduction condition.

By setting the MODE to FCCM operation, the internal zero current detection circuitry is disabled, and full phase switching is enforced. This ensures that the switching frequency remains relatively constant to meet stringent voltage regulation accuracy requirements.

17.4 Automatically Phase Adding/Shedding

In a multiphase converter, the phase adding/shedding function is designed to optimize power efficiency based on the output current. The RTQ5756 series, which features a multiphase configuration, automatically increases the number of operating phases as the output current rises by setting the MODE to Auto mode operation. The phase interleaving function is automatically fine-tuned to correspond with the active phase count, scaling with the output current. For example, in the RTQ5756C (3-phase), an additional phase is seamlessly integrated and interleaved at 180-degree intervals when the load current exceeds the phase adding level from 1 phase to 2 phases. Conversely, when the load current drops below the phase shedding level, transitioning from 2 phases to 1 phase, the device autonomously reduces the number of operating phases.

17.5 Power Good Indication

The RTQ5756 series provides a power good indication to show the output voltage status. When the output voltage is between 110% and 90% of the setting voltage, the power good indication bit changes to “1”. The relative registers are 0x14[7], 0x15[7], 0x16[7] and 0x17[7].

17.6 Watchdog Function

The RTQ5756 series implements a watchdog function which resets the output voltage, DVSx, and ENDVSx registers to the factory default setting value. Register 0x25 can enable or disable the watchdog function and provide watchdog timeout for selection. The minimum watchdog debounce time is 100μs when 0x25[2:0] is set to 000. The operation of the watchdog reset is shown in Figure 8. Table 7 shows the registers that will be reset when the WDOG_RST pin is pulled low. The I^2C command needs to be given after the WDOG_RST pin is pulled high.

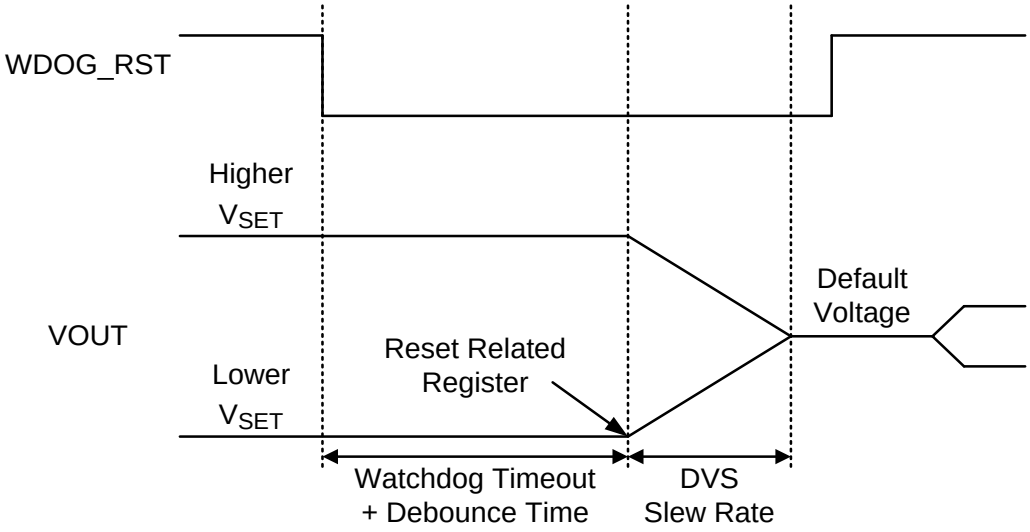


Figure 8. Watchdog Reset Operation

Table 7. Watchdog Reset Register

BUCK1_WDT	BUCK2_WDT	BUCK3_WDT	BUCK4_WDT
0x48	0x62	0x7C	0x96
0x49[0]	0x63[0]	0x7D[0]	0x97[0]
0x4A	0x64	0x7E	0x98
0x4B[0]	0x65[0]	0x7F[0]	0x99[0]
0x52	0x6C	0x86	0xA0

17.7 Fault Detection and Interrupt Pin

The RTQ5756 series implements an interrupt function to alert the host when a warning or a fault event has occurred. The warning events are VIN UVLO and Hot Die, and the fault events include the conditions such as overvoltage, undervoltage, overcurrent, and over-temperature. Registers 0x13, 0x14, 0x15, 0x16, and 0x17 can help the host to determine if a fault or warning event has occurred. These registers will be cleared when read. Moreover, the device provides an INT pin with open-drain output capability (default factory setting) to show these events using an active-low signal. The pull-high voltage of the INT pin will be the same as the VIO voltage. The RTQ5756 series also supports a mask function to either mask or pass the internal event flag output to the external INT pin using 0x32, 0x33, 0x34, 0x35, and 0x36 registers. The overall detection function is shown in Figure 9.

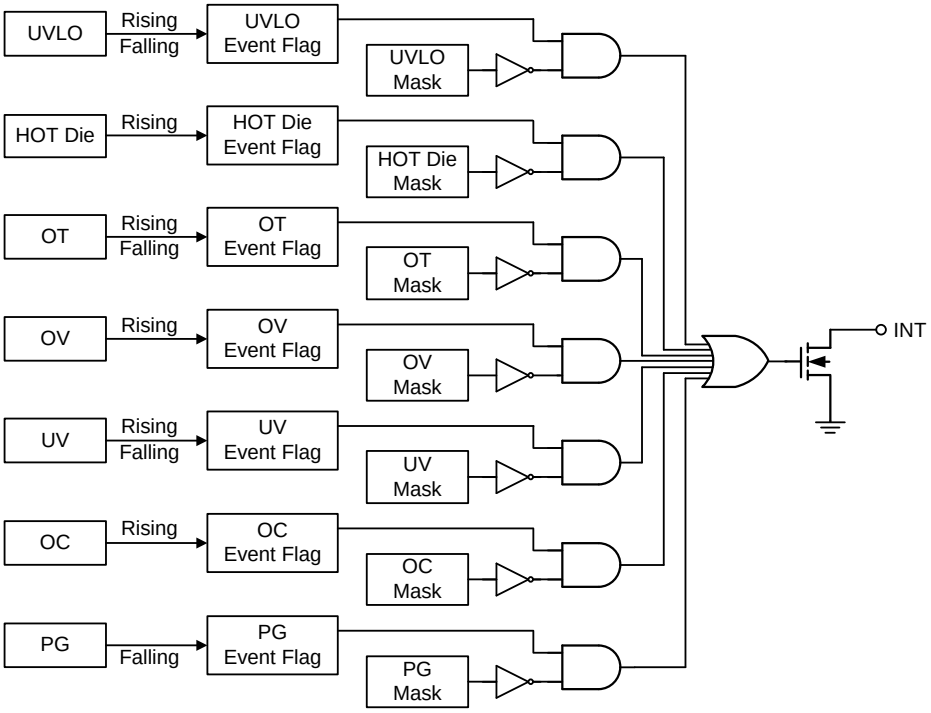


Figure 9. Overall Detection Function

17.8 Current-Limit Protection

The RTQ5756 series features cycle-by-cycle current-limit protection on both the HSFET and LSFET to prevent the device from catastrophic damage in the event of output short-circuit, overcurrent, or inductor saturation conditions.

The HSFET current-limit protection is achieved by an internal current comparator that monitors the inductor current during each on-time. The inductor current is compared with the HSFET peak-current limit (I_{LIM_H}) after a certain amount of delay time when the HSFET is turned on in each cycle. If the peak inductor current rises above the HSFET peak current limit (I_{LIM_H}), the converter will immediately turn off the HSFET and turn on the LSFET to prevent the inductor current from exceeding the HSFET current limit.

The LSFET current-limit protection is achieved by measuring the inductor current during LSFET on-time. Once the inductor current rises above the LSFET valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited, and the next on-time will only be triggered when the inductor current falls below the LSFET valley current limit (I_{LIM_L}). If the output load current exceeds the available inductor current (clamped by the LSFET valley current limit), the output capacitor will need to supply the extra current, so that the output voltage will begin to drop. If it drops below the output undervoltage protection trip threshold, the IC will stop switching to avoid excessive heating.

17.9 Output Undervoltage Protection

The RTQ5756 series includes output undervoltage protection (UVP) against overload or short-circuit conditions by constantly monitoring the output voltage V_{OUT}. If V_{OUT} drops below the undervoltage protection trip threshold (typically 50% of the internal reference voltage), both the HSFET and LSFET will stop switching. Register 0x37[3], 0x38[3], 0x39[3], and 0x3A[3] can be used to select hiccup or latch protection behavior of each buck converter when the converter is in a UV condition. For hiccup behavior, both the HSFET and LSFET remain in a low state for 1ms, and then the IC starts to switch. If the output voltage is not greater than the UV threshold after the internal soft-start end signal is triggered, both the HSFET and LSFET will still keep low state again for the next cycle. When each buck is set to latch mode, UVP will let the converter enter shutdown mode unless resetting the IC by the external EN pin or by falling to the UVLO low threshold.

17.10 Output Overvoltage Protection

The RTQ5756 series supports output overvoltage protection (OVP) by constantly monitoring the output voltage V_{OUT}. If V_{OUT} exceeds above the overvoltage protection trip threshold (typically 133% of the internal reference voltage), the HSFET and LSFET will not turn on until the output voltage is lower than the overvoltage protection recovery threshold (typically 125% of the internal reference voltage).

17.11 Over-Temperature Protection

The RTQ5756 series includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP shuts down the switching operation when the junction temperature exceeds the over-temperature protection threshold (T_{OTP}). Once the junction temperature cools down by the over-temperature protection hysteresis (T_{OTP_HYS}), the IC resumes normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

17.12 Negative Overcurrent Limit (FCCM Only)

The RTQ5756 series can operate in FCCM and allows for negative current operation. During PWM operation, a high negative current may be generated if an external power source is unexpectedly connected to the output terminal. As the risk described above, the internal circuit monitors the negative current during each on-time interval of the LSFET and compares it with the NOC threshold. If the negative current exceeds the NOC threshold, the LSFET is turned off immediately, and then the HSFET will be turned on to discharge the energy from the output inductor. This behavior can keep the valley of the negative current at the NOC threshold to protect the LSFET. However, the negative current cannot be limited to the NOC threshold anymore once the minimum off-time is reached.

18 Application Information

(Note 13)

The RTQ5756 series consists of power management ICs that integrate four high-efficiency buck converters. These series are factory configured as five different part options: RTQ5756A (2+1+1 phase), RTQ5756B (1+1+1+1 phase), RTQ5756C (3+1 phase), RTQ5756D (4-phase) and RTQ5756E (2+2 phase) converters.

18.1 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current, but it still depends on size considerations. The inductor used in the typical application circuit of the datasheet is recommended. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

To enhance efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits within the allotted dimensions. The selected inductor should have a saturation current rating greater than the peak current limit of the device. The core must be large enough to avoid saturation at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating that is equal to or greater than the device switch current limit, rather than just the peak inductor current.

18.2 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the HSFET. The C_{IN} should be sized to accomplish this without causing a large variation in input voltage. Several capacitors may also be paralleled to meet the size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The input capacitor should be placed as close as possible to each VIN pin with a low inductance connection to the PGND of the IC. It is recommended to connect capacitors between the VIN pin and the PGND pin for a 2MHz/2.2MHz switching frequency as shown in the typical application circuit. The larger input capacitance is required when a lower switching frequency is used. The X7R capacitors are recommended for best performance across temperature and input voltage variations.

18.3 Output Capacitor Selection

The selection of C_{OUT} is determined by the need to satisfy the voltage ripple and the transient loads. The peak-to-peak output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times C_{OUT} \times F_{SW}} \right)$$

where the ΔI_L is the peak-to-peak inductor ripple current. The highest output ripple is at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The X7R dielectric capacitor is recommended for the best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage, and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated values when used near their rated voltage.

Transient performance can be improved with a higher value output capacitor. Increasing the output capacitance will also decrease the output voltage ripple.

The recommended output capacitors are shown in Typical Application Circuit.

18.4 Thermal Considerations

In many applications, the RTQ5756 series does not generate significant heat due to its high efficiency and the low thermal resistance of its WL-CSP-54B 2.69x3.92 (BSC) package. However, in applications where the device runs at high ambient temperatures, high input voltages, or high switching frequencies, the generated heat may exceed the maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 160°C, the RTQ5756 series will stop switching the power MOSFETs until the temperature cools down by 40°C.

The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

where

$T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 125°C. T_A is the ambient operating temperature, and $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. This can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply setting $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

From the efficiency measurement, the power loss of system can be found, and the below formula can be used to determine the power loss of the IC by removing the loss of the inductor, including DC loss and AC loss.

4-phase converter power loss:

$$P_{loss} = (V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT}) - \left(\frac{I_{OUT}}{4}\right)^2 \times DCR \times 4 - P_{core\_loss} \times 4 - \left(\frac{V_{OUT}^2 \times ACR}{12 \times L^2 \times f_{SW}^2}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)^2 \times 4$$

where

P_{core_loss} and ACR need to be obtained from the inductor supplier

The total loss of the IC cannot be larger than the maximum power loss. If the application requires a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18.5 Layout Guidelines

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the RTQ5756 series:

- A Four-layer or six-layer PCB with a maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high-frequency decoupling capacitor as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place multiple vias under the device near PVIN and PGND and close to input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add at least 40 thermal vias under and near the device to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW, should be as small as possible. Keep analog components away from the SW node.
- Reduce the area size of the SW exposed copper to reduce electrical coupling from this voltage.
- Connect the feedback sense network behind the via of the output capacitor.
- Connect all analog grounds to the common node and then connect the common node to the power ground with a single point.

Figure 10 and Figure 11 show the layout examples for the RTQ5756B and RTQ5756D, respectively.

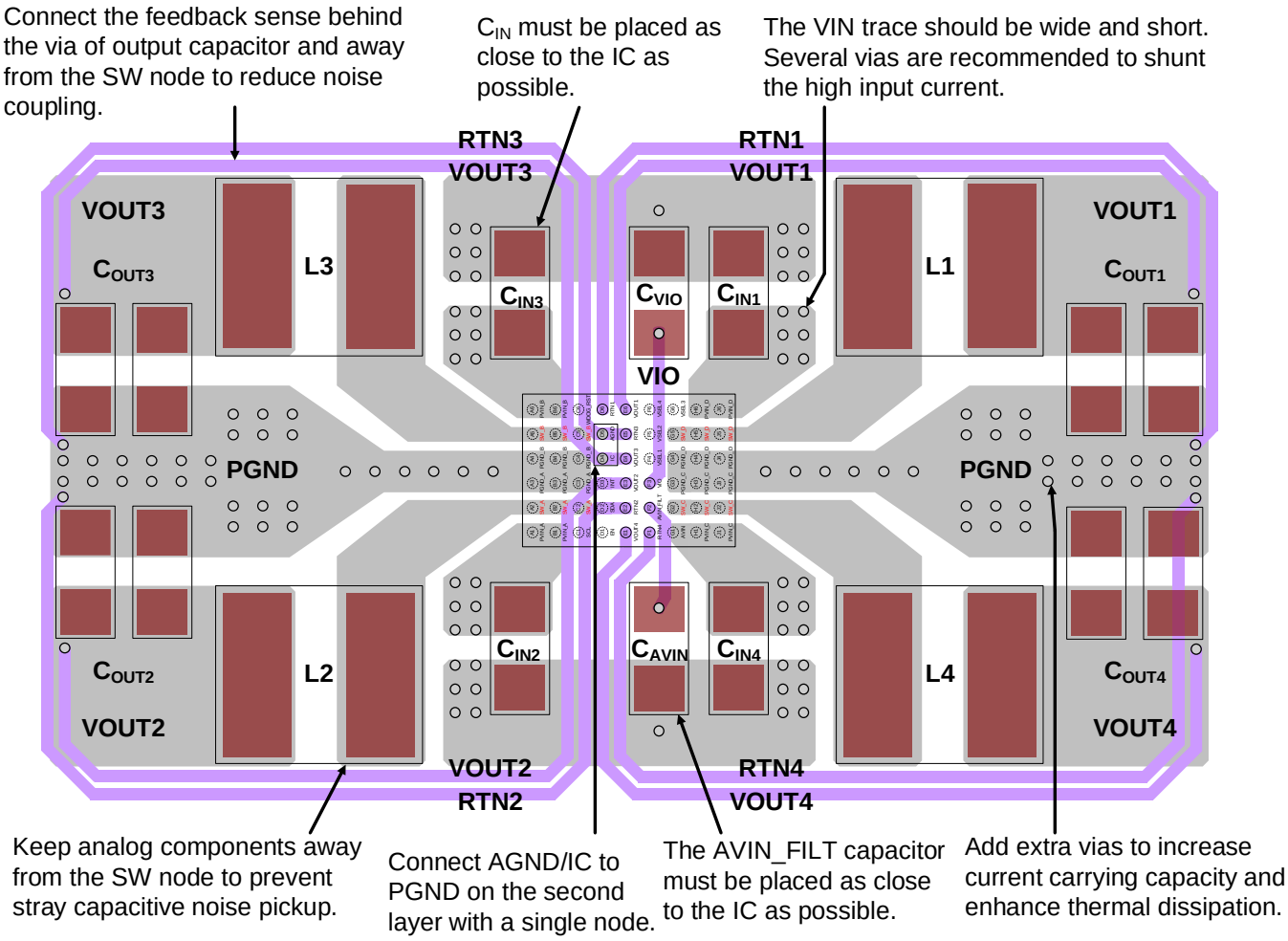


Figure 10. RTQ5756B Layout Guideline

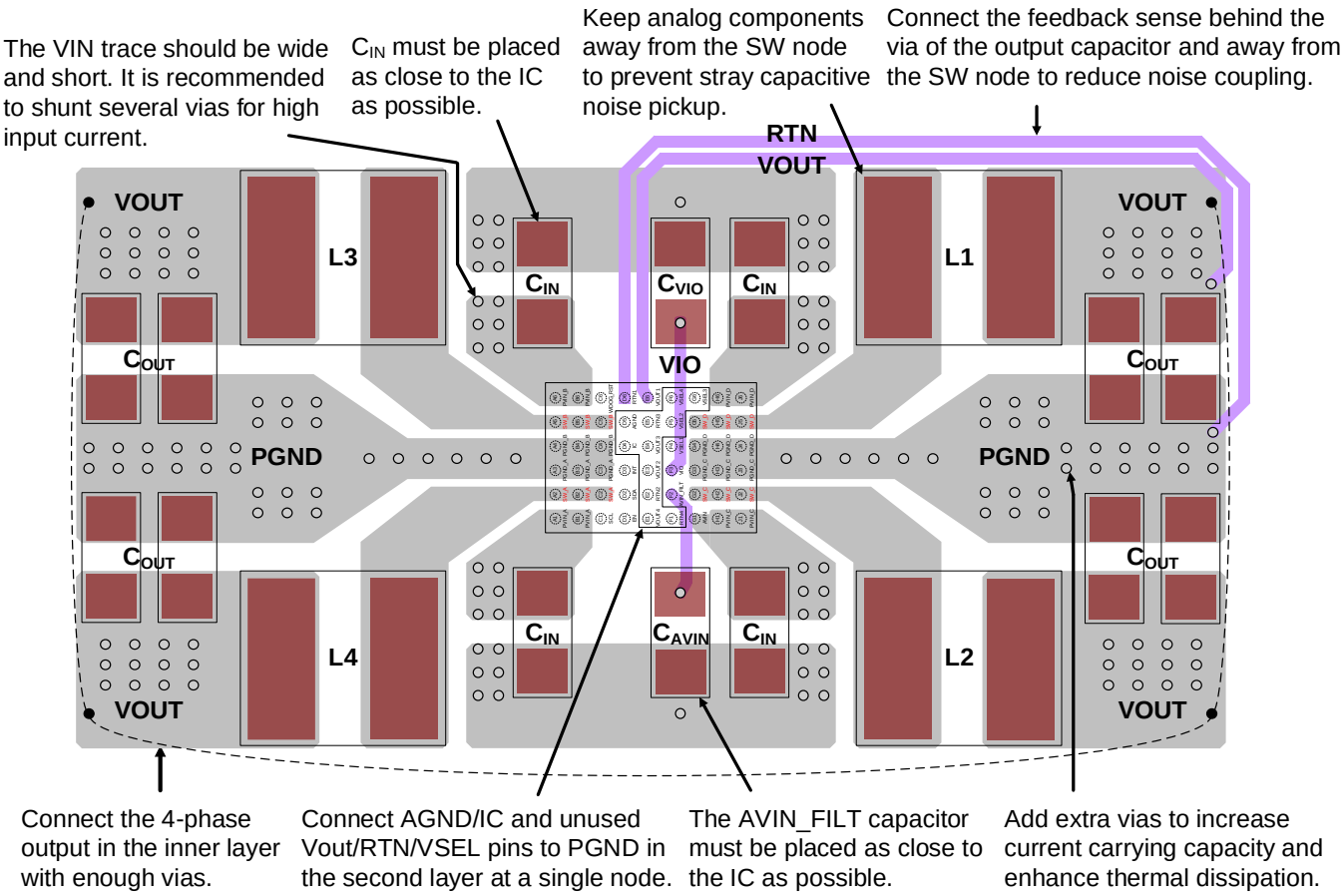


Figure 11. RTQ5756D Layout Guideline

18.6 I²C Interface

The RTQ5756 series utilizes the I²C interface for configuring various settings such as output voltage, Dynamic Voltage Scaling (DVS) slew rate, mode selection, VSEL function setting, and more. The register map provides details on each function's register and how to utilize these functions effectively.

It is important to note that the I²C interface can only execute read/write commands when the digital power (VIO) is operational and the converter boot process has been completed (ensuring that the input voltage and EN voltage are above the UVLO and EN rising threshold). Additionally, the I²C slave ID for the RTQ5756 series is pre-configured by the factory and ranges from 0x18 to 0x1F.

The RTQ5756 series supports fast mode (a bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown in Figure 12.

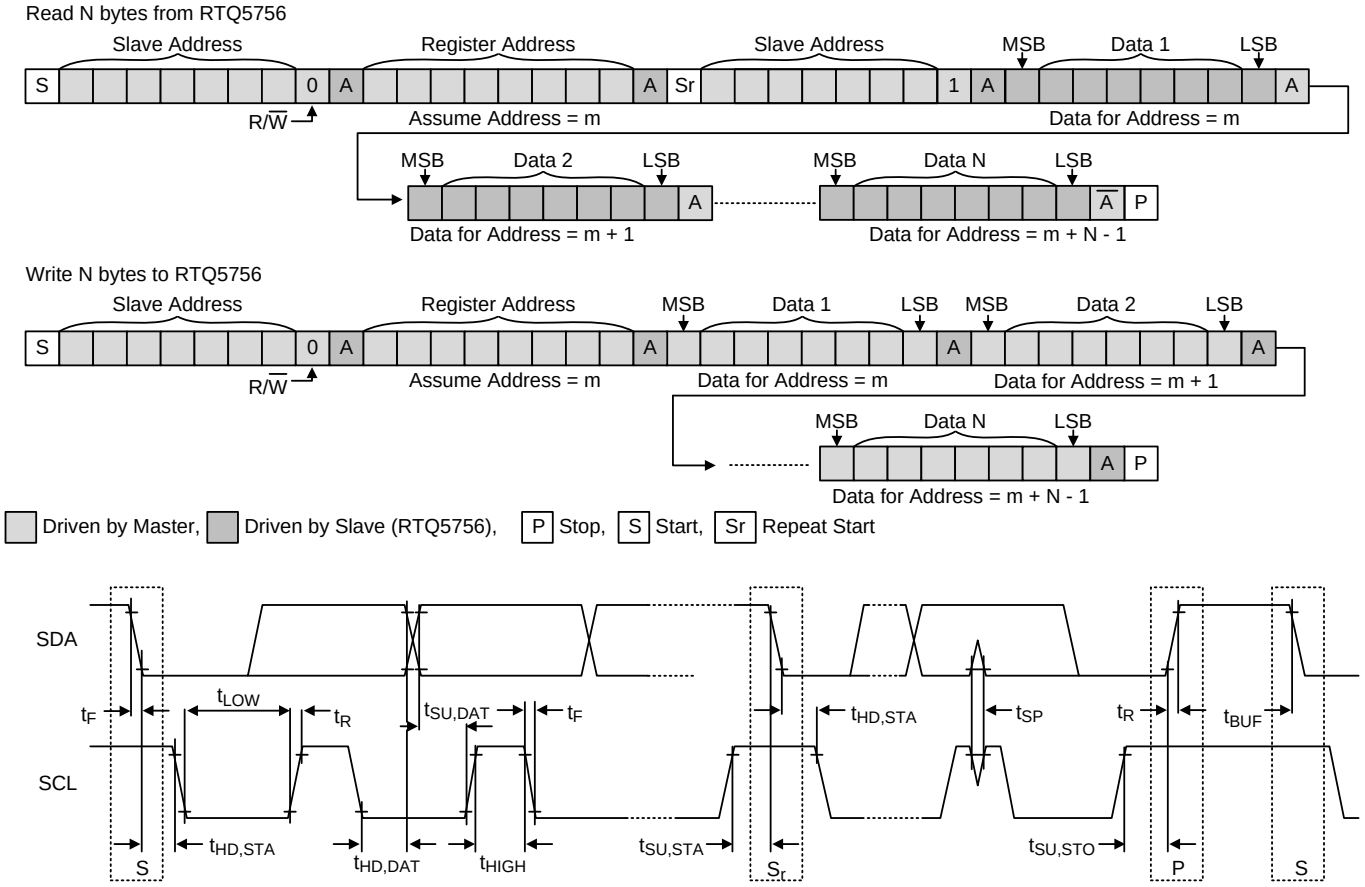


Figure 12. I²C Read and Write Stream and Timing Diagram

The RTQ5756 series also supports High-speed mode (a bit rate up to 3.4Mb/s) with the access code 08H. Figure 13 and Figure 14 show the detailed transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode):

- START condition (S)
- 8-bit master code (00001xxx)
- Not-acknowledge bit ($\overline{A}$)

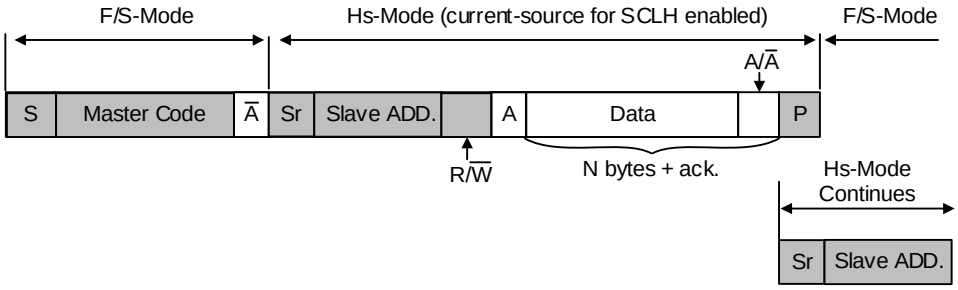


Figure 13. Data Transfer Format in Hs-Mode

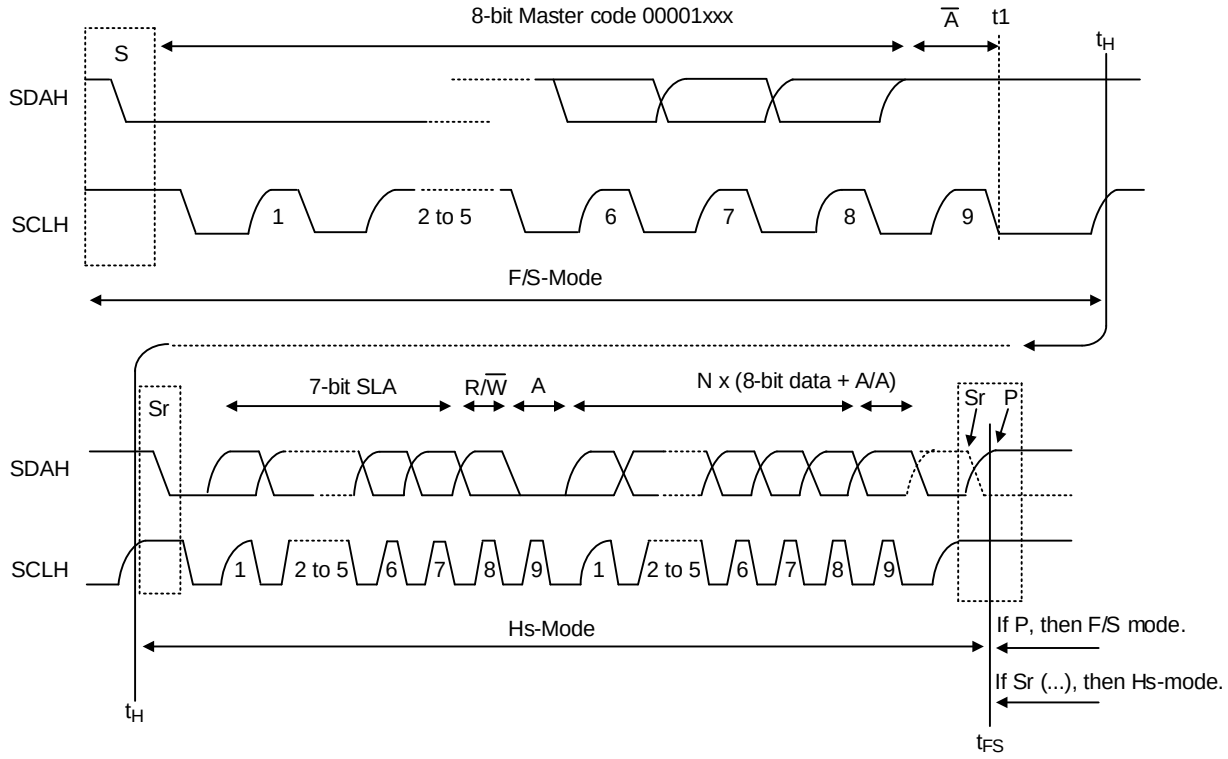


Figure 14. A Complete Hs-mode Transfer

Note 13. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Functional Register Description

Table 8. VOUT Setting

VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value
0.4	0x00	0.66	0x34	0.92	0x68	1.18	0x9C	1.58	0xD0
0.405	0x01	0.665	0x35	0.925	0x69	1.185	0x9D	1.59	0xD1
0.41	0x02	0.67	0x36	0.93	0x6A	1.19	0x9E	1.6	0xD2
0.415	0x03	0.675	0x37	0.935	0x6B	1.195	0x9F	1.61	0xD3
0.42	0x04	0.68	0x38	0.94	0x6C	1.2	0xA0	1.62	0xD4
0.425	0x05	0.685	0x39	0.945	0x6D	1.205	0xA1	1.63	0xD5
0.43	0x06	0.69	0x3A	0.95	0x6E	1.21	0xA2	1.64	0xD6
0.435	0x07	0.695	0x3B	0.955	0x6F	1.215	0xA3	1.65	0xD7
0.44	0x08	0.7	0x3C	0.96	0x70	1.22	0xA4	1.66	0xD8
0.445	0x09	0.705	0x3D	0.965	0x71	1.225	0xA5	1.67	0xD9
0.45	0x0A	0.71	0x3E	0.97	0x72	1.23	0xA6	1.68	0xDA
0.455	0x0B	0.715	0x3F	0.975	0x73	1.235	0xA7	1.69	0xDB
0.46	0x0C	0.72	0x40	0.98	0x74	1.24	0xA8	1.7	0xDC
0.465	0x0D	0.725	0x41	0.985	0x75	1.245	0xA9	1.71	0xDD
0.47	0x0E	0.73	0x42	0.99	0x76	1.25	0xAA	1.72	0xDE
0.475	0x0F	0.735	0x43	0.995	0x77	1.255	0xAB	1.73	0xDF
0.48	0x10	0.74	0x44	1	0x78	1.26	0xAC	1.74	0xE0
0.485	0x11	0.745	0x45	1.005	0x79	1.265	0xAD	1.75	0xE1
0.49	0x12	0.75	0x46	1.01	0x7A	1.27	0xAE	1.76	0xE2
0.495	0x13	0.755	0x47	1.015	0x7B	1.275	0xAF	1.77	0xE3
0.5	0x14	0.76	0x48	1.02	0x7C	1.28	0xB0	1.78	0xE4
0.505	0x15	0.765	0x49	1.025	0x7D	1.285	0xB1	1.79	0xE5
0.51	0x16	0.77	0x4A	1.03	0x7E	1.29	0xB2	1.8	0xE6
0.515	0x17	0.775	0x4B	1.035	0x7F	1.295	0xB3	1.81	0xE7
0.52	0x18	0.78	0x4C	1.04	0x80	1.3	0xB4	1.82	0xE8
0.525	0x19	0.785	0x4D	1.045	0x81	1.31	0xB5	1.83	0xE9
0.53	0x1A	0.79	0x4E	1.05	0x82	1.32	0xB6	1.84	0xEA
0.535	0x1B	0.795	0x4F	1.055	0x83	1.33	0xB7	1.85	0xEB
0.54	0x1C	0.8	0x50	1.06	0x84	1.34	0xB8	1.86	0xEC
0.545	0x1D	0.805	0x51	1.065	0x85	1.35	0xB9	1.87	0xED
0.55	0x1E	0.81	0x52	1.07	0x86	1.36	0xBA	1.88	0xEE
0.555	0x1F	0.815	0x53	1.075	0x87	1.37	0xBB	1.89	0xEF

VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value	VOUT (V)	Value
0.56	0x20	0.82	0x54	1.08	0x88	1.38	0xBC	1.9	0xF0
0.565	0x21	0.825	0x55	1.085	0x89	1.39	0xBD	1.91	0xF1
0.57	0x22	0.83	0x56	1.09	0x8A	1.4	0xBE	1.92	0xF2
0.575	0x23	0.835	0x57	1.095	0x8B	1.41	0xBF	1.93	0xF3
0.58	0x24	0.84	0x58	1.1	0x8C	1.42	0xC0	1.94	0xF4
0.585	0x25	0.845	0x59	1.105	0x8D	1.43	0xC1	1.95	0xF5
0.59	0x26	0.85	0x5A	1.11	0x8E	1.44	0xC2	1.96	0xF6
0.595	0x27	0.855	0x5B	1.115	0x8F	1.45	0xC3	1.97	0xF7
0.6	0x28	0.86	0x5C	1.12	0x90	1.46	0xC4	1.98	0xF8
0.605	0x29	0.865	0x5D	1.125	0x91	1.47	0xC5	1.99	0xF9
0.61	0x2A	0.87	0x5E	1.13	0x92	1.48	0xC6	2	0xFA
0.615	0x2B	0.875	0x5F	1.135	0x93	1.49	0xC7	2.01	0xFB
0.62	0x2C	0.88	0x60	1.14	0x94	1.5	0xC8	2.02	0xFC
0.625	0x2D	0.885	0x61	1.145	0x95	1.51	0xC9	2.03	0xFD
0.63	0x2E	0.89	0x62	1.15	0x96	1.52	0xCA	2.04	0xFE
0.635	0x2F	0.895	0x63	1.155	0x97	1.53	0xCB	2.05	0xFF
0.64	0x30	0.9	0x64	1.16	0x98	1.54	0xCC		
0.645	0x31	0.905	0x65	1.165	0x99	1.55	0xCD		
0.65	0x32	0.91	0x66	1.17	0x9A	1.56	0xCE		
0.655	0x33	0.915	0x67	1.175	0x9B	1.57	0xCF		

Table 9. Register List

Address	Register Name	Default	Type	Note
0x01	VENDOR ID	0x18	RO	All Devices
0x0F	IO_SOFTRESET	0x00	RW	All Devices
0x13	FLT_RECORDTEMP	0x00	RC	All Devices
0x14	FLT_RECORDBUCK1	0x00	RO, RC	All Devices
0x15	FLT_RECORDBUCK2	0x00	RO, RC	RTQ5756A/B/C/E
0x16	FLT_RECORDBUCK3	0x00	RO, RC	RTQ5756A/B
0x17	FLT_RECORDBUCK4	0x00	RO, RC	RTQ5756B
0x22	IO_I2CCFG	--	RO	All Devices Factory Setting
0x23	IO_INTCFG	0x08	RW	All Devices
0x25	IO_RSTDVS	0xF0	RW	All Devices
0x32	FLT_MASKTEMP	0x00	RW	All Devices
0x33	FLT_MASKBUCK1	0x00	RW	All Devices
0x34	FLT_MASKBUCK2	0x00	RW	RTQ5756A/B/C/E
0x35	FLT_MASKBUCK3	0x00	RW	RTQ5756A/B
0x36	FLT_MASKBUCK4	0x00	RW	RTQ5756B
0x37	FLT_BUCK1_CTRL	0x0C	RW	All Devices
0x38	FLT_BUCK2_CTRL	0x0C	RW	RTQ5756A/B/C/E
0x39	FLT_BUCK3_CTRL	0x0C	RW	RTQ5756A/B
0x3A	FLT_BUCK4_CTRL	0x0C	RW	RTQ5756B
0x3E	BUCK1_RAMP	0x44	RW	All Devices
0x48	BUCK1_DVS0CFG1	0x78	RW	All Devices
0x49	BUCK1_DVS0CFG0	0x20	RW	All Devices
0x4A	BUCK1_DVS1CFG1	0x78	RW	All Devices
0x4B	BUCK1_DVS1CFG0	0x20	RW	All Devices
0x52	BUCK1_DVSCFG	0x00	RW	All Devices
0x54	BUCK1_RSPCFG	0x14	RW	All Devices
0x55	BUCK1_SLEWCTRL	0x00	RW	All Devices
0x56	BUCK1_EN_DLY	0x00	RW	All Devices
0x57	BUCK1_SHUTDN_DLY	0x00	RW	All Devices
0x5B	BUCK2_RAMP	0x44	RW	RTQ5756A/B/C/E
0x62	BUCK2_DVS0CFG1	0x78	RW	RTQ5756A/B/C/E
0x63	BUCK2_DVS0CFG0	0x20	RW	RTQ5756A/B/C/E
0x64	BUCK2_DVS1CFG1	0x78	RW	RTQ5756A/B/C/E

Address	Register Name	Default	Type	Note
0x65	BUCK2_DVS1CFG0	0x20	RW	RTQ5756A/B/C/E
0x6C	BUCK2_DVSCFG	0x00	RW	RTQ5756A/B/C/E
0x6E	BUCK2_RSPCFG	0x14	RW	RTQ5756A/B/C/E
0x6F	BUCK2_SLEWCTRL	0x00	RW	RTQ5756A/B/C/E
0x70	BUCK2_EN_DLY	0x00	RW	RTQ5756A/B/C/E
0x71	BUCK2_SHUTDN_DLY	0x00	RW	RTQ5756A/B/C/E
0x75	Buck3_RAMP	0x44	RW	RTQ5756A/B
0x7C	Buck3_DVS0CFG1	0x78	RW	RTQ5756A/B
0x7D	Buck3_DVS0CFG0	0x20	RW	RTQ5756A/B
0x7E	Buck3_DVS1CFG1	0x78	RW	RTQ5756A/B
0x7F	Buck3_DVS1CFG0	0x20	RW	RTQ5756A/B
0x86	Buck3_DVSCFG	0x00	RW	RTQ5756A/B
0x88	Buck3_RSPCFG	0x14	RW	RTQ5756A/B
0x89	Buck3_SLEWCTRL	0x00	RW	RTQ5756A/B
0x8A	BUCK3_EN_DLY	0x00	RW	RTQ5756A/B
0x8B	BUCK3_SHUTDN_DLY	0x00	RW	RTQ5756A/B
0x8F	Buck4_RAMP	0x44	RW	RTQ5756B
0x96	Buck4_DVS0CFG1	0x78	RW	RTQ5756B
0x97	Buck4_DVS0CFG0	0x20	RW	RTQ5756B
0x98	Buck4_DVS1CFG1	0x78	RW	RTQ5756B
0x99	Buck4_DVS1CFG0	0x20	RW	RTQ5756B
0xA0	Buck4_DVSCFG	0x00	RW	RTQ5756B
0xA2	Buck4_RSPCFG	0x14	RW	RTQ5756B
0xA3	Buck4_SLEWCTRL	0x00	RW	RTQ5756B
0xA4	BUCK4_EN_DLY	0x00	RW	RTQ5756B
0xA5	BUCK4_SHUTDN_DLY	0x00	RW	RTQ5756B

Table 10. VENDOR ID

Address: 0x01								
Bit	7	6	5	4	3	2	1	0
Field	VENDOR ID							
Default	0	0	0	1	1	0	0	0
Type	RO							

Bit	Name	Description
7:0	VENDOR ID	VENDOR ID

Table 11. IO_SOFTRESET

Address: 0x0F								
Bit	7	6	5	4	3	2	1	0
Field	Reserved							IO_SOFTRESET
Default	0	0	0	0	0	0	0	0
Type	RV							RW

Bit	Name	Description
7:1	Reserved	Reserved bits
0	IO_SOFTRESET	Reset all digital functions to their default settings. 0: Not changed 1: Reset and bit cleared

Table 12. FLT_RECORDTEMP

Address: 0x13								
Bit	7	6	5	4	3	2	1	0
Field	FLT_UVLO	Reserved				FLT_HOTDIE	FLT_TEMPSDR	Reserved
Default	0	0	0	0	0	0	0	0
Type	RC	RV				RC	RC	RV

Bit	Name	Description
7	FLT_UVLO	Boot interrupt indicator. 0: Boot process has not occurred. AVIN is less than the UVLO rising threshold. 1: Boot process has occurred. AVIN is greater than the UVLO rising threshold (except for the first trigger) or less than the UVLO falling threshold.
6:3	Reserved	Reserved bits
2	FLT_HOTDIE	Hot die interrupt indicator. 0: Temperature of the die is lower than the threshold. 1: Die is hot. Temperature is above the threshold.
1	FLT_TEMPSDR	OT interrupt indicator. Read only and cleared when read. 0: No Fault. Temperature is below the threshold. 1: Fault. Temperature is above the threshold or has recovered after dropping below the threshold.
0	Reserved	Reserved bits

Table 13. FLT_RECORDBUCK1

Address: 0x14								
Bit	7	6	5	4	3	2	1	0
Field	BUCK1_PG	FLT_BUCK1_OC	FLT_BUCK1_OV	FLT_BUCK1_UV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RO	RC	RC	RC	RV			RV

Bit	Name	Description
7	BUCK1_PG	Power-good status indicator. 0: VOUT > 110% of the set VOUT or VOUT < 90% of the set VOUT 1: VOUT < 110% of the set VOUT and VOUT > 90% of the set VOUT
6	FLT_BUCK1_OC	OC interrupt indicator. Read only and cleared when read. 0: No Fault. Current is below the threshold. 1: Fault. Current is above the threshold.
5	FLT_BUCK1_OV	OV interrupt indicator. 0: No Fault. Voltage is below the threshold. 1: Fault. Voltage is above the threshold.
4	FLT_BUCK1_UV	UV interrupt indicator. 0: No Fault. Voltage is above the threshold. 1: Fault. Voltage is below the threshold or has recovered after being higher than the threshold.
3:0	Reserved	Reserved bits

Table 14. FLT_RECORDBUCK2

Address: 0x15								
Bit	7	6	5	4	3	2	1	0
Field	BUCK2_PG	FLT_BUCK2_OC	FLT_BUCK2_OV	FLT_BUCK2_UV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RO	RC	RC	RC	RV			RV

Bit	Name	Description
7	BUCK2_PG	Power-good status indicator. 0: VOUT > 110% of the set VOUT or VOUT < 90% of the set VOUT 1: VOUT < 110% of the set VOUT and VOUT > 90% of the set VOUT
6	FLT_BUCK2_OC	OC interrupt indicator. Read only and cleared when read. 0: No Fault. Current is below the threshold. 1: Fault. Current is above the threshold.
5	FLT_BUCK2_OV	OV interrupt indicator. 0: No Fault. Voltage is below the threshold. 1: Fault. Voltage is above the threshold.
4	FLT_BUCK2_UV	UV interrupt indicator. 0: No Fault. Voltage is above the threshold. 1: Fault. Voltage is below the threshold or has recovered after being higher than the threshold.
3:0	Reserved	Reserved bits

Table 15. FLT_RECORDBUCK3

Address: 0x16								
Bit	7	6	5	4	3	2	1	0
Field	BUCK3_PG	FLT_BUCK3_OC	FLT_BUCK3_OV	FLT_BUCK3_UV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RO	RC	RC	RC	RV			RV

Bit	Name	Description
7	BUCK3_PG	Power good status indicator. 0: VOUT > 110% of the set VOUT or VOUT < 90% of the set VOUT 1: VOUT < 110% of the set VOUT and VOUT > 90% of the set VOUT
6	FLT_BUCK3_OC	OC interrupt indicator. Read only and cleared when read. 0: No Fault. Current is below the threshold. 1: Fault. Current is above the threshold.
5	FLT_BUCK3_OV	OV interrupt indicator. 0: No Fault. Voltage is below the threshold. 1: Fault. Voltage is above the threshold.
4	FLT_BUCK3_UV	UV interrupt indicator. 0: No Fault. Voltage is above the threshold. 1: Fault. Voltage is below the threshold or has recovered after being higher than the threshold.
3:0	Reserved	Reserved bits

Table 16. FLT_RECORDBUCK4

Address: 0x17								
Bit	7	6	5	4	3	2	1	0
Field	BUCK4_PG	FLT_BUCK4_OC	FLT_BUCK4_OV	FLT_BUCK4_UV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RO	RC	RC	RC	RV			RV

Bit	Name	Description
7	BUCK4_PG	Power-good status indicator. 0: VOUT > 110% of the set VOUT or VOUT < 90% of the set VOUT 1: VOUT < 110% of the set VOUT and VOUT > 90% of the set VOUT
6	FLT_BUCK4_OC	OC interrupt indicator. Read only and cleared when read. 0: No Fault. Current is below the threshold. 1: Fault. Current is above the threshold.
5	FLT_BUCK4_OV	OV interrupt indicator. 0: No Fault. Voltage is below the threshold. 1: Fault. Voltage is above the threshold.
4	FLT_BUCK4_UV	UV interrupt indicator. 0: No Fault. Voltage is above the threshold. 1: Fault. Voltage is below the threshold or has recovered after being higher than the threshold.
3:0	Reserved	Reserved bits

Table 17. IO_I2CCFG

Address: 0x22								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	IO_I2CADDR						
Default	0	0	0	1	1	1	1	0
Type	RV	RO						

Bit	Name	Description
7	Reserved	Reserved bits
6:0	IO_I2CADDR	The I2C slave ID for the RTQ5756 series is factory-set and ranges from 0x18 to 0x1F.

Table 18. IO_INTCFG

Address: 0x23								
Bit	7	6	5	4	3	2	1	0
Field	Reserved			IO_IRQ_CMOS	IO_IRQ_INVERT	Reserved		Reserved
Default	0	0	0	0	1	0	0	0
Type	RV			RW	RW	RV		RV

Bit	Name	Description
7:5	Reserved	Reserved bits
4	IO_IRQ_CMOS	INT pin output 0: Open-drain 1: Push-pull
3	IO_IRQ_INVERT	INT pin polarity 0: Active high 1: Active low
2:0	Reserved	Reserved bits

Table 19. IO_RSTDVS

Address: 0x25								
Bit	7	6	5	4	3	2	1	0
Field	IO_RSTDVS	IO_RSTDVS	IO_RSTDVS	IO_RSTDVS	Reserved	IO_WDOG_TIMEOUT		
Default	1	1	1	1	0	0	0	0
Type	RW	RW	RW	RW	RV	RW		

Bit	Name	Description
7	IO_RSTDVS	Enable or disable the Buck4 watchdog reset function to the default voltage setting when the WDOG_RST pin is pulled low. 0: Disable 1: Enable
6	IO_RSTDVS	Enable or disable the Buck3 watchdog reset function to the default voltage setting when the WDOG_RST pin is pulled low. 0: Disable 1: Enable
5	IO_RSTDVS	Enable or disable the Buck2 watchdog reset function to the default voltage setting when the WDOG_RST pin is pulled low. 0: Disable 1: Enable
4	IO_RSTDVS	Enable or disable the Buck1 watchdog reset function to the default voltage setting when the WDOG_RST pin is pulled low. 0: Disable 1: Enable
3	Reserved	Reserved bits
2:0	IO_WDOG_TIMEOUT	Watchdog timeout setting. 000: 0ms (default) 100: 12.5ms 001: 1.56ms 101: 9ms 010: 3.125ms 110: 15.25ms 011: 6.25ms 111: 14.5ms Note: The minimum watchdog debounce time is 100μs.

Table 20. FLT_MASKTEMP

Address: 0x32								
Bit	7	6	5	4	3	2	1	0
Field	FLT_MASKUVLO	Reserved				FLT_MASKHD	FLT_MASKTSDR	Reserved
Default	0	0	0	0	0	0	0	0
Type	RW	RV				RW	RW	RV

Bit	Name	Description
7	FLT_MASKUVLO	Masking the UVLO detection signal. 0: Pass internal logic output to INT pin. 1: Mask internal logic output to INT pin.
6:3	Reserved	Reserved bits
2	FLT_MASKHD	Masking the hot die detection signal. 0: Pass internal logic output to INT pin. 1: Mask internal logic output to INT pin.
1	FLT_MASKTSDR	Masking the thermal shutdown detection signal. 0: Pass internal logic output to INT pin. 1: Mask internal logic output to INT pin.
0	Reserved	Reserved bits

Table 21. FLT_MASKBUCK1

Address: 0x33								
Bit	7	6	5	4	3	2	1	0
Field	FLT_BUCK1 MASKPG	FLT_BUCK1 MASKOC	FLT_BUCK1 MASKOV	FLT_BUCK1 MASKUV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RV			RV

Bit	Name	Description
7	FLT_BUCK1MASKPG	Masking the Buck1 power good detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
6	FLT_BUCK1MASKOC	Masking the Buck1 overcurrent detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
5	FLT_BUCK1MASKOV	Masking the Buck1 overvoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
4	FLT_BUCK1MASKUV	Masking the Buck1 undervoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
3:0	Reserved	Reserved bits

Table 22. FLT_MASKBUCK2

Address: 0x34								
Bit	7	6	5	4	3	2	1	0
Field	FLT_BUCK2 MASKPG	FLT_BUCK2 MASKOC	FLT_BUCK2 MASKOV	FLT_BUCK2 MASKUV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RV			RV

Bit	Name	Description
7	FLT_BUCK2MASKPG	Masking the Buck2 power good detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
6	FLT_BUCK2MASKOC	Masking the Buck2 overcurrent detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
5	FLT_BUCK2MASKOV	Masking the Buck2 overvoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
4	FLT_BUCK2MASKUV	Masking the Buck2 undervoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
3:0	Reserved	Reserved bits

Table 23. FLT_MASKBUCK3

Address: 0x35								
Bit	7	6	5	4	3	2	1	0
Field	FLT_BUCK3 MASKPG	FLT_BUCK3 MASKOC	FLT_BUCK3 MASKOV	FLT_BUCK3 MASKUV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RV			RV

Bit	Name	Description
7	FLT_BUCK3MASKPG	Masking the Buck3 power good detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
6	FLT_BUCK3MASKOC	Masking the Buck3 overcurrent detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
5	FLT_BUCK3MASKOV	Masking the Buck3 overvoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
4	FLT_BUCK3MASKUV	Masking the Buck3 undervoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
3:0	Reserved	Reserved bits

Table 24. FLT_MASKBUCK4

Address: 0x36								
Bit	7	6	5	4	3	2	1	0
Field	FLT_BUCK4 MASKPG	FLT_BUCK4 MASKOC	FLT_BUCK4 MASKOV	FLT_BUCK4 MASKUV	Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RV			RV

Bit	Name	Description
7	FLT_BUCK4MASKPG	Masking the Buck4 power good detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
6	FLT_BUCK4MASKOC	Masking the Buck4 overcurrent detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
5	FLT_BUCK4MASKOV	Masking the Buck4 overvoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
4	FLT_BUCK4MASKUV	Masking the Buck4 undervoltage detection signal. 0: Pass the internal logic output to the INT pin. 1: Mask the internal logic output from the INT pin.
3:0	Reserved	Reserved bits

Table 25. FLT_BUCK1_CTRL

Address: 0x37								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FLT_BUCK1_CTRLUV	Reserved		Reserved
Default	0	0	0	0	1	1	0	0
Type	RV				RW	RV		RV

Bit	Name	Description
7:4	Reserved	Reserved bits
3	FLT_BUCK1_CTRLUV	Latch or hiccup protection behavior when the Buck1 suffers UV detection. 0: UV Shutdown 1: UV Hiccup
2:0	Reserved	Reserved bits

Table 26. FLT_BUCK2_CTRL

Address: 0x38								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FLT_BUCK2_CTRLUV	Reserved		Reserved
Default	0	0	0	0	1	1	0	0
Type	RV				RW	RV		RV

Bit	Name	Description
7:4	Reserved	Reserved bits
3	FLT_BUCK2_CTRLUV	Latch or hiccup protection behavior when the Buck2 suffers UV detection. 0: UV Shutdown 1: UV Hiccup
2:0	Reserved	Reserved bits

Table 27. FLT_BUCK3_CTRL

Address: 0x39								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FLT_BUCK3_CTRLUV	Reserved		Reserved
Default	0	0	0	0	1	1	0	0
Type	RV				RW	RV		RV

Bit	Name	Description
7:4	Reserved	Reserved bits
3	FLT_BUCK3_CTRLUV	Latch or hiccup protection behavior when the Buck3 suffers UV detection. 0: UV Shutdown 1: UV Hiccup
2:0	Reserved	Reserved bits

Table 28. FLT_BUCK4_CTRL

Address: 0x3A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved				FLT_BUCK4_CTRLUV	Reserved		Reserved
Default	0	0	0	0	1	1	0	0
Type	RV				RW	RV		RV

Bit	Name	Description
7:4	Reserved	Reserved bits
3	FLT_BUCK4_CTRLUV	Latch or hiccup protection behavior when the Buck4 suffers UV detection. 0: UV Shutdown 1: UV Hiccup
2:0	Reserved	Reserved bits

Table 29. BUCK1_RAMP

Address: 0x3E								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	BUCK1_DVS_UP	Reserved			BUCK1_DVS_DOWN	Reserved	Reserved
Default	0	1	0	0	0	1	0	0
Type	RV	RW	RV			RW	RV	RV

Bit	Name	Description
7	Reserved	Reserved bits
6	BUCK1_DVS_UP	The operation mode when Buck1 ramps up. 0: Auto Mode 1: FCCM
5:3	Reserved	Reserved bits
2	BUCK1_DVS_DOWN	The operation mode when Buck1 ramps down. 0: Decay Mode 1: FCCM
1:0	Reserved	Reserved bits

Table 30. BUCK1_DVS0CFG1

Address: 0x48								
Bit	7	6	5	4	3	2	1	0
Field	BUCK1_DVS0							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	BUCK1_DVS0	Buck1 DVS0 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 31. BUCK1_DVS0CFG0

Address: 0x49								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK1_DVS0MODE	Reserved				BUCK1_ENDVS0
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	BUCK1_DVS0MODE	Buck1 DVS0 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	BUCK1_ENDVS0	Enable or disable Buck1 DVS0. 0: Disable 1: Enable

Table 32. BUCK1_DVS1CFG1

Address: 0x4A								
Bit	7	6	5	4	3	2	1	0
Field	BUCK1_DVS1							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	BUCK1_DVS1	Buck1 DVS1 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 33. BUCK1_DVS1CFG0

Address: 0x4B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK1_DVS1MODE	Reserved				BUCK1_ENDVS1
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	BUCK1_DVS1MODE	Buck1 DVS1 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	BUCK1_ENDVS1	Enable or disable Buck1 DVS1. 0: Disable 1: Enable

Table 34. BUCK1_DVSCFG

Address: 0x52								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					BUCK1_DVSPIN_POL	BUCK1_DVS_CTRL	
Default	0	0	0	0	0	0	0	0
Type	RV					RW	RW	

Bit	Name	Description
7:3	Reserved	Reserved bits
2	BUCK1_DVSPIN_ POL	When the Buck1 DVS up and down operations are controlled by using the external VSEL1 pin, this bit defines the polarity for VSEL1. 0: when VSEL1 = 1, use the DVS0 setting when VSEL1 = 0, use the DVS1 setting 1: when VSEL1 = 1, use the DVS1 setting when VSEL1 = 0, use the DVS0 setting
1:0	BUCK1_DVS_CTRL	The Buck1 DVS up and down operations are controlled by software or an external pin. 00: Use the DVS0 setting 01: Use the DVS1 setting 10: Controlled by the VSEL1 pin

Table 35. BUCK1_RSPCFG

Address: 0x54								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	BUCK1_RSPUP			Reserved	BUCK1_RSPDN		
Default	0	0	0	1	0	1	0	0
Type	RV	RW			RV	RW		

Bit	Name	Description
7	Reserved	Reserved bits
6:4	BUCK1_RSPUP	Buck1 DVS slew rate setting for DVS Up. 000: 16mV step/μs 100: 4mV step/μs 001: 16mV step/μs (default) 101 = 2mV step/μs 010: 16mV step/μs 110 = 1mV step/μs 011: 8mV step/μs 111 = 0.5mV step/μs
3	Reserved	Reserved bits
2:0	BUCK1_RSPDN	Buck1 DVS slew rate setting for DVS Down. 000: 16mV step/μs 100: 4mV step/μs (default) 001: 16mV step/μs 101 = 2mV step/μs 010: 16mV step/μs 110 = 1mV step/μs 011: 8mV step/μs 111 = 0.5mV step/μs

Table 36. BUCK1_SLEWCTRL

Address: 0x55								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK1_SS_SLEW		Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RV		RW		RV			RV

Bit	Name	Description
7:6	Reserved	Reserved bits
5:4	BUCK1_SS_SLEW	Set the soft-start slew rate when Buck1 is turned on by software or an external enable pin. The default is fixed to 10mV/μs for Buck1 turned on by the external enable pin. 00: 10mV/μs (default) 10 = 2.5mV/μs 01: 5mV/μs 11 = 1.25mV/μs
3:0	Reserved	Reserved bits

Table 37. BUCK1_EN_DLY

Address: 0x56								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK1_EN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK1_EN_DLY	Buck1 power on delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 38. BUCK1_SHUTDN_DLY

Address: 0x57								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK1_SHUTDN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK1_SHUTDN_DLY	Buck1 power off delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 39. BUCK2_RAMP

Address: 0x5B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	BUCK2_DVS_UP	Reserved			BUCK2_DVS_DOWN	Reserved	Reserved
Default	0	1	0	0	0	1	0	0
Type	RV	RW	RV			RW	RV	RV

Bit	Name	Description
7	Reserved	Reserved bits
6	BUCK2_DVS_UP	The operation mode when Buck2 ramps up. 0: Auto Mode 1: FCCM
5:3	Reserved	Reserved bits
2	BUCK2_DVS_DOWN	The operation mode when Buck2 ramps down. 0: Decay Mode 1: FCCM
1:0	Reserved	Reserved bits

Table 40. BUCK2_DVS0CFG1

Address: 0x62								
Bit	7	6	5	4	3	2	1	0
Field	BUCK2_DVS0							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	BUCK2_DVS0	Buck2 DVS0 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 41. BUCK2_DVS0CFG0

Address: 0x63								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK2_DVS0MODE	Reserved				BUCK2_ENDVS0
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	BUCK2_DVS0MODE	Buck2 DVS0 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	BUCK2_ENDVS0	Enable or disable Buck2 DVS0. 0: Disable 1: Enable

Table 42. BUCK2_DVS1CFG1

Address: 0x64								
Bit	7	6	5	4	3	2	1	0
Field	BUCK2_DVS1							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	BUCK2_DVS1	Buck2 DVS1 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 43. BUCK2_DVS1CFG0

Address: 0x65								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK2_DVS1MODE	Reserved				BUCK2_ENDVS1
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	BUCK2_DVS1MODE	Buck2 DVS1 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	BUCK2_ENDVS1	Enable or disable Buck2 DVS1. 0: Disable 1: Enable

Table 44. BUCK2_DVSCFG

Address: 0x6C								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					BUCK2_DVSPIN_ POL	BUCK2_DVS_CTRL	
Default	0	0	0	0	0	0	0	0
Type	RV					RW	RW	

Bit	Name	Description
7:3	Reserved	Reserved bits
2	BUCK2_DVSPIN_ POL	When the Buck2 DVS up and down operations are controlled by using the external VSEL2 pin, this bit defines the polarity for VSEL2. 0: when VSEL2 = 1, use the DVS0 setting when VSEL2 = 0, use the DVS1 setting 1: when VSEL2 = 1, use the DVS1 setting when VSEL2 = 0, use the DVS0 setting
1:0	BUCK2_DVS_CTRL	The Buck2 DVS up and down operations are controlled by software or an external pin. 00: Use the DVS0 setting 01: Use the DVS1 setting 10: Controlled by the VSEL2 pin

Table 45. BUCK2_RSPCFG

Address: 0x6E								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	BUCK2_RSPUP			Reserved	BUCK2_RSPDN		
Default	0	0	0	1	0	1	0	0
Type	RV	RW			RV	RW		

Bit	Name	Description
7	Reserved	Reserved bits
6:4	BUCK2_RSPUP	Buck2 DVS slew rate setting for DVS Up. 000: 16mV step/μs 100: 4mV step/μs 001: 16mV step/μs (default) 101 = 2mV step/μs 010: 16mV step/μs 110 = 1mV step/μs 011: 8mV step/μs 111 = 0.5mV step/μs
3	Reserved	Reserved bits
2:0	BUCK2_RSPDN	Buck2 DVS slew rate setting for DVS Down. 000: 16mV step/μs 100: 4mV step/μs (default) 001: 16mV step/μs 101 = 2mV step/μs 010: 16mV step/μs 110 = 1mV step/μs 011: 8mV step/μs 111 = 0.5mV step/μs

Table 46. BUCK2_SLEWCTRL

Address: 0x6F								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK2_SS_SLEW		Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RV		RW		RV			RV

Bit	Name	Description
7:6	Reserved	Reserved bits
5:4	BUCK2_SS_SLEW	Set the soft-start slew rate when Buck2 is turned on by software or an external enable pin. The default is fixed to 10mV/μs for Buck2 turned on by the external enable pin. 00: 10mV/μs (default) 10 = 2.5mV/μs 01: 5mV/μs 11 = 1.25mV/μs
3:0	Reserved	Reserved bits

Table 47. BUCK2_EN_DLY

Address: 0x70								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK2_EN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK2_EN_DLY	Buck2 power on delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 48. BUCK2_SHUTDN_DLY

Address: 0x71								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK2_SHUTDN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK2_SHUTDN_DLY	Buck2 power off delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 49. Buck3_RAMP

Address: 0x75								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Buck3_DVS_UP	Reserved			Buck3_DVS_DOWN	Reserved	Reserved
Default	0	1	0	0	0	1	0	0
Type	RV	RW	RV			RW	RV	RV

Bit	Name	Description
7	Reserved	Reserved bits
6	Buck3_DVS_UP	The operation mode when Buck3 ramps up. 0: Auto Mode 1: FCCM
5:3	Reserved	Reserved bits
2	Buck3_DVS_DOWN	The operation mode when Buck3 ramps down. 0: Decay Mode 1: FCCM
1:0	Reserved	Reserved bits

Table 50. Buck3_DVS0CFG1

Address: 0x7C								
Bit	7	6	5	4	3	2	1	0
Field	Buck3_DVS0							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	Buck3_DVS0	Buck3 DVS0 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 51. Buck3_DVS0CFG0

Address: 0x7D								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		Buck3_DVS0MODE	Reserved				Buck3_ENDVS0
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	Buck3_DVS0MODE	Buck3 DVS0 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	Buck3_ENDVS0	Enable or disable Buck3 DVS0. 0: Disable 1: Enable

Table 52. Buck3_DVS1CFG1

Address: 0x7E								
Bit	7	6	5	4	3	2	1	0
Field	Buck3_DVS1							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	Buck3_DVS1	Buck3 DVS1 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 53. Buck3_DVS1CFG0

Address: 0x7F								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		Buck3_DVS1MODE	Reserved				Buck3_ENDVS1
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	Buck3_DVS1MODE	Buck3 DVS1 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	Buck3_ENDVS1	Enable or disable Buck3 DVS1. 0: Disable 1: Enable

Table 54. Buck3_DVSCFG

Address: 0x86								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					Buck3_DVSPIN_POL	Buck3_DVS_CTRL	
Default	0	0	0	0	0	0	0	0
Type	RV					RW	RW	

Bit	Name	Description
7:3	Reserved	Reserved bits
2	Buck3_DVSPIN_ POL	When the Buck3 DVS up and down operations are controlled by using the external VSEL3 pin, this bit defines the polarity for VSEL3. 0: when VSEL3 = 1, use the DVS0 setting when VSEL3 = 0, use the DVS1 setting 1: when VSEL3 = 1, use the DVS1 setting when VSEL3 = 0, use the DVS0 setting
1:0	Buck3_DVS_CTRL	The Buck3 DVS up and down operations are controlled by software or an external pin. 00: Use the DVS0 setting 01: Use the DVS1 setting 10: Controlled by the VSEL3 pin

Table 55. Buck3_RSPCFG

Address: 0x88								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Buck3_RSPUP			Reserved	Buck3_RSPDN		
Default	0	0	0	1	0	1	0	0
Type	RV	RW			RV	RW		

Bit	Name	Description
7	Reserved	Reserved bits
6:4	Buck3_RSPUP	Buck3 DVS slew rate setting for DVS Up. 000: 16mV step/μs 100: 4mV step/μs 001: 16mV step/μs (default) 101 = 2mV step/μs 010: 16mV step/μs 110 = 1mV step/μs 011: 8mV step/μs 111 = 0.5mV step/μs
3	Reserved	Reserved bits
2:0	Buck3_RSPDN	Buck3 DVS slew rate setting for DVS Down. 000: 16mV step/μs 100: 4mV step/μs (default) 001: 16mV step/μs 101 = 2mV step/μs 010: 16mV step/μs 110 = 1mV step/μs 011: 8mV step/μs 111 = 0.5mV step/μs

Table 56. Buck3_SLEWCTRL

Address: 0x89								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		Buck3_SS_SLEW		Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RV		RW		RV			RV

Bit	Name	Description
7:6	Reserved	Reserved bits
5:4	Buck3_SS_SLEW	Set the soft-start slew rate when Buck3 is turned on by software or an external enable pin. The default is fixed to 10mV/μs for Buck3 turned on by the external enable pin. 00: 10mV/μs (default) 10 = 2.5mV/μs 01: 5mV/μs 11 = 1.25mV/μs
3:0	Reserved	Reserved bits

Table 57. BUCK3_EN_DLY

Address: 0x8A								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK3_EN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK3_EN_DLY	Buck3 power on delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 58. BUCK3_SHUTDN_DLY

Address: 0x8B								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK3_SHUTDN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK3_SHUTDN_DLY	Buck3 power off delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 59. Buck4_RAMP

Address: 0x8F								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Buck4_DVS_UP	Reserved			Buck4_DVS_DOWN	Reserved	Reserved
Default	0	1	0	0	0	1	0	0
Type	RV	RW	RV			RW	RV	RV

Bit	Name	Description
7	Reserved	Reserved bits
6	Buck4_DVS_UP	The operation mode when Buck4 ramps up. 0: Auto Mode 1: FCCM
5:3	Reserved	Reserved bits
2	Buck4_DVS_DOWN	The operation mode when Buck4 ramps down. 0: Decay Mode 1: FCCM
1:0	Reserved	Reserved bits

Table 60. Buck4_DVS0CFG1

Address: 0x96								
Bit	7	6	5	4	3	2	1	0
Field	Buck4_DVS0							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	Buck4_DVS0	Buck4 DVS0 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 61. Buck4_DVS0CFG0

Address: 0x97								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		Buck4_DVS0MODE	Reserved				Buck4_ENDVS0
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	Buck4_DVS0MODE	Buck4 DVS0 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	Buck4_ENDVS0	Enable or disable Buck4 DVS0. 0: Disable 1: Enable

Table 62. Buck4_DVS1CFG1

Address: 0x98								
Bit	7	6	5	4	3	2	1	0
Field	Buck4_DVS1							
Default	0	1	1	1	1	0	0	0
Type	RW							

Bit	Name	Description
7:0	Buck4_DVS1	Buck4 DVS1 output voltage setting. SEL[7:0] = 11111111: VOUT = 2.05V ... SEL[7:0] = 10110100: VOUT = 1.3V ... SEL[7:0] = 0000000: 0.4V For 0.4V to 1.3V, VOUT = 0.4V + SEL[7:0](decimal) x 5mV For 1.3V to 2.05V, VOUT = 1.3V + {SEL[7:0](decimal) - 180 } x 10mV

Table 63. Buck4_DVS1CFG0

Address: 0x99								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		Buck4_DVS1MODE	Reserved				Buck4_ENDVS1
Default	0	0	1	0	0	0	0	0
Type	RV		RW	RV				RW

Bit	Name	Description
7:6	Reserved	Reserved bits
5	Buck4_DVS1MODE	Buck4 DVS1 operation mode setting. 0: Auto Mode 1: FCCM
4:1	Reserved	Reserved bits
0	Buck4_ENDVS1	Enable or disable Buck4 DVS1. 0: Disable 1: Enable

Table 64. Buck4_DVSCFG

Address: 0xA0								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					Buck4_DVSPIN_ POL	Buck4_DVS_CTRL	
Default	0	0	0	0	0	0	0	0
Type	RV					RW	RW	

Bit	Name	Description
7:3	Reserved	Reserved bits
2	Buck4_DVSPIN_ POL	When the Buck4 DVS up and down operations are controlled by using the external VSEL4 pin, this bit defines the polarity for VSEL4. 0: when VSEL4 = 1, use the DVS0 setting when VSEL4 = 0, use the DVS1 setting 1: when VSEL4 = 1, use the DVS1 setting when VSEL4 = 0, use the DVS0 setting
1:0	Buck4_DVS_CTRL	The Buck4 DVS up and down operations are controlled by software or an external pin. 00: Use the DVS0 setting 01: Use the DVS1 setting 10: Controlled by the VSEL4 pin

Table 65. Buck4_RSPCFG

Address: 0xA2								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Buck4_RSPUP			Reserved	Buck4_RSPDN		
Default	0	0	0	1	0	1	0	0
Type	RV	RW			RV	RW		

Bit	Name	Description
7	Reserved	Reserved bits
6:4	Buck4_RSPUP	Buck4 DVS slew rate setting for DVS Up. 000: 16mV step/μs 001: 16mV step/μs (default) 010: 16mV step/μs 011: 8mV step/μs 100: 4mV step/μs 101 = 2mV step/μs 110 = 1mV step/μs 111 = 0.5mV step/μs
3	Reserved	Reserved bits
2:0	Buck4_RSPDN	Buck4 DVS slew rate setting for DVS Down. 000: 16mV step/μs 001: 16mV step/μs 010: 16mV step/μs 011: 8mV step/μs 100: 4mV step/μs (default) 101 = 2mV step/μs 110 = 1mV step/μs 111 = 0.5mV step/μs

Table 66. Buck4_SLEWCTRL

Address: 0xA3								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		Buck4_SS_SLEW		Reserved			Reserved
Default	0	0	0	0	0	0	0	0
Type	RV		RW		RV			RV

Bit	Name	Description
7:6	Reserved	Reserved bits
5:4	Buck4_SS_SLEW	Set the soft-start slew rate when Buck4 is turned on by software or external enable pin. The default is fixed to 10mV/μs for Buck4 turned on by an external enable pin. 00: 10mV/μs (default) 10 = 2.5mV/μs 01: 5mV/μs 11 = 1.25mV/μs
3:0	Reserved	Reserved bits

Table 67. BUCK4_EN_DLY

Address: 0xA4								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK4_EN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

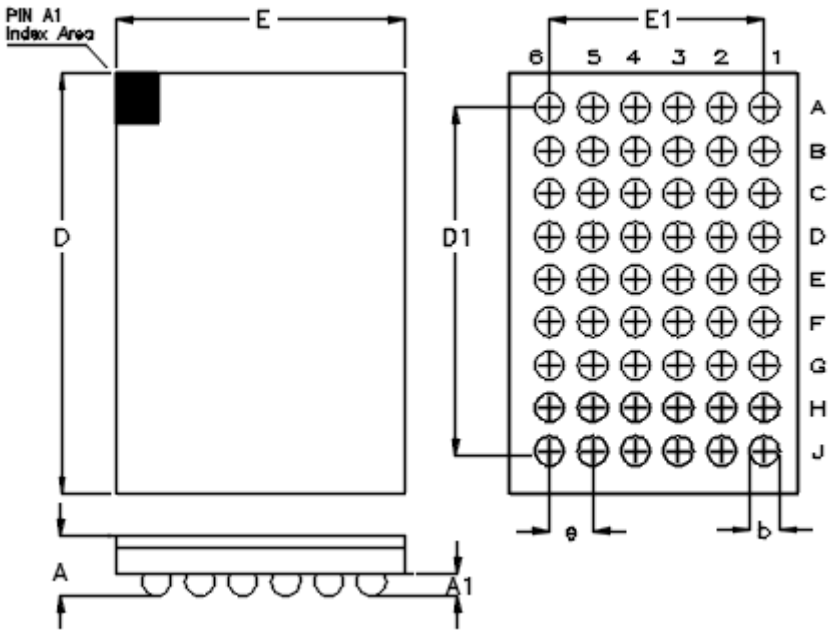
Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK4_EN_DLY	Buck4 power on delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

Table 68. BUCK4_SHUTDN_DLY

Address: 0xA5								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		BUCK4_SHUTDN_DLY					
Default	0	0	0	0	0	0	0	0
Type	RV		RW					

Bit	Name	Description
7:6	Reserved	Reserved bits
5:0	BUCK4_SHUTDN_DLY	Buck4 power off delay from the master chip enable pin 000000: 0ms - 111111b = 63ms (steps of 1ms)

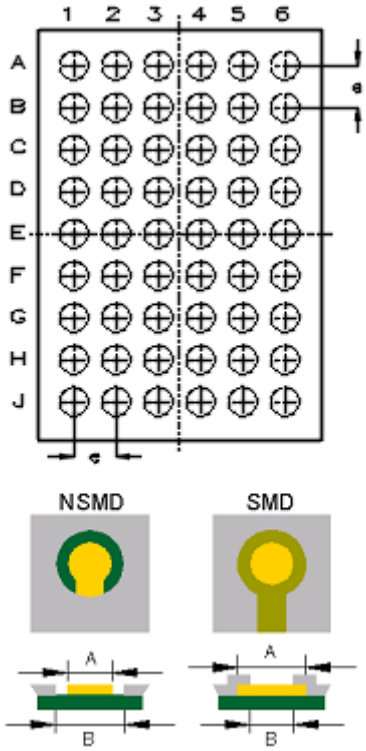
20 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.880	3.960	0.153	0.156
D1	3.200		0.126	
E	2.650	2.730	0.104	0.107
E1	2.000		0.079	
e	0.400		0.016	

54B WL-CSP 2.69x3.92 Package (BSC)

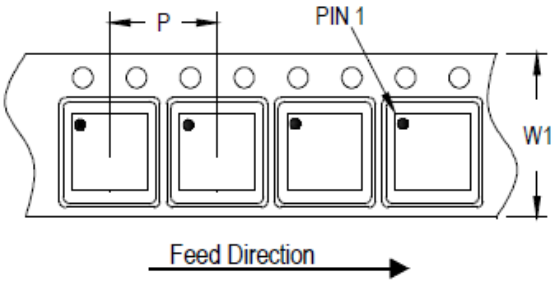
21 Footprint Information

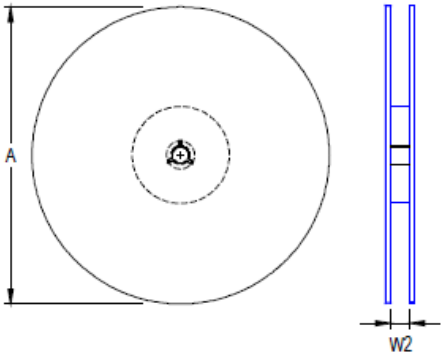


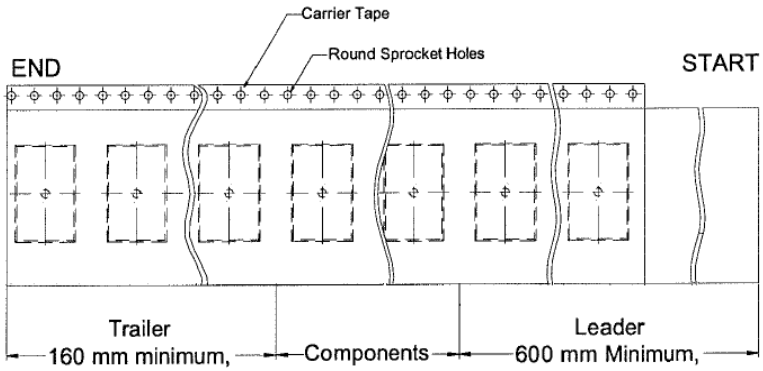
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.69*3.92-54(BSC)	54	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

22 Packing Information

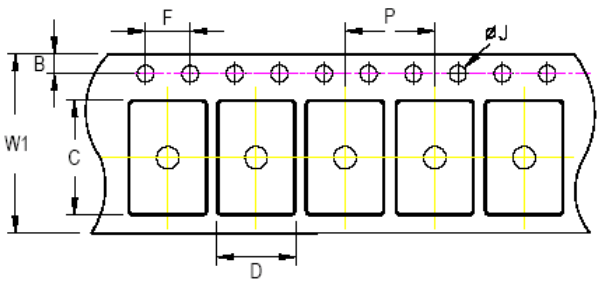
22.1 Tape and Reel Data

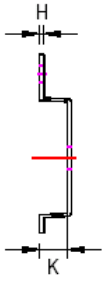






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.69x3.92	12	8	180	7	1,500	160	600	12.4/14.4





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.69x3.92	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Un-full Reel.		

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description	Item
00	2024/10/21	Final	

24 Product Status

Product Number	Status(1)	Product Code(2)	Slave ID	Power Rails	Defaults Output Voltage	Defaults Output Mode	Enable Delay Time	Disable Delay Time
RTQ5756AWSC-00	Active	36	0x1A	Vout1 Vout2 Vout3	None	FCCM	0ms	0ms
RTQ5756BWSC-00	Active	3C	0x1B	Vout1 Vout2 Vout3 Vout4	None	FCCM	0ms	0ms
RTQ5756CWSC-00	Active	37	0x1C	Vout1 Vout2	None	FCCM	0ms	0ms
RTQ5756DWSC-00	Active	3D	0x1D	Vout1	None	FCCM	0ms	0ms
RTQ5756EWSC-00	Active	35	0x1E	Vout1 Vout2	None	FCCM	0ms	0ms
RTQ5756AWSC-01	Active	42	0x18	Vout1 Vout2 Vout3	None	FCCM	0ms	0ms
RTQ5756BWSC-01	Active	44	0x19	Vout1 Vout2 Vout3 Vout4	None	FCCM	0ms	0ms

Note 14.

- Marked with (1) indicated: The part status are defined as follows:

  Active: Device is in production and is recommended for new designs.

  NRND: Not recommended for new designs.

  Last Time Buy: The device will be discontinued, and a lifetime-buy period is in effect.

  EOL: Richtek has discontinued the production of the device.

- Marked with (2) indicated: The product code can be found on device marking.

ZZ : Product Code
XXYY : Wafer ID with Check Sum
CCC-RRR : IC Coordinate (X, Y)
YMDAN : Date Code