RICHTEK®

RTQ5132

DDR5 Client VR on DIMM PMIC

1 General Description

The RTQ5132 is an integrated power management IC suitable for general DDR5 SODIMM and UDIMM applications. This device provides three Buck converters (SWA, SWB, and SWC) and two LDOs (VLDO_1.0V and VLDO_1.8V). Additionally, the RTQ5132 supports a selectable interface (I^2C or I3C Basic) to accommodate various application environments. A comprehensive protection mechanism is embedded to ensure safe power distribution, with the capability to record fault events in registers and signal them through PWR_GOOD and GSI_n open-drain indicators. The RTQ5132 is available in a WQFN-28L 3x4 (FC) package. The recommended junction temperature range is from –10°C to 125°C and ambient temperature range is 0°C to 85°C.

2 Ordering Information

RTQ5132 □□-□□□

- MTP Serial Number
  0 = JEDEC Default Code
- Single or Dual Phase
  1 = SWA/SWB Single Phase
  2 = SWA/SWB Dual Phase
- Version
- Package Type(1)
  QWF: WQFN-28L 3x4 (FC) (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

4 Features

- **VIN_Bulk with Input Supply Range: 4.25V to 5.5V**
- **High Integration:**
  - **Three High Efficiency Buck Converters**
    - **SWA: I_{TDC} = 4A, I_{MAX} = 5A**
    - **SWB: I_{TDC} = 4A, I_{MAX} = 5A**
    - **SWC: I_{TDC} = 1A, I_{MAX} = 2A**
  - **Two LDOs**
    - **VLDO_1.8V: I_{MAX} = 25mA**
    - **VLDO_1.0V: I_{MAX} = 20mA**
- **0.75% Converter Output Accuracy**
- **Fast Transient Response with A^2RCOT Control**
- **Support I^2C and I3C Slave Control**
- **Error Log Counter and Data Storage (NVM)**
- **MTP Registers with Secured R/W Access**
- **Programmable and DIMM Specific Registers for Customization**
- **Programmable Mode for Debug and Validation**
- **Telemetry for Output Current, Voltage and Power**
- **Complete Protection Mechanisms**
  - **VIN_Bulk Input Supply OVP**
  - **OVP, UVP, OCP, HCW for Each Rails**
  - **High Temp Warning and OTP**
- **General Status Interrupt Function**
- **Power-Good Indicator**

5 Applications

- DDR5 SODIMM/ UDIMM

6 Simplified Application Circuit

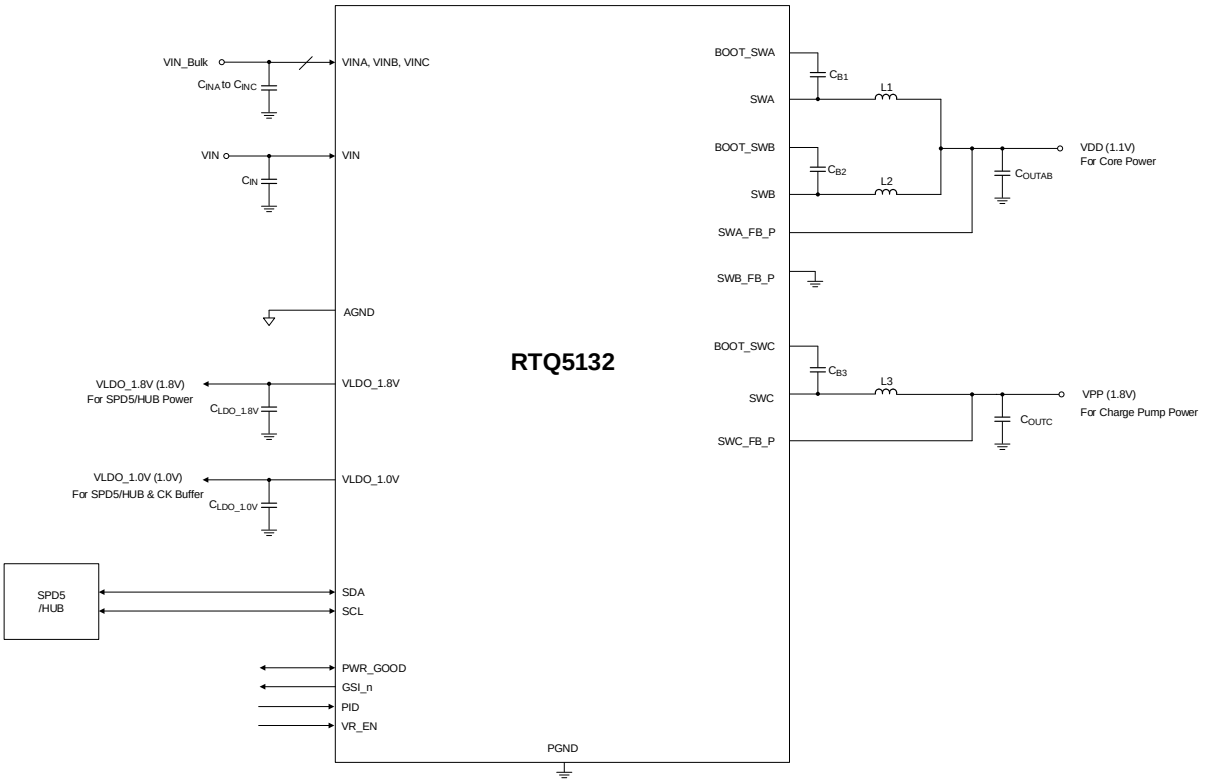

Figure 1. SWA and SWB are combined as Dual-Phase Mode

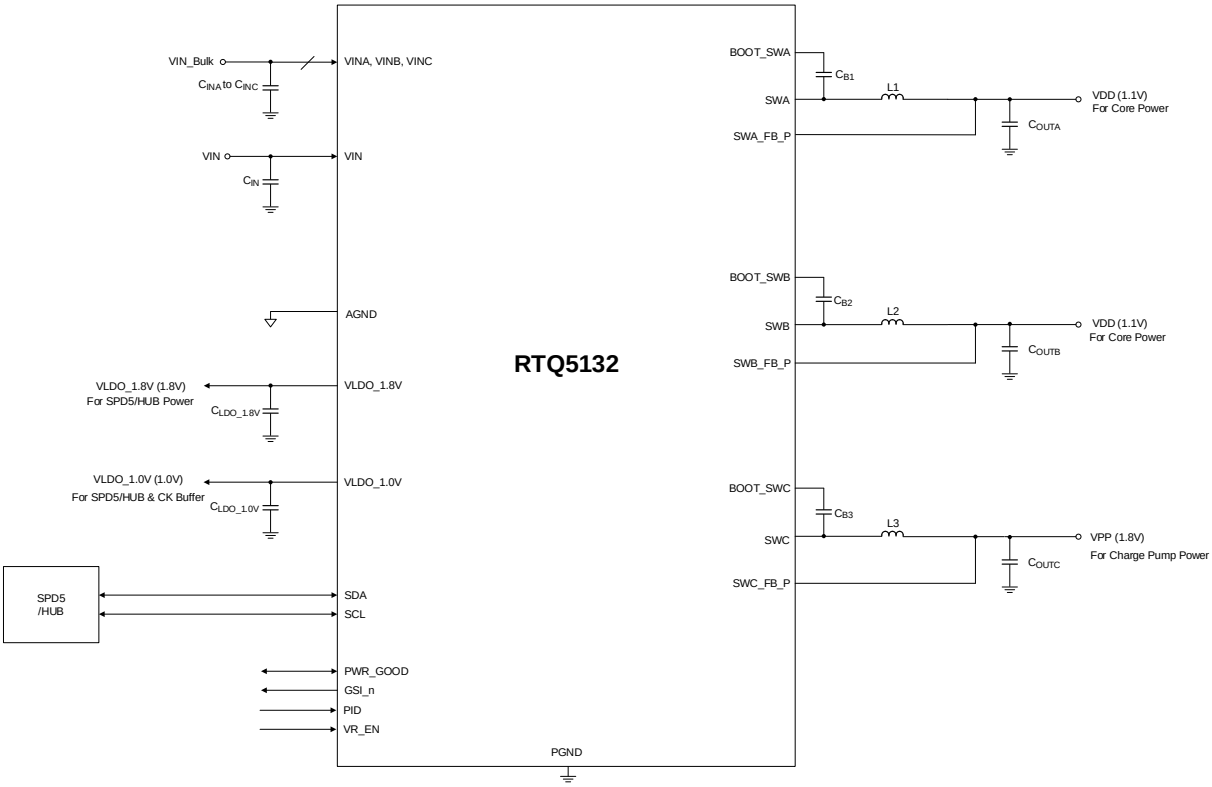

Figure 2. SWA and SWB are operating in Single-Phase Mode

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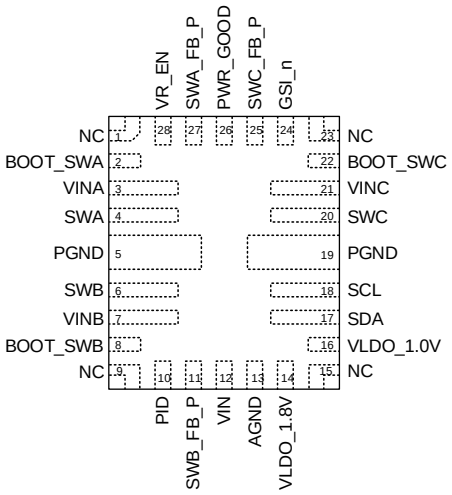
7 Pin Configuration

(TOP VIEW)



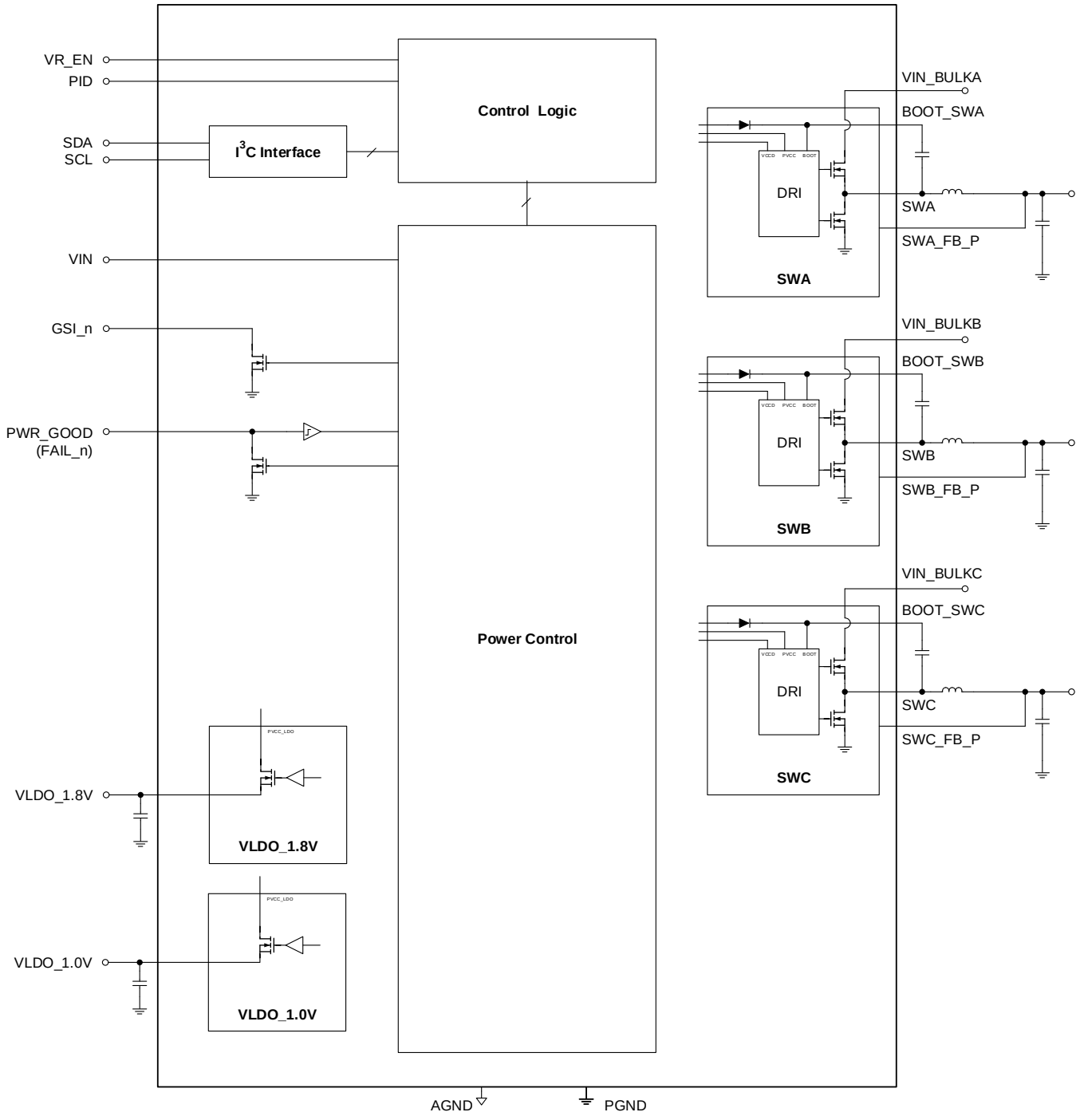
WQFN-28L 3x4 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 9, 15, 23	NC	Non-functional pins. No internal connections to the chip.
2	BOOT_SWA	Buck A bootstrap. Bootstrap node for switch node SWA high-side NMOS driver. Connect a capacitor between SWA and BOOT_SWA to form a floating supply across the high-side switch driver of Buck A.
3	VINA	Input supply of Buck A. VINA is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
4	SWA	Buck A switch output. Output switch node SWA regulator. This pin is connected to an external inductor (L1).
5, 19	PGND	Common Power ground. Connect PGND to DIMM ground plane. PGND pins require special consideration during PCB layout.
6	SWB	Buck B switch output. Output switch node SWB regulator. This pin is connected to an external inductor (L2).
7	VINB	Input supply of Buck B. VINB is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
8	BOOT_SWB	Buck B bootstrap. Bootstrap node for switch node SWB high-side NMOS driver. Connect a capacitor between SWB and BOOT_SWB to form a floating supply across the high-side switch driver of Buck B.
10	PID	PMIC ID pin for I^2C and I3C Basic bus.
11	SWB_FB_P	Positive feedback of Buck B. This pin is connected to the SWB remote positive sense feedback.
12	VIN	5 V power input supply to the PMIC for analog circuits.
13	AGND	Analog ground. Connect AGND to the power ground pin with a single via.
14	VLDO_1.8V	PMIC 1.8V LDO supply. Connect a 4.7μF decoupling capacitor near this pin.

Pin No.	Pin Name	Pin Function
16	VLDO_1.0V	PMIC 1.0V LDO supply for I3C push-pull driver. Connect a 4.7μF decoupling capacitor near this pin.
17	SDA	Bus data of I^2C and I3C.
18	SCL	Bus clock of I^2C and I3C.
20	SWC	Buck C switch output. Output switch node SWC regulator. This pin is connected to an external inductor (L3).
21	VINC	Input supply of Buck C. VINC is connected to 5V power plane on the DIMM. All three VINx input pins must be connected to 5V supply, even if one or more regulators are not intended to be used.
22	BOOT_SWC	Buck C bootstrap. Bootstrap node for switch node SWC high-side NMOS driver. Connect a capacitor between SWC and BOOT_SWC to form a floating supply across the high-side switch driver of Buck C.
24	GSI_n	General status interrupt. Open Drain Output. The PMIC asserts this pin low to communicate one or more events to the host. This pin remains asserted until the appropriate registers are explicitly cleared and the event is no longer present.
25	SWC_FB_P	Positive feedback of Buck C. Switch node SWC remote positive sense feedback.
26	PWR_GOOD	Power good indicator. This pin can be configured as an open drain output pin or as an input pin. As an open-drain output pin: The PMIC allows this pin to float high when the VIN_Bulk input supply, all enabled buck output regulators, and all LDO regulators maintain the tolerance thresholds configured in the appropriate registers. The PMIC drives this pin low if the VIN_Bulk input falls below the threshold, or if any of the enabled buck output regulators or any LDO output regulator exceeds the configured threshold tolerance. As an input pin: The PMIC disables its output regulators when this pin is driven low; however, the LDO outputs should remain on.
27	SWA_FB_P	Positive feedback of Buck A. This pin is connected to the SWA remote positive sense feedback.
28	VR_EN	PMIC Enable. When this pin is high, the PMIC turns the regulator on. Conversely, when the pin is low, the PMIC turns the regulator off. This pin should not be left floating. If unused, it should be connected to GND.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VINA, VINB, VINC ---------- –0.3V to 6V
- Supply Input Voltage, VIN ---------- –0.3V to 6V
- AGND to PGND ---------- –0.3V to 0.3V
- Switching PIN, SWA, SWB, SWC
  - DC ---------- –0.3V to 6V
  - < 25ns ---------- –3V to 9V
- Boot Voltage
  - BOOT to SWA (BOOT-SWA) ---------- –0.3V to 6V
  - BOOT to SWB (BOOT-SWB) ---------- –0.3V to 6V
  - BOOT to SWC (BOOT-SWC) ---------- –0.3V to 6V
- Other I/O ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-28L 3x4 (FC) ---------- 2.43W
- Package Thermal Resistance (Note 3)
  - WQFN-28L 3x4 (FC), θ_{JA} ---------- 41°C/W
  - WQFN-28L 3x4 (FC), θ_{JC} ---------- 15.8°C/W
  - WQFN-28L 3x4 (FC), θ_{JB} ---------- 8.38°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 155°C
- Storage Temperature Range ---------- –55°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM ---------- 2kV
  - CDM ---------- 500V

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, V_{INA}, V_{INB}, V_{INC} ---------- 4.25V to 5.5V
- Supply Input Voltage, V_{IN} ---------- 4.25V to 5.5V
- Junction Temperature Range ---------- –10°C to 125°C
- Ambient Temperature Range ---------- 0°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN_SWA} = V_{IN_SWB} = V_{IN_SWC} = 5V, V_{IN} = 5V, T_A = −10°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply Electrical Characteristics						
Bulk Input Supply Voltage Ramp Up Rate	VIN_Bulk_Ramp_Up	The ramp up rate between 300 mV and 4.0V	0.1	--	3	V/ms
Bulk Input Supply Voltage Ramp Down Rate	VIN_Bulk_Ramp_Down	The ramp down rate between 4.0 V and 300mV.	0.5	--	1	V/ms
(VIN) Shutdown Current	I_{SHDN_VIN}	T_A = 25°C; VIN = VIN_Bulk = 5V, VR_EN = 0, All circuitry including output regulators and LDOs are off.	--	--	25	μA
VIN Supply Current (non-switching)	$I_{Q\_VIN\_NSW}$	T_A = 25°C; I_{OUT} = 0mA, all LDO, SWA to SWC on, no switching	--	1.9	--	mA
VIN Undervoltage Lockout and OVP Threshold						
VIN Undervoltage Lockout Rising Threshold	$V_{IN\_UVLO\_R}$	Rising edge	--	4	--	V
VIN Undervoltage Lockout Falling Threshold	$V_{IN\_UVLO\_F}$	Falling edge	--	3.8	--	V
VIN Overvoltage Rising Threshold	$V_{IN\_OVP\_R}$	Setting by reg_0x1B"[7] = "0"	--	6	--	V
I^2C, I3C and Interface DC Electrical Specification						
SDA, SCL I^2C Operate Frequency	f_{SCL_I2C}		0.01	--	1	MHz
SDA, SCL I3C Operate Frequency	f_{SCL_I3C}		0.01	--	12.5	MHz
SDA, SCL Input High Voltage	V_{IH_I2C}		0.7	--	3.6	V
SDA, SCL Input Low Voltage	V_{IL_I2C}		−0.3	--	0.3	V
PWR_GOOD Input High Voltage	V_{IH_PGOOD}		1.26	--	3.6	V
VR_EN Input High Voltage	V_{IH_EN}		1.26	--	3.6	V
PWR_GOOD Input Low Voltage	V_{IL_PGOOD}		−0.3	--	0.3	V
VR_EN Input Low Voltage	V_{IL_EN}		−0.3	--	0.3	V
PID Input High Voltage	V_{IH_PID}		1.2	--	--	V
PID Input Low Voltage	V_{IL_PID}		--	--	0.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA Output High Voltage	V_{OH_SDA}	I_O = -3mA	0.75	--	--	V
(SDA, GSI_n, PWR_GOOD) Output Low Voltage	V_{OL}	I_O = 3mA	--	--	0.3	V
SDA Output High Current	I_{OH_SDA}		–3	--	--	mA
(SDA, GSI_n, PWR_GOOD Output Low Current	I_{OL}		--	--	3	mA
SDA Output Pull-up Impedance	R_{PU_SDA}		--	40	--	Ω
SDA Output Pull-down Impedance	R_{PD_SDA}		--	20	--	Ω
GSI_n Output Pull-down Impedance	$R_{PD\_GSI\_n}$		--	50	--	Ω
PWR_GOOD Output Pull-down Impedance	R_{PD_PGOOD}		--	50	--	Ω
SWA/B Rail – VDD/VDDQ (1.1V) - Single Phase Regulator (0.8V to 1.435V, ITDCA/B = 4A/4A respectively)						
Output Voltage Setting	V_{OUT}	SWAB setting by reg_0x21"[7:1]	0.8	--	1.435	V
Output Voltage Accuracy	$V_{OUT\_AB\_ACC}$	I_{OUT} = 0A, operating at CCM	–0.75	--	0.75	% of V_{OUT_AB}
VID Slew Rate	SR_{VID_AB}		--	1	--	mV/μs
SWA/B Soft-Start/Stop Time						
Soft-Start Time	t_{SS}	t_{set} = 1ms to 14ms	–15	--	15	% of t_{SS}
Soft-Stop Time	t_{STOP}	t_{set} = 0.5ms to 4ms	–20	--	20	% of t_{STOP}
SWA/B Internal MOSFET Turn On Resistance						
On-Resistance of High-side MOSFET	R_{DSON_H}	T_A = 25°C	--	16	--	mΩ
On-Resistance of Low-side MOSFET	R_{DSON_L}	T_A = 25°C	--	10	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWA/B Switching Frequency						
Switching Frequency	f_{SW_AB}	Setting by reg_0x29"[5:4]/0x2A"[7:6] = "00" (default)	0.6375	0.75	0.8625	MHz
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "01"	0.85	1	1.15	
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "10"	1.0625	1.25	1.4375	
		Setting by reg_0x29"[5:4]/0x2A"[7:6] = "11"	1.275	1.5	1.725	
SWA/B Power Good Indicator						
(Power Good) Falling Threshold	$V_{OUT\_AB\_PGOOD\_F}$	Setting by reg_0x21"[0]/0x25"[0] = "0" (default)	--	–5	--	% of V_{OUT_AB}
		Setting by reg_0x21"[0]/0x25"[0] = "1"	--	–7.5	--	
(Power Good) Falling Propagation Delay	$t_{DLY\_PGOOD\_F\_AB}$		--	5	--	µs
(Power Good) Rising Threshold	$V_{OUT\_AB\_PGOOD\_R}$	Setting by reg_0x22"[7:6]/0x26"[7:6] = "00"	--	5	--	% of V_{OUT_AB}
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "01" (default)	--	7.5	--	
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "10"	--	10	--	
		Setting by reg_0x22"[7:6]/0x26"[7:6] = "11"	--	2.5	--	
(Power Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_AB}$		--	5	--	µs
SWA/B Protections						
Output Overvoltage Rising Threshold	$V_{OUT\_AB\_OVP\_R}$	Setting by reg_0x22"[5:4]/0x26"[5:4] = "00"	--	7.5	--	% of V_{OUT_AB}
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "01"	--	10	--	
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "10" (default)	--	12.5	--	
		Setting by reg_0x22"[5:4]/0x26"[5:4] = "11"	--	20	--	
Output Overvoltage Protection Propagation Delay	$t_{DLY\_OVP\_AB}$		--	5	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Undervoltage Falling Threshold	$V_{OUT\_AB\_UVP\_F}$	Setting by reg_0x22"[3:2]/0x26"[3:2] = "00" (default)	--	–10	--	% of V_{OUT_AB}
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "01"	--	–12.5	--	
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "10"	--	–7.5	--	
		Setting by reg_0x22"[3:2]/0x26"[3:2] = "11"	--	–20	--	
Output Undervoltage Protection Propagation Delay	$t_{DLY\_UVP\_AB}$		--	5	--	µs
SWA/B Current Limit						
Current Limit	$I_{LIM\_SWA/B}$	Valley current limited Setting by reg_0x20"[7:6]/[3:2] = "00"	--	3	--	A
		Setting by reg_0x20"[7:6]/[3:2] = "01"	--	3.5	--	
		Setting by reg_0x20"[7:6]/[3:2] = "10"	--	4	--	
		Setting by reg_0x20"[7:6]/[3:2] = "11" (default)	--	4.5	--	
SWC Rail – VPP(1.8V) – Single Phase Regulator (1.5V to 2.135V, ITDC = 1A)						
Output Voltage Setting	V_{OUT_C}	Setting by reg_0x27"[7:1]	1.5	1.8	2.135	V
Output Voltage Accuracy	$V_{OUT\_C\_ACC}$	I_{OUT} = 0A, operating at CCM	–0.75	--	0.75	% of V_{OUT_C}
VID Slew Rate	SR_{VID_C}		--	1	--	mV/µs
SWC Soft-Start/Stop Time						
Soft-Start Time	t_{SS}	t_{set} = 1ms to 14ms	–15	--	15	% of t_{SS}
Soft-Stop Time	t_{STOP}	t_{set} = 1ms to 8ms	–20	--	20	% of t_{STOP}
SWC Internal MOSFET Turn On Resistance						
On-Resistance of High-side MOSFET	R_{DSON_H}	T_A = 25°C	--	55	--	mΩ
On-Resistance of Low-side MOSFET	R_{DSON_L}	T_A = 25°C	--	45	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWC Switching Frequency						
Switching Frequency	f_{SW_C}	Setting by reg_0x2A"[1:0] = "00"	0.6375	0.75	0.8625	MHz
		Setting by reg_0x2A"[1:0] = "01" (default)	0.85	1	1.15	
		Setting by reg_0x2A"[1:0] = "10"	1.0625	1.25	1.4375	
		Setting by reg_0x2A"[1:0] = "11"	1.275	1.5	1.725	
SWC Power Good Indicator						
(Power Good) Falling Threshold	$V_{OUT\_C\_PGOOD\_F}$	Setting by reg_0x27"[0] = "0" (default)	--	–5	--	% of V_{OUT_C}
		Setting by reg_0x27"[0] = "1"	--	–7.5	--	
(Power Good) Falling Propagation Delay	$t_{DLY\_PGOOD\_F\_C}$		--	5	--	µs
(Power Good) Rising Threshold	$V_{OUT\_C\_PGOOD\_R}$	Setting by reg_0x28"[7:6] = "00"	--	5	--	% of V_{OUT_C}
		Setting by reg_0x28"[7:6] = "01" (default)	--	7.5	--	
		Setting by reg_0x28"[7:6] = "10"	--	10	--	
		Setting by reg_0x28"[7:6] = "11"	--	2.5	--	
(Power Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_C}$		--	5	--	µs
SWC Protections						
Output Overvoltage Rising Threshold	$V_{OUT\_C\_OVP\_R}$	Setting by reg_0x28"[5:4] = "00"	--	7.5	--	% of V_{OUT_C}
		Setting by reg_0x28"[5:4] = "01"	--	10	--	
		Setting by reg_0x28"[5:4] = "10" (default)	--	12.5	--	
		Setting by reg_0x28"[5:4] = "11"	--	20	--	
Output Overvoltage Protection Propagation Delay	$t_{DLY\_OVP\_C}$		--	5	--	µs
Output Undervoltage Falling Threshold	$V_{OUT\_C\_UVP\_F}$	Setting by reg_0x28"[3:2] = "00" (default)	--	–10	--	% of V_{OUT_C}
		Setting by reg_0x28"[3:2] = "01"	--	–12.5	--	
		Setting by reg_0x28"[3:2] = "10"	--	–7.5	--	
		Setting by reg_0x28"[3:2] = "11"	--	–20	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Undervoltage Protection Propagation Delay	$t_{DLY\_UVP\_C}$		--	5	--	μs
SWC Current Limit						
Positive Inductor Valley Current Limit	$I_{LIM\_VALLEY\_C}$	For Low Current, valley current limited Setting by reg_0x20"[1:0] = "00"	--	0.5	--	A
		Setting by reg_0x20"[1:0] = "01"	--	1.0	--	
		Setting by reg_0x20"[1:0] = "10"	--	1.5	--	
		Setting by reg_0x20"[1:0] = "11" (default)	--	2.0	--	
VLDO_1.8V (1.8V, I_{MAX} = 25mA)						
Output Voltage	$V_{LDO\_1.8V}$	Setting by reg_0x2B"[7:6] = "00"	1.66	1.7	1.74	V
		Setting by reg_0x2B"[7:6] = "01" (default)	1.76	1.8	1.84	
		Setting by reg_0x2B"[7:6] = "10"	1.85	1.9	1.95	
		Setting by reg_0x2B"[7:6] = "11"	1.95	2.0	2.05	
Soft-Start Time	t_{SS}		--	0.25	--	ms
(Power Good) Rising Threshold	$V_{LDO\_1.8V\_PGOOD\_R}$	Setting by reg_0x1A"[2] = "0"	--	1.6	--	V
(Power Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_LDO\_1.8V}$		--	5	--	μs
Current Limit	$I_{LIM\_LDO\_1.8V}$		50	--	--	mA
VLDO_1.0V (1.0V, I_{MAX} = 20mA)						
Output Voltage	$V_{LDO\_1.0V}$	Setting by reg_0x2B"[2:1] = "00"	0.88	0.9	0.92	V
		Setting by reg_0x2B"[2:1] = "01" (default)	0.98	1.0	1.02	
		Setting by reg_0x2B"[2:1] = "10"	1.08	1.1	1.12	
		Setting by reg_0x2B"[2:1] = "11"	1.18	1.2	1.22	
Soft-Start Time	t_{SS}		--	0.12	--	ms
(Power Good) Rising Threshold	$V_{LDO\_1.0V\_PGOOD\_R}$	Setting by reg_0x1A"[0] = "0" (default)	--	–10	--	% of V_{LDO}
		Setting by reg_0x1A"[0] = "1"	--	–15	--	
(Power Good) Rising Propagation Delay	$t_{DLY\_PGOOD\_R\_LDO\_1.0V}$		--	5	--	μs
Current Limit	$I_{LIM\_LDO\_1.0V}$		50	--	--	mA

13 Typical Application Circuit

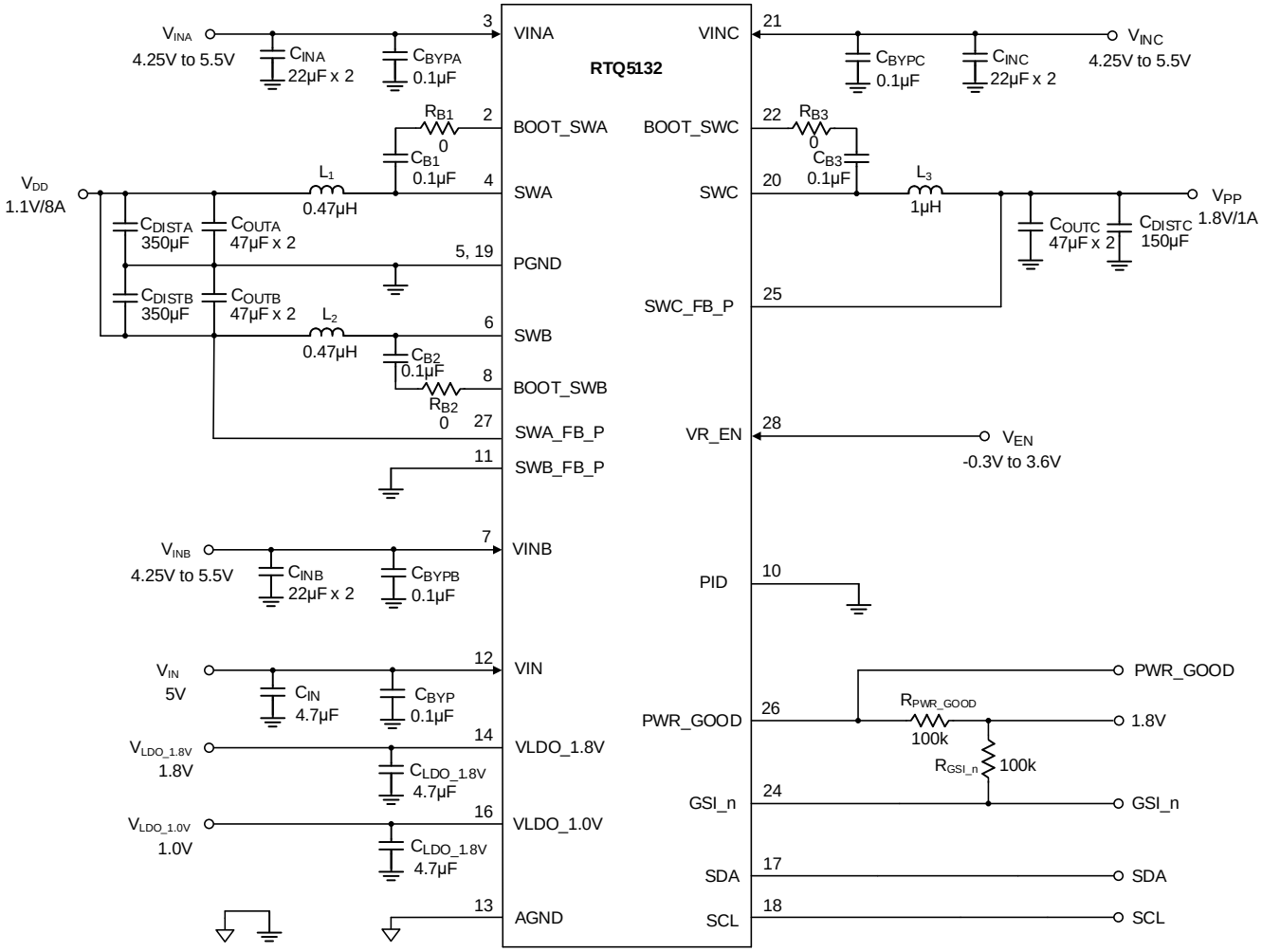


Figure 3. Typical Application Circuit when SWA and SWB are combined as Two Phase, Single Output Rail.

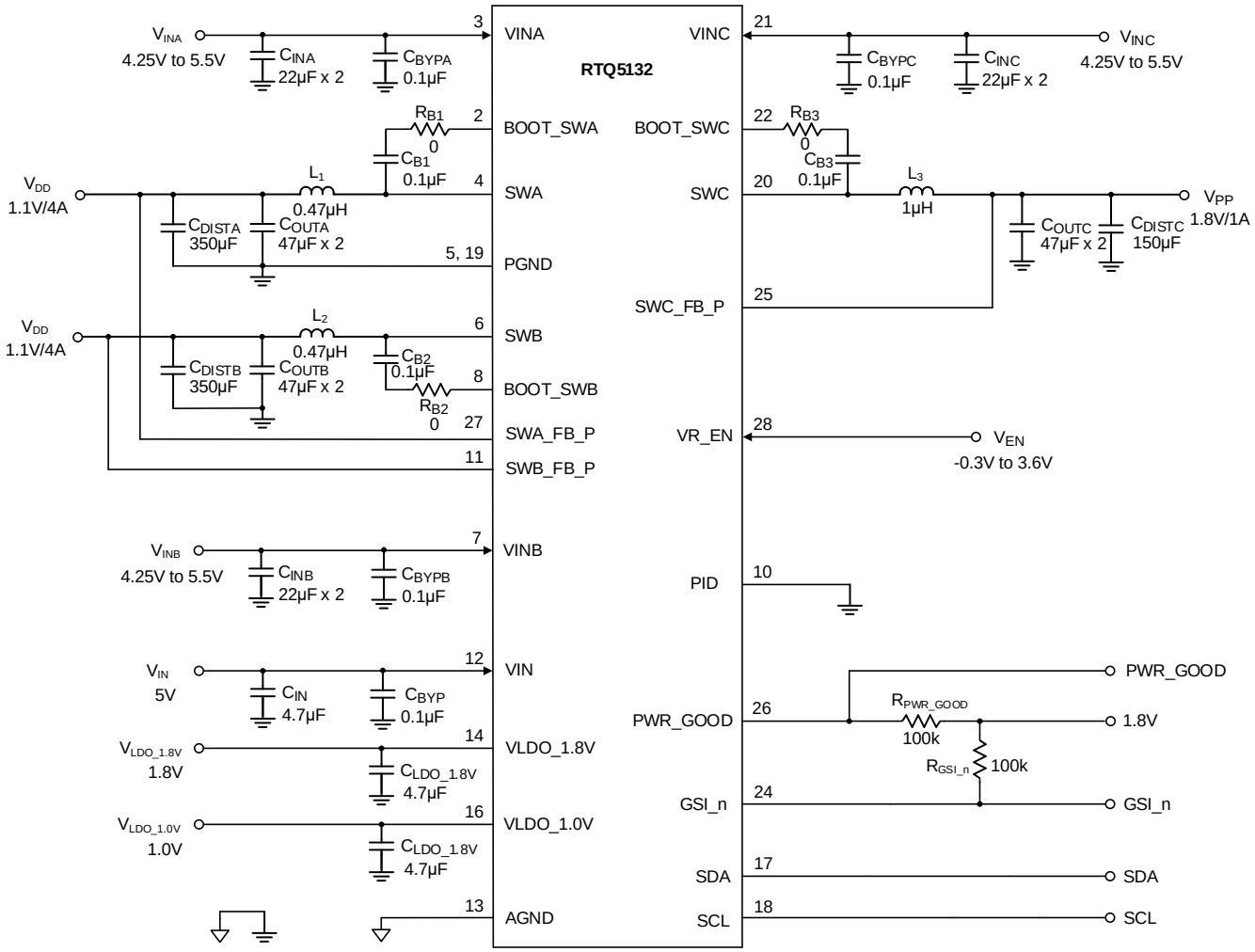
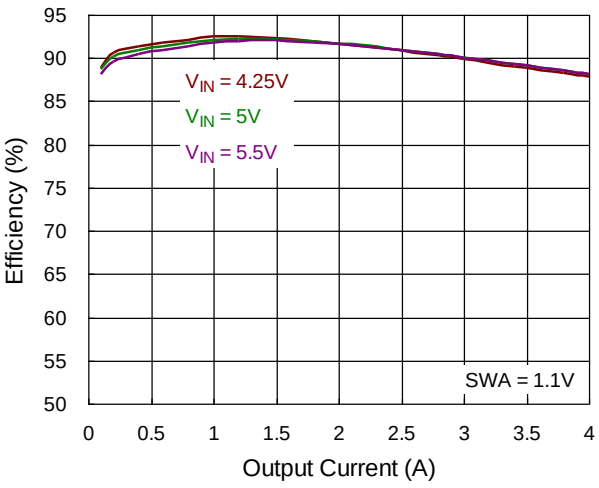


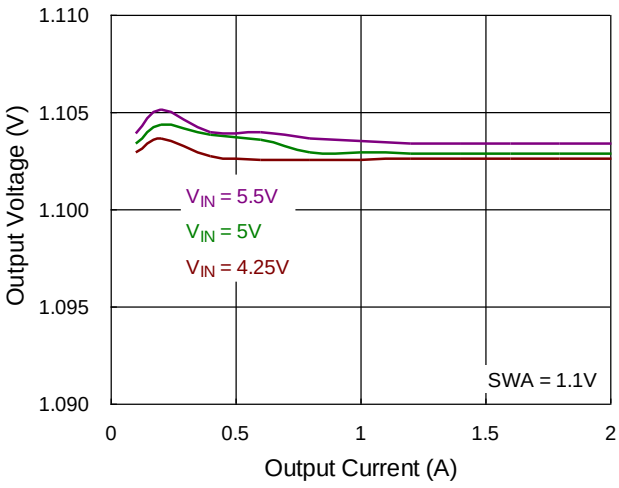
Figure 4. Typical Application Circuit when SWA and SWB are separated for 2-Outputs.

14 Typical Operating Characteristics

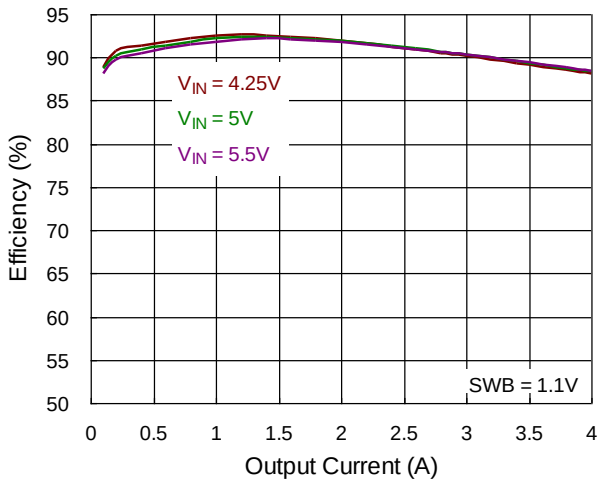
SWA Efficiency vs. Output Current



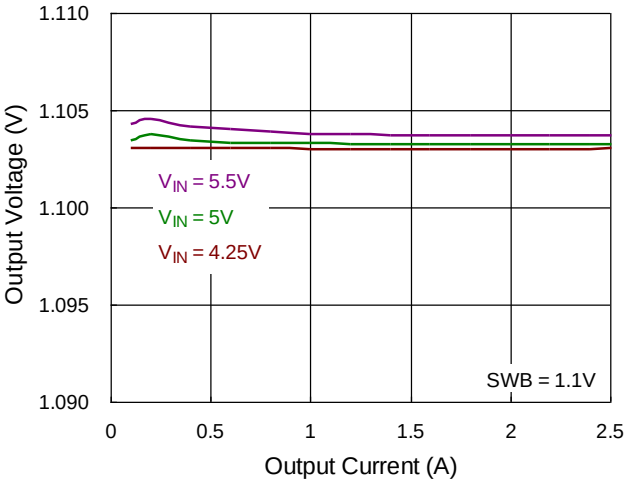
SWA Output Voltage vs. Output Current



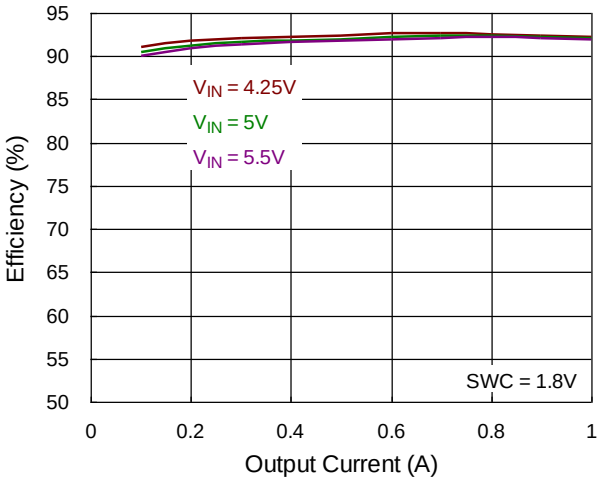
SWB Efficiency vs. Output Current



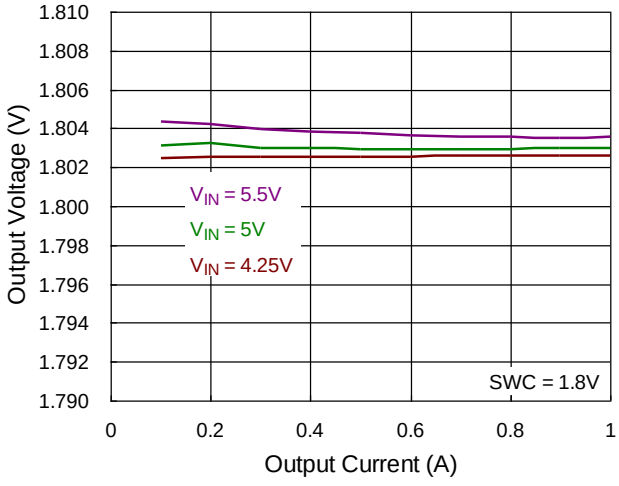
SWB Output Voltage vs. Output Current



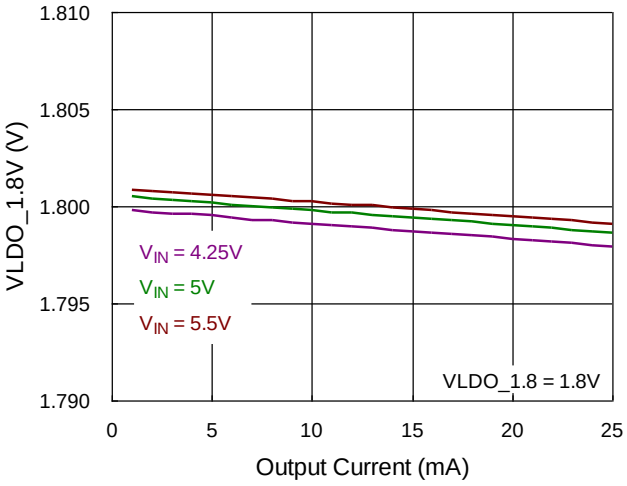
SWC Efficiency vs. Output Current



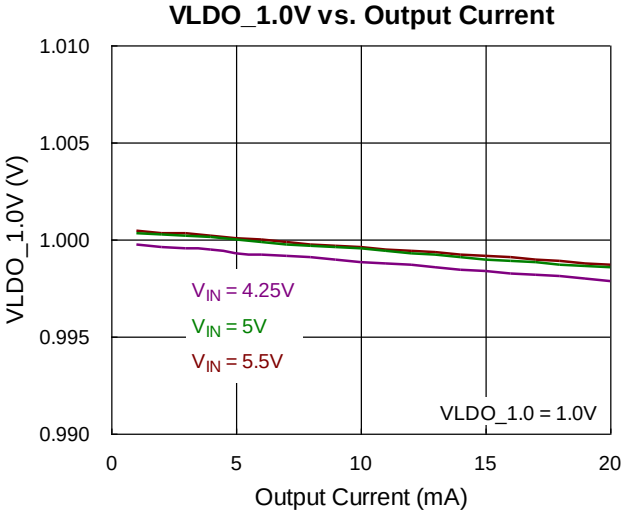
SWC Output Voltage vs. Output Current



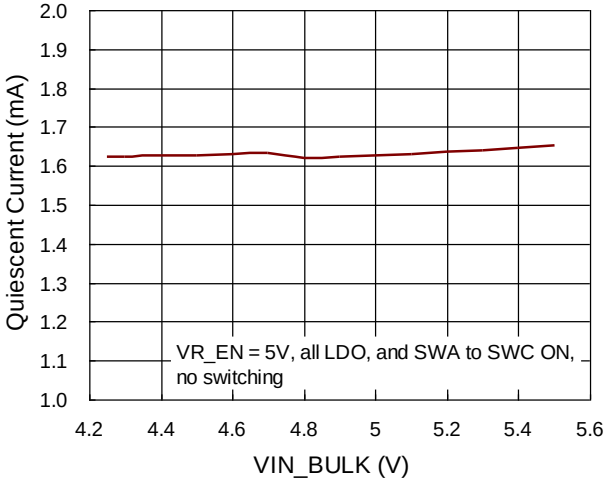
VLDO_1.8V vs. Output Current



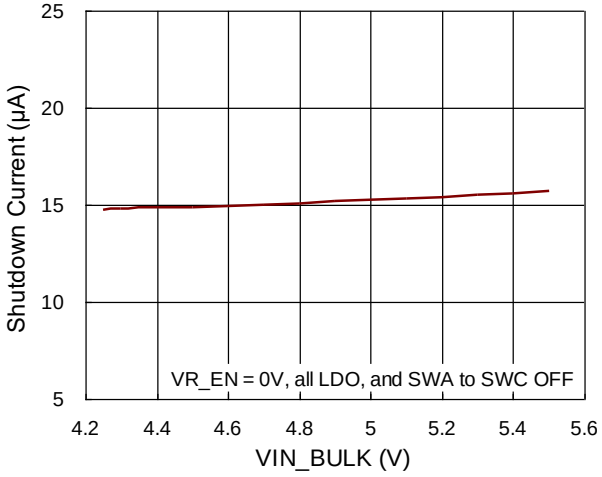
VLDO_1.0V vs. Output Current



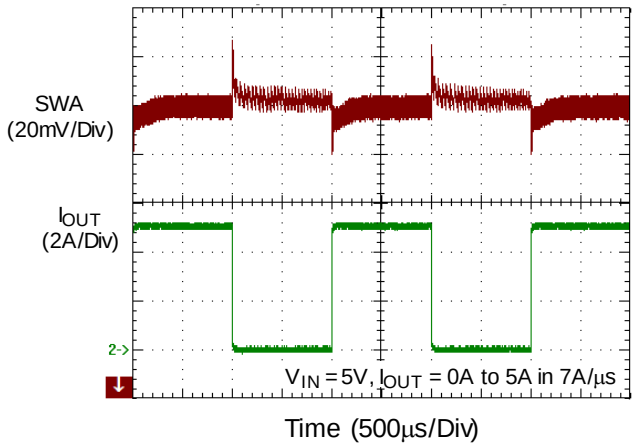
Quiescent Current vs. VIN_BULK



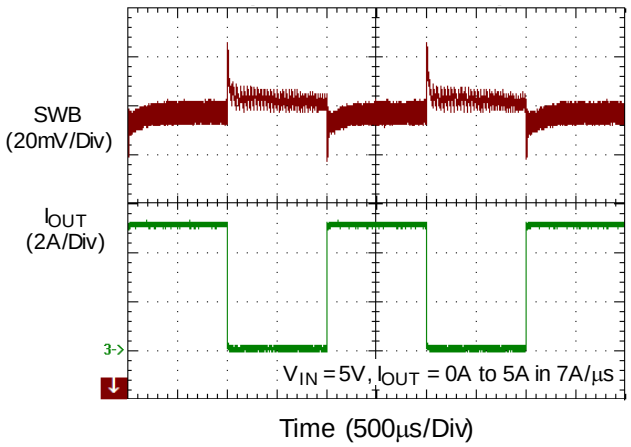
Shutdown Current vs. VIN_BULK



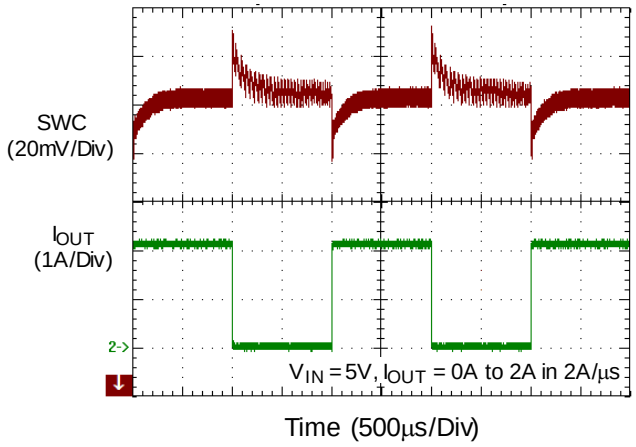
SWA Load Transient Response



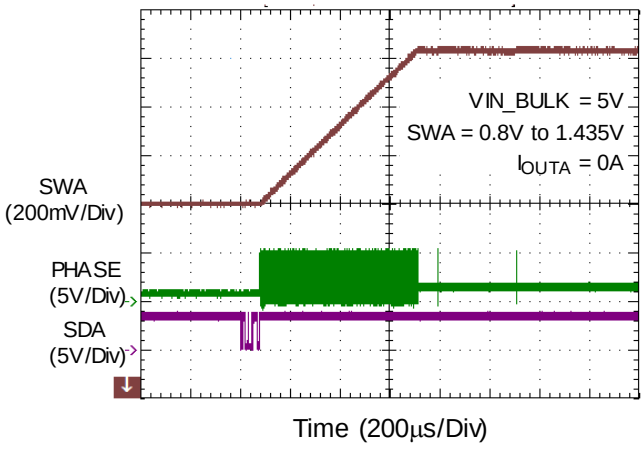
SWB Load Transient Response



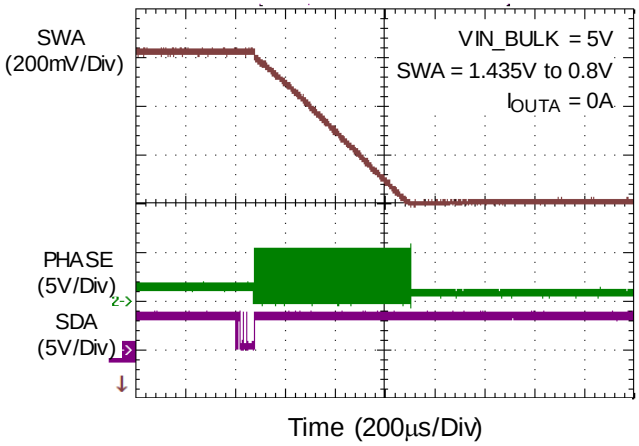
SWC Load Transient Response



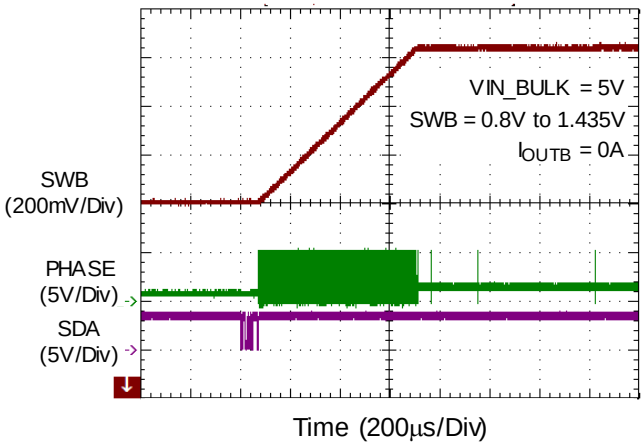
SWA VID Up



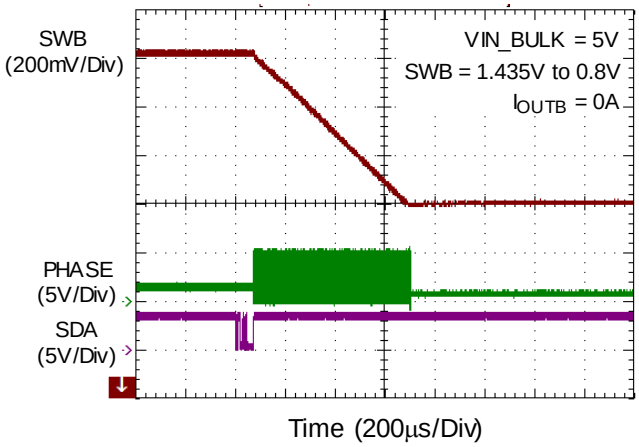
SWA VID Down



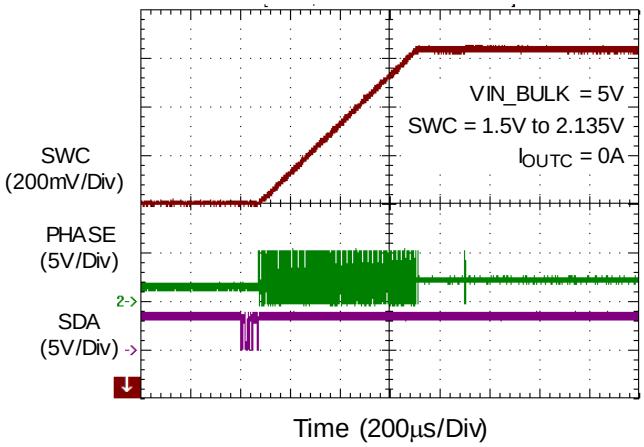
SWB VID Up



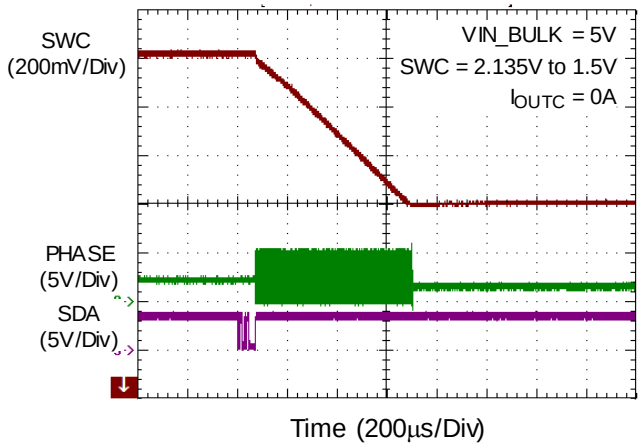
SWB VID Down



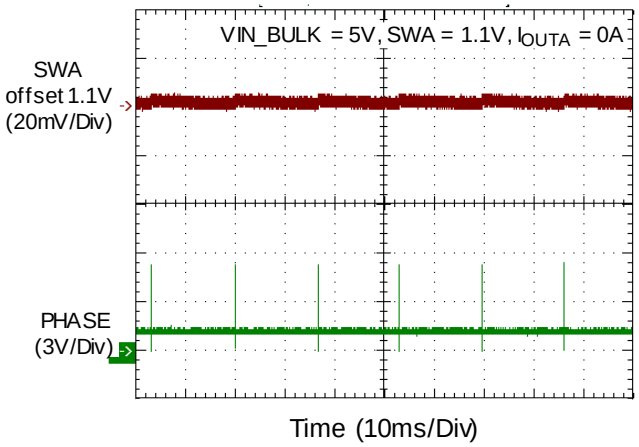
SWC VID Up



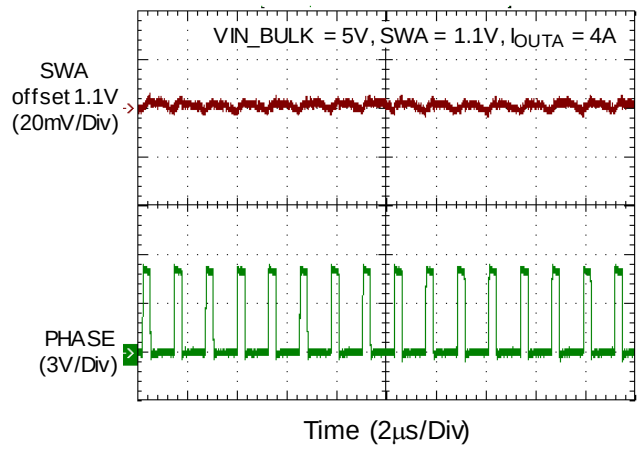
SWC VID Down



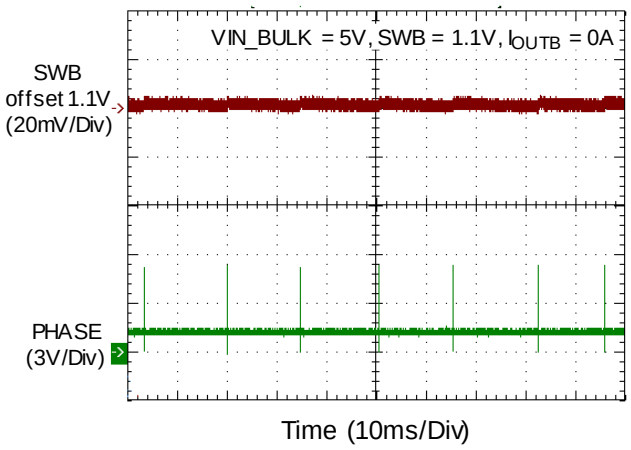
SWA Stability in DEM



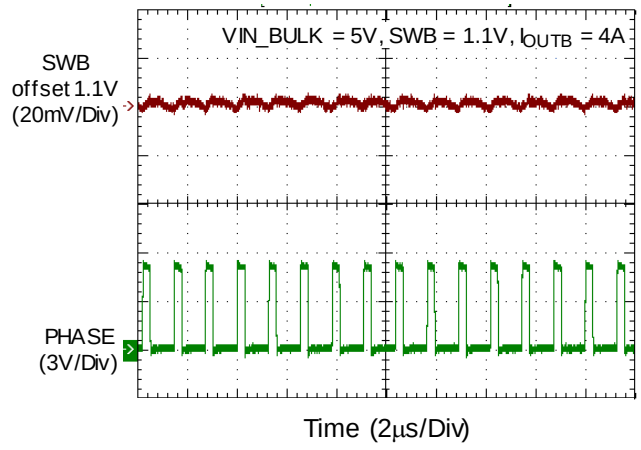
SWA Stability in CCM



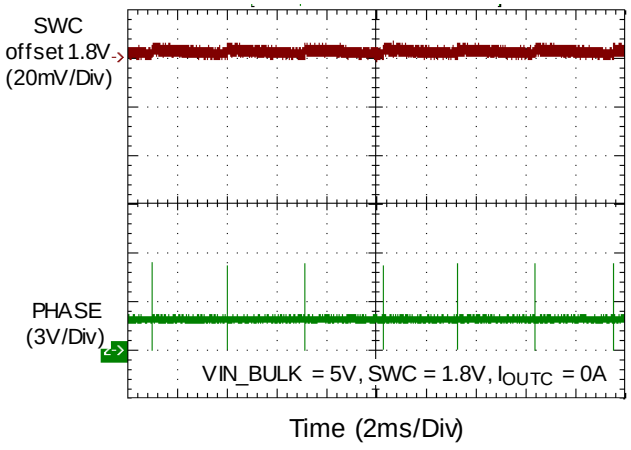
SWB Stability in DEM



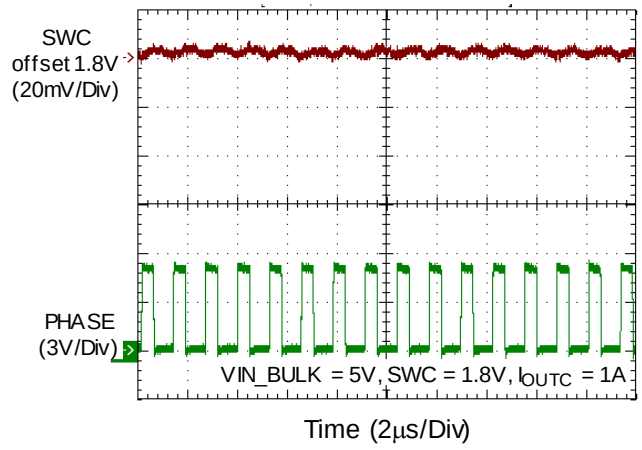
SWB Stability in CCM



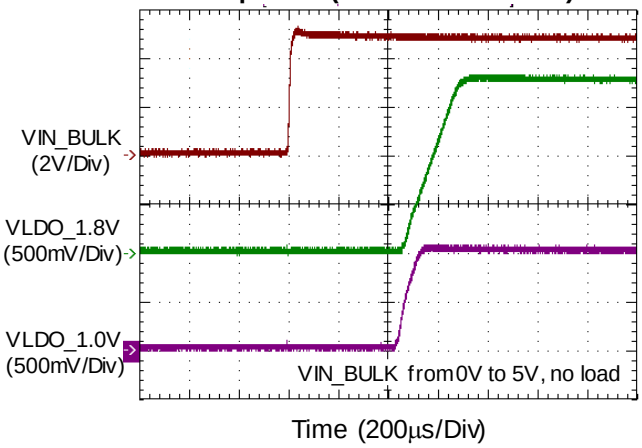
SWC Stability in DEM



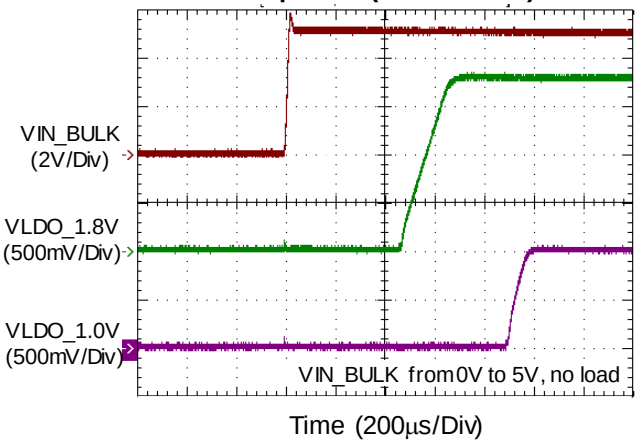
SWC Stability in CCM



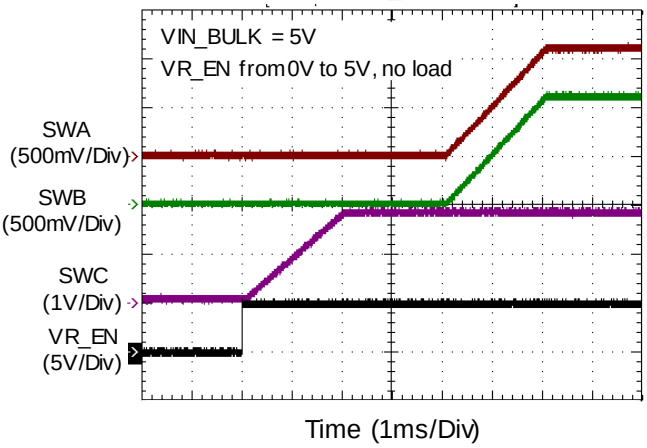
VLDO_1.8V and VLDO_1.0V Power-On Sequence (Version 2xx & 3xx)



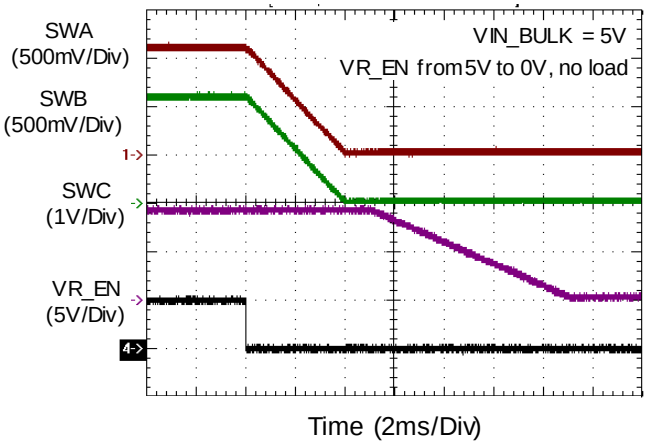
VLDO_1.8V and VLDO_1.0V Power-On Sequence (Version 5xx)



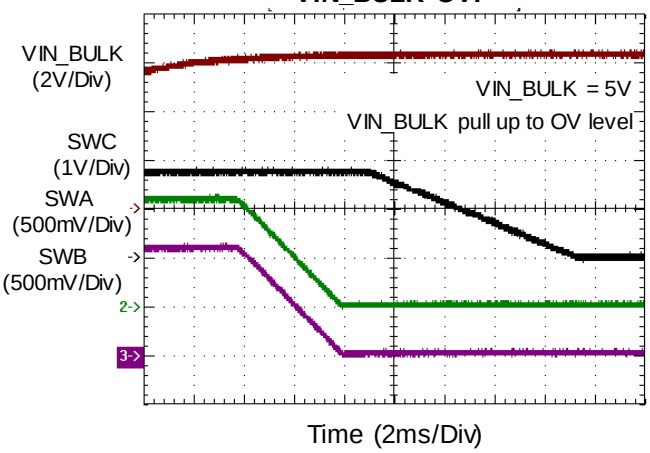
PMIC Power-On Sequence by VR_EN



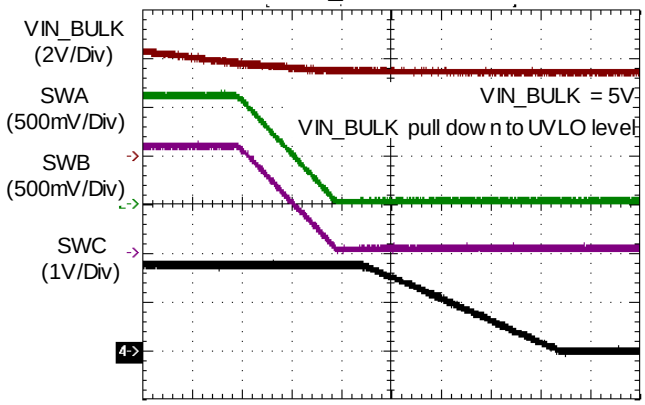
PMIC Power-Off Sequence by VR_EN



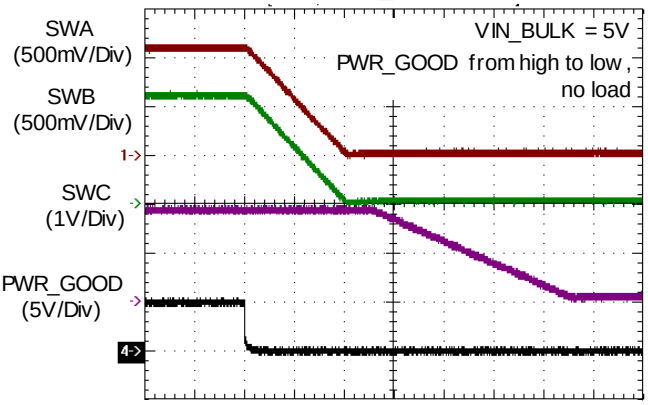
PMIC Power-Off Sequence by VIN_BULK OVP



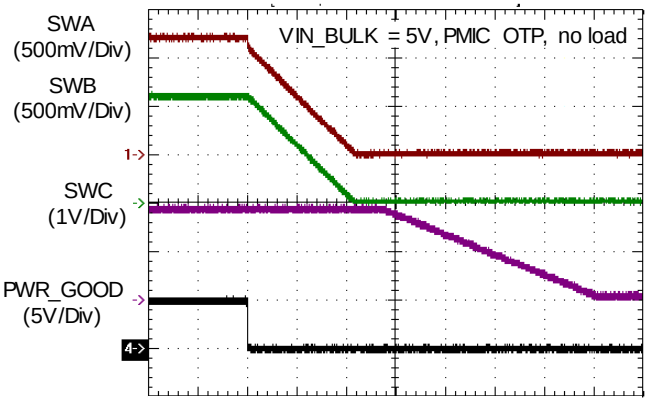
PMIC Power-Off Sequence by VIN_BULK UVLO



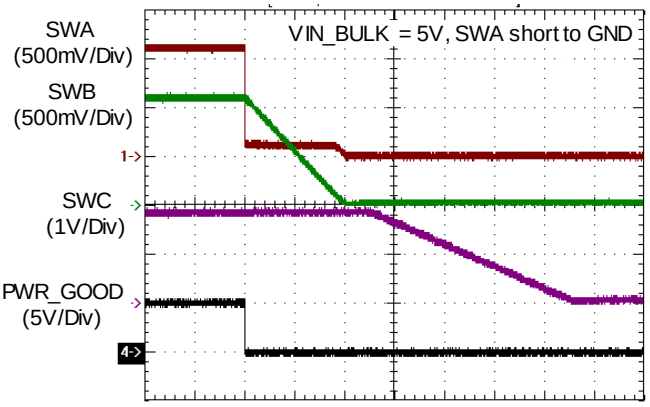
PMIC Power-Off Sequence by PWR_GOOD



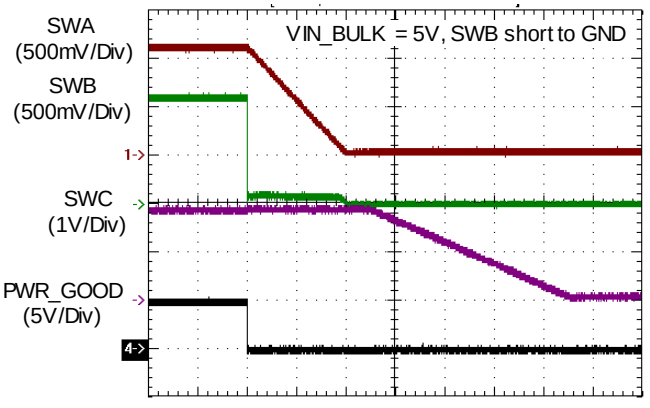
PMIC Power-Off Sequence by OTP



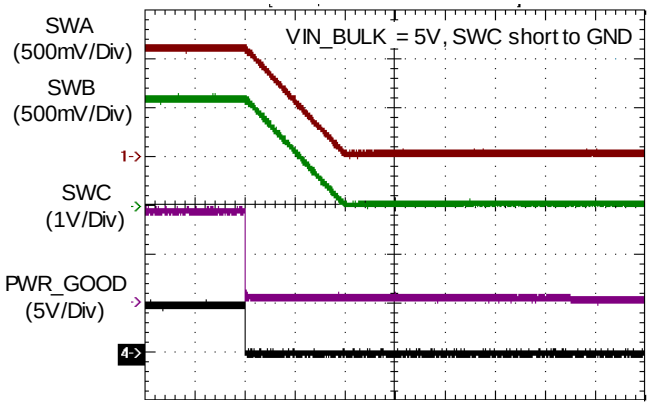
PMIC Power-Off Sequence by SWA Short to GND



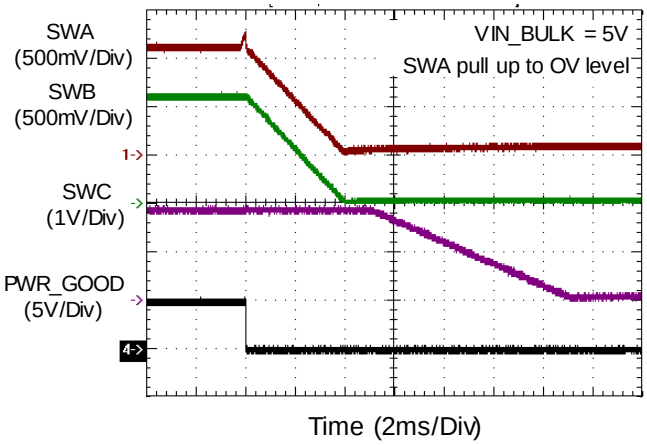
PMIC Power-Off Sequence by SWB Short to GND



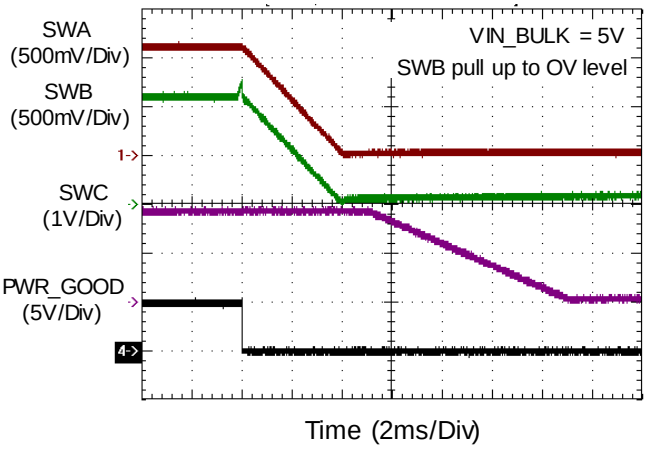
PMIC Power-Off Sequence by SWC Short to GND



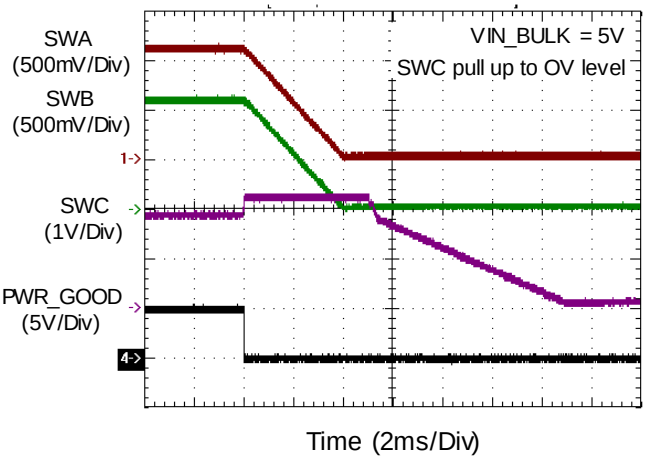
PMIC Power-Off Sequence by SWA OVP



PMIC Power-Off Sequence by SWB OVP



PMIC Power-Off Sequence by SWC OVP



15 Operation

15.1 PMIC Input Voltage Supply & Ramp Condition

The VIN_Bulk supply is used by the RTQ5132 for all three switch (SWA, SWB, and SWC) output regulators and two LDO output (VLDO_1.8V & VLDO_1.0V) regulators. Note that the VLDO_1.8V LDO output is separate and independent from the SWC output, which is for the DRAM VPP rail. The VLDO_1.0V LDO output is separate and independent from SWA or SWB.

At the first power-on, the VIN_Bulk input supply should reach a minimum threshold voltage of 4.25V before it can be detected as a valid input supply by the RTQ5132.

Once the VIN_Bulk supply is valid and stable, the RTQ5132 should assert the PWR_GOOD output low and drive VLDO_1.8V & VLDO_1.0V supply within t1.8V_Ready (typically = 500μs) and t1.0V_Ready (typically = 500μs) time, respectively. The RTQ5132 only drives the PWR_GOOD output signal low when the VIN_Bulk input supply reaches a minimum of 4.25V. The PWR_GOOD output is pulled up to either 1.8V or 3.3V on the platform or the host controller.

The PWR_GOOD pullup voltage (either 1.8V or 3.3V) is available before or after the VIN_Bulk is valid and stable. If the PWR_GOOD pullup voltage is available before the VIN_Bulk is applied, the PWR_GOOD signal is high. When the VIN_Bulk is applied to the RTQ5132, the RTQ5132 asserts the PWR_GOOD output low.

The RTQ5132 should enable the I^2C/I3C bus interface function within tManagement_Ready (maximum = 3ms). The user should not attempt to access the RTQ5132's memory registers until the tManagement_Ready timing requirement is satisfied.

During power-on, the user should:

1. Ramp up the VIN_BULK supply.

2. Hold the VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_VR_Enable time (minimum = 6.5ms).

3. Keep the VR_EN pin static, either low or high.

4. If the VR_EN signal is held low during the VIN_Bulk ramp, it may transition to high only once. Once high, it should remain high. The VR_EN signal is not allowed to transition to low during the VIN_Bulk ramp-up.

5. If the VR_EN pin is held high during the VIN_Bulk ramp-up, or transitions to high, the RTQ5132 turns on its output rails.

6. If the VR_EN pin is held low during the VIN_Bulk Ramp, assert the VR_EN signal high to turn on the RTQ5132 output rails. Alternatively, the user can issue a VR Enable command by setting the register, Register 0x32[7] = 1, via I^2C/I3C Basic bus or via DEVCTRL CCC to turn on the RTQ5132 output rails.

Figure 6 to Figure 8 show examples of the PMIC power-up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB, and SWC) is for example purposes only. The specific ramp-up sequence is configurable through power-on sequence configuration registers.

After the VR Enable command is registered on the I^2C or I3C Basic bus, or the VR_EN pin is registered high, the RTQ5132 should complete the following steps within tPMIC_PWR_GOOD_OUT:

1. Check that the VIN_Bulk Power Good status is valid.

2. Power up itself – the RTQ5132 executes Power-on Sequence Config0 to Power-on Sequence Config2 registers and configures its internal registers as programmed in the DIMM vendor's memory space registers.

3. Power up all enabled output switch regulators and prepare for normal operation.

4. Update status registers "Register 0x08" [5,3:2] and float the PWR_GOOD signal within a maximum of the tPMIC_PWR_GOOD_OUT time.

If the RTQ5132's PWR_GOOD signal is not floated within the tPMIC_PWR_GOOD_OUT time, the user can access RTQ5132 status registers for detailed information after the tPMIC_PWR_GOOD_OUT time. The RTQ5132 may NACK (Negative-Acknowledge) any host request on the I^2C or I3C Basic bus after the VR Enable command (either with the VR_EN pin high or on the I^2C/I3C Basic Bus) until the tPMIC_PWR_GOOD_OUT time expires.

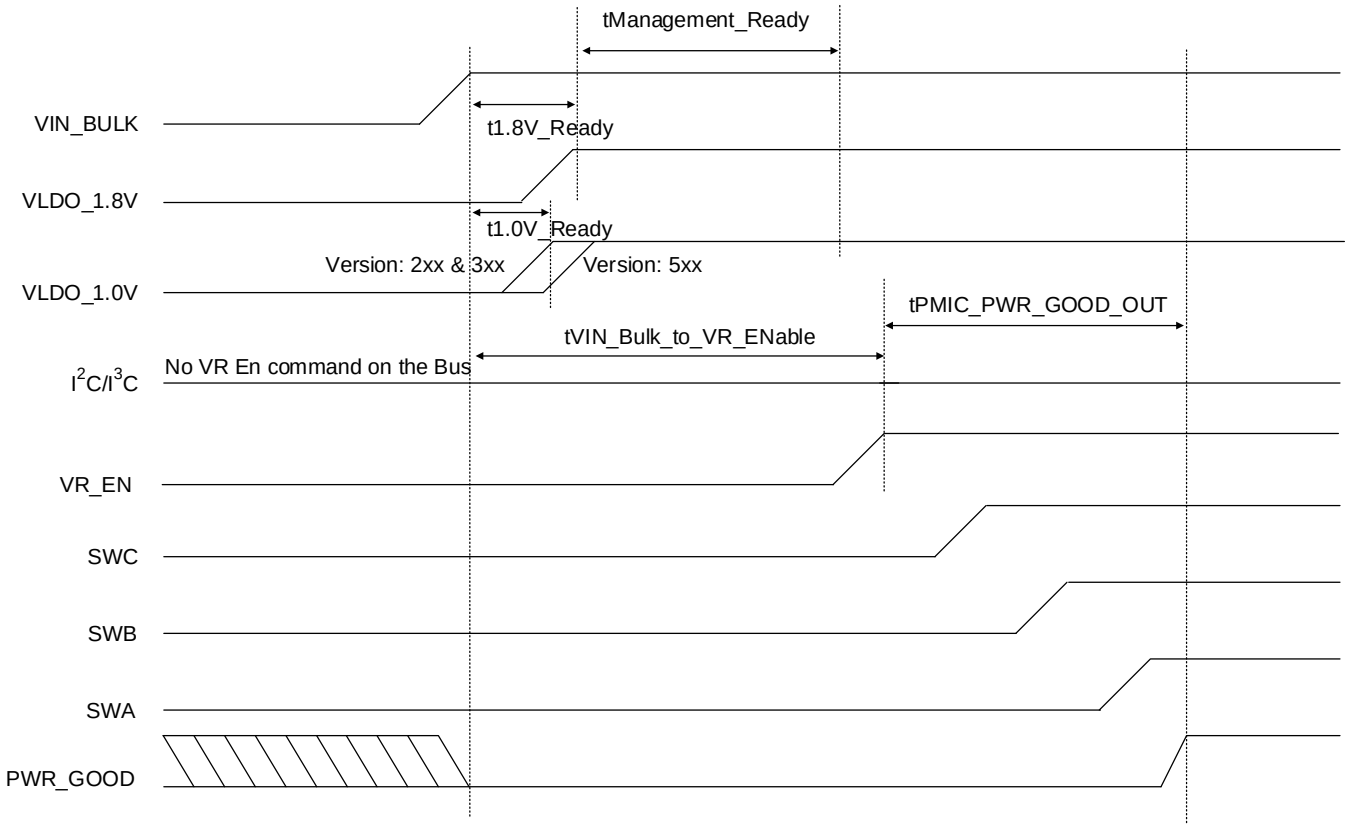


Figure 5. Power Up Sequence; VR_EN pin High after VIN_Bulk Ramp; No Bus Command

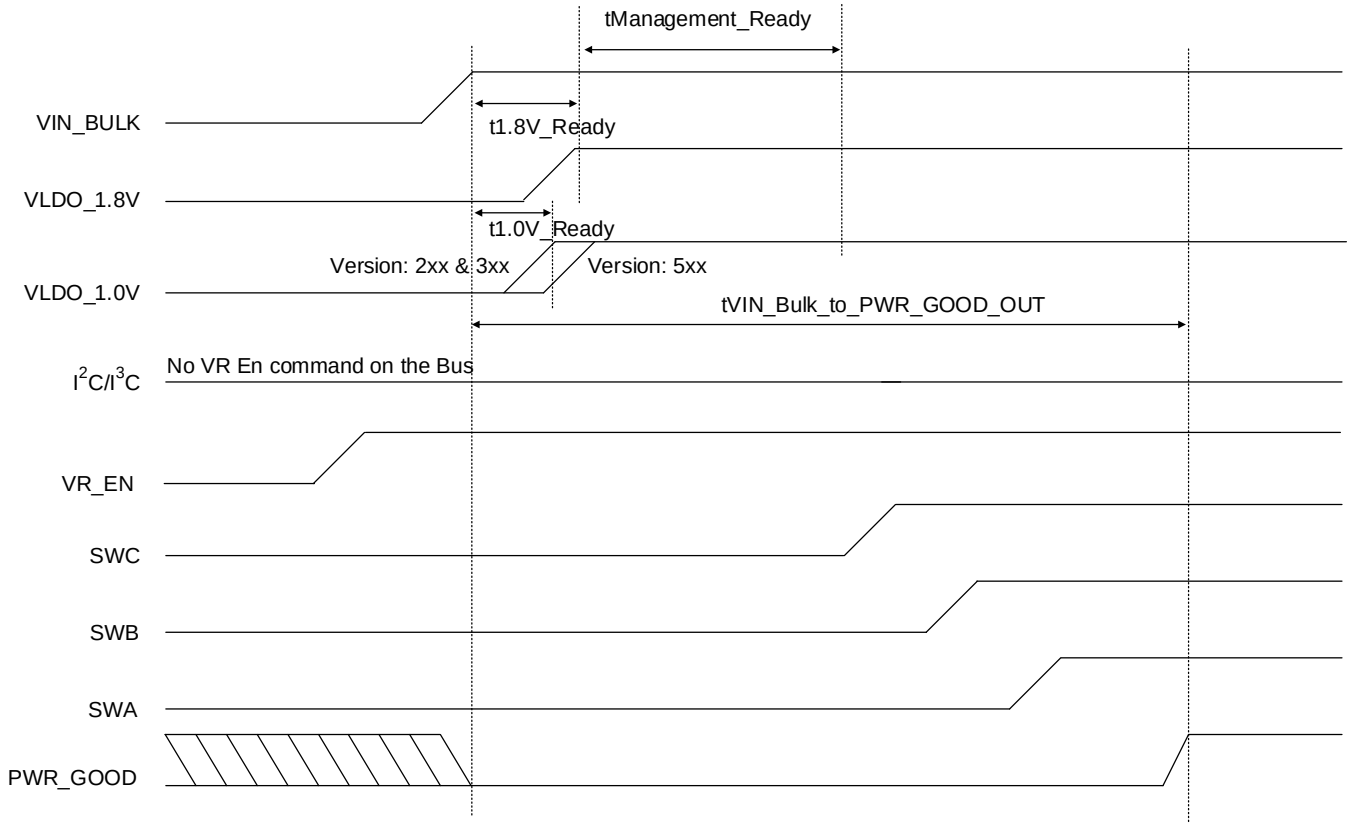


Figure 6. Power Up Sequence; VR_EN pin High before VIN_Bulk Ramp; No Bus Command

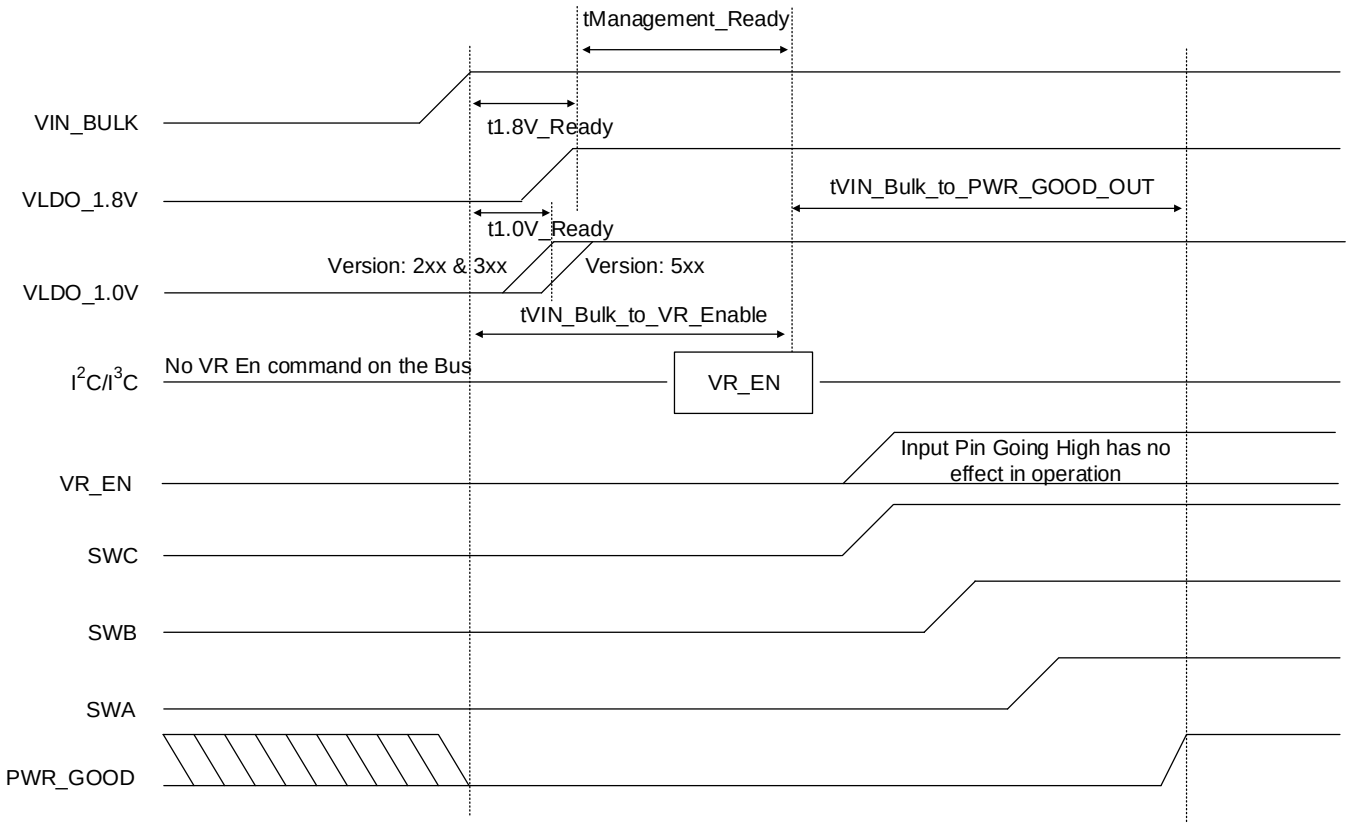


Figure 7. PMIC Power Up Sequence; w/ VR_EN Pin followed by Bus Command

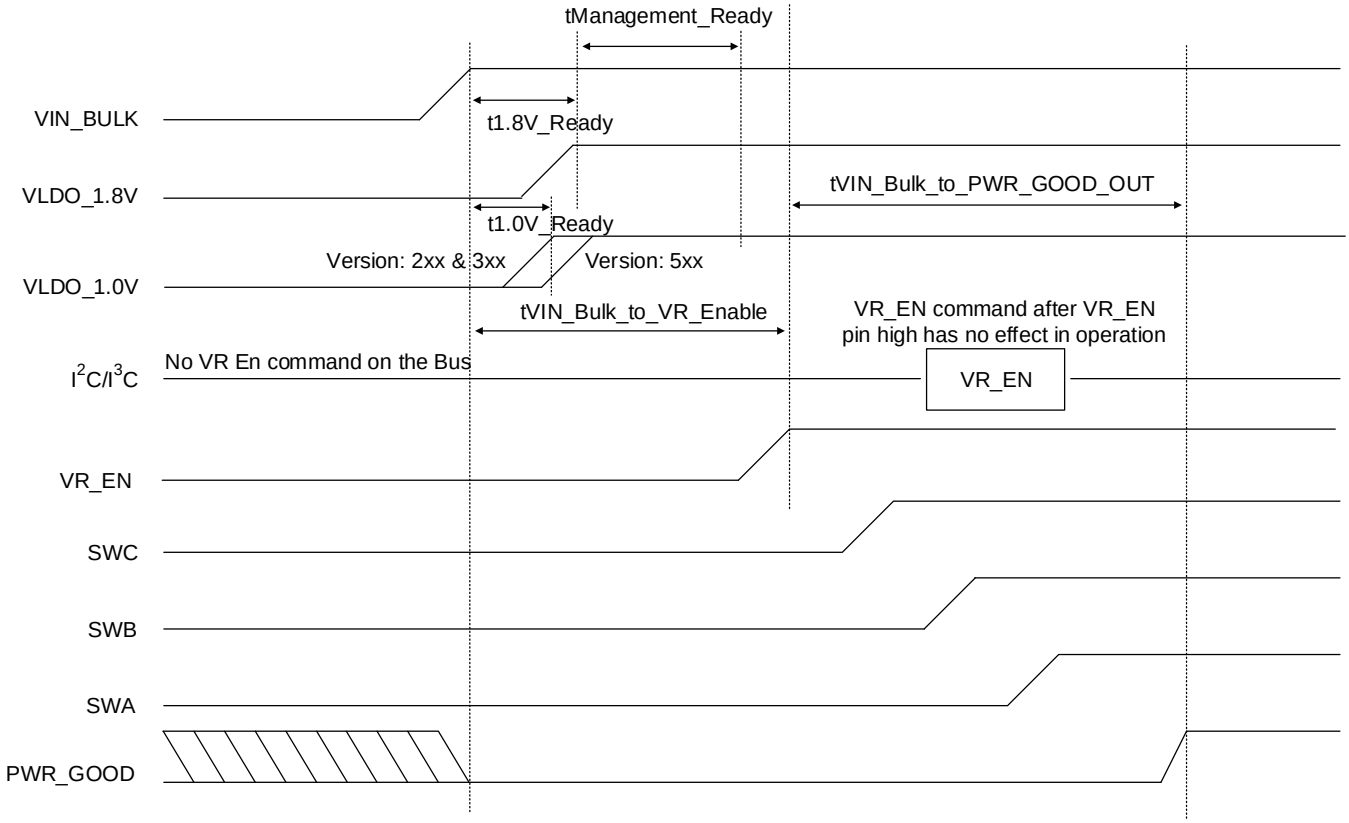


Figure 8. PMIC Power Up Sequence; w/ VR_EN Pin followed by Bus Command

15.2 Enabling PMIC Output Switch Voltage Regulators

Figure 9 below illustrates the timing relationship for when the RTQ5132 receives a VR Enable command (either via the VR_EN pin or on the I^{2}C/I3C Basic bus) and subsequently floats the PWR_GOOD output signal. The timing parameter tPMIC_PWR_GOOD_OUT applies here. This parameter represents the sum of the maximum soft-start time, the delay configured for each power-on sequence configuration register executed, plus an additional timing margin error of 5ms. The waveform indicates the soft-start time for each buck regulator output, as well as the delay time once the soft-start period concludes for each power-on sequence, from config0 to config2 registers.

It is important to note that if more than one regulator is enabled in a power-on sequence config register, and these regulators have different programmed soft-start times, the longer soft-start time will be used as the reference for the delay timer to initiate. However, each regulator will still adhere to its distinct soft-start time for powering on the buck regulator.

In the specific example shown in Figure 9, three power-on sequence config registers (config0 to config2) are used, and only one buck regulator is enabled in each of these registers.

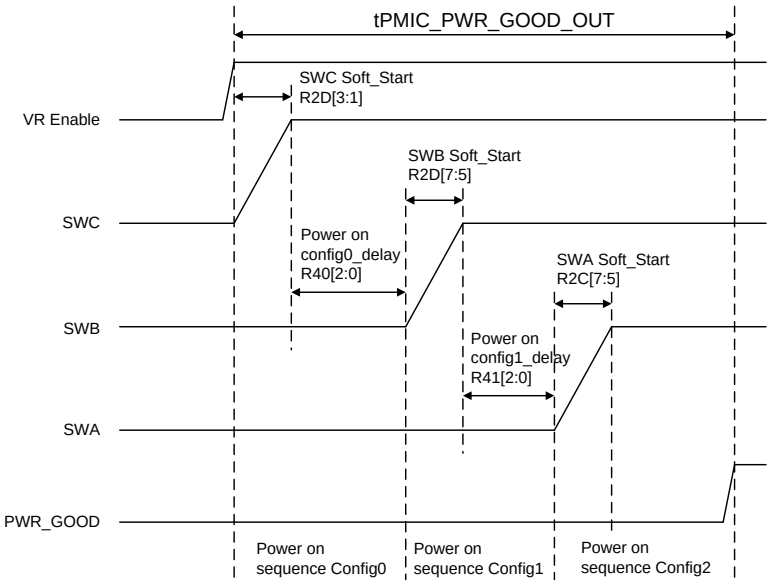


Figure 9. RTQ5132 Rails Power On Timing

15.3 Secure Mode & Programmable Mode of Operation

Before issuing a VR Enable command (using the VR_EN pin or via the I^{2}C/I3C Basic bus), the host must appropriately configure Register 0x2F [2] as required. Once the VR Enable command is received, the RTQ5132 offers two modes of operation:

Programmable Mode - In this mode, regardless of when the VR Enable command is issued, the RTQ5132 permits the host to modify any register in the host region, and the PMIC responds accordingly.

Secure Mode - In this mode, following the issuing of the VR Enable command, the RTQ5132 prohibits modification to certain registers, including Register 0x15 to Register 0x2F, Register 0x32 [7,5:0] in the host region, and Register 0x40 to Register 0x6F in the DIMM vendor region. These registers are write-protected. To make any changes, the host must power cycle the RTQ5132, defined as completely removing the VIN_Bulk input supply to the RTQ5132. This definition is consistent throughout the entire specification.

Note that Secure Mode becomes relevant only after the VR Enable command has been registered. By default, Register 0x2F [2] is set to ‘0’ when the RTQ5132 is first powered up. Before the VR Enable command is issued, the RTQ5132 permits modifications to any registers in the host region.

15.4 Power Down Output Regulators

Regardless of how the RTQ5132's output regulators are activated (whether with the VR_EN pin or a VR Enable command on the I^{2}C/I3C Basic bus), the RTQ5132 powers down its output regulators as described below, depending on its mode of operation.

Programmable Mode Operation; 0x1A[4] = ’0’

The RTQ5132 allows user to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (setting Register 0x32[7] to '0' or transitioning the VR_EN pin to low) triggers the RTQ5132 to execute the power-off sequence from config0 (Register 0x58) to config2 (Register 0x5A) in order to maintain the appropriate voltage relationships as configured in the registers. The RTQ5132 then controls the PWR_GOOD signal as follows in points (a) and (b):

(a) If the VR Disable command is initiated by a pin transition (e.g., the VR_EN pin transitioning to Low), the RTQ5132 asserts the PWR_GOOD signal to Low. The host can re-enable the RTQ5132’s output regulators by transitioning the VR_EN pin to High. After this transition, the RTQ5132 will execute the power-on sequence from config 0 to config 2 registers and will float the PWR_GOOD signal once the tPMIC_PWR_GOOD_OUT timing parameter is met.

(b) If the VR Disable command is issued on an I^{2}C/I3C bus (i.e., setting Register 0x32[7] to '0'), the RTQ5132 keeps the PWR_GOOD signal floating. This indicates an intentional command from the host rather than a fault condition. The host can re-enable the RTQ5132’s output regulators by issuing a VR_EN command on the I^{2}C/I3C bus (setting Register 0x32[7] to '1'). The RTQ5132 then executes the power-on sequence from config 0 to config 2 registers, continuing to float the PWR_GOOD signal until the tPMIC_PWR_GOOD_OUT time is satisfied. At that point, the RTQ5132 assumes normal control of the PWR_GOOD signal.

(c) Simultaneous use of the VR_EN pin and the I^{2}C/I3C bus command to control the RTQ5132 is not permitted. If the VR_EN pin transitions to Low first, the PWR_GOOD signal responds as described in point (a), and remains low even if a subsequent I^{2}C/I3C bus command is issued, as mentioned in point (b).

2. Configuring one or more bits in Register 0x2F[6,4:3] to '0' allows the user to determine a specific sequence. The RTQ5132 will not automatically execute the power-off sequence from config0 (Register 0x58) to config2 (Register 0x5A). It maintains the PWR_GOOD signal in a floating state because this represents an intentional

command by the user rather than a fault condition. Note that the user can re-enable any disabled output regulators by setting one or more bits in Register 0x2F[6,4:3] to '1', following any specific sequence it prefers. During this process, the PWR_GOOD signal remains floating.

3. If Register 0x32[5] = '1', driving PWR_GOOD input low. The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The RTQ5132 preserves all register contents including the MTP error log registers. If the user re-enables RTQ5132's output regulators by issuing VR_EN command on the I^2C/I3C Basic bus (i.e. Register 0x32[7] = '1'), the RTQ5132 executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The RTQ5132 does not require power cycle.

The RTQ5132, on its own, can generate internal VR Disable command at any time due to one or more events listed in "Trigger VR Disable". The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The RTQ5132 asserts PWR_GOOD signal low. The user can re-enable RTQ5132's output regulators with VR Enable command with either Register 0x32[7] ='1' or VR_EN pin transitions to high and RTQ5132 turns on its output regulators and floats PWR_GOOD signal. The RTQ5132 does not require power cycle.

Programmable Mode Operation; 0x1A[4] = '1'

The RTQ5132 allows user to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Register 0x32[7] ='0' or VR_EN pin transitions to low). The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The RTQ5132 controls the PWR_GOOD signal as following in bullet a and bullet b:

(a) If VR Disable command comes with a pin (i.e. VR_EN pin transitions to Low), RTQ5132 asserts PWR_GOOD signal Low. The user can re-enable the RTQ5132's output regulators by VR_EN pin transition to High. The RTQ5132 exits from P1 state and executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied.

(b) If VR Disable command is on a I^2C/I3C Basic Bus (i.e Register 0x32[7] ='0'), RTQ5132 keeps the PWR_GOOD signal floating because this is an intentional command from the user and not a fault condition. The RTQ5132 exits from P1 state with only VR_EN pin transition to High. The user can re-enable the RTQ5132's output regulators by VR_EN pin transition to High and RTQ5132 executes power-on sequence config 0 to power-on sequence config 2 registers. The RTQ5132 continues to float PWR_GOOD signal until tPMIC_PWR_GOOD_OUT timing parameter is satisfied and at that point RTQ5132 assumes normal control of PWR_GOOD signal.

(c) The simultaneous usage of VR_EN pin and I^2C/I3C bus command to turn on/off the RTQ5132 is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet (a) and PWR_GOOD signal remains low even if there is a subsequent I^2C/I3C bus command as described in bullet (b).

2. Configuring one or more bits in Register 0x2F [6,4:3] to '0' in any specific sequence desired by the user. The RTQ5132 does not execute power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) on its own. The RTQ5132 keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. Note that user can re-enable any of disabled output regulators by configuring one or more bits in Register 0x2F[6,4:3] to '1' in any specific sequence desired by the host. The RTQ5132 keeps the PWR_GOOD signal floating.

3. If Register 0x32[5] = '1', driving PWR_GOOD input low. The RTQ5132 executes power-off sequence config0

(Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The RTQ5132 preserves all register contents including the MTP error log registers. The RTQ5132 does not enter in P1 state. If user re-enables RTQ5132's output regulators by issuing VR_EN command on I^2C/I3C Basic bus (i.e. Register 0x32[7] = '1'), the RTQ5132 executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The RTQ5132 does not require power cycle.

The RTQ5132, on its own, can generate internal VR Disable command at any time due to one or more events listed in "Trigger VR Disable". The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The RTQ5132 does not enter in P1 state. The RTQ5132 assert PWR_GOOD signal low. The user can re-enable RTQ5132's output regulators with VR Enable command with either Register 0x32[7] = '1' or VR_EN pin transitions to high and RTQ5132 turns on its output regulators and floats PWR_GOOD signal. The RTQ5132 does not require power cycle.

Secure Mode Operation; R1A[4] = '0'

The RTQ5132 allows user to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The RTQ5132 asserts PWR_GOOD signal Low. The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The user can re-enable the RTQ5132's output regulators by VR_EN pin transition to High. The RTQ5132 executes power-on sequence config 0 to power-on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The RTQ5132 does not require power cycle. Note that VR Disable or Enable command on a I^2C/I3C Basic Bus (i.e Register 0x32[7] = '0' or '1') has no effect on the RTQ5132. Also, configuring one or more bits in Register0x2F[6,4:3] to '0' has no effect on the RTQ5132.
2. If Register 0x32[5] ='1', driving PWR_GOOD input low. The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only Register 0x32[7]. The RTQ5132 preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the Register 0x32[7]. When user issues VR Enable command by I^2C/I3C Basic bus, the RTQ5132 executes Power-on sequence config 0 to Power-on sequence config 2 registers, floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks register Register 0x32[7]. The RTQ5132 does not require power cycle to re-enable RTQ5132's output regulators.

The RTQ5132, on its own, can generate internal VR Disable command at any time due to one or more events listed in "Trigger VR Disable". The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The RTQ5132 assert PWR_GOOD signal low. The RTQ5132 requires power cycle. The VR Enable command with, Register 0x32[7] = '1' or VR_EN pin transitions to high has no effect on RTQ5132 and RTQ5132 keeps it PWR_GOOD signal low.

Secure Mode Operation; 0x1A[4] = '1'

The RTQ5132 allows user to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The RTQ5132 asserts PWR_GOOD signal Low. The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state.

The user can re-enable the RTQ5132's output regulators by VR_EN pin transition to High. The RTQ5132 exits from P1 state and executes power-on sequence config 0 to config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. Note that VR Disable or Enable command on a I^2C/I3C Basic Bus (i.e Register 0x32[7] = '0' or '1') has no effect on the RTQ5132. Also, configuring one or more bits in Register0x2F[6,4:3] to '0' has no effect on the RTQ5132.

2. If Register 0x32[5] ='1', driving PWR_GOOD input low. The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only Register 0x32[7]. The RTQ5132 preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the Register 0x32[7]. When user issues VR Enable command by I^2C/I3C Basic bus, the RTQ5132 executes Power-on sequence config 0 to Power-on sequence config 2 registers, floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks register Register 0x32[7]. The RTQ5132 does not require power cycle to re-enable RTQ5132's output regulators.

The RTQ5132, on its own, can generate internal VR Disable command at any time due to one or more events listed in "Trigger VR Disable". The RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A) to preserve the appropriate voltage relationship as configured in the registers. The RTQ5132 does not enter in P1 state. The RTQ5132 assert PWR_GOOD signal low. The RTQ5132 requires power cycle. The VR Enable command with either Register 0x32[7] = '1' or VR_EN

pin transitions to high has no effect on RTQ5132 and RTQ5132 keeps it PWR_GOOD signal low.

15.5 PMIC Output Rail Off Timing

The Figure 10 below shows the timing relationship once the RTQ5132 registers see VR Disable command internally due to fault condition as listed in "Events Interrupt Summary". The waveform shows each buck regulator output soft- stop time and delay time once the soft-stop time expires from each power-off sequence config0 to power-off sequence config2 registers. Note that if more than one regulators are disabled in a power-off sequence config register and if those regulators have different soft-stop time programmed, then the larger value of that soft-stop time is used as a reference for delay timer to start. Each regulator will still follow different soft-stop time to turn off the buck regulator.

The specific example in Figure 12 uses only three power-off sequence config0 to config2 registers and only one buck regulator is disabled in power-off sequence config 0, config 1 and config 2 registers.

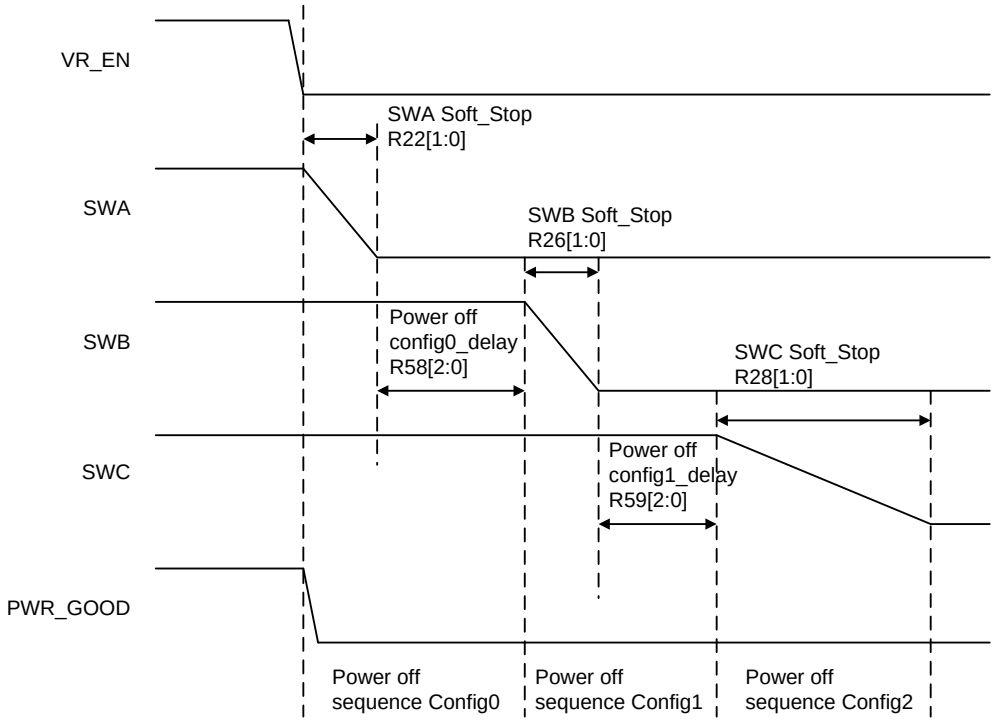


Figure 10. PMIC Power Off Timing Due to Internal Fault Condition

15.6 GSI_n Signal

The RTQ5132 features a general purpose interrupt, GSI_n, for signaling any other event to the user. The GSI_n is an open-drain output pin which needs an external pull-up resistor (~10kΩ) to 3.3V or 1.8V.

The interrupts are active Low “latched” signal (when an interrupt event occurs in the RTQ5132, a low level shall be output on the corresponding interrupt pin).

The interrupt pin is held low until both of the following requirements are met:

(1) The condition causing the interrupt (or others condition has occurred since) no longer persists.

(2) The register is cleared through I^2C or I3C write to the clear bit.

All warning status bits should be latched to ‘1’ (based on their condition occurring). The latch shall remain a ‘1’ until the corresponding clear bit is written with a ‘1’. If an exception bit is cleared, but the condition continues to persist, a new interrupt will be generated (as if it is a new condition).

When GSI_n signal is asserted, the RTQ5132 continues to operate as normal.

The user can query appropriate status registers to determine and isolate the cause of the GSI_n signal assertion.

Table 1. Summary of GSI_n Assertion Events

No	Event Description
1	Input (VIN_BULK) Power Good status.
2	Input (VIN_BULK) Overvoltage protection.
3	Output (SW[A:C] or VLDO_1.8V, VLDO_1.0V) Power Good status.
4	Output (SW[A:C]) Overvoltage protection.
5	Output (SW[A:C]) Undervoltage Lockout protection.
6	LDO Output or VIN_BULK Input Undervoltage Lockout protection.
7	Output (SW[A:C]) Current Limiter Warning event.

8	Output (SW[A:C]) High Current Consumption Warning event.
9	PMIC High Temperature Warning status.
10	PMIC Critical Temperature protection.
11	PEC Error.
12	Parity Error.

15.7 Idle State and Quiescent Power State

Quiescent Power State definition: VIN_Bulk nominal = 5.0V. All circuits including RTQ5132 switch output and LDO output regulators are off. VR_EN signal is at static low or high level. I^2C or I3C Basic interface access is not allowed and is pulled high. PID signal is at static low or high level. This state is only applicable if Register 0x1A[4] = '1'. This state is labeled as P1 state below.

Idle Power State definition: VIN_Bulk nominal = 5.0V. All circuits including RTQ5132 switch output and LDO output regulators are on with 0A load. VR_EN signal is at static low or high level. I^2C or I3C Basic interface access is allowed but bus is pulled high. PID signal is at static low or high level. This state is only applicable if Register 0x1A[4] = '0'. This state is the same as P3 state but load on all switch outputs regulators and LDO output regulators is 0A.

Table 2. High Level Finite State Description

State	Description
P0	1. VIN_Bulk is invalid
P1	1. 0x1A[4] = '1' 2. Entry from P3 State Only
P2_B	1. Transition from P0 or P1 State; Before VR Enable Command 2. All Switch Regulators are OFF 3. All LDOs are ON 4. PWR_GOOD Output = L 5. VR_EN Input = L 6. 0x32[7] = '0'
P2_A1 (No Fault Event)	1. Transition from P3; After VR Enable Command 2. All Switch Regulators are OFF 3. All LDOs are ON 4. PWR_GOOD Output = L or H 5. VR_EN Input = L or H 6. 0x32[7] = '0'
P2_A2 (Fault Event)	1. Transition from P3; After VR Enable Command 2. All Switch Regulators are OFF 3. All LDOs are ON 4. PWR_GOOD Output = L 5. VR_EN Input = L or H 6. 0x32[7] = '0'
P3 (Regulation Mode or Bulk Link Monitor Mode)	1. All Switch Regulators are ON 2. 0x32[7] = '1'

15.8 Function Interrupt - PWR_GOOD and GSI_n Output Signals

This section defines the output functionality of GSI_n pin and PWR_GOOD pin.

When mask register bits are not set, the RTQ5132 asserts its GSI_n output and PWR_GOOD output signals as

shown in Table 3 when any event occurs. The table also highlights 9 events that cause RTQ5132 to generate internal VR Disable command. For other events that does not trigger internal VR Disable command, the RTQ5132 continues to operate as normal.

Table 3. Events Interrupt Summary

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	PWR_GOOD Output	GSI_n
VIN_BULK Overvoltage	0x08[0]	0x10[0]	0x15[0]	0x1B[7]	Yes	Low	Low
SWA Output Power Good	0x08[5]	0x10[5]	0x15[5]	0x21[1:0], 0x22[7:6]	No	Low	Low
SWB Output Power Good	0x08[3]	0x10[3]	0x15[3]	0x25[1:0], 0x26[7:6]	No	Low	Low
SWC Output Power Good	0x08[2]	0x10[2]	0x15[2]	0x27[1:0], 0x28[7:6]	No	Low	Low
1.8V LDO Power Good	0x09[5]	0x11[5]	0x16[5]	0x1A[2]	No	Low	Low
1.0V LDO Power Good	0x33[2]	0x14[2]	0x19[2]	0x1A[0]	No	Low	Low
SWA Output Overvoltage	0x0A[7]	0x12[7]	0x17[7]	0x22[5:4]	Yes	Low	Low
SWB Output Overvoltage	0x0A[5]	0x12[5]	0x17[5]	0x26[5:4]	Yes	Low	Low
SWC Output Overvoltage	0x0A[4]	0x12[4]	0x17[4]	0x28[5:4]	Yes	Low	Low
SWA Output Undervoltage	0x0B[3]	0x13[3]	0x18[3]	0x22[3:2]	Yes	Low	Low
SWB Output Undervoltage	0x0B[1]	0x13[1]	0x18[1]	0x26[3:2]	Yes	Low	Low
SWC Output Undervoltage	0x0B[0]	0x13[0]	0x18[0]	0x28[3:2]	Yes	Low	Low
VIN_BULK Input Undervoltage	N/A	N/A	N/A	3.8V	Yes	Low	Low
SWA Output Current Limit	0x0B[7]	0x13[7]	0x18[7]	0x20[7:6]	No	High	Low
SWB Output Current Limit	0x0B[5]	0x13[5]	0x18[5]	0x20[3:2]	No	High	Low
SWC Output Current Limit	0x0B[4]	0x13[4]	0x18[4]	0x20[1:0]	No	High	Low
SWA Output High Current /Power	0x09[3]	0x11[3]	0x16[3]	0x1C[7:2]	No	High	Low
SWC Output High Current /Power	0x09[0]	0x11[0]	0x16[0]	0x1F[7:2]	No	High	Low
High Temperature Warning	0x09[7]	0x11[7]	0x16[7]	0x1B[2:0]	No	High	Low

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	PWR_GOOD Output	GSI_n
Critical Temperature	0x08[6]	N/A	N/A	0x2E[2:0]	Yes	Low	Low
PEC Error	0x0A[3]	0x12[3]	0x17[3]	N/A	No	High	Low
Parity Error	0x0A[2]	0x12[2]	0x17[2]	N/A	No	High	Low

- The user is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or PWR_GOOD signal assertion. The user may attempt to clear or mask the appropriate corresponding interrupt event. The RTQ5132 keeps the GSI_n signal asserted or PWR_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the user. Table 4 and Table 5 show the RTQ5132's response of GSI_n signal and PWR_GOOD output signal for each event before and after user issues the Clear command. The Table 4 and Table 5 assume that all mask bits are either '0' or '1' for simplicity.

Table 4. RTQ5132 Response for Clear Command by Host (Part I)

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			0x2F[1:0] = "00" or "01" or "10"		0x2F[1:0] = "00"		0x2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
1.8V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0V LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Undervoltage	Low	Low	Low	High	Low	High	Low	High

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			0x2F[1:0] = "00" or "01" or "10"		0x2F[1:0] = "00"		0x2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWC Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
VIN_BULK Input Undervoltage	Low	Low	N/A	N/A	N/A	N/A	N/A	N/A
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 5 shows the RTQ5132's response of GSI_n signal and PWR_GOOD signal for each event before and after user issues the Clear command. The table assumes that all mask bits are '1'.

Table 5. RTQ5132 Response for Clear Command by Host (Part II)

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	0x2F[1:0] = "01"		0x2F[1:0] = "01"		0x2F[1:0] = "10"		0x2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	0x2F[1:0] = "01"		0x2F[1:0] = "01"		0x2F[1:0] = "10"		0x2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
1.8V LDO Power Good	High	Low	High	High	High	High	High	High
1.0V LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Overvoltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Undervoltage	Low	Low	Low	High	Low	High	Low	High
VIN_BULK Input Undervoltage	Low	Low	N/A	N/A	N/A	N/A	N/A	N/A
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	0x2F[1:0] = "01"		0x2F[1:0] = "01"		0x2F[1:0] = "10"		0x2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when user masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of PWR_GOOD output signal. The RTQ5132 functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of PWR_GOOD output signal.

15.9 Power Good Signal

The PWR_GOOD output signal type can be configured as either output only or input and output through register Register 0x32[5]. By default, PWR_GOOD is an output signal. The PWR_GOOD signal can only be configured once, at power on, before issuing VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus). The PWR_GOOD signal configuration applies to both secure mode or programmable mode of operation.

15.10 Power Good as Output Only Signal

When Register 0x32[5] = '0', the PWR_GOOD signal type is output only; the input of PWR_GOOD signal is ignored. The RTQ5132's PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (SWA, SWB, SWC, VLDO_1.8V, VLDO_1.0V). The RTQ5132 floats PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator's (SWA, SWB, SWC, VLDO_1.8V, VLDO_1.0V) tolerances are maintained as configured in the appropriate register space. At first power-up, when input supply VIN_Bulk is ramped up and stable, the RTQ5132 keeps PWR_GOOD pin asserted to low; however, the RTQ5132 updates corresponding status register. By default, the Register 0x32[5] = '0'. Once RTQ5132 receives VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) from the user, the RTQ5132 enables all appropriate output regulators and updates corresponding status registers and enters into operating state called as "Regulation". At this point, RTQ5132 floats PWR_GOOD pin and the external board pull-up resistor pulls the pin high as other PMICs on different DIMM may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e no other PMIC is driving the PWR_GOOD pin low), the RTQ5132 remains in "Regulation" state.

Once the PWR_GOOD pin is high, if RTQ5132 detects any condition either on VIN_Bulk input supply or any of the output regulators (SWA, SWB, SWC, VLDO_1.8V, VLDO_1.0V) that causes the RTQ5132 to update it status registers to indicate the power status is not good, then RTQ5132 asserts PWR_GOOD pin low and keeps it asserted until the user explicitly takes a specific action corresponding to it. The RTQ5132 does not automatically let the PWR_GOOD pin float (i.e get High) even if the condition that triggered the RTQ5132 to assert the PWR_GOOD pin no longer exists. In other words, the RTQ5132's PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the user.

15.11 PWR_GOOD as Input & Output Signal

When Register 0x32[5] = '1', the PWR_GOOD signal type is both input and output and is only applicable after user issues VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus). Also note that simultaneous usage

of PWR_GOOD pin as IO and VR_EN pin is not allowed and considered an illegal configuration. In other words, if VR_EN pin is intended to be used to turn on and turn off output rails, the PWR_GOOD pin must be configured as output only. If PWR_GOOD pin is intended to be used as IO, the VR_EN pin must be connected to GND on the board.

The RTQ5132's PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (SWA, SWB, SWC, VLDO_1.8V, VLDO_1.0V). The RTQ5132 floats PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator's (SWA, SWB, SWC, VLDO_1.8V, VLDO_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power-up, when input supply VIN_Bulk is ramped up and stable, the RTQ5132 keeps PWR_GOOD pin asserted to low; however, the PMIC updates corresponding status register. The user, prior to issuing VR Enable command on I^2C/I3C Basic bus, can configure the Register 0x32[5] = '1'. When user issues VR Enable command on I^2C/I3C Basic bus, the RTQ5132 turns on its output regulators and updates corresponding status registers and enters into operating state called "Regulation". At this point, the RTQ5132 floats PWR_GOOD pin and waits for external board pull-up resistor to pull the pin high as other PMICs on different DIMM may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e no other PMIC is driving the PWR_GOOD pin low), the RTQ5132 automatically enters into operating state called "Bulk Control Link Monitor".

Once the PWR_GOOD pin is high, if RTQ5132 detects any condition either on VIN_Bulk input supply or any of the output regulators (SWA, SWB, SWC, VLDO_1.8V, VLDO_1.0V) that causes the RTQ5132 to update it status registers to indicate the power status is not good, then RTQ5132 asserts PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The RTQ5132 does not automatically let the PWR_GOOD pin float (i.e get High) even if the condition that triggered the RTQ5132 to assert the PWR_GOOD pin no longer exists. In other words, the RTQ5132's PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the user.

If RTQ5132 is operating in Secure mode of operation, RTQ5132 allows PWR_GOOD input signal to be low at any time. The host must keep the PWR_GOOD signal low for minimum tPWR_GOOD_Low_Pulse_Width to issue command to RTQ5132 to execute VR Disable. When RTQ5132 detects PWR_GOOD signal low, the RTQ5132 internally triggers VR Disable command and shuts off all output regulators (the RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A); drives PWR_GOOD signal low and unlocks only Register 0x32[7]. The RTQ5132 preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the Register 0x32 [7]. As long as there is valid VIN_Bulk input supply, the RTQ5132 allows read access to all its configuration registers. The RTQ5132 allows write access to non-locked configuration registers and Register 0x32[7]. If user issues VR Enable command by I^2C/I3C bus, the RTQ5132 executes Power-on sequence config 0 to Power-on sequence config 2 registers, floats PWR_GOOD output signal and re-locks Register 0x32[7].

If RTQ5132 is in Programmable mode of operation, RTQ5132 allows PWR_GOOD input signal low at any time. The user must keep the PWR_GOOD signal low for minimum tPWR_GOOD_Low_Pulse_Width to issue command to RTQ5132 to execute VR Disable. When RTQ5132 detects PWR_GOOD signal low, the RTQ5132 internally triggers VR Disable command and shuts off all output regulators (the RTQ5132 executes power-off sequence config0 (Register 0x58) to power-off sequence config2 (Register 0x5A); drives PWR_GOOD signal low. The RTQ5132 preserves all register contents including the MTP error log registers. As long as there is valid VIN_Bulk input supply, the RTQ5132 allows read and write access to all its configuration registers. The user can issue VR Enable command with VR_EN command on I^2C/I3C Basic bus (i.e. Register 0x32[7] = '1') again to turn on the RTQ5132's output regulator and RTQ5132 will execute Power On Config0 to Config2 registers and floats PWR_GOOD output signal.

15.12 Input Overvoltage Protection

An input overvoltage protection mechanism is implemented to limit the voltages to the RTQ5132. The RTQ5132 actively monitors the input voltage VIN_BULK rail.

When VIN_BULK input goes above the threshold set in Register 0x1B[7].

When this event lasts longer than tInput_OV_GSI_Assertion time (max. = 10μs), the RTQ5132 sets the Register 0x08[0] accordingly and drives GSI_n output signal as shown in Table 3 at the same time. Note that at this point, the RTQ5132 does not assert PWR_GOOD output signal. The RTQ5132 allows access to all registers and continues to operate as normal. The user can clear the VIN_BULK input overvoltage status register by writing '1' to Register 0x10[0] appropriately or by writing '1' to global status clear Register 0x14[0]. If the input overvoltage condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the status Register 0x08[0] will remain at '1'.

In programmable mode, if VIN_BULK input supply overvoltage condition persists greater than tInput_OV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The output regulators stop switching once VR disable command is issued by the RTQ5132, and following the power-off sequence Config0 to Config3 to discharge the output voltage by an internal discharging resistor. The RTQ5132 keeps VLDO_1.8V and VLDO_1.0V LDO output regulators active. The RTQ5132 allows access to all registers. The user can query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once the user determines the cause, the user must first clear the VIN_BULK input overvoltage status register as well as any other relevant status registers individually or by writing '1' to global status clear Register 0x14[0] which de-asserts the GSI_n signal. If the input overvoltage condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the status Register 0x08[0] will remain at '1'. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5132's output switching regulator by issuing VR Enable command. The RTQ5132 enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal and input overvoltage condition is no longer present.

In secure mode, if VIN_BULK input supply overvoltage condition persists greater than tInput_OV_VR_Disable time (max. = 20μs), then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators by executing Power-off sequence configuration registers, asserts PWR_GOOD signal low and returns to configuration mode. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

Output Power Good Status (SWABC, LDO_1.8V, LDO_1.0V)

The RTQ5132 provides output power good indicators to determine that the output regulators have crossed the desired voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWB and SWC is programmed in Register 0x21[7:1], Register 0x25[7:1] and Register 0x27[7:1] respectively. The RTQ5132 offers the PWR_GOOD condition to be set independently for low-side threshold and high-side threshold regarding to voltage regulators (SWA, SWB, and SWC). In addition, there are two LDO regulators: VLDO_1.8V and VLDO_1.0V in the RTQ5132.

There are four possibilities where RTQ5132 recognizes the output power good event for any output regulator.

(1) Output voltage goes below the threshold set in Register 0x21[0] for SWA or Register 0x25[0] for SWB or Register 0x27[0] for SWC.

(2) Output voltage goes above the threshold set in Register 0x22[7:6] for SWA or Register 0x26[7:6] for SWB or Register 0x28[7:6] for SWC.

(3) LDO output VLDO_1.8V goes below the threshold set in Register 0x1A[2].

(4) LDO output VLDO_1.0V goes below the threshold set in Register 0x1A[0].

When any of the above event lasts longer than Output_PWR_GOOD_GSI_Assertion time (max. = 10μs), then RTQ5132 sets the Register 0x08[5, 3:2] or Register 0x09[5] or Register 0x33[2] appropriately and drives PWR_GOOD and GSI_n output signal as shown in Table 3 at the same time. The RTQ5132 continues to operate but DDR5 DIMM functionality may not be guaranteed.

The user can query the register space to determine and identify the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once the user determines the cause, the user may clear the appropriate status register individually or by writing '1' to global status clear Register 0x14[0] which de-asserts the GSI_n signal and PWR_GOOD signal. If the output power not good condition is still present then RTQ5132 will continue to assert GSI_n output signal and assert PWR_GOOD signal and the appropriate status Register 0x08[5; 3:2] or Register 0x09[5] or Register 0x33[2] will remain at '1'. If the output power not good condition persists, the user may set the appropriate mask register to remove GSI_n or PWR_GOOD output signal as shown in Table 4 and Table 5.

Output Overvoltage Protection (SWABC)

An output overvoltage protection mechanism is implemented to limit the voltages on the RTQ5132 output regulators. The RTQ5132 actively monitors the output voltage on each enabled regulator.

There are three possibilities where RTQ5132 recognizes the overvoltage event.

(1) SWA output regulator goes above the threshold set in Register 0x22[5:4].

(2) SWB output regulator goes above the threshold set in Register 0x26[5:4].

(3) SWC output regulator goes above the threshold set in Register 0x28[5:4].

In programmable mode (i.e. Register 0x2F[2] = '1'), if any output overvoltage condition persists greater than tOutput_OV_VR_Disable (max. = 20μs) time then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0A[7,5:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active. The user may query the RTQ5132 register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion.

Once user determines the cause, the user must first clear the appropriate output overvoltage status register as well as any other relevant status registers individually or by writing '1' to global status clear Register 0x14[0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5132's output switching regulator by issuing VR Enable command.

The RTQ5132 enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal.

In secure mode (i.e. Register 0x2F[2] = '0'), if any output overvoltage condition persists greater than tOutput_OV_VR_Disable (max. = 20μs) time then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0A[7,5:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

15.13 Output Undervoltage & VIN_BULK Undervoltage Lockout Protection

An output undervoltage lockout protection mechanism is implemented to limit the voltages on the RTQ5132 output regulators. The RTQ5132 actively monitors the output voltage on each enabled regulator.

There are four possibilities where RTQ5132 recognizes the undervoltage lockout event.

(1) SWA output regulator goes below the threshold set in Register 0x22[3:2].

(2) SWB output regulator goes below the threshold set in Register 0x26[3:2].

(3) SWC output regulator goes below the threshold set in Register 0x28[3:2].

(4) VIN_BULK Input Voltage goes below 3.8V.

In programmable mode (i.e. Register 0x2F[2] = '1'), if any output undervoltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable (max. = 20μs) time then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0B[3,1:0], Register 0x33[3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

The user may query the RTQ5132's register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once user determines the cause, the user must first clear the appropriate output undervoltage status register as well as any other relevant status registers individually or by writing '1' to global status clear Register 0x14[0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the user may re-enable the RTQ5132's output switching regulator by issuing VR Enable command assuming valid VIN_Bulk input voltage. The RTQ5132 enables output switching regulators and floats PWR_GOOD signal High when all of its output regulators are normal.

In secure mode (i.e. Register 0x2F[2] = '0'), if any output undervoltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable (max. = 20μs) time then RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets Register 0x0B[3,2:0], Register 0x33[3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The RTQ5132 keeps its VLDO_1.8V and VLDO_1.0V output regulators active.

15.14 Output Current Limiter Warning Event

The RTQ5132 has output current limiter mechanism to limit the current on the output voltage regulators. The inductor current is actively monitored through low-side MOSFET during conduction. The voltage drop across phase node to PGND is compared with current-limit threshold, which is set in Register 0x20, and the valley point of inductor current is limited cycle-by-cycle. When output voltage regulators operate in current limit mode, the PWM on-time one-shot should wait inductor current discharging below current-limit threshold to trigger next on-time output even the output voltage has been below the reference feedback voltage. Hence, the output voltage starts dropping in current limit condition due to insufficient energy to output load. The output undervoltage event will occur after that if output voltage is lower than undervoltage threshold as describes in previous section. The protection mechanism of output current limit is shown in Figure 11.

There are three possibilities where RTQ5132 recognizes the current limiter event.

(1) SWA output regulator current goes above the threshold set in Register 0x20 [7:6].

(2) SWB output regulator current goes above the threshold set in Register 0x20 [3:2].

(3) SWC output regulator current goes above the threshold set in Register 0x20 [1:0].

When any of the event lasts longer than tOutput_Current_Limiter time (max. = 10μs) then RTQ5132 sets the Register 0x0B[7, 5:4] appropriately, drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5132 continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once user determine the cause, the user may clear the appropriate output current limiter status register as well as any other status registers individually or by writing '1' to global status clear Register 0x14[0] which de-asserts the GSI_n signal. If the output current limiter condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the appropriate status Register 0x0B[7, 5:4] will remain at '1'. If the output current limiter condition persists, the user can set the appropriate mask register to remove the GSI_n output signal as shown in Table 4 and Table 5.

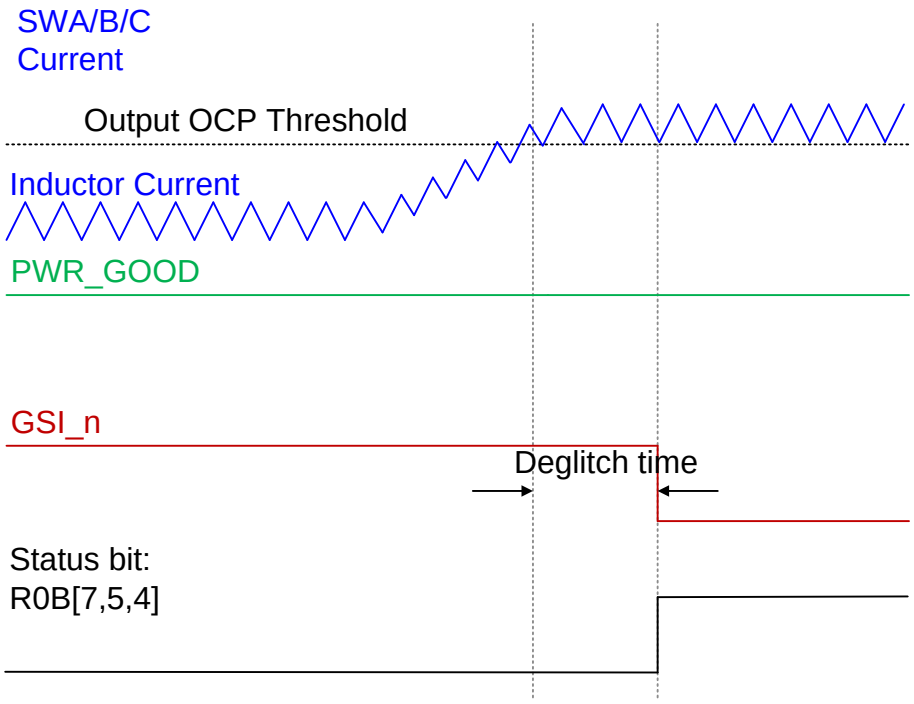


Figure 11. Output Current Limiter Protection

15.15 Output High Current Consumption Warning Event

The RTQ5132 supports high output current consumption warning mechanism for each of its regulator output. Through sensing the voltage drop across low-side MOSFET during conduction, the inductor current can be detected. If enabled, the RTQ5132 actively monitors the average output current of the regulator.

There are three possibilities where RTQ5132 recognizes the high output current consumption.

(1) SWA output regulator average current goes above the threshold set in Register 0x1C[7:2].

(2) SWB output regulator average current goes above the threshold set in Register 0x1E[7:2].

(3) SWC output regulator average current goes above the threshold set in Register 0x1F[7:2].

When either event occurs, then RTQ5132 sets the Register 0x09[3, 1:0] appropriately, and drives GSI_n output signal as shown in Table 3 at the same time. The RTQ5132 continues to operate as normal.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once the user determines the cause, the user can clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing '1' to global status clear Register 0x14[0] which de-asserts the GSI_n signal. If the output current consumption warning condition is still present then RTQ5132 will continue to assert GSI_n output signal and the appropriate status Register 0x09[3, 1:0] will remain at '1'. If the output current consumption warning condition persists, the user can set the appropriate mask register to remove GSI_n output signal as shown in Table 4 and Table 5.

15.16 PMIC High Temperature Warning and Critical Temperature Protection

The RTQ5132 provides a high temperature warning mechanism as well as critical temperature shutdown. An internal temperature sensor is placed near the heating MOSFET to detect the die temperature and protects RTQ5132 from over-heat operation. There are two registers associated with RTQ5132's die temperature: The high temperature warning threshold Register 0x1B[2:0] and shutdown temperature threshold Register 0x2E[2:0]. The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

If the die temperature goes above the threshold set in Register 0x1B[2:0] for a period longer than tHigh_Temp_Warning time (max. = 10μs), the RTQ5132 sets the Register 0x09[7] and drives GSI_n output signal as shown in Table 3 at the same time.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once the user determines the cause, the user can clear the temperature warning status register as well as any other status registers individually or by writing '1' to global status clear Register 0x14[0] which de-asserts the GSI_n signal. If the high temperature warning condition is still present, then RTQ5132 will continue to assert GSI_n output signal and the appropriate status Register 0x09[7] will remain at '1'. If the high temperature warning condition persists, the user can set the appropriate mask register to remove GSI_n output signal as shown in Table 4 and Table 5.

If the die temperature goes above the threshold set in Register 0x2E[2:0] for a period longer than tShut_Down_Temp time (max.=10μs), the RTQ5132 internally generates VR Disable command and disables all of its switching output regulators, sets the code in Register 0x05[2:0], updates Register 0x08[6], and drives GSI_n and PWR_GOOD output signal as shown in Table 3 at the same time. The VLDO_1.8V and VLDO_1.0V output regulator keep active.

The user is expected to monitor the temperature status registers. When the temperature drops below the threshold, the user must re-start the RTQ5132 by going through the power cycle of the VIN_BULK input supply.

15.17 Packet Error Code (PEC) and Parity Error Event

There are two types of error checking done by the RTQ5132. Parity error checking and packet error checking. By default, the parity error checking is always enabled and packet error checking is disabled. The user may enable the packet error checking at any time. The parity error is checked for each byte in a packet except for the device select code byte from the user. The user sends parity error information in "T" bit.

I3C Basic defines S0, S1, S2, S3, S4, S5, S6 error detection for slave devices. Only S1 and S2 error detection is supported by the RTQ5132 for parity checking. All other errors are not supported and not applicable.

In I3C Basic mode, on RTQ5132's primary management interface, PEC function and parity function can be enabled. If enabled, when RTQ5132 detects either PEC error or parity error, the RTQ5132 sets the Register 0x0A[3:2] appropriately, drives GSI_n output signal as shown in Table 3, continues to operate as normal, and allows access to all registers.

The user can query the register space to determine the cause of the GSI_n signal assertion. Once the user determines the cause, the user can clear the status register individually or by writing '1' to global status clear Register 0x14[0] which de-asserts the GSI_n signal. No further action is needed by the user at this point.

15.18 RTQ5132 Output Regulator Control Topology

The RTQ5132 applies A^{2}RCOT (Accurate Adaptive Ramp COT) to regulate the output voltage of VDD, VDDQ and VPP. The SWA and SWB can operate in either single phase mode or dual-phase mode. When operating as dual-phase mode, the interleaving PWM control is applied to balance the output current.

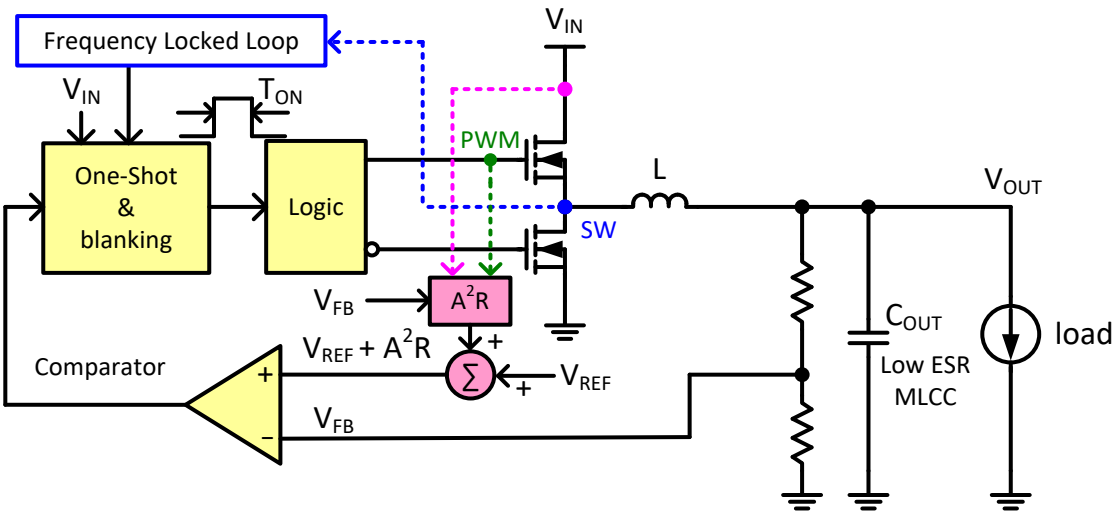


Figure 12. A^{2}RCOT Control Mechanism

Figure 12 illustrates a standard A^{2}RCOT control Buck converter. In order to achieve good stability with low-ESR ceramic capacitors, A^{2}RCOT generates an internal ramp by sensing V_{IN}, V_{FB} and PWM signal. The internal ramp is in phase with PWM signal and its magnitude is proportional to V_{IN}. Moreover, the average of V_{FB} can be well regulated at V_{REF} which makes good output load and line regulation. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

However, making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for the following reasons. The voltage drops across MOSFET and inductor make equivalent conversion ratio to be smaller than ideal duty ratio. That is, the switching frequency is not fixed at different output load conditions. Frequency is increasing at higher loading and junction temperature as compared to smaller loading and junction temperature.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. The A^{2}RCOT uses the frequency locked loop, measuring the actual switching frequency and modifying the on-time with a feedback loop to make the average switching frequency in the desired range.

The RTQ5132 control algorithm is simple to understand as depicted in Figure 13. The feedback voltage is compared to the reference voltage, V_{REF}, with the accurate adaptive ramp (A^{2}R) added. When the feedback signal is less than the combined reference, the on-time one-shot is triggered as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

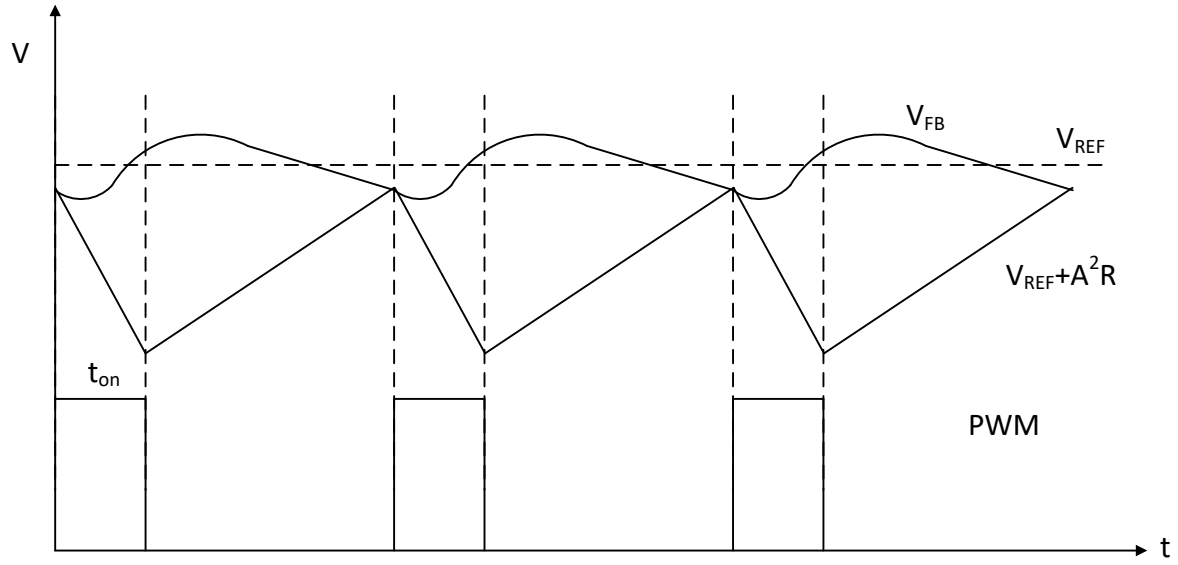


Figure 13. A^{2}RCOT PWM Control Diagram

Regulator Operating Mode Selection

The RTQ5132 offers two kinds of PWM operation in the light load. One is diode emulation mode (DEM), and the other is forced continuous conduction mode (FCCM). The user can switch between DEM and FCCM by the Register 0x29[7:6], Register 0x2A[7:6] and Register 0x2A[3:2] in programmable mode or in the configuration state of FSM before issuing the VR_EN command. The details of the two operation modes are described below.

(1) DEM (Diode Emulation Mode)

In diode emulation mode, the RTQ5132 automatically reduces switching frequency at light load conditions to maintain high efficiency. The reduction of frequency is achieved smoothly. As the output current decreases from heavy load conditions, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor free-wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next “ON” cycle. Contrarily, when the output current increases from light load to heavy load, the switching frequency increases to the pre-set value as the inductor current reaches the continuous conduction. The transition load point between DEM and CCM operation is shown in Figure 14 and can be calculated as follows:

$$I_{LOAD\_BCM} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

, where t_{ON} is the on-time of high-side MOSFET.

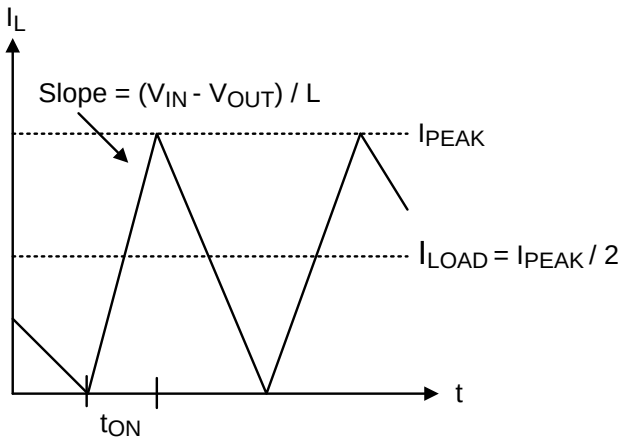


Figure 14. Boundary Condition of DEM/CCM

The switching frequency in DEM can be calculated as follows:

$$f_{SW}(I_{LOAD}) = \frac{2LI_{LOAD}}{V_{IN}t_{ON}^2\left(\frac{V_{IN}}{V_{OUT}}-1\right)}$$

, where I_{LOAD} is smaller than I_{LOAD_BCM}.

As shown in the equation, switching frequency is a function of output load current, I_{LOAD}, and it is proportional to I_{LOAD}, which means it becomes higher at heavy load and reduces to almost zero at a very light load. Besides, inductor selection can also change the switching frequency in DEM. Choosing large inductance makes more switching loss as compared to small inductance. However, the core loss of inductor increases with larger inductor current ripple for a given inductor. That is, proper selection of inductor based on efficiency target is important.

Moreover, in order to achieve smooth transition from DEM to CCM or backward, during discontinuous switching, the on-time is immediately increased to add “hysteresis” to discourage the IC from switching back to continuous switching unless the load increases substantially. The RTQ5132 returns to continuous conduction as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for presetting switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

(2) FCCM (Forced Continuous Conduction Mode)

Unlike diode emulation mode (DEM) that enables zero current detection (ZDC) to reject negative inductor current during low-side MOSFET turns on. The inductor current can be negative until next on-time is generated in FCCM. The switching frequency is fixed from no load to full load. Therefore, benefits like better transient response from light load to heavy load and smaller EMI/EMC come along with FCCM. Nevertheless, poor efficiency in light load is a tradeoff.

Analog-to-Digital Converter (ADC)

The RTQ5132 supports analog to digital converter (ADC) to monitor input supply voltages VIN as well as output voltage regulator voltage (SWA, SWB, SWC, VLDO_1.8V and VLDO_1.0V). The Register 0x30[7:3] allows to enable the ADC and select the desire input supply voltage or output supply voltage. The Register 0x31[7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is as follows:

Table 6. RTQ5132 ADC Accuracy Table

Input Rail	ADC Range	ADC Accuracy
SWA, SWB Output Voltage	1050mV to 1160mV	± 1 LSB
	Outside of 1050mV to 1160mV	± 3 LSB
SWC Output Voltage	1750mV to 1850mV	± 1 LSB
	Outside of 1750 mV to 1850mV	± 3 LSB
VLDO_1.8V, VLDO_1.0V Output Voltage	--	± 3 LSB
VIN_BULK Input Voltage	--	± 6 LSB

The RTQ5132 also monitors output voltage regulator current or power (SWA, SWB and SWC) and updates Register 0x0C[7:0] for SWA, Register 0x0E[5:0] for SWB and Register 0x0F[5:0] for SWC. The Register 0x1B[6] allows user to select whether RTQ5132 should report current measurements or power measurements. The current or power measurement reported in these registers are an average measurement over time period defined in Register 0x30[1:0]. If Register 0x1B[6] = '1', the Register 0x1A [1] allows user to select whether RTQ5132 should report individual rail power or total power in Register 0x0C[7:0]. The register update frequency of this register is configured in Register 0x30[1:0]. The accuracy of the current (>0.5A) or corresponding power measurement is ± 3 LSB or ± 6 LSB respectively. The accuracy of the current measurement (<0.5A) is ± 4 LSB or corresponding power measurement is ± 7 LSB respectively.

If Register 0x1A[1] = '1', the accuracy of total power reported in Register 0x0C = ± 12 LSB

Besides, the RTQ5132 die temperature is also monitored and converted to ADC value, the temperature is reported in Register 0x33[7:5]. The ADC for temperature automatically works as die temperature is higher than 85°C.

Table 7. General Purpose of ADC Units

Default Monitoring (5-channel) ± User Selection (1-channel)			
Channel Sensor	**Type**	**Monitor Register**	**Current/Power Measurement Selector**
SWA Output Current or Power	Default monitor	0x0C[7:0]	0x1B[6]=0 Set for current 0x1B[6]=1 Set for power 0x1A[1]=0 Report power for single switcher output 0x1A[1]=1 Report the sum of power for all switcher outputs (SWA, SWB, SWC)
SWB Output Current or Power		0x0E[5:0]	
SWC Output Current or Power		0x0F[5:0]	
PMIC die Temperature		0x33[7:5]	
SWA Output voltage	User selection 0x30[6:3]	0x31[7:0]	
SWB Output voltage			
SWC Output voltage			
VIN_BULK Input voltage			
VLDO_1.8V Output voltage			
VLDO_1.0V Output voltage			

15.19 PMIC Address ID (PID)

The RTQ5132 has PID input pin which allows assigning up to three different unique ID for I^2C and I3C Basic protocol.

At first power on, when VIN_BULK input is applied, the RTQ5132 automatically senses its ID as shown in Table 8.

Table 8. PMIC ID

PID Pin Connection on DIMM Board	PMIC ID	Comment
Short to GND	PID = 1001	PMIC can be configured
Floating	PID = 1000	
Short to 1.8V	PID = 1100	Connected to RTQ5132's VLDO_1.8V

Error Injection

The RTQ5132 offers error injection capability for the purpose of debug, test and validation at various stages as well as to isolate and map out faulty PMIC in memory subsystem for normal application environment. There are two conditions for error injection test.

(1) Error Injection Function Usage prior to VR Enable:

Prior to VR Enable command, the Error injection function can be invoked by setting error injection enable bit Register 0x35[7] = '1' during the configuration state. If any of either VIN_BULK UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected prior to VR Enable command, the RTQ5132 will not execute power-on sequence and will not enable output regulators when receiving VR Enable command. The RTQ5132 will not update error log registers (Register 0x04 to Register 0x06). The RTQ5132 enters in secure mode if Register 0x2F[2] = '0' and programmable mode if Register 0x2F[2] = '1'.

(2) Error Injection Function Usage after VR Enable:

After RTQ5132 output regulators are enabled with VR Enable command and RTQ5132 is in programmable mode, the error injection function can be invoked by setting error injection enable bit Register 0x35[7] = '1'. If any of either VIN_BULK UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected, the RTQ5132 executes power-off sequence to disable output regulators and updates the error log registers (Register 0x04 to Register 0x06) as well as status registers accordingly.

To exit error injection mode of operation, the RTQ5132 requires power cycle of VIN_BULK input supply.

16 Application Information

(Note 6)

16.1 Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response; however, they increase the inductor ripple current and output voltage ripple, and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required. Also, transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad \text{and} \quad I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current-limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses, some types of shielded ferrite core are usually better. Although they are possibly larger or more expensive, they will probably give fewer EMI and other noise problems.

Since DDR5 on DIMM has layout space limitation to power management IC on DIMM as well as the surrounding components like inductors and input/output capacitors, a standard inductor mechanical specification is defined in Table 9 and Table 10. Moreover, the electrical specification of inductor is also defined in Table 11 and Table 12. The electrical specifications include inductance, maximum DCR, maximum ACR and the minimum inductance requirement after de-rating at a specified operating current. The DIMM vendors can select an inductor based on the Table 11 and Table 12. Because the inductor size is fixed, the tradeoff between efficiency and transient response is the main concern on selection. Generally, the inductance for SWA, and SWB, which are 1.1V output rails, is recommended to choose between 0.47μH and 0.68μH. The transient performance with L = 0.47μH is better than that with L = 0.68μH. However, the efficiency performance with L = 0.68μH is better than that with L = 0.47μH. On the other hand, the output rail with V_{OUT} = 1.8V, which is SWC or VPP rail, is suggested to apply inductance between 1μH to 1.5μH.

Table 9. SWA an SWB Inductor Mechanical Specifications

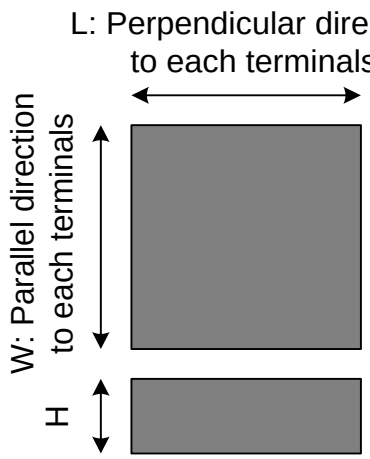
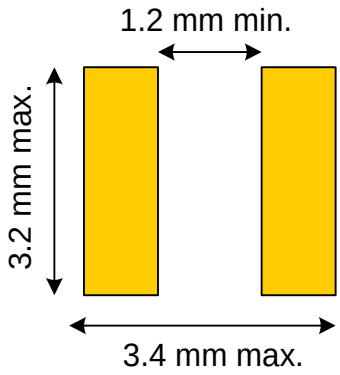
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	3.4max		
W [mm]	3.2max		
H [mm]	1.2max		

Table 10. SWC Inductor Mechanical Specifications

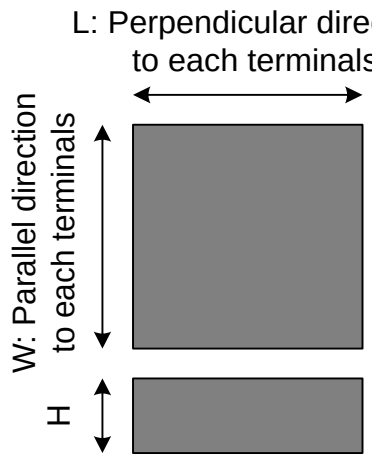
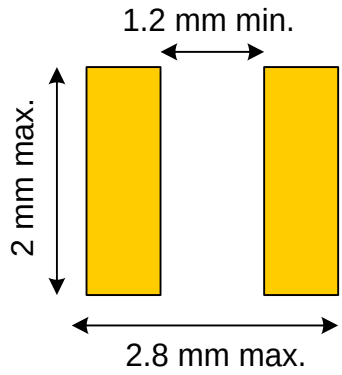
Package Size		Reference Drawings	Recommended Land Pattern
L [mm]	2.7max		
W [mm]	2.2max		
H [mm]	1.2max		

Table 11. SWA and SWB Inductor Electrical Specifications

Package Height	L @ 0.5-1MHz/0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 6A [µH]
1.2 Max [mm]	0.47	14.5	93	0.30
	0.68	18.5	113	0.38

Table 12. SWC Inductor Electrical Specifications

Package Height	L @ 0.5-1MHz/0bias ± 20% [µH]	Max DCR [mΩ]	Max ACR @ 1MHz [mΩ]	Min. L @ 2A [µH]
1.2 Max [mm]	1.0	48	182	0.56
	1.5	75	300	0.82

16.2 Output Cap. Selection

The Buck output regulators of RTQ5132 are optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR, ESL and stored charge. These three ripple components are called ESR ripple, ESL ripple, and capacitive ripple. Since ceramic capacitors have extremely low ESR, ESL and relatively little capacitance, all these components should be considered if ripple is critical. The decomposition of output ripple is shown in Figure 15. The formulas to describe each component are listed below.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(ESL)} = \frac{d}{dt} I_L \times ESL$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

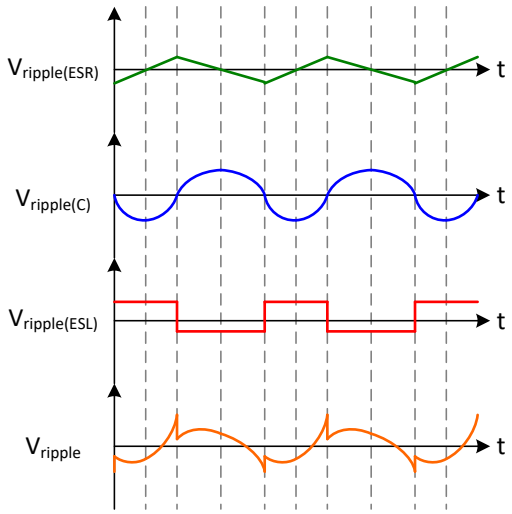


Figure 15. Output Ripple Decomposition

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The A^2RCOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the A^2RCOT control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. The behavior diagram of

output voltage drop is depicted as Figure 16. Calculate the approximate on-time (neglecting parasitic) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ ,and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but it can be neglected both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

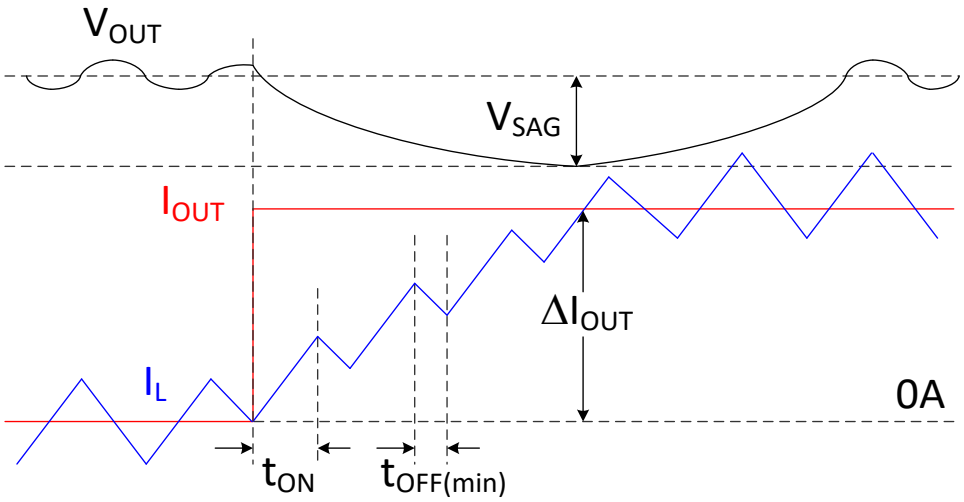


Figure 16. Output Voltage Drop (V_{SAG}) Estimation as Output Load Current Step Up

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

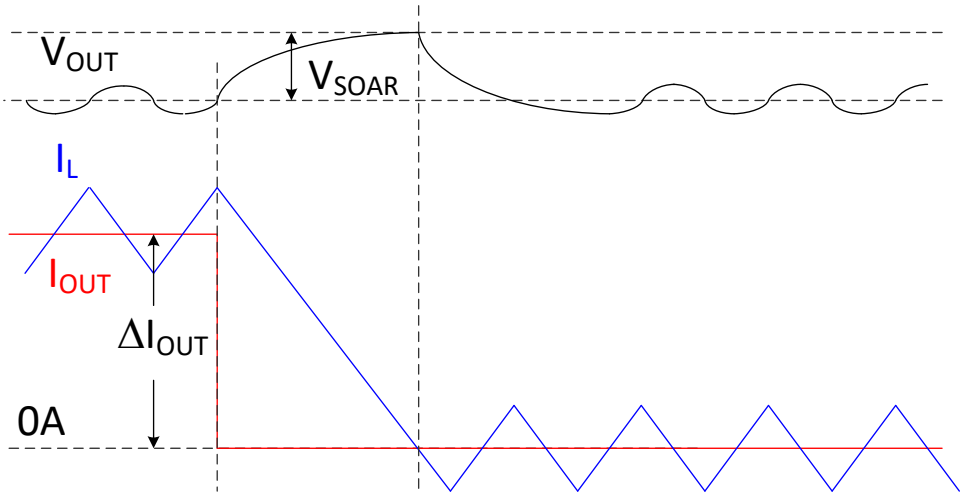


Figure 17. Output Voltage Soar (V_{SOAR}) Estimation as Output Load Current Step Down

Most applications never experience instantaneous full load steps and the RTQ5132's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that overvoltage protection and undervoltage protection will not be triggered.

In addition, the recommended dielectric type of the capacitor is X7R which has the best performance among temperature and DC and AC bias voltage variations. The variation of the capacitance value with temperature, DC bias voltage and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

A standard output capacitors' electrical specification is defined in Table 13. The electrical specifications include capacitance, rated voltage and the size code in inch. The DIMM vendors should select the capacitors based on the Table 13.

Table 13. Output Capacitor Electrical Specifications

Component	Value	Physical Size
C_{OUTA}	47µF (x2)	6.3V; 0603
C_{OUTB}	47µF (x2)	6.3V; 0603
C_{OUTC}	47µF (x2)	6.3V; 0603
C_{DISTA}*	350µF	6.3V; 0402
C_{DISTB}*	350µF	6.3V; 0402
C_{DISTC}*	150µF	6.3V; 0402
$C_{LDO\_1.8V}$	4.7µF	6.3V; 0402
$C_{LDO\_1.0V}$	4.7µF	6.3V; 0402

*Note that capacitors C_{DISTA}, C_{DISTB}, and C_{DISTC} represent the lump sum of distributed capacitance across the entire DIMM.

16.3 Input Cap. Selection

A buck converter generates a pulsating ripple current with high di/dt at the input. Without input capacitors, ripple current is supplied by the upper power source. Printed circuit board (PCB) resistance and inductance cause high-voltage ripple that disrupts electronic devices. The circulating ripple current results in increased conducted and radiated EMI. Input capacitors provide a short bypass path for ripple current and stabilize bus voltage during a transient event.

The capacitor voltage rating should meet reliability and safety requirements. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. Among the different types of capacitors, the multilayer ceramic capacitor (MLCC) is particularly good regarding allowable ripple current due to low ESR and ESL. Following equation is used to estimate the required effective capacitance that will meet the ripple requirement.

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{\Delta V_{IN\_PP} \times f_{SW}}$$

where D is calculated as below:

$$D = \frac{V_O}{V_{IN} \times \eta}$$

Besides the ripple-voltage requirement, the ceramic capacitors should meet the thermal stress requirement as well. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[(1-\frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Besides, since the ESL of ceramic capacitors plays a significant role on voltage spike at input and phase node, it is desirable to add a small capacitor with low ESL near VIN pin.

While the MLCC is excellent regarding allowable ripple current, it is well-known regarding effective capacitance that is necessary to meet transient response requirements. There can be two VIN spikes during the transient: the first spike is related to the ESR; and the second spike is caused by the difference between the buck-converter input current (i_{IN_B}) and the bus-converter output current (i_{PS}) as depicted in Figure 18. Both spikes should be lower than the VIN undershoot or overshoot requirement (VIN_tran). First, since the MLCCs have very small ESR, the component of ESR drop can almost be ignored. The second spike is related to the response of the bus converter. The converter output-current rise time during a transient event, T_{R_PS}, can be approximated by the following equation:

$$T_{R\_PS} \cong \frac{0.35}{f_{BW\_PS}}$$

, where f_{BW_PS} is the control loop bandwidth of Buck converter.

The equivalent capacitance of the input capacitors should be greater than that calculated with following equation:

$$C_{IN} \geq \frac{\frac{1}{2} \times I_{Step} \times D_{max} \times T_{R\_PS}}{V_{IN\_Tran}}$$

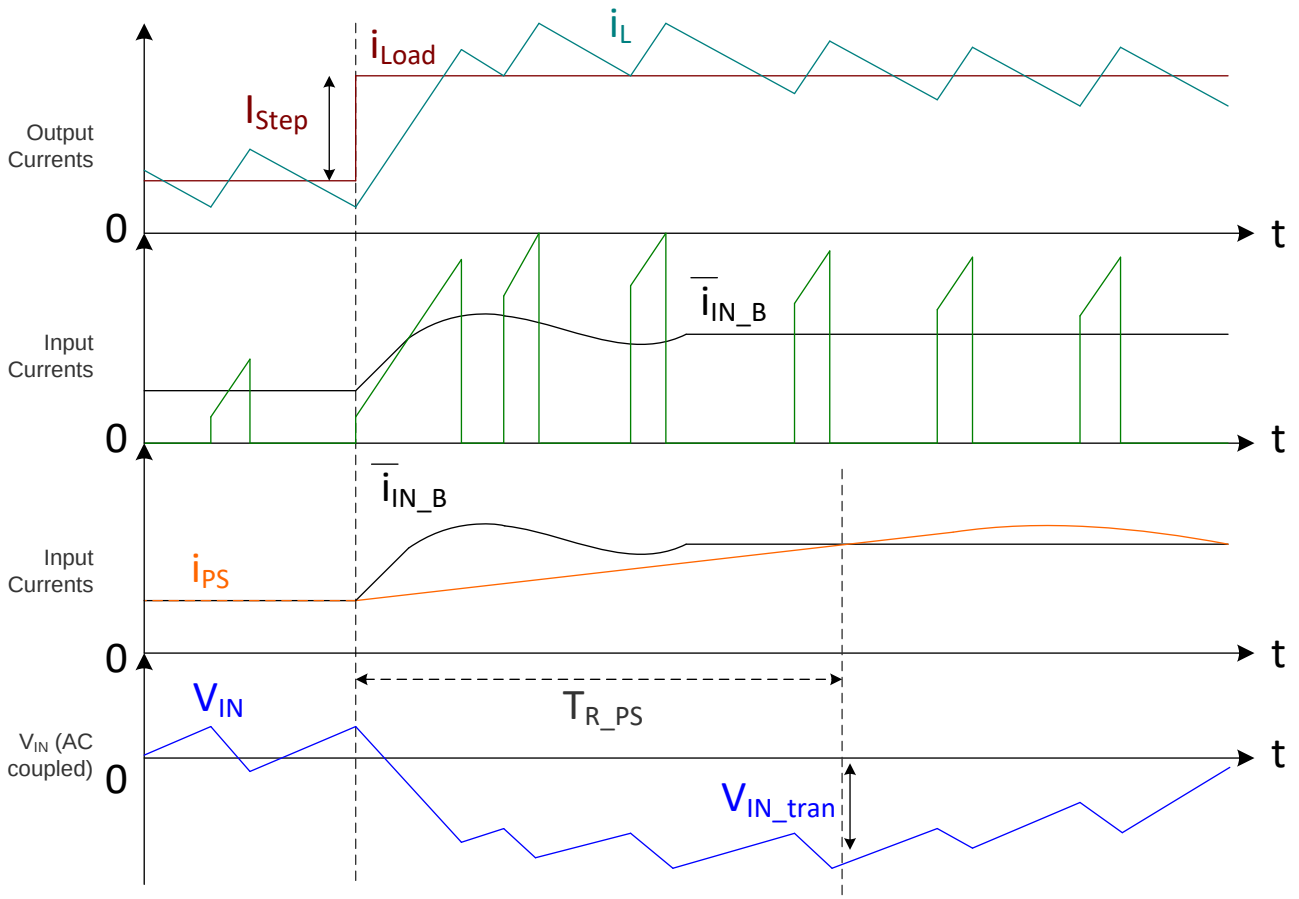


Figure 18. VIN Transient Current Diagram

Either VIN ripple (ΔV_{IN_PP}) or Vin transient ripple (V_{IN_Tran}) should meet the design requirements. For RTQ5132, the input voltage should be always higher than VIN_UVLO threshold to confirm the PMIC's functionality. Moreover, it should be noticed that many de-rating factors, including VIN dc voltage, ac voltage and operating temperature, make equivalent capacitance smaller than the capacitance without bias.

The standard electrical specifications for input capacitors are outlined in Table 14. These specifications include capacitance, rated voltage, and the size code in inches. DIMM vendors can choose the input capacitors based on Table 14.

Table 14. Input Capacitor Electrical Specifications

Component	Value	Physical Size
C_{IN}	4.7µF	10V; 0402
C_{INA}	22µF (x2)	10V; 0603
C_{INB}	22µF (x2)	10V; 0603
C_{INC}	22µF (x2)	10V; 0603
C_{BYP}	0.1µF	10V; 0201
C_{BYPA}	0.1µF	10V; 0201
C_{BYPB}	0.1µF	10V; 0201
C_{BYPC}	0.1µF	10V; 0201

16.4 Bootstrap Circuit

The bootstrap circuit is useful in a high-voltage gate driver and operates as follows. When the SW node goes below the IC supply voltage V_{CC} (V_{DD}) or is pulled down to ground (the low-side MOSFET is turned on and the high-side MOSFET is turned off), the bootstrap capacitor, C_{BOOT}, charges through the bootstrap resistor, R_{BOOT}, and bootstrap diode, D_{BOOT}, from the VCC power supply, as shown in Figure 19. On the other hand, the voltage across V_{BOOT} and SW can supply gate charge to high-side MOSFET when low-side MOSFET is turned off and SW node goes to a higher voltage, VOUT. In the meantime, the bootstrap diode reverses bias and blocks the rail voltage from the IC supply voltage, V_{CC}.

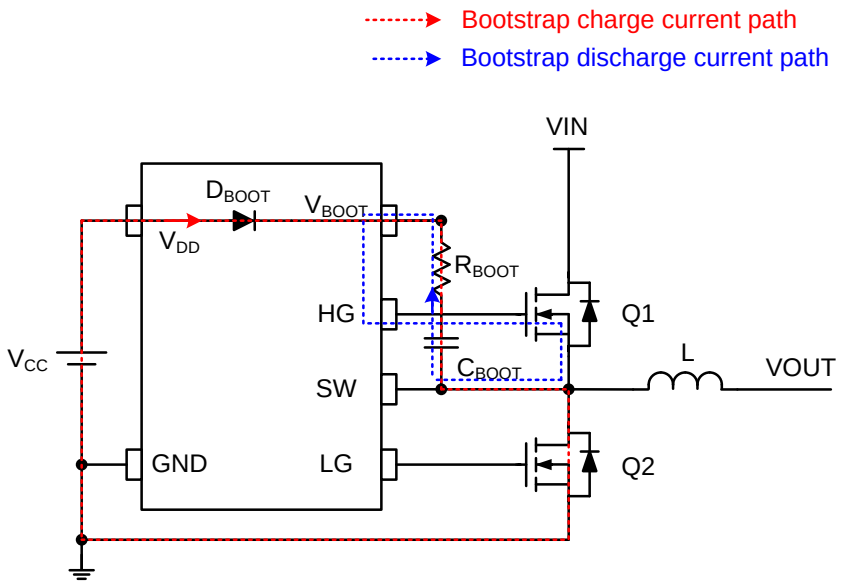


Figure 19. Bootstrap Power Supply Circuit

There are some design considerations for a bootstrap circuit. First, the selection of bootstrap capacitor (C_{BOOT}) is based on the maximum voltage drop across C_{BOOT} to guarantee the high-side MOSFET has enough charge to turn on periodically. The maximum allowable voltage drop (ΔV_{BOOT}) depends on the minimum gate drive voltage (for the high-side MOSFET) to maintain. If V_{GSMIN} is the minimum gate-source voltage, the capacitor drop must be:

$$\Delta V_{BOOT} = V_{CC} - V_F - V_{GSMIN}$$

where V_{CC} is the supply voltage of gate driver, and VF is the forward voltage drop of bootstrap diode.

Therefore, the value of bootstrap capacitor is calculated as:

$$C_{BOOT} = \frac{Q_{Total}}{\Delta V_{BOOT}}$$

where Q_{Total} is the total amount of the charge required for driving the high-side MOSFET and some leakage charge in the chip.

Second, when the external bootstrap resistor is used, the resistance, R_{BOOT}, introduces an additional voltage drop:

$$V_{RBOOT} = \frac{Q_{Total}}{t_{Charge}} \times R_{BOOT}$$

where t_{Charge} is the bootstrap charging time (the low-side MOSFET turn-on time).

The power dissipation on R_{BOOT} should be considered when choosing the package size of resistor. When estimating the maximum allowable voltage drop, the value of voltage drop of bootstrap resistor should be taken into account.

For example, assume V_{CC} = 5V, V_F = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and Q_{Total} = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔV_{BOOT} is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including VIN dc voltage, ac voltage and operating temperature, makeor example, assume V_{CC} = 5V, V_F = 0.7V, R_{BOOT} = 1Ω, V_{GSMIN} = 2.5V and Q_{Total} = 5nC. The ΔV_{BOOT} can be calculated as 1.8V. The estimated C_{BOOT} is 2.8nF. Generally, the ΔV_{BOOT} is not suggested to be too large and also need to consider the additional voltage drop on R_{BOOT}. Moreover, the de-rating factors, including VIN dc voltage, ac voltage and operating temperature, make equivalent capacitance be smaller. The common selection value of C_{BOOT} is 100nF~220nF, that makes the ΔV_{BOOT} to be 50mV and 25mV separately. If choosing the bias capacitor with 0201 package and 6.3V voltage rating, the de-rating factor is about 0.5. Therefore, the ΔV_{BOOT} increases to 100mV and 50mV. In addition, the voltage drop on R_{BOOT} = 1Ω is 25mV as t_{Charge} is 200nsec. Adding the R_{BOOT} can reduce the EMI noise as well as voltage spike on phase node. However, the additional power loss will reduce the system efficiency.

16.5 VLDO_1.8V and VLDO_1.0V Decoupling Capacitor

The RTQ5132 integrates two LDO regulators: VLDO_1.8V and VLDO_1.0V. Both the VLDO_1.8V and VLDO_1.0V LDOs are powered by VIN and supply power to system devices such as SPD/HUB and CK on the DIMM. Each of them requires a decoupling capacitor to be placed near the output pin, with a minimum equivalent capacitance of at least 2.2μF. In many applications, a 4.7μF/6.3V/X5R/0402 capacitor is recommended. When selecting the capacitor's package size and voltage rating, it is important to consider the de-rating coefficient based on voltage and temperature to account for the equivalent capacitance under actual operating conditions.

16.6 Thermal Consideration

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-28L 3x4 (FC) package, the thermal resistance, θ_{JA}, is 41°C/W on high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$$P_{D(MAX)} = (125°C - 25°C)/(41°C/W) = 2.43W$$ for a WQFN-28L 3x4 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 20 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

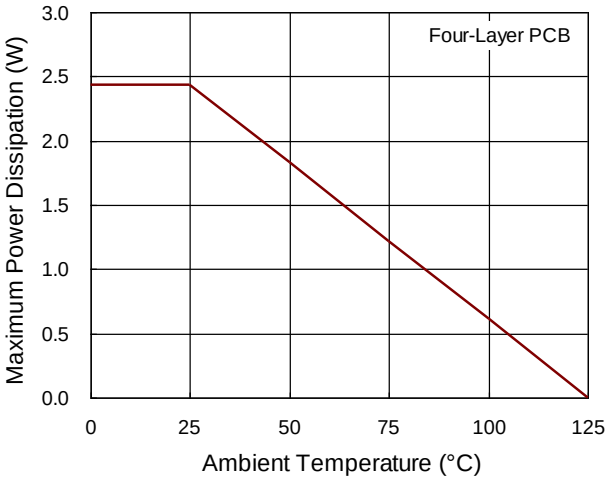


Figure 20. Derating Curve of Maximum Power Dissipation

16.7 Layout Consideration

Layout is crucial in high-frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to converter instability. The following points must be considered before starting a layout for the RTQ5132. Figure 21 and Figure 22 show the recommended layout guide for reference. In Figure 21, the top layer layout of the RTQ5132's EVB is demonstrated. Note that the components' sizes are considered and depicted in their actual relative sizes. In Figure 22, the bottom layer layout of the RTQ5132's EVB is demonstrated. Due to PMIC layout area limitations on the DIMM, the input caps and output caps are placed on this layer. Furthermore, the input caps have been divided into two parts: a small decoupling capacitor with a smaller package size and capacitance is mounted under one side of the VIN pin for each rail, and two bulk capacitors are placed directly beneath the VIN pin on the other side for each rail. The placement of the small decoupling capacitor helps filter out high-frequency voltage spikes, reducing phase ringing on the phase pin. The bulk capacitors provide prompt energy during output load transients. It is essential to keep noisy signals, such as the switching node and output caps' vias, away from sensitive areas. Below are the key considerations for the RTQ5132's EVB layout.

- Make the traces for high current paths as short and wide as possible to minimize resistance and inductance.
- Place the input capacitors as close to the device pins (VINA, VINB, and VINC) as possible to improve filtering and reduce noise.
- The SW node experiences high-frequency voltage swings, so keep it confined to a small area. Also, keep sensitive components away from the SW node to prevent noise coupling.
- Connect the PGND pin to a robust ground plane for effective heat sinking and noise suppression. For enhanced thermal dissipation, it is advisable to add thermal vias near the PGND pin to link different layers.
- It is recommended to connect the ground of VIN to AGND and then to the PGND layer through a single via to maintain signal integrity.
- Position decoupling capacitors as close to the device pins (VIN and AGND) as possible for optimal noise suppression.
- Differential route the feedback traces for each rail and ensure they are distanced from noisy signals on the EVB to avoid interference.
- The NC (No Connection) pins at the four corners are recommended to be connected to PGND for better heat dissipation.
- For the dual-phase applications, it is necessary to place the output capacitors (C_{OUTA} and C_{OUTB}) as close as possible to each other, and position the sense feedback node of SWA_FB_P at the center between VDD and VDDQ.

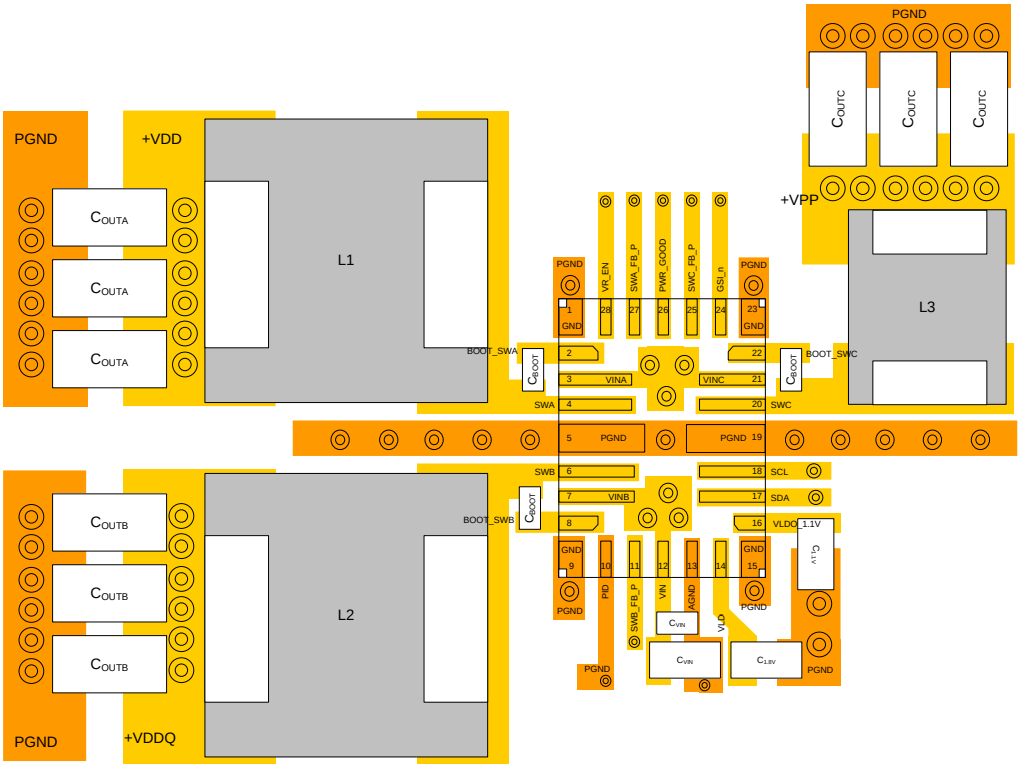


Figure 21. RTQ5132 Layout Guide (Top Layer)

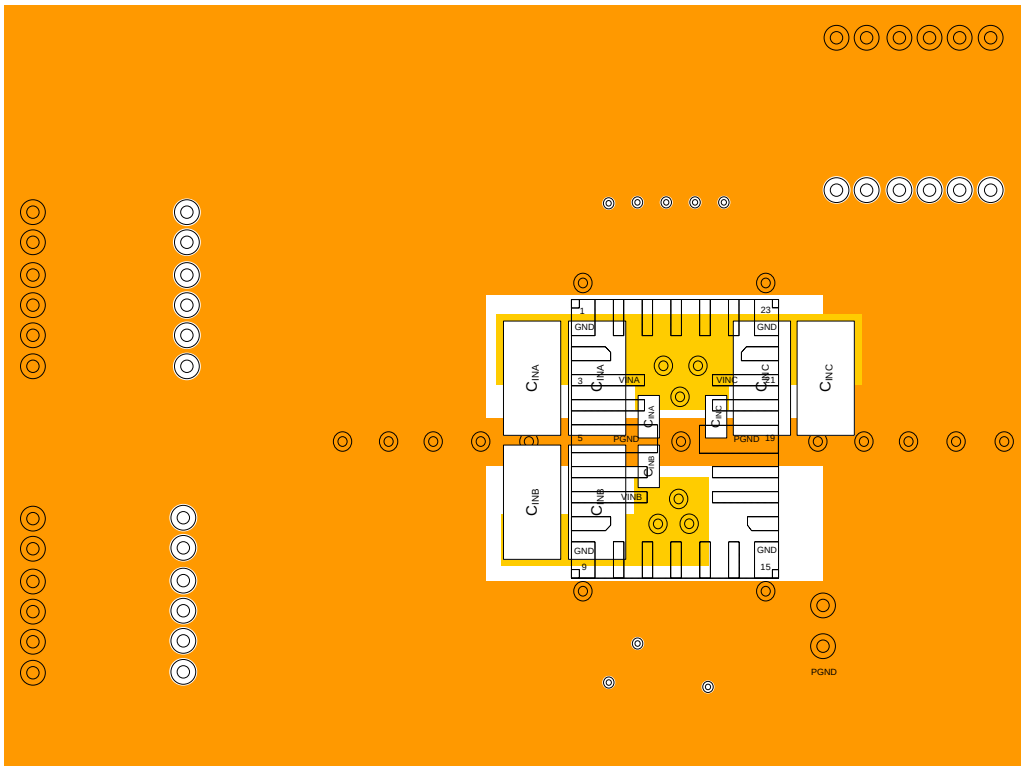


Figure 22. RTQ5132 Layout Guide (Bottom Layer)

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Functional Register Description

Register Attribute Definition

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Write has no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	WO	This bit can only be written by host. Read from this bit return ‘0’.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return ‘0’ when read. Write has no effect.
Write ‘1’ Only	1O	This bit can only be set (i.e. write ‘1’) but not reset (i.e. write ‘0’). Write ‘0’ has no effect.
Persistent	E	This bit is persistent during power cycle
Protected	P	This bit is protected by the password registers. This bit cannot be read to or written unless the password code has been written into the password registers.

Register Map Breakdown

Region	Register Range	Restriction
Host User (NVM and VM)	[0x15 - 0x2F, 0x32]	Register Modification is NOT allowed in Secure Mode
DIMM Vendor (NVM)	[0x40 - R6F]	
PMIC Vendor (NVM)	[R70 - RFF]	
Host Region	[0x20 – 0x2D]	Registers are copied from DIMM Vendor Region Setting at power-on

17.1 Register Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor registers is (Register_0x37 = 0x73) and (Register_0x38 = 0x94). The PMIC offers DIMM vendors to select their own password for DIMM vendor registers.

17.2 Steps to Access DIMM Vendor Region Registers

The steps to access the DIMM vendor registers are as following:

1. Write to “Register 0x37” = 8 bit password LSB code.
2. Write to “Register 0x38” = 8 bit password MSB code.
3. Write to “Register 0x39” = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to “Register 0x39” = 0x00 (Lock).

17.3 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default

password are as following:

1. Write to “Register 0x37” = 0x73. (default)
2. Write to “Register 0x38” = 0x94. (default)
3. Write to “Register 0x39” = 0x40.
4. Write to “Register 0x37” = New 8 bit password LSB code as desired by DIMM vendor.
5. Write to “Register 0x38” = New 8 bit password MSB code as desired by DIMM vendor.
6. Write to “Register 0x39” = 0x80.
7. Wait 200ms.
8. Write to “Register 0x39” = 0x00 (Lock).
9. Power cycle the PMIC. Remove VIN_BULK supply from the PMIC. The new password is in effect after the power cycle.

To change the password again from this point on, repeat steps 1 to 8 but note that in steps 1 and 2 current password is required.

17.4 Steps to Burn or Program DIMM Vendor Region Registers

The steps to burn or to program the DIMM vendor registers are as following:

1. Write to “Register 0x37” = 8 bit password LSB code.
2. Write to “Register 0x38” = 8 bit password MSB code.
3. Write to “Register 0x39” = 0x40.
4. Programming DIMM vendor registers are done at block level.
   Block 40 addresses: 0x40 - 0x4F;
   Block 50 addresses: 0x50 - 0x5F;
   Block 60 addresses: 0x60 - 0x6F.
   Perform write operation to each block as desired.
5. Burn each block one at a time:
   Block 40 addresses: Write “Register 0x39” = 0x81.
   Block 50 addresses: Write “Register 0x39” = 0x82.
   Block 60 addresses: Write Register 0x39” = 0x85.
6. Wait time 200ms.
7. To check if programming is complete:
   Perform read from “Register 0x39”. The code 0x5A indicates it is complete. It takes 200ms per page to program.
8. To verify if programming is done correctly:
   Perform read operation from appropriate block addresses.
9. Write to “Register 0x39” = 0x00. (Lock)

Table 15. RTQ5132 Registers Map

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x00	Reserved	RV								0x00	RV
0x01	Reserved	RV								0x00	RV
0x02	Reserved	RV								0x00	RV
0x03	Reserved	RV								0x00	RV
0x04	Global ERR Log	COUNT	BUCK_OV_OR_UV	VIN_BULK_OV	OTP	RV				0x00	ROE
0x05	PMIC Fault ERR Log	RV	A_NO_PG	RV	B_NO_PG	C_NO_PG	PMIC_ERROR_LOG			0x00	ROE
0x06	UVLO/OV ERR Log	A_UVLO	RV	B_UVLO	C_UVLO	A_OV	RV	B_OV	C_OV	0x00	ROE
0x07	Reserved	RV								0x00	ROE
0x08	PMIC Status_0	RV	OTP	A_PG	RV	B_PG	C_PG	RV	VIN_BUCK_OV	0x00	RO
0x09	PMIC Status_1	HTW	RV	LDO_1.8V_PG	RV	A_HCW	RV	B_HCW	C_HCW	0x00	RO
0x0A	PMIC Status_2	A_OV	RV	B_OV	C_OV	PEC_ERR	PARITY_ERR	IBI	RV	0x00	RO
0x0B	PMIC Status_3	A_OC	RV	B_OC	C_OC	A_UVLO	RV	B_UVLO	C_UVLO	0x00	RO
0x0C	SWA Current & Power Measurement	SWA_OUTPUT_CURRENT_POWER_MEASUREMENT								0x00	RO
0x0D	Reserved	RV								0x00	RV
0x0E	SWB Current & Power Measurement	RV		SWB_OUTPUT_CURRENT_POWER_MEASUREMENT						0x00	RO
0x0F	SWC Current & Power Measurement	RV		SWC_OUTPUT_CURRENT_POWER_MEASUREMENT						0x00	RO
0x10	Clear Status Bits_0	RV		A_PG	RV	B_PG	C_PG	RV	VIN_BUCK_OV	0x00	W1O
0x11	Clear Status Bits_1	HTW	RV	LDO_1.8V_PG	RV	A_HCW	RV	B_HCW	C_HCW	0x00	W1O
0x12	Clear Status Bits_2	A_OV	RV	B_OV	C_OV	PEC_ERR	PARITY_ERR	RV		0x00	W1O
0x13	Clear Status Bits_3	A_OC	RV	B_OC	C_OC	A_UVLO	RV	B_UVLO	C_UVLO	0x00	W1O
0x14	Clear Status Bits_4	RV					LDO_1.0V_PG	RV	GLOBAL_CLR	0x00	W1O
0x15	Mask Status_0	RV		A_PG	RV	B_PG	C_PG	RV	VIN_BUCK_OV	0x2C	RW
0x16	Mask Status_1	HTW	RV	LDO_1.8V_PG	RV	A_HCW	RV	B_HCW	C_HCW	0x20	RW
0x17	Mask Status_2	A_OV	RV	B_OV	C_OV	PEC_ERR	PARITY_ERR	RV		0x00	RW
0x18	Mask Status_3	A_OC	RV	B_OC	C_OC	A_UVLO	RV	B_UVLO	C_UVLO	0x00	RW
0x19	Mask Status_4	RV					LDO_1.0V_PG	RV		0x04	RW
0x1A	Threshold Settings_1	RV			LOW_IQ_EN	RV	LDO_1.8V_PG	POWER_MEAS_	LDO_1.0V_PG	0x00	RW

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
								SEL			
0x1B	Threshold Settings_2	VIN_BUCK_OV	CURRENT_OR_POWER_SEL	RV	PG_MASK	GSI_N _EN	HTW			0x05	RW
0x1C	SWA High Current Warning Threshold	SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_TH						RV		0x60	RW
0x1D	Reserved	RV								0x00	RV
0x1E	SWB High Current Warning Threshold	SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_TH						RV		0x60	RW
0x1F	SWC High Current Warning Threshold	SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_TH						RV		0x60	RW
0x20	OC Threshold	A_OC		RV		B_OC		C_OC		0xCF	RW
0x21	SWA Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RW
0x22	SWA Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RW
0x23	Reserved	RV								0x00	RV
0x24	Reserved	RV								0x00	RW
0x25	SWB Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RW
0x26	SWB Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RW
0x27	SWC Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RW
0x28	SWC Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RW
0x29	FSW & Mode_1	A_MODE_SEL		A_FSW		RV				0x80	RW
0x2A	FSW & Mode_2	B_MODE_SEL		B_FSW		C_MODE_SEL		C_FSW		0x88	RW
0x2B	Buck & LDO Output Voltage Range	LDO_1.8V_VOLTAGE		RV			LDO_1.0V_VOLTAGE		RV	0x42	RW
0x2C	Soft-start Time_1	A_SOFT_START_TIME			RV					0x20	RW
0x2D	Soft-start Time_2	B_SOFT_START_TIME			RV	C_SOFT_START_TIME			RV	0x22	RW
0x2E	OTP Threshold	RV					OTP			0x04	RW
0x2F	PMIC Configuration	RV	A_EN	RV	B_EN	C_EN	WRITE_PROTECTION	MASK_BITS_REGISTER_CONTROL		0x06	RW
0x30	ADC Configuration	ADC_EN	ADC_SEL				RV	ADC_UPDATE_FREQ		0x00	RW
0x31	ADC Read	ADC_READ								0x00	RO
0x32	PMIC_EN & Interface	VR_EN	I2C/I3C	PG_IO_TYPE	PG_CONTROL		RV			0x00	RW/RO

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
	Selection										
0x33	PMIC Status_4	TEMP_MEAS			RV		LDO_1.0V_PG	RV		0x00	RO
0x34	PEC/IBI/PARITY/HID_CODE	PEC_EN	IBI_EN	PARITY_DIS	RV	HID_CODE			RV	0x0E	RO
0x35	Error Injection	EN	RAIL_SEL			OV_UV_ERR_TYPE	MISC_ERROR_TYPE			0x00	RW
0x36	Reserved	RV								0x00	RV
0x37	DIMM Vendor Region Password Lower Byte	DIMM_VENDOR_PASSWORD_L								0x00	W
0x38	DIMM Vendor Region Password Upper Byte	DIMM_VENDOR_PASSWORD_H								0x00	W
0x39	DIMM Vendor Password Control	DIMM_VENDOR_PASSWORD_CONTROL								0x00	RW
0x3A	Default Address Pointer Function	RV	EN	STARTING_ADDRESS		BURST_LENGTH		RV		0x00	RW
0x3B	Revision ID	RV		MAJREV		MINREV			RV	--	ROE
0x3C	Vendor ID Byte_0	VENDOR_ID_BYTE0								0x8A	ROE
0x3D	Vendor ID Byte_1	VENDOR_ID_BYTE1								0x8C	ROE
0x3E	Reserved	RV								0x00	RV
0x3F	Reserved	RV								0x00	RV
0x40	Power-on sequence Configuration 0	SEQ_EN	A_EN	RV	B_EN	C_EN	IDLE_TIME			0x89	RWPE
0x41	Power-on sequence Configuration 1	SEQ_EN	A_EN	RV	B_EN	C_EN	IDLE_TIME			0xD9	RWPE
0x42	Power-on sequence Configuration 2	SEQ_EN	A_EN	RV	B_EN	C_EN	IDLE_TIME			0x00	RWPE
0x43	Reserved	RV								0x00	RWPE
0x44	Reserved	RV								0x00	RWPE
0x45	DIMM_SWA Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RWPE
0x46	DIMM_SWA Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RWPE
0x47	Reserved	RV								0x00	RWPE
0x48	Reserved	RV								0x00	RWPE
0x49	DIMM_SWB Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RWPE

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x4A	DIMM_ SWB Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RWPE
0x4B	DIMM_ SWC Voltage & Threshold	VOLTAGE_SETTING							PGL	0x78	RWPE
0x4C	DIMM_ SWC Threshold & Soft-stop Time	PGH		OV		UVLO		SOFT_STOP_TIME		0x63	RWPE
0x4D	DIMM_ FSW & Mode_ 1	A_MODE_SEL		A_FSW		Reserved				0x80	RWPE
0x4E	DIMM_ FSW & Mode_ 2	B_MODE_SEL		B_FSW		C_MODE_SEL		C_FSW		0x88	RWPE
0x4F	Reserved	RV								0x00	RWPE
0x50	DIMM_ OC Threshold	A_OC		RV		B_OC		C_OC		0xCF	RWPE
0x51	DIMM_ Buck & LDO Output Voltage Range	LDO_1.8V_ VOLTAGE		RV		RV	LDO_1.0V_VOLTAGE		RV	0x42	RWPE
0x52	Reserved	RV								0x00	RV
0x53	Reserved	RV								0x00	RV
0x54	Reserved	RV								0x00	RV
0x55	Reserved	RV								0x00	RV
0x56	Reserved	RV								0x00	RV
0x57	Reserved	RV								0x00	RV
0x58	Power-off sequence Configuration 0	SEQ_EN	A_DIS	RV	B_DIS	C_DIS	IDLE_TIME			0xD1	RWPE
0x59	Power-off sequence Configuration 1	SEQ_EN	A_DIS	RV	B_DIS	C_DIS	IDLE_TIME			0xD9	RWPE
0x5A	Power-off sequence Configuration 2	SEQ_EN	A_DIS	RV	B_DIS	C_DIS	IDLE_TIME			0x00	RWPE
0x5B	Reserved	RV								0x00	RV
0x5C	Reserved	RV								0x00	RV
0x5D	DIMM_Soft-start Time_1	A_SOFT_START_TIME			RV					0x20	RWPE
0x5E	DIMM_Soft-start Time_2	B_SOFT_START_TIME			RV	C_SOFT_START_TIME			RV	0x22	RWPE
0x5F	Reserved	RV								0x00	RV
0x60	Reserved	RV								0x00	RV
0x61	Reserved	RV								0x00	RV
0x62	Reserved	RV								0x00	RV
0x63	Reserved	RV								0x00	RV
0x64	Reserved	RV								0x00	RV

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Type
0x65	Reserved	RV								0x00	RV
0x66	Reserved	RV								0x00	RV
0x67	Reserved	RV								0x00	RV
0x68	Reserved	RV								0x00	RV
0x69	Reserved	RV								0x00	RV
0x6A	Reserved	RV								0x00	RV
0x6B	Reserved	RV								0x00	RV
0x6C	Reserved	RV								0x00	RV
0x6D	Reserved	RV								0x00	RV
0x6E	Reserved	RV								0x00	RV
0x6F	Reserved	RV								0x00	RV

B-5 Host Region Registers

Table 16. Reserved 0x00

Address: 0x00 Description: Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x00 [7:0]: Reserved

Table 17. Reserved 0x01

Address: 0x01 Description: Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x01 [7:0]: Reserved

Table 18. Reserved 0x02

Address: 0x02 Description: Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x02 [7:0]: Reserved

Table 19. Reserved 0x03

Address: 0x03 Description: Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x03 [7:0]: Reserved

Table 20. Global Error Log

Address: 0x04 Description: Global Error Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	0x04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation 0 = No Error or Only 1 Error since last Erase Operation 1 = > 1 Error Count since last Erase Operation
6	ROE	0	0x04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Overvoltage or Undervoltage 0 = No Error Occurred 1 = Error Occurred
5	ROE	0	0x04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOTLAGE Global Error Log History for VIN_BULK Overvoltage 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	0x04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	0x04 [3:0]: Reserved

Table 21. PG-on-Reset ERR Log

Address: 0x05 **Description:** PG-on-Reset ERR Log			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	0x05 [7]: Reserved
6	ROE	0	0x05 [6]: SWA_POWER_GOOD SWA Condition from Previous Power Cycle 0 = Normal Power-On 1 = SWA Power Not Good
5	RV	0	0x05 [5]: Reserved
4	ROE	0	0x05 [4]: SWB_POWER_GOOD SWB Condition from Previous Power Cycle 0 = Normal Power-On 1 = SWB Power Not Good
3	ROE	0	0x05 [3]: SWC_POWER_GOOD SWC Condition from Previous Power Cycle 0 = Normal Power-On 1 = SWC Power Not Good
2:0	ROE	0	0x05 [2:0]: PMIC_ERROR_LOG PMIC Power On - High Level Status Bit to Indicate previous power down cycle 000 = Normal Power-On 001 = Reserved 010 = Buck Regulator Output Over or Undervoltage 011 = Critical Temperature 100 = VIN_Bulk Input Overvoltage 101 = Reserved 110 = Reserved 111 = Reserved

Table 22. UVLO/OV ERR Log

Address: 0x06 **Description:** UVLO/OV ERR Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	0x06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWA Undervoltage Lockout 0 = Normal Power-On 1 = Power-On - SWA Undervoltage Lockout
6	RV	0	0x06 [6]: Reserved
5	ROE	0	0x06 [5]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWB Undervoltage Lockout 0 = Normal Power-On 1 = SWB Undervoltage Lockout
4	ROE	0	0x06 [4]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWC Undervoltage Lockout 0 = Normal Power-On 1 = SWC Undervoltage Lockout
3	ROE	0	0x06 [3]: SWA_OVER_VOLTAGE PMIC Power-On - SWA Overvoltage 0 = Normal Power-On 1 = SWA Overvoltage
2	RV	0	0x06 [2]: Reserved
1	ROE	0	0x06 [1]: SWB_OVER_VOLTAGE PMIC Power-On - SWB Overvoltage 0 = Normal Power-On 1 = SWB Overvoltage
0	ROE	0	0x06 [0]: SWC_OVER_VOLTAGE PMIC Power-On - SWC Overvoltage 0 = Normal Power-On 1 = SWC Overvoltage

Table 23. Reserved 0x07

Address: 0x07 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x07 [7:0]: Reserved

Table 24. Power Good Status

Address: 0x08 Description: Power Good Status			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	0x08 [7]: Reserved
6	RO	0	0x08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	0x08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status 0 = Power Good 1 = Power Not Good
4	RV	0	0x08 [4]: Reserved
3	RO	0	0x08 [3]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status 0 = Power Good 1 = Power Not Good
2	RO	0	0x08 [2]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status 0 = Power Good 1 = Power Not Good
1	RV	0	0x08 [1]: Reserved
0	RO	0	0x08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_BULK Input Supply Overvoltage Status 0 = No Overvoltage 1 = Overvoltage

Table 25. PMIC Status_1

Address: 0x09 **Description:** PMIC Status_1			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	0x09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RV	0	0x09 [6]: Reserved
5	RO	0	0x09 [5]: VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS VLDO_1.8V LDO Output Power Good Status 0 = Power Good 1 = Power Not Good
4	RV	0	0x09 [4]: Reserved
3	RO	0	0x09[3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
2	RV	0	0x09 [2]: Reserved
1	RO	0	0x09 [1]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
0	RO	0	0x09 [0]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning

Table 26. PMIC Status_2

Address: 0x0A Description: PMIC Status_2			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	0x0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
6	RV	0	0x0A [6]: Reserved
5	RO	0	0x0A [5]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
4	RO	0	0x0A [5]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Overvoltage Status 0 = No Overvoltage 1 = Overvoltage
3	RO	0	0x0A [3]: PEC_ERROR_STATUS Packet Error Code Status 0 = No PEC Error 1 = PEC Error
2	RO	0	0x0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status 0 = No Parity Error 1 = Parity Error
1	RO	0	0x0A [1]: IBI_STATUS In Band Interrupt Status 0 = No Pending IBI 1 = Pending IBI
0	RV	0	0x0A [0]: Reserved

Table 27. PMIC Status_3

Address: 0x0B **Description:** PMIC Status_3			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	0x0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
6	RV	0	0x0B [6]: Reserved
5	RO	0	0x0B [5]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	0x0B [4]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
3	RO	0	0x0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Undervoltage Lockout Status 0 = No Undervoltage Lockout 1 = Undervoltage Lockout
2	RV	0	0x0B [2]: Reserved
1	RO	0	0x0B [1]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Undervoltage Lockout Status 0 = No Undervoltage Lockout 1 = Undervoltage Lockout
0	RO	0	0x0B [0]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Undervoltage Lockout Status 0 = No Undervoltage Lockout 1 = Undervoltage Lockout

Table 28. SWA Current and Power Measurement

Address: 0x0C **Description:** SWA Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	0x0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT If Register 0x1A [1] = 0, Switch Node A Output Current or Output Power Measurement 0000 0000 = Un-defined 0000 0001 = 0.125A or 125mW 0000 0010 = 0.25A or 250mW 0000 0011 = 0.375A or 375mW 0000 0100 = 0.5A or 500mW 0000 0101 = 0.625A or 625mW 0000 0110 = 0.75A or 750mW 0000 0111 = 0.875A or 875mW 0000 1000 = 1.0A or 1000mW 0000 1001 = 1.125A or 1125mW .. 0011 0111 = 6.875A or 6875mW 0011 1000 = 7.0A or 7000mW 0011 1001 = 7.125A or 7125mW 0011 1010 = 7.25A or 7250mW 0011 1011 = 7.375A or 7375mW 0011 1100 = 7.5A or 7500mW 0011 1101 = 7.625A or 7625mW 0011 1110 = 7.75A or 7750mW 0011 1111 ≥ 7.875A or 7875mW All other encodings are reserved If Register 0x1A [1] = 1, Sum of SWA, SWB and SWC Output Power 0000 0000 = Un-defined 0000 0001 = 125mW 0000 0010 = 250mW 0000 0011 = 375mW 0000 0100 = 500mW ... 1111 1100 = 31500mW 1111 1101 = 31625mW 1111 1110 = 31750mW 1111 1111 ≥ 31875mW

Table 29. Reserved 0x0D

Address: 0x0D **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x0D [7:0]: Reserved

Table 30. SWB Current and Power Measurement

Address: 0x0E **Description:** SWB Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	0x0E [7:6]: Reserved
5:0	RO	0	0x0E [5:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW 001010 = 1.25A or 1250mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 ≥ 7.875A or 7875mW

Table 31. SWC Current and Power Measurement

Address: 0x0F **Description:** SWC Current and Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	0x0F [7:6]: Reserved
5:0	RO	0	0x0F [5:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power Measurement 000000 = Un-defined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 ≥ 7.875A or 7875mW

Table 32. Clear Status Bits_0

Address: 0x10 **Description:** Clear Status Bits_0			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	0x10 [7:6]: Reserved
5	1O	0	0x10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear “Register 0x08” [5]
4	RV	0	0x10 [4]: Reserved
3	1O	0	0x10 [3]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power Good Status. 1 = Clear “Register 0x08” [3]
2	1O	0	0x10 [2]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear “Register 0x08” [2]
1	RV	0	0x10 [1]: Reserved
0	1O	0	0x10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear VIN_BULK Input Supply Overvoltage Status. 1 = Clear “Register 0x08” [0]

Table 33. Clear Status Bits_1

Address: 0x11 **Description:** Clear Status Bits_1			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	0x11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status. 1 = Clear “Register 0x09” [7]
6	RV	0	0x11 [6]: Reserved
5	1O	0	0x11 [5]: CLEAR_VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VLDO_1.8V Output Power Good Status 1 = Clear “Register 0x09” [5]
4	RV	0	0x11 [4]: Reserved
3	1O	0	0x11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear “Register 0x09” [3]
2	RV	0	0x11 [2]: Reserved
1	1O	0	0x11 [1]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status. 1 = Clear “Register 0x09” [1]
0	1O	0	0x11 [0]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. 1 = Clear “Register 0x09” [0]

Table 34. Clear Status Bits_2

Address: 0x12 **Description:** Clear Status Bits_2			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	0x12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Overvoltage Status. 1 = Clear “Register 0x0A” [7]
6	RV	0	0x12 [6]: Reserved
5	1O	0	0x12 [5]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Overvoltage Status. 1 = Clear “Register 0x0A” [5]
4	1O	0	0x12 [4]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Overvoltage Status. 1 = Clear “Register 0x0A” [4]
3	1O	0	0x12 [3]: CLEAR_PEC_ERROR_STATUS Clear PEC Error Status. 1 = Clear “Register 0x0A” [3]
2	1O	0	0x12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear “Register 0x0A” [2]
1:0	RV	0	0x12 [1:0]: Reserved

Table 35. Clear Status Bits_3

Address: 0x13 **Description:** Clear Status Bits_3			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	0x13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear “Register 0x0B” [7]
6	RV	0	0x13 [6]: Reserved
5	1O	0	0x13 [5]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status. 1 = Clear “Register 0x0B” [5]
4	1O	0	0x13 [4]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. 1 = Clear “Register 0x0B” [4]
3	1O	0	0x13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Undervoltage Lockout Status. 1 = Clear “Register 0x0B” [3]
2	RV	0	0x13 [2]: Reserved
1	1O	0	0x13 [1]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Undervoltage Lockout Status. 1 = Clear “Register 0x0B” [1]
0	1O	0	0x13 [0]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Undervoltage Lockout Status. 1 = Clear “Register 0x0B” [0]

Table 36. Clear Status Bits_4

Address: 0x14 **Description:** Clear Status Bits_4			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	0x14 [7:3]: Reserved
2	1O	0	0x14 [2]: CLEAR_VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VLDO_1.0V Output Power Good Status. 1 = Clear “Register 0x33” [2]
1	RV	0	0x14 [1]: Reserved
0	1O	0	0x14 [0]: GLOBAL_CLEAR_STATUS Clear all status bits. 1 = Clear all status bits

Table 37. Mask Status_0

Address: 0x15 **Description:** Mask Status_0			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	0x15 [7:6]: Reserved
5	RW	1	0x15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power Good Status Event. 0 = Do Not Mask SWA Output Power Good Status Event 1 = Mask SWA Output Power Good Status Event
4	RV	0	0x15 [4]: Reserved
3	RW	1	0x15 [3]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power Good Status Event. 0 = Do Not Mask SWB Output Power Good Status Event 1 = Mask SWB Output Power Good Status Event
2	RW	1	0x15 [2]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power Good Status Event. 0 = Do Not Mask SWC Output Power Good Status Event 1 = Mask SWC Output Power Good Status Event
1	RV	0	0x15 [1]: Reserved
0	RW	0	0x15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Overvoltage Status Event. 0 = Do Not Mask VIN_Bulk Input Supply Overvoltage Status Event 1 = Mask VIN_Bulk Input Supply Overvoltage Status Event

Table 38. Mask Status_1

Address: 0x16 Description: Mask Status_1			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event. 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event
6	RV	0	0x16 [6]: Reserved
5	RW	1	0x16 [5]: MASK_VLDO_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VLDO_1.8V Output Power Good Status Event. 0 = Do Not Mask 1.8V Output Power Good Status Event 1 = Mask 1.8V Output Power Good Status Event
4	RV	0	0x16 [4]: Reserved
3	RW	0	0x16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node A High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Consumption Warning Status Event 1 = Mask Switch Node A Output Current Consumption Warning Status Event
2	RV	0	0x16 [2]: Reserved
1	RW	0	0x16 [1]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node B High Output Current Consumption Warning Status Event 0 = Do Not Mask Switch Node B Output Current Consumption Warning Status Event 1 = Mask Switch Node B Output Current Consumption Warning Status Event
0	RW	0	0x16 [0]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node C High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Consumption Warning Status Event 1 = Mask Switch Node C Output Current Consumption Warning Status Event

Table 39. Mask Status_2

Address: 0x17 **Description:** Mask Status_2			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node A Output Overvoltage Status Event. 0 = Do Not Mask Switch Node A Output Overvoltage Status Event 1 = Mask Switch Node A Output Overvoltage Status Event
6	RV	0	0x17 [6]: Reserved
5	RW	0	0x17 [5]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node B Output Overvoltage Status Event. 0 = Do Not Mask Switch Node B Output Overvoltage Status Event 1 = Mask Switch Node B Output Overvoltage Status Event
4	RW	0	0x17 [4]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node C Output Overvoltage Status Event. 0 = Do Not Mask Switch Node C Output Overvoltage Status Event 1 = Mask Switch Node C Output Overvoltage Status Event
3	RW	0	0x17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	0x17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status
1:0	RV	0	0x17 [1:0]: Reserved

Table 40. Mask Status_3

Address: 0x18 **Description:** Mask Status_3			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node A Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Limiter Warning Status Event 1 = Mask Switch Node A Output Current Limiter Warning Status Event
6	RV	0	0x18 [6]: Reserved
5	RW	0	0x18 [5]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node B Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node B Output Current Limiter Warning Status Event 1 = Mask Switch Node B Output Current Limiter Warning Status Event
4	RW	0	0x18 [4]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node C Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Limiter Warning Status Event 1 = Mask Switch Node C Output Current Limiter Warning Status Event
3	RW	0	0x18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node A Output Undervoltage Lockout Status Event. 0 = Do Not Mask Switch Node A Output Undervoltage Lockout Status Event 1 = Mask Switch Node A Output Undervoltage Lockout Status Event
2	RV	0	0x18 [2]: Reserved
1	RW	0	0x18 [1]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node B Output Undervoltage Lockout Status Event. 0 = Do Not Mask Switch Node B Output Undervoltage Lockout Status Event 1 = Mask Switch Node B Output Undervoltage Lockout Status Event
0	RW	0	0x18 [0]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node C Output Undervoltage Lockout Status Event. 0 = Do Not Mask Switch Node C Output Undervoltage Lockout Status Event 1 = Mask Switch Node C Output Undervoltage Lockout Status Event

Table 41. Mask Status_4

Address: 0x19 **Description:** Mask Status_4			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	0x19 [7:3]: Reserved
2	RW	1	0x19 [2]: MASK_VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VLDO_1.0V Output Power Good Status Event. 0 = Do Not Mask 1.0V Output Power Good Status Event 1 = Mask 1.0V Output Power Good Status Event
1:0	RV	0	0x19 [1:0]: Reserved

Table 42. Threshold Settings_1

Address: 0x1A **Description:** Threshold Settings_1			
Bits	**Attribute**	**Default**	**Description**
7:5	RV	0	0x1A [7:5]: Reserved
4	RW	0	0x1A [4]: QUIESCENT_STATE_EN PMIC Quiescent State Entry Enable 0 = Disable 1 = Enable
3	RV	0	0x1A [3]: Reserved
2	RW	0	0x1A [2]: VLDO_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6V 1 = Reserved
1	RW	0	0x1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select 0 = Report Power Measurement for Each Rail in 0x0C, 0x0E & 0x0F 1 = Report Total Power Measurement of Each Rail in 0x0C
0	RW	0	0x1A [0]: VLDO_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = −10% from the setting in “Register 0x51” [2:1] 1 = −15% from the setting in “Register 0x51” [2:1]

Table 43. Threshold Settings_2

Address: 0x1B **Description:** Threshold Settings_2			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_Bulk Input Overvoltage Threshold Setting For GSI_n Assertion 0 = 6V 1 = Reserved
6	RW	0	0x1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers 1 = Report Power Measurements in registers
5	RV	0	0x1B [5]: Reserved
4	RW	0	0x1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin 0 = Not Masked 1 = Masked
3	RW	0	0x1B [3]: GSI_N_PIN_ENABLE Enable GSI_n Pin 0 = Disable GSI_n Pin 1 = Enable GSI_n Pin
2:0	RW	101	0x1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold 000 = Reserved 001 = PMIC temperature ≥ 85°C 010 = PMIC temperature ≥ 95°C 011 = PMIC temperature ≥ 105°C 100 = PMIC temperature ≥ 115°C 101 = PMIC temperature ≥ 125°C 110 = PMIC temperature ≥ 135°C 111 = Reserved

Table 44. SWA High Current Warning Threshold

Address: 0x1C **Description:** SWA High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	0x1C [7:2]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 ≥ 0.125A 000010 ≥ 0.25A 000011 ≥ 0.375A 000100 ≥ 0.5A 000101 ≥ 0.625A 000110 ≥ 0.75A 000111 ≥ 0.875A 001000 ≥ 1.0A 001001 ≥ 1.125A ... ... 010111 ≥ 2.875A 011000 ≥ 3.0A 011001 ≥ 3.125A ... 110111 ≥ 6.875A 111000 ≥ 7.0A 111001 ≥ 7.125A 111010 ≥ 7.25A 111011 ≥ 7.375A 111100 ≥ 7.5A 111101 ≥ 7.625A 111110 ≥ 7.75A 111111 ≥ 7.875A
1:0	RV	0	0x1C [1:0]: Reserved

Table 45. Reserved 0x1D

Address: 0x1D **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x1D [7:0]: Reserved

Table 46. SWB High Current Warning Threshold

Address: 0x1E **Description:** SWB High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	0x1E [7:2]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 ≥ 0.125A 000010 ≥ 0.25A 000011 ≥ 0.375A 000100 ≥ 0.5A 000101 ≥ 0.625A 000110 ≥ 0.75A 000111 ≥ 0.875A 001000 ≥ 1.0A 001001 ≥ 1.125A ... 010111 ≥ 2.875A 011000 ≥ 3.0A ... 110111 ≥ 6.875A 111000 ≥ 7.0A 111001 ≥ 7.125A 111010 ≥ 7.25A 111011 ≥ 7.375A 111100 ≥ 7.5A 111101 ≥ 7.625A 111110 ≥ 7.75A 111111 ≥ 7.875A
1:0	RV	0	0x1E [1:0]: Reserved

Table 47. SWC High Current Warning Threshold

Address: 0x1F **Description:** SWC High Current Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	0x1F [7:2]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 ≥ 0.125A 000010 ≥ 0.25A 000011 ≥ 0.375A 000100 ≥ 0.5A 000101 ≥ 0.625A 000110 ≥ 0.75A 000111 ≥ 0.875A 001000 ≥ 1.0A 001001 ≥ 1.125A ... 010111 ≥ 2.875A 011000 ≥ 3.0A 011001 ≥ 3.125A ... 110111 ≥ 6.875A 111000 ≥ 7.0A 111001 ≥ 7.125A 111010 ≥ 7.25A 111011 ≥ 7.375A 111100 ≥ 7.5A 111101 ≥ 7.625A 111110 ≥ 7.75A 111111 ≥ 7.875A
1:0	RV	0	0x1F [1:0]: Reserved

Table 48. OC Threshold

Address: 0x20 **Description:** OC Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	11	0x20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 3.0A 01 = 3.5A 10 = 4.0A 11 = 4.5A
5:4	RV	0	0x20 [5:4]: Reserved
3:2	RW	11	0x20 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 3.0A 01 = 3.5A 10 = 4.0A 11 = 4.5A
1:0	RW	11	0x20 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 0.5A 01 = 1.0A 10 = 1.5A 11 = 2.0A

Table 49. SWA Voltage Setting

Address: 0x21 **Description:** SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	0x21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RW	0	0x21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register 0x21” [7:1] 1 = –7.5% from the setting in “Register 0x21” [7:1]

Table 50. SWA Threshold & Soft-stop Time

Address: 0x22 **Description:** SWA Threshold & Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	0x22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound level” For Power Good Status 00 = +5% from the setting in “Register 0x21” [7:1] 01 = +7.5% from the setting in “Register 0x21” [7:1] 10 = +10% from the setting in “Register 0x21” [7:1] 11 = +2.5% from the setting in “Register 0x21” [7:1]
5:4	RW	10	0x22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register 0x21” [7:1] 01 = +10% from the setting in “Register 0x21” [7:1] 10 = +12.5% from the setting in “Register 0x21” [7:1] 11 = +5% from the setting in “Register 0x21” [7:1]
3:2	RW	00	0x22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register 0x21” [7:1] 01 = –12.5% from the setting in “Register 0x21” [7:1] 10 = –5% from the setting in “Register 0x21” [7:1] 11 = –7.5% from the setting in “Register 0x21” [7:1]
1:0	RW	11	0x22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 51. Reserved 0x23

Address: 0x23 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x23 [7:0]: Reserved

Table 52. Reserved 0x24

Address: 0x24 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x24 [7:0]: Reserved

Table 53. SWB Voltage Setting

Address: 0x25 **Description:** SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	0x25 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RW	0	0x25 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register 0x25” [7:1] 1 = –7.5% from the setting in “Register 0x25” [7:1]

Table 54. SWB Threshold & Soft-stop Time

Address: 0x26 **Description:** SWB Threshold & Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	0x26 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register 0x25” [7:1] 01 = +7.5% from the setting in “Register 0x25” [7:1] 10 = +10% from the setting in “Register 0x25” [7:1] 11 = +2.5% from the setting in “Register 0x25” [7:1]
5:4	RW	10	0x26 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register 0x25” [7:1] 01 = +10% from the setting in “Register 0x25” [7:1] 10 = +12.5% from the setting in “Register 0x25” [7:1] 11 = +5% from the setting in “Register 0x25” [7:1]
3:2	RW	00	0x26 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register 0x25” [7:1] 01 = –12.5% from the setting in “Register 0x25” [7:1] 10 = –5% from the setting in “Register 0x25” [7:1] 11 = –7.5% from the setting in “Register 0x25” [7:1]
1:0	RW	11	0x26 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 55. SWC Voltage Setting

Address: 0x27 **Description:** SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	0x27 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 1500mV 000 0001 = 1505mV 000 0010 = 1510mV ... 011 1100 = 1800mV ... 111 1101 = 2125mV 111 1110 = 2130mV 111 1111 = 2135mV
0	RW	0	0x27 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register 0x27” [7:1] 1 = –7.5% from the setting in “Register 0x27” [7:1]

Table 56. SWC Threshold & Soft-stop Time

Address: 0x28 **Description:** SWC Threshold & Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	0x28 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register 0x27” [7:1] 01 = +7.5% from the setting in “Register 0x27” [7:1] 10 = +10% from the setting in “Register 0x27” [7:1] 11 = +2.5% from the setting in “Register 0x27” [7:1]
5:4	RW	10	0x26 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register 0x27” [7:1] 01 = +10% from the setting in “Register 0x27” [7:1] 10 = +12.5% from the setting in “Register 0x27” [7:1] 11 = +5% from the setting in “Register 0x27” [7:1]
3:2	RW	00	0x26 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register 0x27” [7:1] 01 = –12.5% from the setting in “Register 0x27” [7:1] 10 = –5% from the setting in “Register 0x27” [7:1] 11 = –7.5% from the setting in “Register 0x27” [7:1]
1:0	RW	11	0x26 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

Table 57. FSW & Mode_1

Address: 0x29 **Description:** FSW & Mode_1			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	0x29 [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	0x29 [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency (Note) 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:0	RV	00	0x29 [3:0]: Reserved

Table 58. FSW & Mode_2

Address: 0x2A **Description:** FSW & Mode_2			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	0x2A [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	0x2A [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RW	10	0x2A [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	00	0x2A [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

Table 59. LDO Output Voltage Range

Address: 0x2B **Description:** LDO Output Voltage Range			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	0x2B [7:6]: VLDO_1.8V _VOLTAGE_SETTING VLDO_1.8V Voltage Setting: 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	000	0x2B [5:3]: Reserved
2:1	RW	01	0x2B [2:1]: VLDO_1.0V _VOLTAGE_SETTING VLDO_1.0V Voltage Setting: 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	0x2B [0]: Reserved

Table 60. Soft-start Time_1

Address: 0x2C **Description:** Soft-start Time_1			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	0x2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4:0	RV	0	0x2C [4:0]: Reserved

Table 61. Soft-start Time_2

Address: 0x2D **Description:** Soft-start Time_2			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	0x2D [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	0x2D [4]: Reserved
3:1	RW	001	0x2D [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	0x2D [0]: Reserved

Table 62. OTP Threshold

Address: 0x2E **Description:** OTP Threshold			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	10110	0x2E [7:3]: Internal settings
2:0	RW	100	0x2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature ≥ 105°C 001 = PMIC Temperature ≥ 115°C 010 = PMIC Temperature ≥ 125°C 011 = PMIC Temperature ≥ 135°C 100 = PMIC Temperature ≥ 145°C 101 = Reserved 110 = Reserved 111 = Reserved

Table 63. PMIC Configuration

Address: 0x2F **Description:** PMIC Configuration			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	0x2F [7]: Reserved
6	RW	0	0x2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	0x2F [5]: Reserved
4	RW	0	0x2F [4]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RW	0	0x2F [3]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2	RW	1	0x2F [2]: SECURE_MODE PMIC Mode Operation 0 = Secure Mode Operation 1 = Programmable Mode Operation
1:0	RW	10	0x2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Only (GSI_n signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved

Table 64. ADC Configuration

Address: 0x30 **Description:** ADC Configuration			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable 1 = Enable
6:3	RW	0	0x30 [6:3]: ADC_SELECT Input Selection for ADC Readout 0000 = SWA Output Voltage 0001 = Reserved 0010 = SWB Output Voltage 0011 = SWC Output Voltage 0100 = Reserved 0101 = VIN_BULK Input Voltage 0110 = Reserved 0111 = Reserved 1000 = VLDO_1.8V Output Voltage 1001 = VLDO_1.0V Output Voltage All other encodings are reserved.
2	RV	0	0x30 [2]: Reserved
1:0	RW	0	0x30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

Table 65. ADC Read

Address: 0x31 **Description:** ADC Read			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	0x31 [7:0]: ADC_READ ADC Output Voltage Reading (Applies to SW[A:C], VLDO_1.8V, VLDO_1.0V) 0000 0000 = Undefined 0000 0001 = 15mV 0000 0010 = 30mV .. 1111 1111 ≥ 3825mV ADC Output Voltage Reading (Applies to VIN_BULK Input Voltage) 0000 0000 = Undefined 0000 0001 = 70mV 0000 0010 = 140mV .. 1111 1111 ≥ 17850mV

Table 66. PMIC_EN & Interface Selection

Address: 0x32 **Description:** PMIC_EN & Interface Selection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x32 [7]: VR_ENABLE PMIC Enable 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	0x32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection 0 = I^2C Interface (Max speed 1MHz) 1 = I3C Basic Protocol
5	RW	0	0x32 [5]: PWR_GOOD_IO_TYPE PMIC PWR_GOOD Output Signal Type 0 = Output only 1 = Input and Output
4:3	RW	0	0x32 [4:3]: PMIC_PWR _OUTPUT_SIGNAL_CONTROL PMIC PWR_GOOD Output Signal Control 0x = PMIC controls PWR_GOOD on its own based on internal status 10 = PWR_GOOD Output Low 11 = PWR_GOOD Output Float
2:0	RV	0	0x32 [2:0]: Reserved

Table 67. PMIC Status_4

Address: 0x33 **Description:** PMIC Status_4			
Bits	**Attribute**	**Default**	**Description**
7:5	RO	0	0x33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature 000 =< 80°C (± 5°C) 001 = 85°C (± 5°C) 010 = 95°C (± 5°C) 011 = 105°C (± 5°C) 100 = 115°C (± 5°C) 101 = 125°C (± 5°C) 110 = 135°C (± 5°C) 111 ≥ 140°C (± 5°C)
4:3	RV	0	0x33 [4:3]: Reserved
2	RO	0	0x33 [2]: VLDO_1.0V_OUTPUT_POWER_GOOD_STATUS VLDO_1.0V LDO Output Power Good Status 0 = Power Good 1 = Power Not Good
1:0	RV	0	0x33 [1:0]: Reserved

Table 68. PEC/IBI/PARITY/HID_CODE

Address: 0x34 **Description:** PEC/IBI/PARITY/HID_CODE			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	0x34 [7]: PEC_ENABLE Packet Error Code Enable (Applicable Only if 0x32 [6] = ‘1’) 0 = Disable 1 = Enable
6	RO	0	0x34 [6]: IBI_ENABLE In Band Interrupt Enable (Applicable Only if 0x32 [6] = ‘1’) 0 = Disable 1 = Enable
5	RO	0	0x34 [5]: PARITY_DISABLE T Bit Parity Code Disable (Applicable Only if 0x32 [6] = ‘1’.) 0 = Enable 1 = Disable
4	RV	0	0x34 [4]: Reserved
3:1	RO	111	0x34 [3:1]: HID_CODE PMIC’s 3-bit HID Code 000 001 010 011 100 101 110 111
0	RV	0	0x34 [0]: Reserved

Table 69. Error Injection

Address: 0x35 **Description:** Error Injection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	0x35 [7]: ERROR_INJECTION_ENABLE Error Injection Enable 0 = Disable 1 = Enable
6:4	RW	0	0x35 [6:4]: ERROR_INJECTION_RAIL_SELECTION Error Injection - Input Rail and Output Rail Selection 000 = Undefined 001 = SWA Output Only 010 = Reserved 011 = SWB Output Only 100 = SWC Output Only 101 = VIN_Bulk Input Only 110 = Reserved 111 = Do Not Use
3	RW	0	0x35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT Overvoltage or Undervoltage Selection for Bits 0x35[6:4] 0 = Overvoltage 1 = Undervoltage
2:0	RW	0	0x35 [2:0]: MISC_ERROR_INJECTION_TYPE Miscellaneous Error Injection Type 000 = Undefined 001 = Reserved 010 = Critical Temperature Shutdown 011 = High Temperature Warning Threshold 100= VLDO_1.8V LDO Power Good 101 = High Current Consumption Warning 110 = Reserved 111 = Current Limiter Warning

Table 70. Reserved 0x36

Address: 0x36 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x36 [7:0]: Reserved

Table 71. DIMM Vendor Region Password Lower Byte

Address: 0x37 **Description:** DIMM Vendor Region Password Lower Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0	0x37 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (0x40 - R6F) Password - Lower Byte [7:0] = 0x73

Table 72. DIMM Vendor Region Password Upper Byte

Address: 0x38 **Description:** DIMM Vendor Region Password Upper Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0	0x38 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (0x40 - R6F) Password - Upper Byte [7:0] = 0x94

Table 73. DIMM Vendor Password Control

Address: 0x39 **Description:** DIMM Vendor Password Control			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0	Host Region Codes: 0x74: Clear Registers 0x04 to 0x07, Erase MTP memory for 0x04 Register. DIMM Vendor Region (0x40 to 0x6F) Write Codes: 0x00: Lock DIMM Vendor Region. 0x40: Unlock DIMM Vendor Region. Password needs to be present in 0x37 & 0x38 registers. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in 0x37 & 0x38. 0x81: Burn DIMM Vendor Region - 0x40 to 0x4F 0x82: Burn DIMM Vendor Region - 0x50 to 0x5F 0x85: Burn DIMM Vendor Region - 0x60 to R6F DIMM Vendor Region (0x40 to 0x6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

Table 74. Default Address Pointer

Address: 0x3A **Description:** Default Address Pointer			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	0x3A [7]: Reserved
6	RW	0	0x3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host) 1 = Enable Default Address Pointer; Address selected by register bits [5:4]
5:4	RW	0	0x3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation 00 = 0x08 01 = 0x0C 10 = Reserved 11 = Reserved
3:2	RW	0	0x3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode 00 = 2 Bytes 01 = 4 Bytes 10 = Reserved 11 = 16 Bytes
1:0	RV	0	0x3A [1:0]: Reserved

Table 75. Revision ID

Address: 0x3B **Description:** Revision ID			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	0x3B [7:6]: Reserved
5:4	ROE	--	0x3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	--	0x3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved.
0	RV	--	0x3B [0]: Reserved

Table 76. Vendor ID Byte 0

Address: 0x3C **Description:** Vendor ID Byte 0			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001010	0x3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0.

Table 77. Vendor ID Byte 1

Address: 0x3D **Description:** Vendor ID Byte 1			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	10001100	0x3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1.

Table 78. Reserved 0x3E

Address: 0x3E **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x3E [7:0]: Reserved

Table 79. Reserved 0x3F

Address: 0x3F **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x3F [7:0]: Reserved

DIMM Vendor Region Registers

Table 80. Power-On Sequence Configuration 0

Address: 0x40 **Description:** Power-On Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	0x40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power-On Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	0	0x40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	0x40 [5]: Reserved
4	RWPE	0	0x40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	1	0x40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	0x40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power-On Sequence Config0 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

Table 81. Power-On Sequence Configuration 1

Address: 0x41 **Description:** Power-On Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	0x41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power-On Sequence Config 1 0 = Do Not Execute Config 1 1 = Execute Command 1
6	RWPE	1	0x41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	0x41 [5]: Reserved
4	RWPE	1	0x41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	1	0x41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	0x41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power-On Sequence Config1 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

Table 82. Power-On Sequence Configuration 2

Address: 0x42 **Description:** Power-On Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	0x42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power-On Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	0x42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	0x42 [5]: Reserved
4	RWPE	0	0x42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	0	0x42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	000	0x42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power-On Sequence Config2 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

Table 83. Reserved 0x43

Address: 0x43 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x43 [7:0]: Reserved

Table 84. Reserved 0x44

Address: 0x44 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x44 [7:0]: Reserved

Table 85. DIMM SWA Voltage Setting

Address: 0x45 **Description:** DIMM SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	0x45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	0x45 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register 0x45” [7:1] 1 = –7.5% from the setting in “Register 0x45” [7:1]

RTQ5132GQWF-XX0: 0x45[7:1] = 0111100 for SWA_VOLTAGE_SETTING = 1.1V
RTQ5132GQWF-XX2: 0x45[7:1] = 0111011 for LPCAMM2 SWA_VOLTAGE_SETTING = 1.05V

Table 86. DIMM SWA Threshold & Soft-stop Time

Address: 0x46 **Description:** DIMM SWA Threshold & Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	0x46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register 0x45” [7:1] 01 = +7.5% from the setting in “Register 0x45” [7:1] 10 = +10% from the setting in “Register 0x45” [7:1] 11 = +2.5% from the setting in “Register 0x45” [7:1]
5:4	RWPE	10	0x46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Overvoltage Status 00 = +7.5% from the setting in “Register 0x45” [7:1] 01 = +10% from the setting in “Register 0x45” [7:1] 10 = +12.5% from the setting in “Register 0x45” [7:1] 11 = +5% from the setting in “Register 0x45” [7:1]
3:2	RWPE	00	0x46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register 0x45” [7:1] 01 = –12.5% from the setting in “Register 0x45” [7:1] 10 = –5% from the setting in “Register 0x45” [7:1] 11 = –7.5% from the setting in “Register 0x45” [7:1]
1:0	RWPE	11	0x46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 87. Reserved 0x47

Address: 0x47 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x47 [7:0]: Reserved

Table 88. Reserved 0x48

Address: 0x48 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x48[7:0]: Reserved

Table 89. DIMM SWB Voltage Setting

Address: 0x49 **Description:** DIMM SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	0x49 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	0x49 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register 0x49” [7:1] 1 = –7.5% from the setting in “Register 0x49” [7:1]

Table 90. DIMM SWB Threshold, Soft-stop Time

Address: 0x4A **Description:** DIMM SWB Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	0x4A [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register 0x49” [7:1] 01 = +7.5% from the setting in “Register 0x49” [7:1] 10 = +10% from the setting in “Register 0x49” [7:1] 11 = +2.5% from the setting in “Register 0x49” [7:1]
5:4	RWPE	10	0x4A [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold for Overvoltage Status 00 = +7.5% from the setting in “Register 0x49” [7:1] 01 = +10% from the setting in “Register 0x49” [7:1] 10 = +12.5% from the setting in “Register 0x49” [7:1] 11 = +5% from the setting in “Register 0x49” [7:1]
3:2	RWPE	00	0x4A [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register 0x49” [7:1] 01 = –12.5% from the setting in “Register 0x49” [7:1] 10 = –5% from the setting in “Register 0x49” [7:1] 11 = –7.5% from the setting in “Register 0x49” [7:1]
1:0	RWPE	11	0x4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

Table 91. DIMM SWC Voltage Setting

Address: 0x4B **Description:** DIMM SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	0x4B [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting2 000 0000 = 1500mV 000 0001 = 1505mV 000 0010 = 1510mV ... 011 1100 = 1800mV ... 111 1101 = 2125mV 111 1110 = 2130mV 111 1111 = 2135mV
0	RWPE	0	0x4B [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = –5% from the setting in “Register 0x4B” [7:1] 1 = –7.5% from the setting in “Register 0x4B” [7:1]

Table 92. DIMM SWC Threshold, Soft-stop Time

Address: 0x4C **Description:** DIMM SWC Threshold, Soft-stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	0x4C [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register 0x4B” [7:1] 01 = +7.5% from the setting in “Register 0x4B” [7:1] 10 = +10% from the setting in “Register 0x4B” [7:1] 11 = +2.5% from the setting in “Register 0x4B” [7:1]
5:4	RWPE	10	0x4C [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Overvoltage Status 00 =+7.5% from the setting in “Register 0x4B” [7:1] 01 = +10% from the setting in “Register 0x4B” [7:1] 10 = +12.5% from the setting in “Register 0x4B” [7:1] 11 = +5% from the setting in “Register 0x4B” [7:1]
3:2	RWPE	00	0x4C [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Undervoltage Lockout Status 00 = –10% from the setting in “Register 0x4B” [7:1] 01 = –12.5% from the setting in “Register 0x4B” [7:1] 10 = –5% from the setting in “Register 0x4B” [7:1] 11 = –7.5% from the setting in “Register 0x4B” [7:1]
1:0	RWPE	11	0x4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

Table 93. DIMM FSW & Mode_1

Address: 0x4D **Description:** DIMM FSW & Mode_1			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	0x4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	0x4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:0	RWPE	00	0x4D [3:2]: Reserved

Table 94. DIMM FSW & Mode_2

Address: 0x4E **Description:** DIMM FSW & Mode_2			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	0x4E [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	0x4E [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RWPE	10	0x4E [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	0x4E [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

Table 95. Reserved 0x4F

Address: 0x4F **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:1	RV	0	Reserved
0	RWPE	0	0x4F [0]: SWA_SWB_PHASE_MODE_SELECT Switch Node A and Switch Node B Phase Regulator Mode Selection 0 = Single Phase Regulator Mode 1 = Dual Phase Regulator Mode

RTQ5132GQWF-X2X: 0x4F[0] = 1; RTQ5132GQWF-X1X: R4F[0] = 0

Table 96. DIMM OC Threshold

Address: 0x50 **Description:** DIMM OC Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	11	0x50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node A Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 3.0A 01 = 3.5A 10 = 4.0A 11 = 4.5A
5:4	RWPE	0	0x50 [5:4]: Reserved
3:2	RWPE	11	0x50 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node B Output Current Limiter Warning Threshold Setting1 For COT Mode, Ivalley_limit: 00 = 3.0A 01 = 3.5A 10 = 4.0A 11 = 4.5A
1:0	RWPE	11	0x50 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node C Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 0.5A 01 = 1.0A 10 = 1.5A 11 = 2.0A

Table 97. DIMM Buck & LDO Output Voltage Range

Address: 0x51 **Description:** DIMM Buck & LDO Output Voltage Range			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	0x51 [7:6]: VLDO_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting1 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	0	0x51 [5:3]: Reserved
2:1	RWPE	01	0x51 [2:1]: VLDO_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	0x51 [0]: Reserved

Table 98. Reserved 0x52-0x57

Address: 0x52 – 0x57 **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x52 [7:0] – 0x57 [7:0]: Reserved

Table 99. Power-Off Sequence Configuration 0

Address: 0x58 **Description:** Power-Off Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	0x58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power-off sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	1	0x58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	0x58 [5]: Reserved
4	RWPE	1	0x58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Enable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	0x58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	0x58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power-off sequence Config0 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

Table 100. Power-Off Sequence Configuration 1

Address: 0x59 **Description:** Power-Off Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	0x59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power-off sequence Config1 0 = Do Not Execute Config1 1 = Execute Config1
6	RWPE	1	0x59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	0x59 [5]: Reserved
4	RWPE	1	0x59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	1	0x59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	0x59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power-off sequence Config1 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

Table 101. Power-Off Sequence Configuration 2

Address: 0x5A **Description:** Power-Off Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	0x5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power-off sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	0x5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	0x5A [5]: Reserved
4	RWPE	0	0x5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	0x5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	0x5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power-off sequence Config2 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

Table 102. Reserved 0x5B

Address: 0x5B **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x5B [7:0]: Reserved

Table 103. Reserved 0x5C

Address: 0x5C **Description:** Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	0x5C [7:0]: Reserved

Table 104. DIMM Soft-start Time_1

Address: 0x5D **Description:** DIMM Soft-start Time_1			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	0x5D [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4:0	RV	0	0x5D [4:0]: Reserved

Table 105. DIMM Soft-start Time_1

Address: 0x5E **Description:** DIMM Soft-start Time_2			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	0x5E [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	0x5E [4]: Reserved
3:1	RWPE	001	0x5E [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	0x5E [0]: Reserved

17.5 Recommended Component Selection for Typical Application Circuit

Suggested Component for SWA and SWB

Component	Value	Physical Size	Part No.
L1, L2	0.47μH	3.2 x 2.5 x 1.2	HTTD32251BR47MMR/GLVQMR4701A
L1, L2	0.68μH	3.2 x 2.5 x 1.2	HTTD32251BR68MMR/GLVQMR6801A
C_{BYPx}	0.1μF	10V; 0201	GRM033C81E104KE14
C_{INx}	22μF (x2)	10V; 0603	GRM188R61A226ME15
C_{OUTx}	47μF (x2)	6.3V; 0603	GRM188R60J476ME01

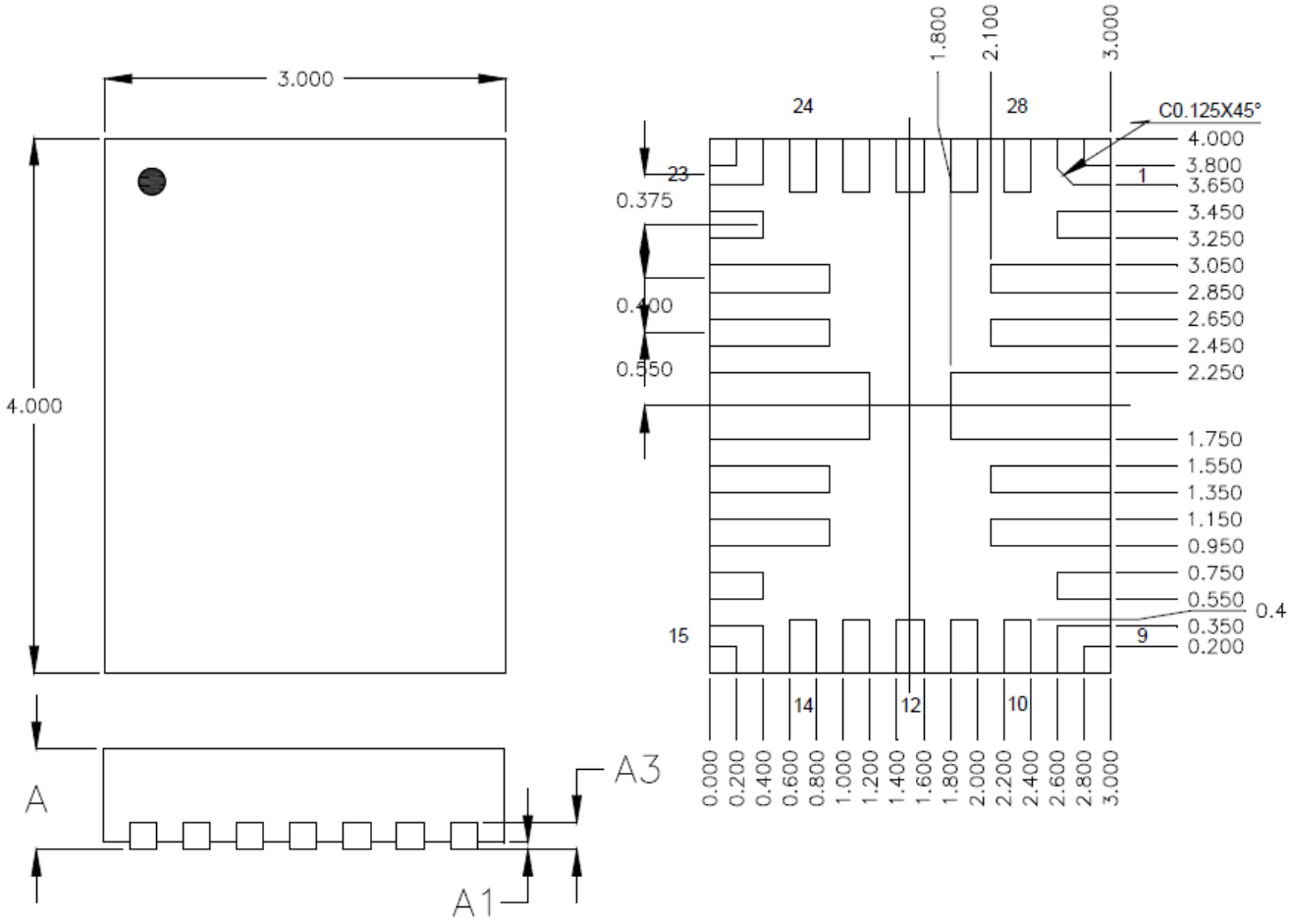
Suggested Component for SWC

Component	Value	Physical Size	Part No.
L3	1.0μH	2.5 x 2.0 x 1.2	HTTD25201B1R0MSR/GLULM1R001A/DFE252012P-1R0M
L3	1.5μH	2.5 x 2.0 x 1.2	HTTD25201B1R5MSR/GLULM1R501A/MEMK2520D1R5ML
C_{BYPC}	0.1μF	10V; 0201	GRM033C81E104KE14
C_{INC}	22μF (x2)	10V; 0603	GRM188R61A226ME15
C_{OUTC}	47μF (x2)	6.3V; 0603	GRM188R60J476ME01

Suggested Component for VLDO_1.8V and VLDO_1.0V

Component	Value	Physical Size	Part No.
C_{BYP}	0.1μF	10V; 0201	GRM033C81E104KE14
C_{IN}	4.7μF	10V; 0402	GRM155R61A475MEAA
$C_{LDO\_1.8V}$	4.7μF	6.3V; 0402	GRM155R60J475ME47
$C_{LDO\_1.0V}$	4.7μF	6.3V; 0402	GRM155R60J475ME47

18 Outline Dimension

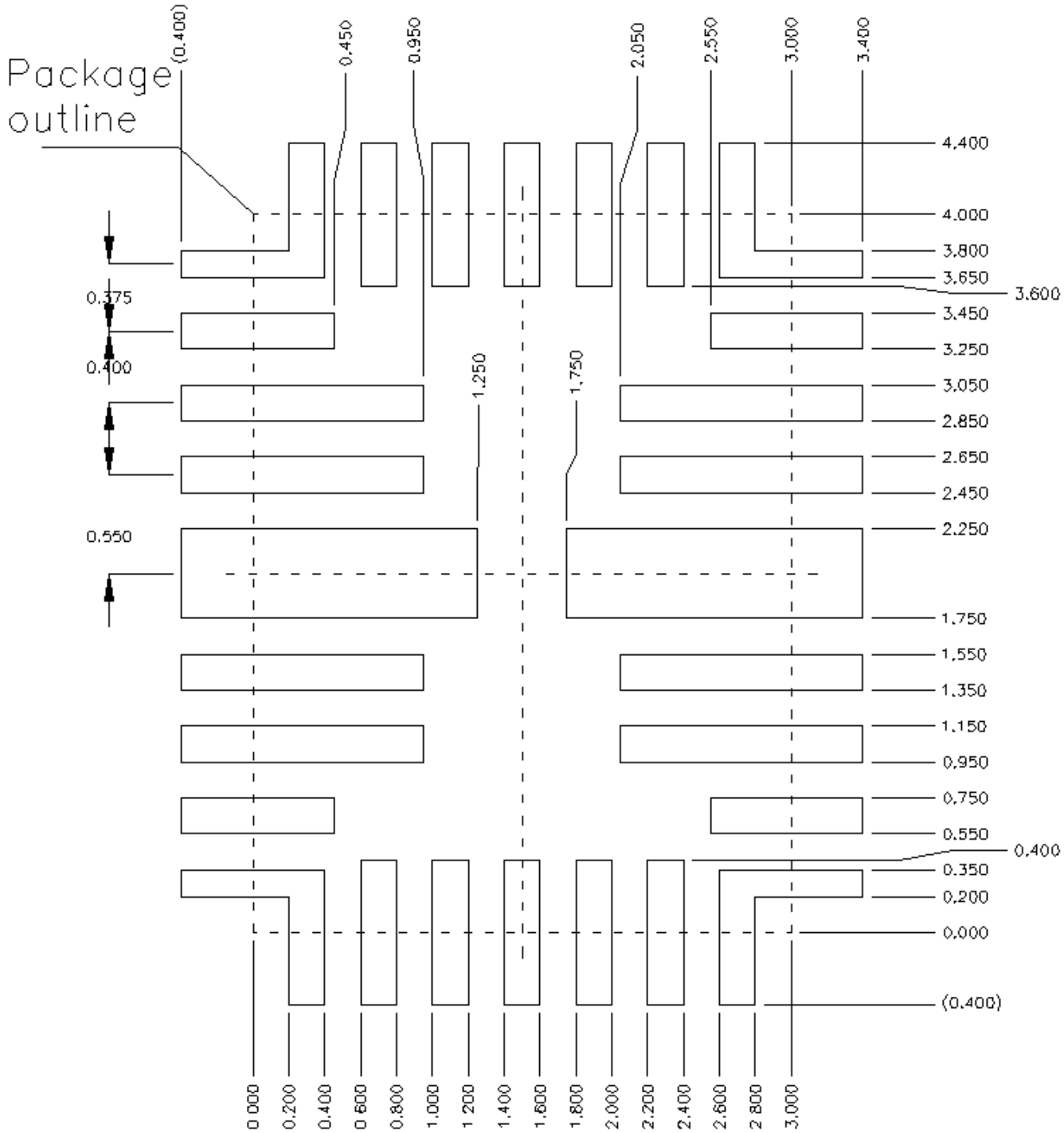


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 28L QFN 3x4 (FC) Package

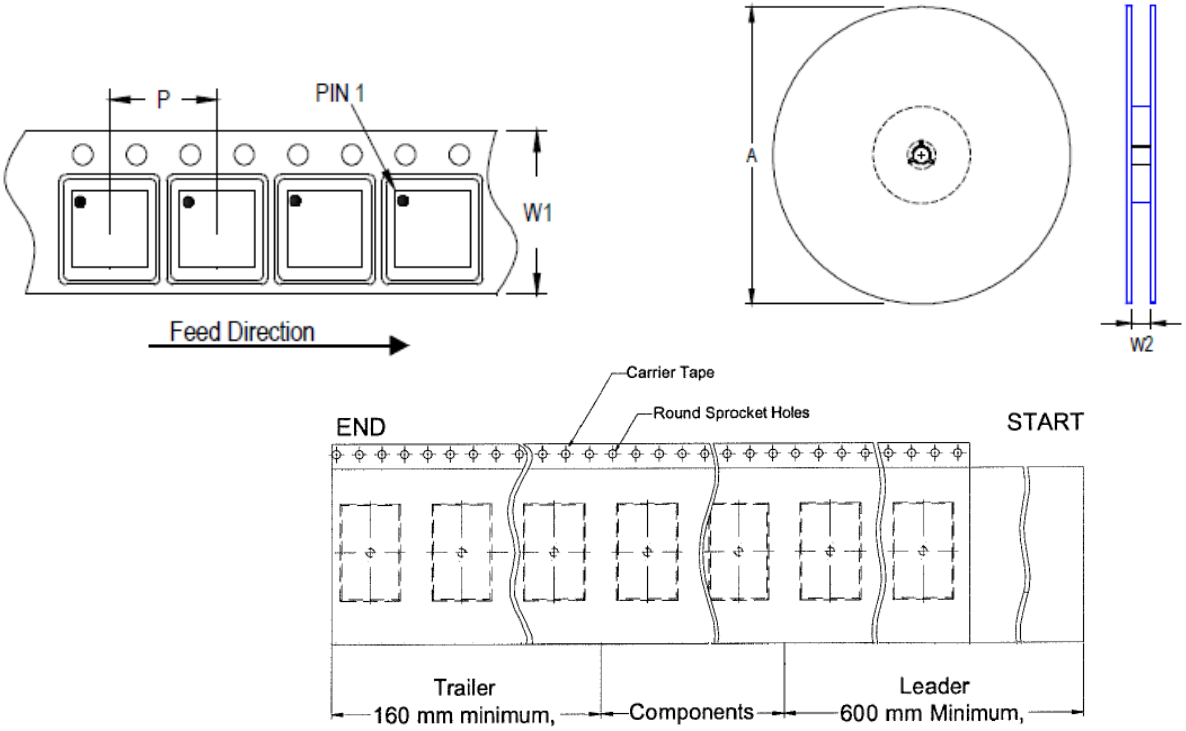
19 Footprint Information



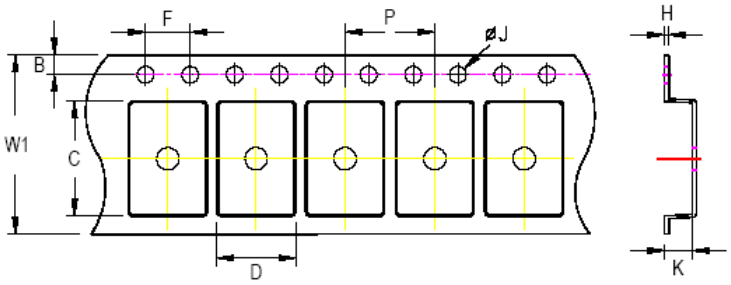
Package	Number of Pin	Tolerance
V/W/U/XQFN3x4-28(FC)	28	±0.05

20 Packing Information

20.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
05	2022/12/19	Modify	*Electrical Characteristics on page 1* *Application Information on page 52*
06	2023/9/14	Modify	*Ordering Information on page 1* *General Description on page 1* *Simplified Application Circuit on page 2* *Electrical Characteristics page 40* *Note 2 on page 42* *Typical Application Circuit on page 44* *Application Information on page 60, 61, 67*
07	2024/7/4	Modify	*General Description on page 1* *Ordering Information on page 1* *Features on page 1* *Functional Pin Description on page 4, 5* *Absolute Maximum Ratings on page 7* *Recommended Operating Conditions on page 7* *Electrical Characteristics page 8 to 13* *Operation page 23 to 49* *Application Information on page 54 to 60* *Functional Register Description on page 66 to 117*