12A, 17V, ACOT® High-Efficiency Synchronous Step-Down Converter

1 General Description

The RTQ2812A is a high-performance, synchronous step-down converter that can deliver up to 12A output current with a wide input supply voltage range of 3.5V to 17V. The device integrates low $R_{DS(ON)}$ power MOSFETs, an accurate 0.6V ± 1% reference over the full operating junction temperature range, and an integrated diode for the bootstrap circuit, offering a very compact solution.

The RTQ2812A adopts Advanced Constant-On-Time (ACOT®) control architecture that provides excellent transient performance and reduces the count of external components. In steady states, the ACOT® can operate at nearly constant switching frequency over line, load and output voltage ranges, making the EMI filter design easier.

The device offers a variety of functions to provide more design flexibility. The selectable switching frequency, current limit level, PWM operation modes make the RTQ2812A easy-to-use over wide application range. An independent enable control input pin and power-good indicator are also provided for easy sequence control. The device provides a programmable soft-start-up by an external capacitor connected to the SS/TR pin to control the inrush current during start-up

The RTQ2812A provides complete protection functions including input undervoltage lockout, output undervoltage protection, output overvoltage protection, overcurrent protection, and thermal shutdown. The RTQ2812A is available in a thermally enhanced WQFN-21TL 3x4 (FC) package.

The recommended junction temperature range is –40°C to 150°C.

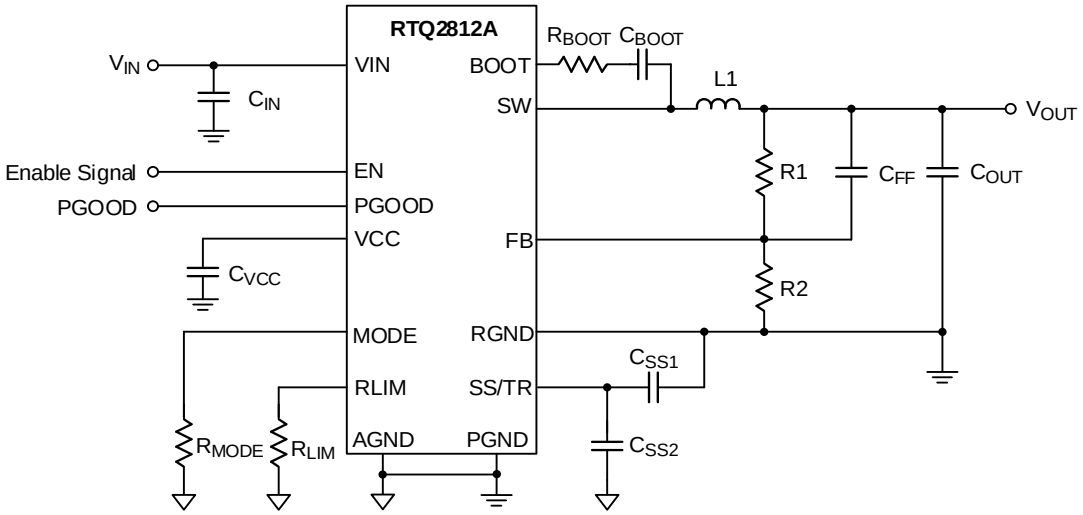
2 Features

- **Wide Input Voltage Range**
  - **2.7V to 17V with External 3.3V VCC Bias**
  - **3.5V to 17V with Internal VCC Bias**
- **Output Voltage from 0.6V to 5.5V**
- **0.6V ± 0.5% Voltage Reference from 0°C to 70°C Junction Temperature Range**
- **0.6V ± 1% Voltage Reference from –40°C to 150°C Junction Temperature Range**
- **ACOT® Control for Excellent Transient Performance**
- **Stable with Ceramic Output Capacitors**
- **Selectable FCCM or PSM Operation at Light Load**
- **Selectable Operation Switching Frequency (600KHz/800KHz/1MHz)**
- **Non-Latch for OCP, UVP, UVLO, and OTP Faults, Latch Off for OVP**
- **Differential Remote Sense Voltage for High Output Accuracy**
- **Power-Good Indicator**
- **Enable Control**
- **Programmable Soft-Start Time with a Default 1ms**
- **Programmable Valley Current Limit Level**
- **Monotonic Start-Up into Pre-Biased Outputs**
- **Output Voltage Tracking**
- **Small 21T-Lead WQFN (3x4) (FC) Package**

3 Applications

- Servers, Storage and Network Equipment
- Telecom Infrastructure
- Point of Load (POL) Power Modules
- High Density DC-DC Converters

4 Simplified Application Circuit



5 Ordering Information

RTQ2812A □□

Package Type
QWF : WQFN-21TL 3x4 (FC) (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant (1)

Note 1.

Marked with (1) indicated: Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

0T=: Product Code
YMDAN: Date Code

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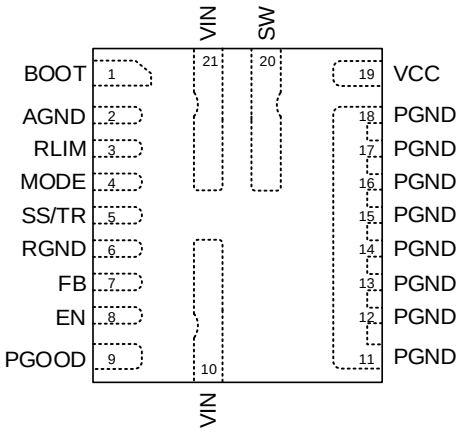
7 Pin Configuration

(TOP VIEW)



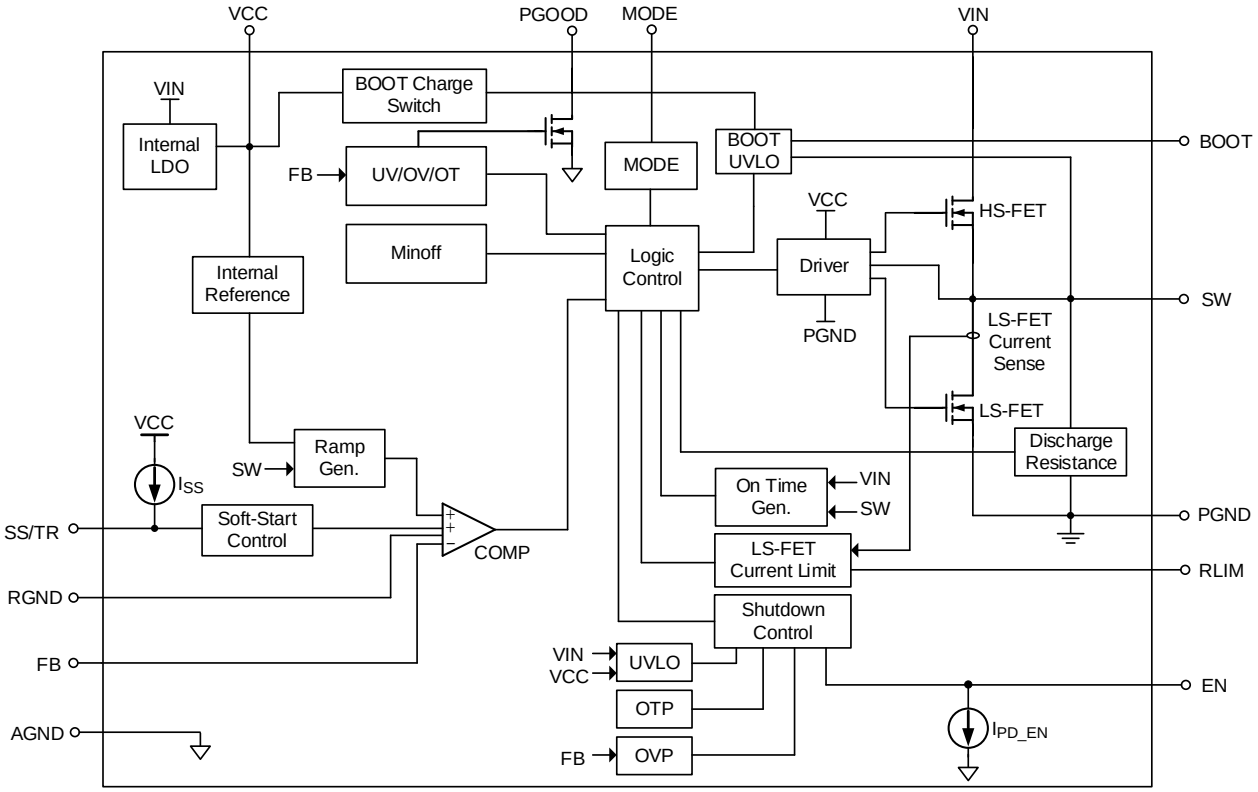
WQFN-21TL 3x4 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.
2	AGND	Analog ground. Reference point for the internal control circuit. Connect AGND and PGND with a short trace and at only one point to reduce circulating currents.
3	RLIM	Valley current limit setup pin. Connect a resistor from this pin to AGND to set the valley current limit value. At least ±1% resistor is required.
4	MODE	Mode selection setup pin. The mode pin can be set to force continuous-conduction mode (FCCM) or pulse skipping mode (PSM) for high light-load efficiency, and the operation switching frequency. At least ±1% resistor is required.
5	SS/TR	Soft-start and tracking control input. Connect a ceramic capacitor from this pin to RGND to program the soft-start time. The internal minimum start-up time is 1 ms (typ.). A minimum capacitor of 22nF on this pin is required for smooth charging. For the tracking function, the device can track the pin voltage as the reference for tracking applications because the SS/TR pin voltage can override the internal V_{REF}.
6	RGND	Differential remote voltage sense. Connect this pin to the negative side of the remote voltage sense point. Short to GND as internal reference if the remote voltage sense is not used.
7	FB	Feedback voltage input. The pin is used to set the converter's output voltage via a resistor divider. It is suggested to place the feedback resistor divider as close to the FB pin as possible.
8	EN	Enable control input. A logic-high enables the converter; however, a logic-low forces the device into shutdown mode. Do not leave this pin floating.

Pin No.	Pin Name	Pin Function
9	PGOOD	Open-drain, power-good indication output. It is pulled low if the feedback voltage is out of the PGOOD threshold, IC shuts down from fault state and EN goes low, and before the soft-start is finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
10, 21	VIN	Power input voltage. Support 3.5V to 17V input voltage. It is suggested to place decoupling input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
11, 12, 13 14, 15, 16, 17, 18	PGND	The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces to make the connections.
19	VCC	3V internal LDO output. An external DC voltage source 3.3V±5% can be connected to this pin for less power losses on the internal LDO and supply both the internal circuitry and gate driver. Connect a 1μF, X7R ceramic capacitor as close to the VCC pin as possible. It is not recommended to connect VCC to supply other rails.
20	SW	Switch node. Output switching state between high-side MOSFET switching and low-side MOSFET switching of the power converter. Connect SW pin to the external inductor and bootstrap capacitor.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN Voltage, V_{IN} ---------- –0.3V to 18V
- Enable Pin Voltage, V_{EN} ---------- –0.3V to 18V
- VIN to SW ---------- –0.3V to 18V

  V_{IN} to V_{SW} ($t \leq 25ns$) ---------- –4V to 25V
- SW Voltage, V_{SW} ---------- –0.3V to 18V

  V_{SW} ($t \leq 25ns$) ---------- –5V to 25V
- BOOT Voltage, V_{BOOT} ---------- –0.3V to 24V
- BOOT to SW Voltage (V_{BOOT}-V_{SW}) ---------- –0.3V to 6V
- VCC ---------- 6V
- All Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 170°C
- Storage Temperature Range ---------- –65°C to 170°C

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model), All Other pins ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- VIN with Internal VCC Bias, V_{IN} ---------- 3.5V to 17V
- VIN with External 3.3V VCC Bias, V_{IN} ---------- 2.7V to 17V
- Output Voltage ---------- 0.6V to 5.5V
- External VCC bias, V_{CC_EXT} ---------- 3.12V to 3.6V
- Enable voltage, V_{EN} ---------- 3.6V
- Junction Temperature Range ---------- –40°C to 150°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal parameter		WQFN 21TL 3x4	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	50.7	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	26.9	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	1.47	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	23.52	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.75	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 80mm x85mm; furthermore, all layers with 2 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 12V, T_J = –40°C to 150°C, typical values are at T_J = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	5	15	μA
Supply Current (non-switching)	I_{Q_NSW}	V_{EN} = 2V, non-switching	--	1150	1300	μA
Logic Threshold						
EN Input Voltage Rising Threshold	V_{EN_R}		1.17	1.22	1.27	V
EN Threshold Hysteresis	V_{EN_HYS}		--	200	--	mV
EN Pull-Down Current	I_{PD_EN}	V_{EN} = 2V	--	0.5	5	μA
Reference Voltage						
Internal Reference Voltage	V_{REF}	T_J = –40°C to +150°C	0.594	0.6	0.606	V
		T_J = 0°C to +70°C	0.597	0.6	0.603	V
Soft-Start and Tracking						
Internal Soft-Start Time	t_{SS}	T_J = 25°C, C_{SS} = 22nF, V_{OUT} is 0% to 100% (Note 7)	--	1	1.4	ms
SS/TR Charge Current	I_{SS/TR_CHG}	$V_{SS/TR}$ = 0V	--	42	--	μA
SS/TR Discharge Current	I_{SS/TR_DISCHG}	$V_{SS/TR}$ = 1V	--	12	--	μA
MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}	T_J = 25°C, V_{CC} = 3V	--	13.3	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	T_J = 25°C, V_{CC} = 3V	--	3.8	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
Current Limit Voltage Threshold	V_{LIM}	T_J = 25°C, valley current	--	1.2	--	V
I_{CS} to I_{OUT} Ratio	G_{CS} (I_{CS}/I_{OUT})	$I_{OUT} \geq$ 2A	--	20	--	μA/A
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	T_J = 25°C, valley current, R_{LIM} = 5kΩ	--	12	--	A
Low-Side MOSFET Negative Current-Limit Threshold	I_{LIM_NEG}	T_J = 25°C, valley current	--	−10	--	A
Switching Frequency						
Switching Frequency	f_{SW}	R_{MODE} = 0Ω, I_{OUT} = 0A, FCCM, V_{OUT} = 1V	480	600	720	kHz
		R_{MODE} = 30.1kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V	680	800	920	
		R_{MODE} = 60.4kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1V	850	1000	1150	
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	T_J = 25°C (Note 7)	--	--	50	ns
Minimum Off-Time	t_{OFF_MIN}	T_J = 25°C (Note 7)	--	--	210	ns
UVLO						
Input Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising, V_{CC_EXT} = 3.3V	2.1	2.4	2.7	V
Input Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} hysteresis	--	550	--	mV
LDO Output						
LDO Output Voltage	V_{CC}	I_{VCC} = 1mA	2.88	3.00	3.18	V
VCC Undervoltage Lockout Rising Threshold	$V_{CC\_UVLO\_R}$	V_{CC} rising	2.65	2.8	2.95	V
VCC Undervoltage Lockout Hysteresis	$V_{CC\_UVLO\_HYS}$	V_{CC} hysteresis	--	300	--	mV
VCC Load Regulation		I_{VCC} = 25mA	--	0.5	--	%
LDO Output Current Limit	I_{LIM_LDO}		--	105	--	mA
Output Overvoltage and Undervoltage Protections						
Output Undervoltage Protection Threshold	V_{UVP}	UVP detect	77	80	83	%V_{REF}
Output Overvoltage Protection Threshold	V_{OVP}	OVP detect	113	116	119	%V_{REF}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good						
Power-Good Voltage Threshold	V_{TH_PGLH1}	V_{FB} rising threshold, PGOOD from low to high (GOOD)	89.5	91.5	95.5	%V_{REF}
	V_{TH_PGHL1}	V_{FB} rising threshold, PGOOD from high to low (FAULT)	113	116	119	
	V_{TH_PGLH2}	V_{FB} falling threshold, PGOOD from low to high (GOOD)	102	106	109	
	V_{TH_PGHL2}	V_{FB} falling threshold, PGOOD from high to low (FAULT)	77	80	83	
Power-Good Output Low-Level Voltage	$V_{PG\_L\_100}$	T_J = 25°C, V_{IN} & V_{CC} & V_{EN} = 0V, PGOOD Pull up to 3.3V bias with 100k resister	--	650	850	mV
	$V_{PG\_L\_10}$	T_J = 25°C, V_{IN} & V_{CC} & V_{EN} = 0V, PGOOD Pull up to 3.3V bias with 10k resister	--	800	1000	mV
Power-Good Delay	t_{PGDLY_LH}	T_J = 25°C, V_{TH_PGLH1} and V_{TH_PGLH2}, PGOOD from low to high (GOOD)	0.5	0.8	1.1	ms
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	30	--	°C
Output Discharge Resistor						
Output Discharge Resistor	R_{DISCHG}	V_{EN} = 0V or Protection	--	80	150	Ω

Note 7. Guaranteed by design.

15 Typical Application Circuit

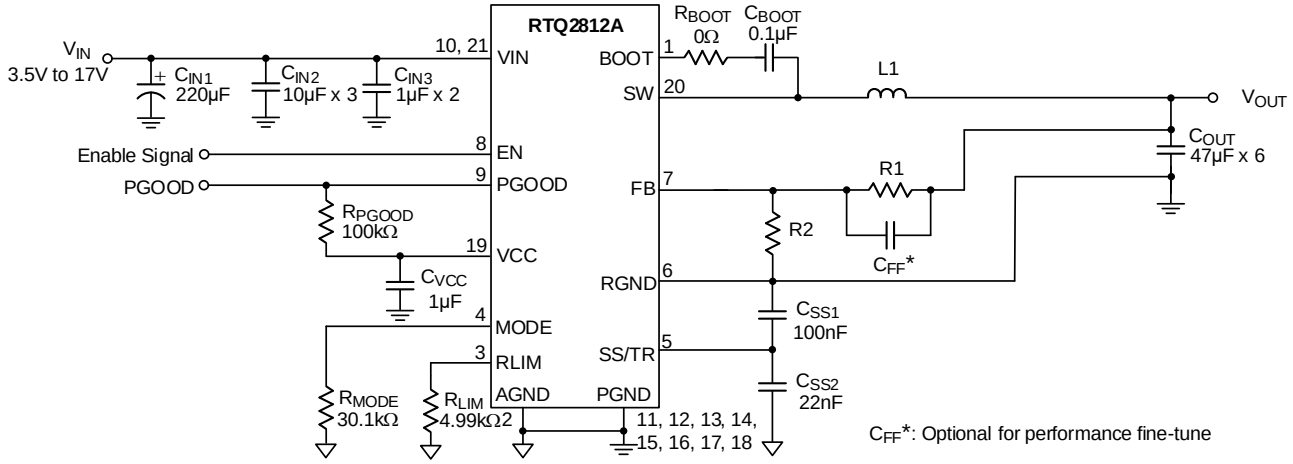


Table 1. Suggested Component Selection for the Application of 600kHz

VOUT(V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	COUT_MIN (µF)	COUT_TYPICAL (µF)	CFF (pF)
0.8	3.32	10	0.40	84	282	1000 to 2200
1.2	10		0.68	84	282	470 to 1000
3.3	45.3		1.2	84	282	220 to 470
5	73.2		1.5	84	282	150 to 330

Table 2. Suggested Component Selection for the Application of 800kHz

VOUT(V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	COUT_MIN (µF)	COUT_TYPICAL (µF)	CFF (pF)
0.8	3.32	10	0.33	84	282	1000 to 2200
1.2	10		0.47	84	282	470 to 1000
3.3	45.3		1	84	282	220 to 470
5	73.2		1.2	84	282	150 to 330

Table 3. Suggested Component Selection for the Application of 1000kHz

VOUT(V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)	COUT_MIN (µF)	COUT_TYPICAL (µF)	CFF (pF)
0.8	3.32	10	0.22	84	282	1000 to 2200
1.2	10		0.33	84	282	470 to 1000
3.3	45.3		0.68	84	282	220 to 470
5	73.2		1	84	282	150 to 330

Table 4. Suggested Inductors for Typical Application Circuit

Inductance (µH)	Part No.	ISAT (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.22	VLBU1007090T-R22L	57	0.18	10 x 7 x 9	TDK
0.33	VLBU1007090T-R33L	39	0.18	10 x 7 x 9	TDK
0.4	VLBU1007090T-R40L	30	0.18	10 x 7 x 9	TDK

Inductance (µH)	Part No.	ISAT (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.47	744314047	20	1.35	6.9 x 6.9 x 4.8	WE
0.68	744393580068	52.2	1.41	8.8 x 8.3 x 7.8	WE
1	74439358010	38.15	2.1	8.8 x8.3 x 7.8	WE
1.2	744325120	25	1.8	10.2 x 12.1 x 4.7	WE
1.5	744393580150	32	2.91	8.8 x8.3 x 7.8	WE

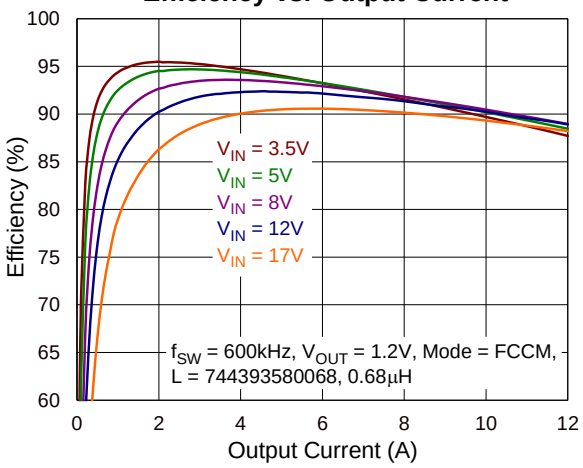
Table 2. Suggested Capacitors for Typical Application Circuit

Capacitance (µF)	Part No.	Case Size	Component Supplier
220	250ARHA221M08A2	8 mm x 11.5mm	APAQ
10	GRM31CR71E106KA12L	1206	Murata
47	GRM31CR60J476ME19	1206	Murata
1	GRM155C81E105KE11D	0402	Murata

Note: (1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

16 Typical Operating Characteristics

Efficiency vs. Output Current



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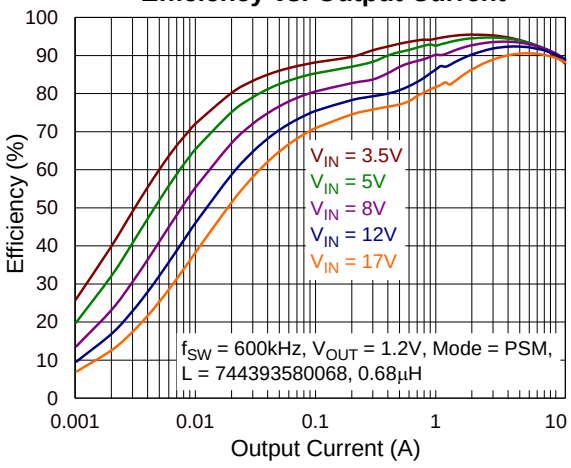

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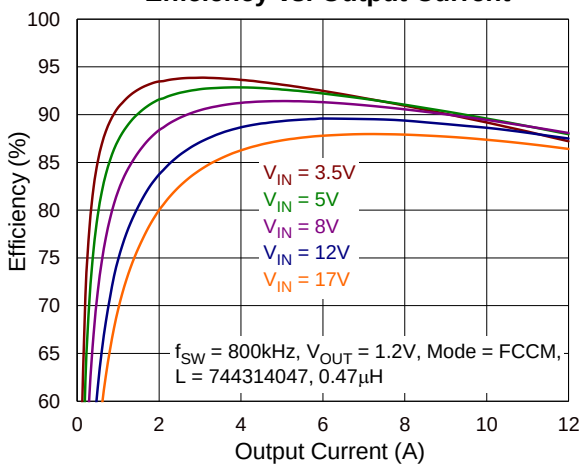

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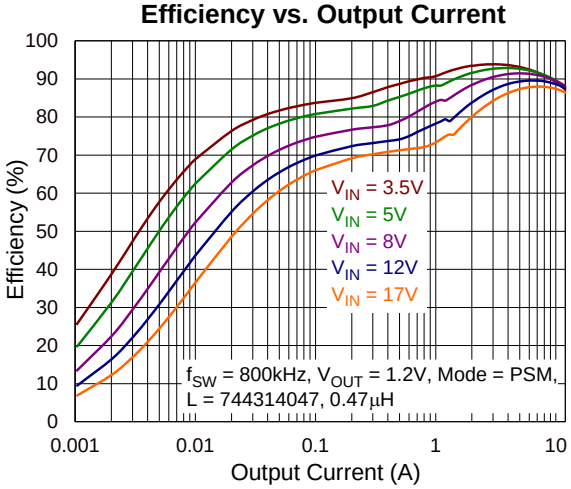

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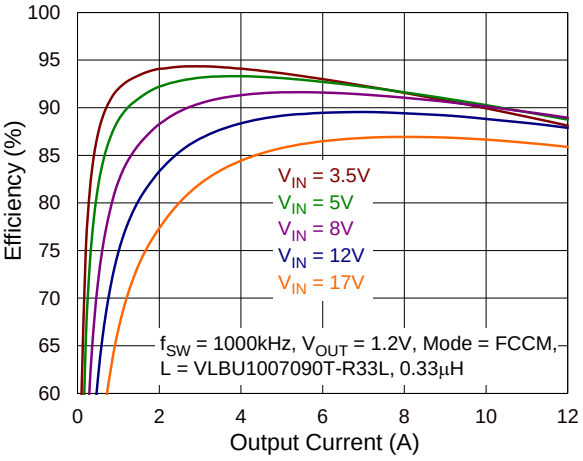

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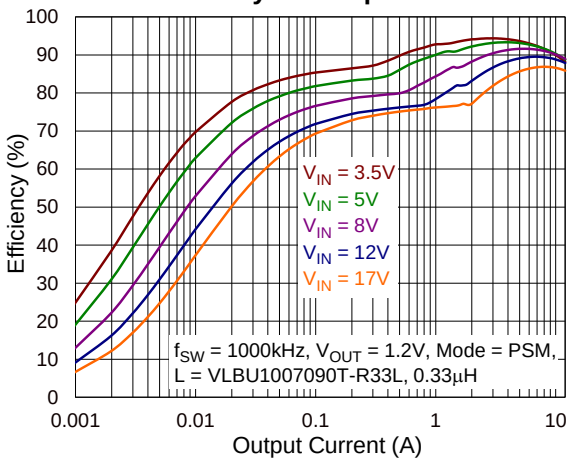

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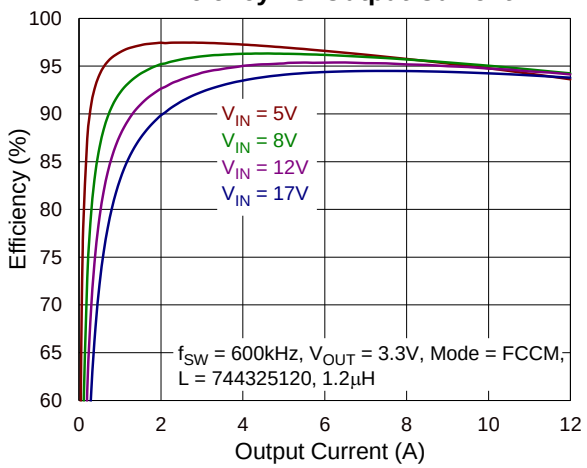

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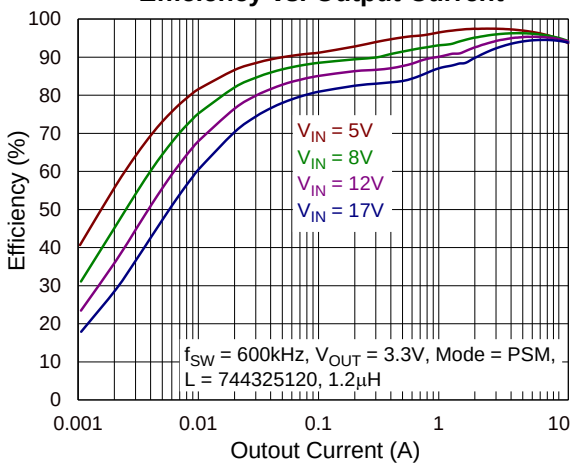

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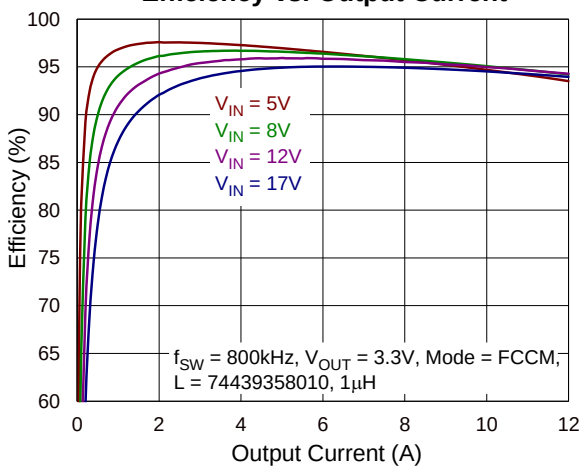

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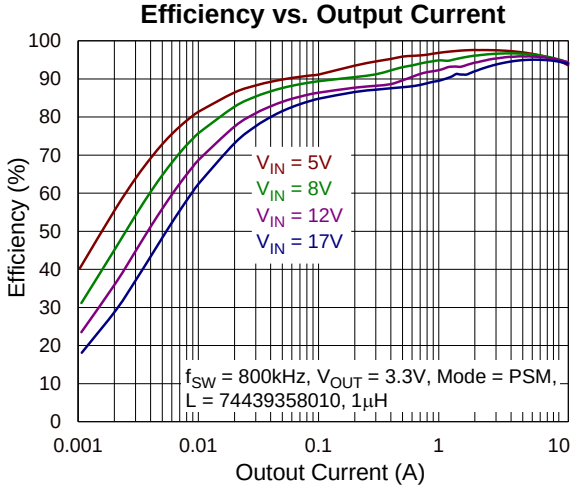

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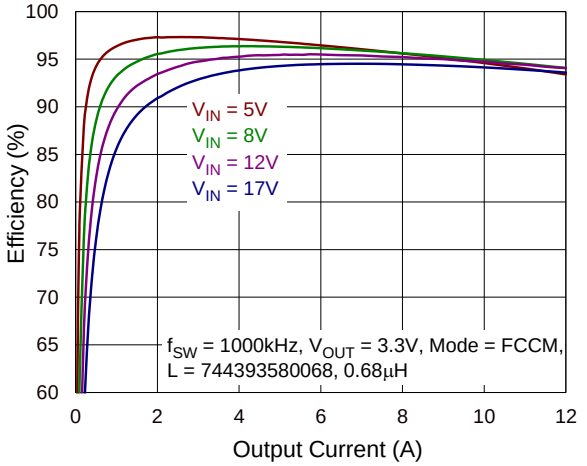

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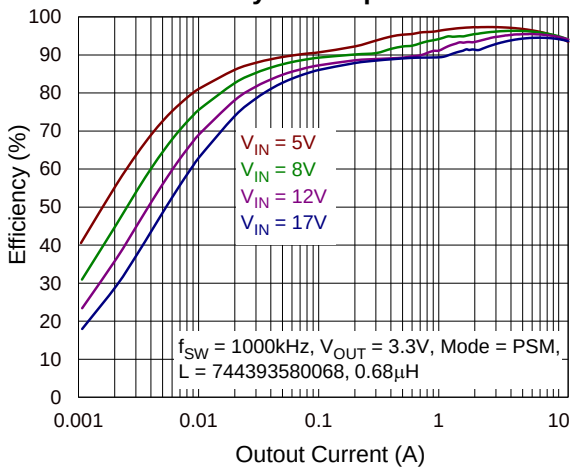

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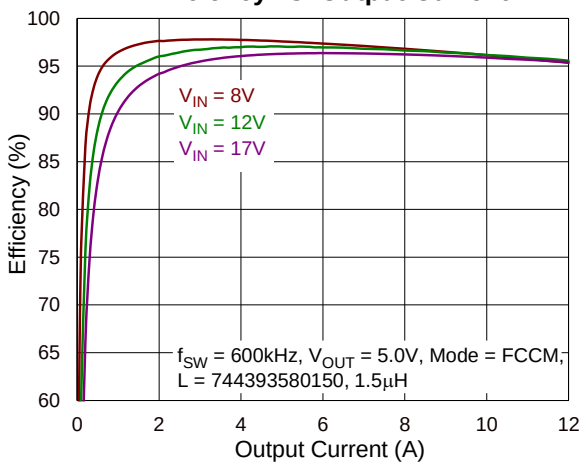

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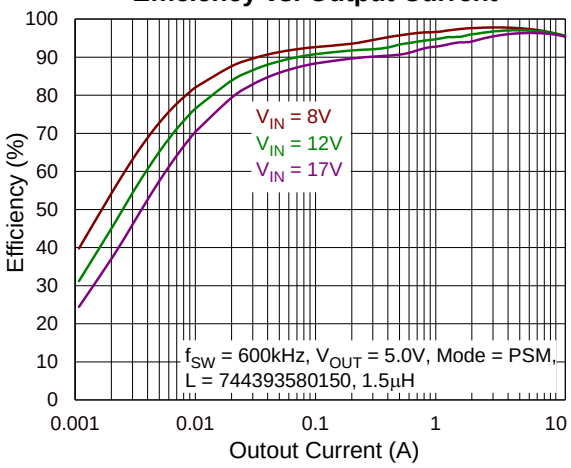

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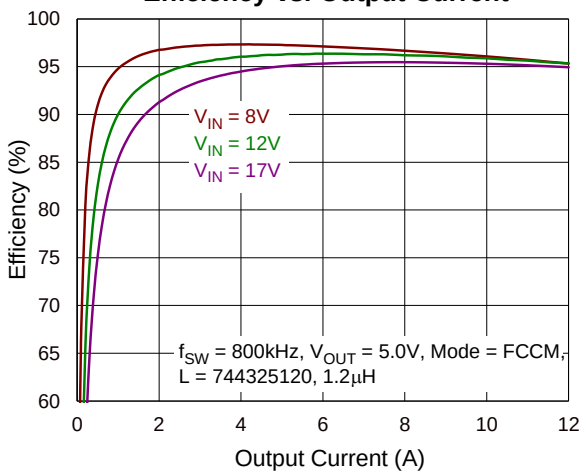

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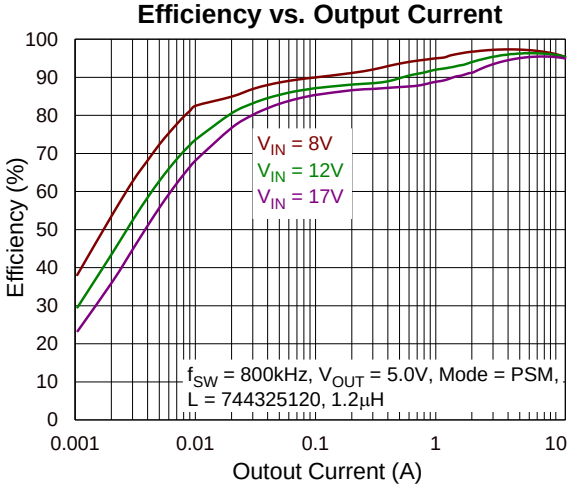

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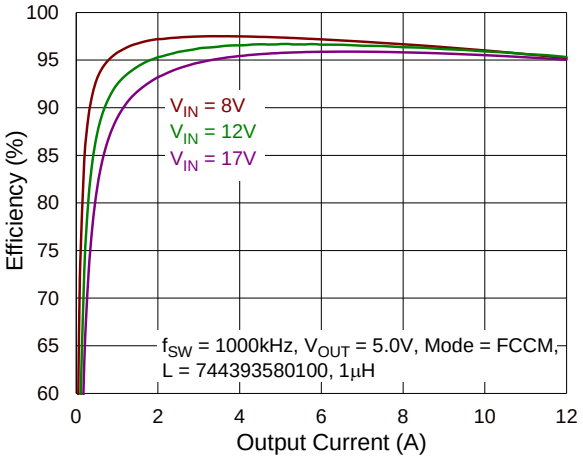
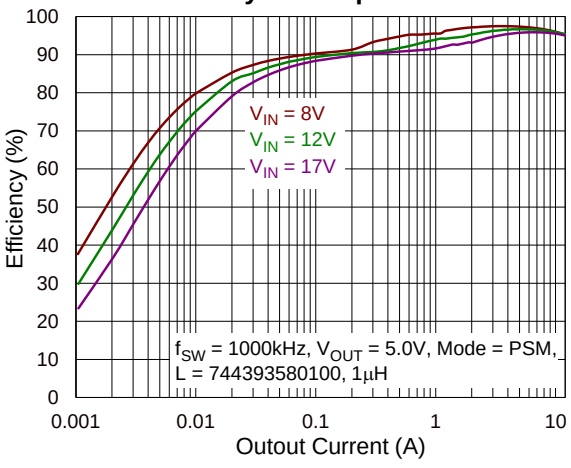
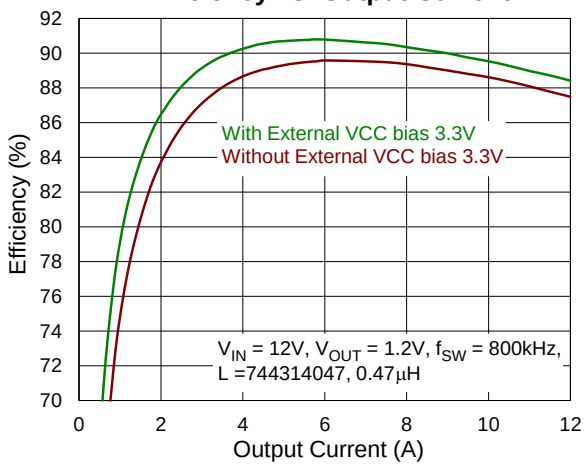


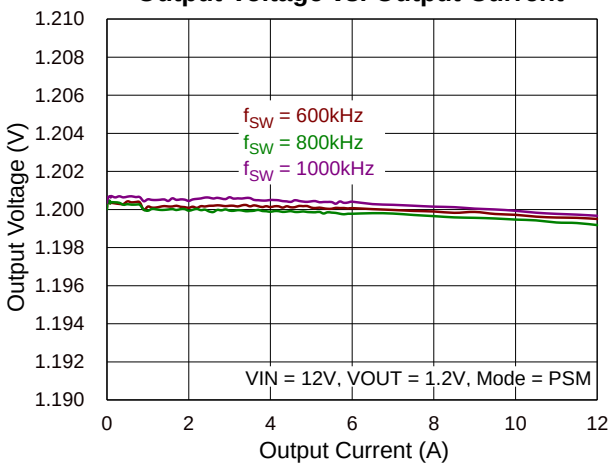
Efficiency vs. Output Current



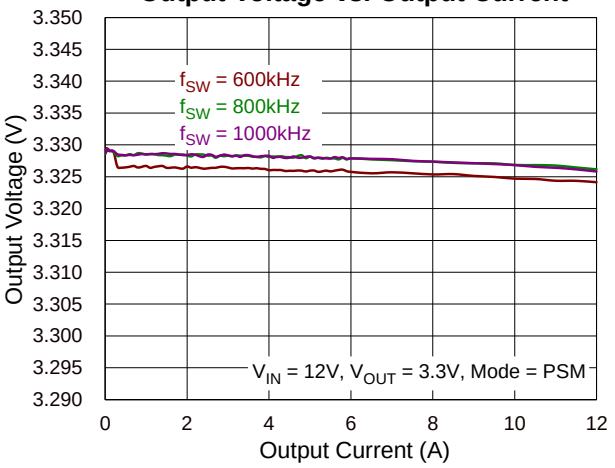
Efficiency vs. Output Current



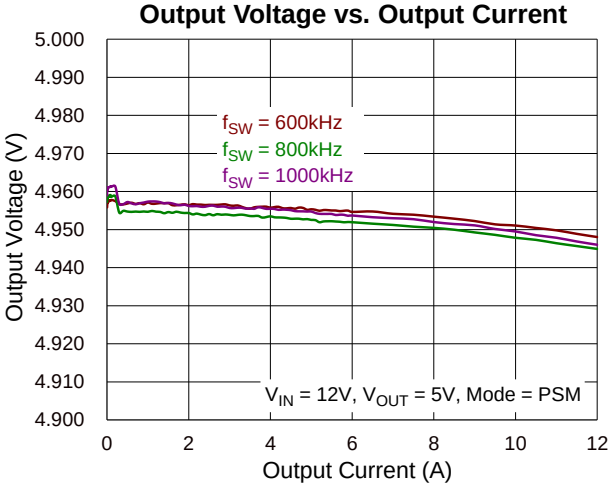
Output Voltage vs. Output Current



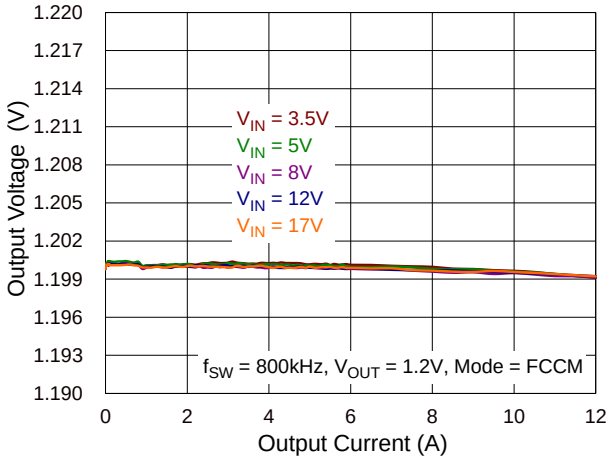
Output Voltage vs. Output Current



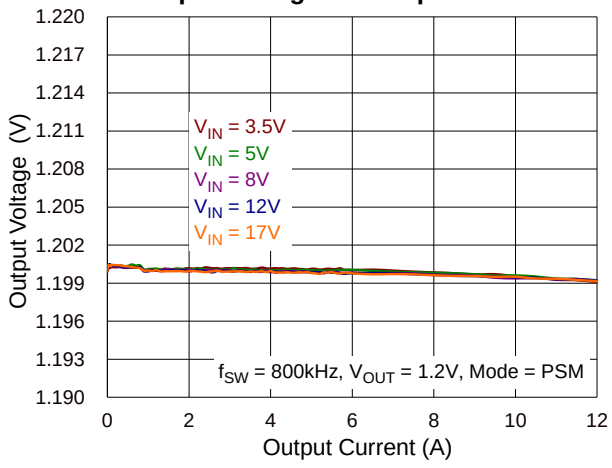
Output Voltage vs. Output Current

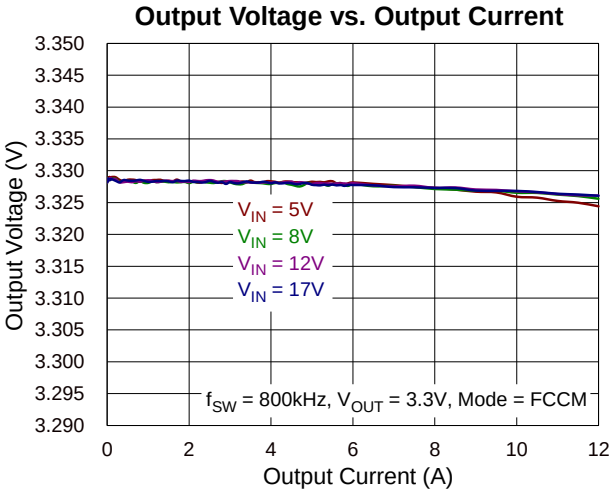


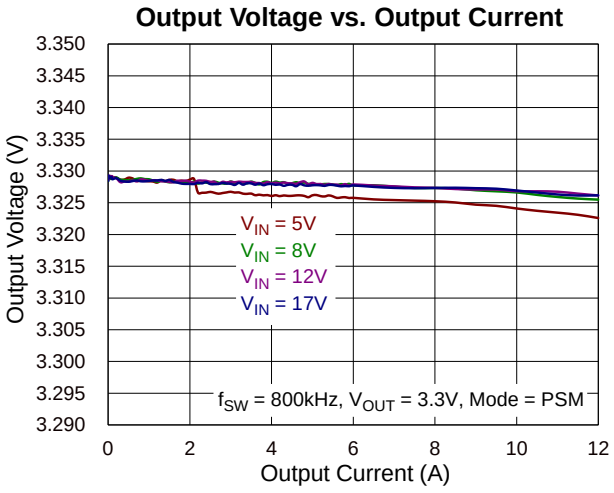
Output Voltage vs. Output Current

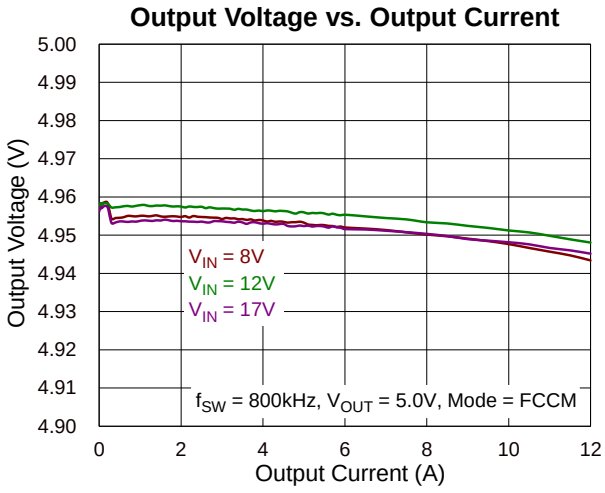


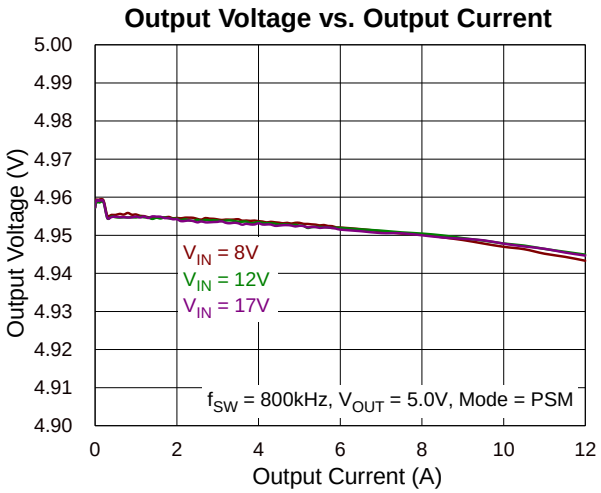
Output Voltage vs. Output Current

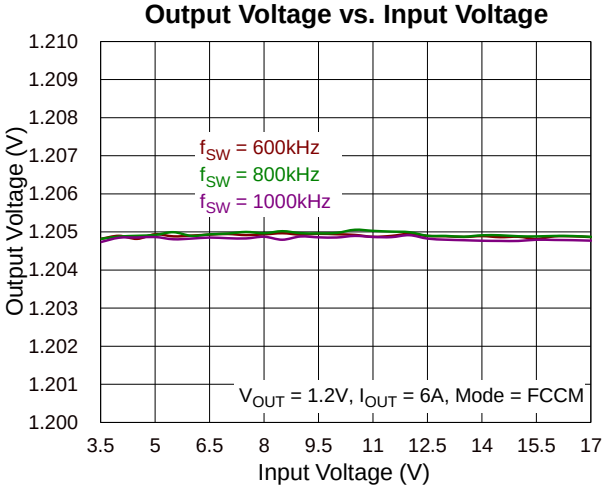


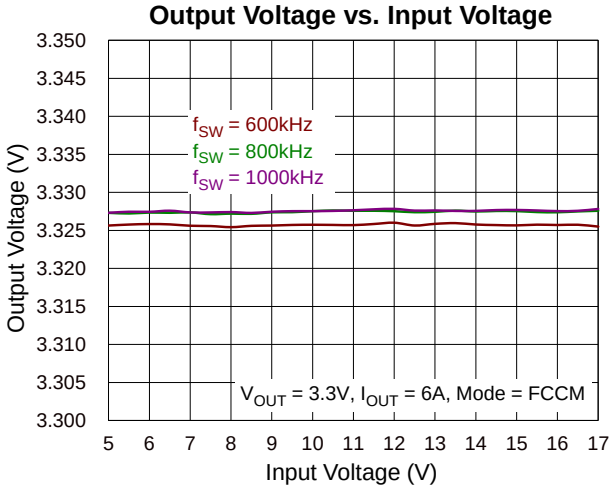




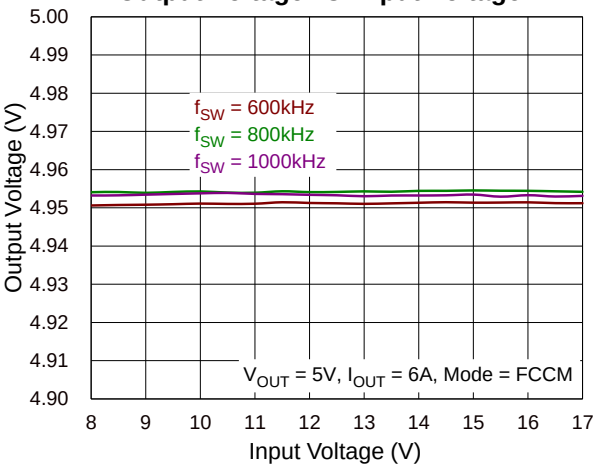




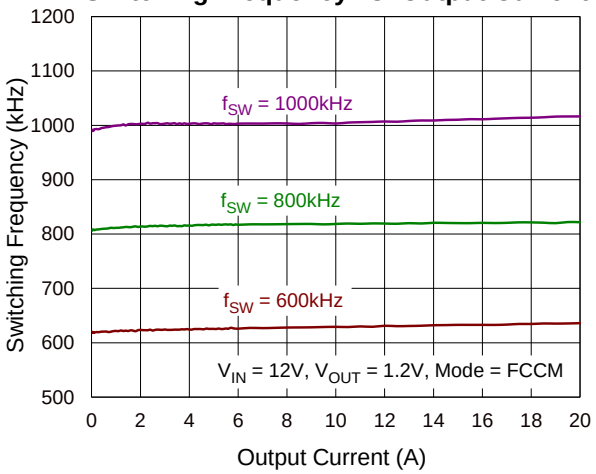




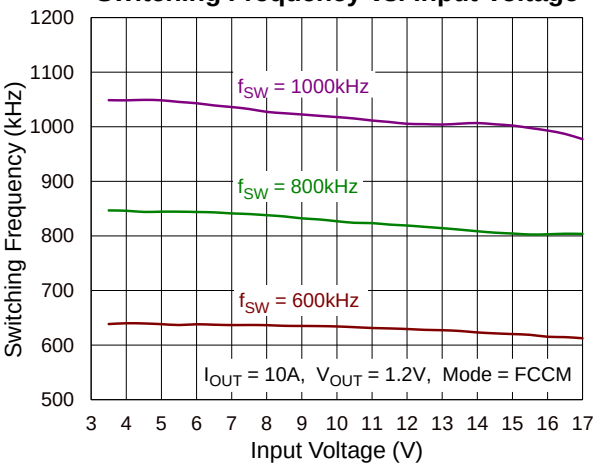
Output Voltage vs. Input Voltage



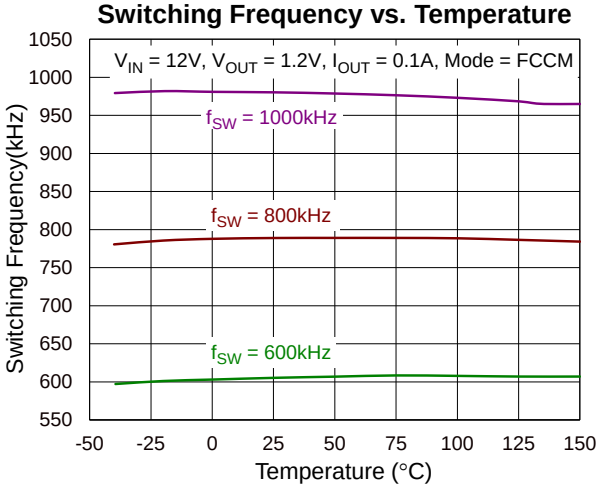
Switching Frequency vs. Output Current



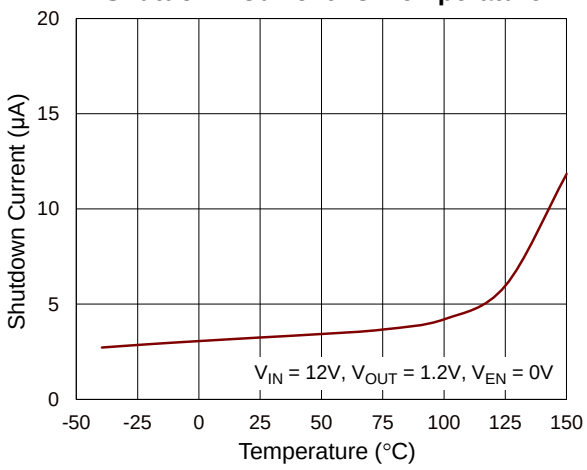
Switching Frequency vs. Input Voltage



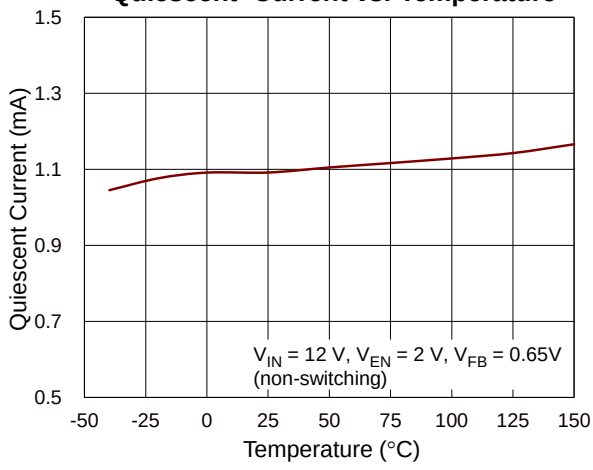
Switching Frequency vs. Temperature



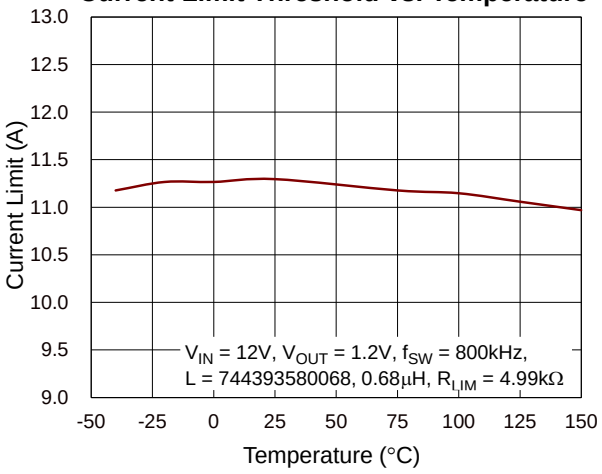
Shutdown Current vs. Temperature



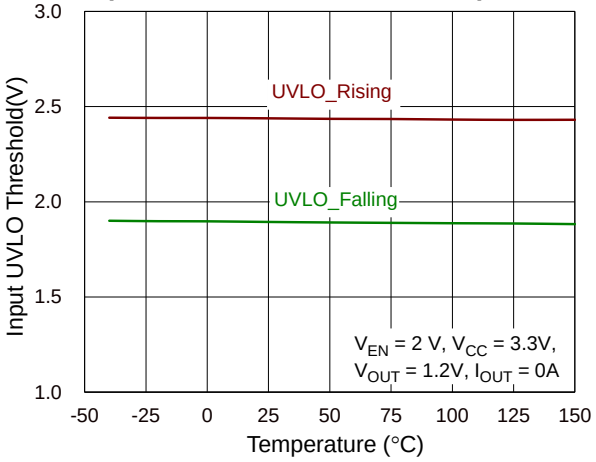
Quiescent Current vs. Temperature



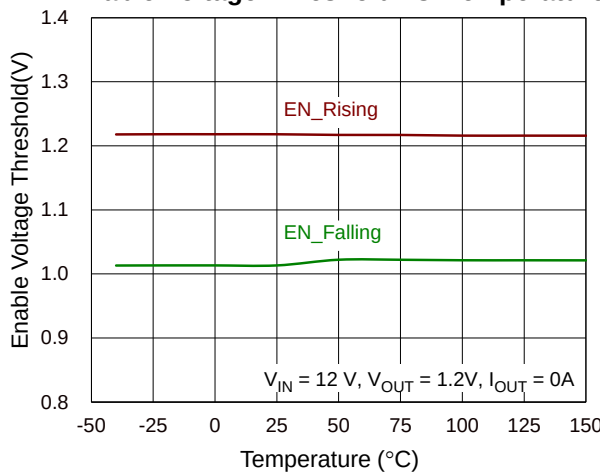
Current Limit Threshold vs. Temperature



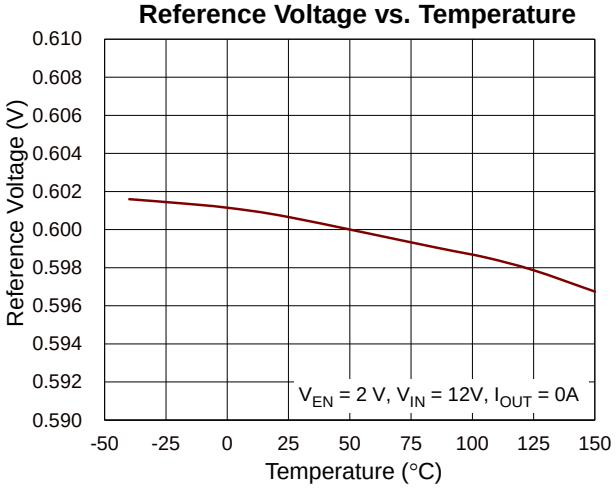
Input UVLO Threshold vs. Temperature



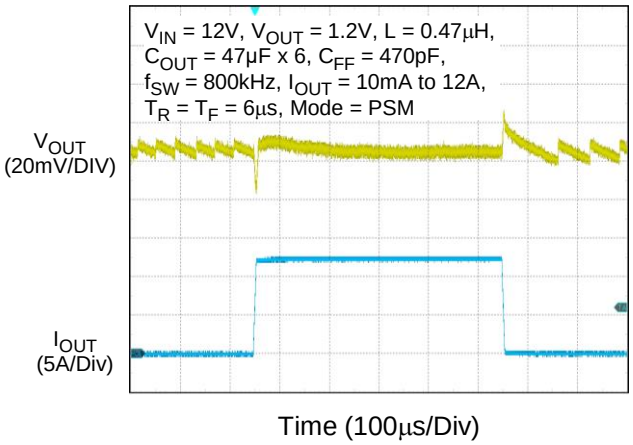
Enable Voltage Threshold vs. Temperature



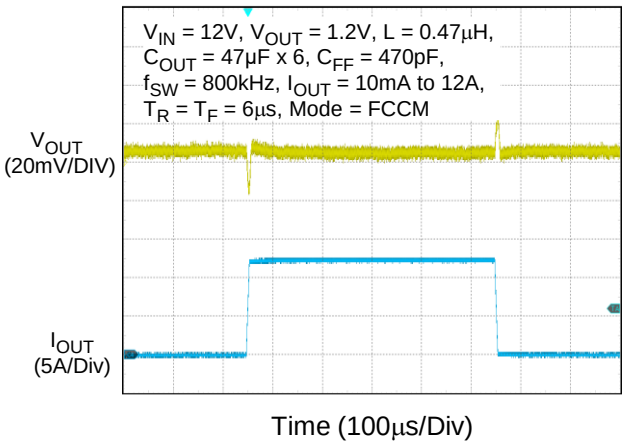
Reference Voltage vs. Temperature



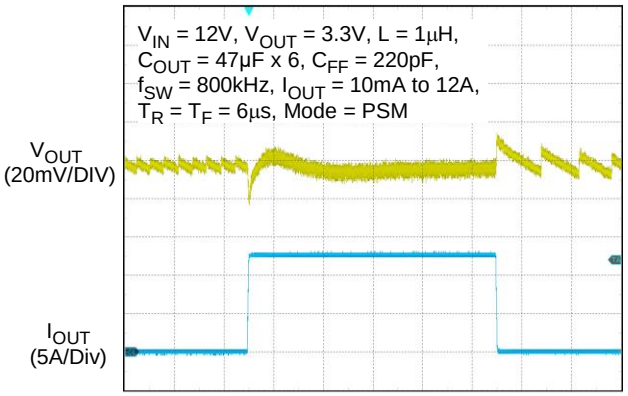
Load Transient Response



Load Transient Response



Load Transient Response



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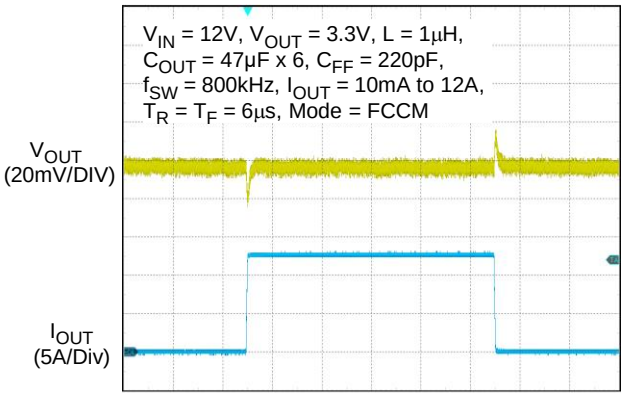

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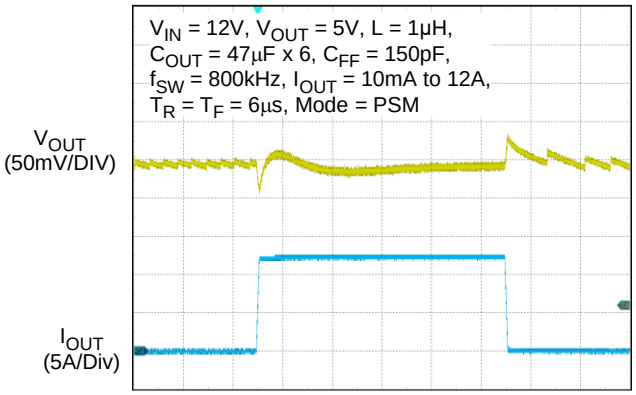
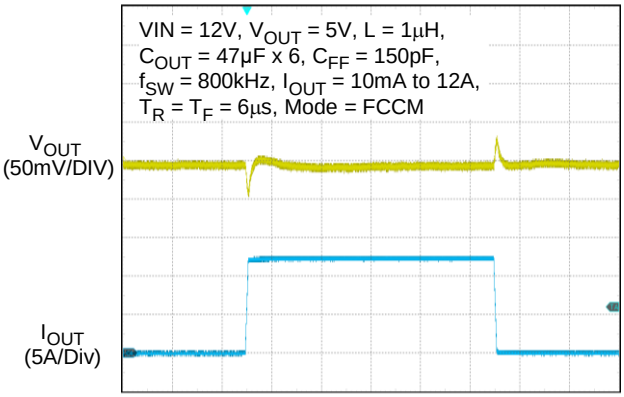
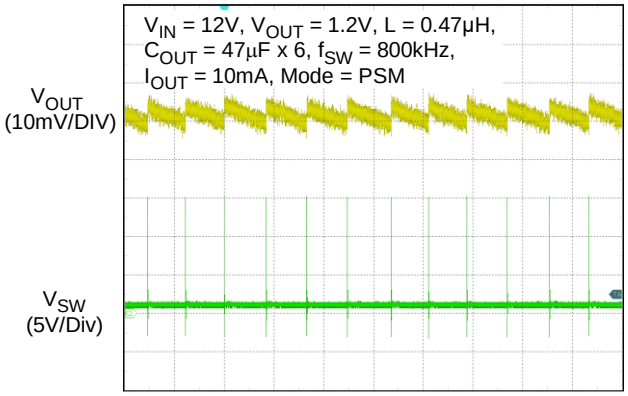


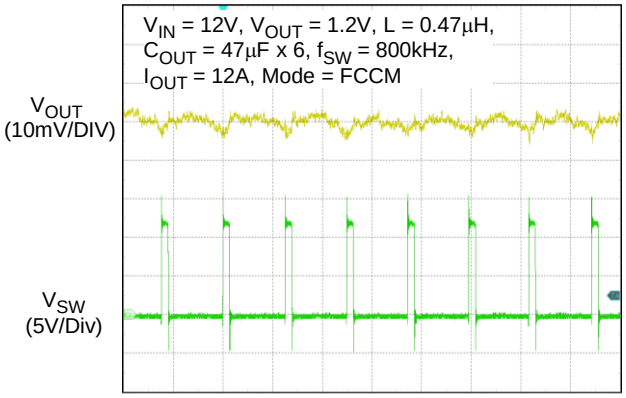
Load Transient Response



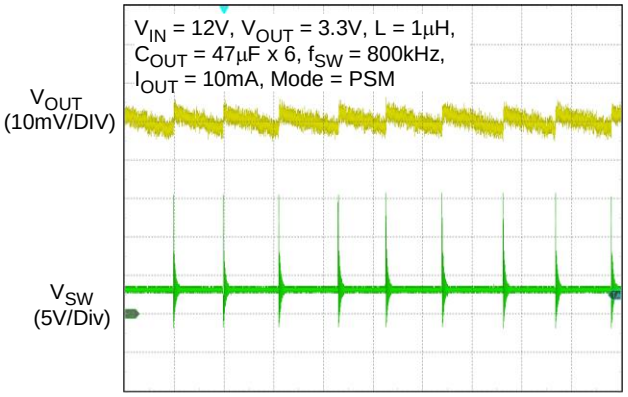
Output Ripple Voltage



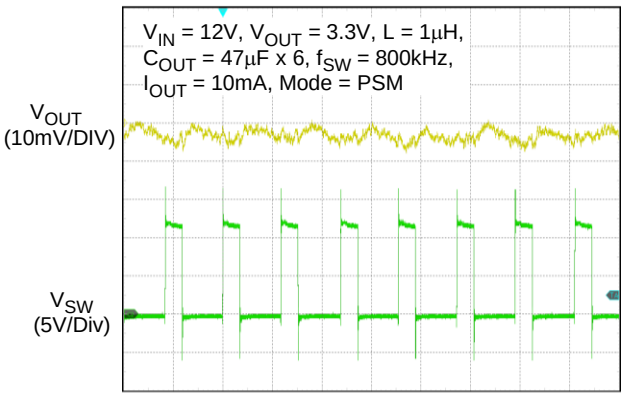
Output Ripple Voltage



Output Ripple Voltage



Output Ripple Voltage



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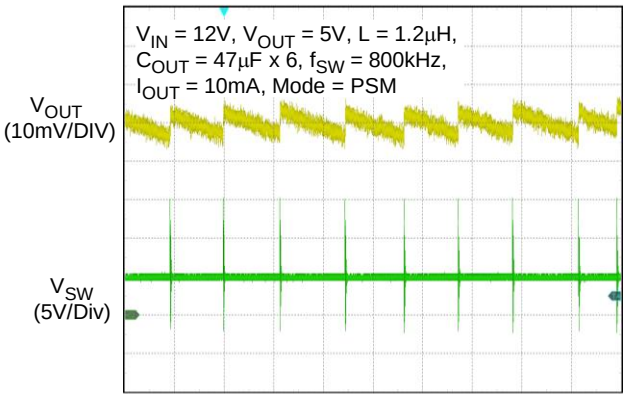
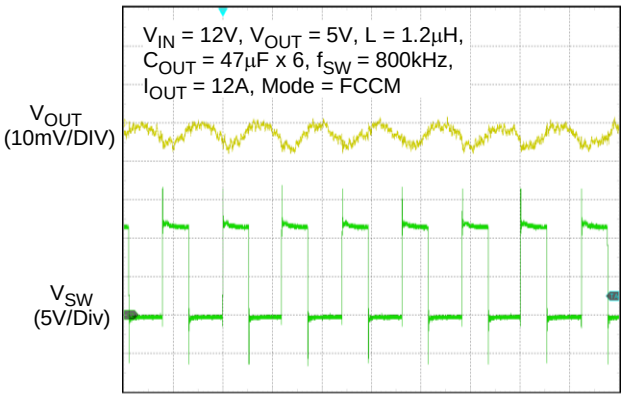
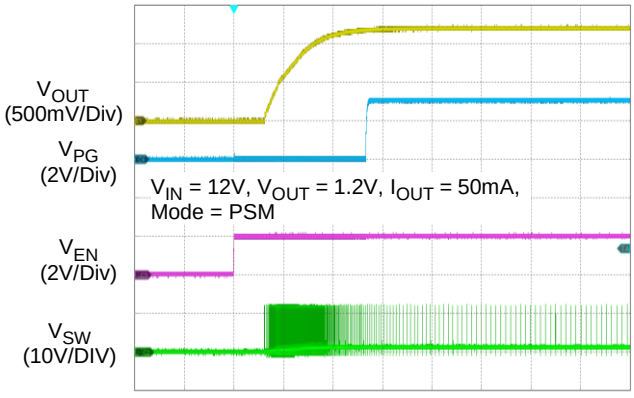


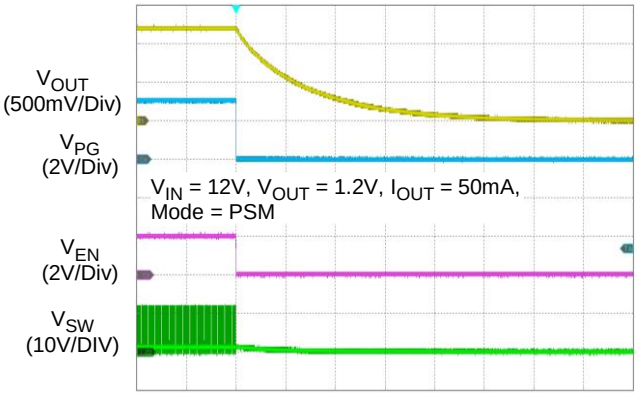
Output Ripple Voltage



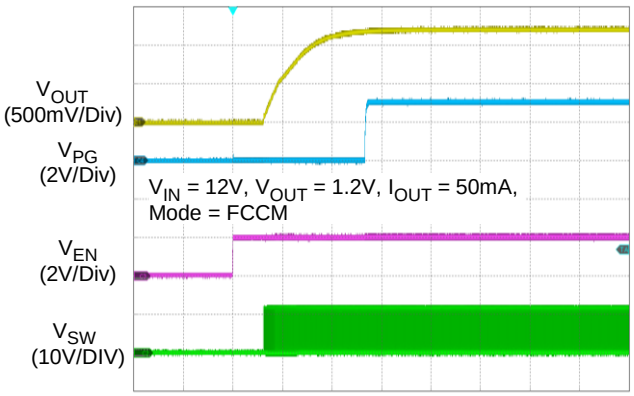
Power On from EN



Power Off from EN

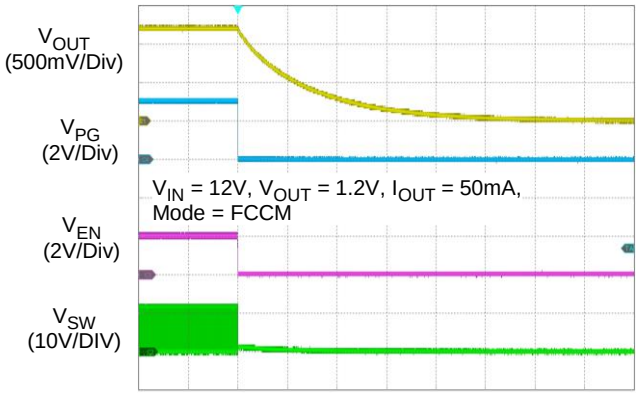


Power On from EN



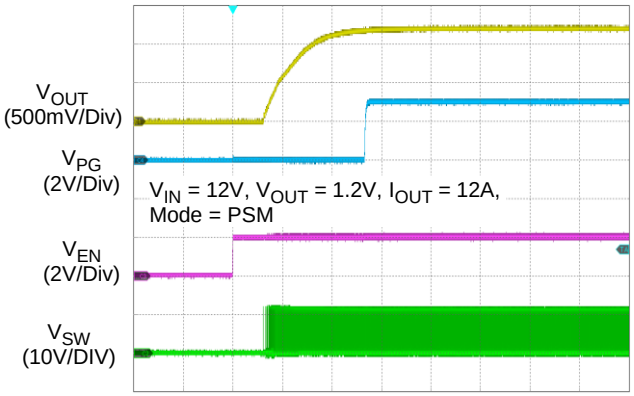
Time (1ms/Div)

Power Off from EN



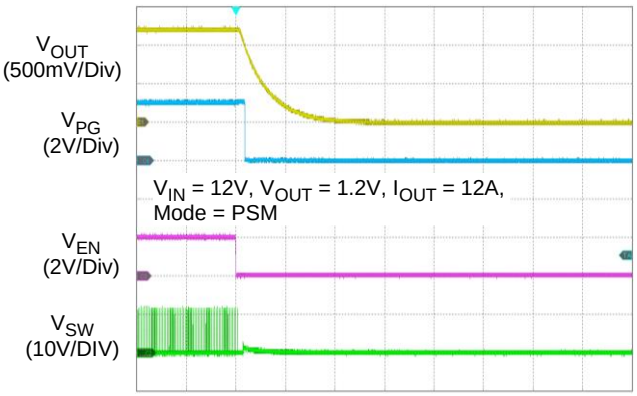
Time (10ms/Div)

Power On from EN



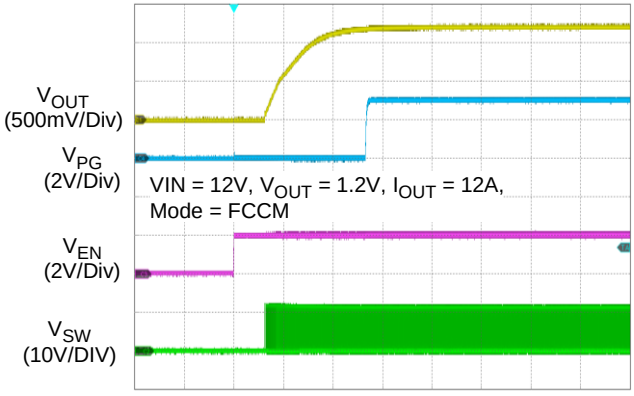
Time (1ms/Div)

Power Off from EN



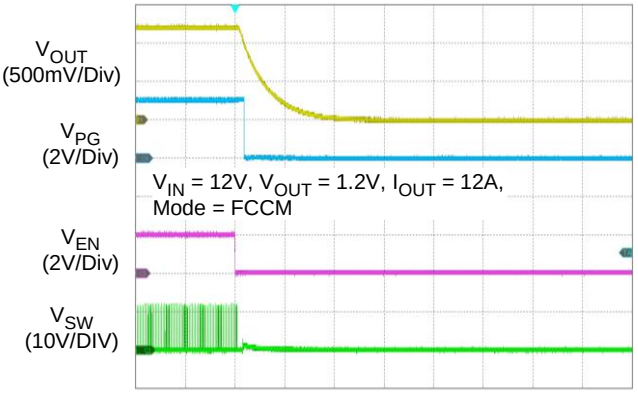
Time (40µs/Div)

Power On from EN



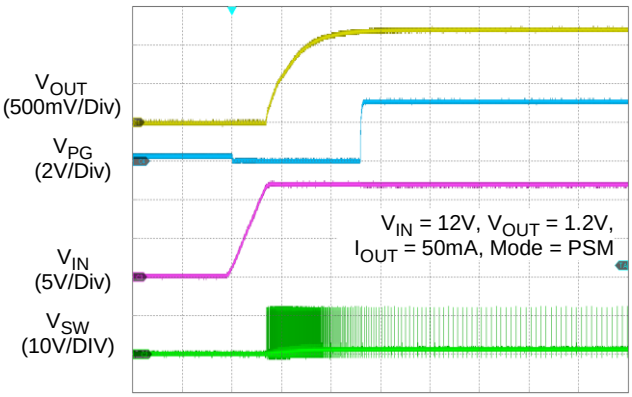
Time (1ms/Div)

Power Off from EN



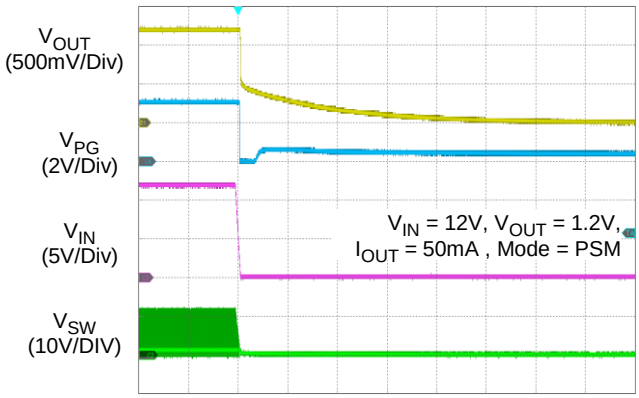
Time (40µs/Div)

Power On from VIN



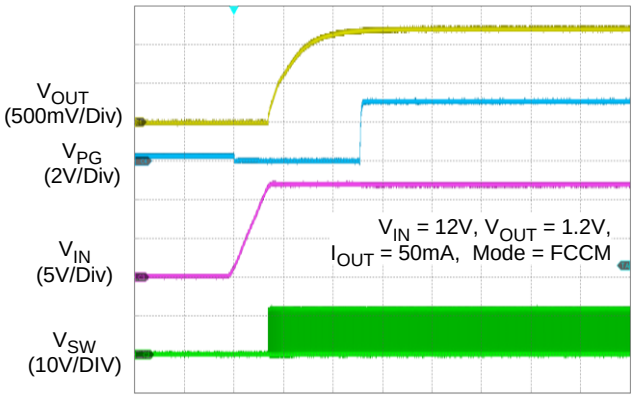
Time (1ms/Div)

Power Off from VIN



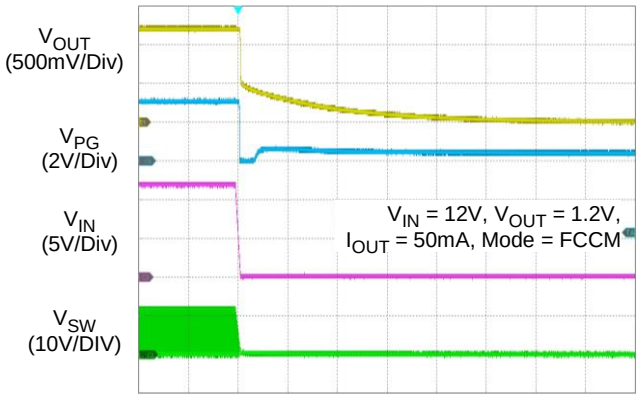
Time (20ms/Div)

Power On from VIN



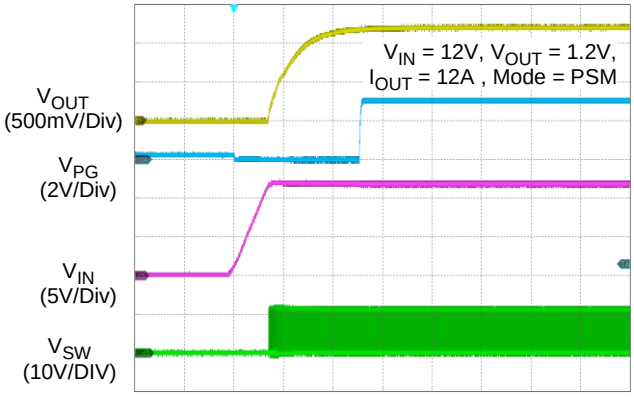
Time (1ms/Div)

Power Off from VIN



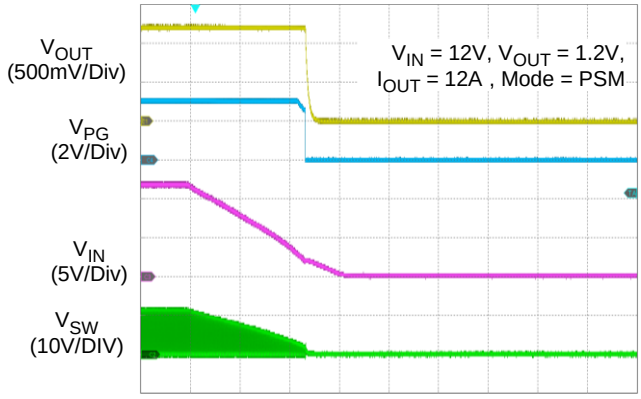
Time (20ms/Div)

Power On from VIN



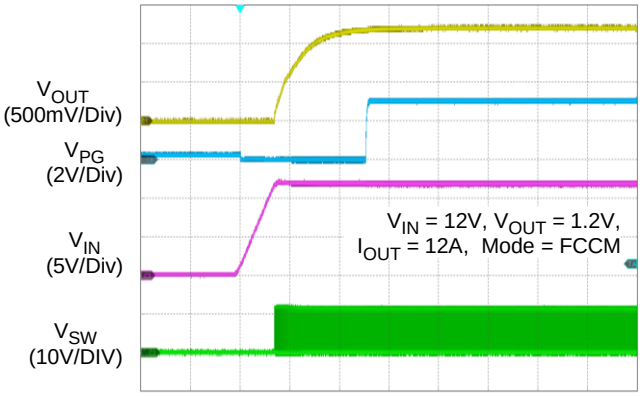
Time (1ms/Div)

Power Off from VIN



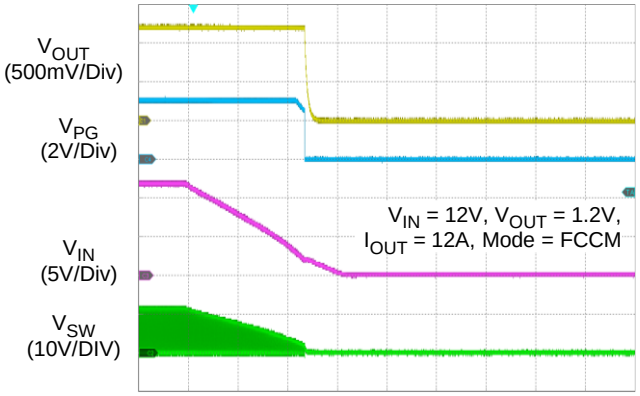
Time (500µs/Div)

Power On from VIN



Time (1ms/Div)

Power Off from VIN



Time (500µs/Div)

17 Operation

The RTQ2812A is a high-efficiency synchronous step-down converter that utilizes the proprietary Advanced Constant-On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small capacitance to reduce PCB size.

During normal operation, the internal high-side MOSFET (HS-FET) turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the high-side MOSFET turns off, the low-side MOSFET (LS-FET) turns on. Due to the output capacitor ESR, the voltage ripple on the output has a similar shape to the inductor current. Via the feedback resistor network, this voltage ripple is compared with the internal reference. When the minimum off-time one-shot (210ns, max.) has timed out and the inductor current is below the current-limit threshold, the one-shot is triggered again if the feedback voltage falls below the internal V_{REF} (0.6V, typ.). The RTQ2812A supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). The ACOT® control architecture also features excellent transient response, further improving the output variation during high-frequency load transients, especially when a load suddenly increases.

The conventional COT controller implements the on-time to be inversely proportional to input voltage and directly proportional to the output voltage to achieve pseudo-fixed frequency over the input voltage range. However, even with defined input and output voltages, a fixed ON time means that the frequency has to increase at higher load levels to compensate for the power losses in the MOSFETs and the inductor. The ACOT® control further adds a frequency locked loop system, which slowly adjusts the ON time to compensate for the power losses without influencing the fast transient behavior of the COT topology.

17.1 Power and Bias Supply

The VIN pins on the RTQ2812A supply voltage to the drain terminal of the internal high-side MOSFET. These pins also supply bias voltage for an internal regulator that generates 3V at the VCC pin. The voltage on the VCC pin is used for internal chip bias and gate drive for the low-side MOSFET. The gate drive for the high-side MOSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins. C_{BOOT} is charged by an internal synchronous diode from VCC. In addition, an internal charge pump maintains that the C_{BOOT} voltage is sufficient to turn on the high-side MOSFET.

To improve efficiency and limit power dissipation in the VIN, an external voltage that is higher than the LDO's internal output voltage can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequencing can be applied. However, it is important to understand that if there is a discharge path on the VCC rail that can draw a current higher than the internal LDO's current limit from the VCC, then the VCC drops below the UVLO falling threshold and cause the output of the RTQ2812A to shut down.

17.2 Enable, Start-Up, Shutdown and UVLO

The RTQ2812A implements undervoltage lockout protection (UVLO) to prevent operation without fully turning on the internal power MOSFETs. The UVLO monitors the internal LDO regulator voltage. When the VCC voltage is lower than the UVLO threshold voltage, the device is shutdown.

The EN pin is provided to control the device turn-on and turn-off. When the EN pin voltage is above the turn-on threshold (V_{EN_R}), the device is enabled. When the EN pin voltage falls below the turn-off threshold (V_{EN_F}), RTQ2812A is disabled. If the EN pin is floating, the RTQ2812A internally pulls down the EN pin continuously.

When the EN pin voltage rises above the enable threshold voltage, and V_{CC} rises above the $V_{CC\_UVLO\_R}$, the device enters its start-up sequence and initiates a soft-start ramp of the output voltage. An internal soft-start ramp of 1ms (typ.) will limit the ramp rate of the output voltage to prevent excessive input current during start-up. If a longer ramp time is desired, the capacitors can be placed between the SS/TR pin and both the AGND and RGND

pins. Use a 22nF capacitor for C_{SS2}, and a larger value ranging from 22nF to 220nF for C_{SS1}. If this external ramp rate is slower than the internal 1ms soft-start, the output voltage will be limited by the ramp rate on the SS/TR pin instead. The typical external soft-start time from 0% to 91.5% of V_{REF} can be calculated by the equation below.

$$C_{SS1}(nF) + C_{SS2}\ (nF) = \frac{t_{SS}(ms) \times 42(\mu A)}{0.55V}$$

where C_{SS2} is required to be a minimum of 22nF; C_{SS1} is recommended 22nF to 220nF

When the V_{EN} is lower than V_{EN_F}, the voltage of the SS/TR pin discharges to RGND.

Figure 1 below shows the typical power-up sequence of the device. When the voltage on the VIN and EN pins crosses the input undervoltage lockout rising threshold and EN input rising threshold. After the voltage on the VCC pin reaches the VCC undervoltage lockout rising threshold, the device will start switching if the voltage difference between the SS/TR pin and FB pin is equal to 100mV (i.e. $V_{SS/TR} - V_{FB}$ = 100mV, typ.) after setting detection is completed. The SS/TR pin should never be left unconnected for soft-start control. After the V_{FB} rises above the V_{TH_PGLH1} (91.5% of the V_{REF}, typ.), the PGOOD pin will enter a high impedance state after delay time t_{PGDLY} (0.8ms, typ.).

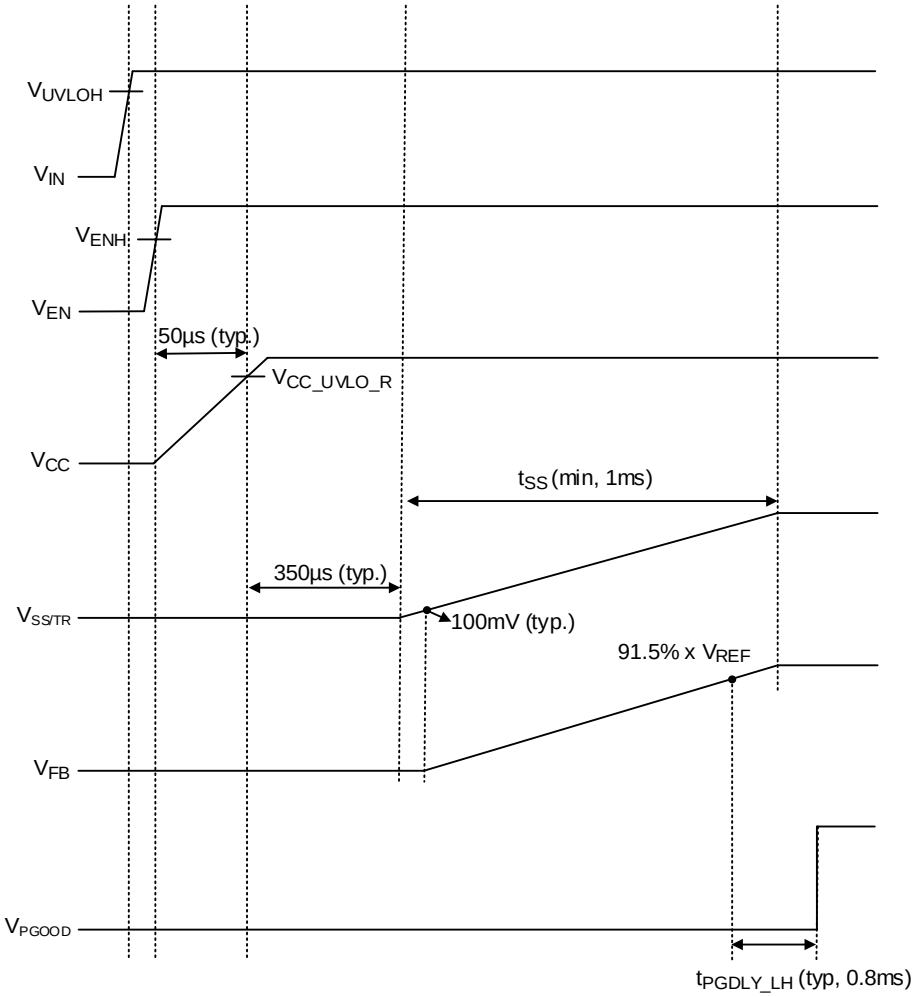


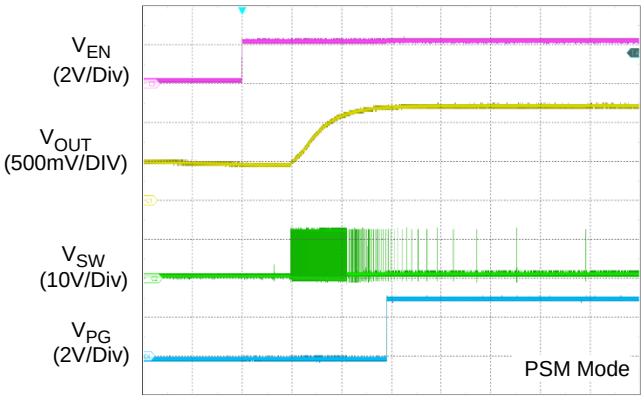
Figure 1. Power-Up Sequence

17.3 Output Voltage Tracking and External Reference

The RTQ2812A can replace the internal voltage reference (V_{REF}) or track an external power rail by adding an external voltage signal to the SS/TR pin. The V_{FB} will track this signal, which ranges from 0.3 V to 1.4 V. During startup, it is essential to ensure that the SS/TR pin voltage reaches 600mV or higher for proper operation. The Power-Good Output function is activated if V_{REF} or an external voltage signal exceeds 550mV, and it is disabled if the external voltage signal at the SS/TR pin is lower than 500mV.

17.4 Pre-Bias

If there is a residual voltage on the output voltage before startup, both the high-side and low-side MOSFETs are prohibited from switching until the internal soft-start ramp is higher than the feedback voltage.
Switching will begin when the soft-start ramp crosses above the feedback voltage**,** and the output voltage will smoothly rise from the pre-biased level to its regulated target. Figure 2 shows an example of pre-bias start-up.



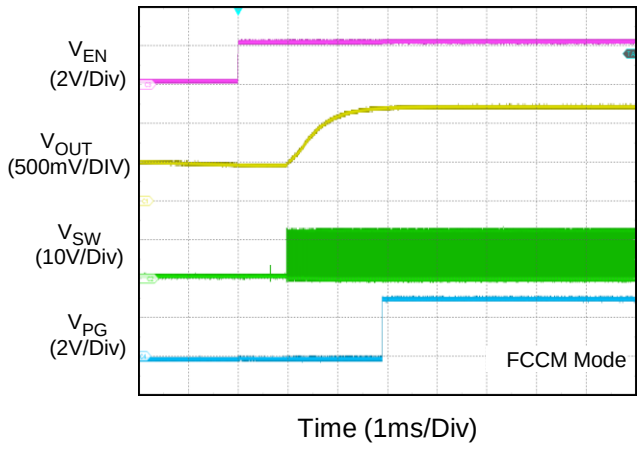


Figure 2. Pre-bias Start-Up (Updated)

17.5 Minimum On-Time and Minimum Off-Time

The constraint on the operating duty cycle is determined by the minimum controllable on-time and off-time. The minimum on-time is the smallest duration of time in which the high-side MOSFET can be in its "ON" state. In continuous mode operation, the effective switching frequency will be decreased to regulate the output voltage target when the minimum on-time limits of a converter are reached. However, reducing the operating frequency will alleviate the constraint on the minimum duty cycle. The equation can be ideally estimated without resistive

drop as follows.

$$V_{IN}(max) \le \frac{V_{OUT}}{f_{SW}(max) \times t_{ON\_MIN}(max)}$$

Where t_{ON_MIN}, the minimum on-time is 50ns (max).

The minimum off-time, t_{OFF_MIN}, is the smallest duration during which the RTQ2812A can turn on the low-side MOSFET, trip the current comparator, and then turn the power switch back off. The limit on minimum off-time imposes a maximum duty cycle of t_{ON} /(t_{ON} + t_{OFF_MIN}). The calculation for the minimum off-time and the minimum input voltage considering the loss terms is provided below.

$$V_{IN}(min) \ge \left[\frac{V_{OUT} + I_{OUT\_MAX} \times (R_{DSON\_L} + DCR)}{1 - t_{OFF\_MIN}\ (max) \times f_{SW\ (max)}} \right] + I_{OUT\_MAX} \times (R_{DSON\_H} - R_{DSON\_L})$$

where the minimum off-time of the RTQ2812A is 210ns (max); R_{DSON_H} is the high-side MOSFET on resistance; R_{DSON_L} is the low-side MOSFET on resistance; DCR is the DC resistance of inductor.

17.6 Mode Selection, Switching Frequency

The RTQ2812A offers three different switching frequencies of 600kHz, 800kHz and 1000kHz by setting the MODE pin voltage. The selection of the operating frequency is a tradeoff between efficiency and component size. The high-frequency operation allows the use of smaller inductors and capacitor values, while operation at lower frequencies improves efficiency by reducing internal gate charge and transition losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Furthermore, the RTQ2812A can also offer two modes which are force continuous-conduction mode (FCCM) and pulse skipping mode (PSM) for light load conditions to improve efficiency.

When the MODE pin is left floating, the default status will be set to 600kHz for PSM operation. Users can configure the mode and operating frequency by connecting a resistor to the AGND pin or VCC pin, as specified in Table 3.

Table 3. Mode Pin Selection

Mode Pin Connections	Light Load Mode	Switching frequency (kHz)
Short to VCC	PSM	600
243KΩ ±10% to AGND	PSM	800
121KΩ ±10% to AGND	PSM	1000
Short to AGND	FCCM	600
30.1KΩ ±10% to AGND	FCCM	800
60.4KΩ ±10% to AGND	FCCM	1000

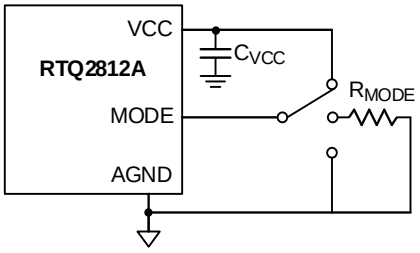


Figure 3. MODE Connection

17.7 Light Load Operation

At low load current, the inductor current can drop to zero and become negative. This condition is detected by internal zero current-detect circuitry that utilizes the low-side MOSFET R_{DSON_L} to sense the inductor current. The low-side MOSFET is turned off when the inductor current drops to zero, resulting in pulse skipping mode (PSM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the feedback voltage falls below the internal V_{REF}. PSM operation maintains high efficiency at light load, while setting MODE to FCCM operation helps meet tight voltage regulation accuracy requirements.

17.8 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of BOOT capacitor for turning on the high-side MOSFET at any conditions. The BOOT UVLO usually actives at extremely high conversion ratio or the higher VOUT application operates at very light load. With such conditions when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_F}$ (2.3V, typ.), the device turns on the BOOT recharge path (200ns, typ.) to charge the BOOT capacitor.

17.9 Power-Good Output

The RTQ2812A features an open-drain power-good indication which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, V_{PGOOD} is actively held low and only allowed to become high after soft-start is finished. If V_{FB} rises above the V_{TH_PGLH1} (91.5% of the V_{REF}, typ.), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} falls below the PGOOD low threshold V_{TH_PGHL2} (80% of the V_{REF}, typ.) or exceeds V_{TH_PGHL1} (116% of the V_{REF}, typ.), the PGOOD pin will be pulled low. For V_{FB} higher than V_{TH_PGHL1}, V_{PGOOD} can be pulled high again if V_{FB} drops back to the PGOOD high threshold V_{TH_PGLH2} (106% of the V_{REF}, typ.). Once being started-up, if any internal protection is triggered, PGOOD pin will be pulled low to GND. The internal open-drain pull-down device will pull the V_{PGOOD} low. This is to prevent false flag operation for short excursions in output voltage, such as during line and load transients. The power-good indication profile is shown in Figure 4.

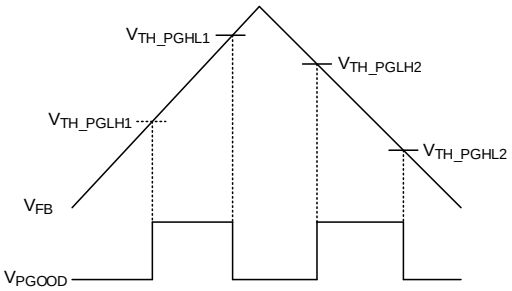


Figure 4. The Logic of PGOOD

17.10 Overcurrent Limit

The RTQ2812A features cycle-by-cycle current-limit protection on low-side MOSFETs and the protection prevents the device from catastrophic damage due to in output short circuit, overcurrent, or inductor saturation.

The low-side MOSFET valley current-limit protection is achieved by measuring the inductor current through the low-side MOSFET and mirroring the RLIM pin with the ratio of G_{CS} using a resistor during the low-side on-time. Once the inductor current through the low-side MOSFET is above the low-side MOSFET valley current-limit threshold (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the I_{LIM_L}; that is, another on-time can only be triggered when the inductor current goes below the I_{LIM_L}. Figure 5. shows an example of overcurrent protection, and the output current-limit threshold can be calculated as below:

$$R_{LIM}(\Omega) = \frac{V_{LIM}}{G_{CS} \times \left(I_{LIM} - \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}} \right)}$$

Where V_{LIM} =1.2V, G_{CS} = 10μA/A, and I_{LIM} is the desired output current limit (A).

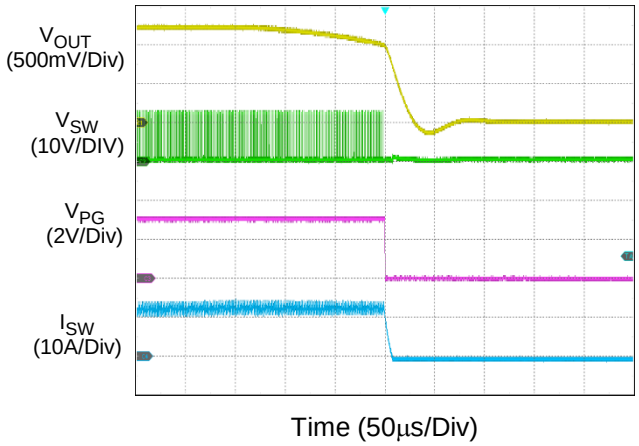


Figure 5. Overcurrent Protection (updated)

17.11 Output Undervoltage Protection

The RTQ2812A includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection threshold V_{UVP} (80% of the V_{REF}, typ.), the UV comparator will go high to turn off both the internal high-side and low-side MOSFETs. The RTQ2812A will enter output undervoltage protection with hiccup mode. During hiccup mode, the device will shut down for t_{HICCUP_OFF} (8.5ms, typ.), and then attempt to recover automatically for t_{HICCUP_ON} (2.4ms, typ.).

If the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resumes normal operation as soon as the overload or short-circuit condition is removed. The behavior of UVP and Hiccup mode is shown in Figure 6.

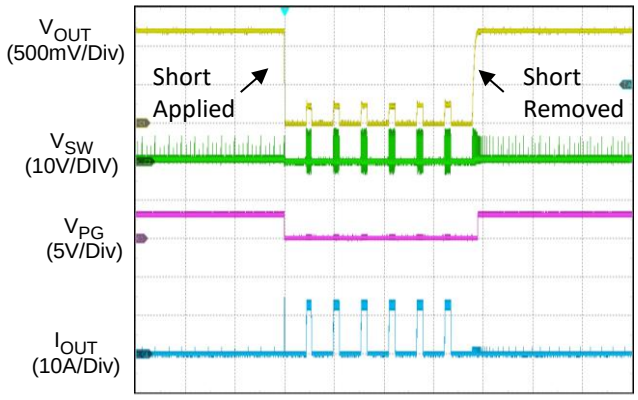


Figure 6. Short-Circuit Protection and Recovery

17.12 Negative Current Limit

The RTQ2812A also monitors inductor current during the "ON" state of the low-side MOSFET to prevent too large negative current flowing through the low-side MOSFET. Once the negative current exceeds the low-side switch negative current-limit threshold I_{LIM_NEG} (–10A, typ.) , the device turns off the low-side MOSFET and turns on the high-side MOSFET for the on-time determined by V_{IN}, V_{OUT} and f_{SW}. After the high-side MOSFET on-time expires, the low-side MOSFET turns on again. This behavior can keep the valley of negative current at I_{LIM_NEG} to protect low-side MOSFET. A designer should choose appropriate inductance to avoid triggering I_{LIM_NEG} during normal operation.

17.13 Output Overvoltage Protection

The RTQ2812A includes an output overvoltage protection (OVP) circuit to limit output voltage and minimize output voltage overshoot. If the V_{FB} goes above 116% of the V_{REF}, the high-side MOSFET will be latched off and the PGOOD pin remains low until the VCC or EN is recycled. In the meantime, if the overvoltage condition still exists, the low-side MOSFET remains on to discharge output voltage until the low-side switch valley current reaches the negative current limit (I_{LIM_NEG}). Once reaching the I_{LIM_NEG} the low-side MOSFET is turned off temporarily around 700ns before it is turned on again.

The RTQ2812A repeats in this cycle until the output voltage is brought down when the V_{FB} goes below 50% of the V_{REF}, the low-side MOSFET continues to turn on. The device needs EN or VIN to recycle to clear the OVP fault. The overvoltage protection is shown in Figure 7.

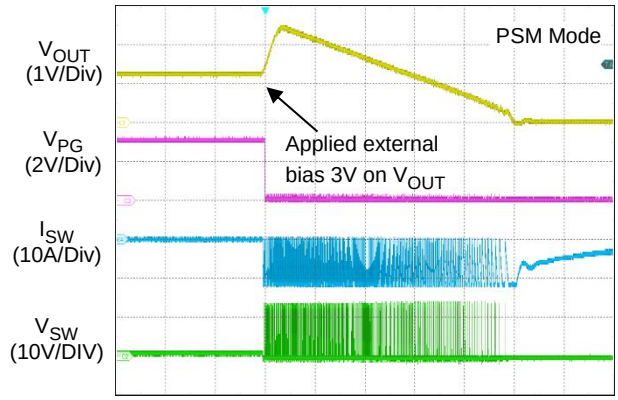


Figure 7. Overvoltage Protection

17.14 Output Quick Discharge Mode

The RTQ2812A features Output Quick Discharge Mode (OQDM) to mitigate overshoot before triggering the output overvoltage protection (OVP). When the V_{FB} voltage exceeds 104% of the V_{REF} but remains below the OVP threshold (116%, typ.), OQDM is activated. During OQDM, the high-side MOSFET is off, while the low-side MOSFET remains on until it reaches −10A (typ.) or the V_{FB} voltage falls below 102%. Once the I_{LIM_NEG} is reached, the low-side MOSFET is briefly turned off for 700ns before being turned on again. This sequence is repeated until the V_{FB} voltage falls below 102% of the V_{REF}. After completing 15 consecutive FCCM cycles, the RTQ2812A exits the OQDM. This mode effectively reduces overshoot and ensures stable operation.

Figure 8. Output-Discharge Mode

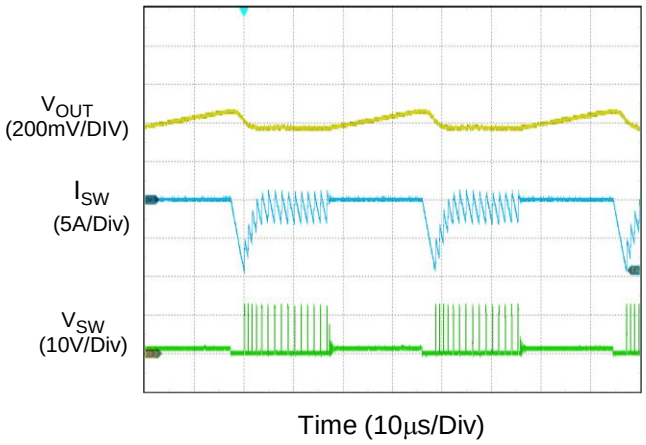


Figure 8. Output Quick Discharge Mode

17.15 Output Voltage Discharge

When the RTQ2812A is disabled by EN pin, UVLO or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (80Ω, typ.) connected to ground. This function prevents the reverse current from flowing the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

17.16 Over-Temperature Protection (OTP)

The RTQ2812A includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds the over-temperature protection threshold T_{OTP} (160°C, typ.). Once the junction temperature cools down by the over-temperature protection hysteresis T_{OTP_HYS} (30°C, typ.), the RTQ2812A will resume normal operation with a complete soft-start. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

A general RTQ2812A application circuit is shown in a typical application circuit section. External component selection is largely driven by the load requirement. Next, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT}, can be selected. Next, feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as the EN and UVLO threshold, external soft-start time, and Power-Good function.

18.1 Switching Frequency and MODE Selection

The switching frequency, current limit, and switching mode (PSM or FCCM) are set by a voltage divider connected solely from VCC to AGND to the MODE pin.

The selection of the switching frequency is a trade-off between efficiency and system component size. High-frequency operation allows the use of smaller inductor and capacitor values. Operating at lower frequencies improves efficiency by reducing internal gate charge and transition losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

18.2 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degrade transient response. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current-limit threshold and increases the AC losses in the inductor. To enhance efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines the ripple current and the load-current value at which the DCM/FCCM switchover occurs.

The selected inductor must require a enough saturate current rating above the peak inductor current before saturation. The peak inductor current (I_{L_PEAK}) is estimated as below.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level

calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

The reverse inductor current should be considered. In FCCM operation, the design of inductor valley current should be higher than I_{LIM_NEG} to prevent triggering the negative current limit at no load operation.

18.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. The C_{IN} should be sized to do this without causing a large variation in input voltage. The peak-to-peak voltage ripple on input capacitor can be estimated as the equation below:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 9 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors.

The equivalent series resistance (ESR) is very low for ceramic capacitors. The ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated as the equation below:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} = 200mV for typical application (V_{IN} > 7V)

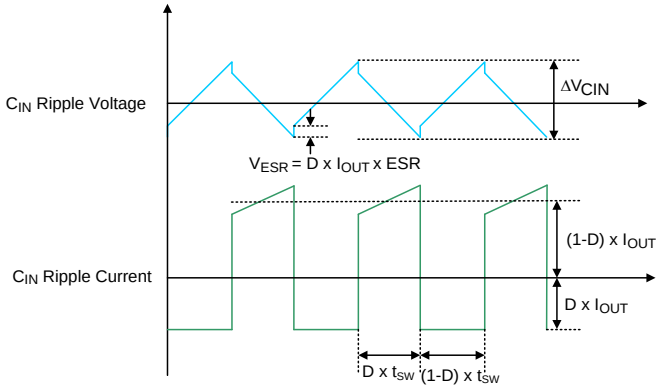


Figure 9. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the converter can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which should be considered when evaluating the current capabilities of the input capacitors. The maximum ripple voltage usually

occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is common to use the worse I_{RMS} ≅ 0.5 x I_{OUT_MAX} at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because its small size, robustness and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2812A circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, one small decoupling ceramic capacitor of 1μF should be placed close to the part. The capacitors should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

18.4 Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple, the transient loads and to ensure that control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, and can be expressed as below:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The highest output ripple is at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined by:

$$\Delta V_{OUT\_SAG} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

18.5 Internal VCC Regulator

Good bypassing at VCC pin is necessary to supply the high transient currents required by the power MOSFET gate drivers. Place a low ESR MLCC capacitor with capacitance ≥ 1μF (or effective capacitance ≥ 0.88μF) as close as possible to VCC pin, and the rated voltage of C_{VCC} is at least 6.3V or higher to minimize DC bias derating, using 0603 or 0805 in size is recommended.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Do not connect VCC to provide power to other devices or loads.

18.6 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal MOSFET switch to a voltage equal to approximately V_{VCC} each time the LS-FET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle.

The selection of C_{BOOT} considers the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BOOT} such that the available gate-drive voltage is not significantly degraded when determining C_{BOOT}. A typical range of ΔV_{BOOT} is from 100mV to 300mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. For most applications, a 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

EMI issue is worse when the switch is turned on rapidly due to high di/dt noises. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 10Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 10, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor connection.

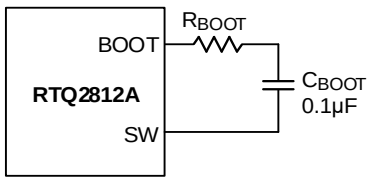


Figure 10 External Bootstrap Resistor at the BOOT Pin

18.7 Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 11 and the output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage V_{REF}, is typically 0.6V

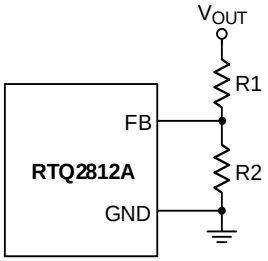


Figure 11. Output Voltage Setting

The recommended resistance of R2 is 10kΩ, ranging from 1kΩ to 10kΩ for good noise immunity consideration. The resistance of R1 can then be obtained as below:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used. The placement of the resistive divider should be very close to the FB pin to minimize PCB trace length and noise immunity consideration. Furthermore, great care should be taken to route the feedback trace away from noise sources, such as the inductor or the SW trace.

18.8 Feedforward Capacitor (C_{FF})

The RTQ2812A is optimized for low duty-cycle applications and the control loop is stable with low ESR ceramic output capacitors. In higher duty-cycle applications (higher output voltages or lower input voltage), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Because of the large internal ripple in this condition, the response may become too slow, and may show an under-damped response. This can cause some ringing in the output, and is especially visible at higher output voltage applications like 12V to 5V where duty-cycle is high and the feedback network attenuation is large, adding to the delay. As shown in Figure 12, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

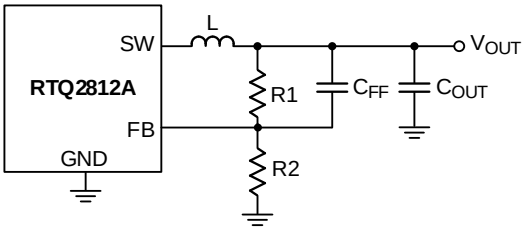


Figure 12. Feedback Loop with Feedforward Capacitor

Loop stability can be checked by viewing the load transient response. A load step with a speed that exceeds the converter bandwidth must be applied. For ACOT®, loop bandwidth can be in the order of 100 to 200kHz, so a load step with 500ns maximum rise time (di/dt ≈ 2A/μs) ensures the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current-limit threshold. A load transient from 30% to 60% of maximum load is reasonable which is shown Figure 13.

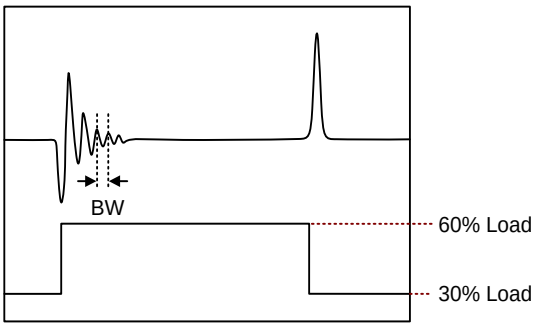


Figure 13. Example of Measuring the Converter BW by Fast Load Transient

C_{FF} can be calculated basing on below equation:

$$C_{FF} = \frac{1}{2\pi \times BW} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Figure 14. shows the transient performance with and without feedforward capacitor.

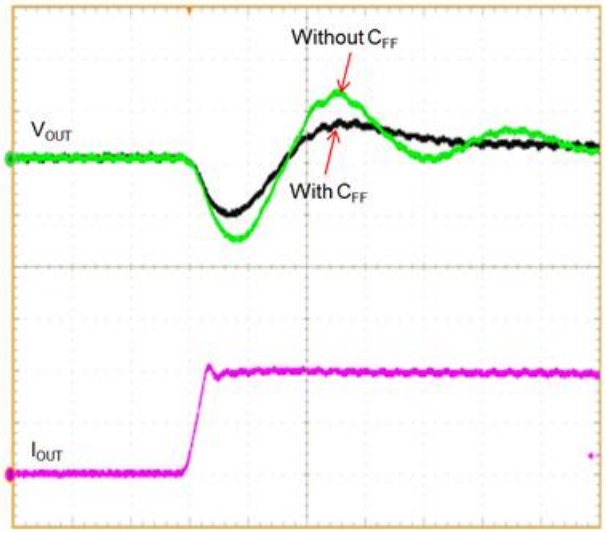


Figure 14. Load Transient Response with and without Feedforward Capacitor

Note that, after defining the C_{FF}, please also check the load regulation because feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage is over specification caused by calculated C_{FF}, please decrease the value of feedforward capacitor C_{FF}.

18.9 Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold (V_{EN_R}), the device starts switching. It stops switching when the EN pin voltage falls below the turn-off threshold (V_{EN_F}). The RTQ2812A internally weekly pull-down the EN pin. For automatic start-up, the EN pin can be connected to the input supply VIN directly through a pull-up resistor R_{EN}. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to VIN by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 15, to have an additional delay.

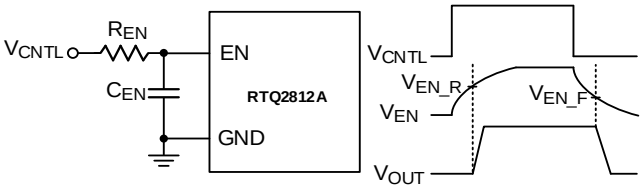


Figure 15. Enable Timing Control

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 16. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin.

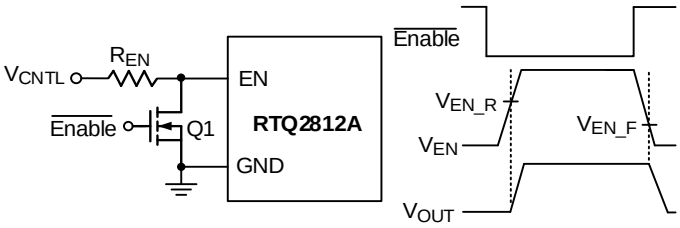


Figure 16. Logic Control for the EN Pin

If the device is desired to enable under specific V_{IN} or be shut down, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input VULO threshold as shown in Figure 17. o set the start voltage, first select the divider resistor REN2, the recommended value is between 10kΩ and 100kΩ. A resistor divider between VIN and EN can establish different turn-on (V_{START}) or turn-off thresholds (V_{STOP}). This is recommended for customer design when without additional EN logic signal, to avoid bouncing occurring at the EN pin.

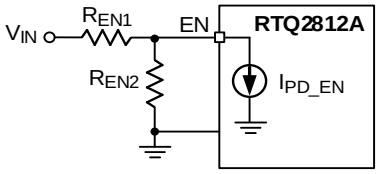


Figure 17. Resistor Divider for Lockout Threshold Setting

To set the start voltage, first select the bottom resistor R_{EN2}, the recommended value is between 10kΩ and 100kΩ. A resistor divider between VIN and EN can set different turn-on (V_{START}) and turn-off thresholds (V_{STOP}), respectively.

$$R_{EN1} = \frac{\left(V_{START} - V_{EN\_R}\right)}{I_{PD\_EN} + \frac{V_{EN\_R}}{R_{EN2}}}$$

$$V_{START} = \left(\frac{V_{EN\_R}}{R_{EN2}} + I_{PDEN}\right) \times R_{EN1} + V_{EN\_R}$$

$$V_{STOP} = \left(\frac{V_{EN\_L}}{R_{EN2}} + I_{PDEN}\right) \times R_{EN1} + V_{EN\_L}$$

18.10 Thermal Considerations

Thermal Considerations In many applications, the RTQ2812A does not generate much heat due to its high efficiency and low thermal resistance of its thermally enhanced WQFN-21L 3x4 (FC) package. However, in applications where the RTQ2812A is running at a high ambient temperature, high input voltage, and high switching frequency, the generated heat may exceed the maximum junction temperature of the part. To avoid permanent damage to the device, the junction temperature should never exceed the maximum junction temperature listed under Absolute Maximum Ratings. If the junction temperature reaches approximately 160°C, the RTQ2812A will stop switching the power MOSFETs until the temperature drops by about 30°C cooler. The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

Where

- $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C.
- T_A is the ambient operating temperature,
- $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be enhanced by incorporating a copper ground heat sink. Additionally, including backside copper with thermal vias, stiffeners, and other enhancements can help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RTQ2812A is used in switching frequency 800kHz applications where V_{IN} = 12V, V_{OUT} = 1V. The efficiency at output current 12A is 86.96% by using VLBU1007090T-R33L (0.33μH, 0.18mΩ DCR) as the inductor and measured at room temperature. The core loss 1.74W can be obtained from its website. In this case, the power dissipation of RTQ2812A is

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I^2_{OUT} \times DCR + P_{CORE}\right) = 0.15 \times 12 - \left(12^2 \times 0.00018 + 0.03386\right) = 1.74W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 25.87°C/W by using RTQ2812A evaluation board with 4 layers PCB and 2oz copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = P_{D,RT} \times \theta_{JA(EFFECTIVE)} + T_A = 1.74W \times 1.1 \times 23.52^oC/W + 25\ ^oC = 95°C$$

18.11 Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2812A:

- Use a four-layer or six-layer PCB with a maximum ground plane for optimal thermal performance.
- Place input MLCC capacitors as close to the VIN and PGND pins as possible. It is highly recommended to use a 1μF/25V/X6S/0402 ceramic capacitor between the VIN pin 10 and PGND pin 11.
- Maximize the width and shorten the main current path, such as the VIN, SW, VOUT, and PGND copper plane, to minimize parasitic impedance.
- Place the decoupling capacitor, C_{VCC}, as close to VCC pin as possible.
- Connect AGND and PGND at the point of the VCC capacitor's ground connection. C_{SS}, R_{MODE}, and R_{LIM} should be connected to AGND using short, direct copper traces.
- Place bootstrap capacitor, C_{BOOT}, as close to IC as possible. Rout the trace with a width of 20mil or wider. A 0.1μF to 1μF with 10V or higher rating is recommended for the bootstrap capacitor.
- Place multiple vias under the device near VIN and PGND, and place near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2812A to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Place capacitors C_{SS1} and C_{SS2} as close to the SS/TR as possible.
- Connect C_{SS1} from the SS/TR to RGND, and connect C_{SS2} from the SS/TR to AGND.
- Connect the feedback sense network behind via the output capacitor rather than the inductor output node.
- Place the feedback components R1/R2/C_{FF} near the device to minimize the FB trace distance, regardless of single-end or remote sensing.
- Ensure that the equivalent impedance of the PCB trace from the RGND pin to the output voltage at a remote location, as well as from the RGND pin to the local main ground, is less than 0.5Ω.
- The ground connection between the analog ground and power ground should be close to the IC to minimize ground current loops. If there is only one ground plane, sufficient isolation should be maintained between analog return signals and high-power signals.
- Figure 18 is the PCB layout example which uses (85mm x 80 mm), four-layer PCB with 2oz copper.

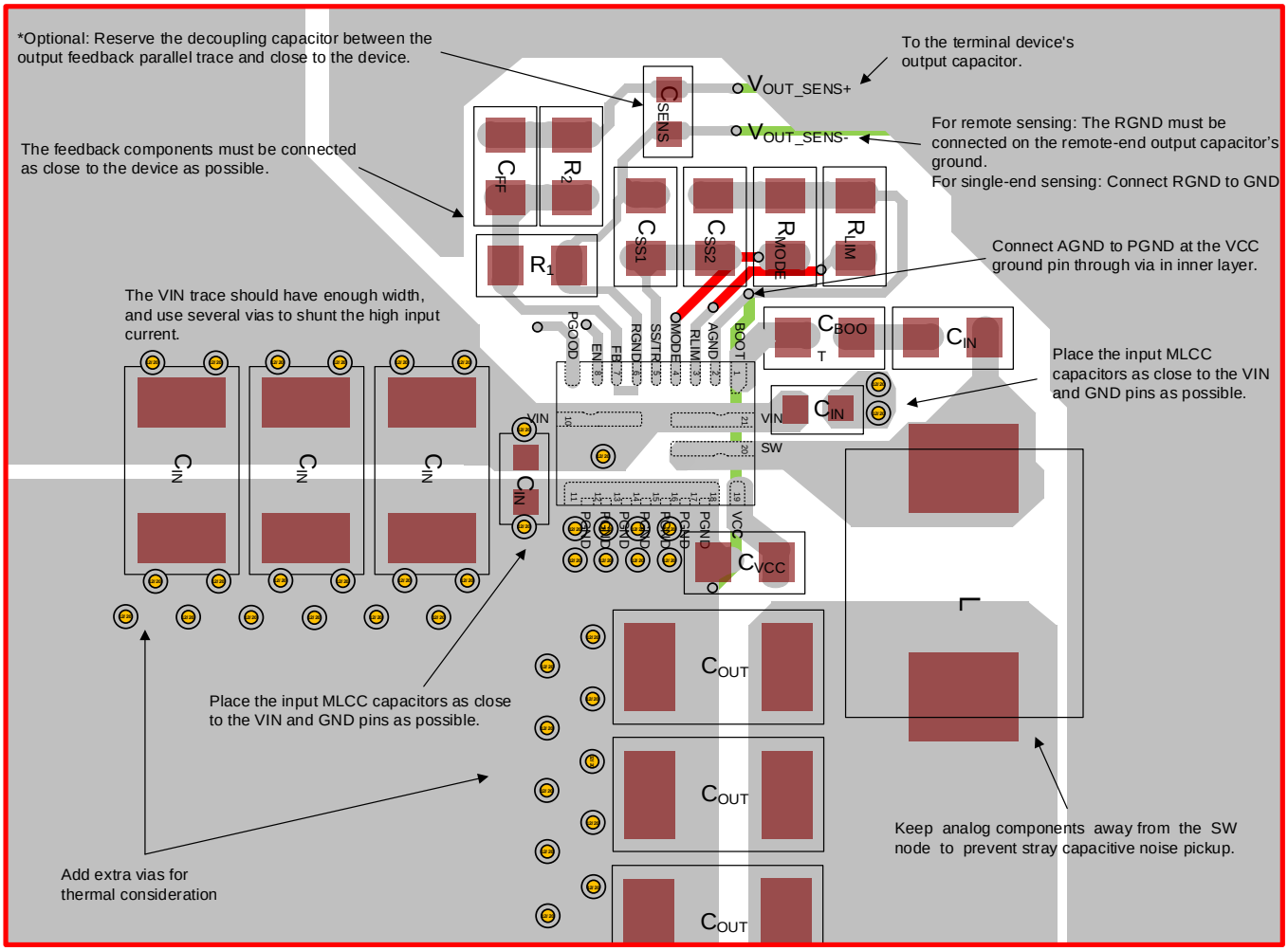
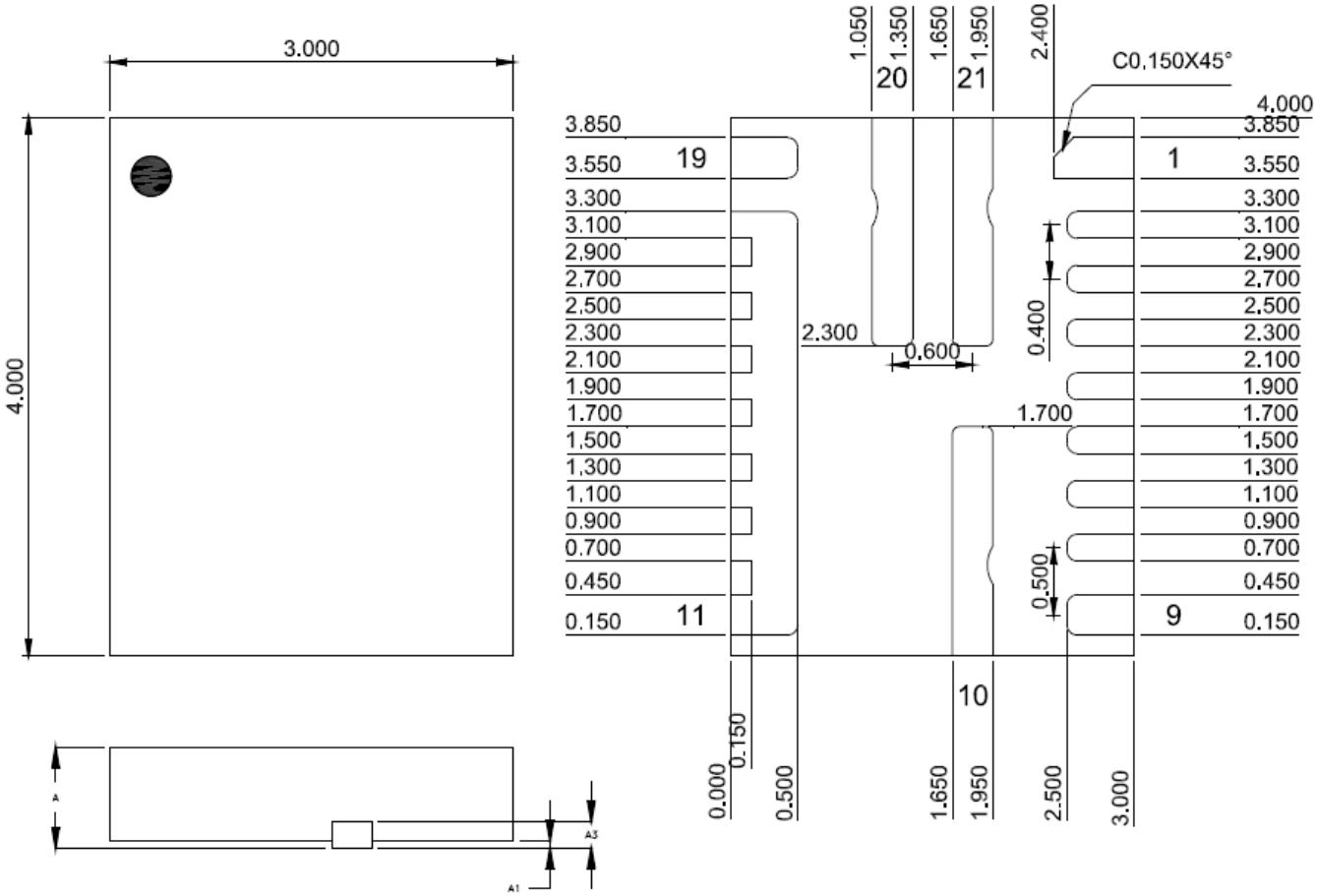


Figure 18 PCB Layout Guide

19 Outline Dimension

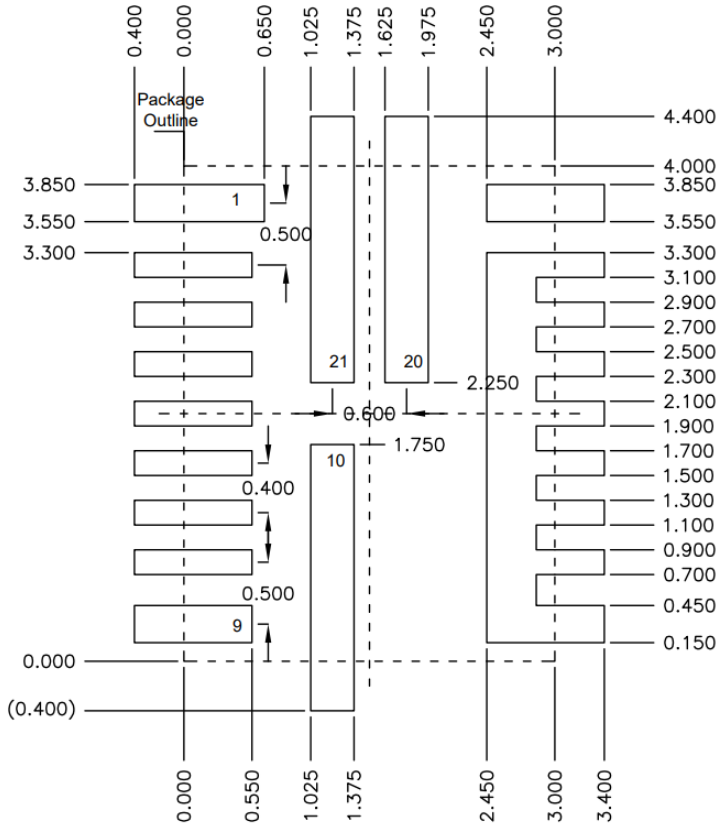


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 21T QFN 3x4 Package (FC)

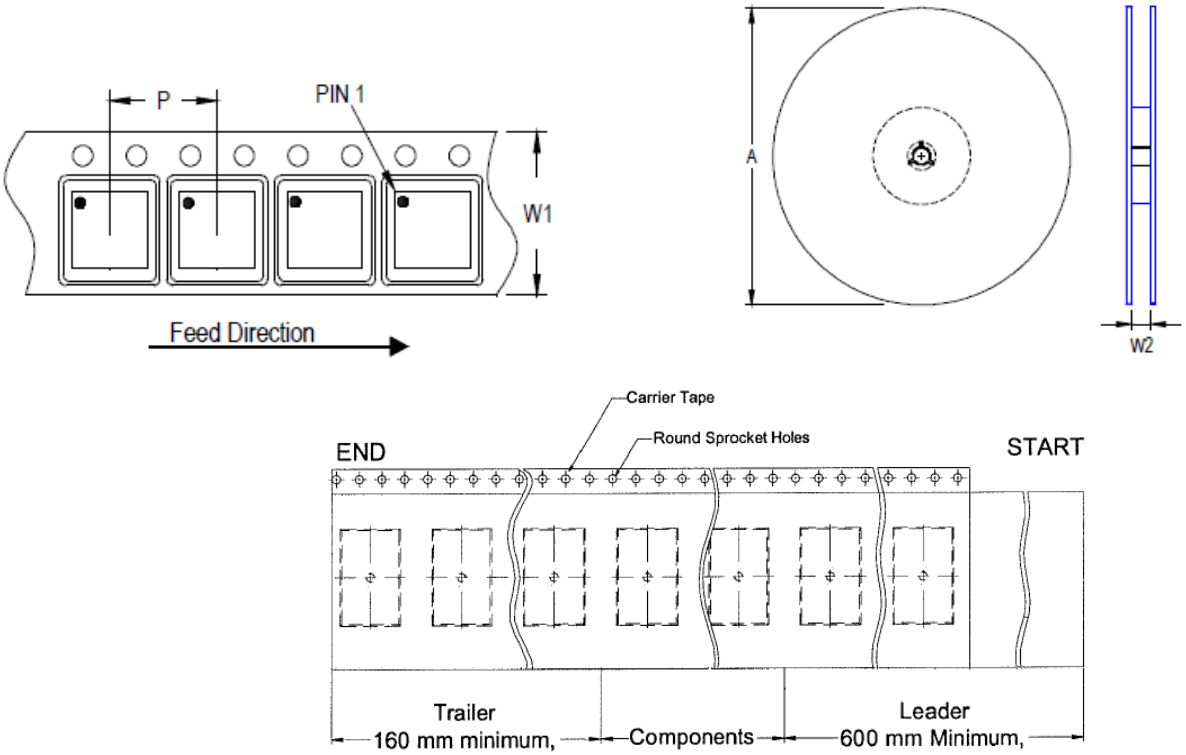
20 Footprint Information



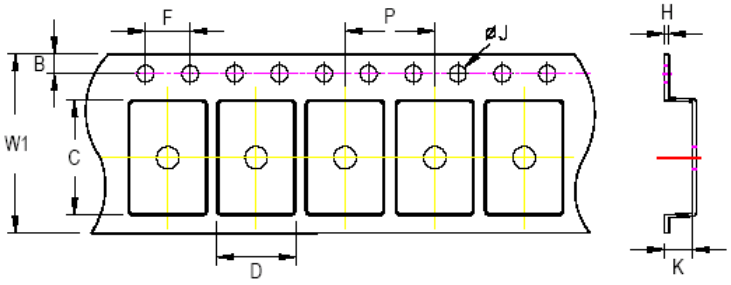
Package	Number of Pin	Tolerance
V/W/U/XQFN3x4-21T(FC)	21	±0.05

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x4	7"	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
00	2024/4/24	Final	Marking Information on P2 Electrical Characteristics on P9 Operation on P29