6A, 17V, ACOT® High-Efficiency Synchronous Step-Down Converter

1 General Description

The RTQ2807A is a high-performance, synchronous step-down converter that can deliver up to 6A output current with a wide input supply voltage range from 3.5V to 17V. The device integrates low R_{DSON} power MOSFETs, an accurate 0.9V ± 1% reference over the full operating junction temperature range, and an integrated diode for the bootstrap circuit, offering a very compact solution.

The RTQ2807A adopts an Advanced Constant On-Time (ACOT®) control architecture that provides excellent transient performance and reduces the count of external components. In steady states, the ACOT® can operate at nearly constant switching frequency across varying line, load, and output voltage ranges, which making the EMI filter design easier.

The device offers a variety of functions that enhance design flexibility. The selectable switching frequency, current limit level, and PWM operation modes make the RTQ2807A easy-to-use across a wide range of applications. An independent enable control input pin and a power-good indicator are also provided for simplified sequencing control. The device provides a programmable soft-start-time by an external capacitor connected to the SS/TR pin to control the inrush current during startup.

The RTQ2807A provides comprehensive protection functions, including input undervoltage lockout, output undervoltage protection, output overvoltage protection, overcurrent protection, and over-temperature protection. The RTQ2807A is available in a thermally enhanced WQFN-14TL 2x3 (FC) package. The recommended junction temperature range is from –40°C to 150°C.

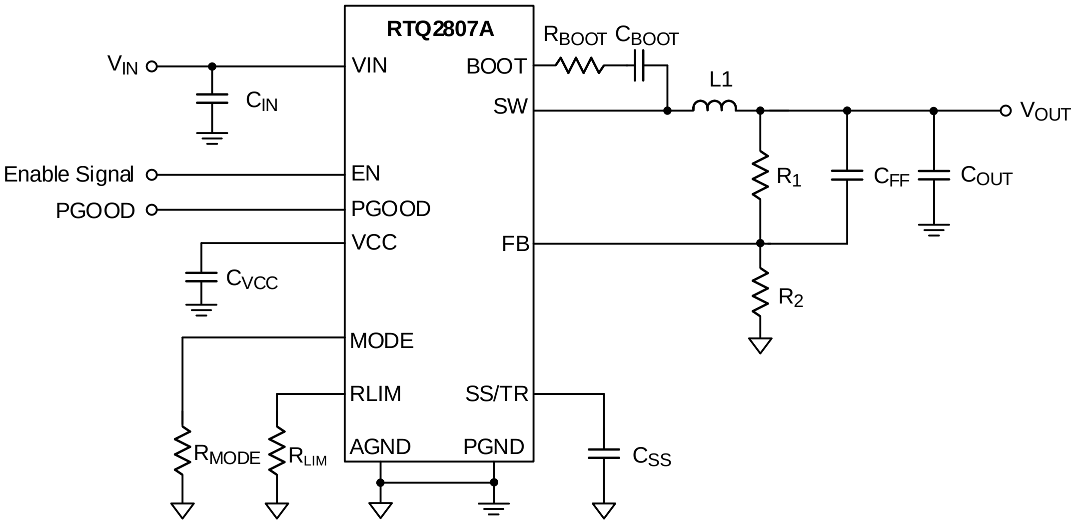
2 Features

- **Wide Input Voltage Range**
  - **2.7V to 17V with External 3.3V VCC Bias**
  - **3.5V to 17V with Internal VCC Bias**
- **Output Voltage from 0.9V to 5.5V**
- **0.9V ± 1% Voltage Reference Over a –40°C to 150°C Junction Temperature Range**
- **ACOT® Control for Excellent Transient Performance**
- **Stable with Ceramic Output Capacitors**
- **Selectable FCCM or PSM Operation at Light Load**
- **Selectable Operation Switching Frequency (660KHz/1100KHz/2200KHz)**
- **Latch-Off for OCP, OVP, UVP, UVLO, and OTP**
- **Power-Good Indicator**
- **Enable Control**
- **Programmable Soft-Start Time with a Default of 1.5ms**
- **Programmable Valley Current Limit Level**
- **Monotonic Start-Up into Pre-Biased Outputs**
- **Output Voltage Tracking**
- **Small 14-Lead WQFN (2x3) (FC) Package (Pin Pitch 0.5mm)**

3 Applications

- Servers, Storage, and Network Equipment
- Telecom Infrastructure
- Point of Load (POL) Power Modules
- High Density DC-DC Converters

4 Simplified Application Circuit



5 Ordering Information

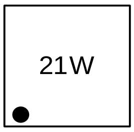
RTQ2807A □□

- Package Type
  QWF: WQFN-14TL 2x3 (FC) (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

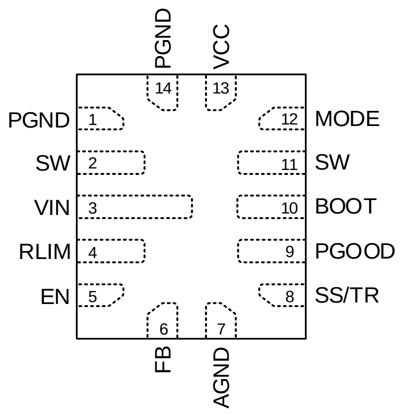


21: Product Code
W: Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)



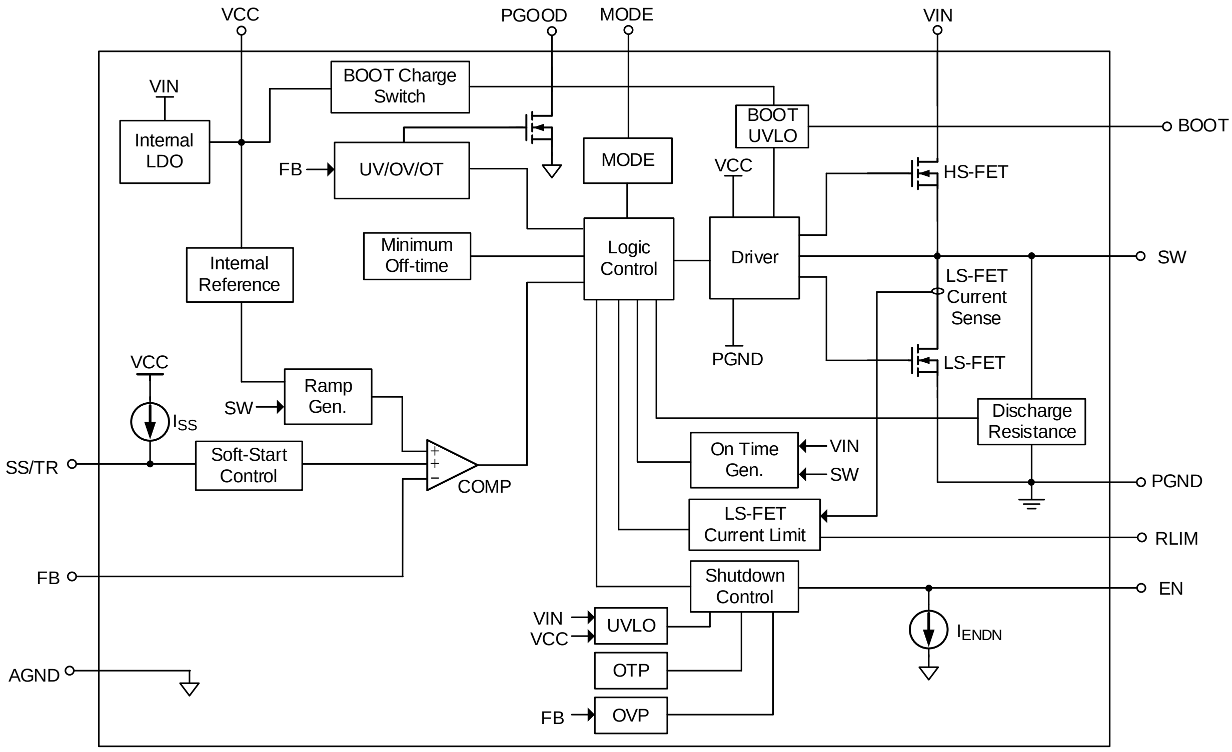
WQFN-14TL 2x3 (FC)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 14	PGND	The power GND of the controller circuit and the regulated output voltage. Use wide PCB traces for this connections.
2, 11	SW	Switch node. The output switching state between the high-side MOSFET and the low-side MOSFET of the power converter. Connect the SW pin to the external inductor and the bootstrap capacitor.
3	VIN	Power input voltage. Support 3.5V to 17V input voltage. It is suggested to place decoupling input capacitors as close to the VIN and PGND pins as possible.
4	RLIM	Valley current limit setup pin. Connect a resistor from this pin to AGND to set the valley current limit value. At least ±1% resistor is required.
5	EN	Enable control input. A logic-high signal enables the converter; however, a logic-low signal forces the device into shutdown mode. Do not leave this pin floating.
6	FB	Feedback voltage input. The pin is used to set the output voltage of the converter via a resistor divider. It is suggested to place the FB resistor divider as close to the FB pin as possible.
7	AGND	Analog ground. The reference point for the internal control circuit. AGND and PGND are connected with a short trace and at only one point to reduce circulating currents.
8	SS/TR	Soft-start and tracking control input. Connecting a ceramic capacitor from this pin to AGND programs the soft-start time. The internal minimum start-up time is 1.5ms (typical). A minimum capacitor of 10nF on this pin is required. For the tracking function, the device can track the pin voltage as the reference for tracking applications because the SS/TR pin voltage can override the internal reference voltage.
9	PGOOD	Open-drain, power-good indication output. It is pulled low if the feedback voltage is out of the power-good voltage threshold, when the IC shuts down from a fault state, when EN goes low, and before the soft-start is finished. A pull-up resistor of 10kΩ to 100kΩ is recommended if this function is used.
10	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor between this pin and SW pin.

Pin No.	Pin Name	Pin Function
12	MODE	Mode selection setup pin. The mode pin can be set to force continuous-conduction mode (FCCM) or pulse-skipping mode (PSM) for high light-load efficiency, and to set the operation switching frequency. A resistor with at least ±1% tolerance is required.
13	VCC	3V internal LDO output. An external DC voltage source 3.3V±5% can be connected to this pin to reduce power losses in the internal LDO and to supply both the internal circuitry and gate driver. Connect a 4.7μF, X7R ceramic capacitor as close to the VCC pin as possible. It is not recommended to connect VCC to supply other rails.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 1)

- VIN Voltage, V_{IN} --- –0.3V to 18V
- Enable Pin Voltage, V_{EN} -- –0.3V to 6V
- VIN to SW --- –0.3V to 18V
- SW Voltage, V_{SW} --- –0.3V to 18.3V

  V_{SW} (t ≤ 25ns) --- –5V to 25V
- BOOT Voltage, V_{BOOT} -- –0.3V to 24V
- BOOT to SW Voltage (V_{BOOT} – V_{SW}) --- –0.3V to 6V
- VCC --- –0.3V to 6V
- All Other Pins --- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature --- 170°C
- Storage Temperature Range --- –65°C to 170°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 2)

- ESD Susceptibility

  HBM (Human Body Model)-- 2kV

Note 2. The device is not guaranteed to function outside its operating conditions.

12 Recommended Operating Conditions

(Note 3)

- VIN with Internal VCC Bias, V_{IN}--- 3.5V to 17V
- VIN with External 3.3V VCC Bias, V_{IN}--- 2.7V to 17V
- Output Voltage --- 0.9V to 5.5V
- Enable Voltage, V_{EN}--- 3.6V
- External VCC bias, V_{CC_EXT} --- 3.12V to 3.6V
- Junction Temperature Range--- –40°C to 150°C

Note 3. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

13 Thermal Information

(Note 4 and Note 5)

Thermal parameter		WQFN-14TL 2x3 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	64.78	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	45.53	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	3.97	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	37.88	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.487	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.64	°C/W

Note 4. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 92.2 mm x 81.4 mm; furthermore, all layers with 2 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 5. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

14 Electrical Characteristics

(V_{IN} = 12V, T_J = –40°C to 150°C, typical values are at T_J = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	5	15	µA
Supply Current (Non-Switching)	I_{Q_NSW}	V_{EN} = 2V, non-switching	--	1050	1300	µA
Logic Threshold						
EN Input Voltage Rising Threshold	V_{EN_R}		1.17	1.22	1.27	V
EN Threshold Hysteresis	V_{EN_HYS}		--	200	--	mV
EN Pull-Down Current	I_{PD_EN}	V_{EN} = 2V	--	0.5	--	µA
Reference Voltage						
Internal Voltage Reference	V_{REF}	T_J = –40°C to +150°C	0.891	0.9	0.909	V
		T_J = 0°C to +70°C	0.895	0.9	0.905	V
Soft-Start and Tracking						
Internal Soft-Start Time	t_{SS}	T_J = 25°C, C_{SS} = 10nF, V_{OUT} is 0% to 100% (Note 6)	--	1.5	--	ms
SS/TR Source Current	I_{SS/TR_sr}	$V_{SS/TR}$ = 0V	--	15	--	µA
SS/TR Sink Current	I_{SS/TR_sk}	$V_{SS/TR}$ = 1V	--	6	--	µA
MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}	T_J = 25°C, V_{CC} = 3V	--	22.6	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	T_J = 25°C, V_{CC} = 3V	--	8.1	--	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit						
Current Limit Voltage Threshold	V_{LIM}	Valley current	1.15	1.2	1.25	V
I_{CS} to I_{OUT} Ratio	G_{CS} (I_{CS}/I_{OUT})	$I_{OUT} \geq 2A$	36	40	44	μA/A
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	Valley current, R_{LIM} = 3.75kΩ	--	8	--	A
Low-Side Switch Negative Current Limit	I_{LIM_NEG}	Valley current	--	–8	--	A
Switching Frequency						
Switching Frequency	f_{SW}	R_{MODE} = 60.4kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 1.8V	530	660	790	kHz
		R_{MODE} = 0Ω, I_{OUT} = 0A, FCCM, V_{OUT} = 1.8V	935	1100	1265	
		R_{MODE} = 30.1kΩ, I_{OUT} = 0A, FCCM, V_{OUT} = 3.3V	1870	2200	2530	
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	T_J = 25°C (Note 6)	--	--	50	ns
Minimum Off-Time	t_{OFF_MIN}	T_J = 25°C (Note 6)	--	--	180	ns
UVLO						
Input Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising, V_{CC_EXT} = 3.3V	2.1	2.4	2.7	V
Input Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} hysteresis	--	550	--	mV
LDO Output						
LDO Output Voltage	V_{CC}	I_{VCC} = 1mA	2.88	3.00	3.18	V
VCC Undervoltage Lockout Rising Threshold	$V_{CC\_UVLO\_R}$	V_{CC} rising	2.65	2.8	2.95	V
VCC Undervoltage Lockout Hysteresis	$V_{CC\_UVLO\_HYS}$	V_{CC} hysteresis	--	300	--	mV
VCC Load Regulation		T_J = 25°C, I_{VCC} = 25mA	--	0.5	--	%
LDO Output Current Limit	I_{LIM_LDO}		--	105	--	mA
Output Overvoltage and Undervoltage Protections						
Output Undervoltage Protection Threshold	V_{UVP}	UVP detect	77	80	83	%V_{REF}
Output Overvoltage Protection Threshold	V_{OVP}	OVP detect	113	116	119	%V_{REF}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power-Good						
Power-Good Voltage Threshold	V_{TH_PGLH1}	V_{FB} rising threshold, PGOOD from low to high (GOOD)	89.5	91.5	95.5	$\%V_{REF}$
	V_{TH_PGHL1}	V_{FB} rising threshold, PGOOD from high to low (FAULT)	113	116	119	
	V_{TH_PGLH2}	V_{FB} falling threshold, PGOOD from low to high (GOOD)	102	106	109	
	V_{TH_PGHL2}	V_{FB} falling threshold, PGOOD from high to low (FAULT)	77	80	83	
Power-Good Output Low-Level Voltage	$V_{PG\_L\_100}$	T_J = 25°C, V_{IN} & V_{CC} & V_{EN} = 0V, PGOOD Pull up to 3.3V bias with 100k resister	--	650	850	mV
	$V_{PG\_L\_10}$	T_J = 25°C, V_{IN} & V_{CC} & V_{EN} = 0V, PGOOD Pull up to 3.3V bias with 10k resister	--	800	1000	
Power-Good Delay	t_{PGDLY}	T_J = 25°C, V_{TH_PGLH1} and V_{TH_PGLH2}, PGOOD from low to high (GOOD)	0.5	0.8	1.1	ms
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		150	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Output Discharge Resistor						
Output Discharge Resistor	R_{DISCHG}	V_{EN} = 0V or Protection	--	80	--	Ω

Note 6. Guaranteed by design.

15 Typical Application Circuit

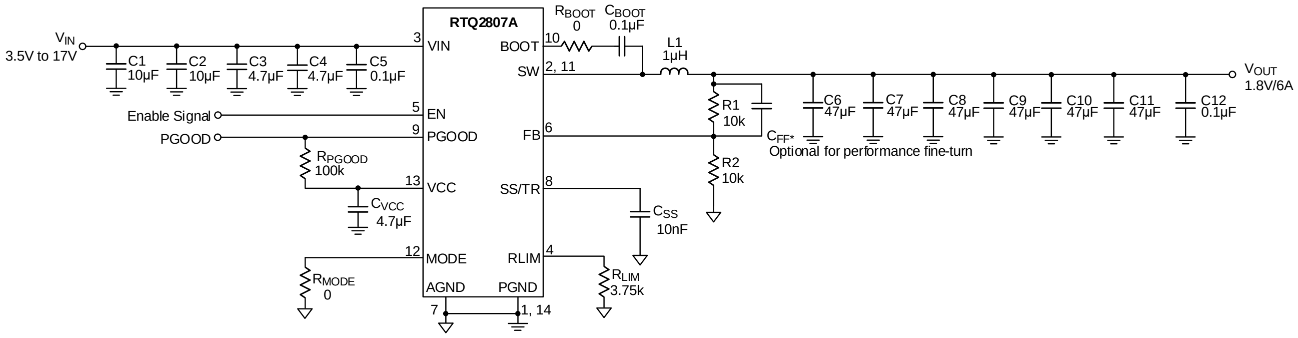


Table 1. Suggested Component Selection for the Application of 660kHz

VOUT(V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)	COUT_MIN (μF)	COUT_TYPICAL (μF)	CFF (pF)
0.9	0	10	0.68	174	282	NC
1.8	10		1.5	174	282	330
3.3	26.7		2.2	174	282	220
5	45.3		3.3	174	282	220

Table 2. Suggested Component Selection for the Application of 1100kHz

VOUT(V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)	COUT_MIN (μF)	COUT_TYPICAL (μF)	CFF (pF)
0.9	0	10	0.47	174	282	NC
1.8	10		1	174	282	330
3.3	26.7		1.5	174	282	220
5	45.3		2.2	174	282	220

Table 3. Suggested Component Selection for the Application of 2200kHz

VOUT(V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)	COUT_MIN (μF)	COUT_TYPICAL (μF)	CFF (pF)
0.9	0	10	0.22	174	282	NC
1.8	10		0.47	174	282	330
3.3	26.7		0.68	174	282	220
5	45.3		1	174	282	220

Table 4. Suggested Inductors for Typical Application Circuit

Inductance (μH)	Part No.	ISAT (A)	DCR (mΩ)	Dimensions (mm)	Component Supplier
0.22	744373460022	54.3	2.8	7.3 x 6.6 x 2.8	WE-LHMI
0.33	744373460033	47	3.9	7.3 x 6.6 x 2.8	WE-LHMI
0.47	744373460047	37.8	4.2	7.3 x 6.6 x 2.8	WE-LHMI
0.68	744373460068	31.6	5.5	7.3 x 6.6 x 2.8	WE-LHMI
1	74437346010	29	10	7.3 x 6.6 x 2.8	WE-LHMI
1.5	74437346015	27.6	15	7.3 x 6.6 x 2.8	WE-LHMI
2.2	74437346022	19.1	20	7.3 x 6.6 x 2.8	WE-LHMI
3.3	744311330	11	17.2	7 x 6.9 x 3.8	WE-HCI

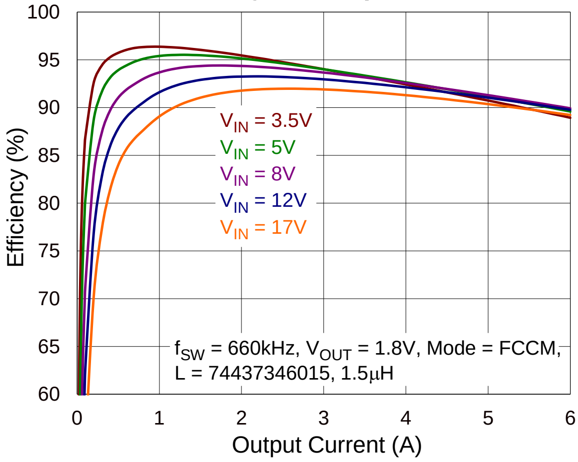
Table 5. Suggested Capacitors for Typical Application Circuit

Capacitance (μF)	Part No.	Case Size	Component Supplier
47	GRM31CR60J476ME19L	1206	Murata
10	GRM31CR71E106KA12L	1206	Murata
4.7	GRM31CR71H475KA12	1206	Murata
0.1	0402B104K500CT	0603	WALSIN

Note 7. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

16 Typical Operating Characteristics

Efficiency vs. Output Current



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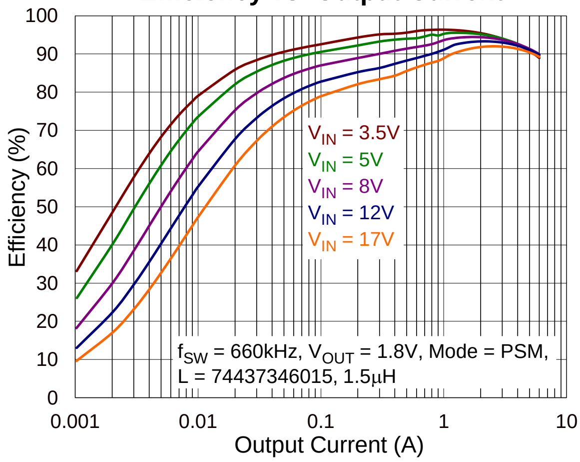

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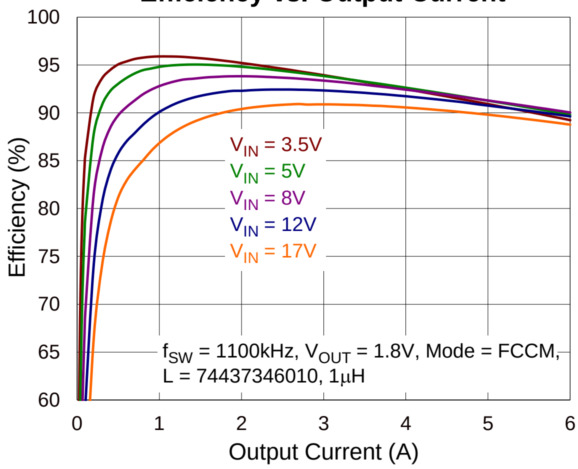

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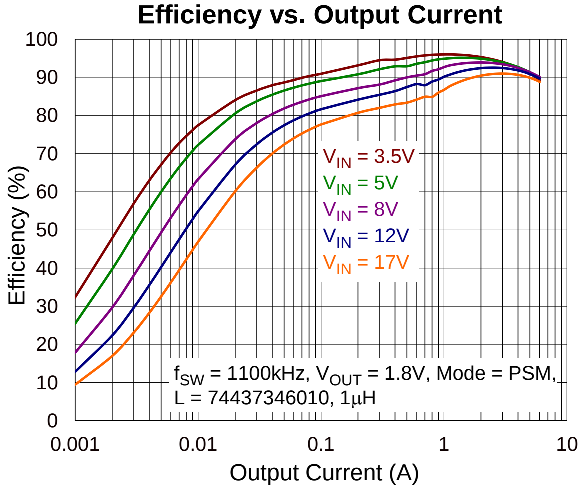

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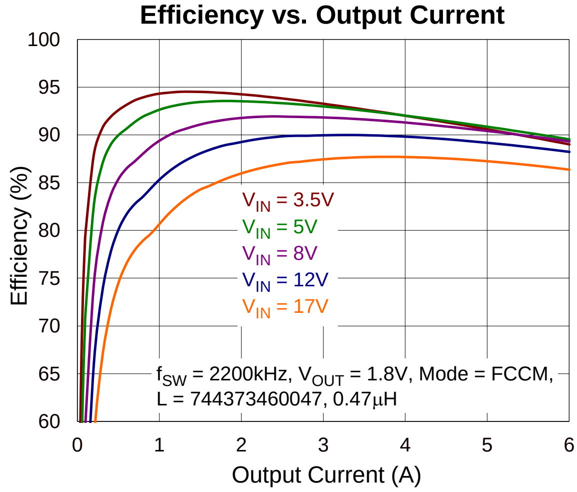

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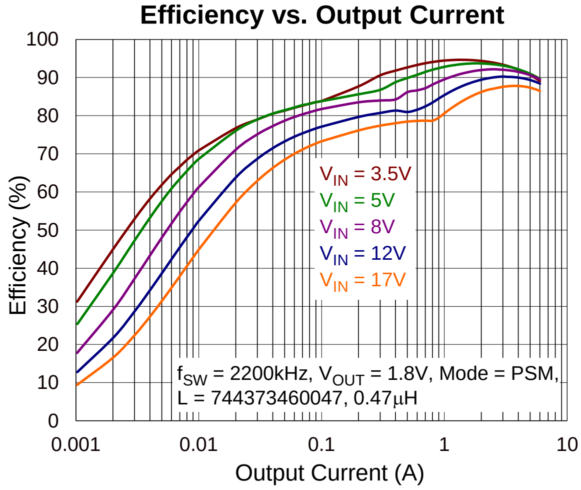

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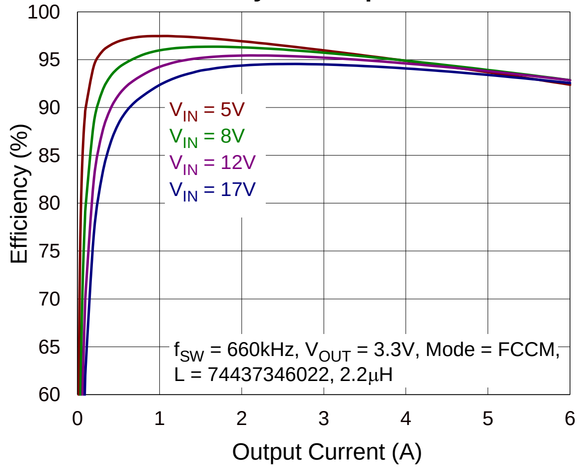

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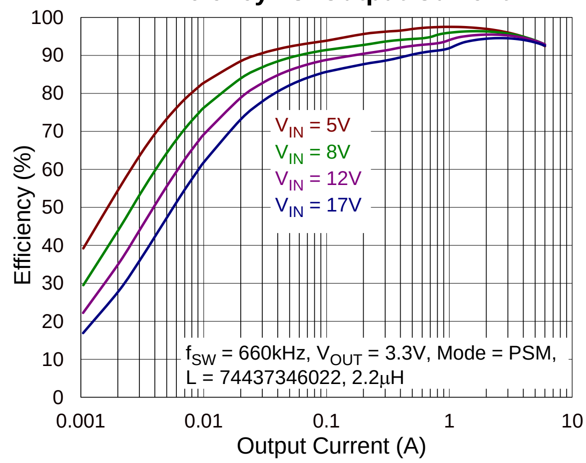

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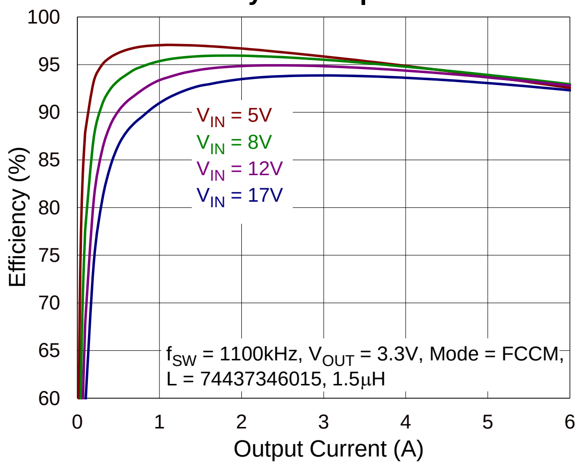
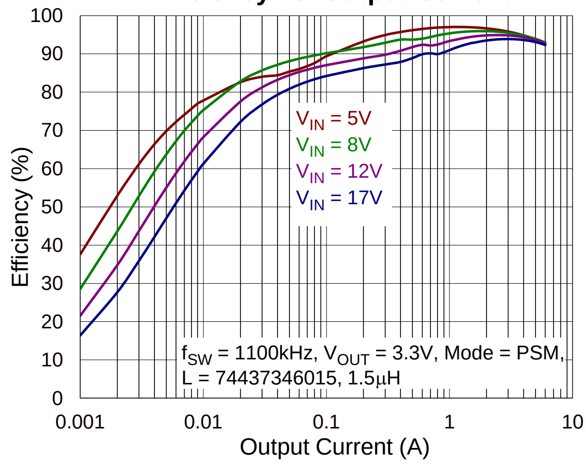


Efficiency vs. Output Current



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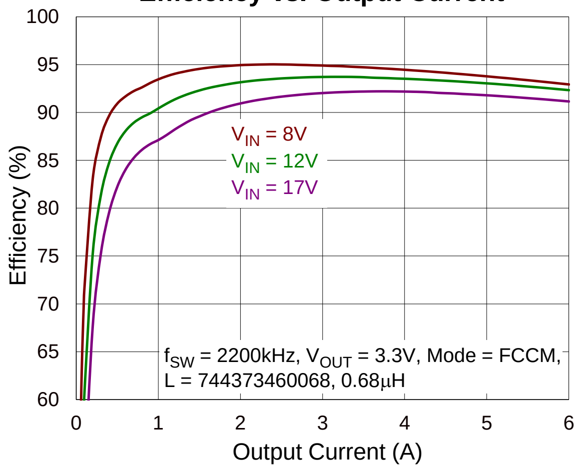

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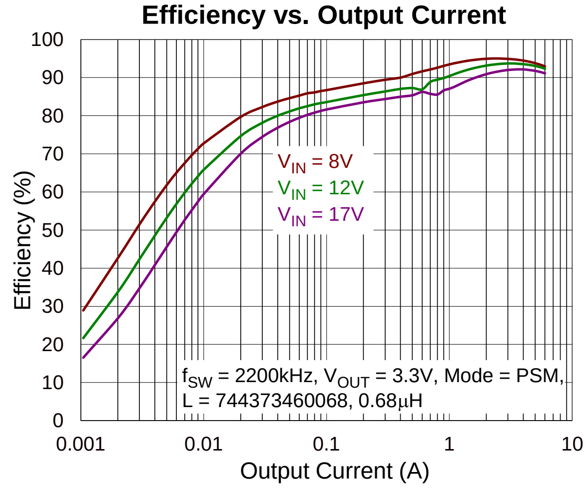
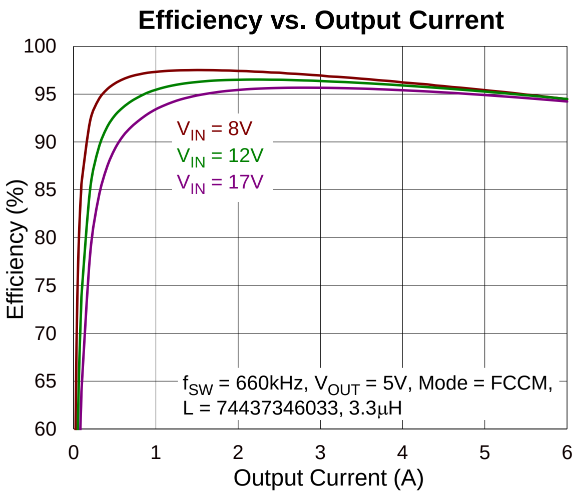
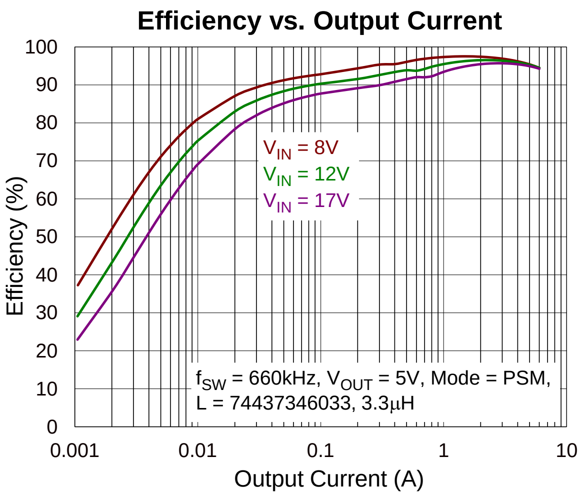
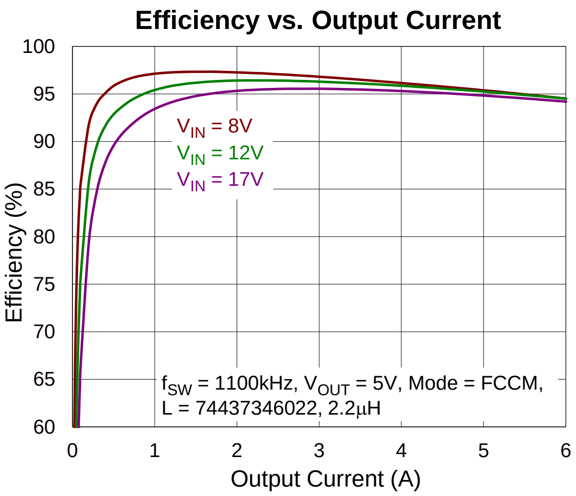
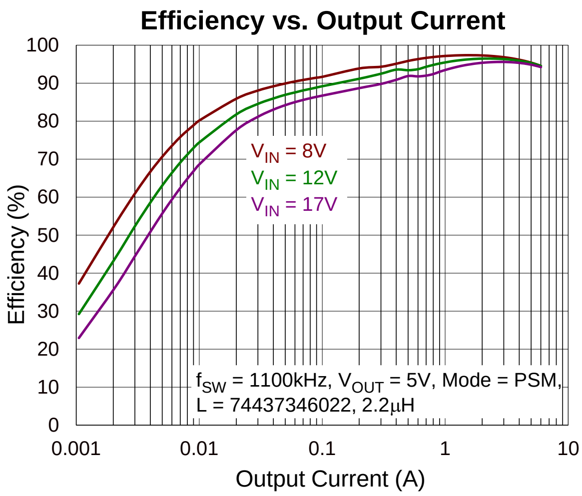
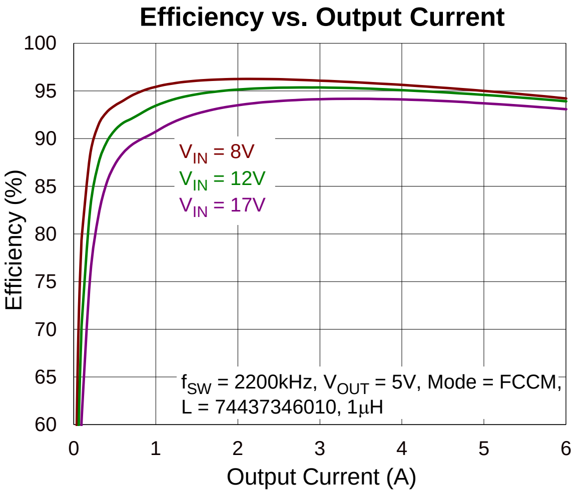


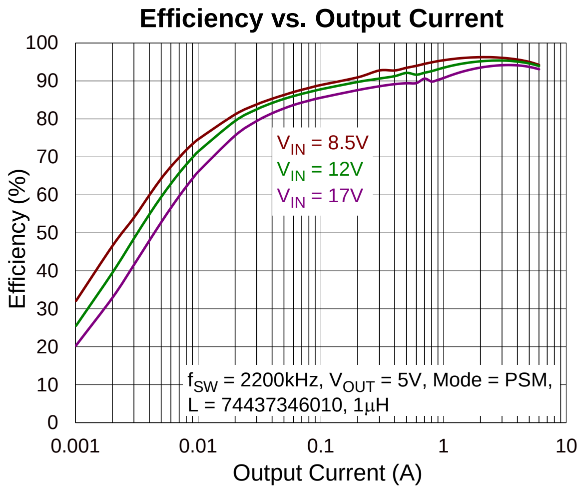

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VIN = 8V
VIN = 12V
VIN = 17V
fSW = 660kHz, VOUT = 5V, Mode = FCCM,
L = 74437346033, 3.3μH

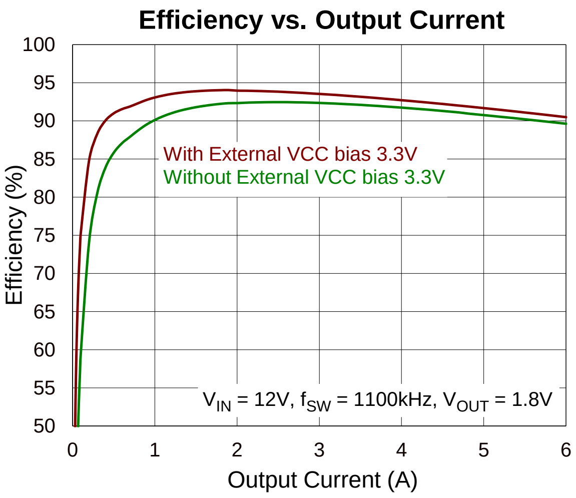

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VIN = 8V
VIN = 12V
VIN = 17V
fSW = 660kHz, VOUT = 5V, Mode = PSM,
L = 74437346033, 3.3μH

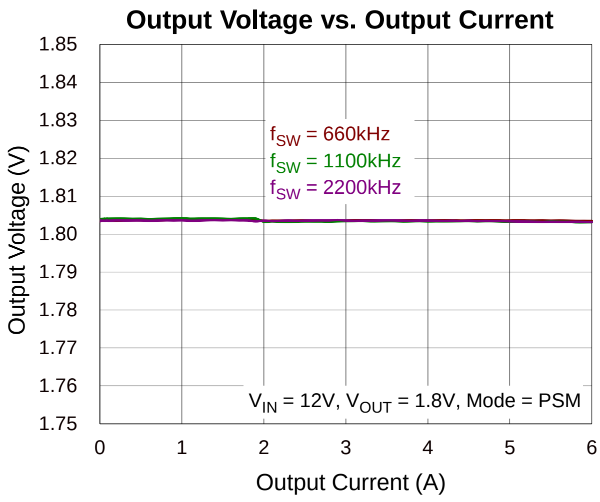

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VIN = 8V
VIN = 12V
VIN = 17V
fSW = 1100kHz, VOUT = 5V, Mode = FCCM,
L = 74437346022, 2.2μH

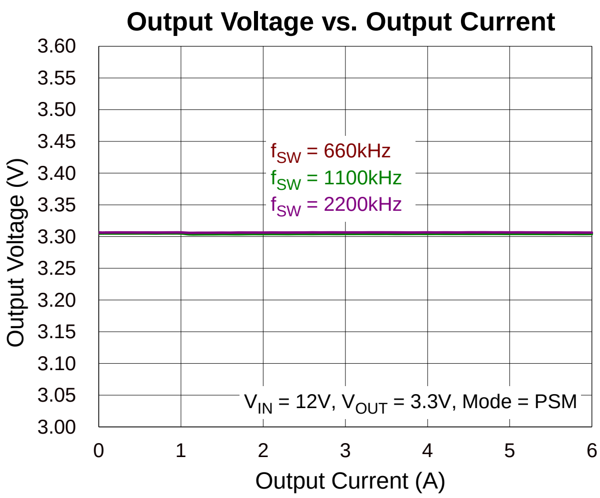

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VIN = 8V
VIN = 12V
VIN = 17V
fSW = 1100kHz, VOUT = 5V, Mode = PSM,
L = 74437346022, 2.2μH

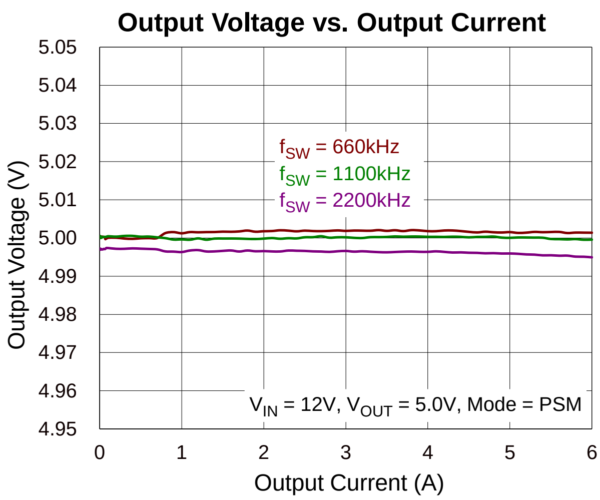

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VIN = 8V
VIN = 12V
VIN = 17V
fSW = 2200kHz, VOUT = 5V, Mode = FCCM,
L = 74437346010, 1μH

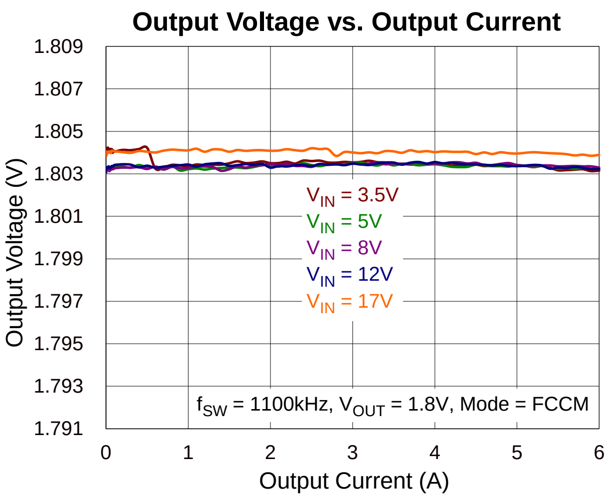

Efficiency vs. Output Current
Efficiency (%)
Output Current (A)
VIN = 8.5V
VIN = 12V
VIN = 17V
fSW = 2200kHz, VOUT = 5V, Mode = PSM,
L = 74437346010, 1μH

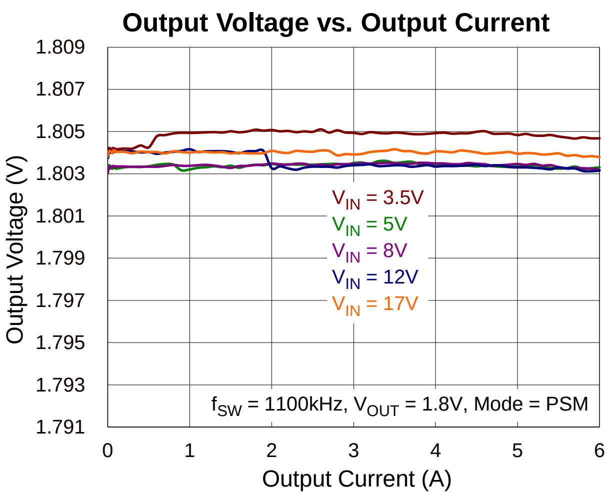

Efficiency vs. Output Current
With External VCC bias 3.3V
Without External VCC bias 3.3V
V_{IN} = 12V, f_{SW} = 1100kHz, V_{OUT} = 1.8V
Efficiency (%)
Output Current (A)


Output Voltage vs. Output Current
f_{SW} = 660kHz
f_{SW} = 1100kHz
f_{SW} = 2200kHz
V_{IN} = 12V, V_{OUT} = 1.8V, Mode = PSM
Output Voltage (V)
Output Current (A)

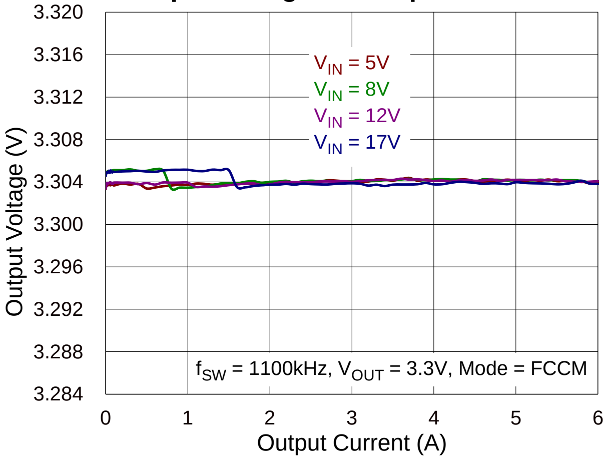

Output Voltage vs. Output Current
f_{SW} = 660kHz
f_{SW} = 1100kHz
f_{SW} = 2200kHz
V_{IN} = 12V, V_{OUT} = 3.3V, Mode = PSM
Output Voltage (V)
Output Current (A)


Output Voltage vs. Output Current
f_{SW} = 660kHz
f_{SW} = 1100kHz
f_{SW} = 2200kHz
V_{IN} = 12V, V_{OUT} = 5.0V, Mode = PSM
Output Voltage (V)
Output Current (A)

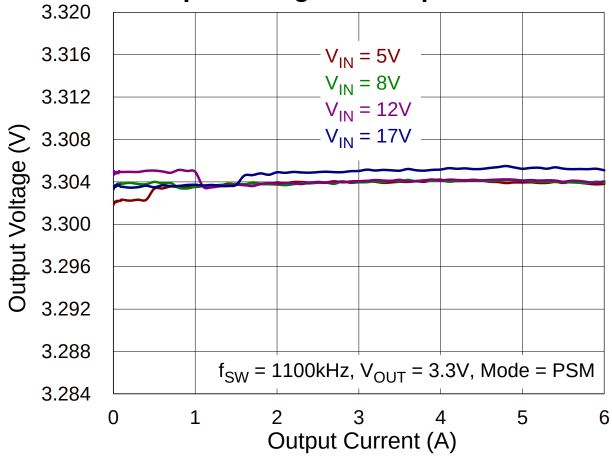

Output Voltage vs. Output Current
V_{IN} = 3.5V
V_{IN} = 5V
V_{IN} = 8V
V_{IN} = 12V
V_{IN} = 17V
f_{SW} = 1100kHz, V_{OUT} = 1.8V, Mode = FCCM
Output Voltage (V)
Output Current (A)


Output Voltage vs. Output Current
V_{IN} = 3.5V
V_{IN} = 5V
V_{IN} = 8V
V_{IN} = 12V
V_{IN} = 17V
f_{SW} = 1100kHz, V_{OUT} = 1.8V, Mode = PSM
Output Voltage (V)
Output Current (A)

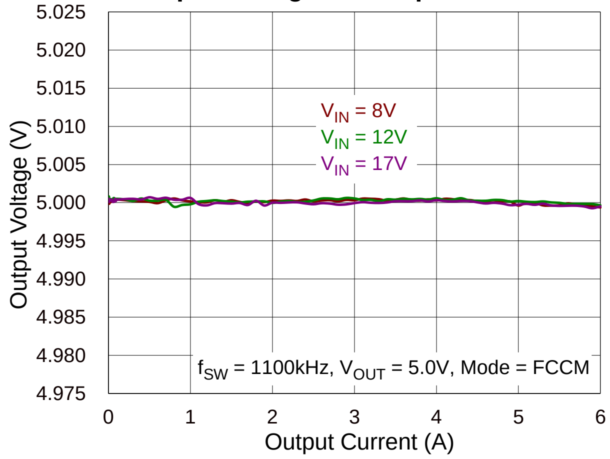
Output Voltage vs. Output Current



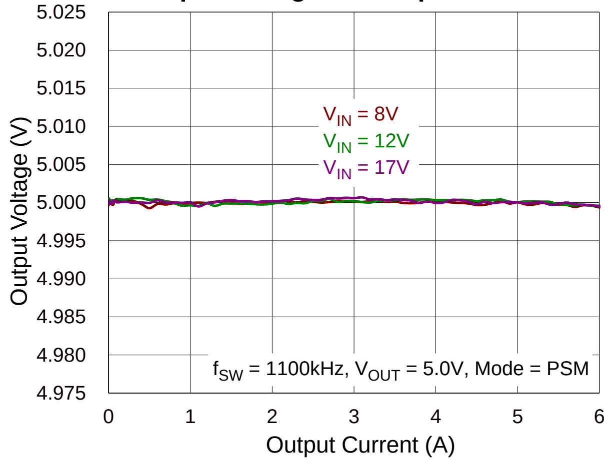
Output Voltage vs. Output Current



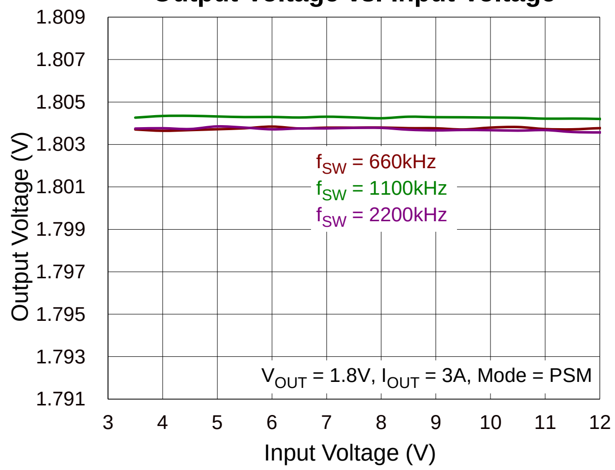
Output Voltage vs. Output Current



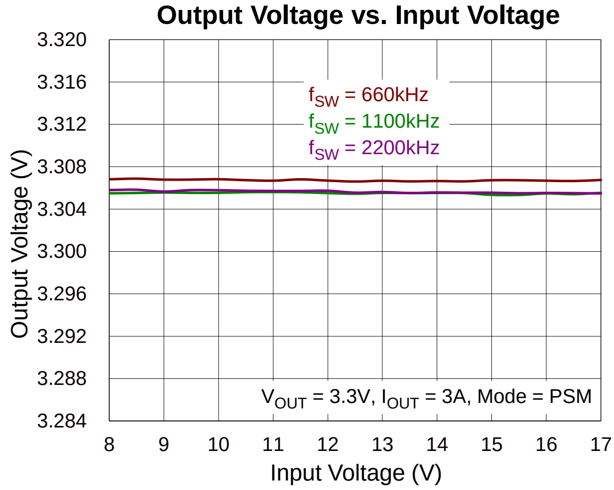
Output Voltage vs. Output Current

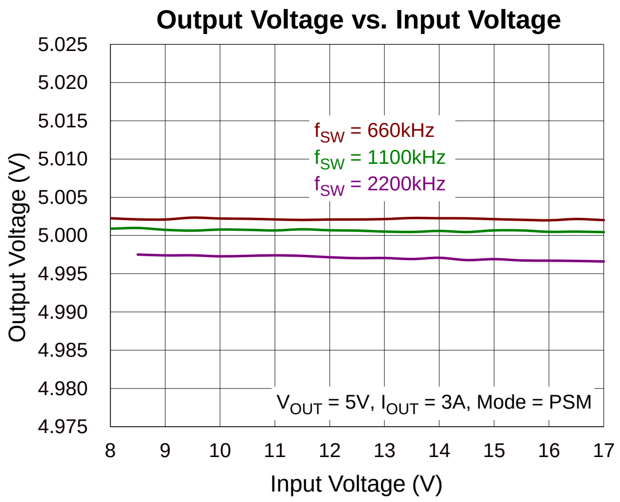


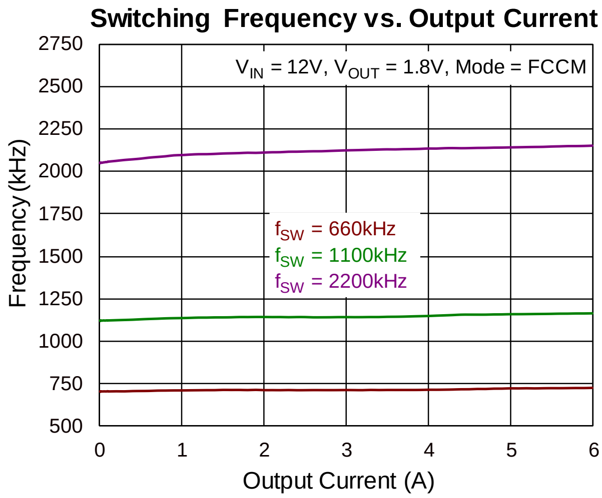
Output Voltage vs. Input Voltage

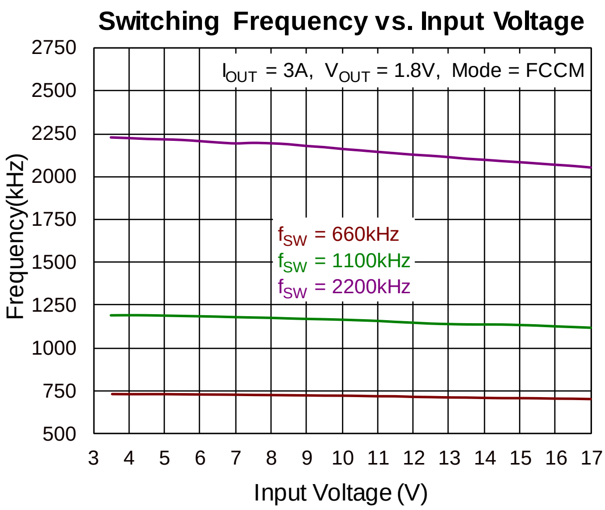


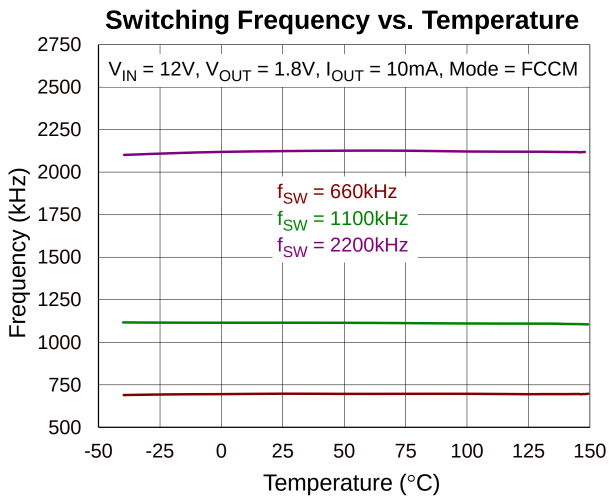
Output Voltage vs. Input Voltage

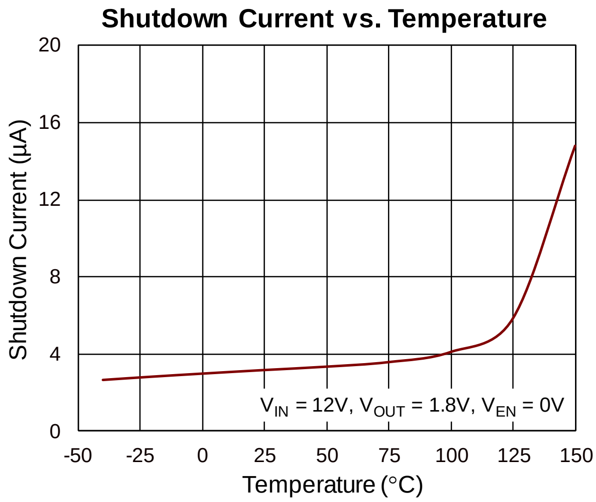


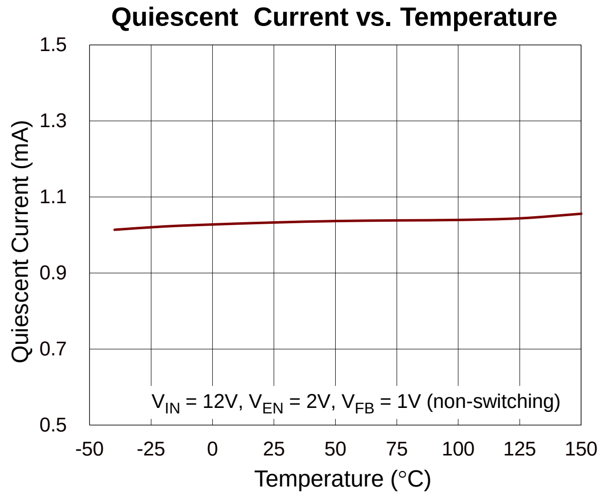

Output Voltage vs. Input Voltage
Output Voltage (V)
5.025
5.020
5.015
5.010
5.005
5.000
4.995
4.990
4.985
4.980
4.975
fSW = 660kHz
fSW = 1100kHz
fSW = 2200kHz
VOUT = 5V, IOUT = 3A, Mode = PSM
8 9 10 11 12 13 14 15 16 17
Input Voltage (V)


Switching Frequency vs. Output Current
Frequency (kHz)
2750
2500
2250
2000
1750
1500
1250
1000
750
500
VIN = 12V, VOUT = 1.8V, Mode = FCCM
fSW = 660kHz
fSW = 1100kHz
fSW = 2200kHz
0 1 2 3 4 5 6
Output Current (A)

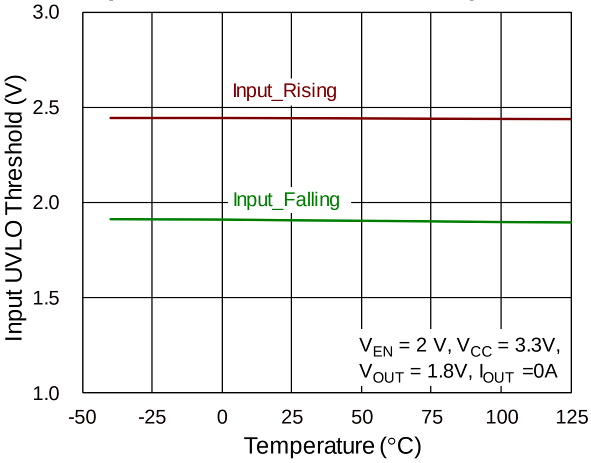

Switching Frequency vs. Input Voltage
Frequency(kHz)
2750
2500
2250
2000
1750
1500
1250
1000
750
500
IOUT = 3A, VOUT = 1.8V, Mode = FCCM
fSW = 660kHz
fSW = 1100kHz
fSW = 2200kHz
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
Input Voltage (V)


Switching Frequency vs. Temperature
Frequency (kHz)
2750
2500
2250
2000
1750
1500
1250
1000
750
500
VIN = 12V, VOUT = 1.8V, IOUT = 10mA, Mode = FCCM
fSW = 660kHz
fSW = 1100kHz
fSW = 2200kHz
-50 -25 0 25 50 75 100 125 150
Temperature (°C)

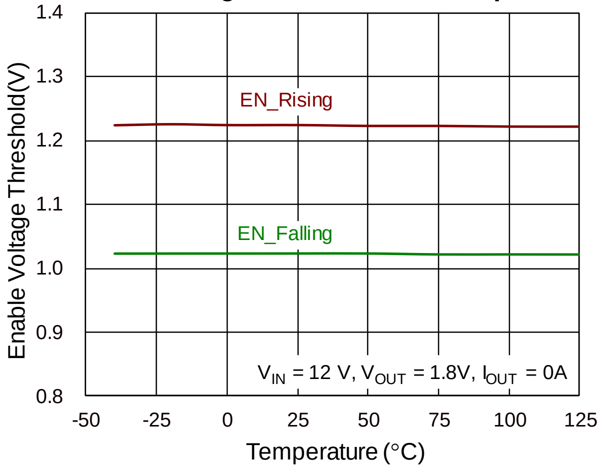

Shutdown Current vs. Temperature
Shutdown Current (μA)
20
16
12
8
4
0
VIN = 12V, VOUT = 1.8V, VEN = 0V
-50 -25 0 25 50 75 100 125 150
Temperature (°C)


Quiescent Current vs. Temperature
Quiescent Current (mA)
1.5
1.3
1.1
0.9
0.7
0.5
VIN = 12V, VEN = 2V, VFB = 1V (non-switching)
-50 -25 0 25 50 75 100 125 150
Temperature (°C)

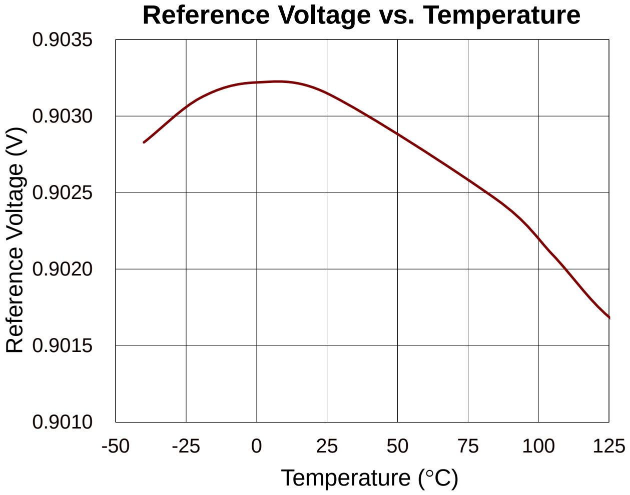
Input UVLO Threshold vs. Temperature



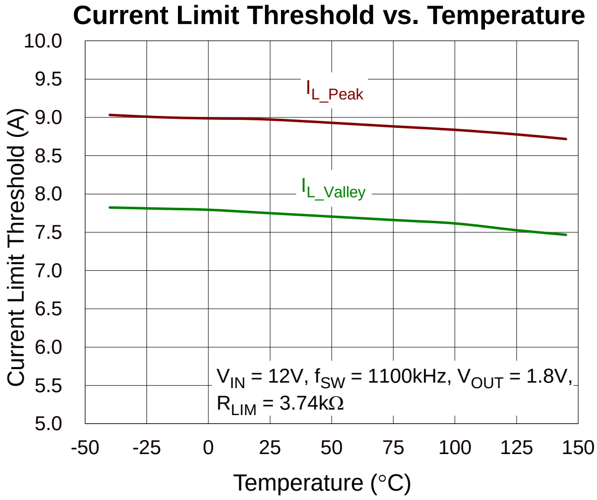
Enable Voltage Threshold vs. Temperature



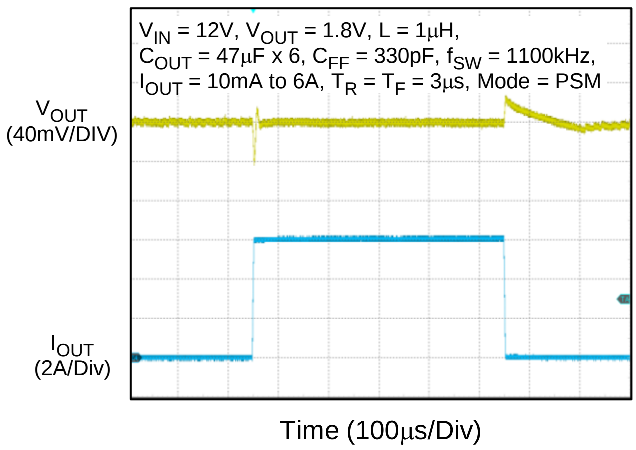
Reference Voltage vs. Temperature



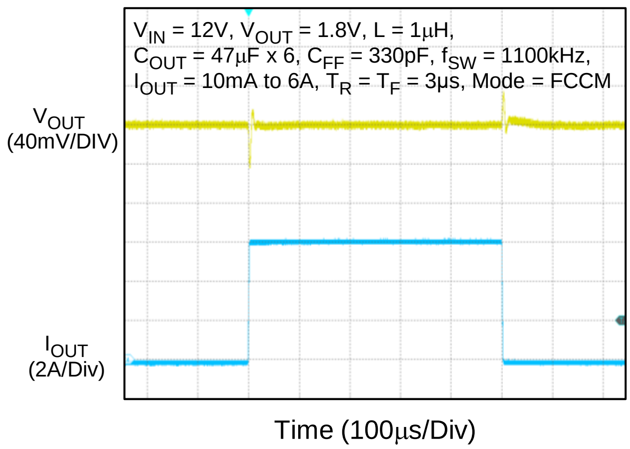
Current Limit Threshold vs. Temperature



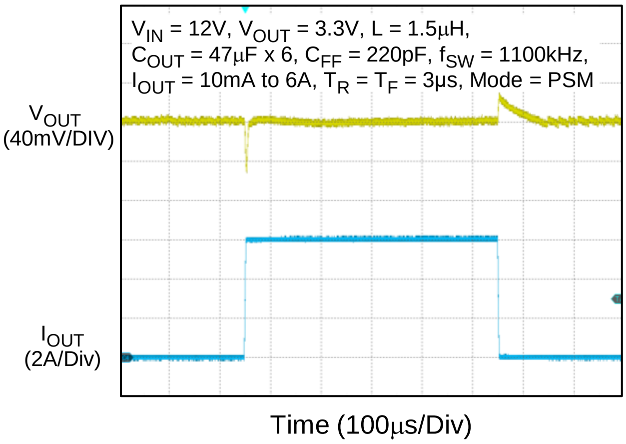
Transient Response



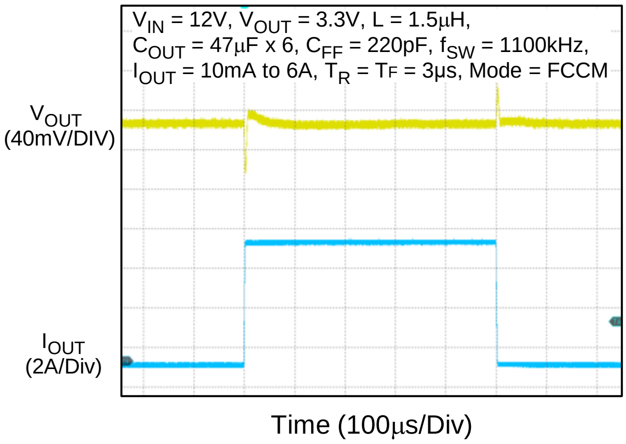
Transient Response



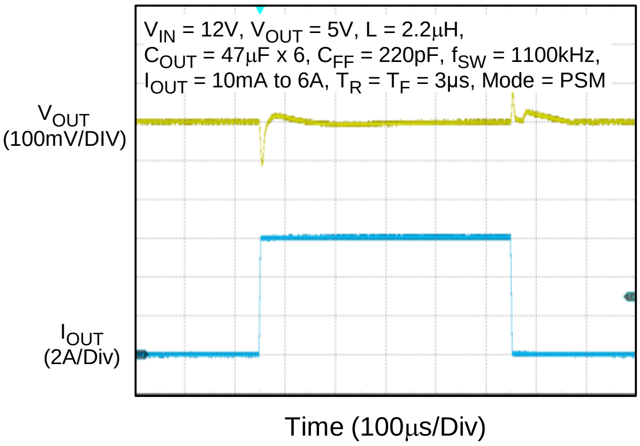
Transient Response



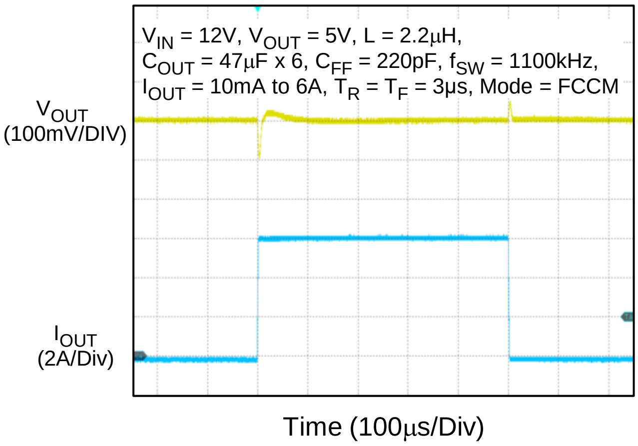
Transient Response



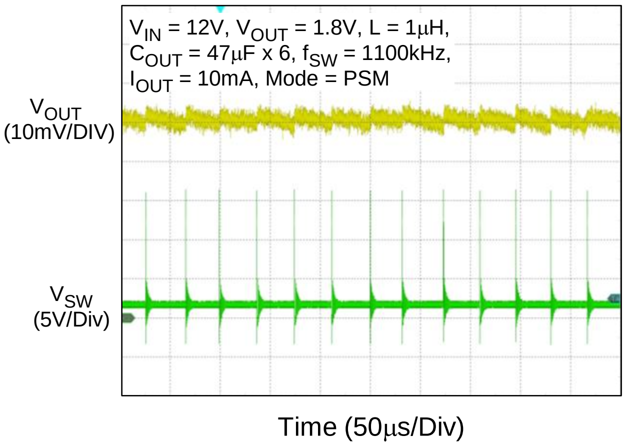
Transient Response



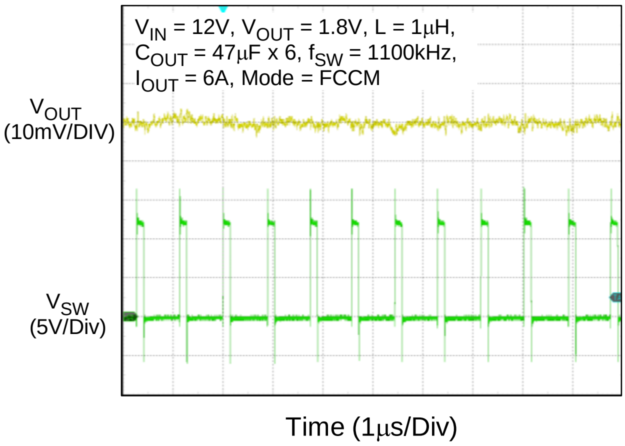
Transient Response



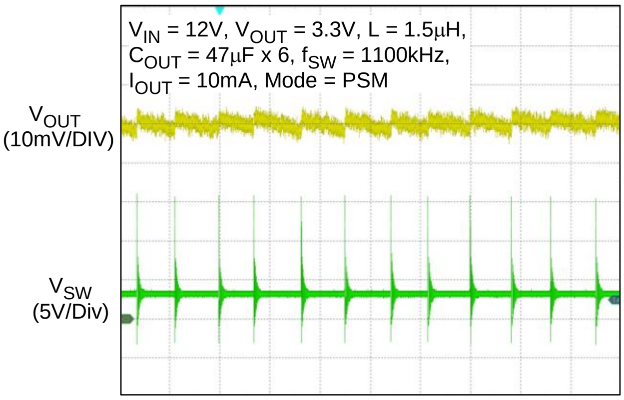
Output Ripple Voltage



Output Ripple Voltage

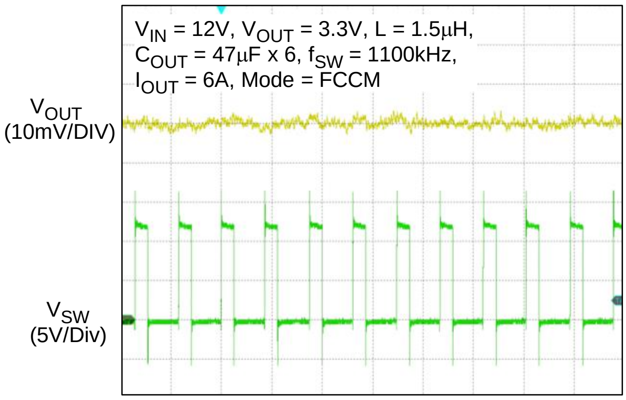


Output Ripple Voltage



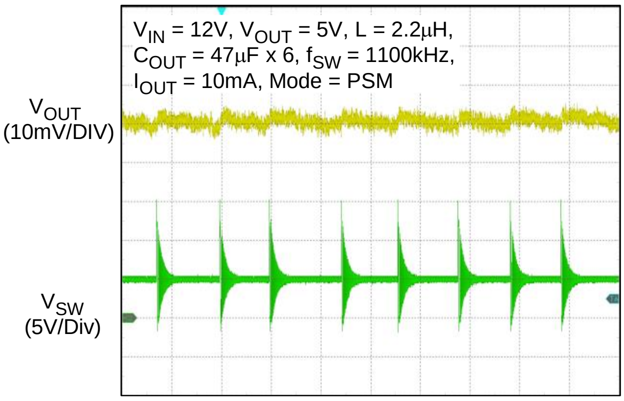
Time (40μs/Div)

Output Ripple Voltage



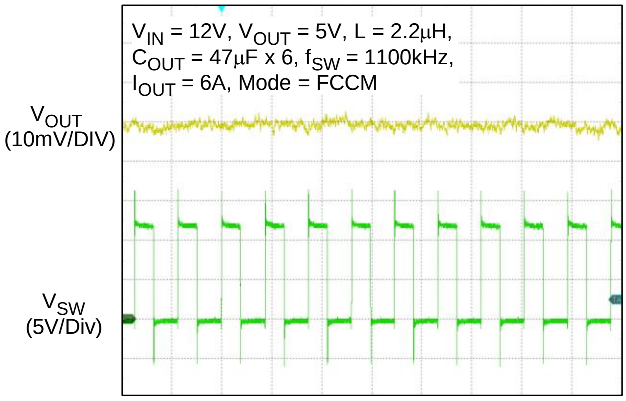
Time (1μs/Div)

Output Ripple Voltage



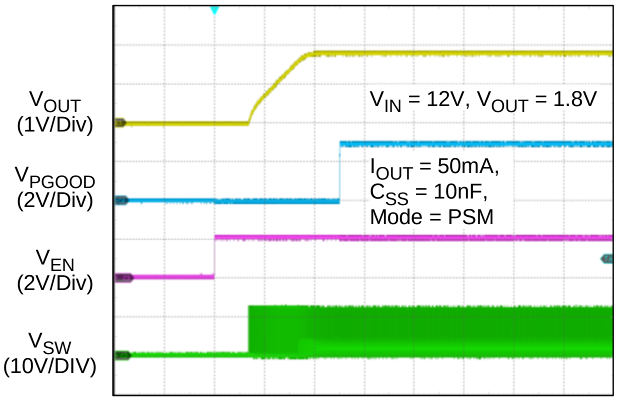
Time (20μs/Div)

Output Ripple Voltage



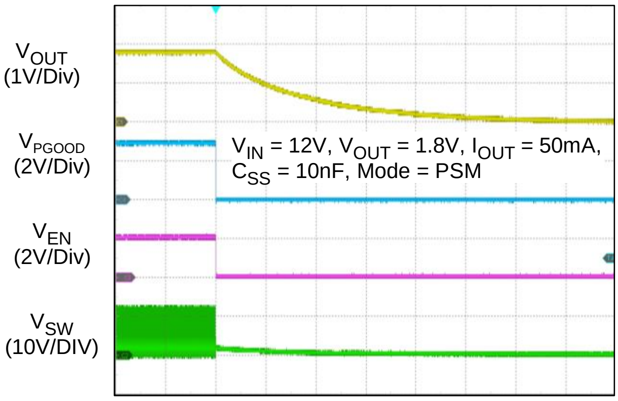
Time (1μs/Div)

Power On from EN



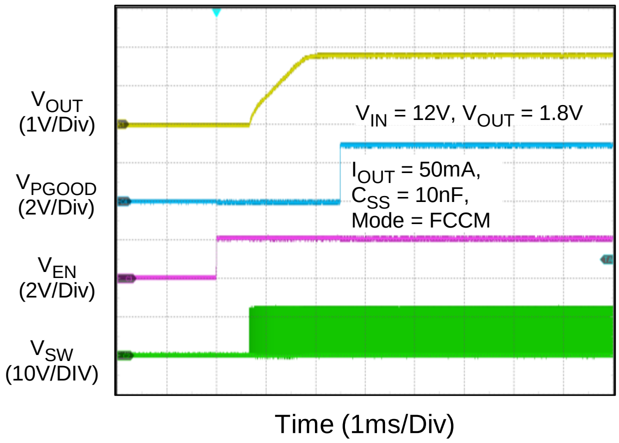
Time (1ms/Div)

Power Off from EN

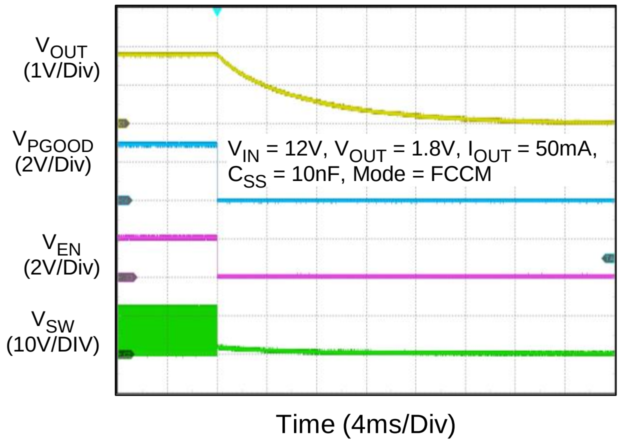


Time (4ms/Div)

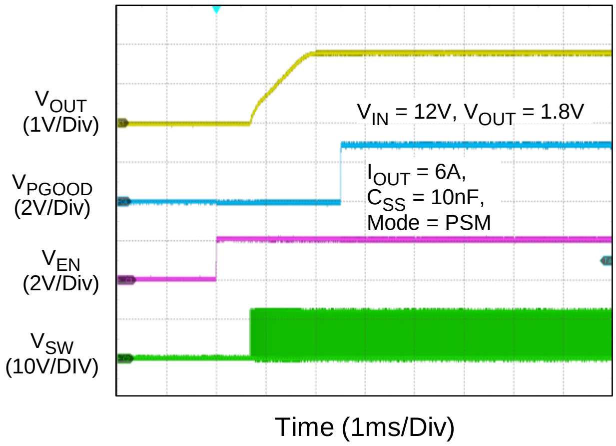
Power On from EN



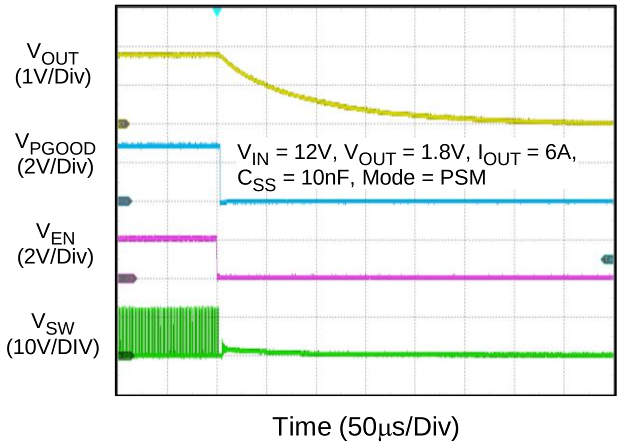
Power Off from EN



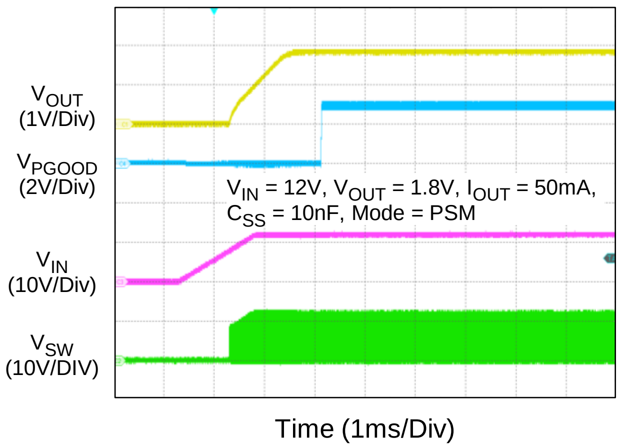
Power On from EN



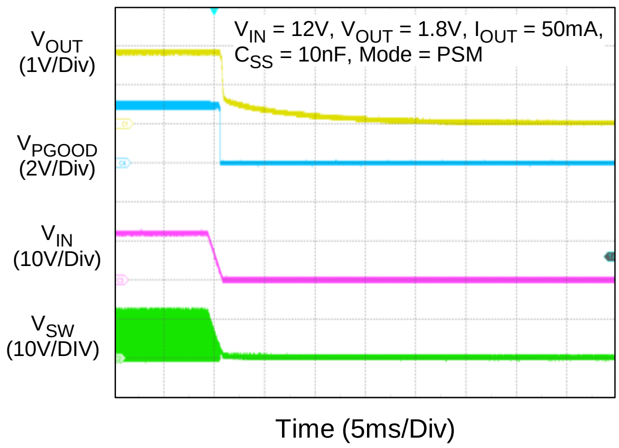
Power Off from EN



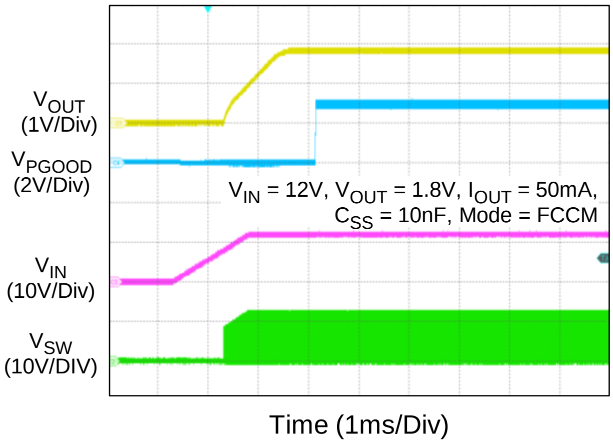
Power On from VIN



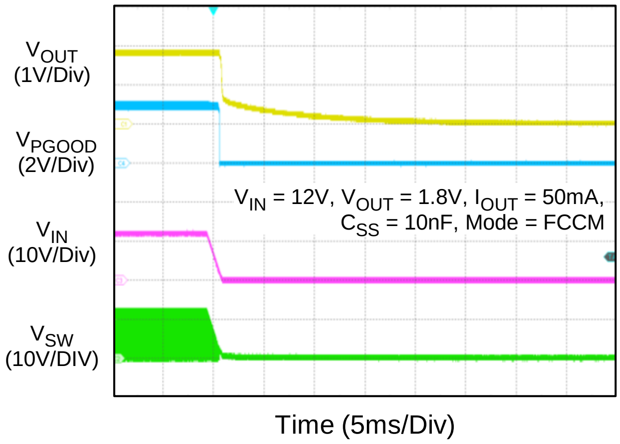
Power Off from VIN



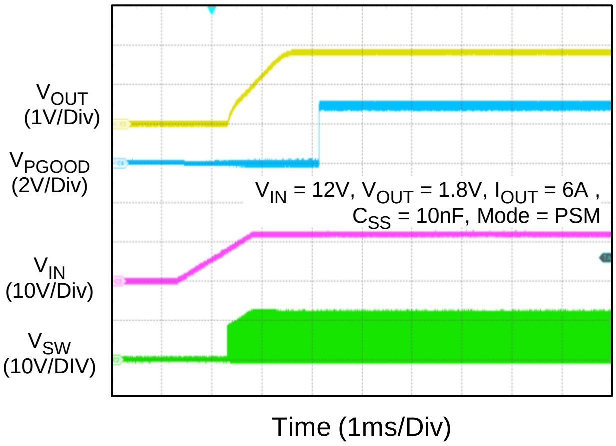
Power On from VIN



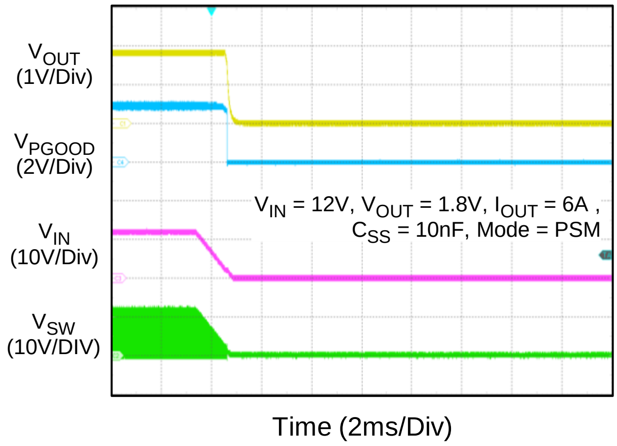
Power Off from VIN



Power On from VIN



Power Off from VIN



17 Operation

The RTQ2807A is a high-efficiency synchronous step-down converter that utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture. The ultrafast ACOT® control enables the use of small capacitance to reduce PCB size.

During normal operation, the internal high-side MOSFET (HS-FET) turns on for a fixed interval determined by a one-shot timer at the beginning of each clock cycle. When the high-side MOSFET turns off, the low-side MOSFET (LS-FET) turns on. Due to the output capacitor ESR, the voltage ripple on the output has a similar shape to the inductor current. Via the feedback resistor network, this voltage ripple is compared with the internal reference. When the minimum off-time of the one-shot timer (180ns, maximum) has timed out and the inductor current is below the current-limit threshold, the one-shot timer is triggered again if the feedback voltage falls below the internal V_{REF} (0.9V, typical). The RTQ2807A supports stable operation with all low-ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). The ACOT® control architecture also features excellent transient response, further improving the output variation during high-frequency load transients, especially when the load suddenly increases.

The conventional COT controller implements the on-time to be inversely proportional to the input voltage and directly proportional to the output voltage to achieve a pseudo-fixed frequency across the input voltage range. However, even with defined input and output voltages, a fixed ON time means that the frequency has to increase at higher load levels. This increase compensates for the power losses in the MOSFETs and the inductor. The ACOT® control further adds a frequency locked loop system, which slowly adjusts the ON time to compensate for the power losses without influencing the fast transient behavior of the COT topology.

17.1 Power and Bias Supply

The VIN pins on the RTQ2807A supply voltage to the drain terminal of the internal high-side MOSFET. These pins also supply bias voltage for an internal regulator that generates 3V at the VCC pin. The voltage at the VCC pin is used for internal chip bias and for gate drive of the low-side MOSFET. The gate drive for the high-side MOSFET is supplied by a floating supply (C_{BOOT}) between the BOOT and SW pins. C_{BOOT} is charged by a BOOT charge switch through VCC. In addition, an internal charge pump maintains that the C_{BOOT} voltage, which is sufficient to turn on the high-side MOSFET.

To improve efficiency and limit power dissipation in the VIN pin, an external voltage that exceeds the output voltage of the internal LDO can override the internal LDO. When using an external bias on the VCC rail, any power-up and power-down sequences can be applied. However, it is important to note that if a discharge path on the VCC rail draws a current exceeding the current limit of the internal LDO, then the VCC drops below the VCC UVLO falling threshold, resulting in the shutdown of the RTQ2807A output.

17.2 Enable, Start-Up, Shutdown, and UVLO

The RTQ2807A implements an undervoltage lockout protection (UVLO) feature to prevent the device from operating before the internal power MOSFETs are fully turned on. The UVLO function monitors the internal LDO regulator voltage. When the VCC voltage falls below the UVLO threshold, the device is shutdown.

The EN pin is provided to control the device turn-on and turn-off. When the EN pin voltage is above the turn-on threshold (V_{EN_R}), the device is enabled. When the EN pin voltage falls below the turn-off threshold (V_{EN_F}), the RTQ2807A is disabled. If the EN pin is floating, the RTQ2807A internally pulls down the EN pin continuously.

When the EN pin voltage rises above the enable threshold, and V_{CC} rises above the $V_{CC\_UVLO\_R}$, the device enters its start-up sequence and initiate a soft-start ramp of the output voltage. An internal soft-start ramp of 1.5ms (typical) will limit the ramp rate of the output voltage to prevent excessive input current during start-up. For applications requiring a longer ramp time, a capacitor C_{SS} can be placed between the SS/TR pin and the AGND pin. The SS/TR pin provides the source current to create a voltage ramp on the C_{SS}. If this external ramp rate is slower than the internal 1.5ms soft-start, the output voltage will be limited by the ramp rate on the SS/TR pin instead. However, if a longer soft-start time (t_{SS}) is desired, the device supports a watchdog function for an abnormal period of soft-start time. When it exceeds 10ms, it will activate the output undervoltage protection. The typical external soft-start time can be calculated using the following equation:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 15(\mu A)}{0.9V}$$

When the V_{EN} is lower than V_{EN_F}, the voltage of the SS/TR pin discharges to AGND.

Figure 1 shows the typical power-up sequence of the device. When the voltage on the VIN and EN pins crosses the input undervoltage lockout rising threshold and EN input rising threshold. After the voltage on the VCC pin reaches the VCC undervoltage lockout rising threshold. The device will start switching if the voltage difference between the SS/TR pin and FB pin is equal to 315mV (for example, $V_{SS/TR} - V_{FB}$ = 315mV, typical) after setting detection is completed. The SS/TR pin should never be left unconnected for soft-start control. After the V_{FB} rises above the V_{TH_PGLH1} (91.5% of V_{REF}, typical), the PGOOD pin will enter a high impedance state after delay time t_{PGDLY} (0.8ms, typical).

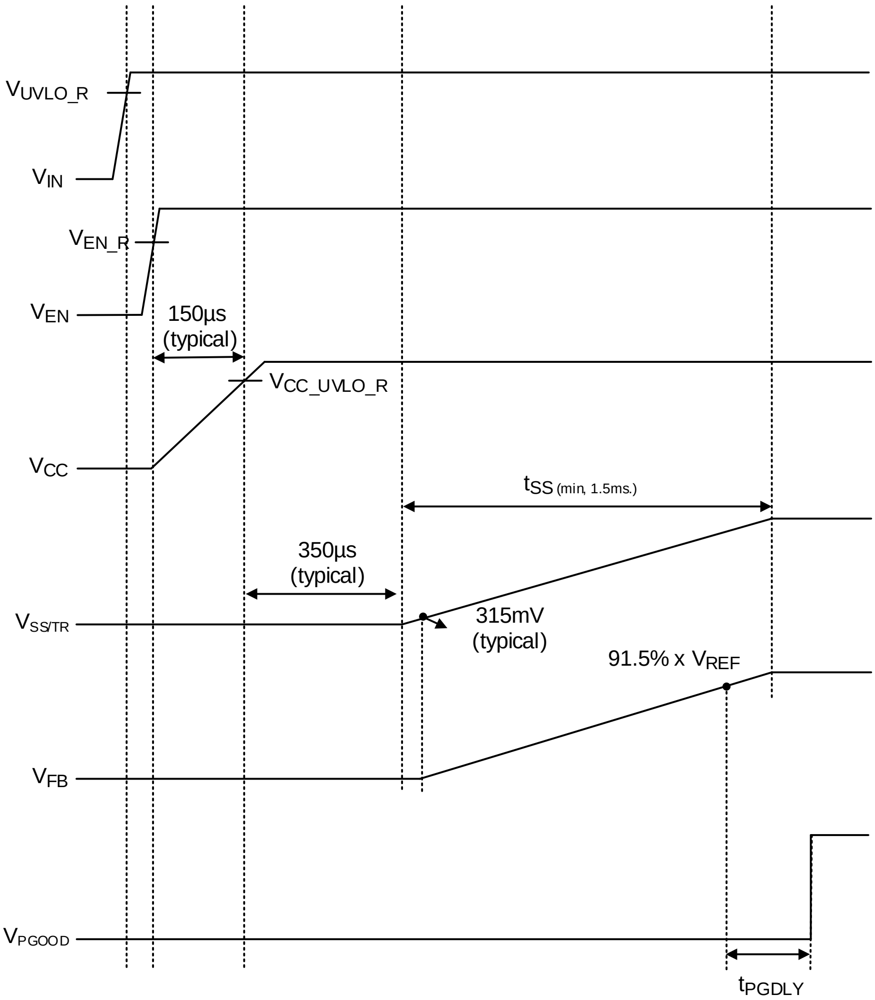


Figure 1. Power-Up Sequence

17.3 Output Voltage Tracking and External Reference

The RTQ2807A can replace the internal voltage reference (V_{REF}) or track an external power rail by inputting an external voltage signal to the SS/TR pin. The V_{FB} will track this signal, which ranges from 0.3 V to 1.4 V. During startup, it is essential to ensure that the SS/TR pin voltage reaches 900mV or higher for proper operation.

The Power-Good Output function is activated if V_{REF} or an external voltage signal exceeds 800mV. This function is disabled if the external voltage signal at the SS/TR pin is lower than 750mV.

17.4 Pre-Bias Start-Up

If there is a residual voltage on the output voltage before start-up, both the high-side and low-side MOSFETs are prevented from switching until the internal soft-start ramp exceeds the feedback voltage. Switching will begin when the soft-start ramp exceeds the feedback voltage, causing the output voltage to increase from the pre-biased level to its regulated target. Figure 2 shows an example of a pre-bias start-up.

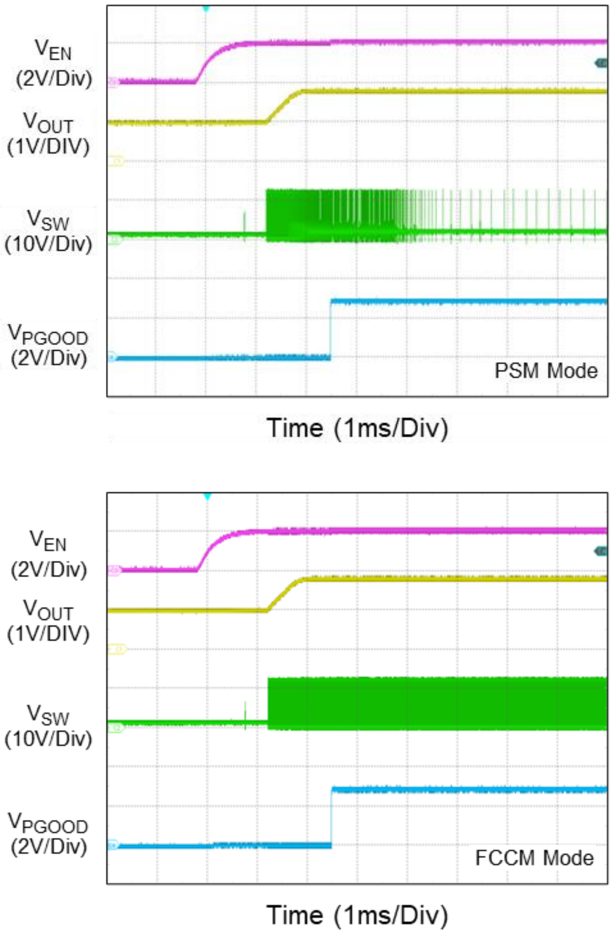


Figure 2. Pre-Bias Start-Up

17.5 Minimum On-Time and Minimum Off-Time

The constraint on the operating duty cycle is determined by the minimum controllable on-time and off-time. The minimum on-time is the shortest duration that the high-side MOSFET can be in its "ON" state. In continuous mode operation, the effective switching frequency is reduced to regulate the target output voltage when the converter reaches its minimum on-time limits. However, reducing the operating frequency will alleviate the constraint on the minimum duty cycle. The equation can be ideally estimated without the resistive drop, as follows.

$$V_{IN}(max) \leq \frac{V_{OUT}}{f_{SW}(max) \times t_{ON\_MIN}(max)}$$

Where t_{ON_MIN} is the minimum on-time, which is 50ns (maximum).

The minimum off-time, t_{OFF_MIN}, is the shortest duration in which the RTQ2807A is capable of turning on the low-side MOSFET, tripping the current comparator, and then turning the power off again. The limit on the minimum off-time imposes the maximum duty cycle, which can be calculated using the following formula: Duty Cycle = t_{ON} / (t_{ON} + t_{OFF_MIN})

The minimum off-time and the minimum input voltage considering the loss terms can be calculated using the following equation:

$$V_{IN}(min) \geq \left[\frac{V_{OUT} + I_{OUT\_MAX} \times (R_{DSON\_L} + DCR)}{1 - t_{OFF\_MIN}(max) \times f_{SW\,(max)}}\right] + I_{OUT\_MAX} \times (R_{DSON\_H} - R_{DSON\_L})$$

where the minimum off-time of the RTQ2807A is 180ns (maximum); R_{DSON_H} is the on-resistance of the high-side MOSFET; R_{DSON_L} is the on-resistance of the low-side MOSFET; DCR is the DC resistance of the inductor.

17.6 Mode Selection and Switching Frequency

The RTQ2807A offers three different switching frequencies: 660kHz, 1100kHz, and 2200kHz, which can be set by adjusting the voltage on the MODE pin. Choosing the operating frequency is a trade-off between efficiency and component size. High-frequency operation allows the use of smaller inductors and capacitor. Operating at lower frequencies enhances efficiency by reducing internal gate charge and transition losses. However, it requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Furthermore, the RTQ2807A offers two modes which are Forced Continuous-Conduction Mode (FCCM) and Pulse Skipping Mode (PSM) for light load conditions to improve efficiency.

When the MODE pin is left floating, the default status will be set to 1100 kHz for PSM operation. Users can configure the operating mode and frequency by connecting a resistor to the AGND pin or VCC pin, as specified in Table 6.

Table 6. Mode Pin Selection

Mode Pin Connections	Light Load Mode	Switching Frequency (kHz)
Short to VCC	PSM	1100
243KΩ ±20% to AGND	PSM	2200
121KΩ ±20% to AGND	PSM	660
60.4KΩ ±20% to AGND	FCCM	660
30.1KΩ ±20% to AGND	FCCM	2200
Short to AGND	FCCM	1100

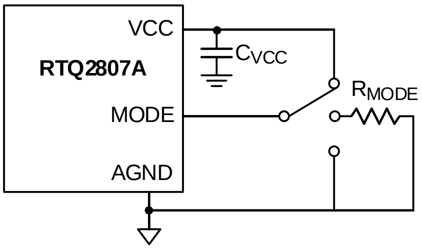


Figure 3. MODE Connection

17.7 Light Load Operation

During low load conditions, the inductor current can drop to zero or even become negative. This condition is detected by the internal zero current-detection circuitry that utilizes the low-side MOSFET R_{DSON_L} to sense the inductor current. The low-side MOSFET is turned off when the inductor current drops to zero, resulting in Pulse Skipping Mode (PSM). Both power MOSFETs will remain off, with the output capacitor supplying the load current, until the feedback voltage falls below the internal V_{REF}. Operating in PSM ensures high efficiency under light loads, while setting MODE to FCCM operation helps meet tight voltage regulation accuracy requirements.

17.8 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure that the BOOT capacitor maintains a sufficient voltage to turn on the high-side MOSFET under any conditions. The BOOT UVLO usually actives at an extremely high conversion ratio, or when a higher VOUT application operates under very light loads. Under such conditions, if the voltage difference between BOOT and SW falls below $V_{BOOT\_UVLO\_F}$ (2.3V, typical), the device turns on the BOOT recharge path (120ns, typical) to charge the BOOT capacitor.

17.9 Power-Good Output

The RTQ2807A features an open-drain power-good indication, which is connected to an external voltage source through a pull-up resistor. The power-good function is activated after the soft-start process is finished and is controlled by the feedback signal V_{FB}. During soft-start, V_{PGOOD} is actively held low and only allowed to become high after soft-start is finished. If V_{FB} rises above the V_{TH_PGLH1} (91.5% of the V_{REF}, typical), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} falls below V_{TH_PGHL2} (80% of the V_{REF}, typical) or exceeds V_{TH_PGHL1} (116% of the V_{REF}, typical), V_{PGOOD} will be pulled low. For V_{FB} is higher than V_{TH_PGHL1}, V_{PGOOD} can be pulled high again if V_{FB} drops back to V_{TH_PGLH2} (106% of the V_{REF}, typical). Once startup, if any internal protection is triggered, V_{PGOOD} will be pulled down to GND. The internal open-drain pull-down device will pull the V_{PGOOD} low. This is to prevent false flag operation for short excursions in output voltage, such as during line and load transients. The profile for the power-good indication is shown in Figure 4.

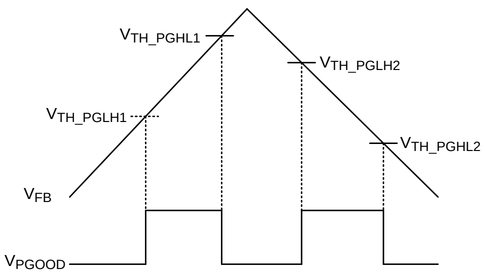


Figure 4. The Logic of PGOOD

17.10 Overcurrent-Limit Protection

The RTQ2807A features cycle-by-cycle current-limit protection on the low-side MOSFETs, and the protection prevents the device from catastrophic damage due to output short circuits, overcurrent events, or inductor saturation.

The low-side MOSFET valley current-limit protection, as shown in Figure 5, is achieved by measuring the inductor current through the low-side MOSFET and mirroring to the RLIM pin with the ratio of G_{CS} using a resistor during the low-side on-time. Once the inductor current rises above the low-side switch valley current-limit threshold (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the I_{LIM_L}; that is, another on-time can only be triggered when the inductor current goes below I_{LIM_L}.

The RTQ2807A provides a programmable cycle-by-cycle valley current limit for the low-side MOSFET switch by the RLIM pin. The output current-limit threshold can be calculated as follows:

$$R_{LIM}(\Omega) = \frac{V_{LIM}}{G_{CS}\times\left(I_{LIM} - \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}}\times\frac{1}{2\times L\times f_{SW}}\right)}$$

Where V_{LIM} =1.2V, G_{CS} = 40μA/A, and I_{LIM} is the desired output current limit (A).

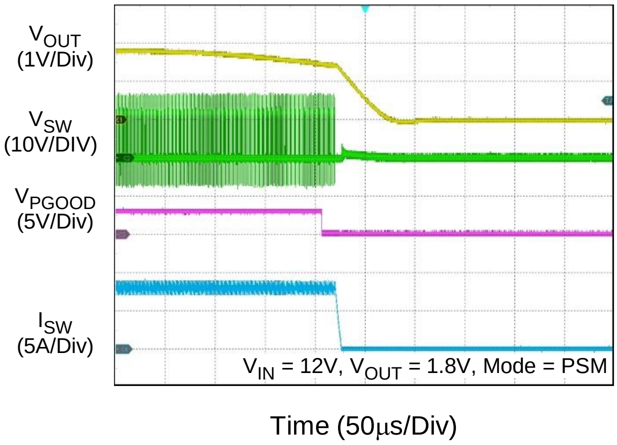


Figure 5. Overcurrent-Limit Protection

17.11 Output Undervoltage Protection

The RTQ2807A includes output undervoltage protection (UVP) against overload or short-circuit conditions by constantly monitoring the feedback voltage, V_{FB}. If V_{FB} drops below the undervoltage protection threshold V_{UVP} (80% of the V_{REF}, typical), the UV comparator will go high, and then the IC enters latch-off mode until the VCC or EN is recycled. The behavior of UVP is shown in Figure 6.

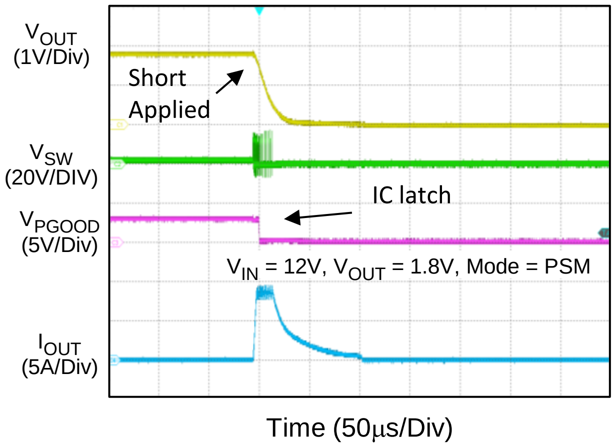


Figure 6. Output Undervoltage Protection

17.12 Negative Current Limit

The RTQ2807A also monitors the inductor current during the "ON" state of the low-side MOSFET to prevent excessive negative current flowing through the low-side MOSFET. Once the negative current exceeds the low-side switch negative current-limit threshold I_{LIM_NEG} (–8A, typical), the device turns off the low-side MOSFET for 700ns. This behavior can keep the valley of the negative current at I_{LIM_NEG} to protect the low-side MOSFET. Designers should choose appropriate inductance value to avoid triggering I_{LIM_NEG} during normal operation.

17.13 Output Overvoltage Protection

The RTQ2807A includes an output overvoltage protection (OVP) circuit to limit the output voltage and minimize overshoot, as shown in Figure 7. If the V_{FB} exceeds 116% of the V_{REF}, the high-side MOSFET will be latched off, and the PGOOD pin remains low until the VCC or EN is cycled. In the meantime, if the overvoltage condition still exists, the low-side MOSFET remains on to discharge output voltage until the low-side MOSFET valley current reaches the negative current-limit threshold (I_{LIM_NEG}). Once reaching I_{LIM_NEG}, the low-side MOSFET is turned off for approximately 700ns before the low-side MOSFET is turned on again.

The RTQ2807A repeats this cycle until the output voltage drops. When the V_{FB} goes below 50% of the V_{REF}, the low-side MOSFET will remain on. The device requires cycling of either EN or VIN to clear the OVP fault.

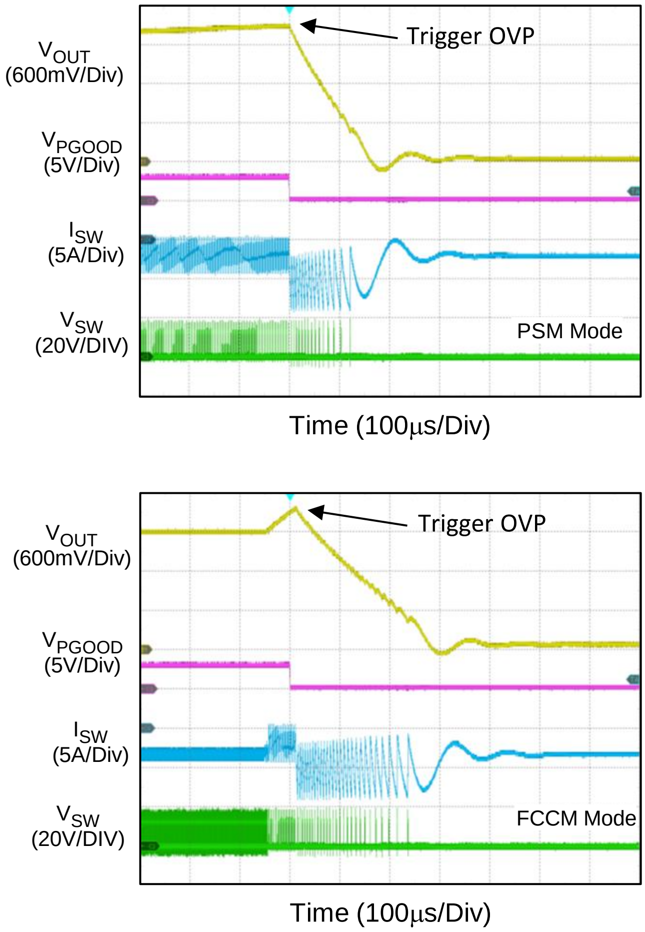


Figure 7. Output Overvoltage Protection

17.14 Output Quick Discharge Mode

The RTQ2807A features an Output Quick Discharge Mode (OQDM) designed to mitigate overshoot before triggering the OVP. When the V_{FB} voltage exceeds 104% of the V_{REF} but remains below the OVP threshold (typically 116%), OQDM is activated. The behavior is shown in Figure 8. During OQDM, the high-side MOSFET is off, while the low-side MOSFET remains on until the inductor current reaches –4A (typicl) or the V_{FB} voltage falls below 102%. Once the inductor current reaches –4A, the low-side MOSFET is briefly turned off for 700ns before being turned on again. This sequence is repeated until the V_{FB} voltage falls below 102% of the V_{REF}. After completing 15 consecutive FCCM cycles, the RTQ2807A exits OQDM. This mode is effective in reducing overshoot and ensuring stable operation.

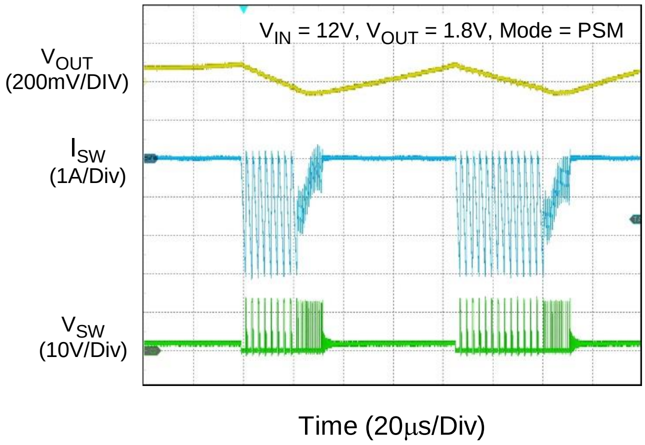


Figure 8. Output Quick Discharge Mode

17.15 Output Voltage Discharge

When the RTQ2807A is disabled by the EN pin, UVLO, or OTP, the device discharges the output capacitors (via the SW pins) through an internal discharge resistor (80Ω, typical) connected to ground. This function prevents reverse current from flowing from the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is cleared.

17.16 Over-Temperature Protection (OTP)

The RTQ2807A includes an over-temperature protection (OTP) circuit to prevent overheating due to excessive power dissipation. The OTP will shut down the switching operation when the junction temperature exceeds the over-temperature protection threshold T_{OTP} (160°C, typical). The device will remain in a latch-off state until the temperature drops by 20°C and then the VCC or EN is restarted.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside the absolute maximum operational range as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or case permanent damage.

18 Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

A typical application circuit for the RTQ2807A is shown in the Typical Application Circuit section. The selection of external components is primarily driven by the load requirements. Next, the inductor L is chosen, and then the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} can be selected. Subsequently, feedback resistors are selected to set the desired output voltage. Lastly, the remaining optional external components can be selected to enable additional functionalities, such as setting the EN operation voltage via by the VIN divider, adjusting the operation frequency, setting the operation at light loads, configuring the valley current limit value, setting the external soft-start time, and setting the Power-Good function.

18.1 Switching Frequency and MODE Selection

The switching frequency, current limit, and switching mode (PSM or FCCM) are set by a voltage divider connected solely from VCC to GND to the MODE pin.

The selection of the switching frequency is a trade-off between efficiency and the size of system components. High-frequency operation allows the use of smaller inductors and capacitors. Operating at lower frequencies enhances efficiency by reducing internal gate charge and transition losses, but it requires larger inductors and/or capacitors to maintain a low output ripple voltage.

18.2 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A balanced compromise between size and loss is achieved with a 30% peak-to-peak ripple current ΔI_L relative to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value, as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degrade transient response. Lower inductance values allow for a smaller case size, but the increased ripple lowers the effective current-limit threshold and increases the AC losses in the inductor. To enhance efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines the ripple current and the load-current value at which the boundary of PSM and FCCM switchover occurs.

The selected inductor must require a sufficient saturation current rating above the peak inductor current to prevent saturation. The peak inductor current (I_{L_PEAK}) is estimated as follows:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power-up, fault conditions, or transient load conditions, the inductor current can exceed the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. Therefore, the most conservative approach is to select an inductor with a saturation current rating equal to or greater than the switch current limit, rather than the peak inductor current.

The reverse inductor current should be considered. In FCCM operation, the design of the inductor valley current should be exceed -4A to prevent triggering the Output Quick Discharge Mode value at no-load operation.

18.3 Input Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. To prevent significant variations in input voltage, C_{IN} should be appropriately sized. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 9 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors.

Ceramic capacitors typically exhibit very low equivalent series resistance (ESR), which allows to ignore the ripple caused by ESR. The minimum input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where

ΔV_{CIN_MAX} = 200mV for typical application (V_{IN} > 7V)

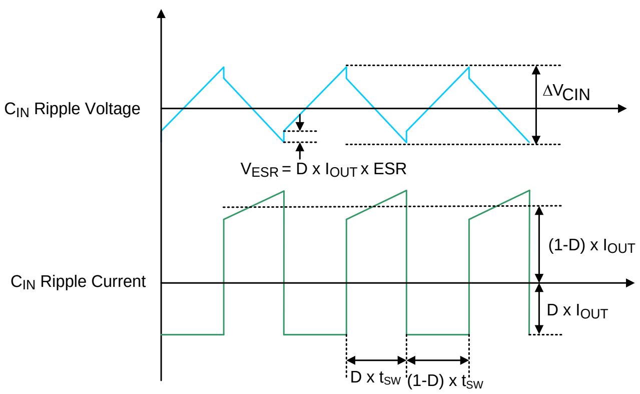


Figure 9. CIN Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the converter can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) using the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at the maximum output load, which should be considered when evaluating the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at a 50% duty cycle, that is, $V_{IN} = 2 \times V_{OUT}$. It is common to use the worst-case $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at $V_{IN} = 2 \times V_{OUT}$ for design purposes. Note that the ripple current ratings from capacitor manufacturers are often based on a lifespan of only 2000 hours. This makes it advisable to de-rate the capacitor further, or choose a capacitor rated for a higher temperature than required.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because their small size, robustness, and very low ESR. However, caution is necessary when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2807A circuit is connected into an active supply, the input voltage can oscillate to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor that has a higher ESR, which helps to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, one small ceramic capacitor of 0.1μF should be placed close to the part. For capacitors sizes, 0402 or 0603 are suitable. X7R capacitors are recommended for optimal performance across temperature and input voltage variations.

18.4 Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple, the transient loads, and ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}. It can be expressed as follows:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Where ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}. The highest output ripple is at maximum input voltage since ΔI_L increases with the input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which can be calculated from the on-time and the minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage can be determined by the following equation:

$$\Delta V_{OUT\_SAG} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The amount of overshoot due to the energy stored in the inductor when the load is removed can be calculated as follows:

$$\Delta V_{OUT\_SOAR} = \frac{L \times (I_{L\_PEAK})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the optimal ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when operated near their rated voltage.

18.5 Internal VCC Regulator

Proper bypassing at the VCC pin is necessary to provide the high transient currents required by the power MOSFET gate drivers. It is recommended to place a low ESR MLCC capacitor with a capacitance ≥ 1μF as close as possible to the VCC pin. Ensure that the rated voltage of C_{VCC} is at least 6.3V or higher to minimize the effects of DC bias derating. Using a capacitor in the 0603 or 0805 size is recommended.

Applications with high input voltages and high switching frequencies will increase die temperature because of the higher power dissipation across the LDO. The VCC pin should not be used to provide power to other devices or loads.

18.6 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage, VIN. Specifically, the bootstrap capacitor is charged through an internal MOSFET switch to a voltage approximately equal to V_{VCC} each time the LSFET is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle.

The selection of C_{BOOT} considers the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose a ΔV_{BOOT} such that the available gate-drive voltage is not significantly degraded when determining C_{BOOT}. A typical range of ΔV_{BOOT} is from 100mV to 300mV. The bootstrap capacitor should be a low-ESR ceramic capacitor. For most applications, a 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises. In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (< 10Ω) resistor between the BOOT pin and the external bootstrap capacitor. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. The recommended application circuit is shown in Figure 10, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor connection.

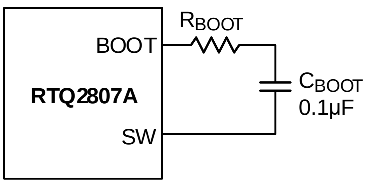


Figure 10. External Bootstrap Resistor at the BOOT Pin

18.7 Output Voltage Programming

The output voltage can be programmed using a resistive divider from the output to ground, with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 11. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage V_{REF}, is typically 0.9V.

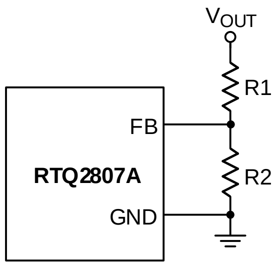


Figure 11. Output Voltage Setting

The recommended resistance of R2 is 10kΩ, ranging from 1kΩ to 10kΩ for good noise immunity consideration. The resistance of R1 can then be obtained as below:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better are recommended. The placement of the resistive divider should be very close to the FB pin to minimize PCB trace length and noise immunity consideration. Furthermore, great care should be taken to route the feedback trace away from noise sources, such as the inductor or the SW trace.

18.8 Feedforward Capacitor (C_{FF})

The RTQ2807A is optimized for low duty-cycle applications and the control loop is stable with low ESR ceramic output capacitors. In higher duty-cycle applications (higher output voltages or lower input voltages), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Because of the large internal ripple in this condition, the response may become too slow, and may show an under-damped response. This can cause some ringing in the output, and is especially visible at higher output voltage applications like 12V to 5V where the duty-cycle is high and the feedback network attenuation is large, adding to the delay. As shown in Figure 12, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

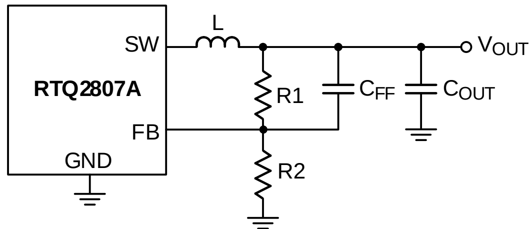


Figure 12. Feedback Loop with Feedforward Capacitor

Loop stability can be checked by viewing the load transient response. A load step with a speed that exceeds the converter bandwidth must be applied. For ACOT®, the loop bandwidth can be in the order of 100 to 200kHz, so a load step with 500ns maximum rise time (di/dt ≈ 2A/μs) ensures the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current-limit threshold. A load transient from 30% to 60% of the maximum load is reasonable, as shown in Figure 13.

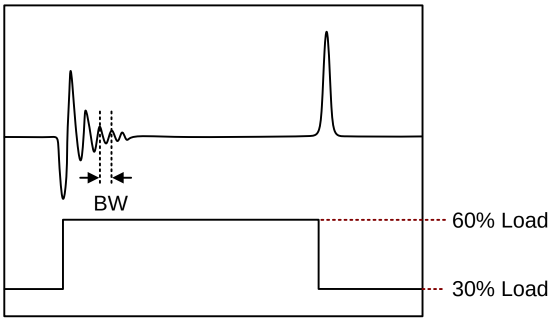


Figure 13. Example of Measuring the Converter BW by Fast Load Transient

C_{FF} can be calculated basing on below equation:

$$C_{FF} = \frac{1}{2\pi \times BW} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Figure 14. shows the transient performance with and without a feedforward capacitor.

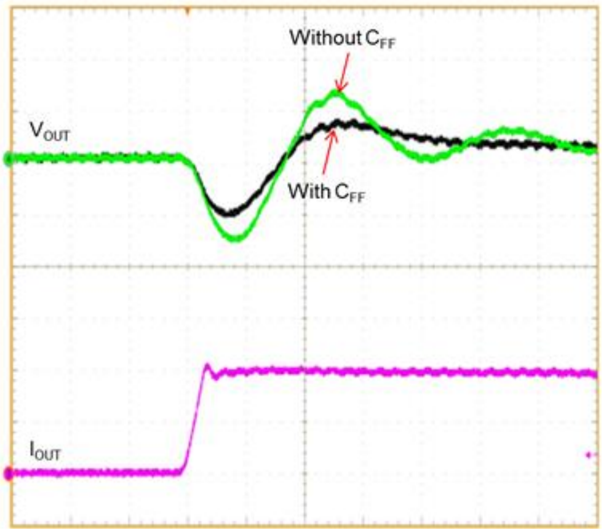


Figure 14. Load Transient Response with and without a Feedforward Capacitor

Note that after defining the C_{FF}, it is important to verify the load regulation because the feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage exceeds the specified limits caused by calculated C_{FF}, decrease the value of feedforward capacitor C_{FF}.

18.9 Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off operations for the device. When the EN pin voltage is above the turn-on threshold (V_{EN_R}), the device starts switching. It stops switching when the EN pin voltage falls below the turn-off threshold (V_{EN_F}). The RTQ2807A internally weakly pull-down on the EN pin. For automatic start-up, the EN pin can be connected to the input supply VIN directly through a pull-up resistor R_{EN}. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. For an added delay, the EN pin can be externally connected to VIN by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 15.

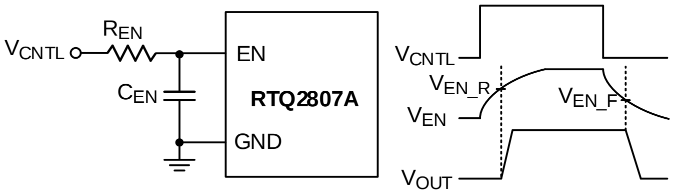


Figure 15. Enable Timing Control

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 16. In this case, a pull-up resistor, R_{EN}, is connected between V_{CNTL} and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin.

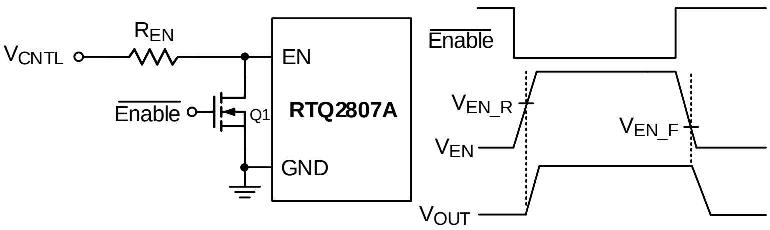


Figure 16. Logic Control for the EN Pin

If it is necessary to enable the device for a specific V_{IN} or shut it down, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input VULO threshold, as shown in Figure 17.

To set the start voltage, first select the bottom resistor R_{EN2}, and the recommended value is between 10kΩ and 100kΩ.

A resistive divider connected between VIN and EN can set a different turn-on (V_{START}) or turn-off thresholds (V_{STOP}).

This is recommended for customer designs that do not have an additional EN logic signal, to avoid bouncing at the EN pin.

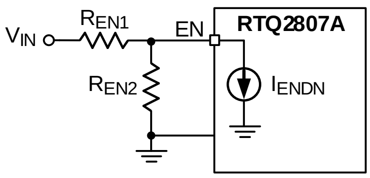


Figure 17. Resistor Divider for Lockout Threshold Setting

$$R_{EN1} = \frac{\left(V_{START} - V_{EN\_R}\right)}{I_{PD\_EN} + \frac{V_{EN\_R}}{R_{EN2}}}$$

$$V_{START} = \left(\frac{V_{EN\_R}}{R_{EN2}} + I_{PD\_EN}\right) \times R_{EN1} + V_{EN\_R}$$

$$V_{STOP} = \left(\frac{V_{EN\_L}}{R_{EN2}} + I_{PD\_EN}\right) \times R_{EN1} + V_{EN\_L}$$

18.10 Thermal Considerations

In many applications, the RTQ2807A does not generate much heat due to its high efficiency and low thermal resistance of its thermally enhanced WQFN-14L 2x3 (FC) package. However, in applications where the RTQ2807A is running at a high ambient temperature, high input voltage, and high switching frequency, the generated heat may exceed the maximum junction temperature of the part. To avoid permanent damage to the device, the junction temperature should never exceed the maximum junction temperature listed under Absolute Maximum Ratings. If the junction temperature reaches approximately 160°C, the RTQ2807A will stop switching the power MOSFETs until the temperature falls to about 20°C below this threshold and re-start the power of EN or VIN. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

where

- $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C.
- T_A is the ambient operating temperature, $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be enhanced by incorporating a copper ground heat sink. Additionally, including backside copper with thermal vias, stiffeners, and other enhancements can help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply setting $\theta_{JA(EFFECTIVE)}$ to approximately 110% to 120% of the standard θ_{JA} provides a reasonable approximation for determining the allowed $P_{D(MAX)}$. The simulated thermal resistance of the RTQ2807A when mounted on PCBs with varying stack-up and copper thickness. The thermal model layout is based on the RTQ2807A evaluation board.

Table 7 shows the simulated thermal resistance of the RTQ2807A when mounted on PCBs with varying stack-up and copper thickness. The thermal model layout is based on the RTQ2807A evaluation board.

Table 7. Simulated Thermal Resistance with Difference Tack-Up and Copper Thickness

Simulated θ_{JA}	$\theta_{JA(EFFECTIVE)}$ (°C/W)
4 Layer with 2oz copper	37.88 * 1.1

As an example, consider the case when the RTQ2807A is used in applications where V_{IN} = 12V, I_{OUT} = 6A, V_{OUT} = 1.8V.

The efficiency at 1.8V, 6A is 88.3% by using WE-74437346010 (1μH, 10mΩ DCR) as the inductor and measured at room temperature. The AC core loss of the inductor is 34.9mW, as specified on the manufacturer's website. In this case, the power dissipation of the RTQ2807A can be calculated as follows:

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I^2_{OUT} \times DCR + P_{CORE\_AC}\right) = 1.035W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 41.67°C/W by using the RTQ2807A evaluation board with 4 layers PCB and 2oz copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

T_J = 68°C

18.11 Layout Guidelines

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2807A:

- Use a four-layer or six-layer PCB with a maximum ground plane for optimal thermal performance.
- Place input capacitors as close to the VIN pins as possible.
- Place input MLCC capacitors as close to the VIN and PGND pins as possible. It is highly recommended to use a 0.1μF/0402 ceramic capacitor between the VIN pin 3 and PGND pin 1.
- Place the VCC decoupling capacitor, C_{VCC}, as close to the VCC pin as possible.
- Place the bootstrap capacitor, C_{BOOT}, as close to the IC as possible. A 0.1μF to 1μF with 10V or higher rating is recommended for the bootstrap capacitor.
- Place multiple vias under the device near VIN and PGND, and place near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and adds thermal vias under and near the RTQ2807A to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Place capacitors C_{SS} as close to the SS/TR pin as possible.
- Connect the feedback sense network behind via of the output capacitor.
- Place the feedback components R_1/R_2/C_{FF} near the IC.
- The ground connection between the analog ground and power ground should be close to the IC to minimize the ground current loops. If there is only one ground plane, it should keep enough isolation between analog return signals and high-power signals.

Figure 18 is a layout example using a (92mm x81mm), four-layer PCB with 2oz copper.

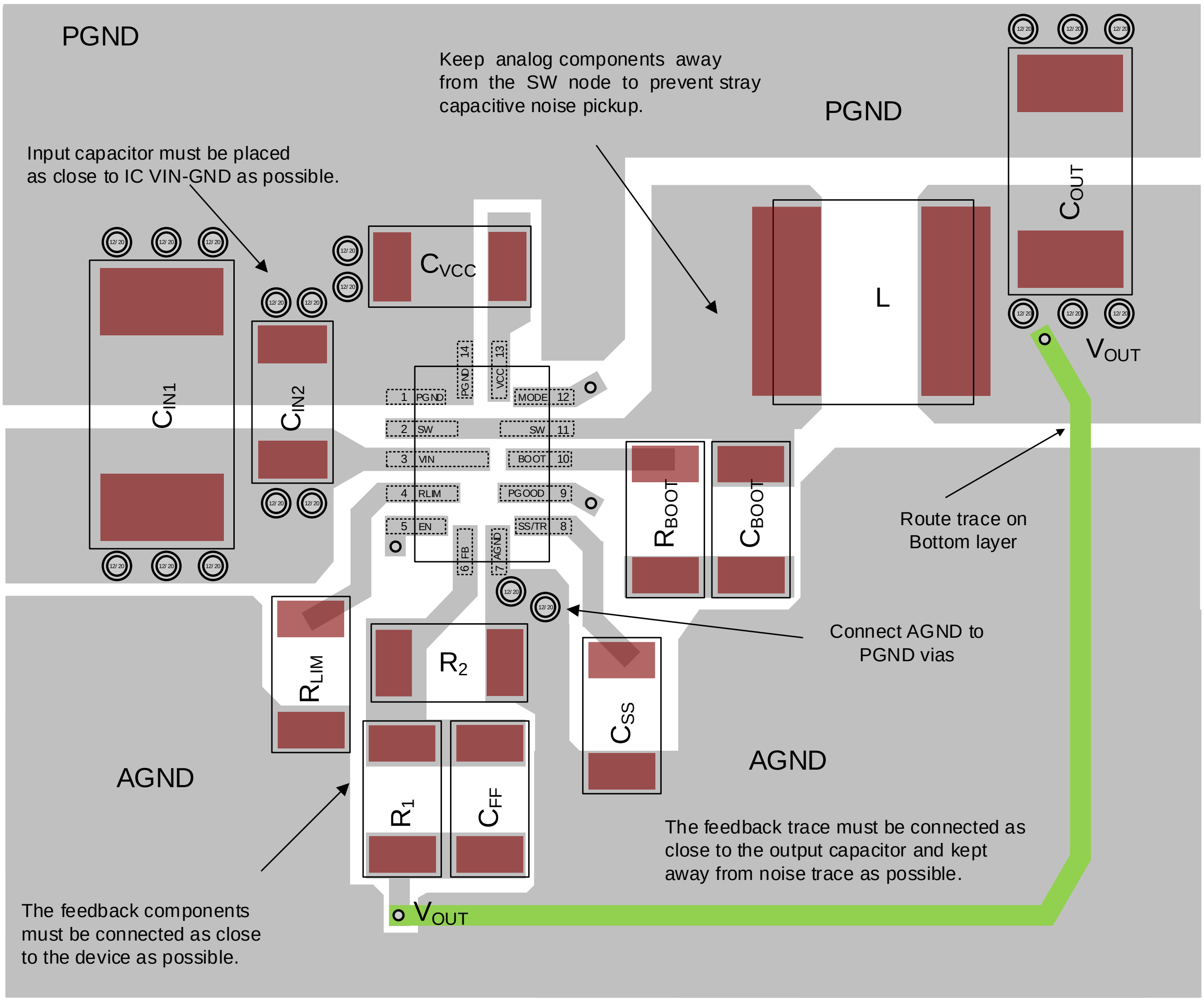
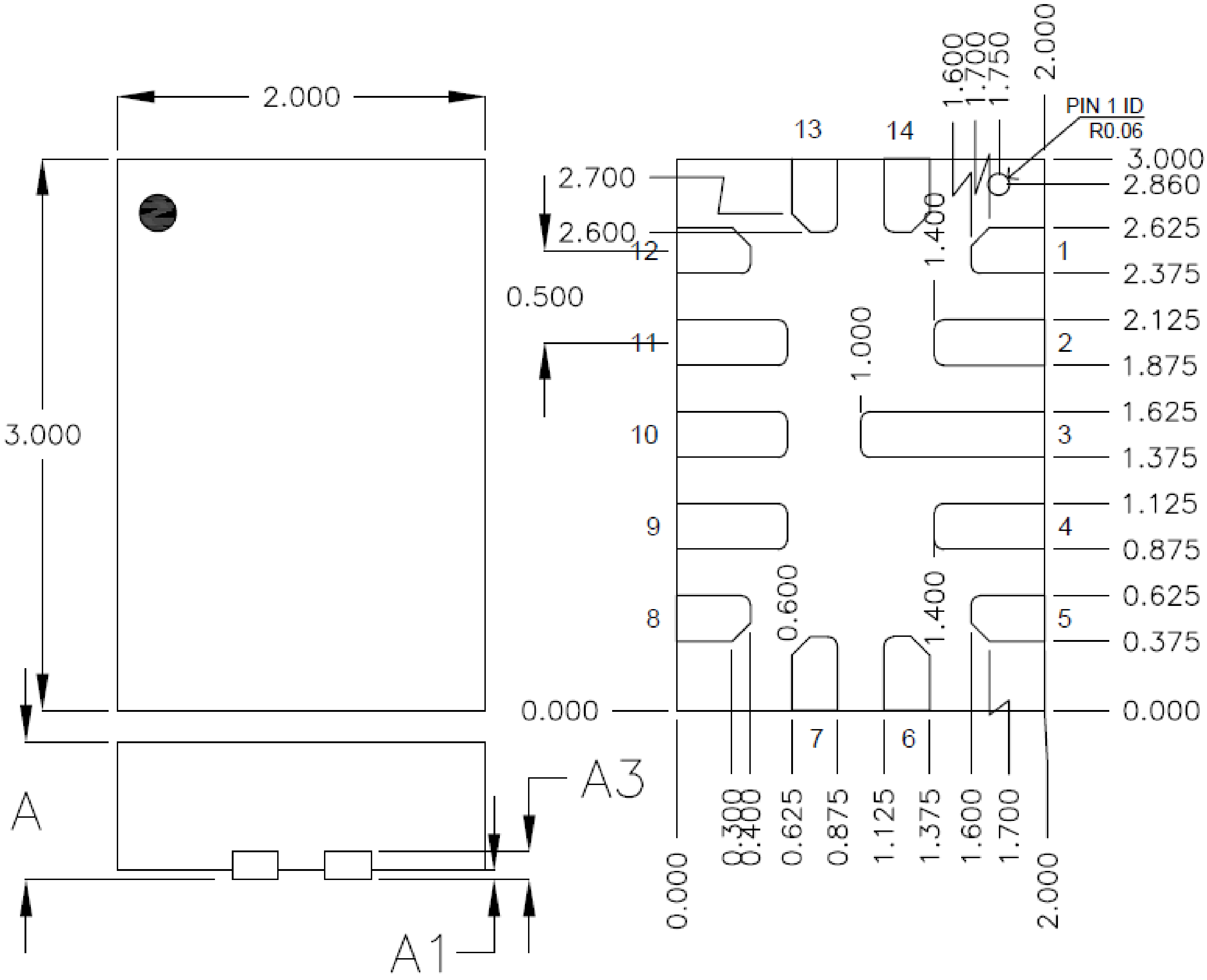


Figure 18. Layout Guide (Top Layer)

19 Outline Dimension

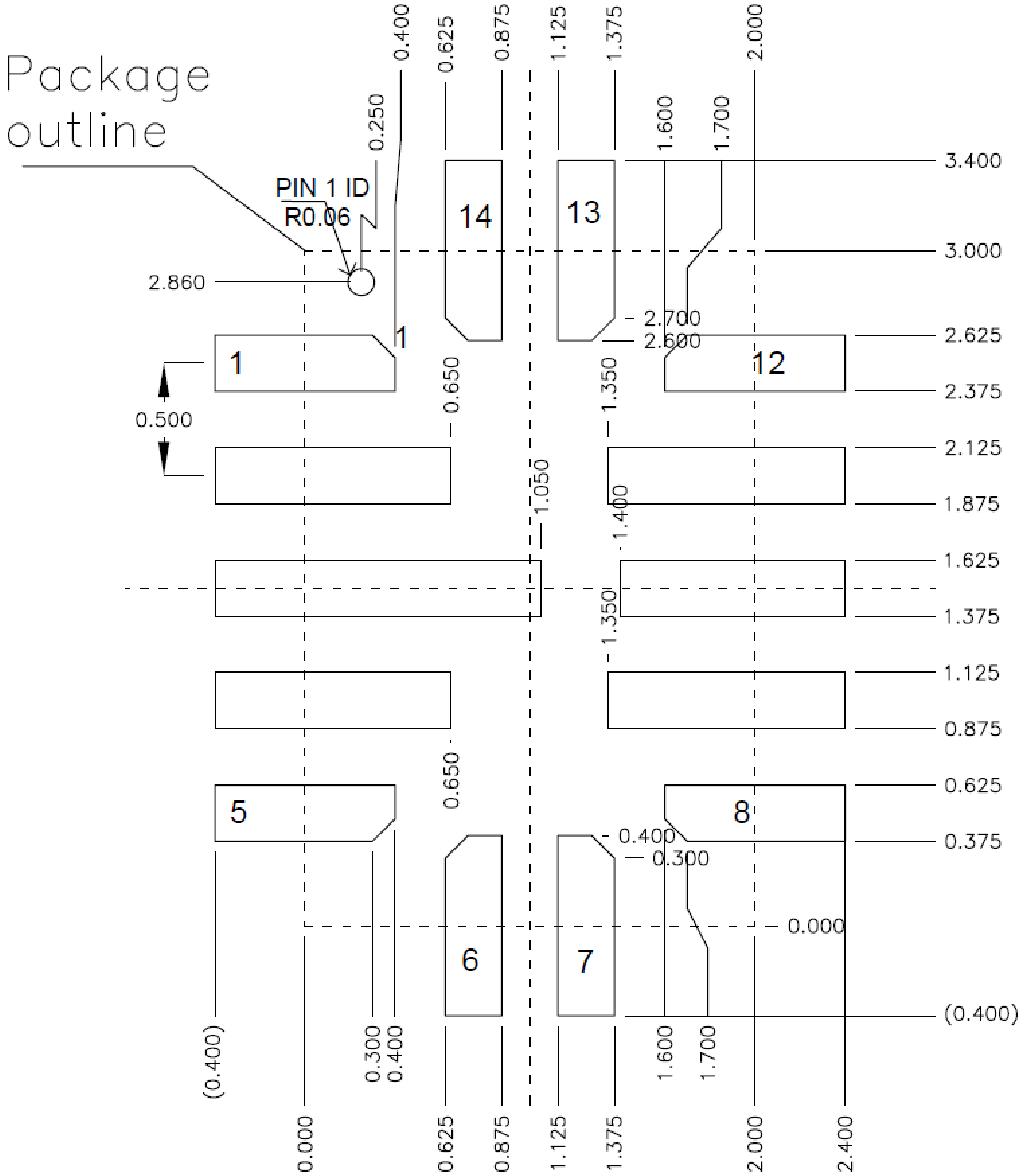


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 14T QFN 2x3 Package (FC)

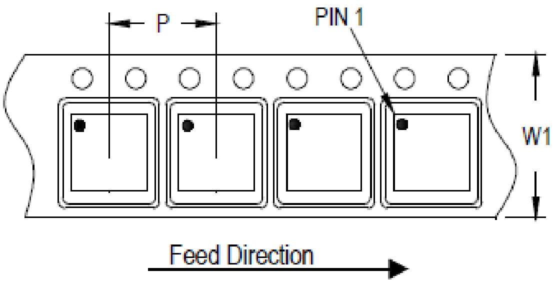
20 Footprint Information

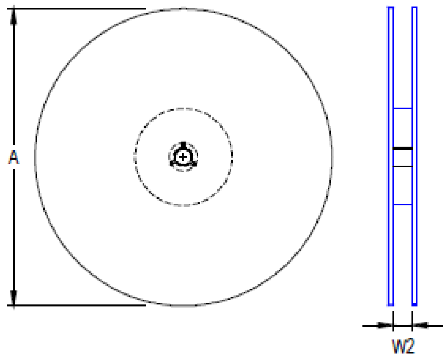


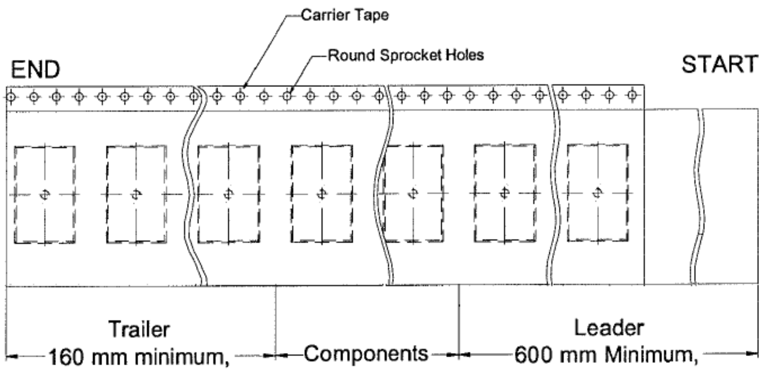
Package	Number of Pin	Tolerance
V/W/U/XQFN2x3-14T(FC)	14	±0.05

21 Packing Information

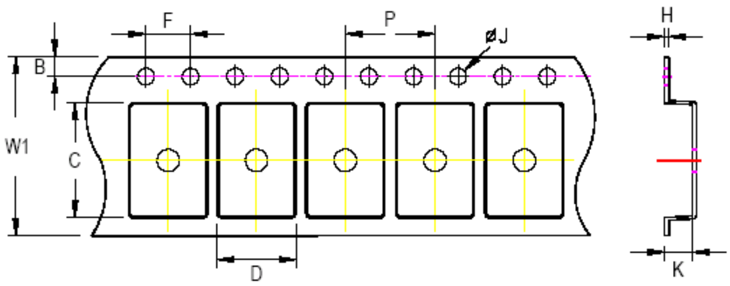
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leade r(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 2x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container	Reel		Box			Carton		
Package	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 2x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
00	2024/4/29	Final	ESD Ratings on P7