Automotive High-Accuracy Reset IC with Functional Safety Support

1 General Description

The RTQ2588-QB is a high-accuracy and low-quiescent automotive reset IC. The RTQ2588-QB provides factory-set sensing options with 50mV steps ranging from 0.5V to 1.1V, and 0.1V steps ranging from 1.2V to 5V, covering most automotive applications. It features overvoltage and undervoltage window voltage sensing with factory-set thresholds of ±4%, ±5%, ±7%, ±9%, and a 3.5μA low supply current.

The RTQ2588-QB does not require external divider resistors to sense the voltage, helping system designers save on solution size and cost while maintaining high accuracy performance. It also provides manual reset ($\overline{MR}$) and capacitor time (CT) functions to facilitate easy system design.

For automotive functional safety applications, the RTQ2588-QB features the built-in self-test (BIST) as a safety mechanism to enhance the system latent point fault metrics (LPFM) scores. The RTQ2588-QB is qualified for AEC-Q100 Grade 1 and is an automotive quality-managed (QM) product from Richtek. It is available in a WDFN-6L 1.5x1.5 (COL) package.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 125°C.

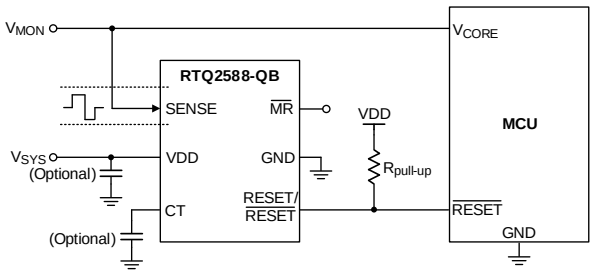
2 Applications

- Advanced Driver Assistance System (ADAS)
- DSP, Microcontroller, SoC Applications
- Body Control Module (BCM)
- In-Vehicle Infotainment (IVI)
- Digital Instrument Cluster
- Telematics Box (T-Box)

3 Features

- **AEC-Q100 Grade 1 Qualified**
- **Input Voltage Range from 1.7V to 5.5V**
- **Low Supply Current with 3.5μA (Typical)**
- **Undervoltage-Lockout (UVLO) with 1.65V Falling Threshold**
- **High Threshold Accuracy**
  - **±0.25% in Typical, ±0.78% in Full Temperature Range**
- **Factory-Set Wide Voltage-Sensing Range**
  - **0.5V to 1.1V in 50mV/step, 1.2V to 5V in 0.1V/step**
- **Factory-Set Input Threshold Levels**
  - **Available in UV Only and Window Configurations**
  - **Factory-Set Threshold Options Available: ±4%, ±5%, ±7%, ±9%**
- **Factory-Set Output Type**
  - **Open-Drain (Active-Low); Push-Pull (Active-High or Low)**
- **Manual Reset Capable**
- **Factory-Set Fixed Options for Reset Recovery Time Delay**
  - **Option A, E: 50μs, 200μs**
  - **Option B, F: 1ms, 20ms**
  - **Option C, G: 5ms, 100ms**
  - **Option D, H: 10ms, 200ms**
- **Programmable Reset Recovery Time Delay Option via an External Capacitor**
- **Support the Systematic Capability up to ASIL B Target**
  - **Built-In Self-Test (BIST) for OV/UV Monitors**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 125°C**

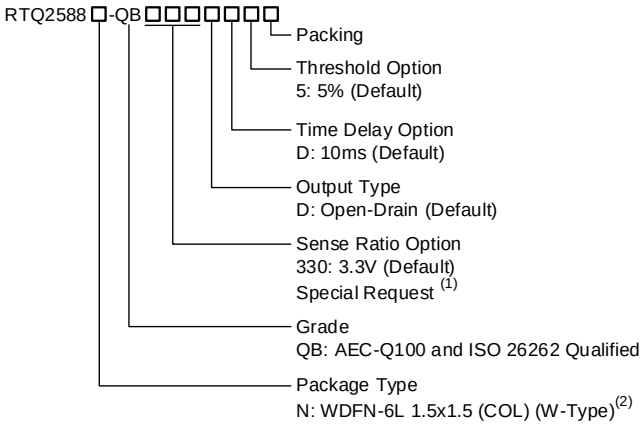
4 Simplified Application Circuit



5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Ordering Information



Note 1.

- Marked with (1) indicated Special Request: Available sensing voltage target with 50mV steps ranging from 0.5V to 1.1V; with 0.1V steps ranging from 1.2V to 5V under specific business agreement.
- Richtek products are Richtek Green Policy compliant and marked with (2) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6.1 Output Type

Code	Function
D	Open-drain type, active-low
L	Push-pull type, active-low
H	Push-pull type, active-high

6.2 Protection Type and Time Delay Option

Code	Function
A	Window, CT pin left floating = 50μs, CT pin tied to VDD = 200μs
B	Window, CT pin left floating = 1ms, CT pin tied to VDD = 20ms
C	Window, CT pin left floating = 5ms, CT pin tied to VDD = 100ms
D	Window, CT pin left floating = 10ms, CT pin tied to VDD = 200ms
E	UV only, CT pin left floating = 50μs, CT pin tied to VDD = 200μs
F	UV only, CT pin left floating = 1ms, CT pin tied to VDD = 20ms
G	UV only, CT pin left floating = 5ms, CT pin tied to VDD = 100ms
H	UV only, CT pin left floating = 10ms, CT pin tied to VDD = 200ms

6.3 Threshold Option

Code	Function
4	UV/OV = ± 4% protection threshold
5	UV/OV = ± 5% protection threshold
7	UV/OV = ± 7% protection threshold
9	UV/OV = ± 9% protection threshold

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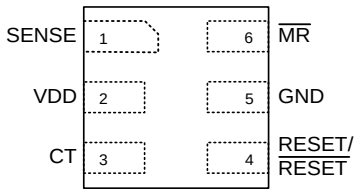
7 Pin Configuration

(TOP VIEW)

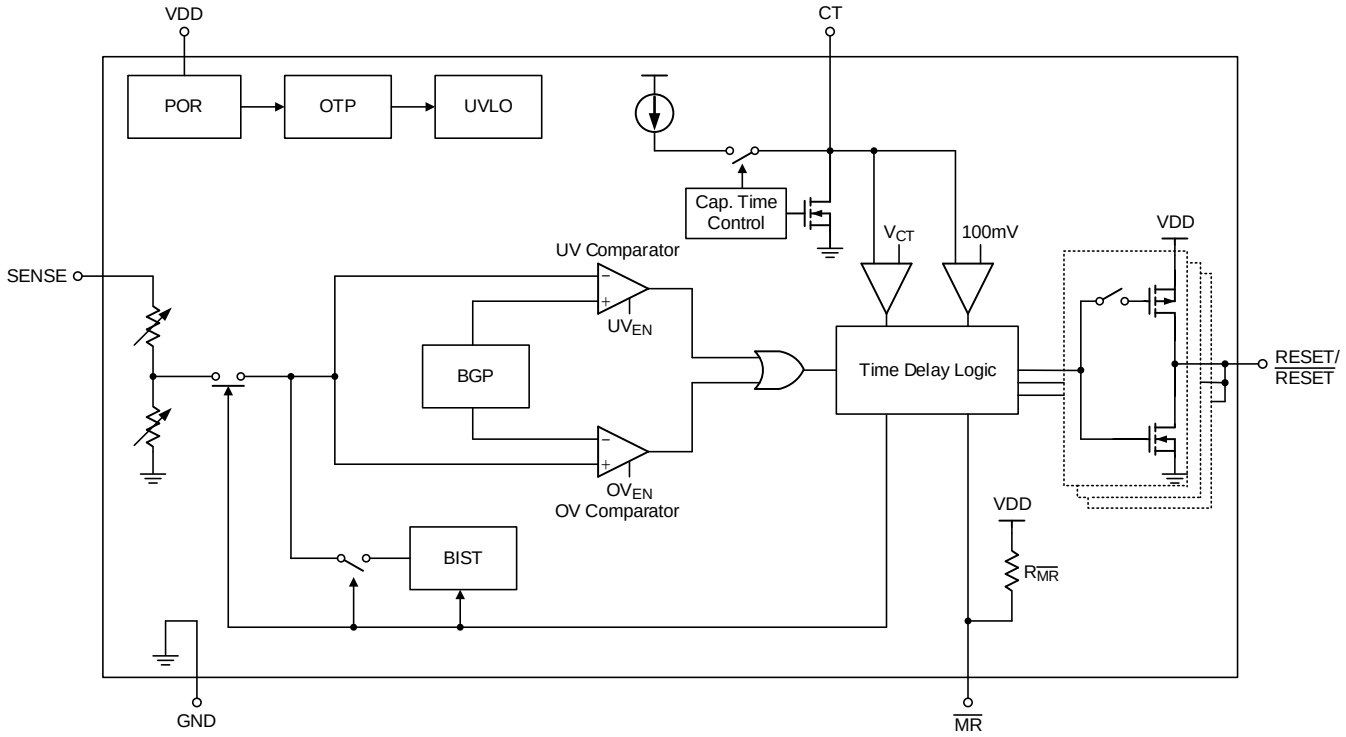


WDFN-6L 1.5x1.5 (COL)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SENSE	Input for monitoring the voltage rail. When the SENSE detects OV or UV conditions, the RESET/ $\overline{\text{RESET}}$ pin is asserted. Place a 10nF to 100nF ceramic capacitor close to this pin to improve noisy immunity.
2	VDD	Power supply input pin. Place a 0.1μF to 1μF bypass capacitor close to the VDD pin is recommended.
3	CT	Programmable pin for reset recovery time delay. When the CT pin is pulled up to VDD or left floating, it offers two fixed release time delays. Additionally, connecting an external capacitor to ground allows programming different time delays.
4	RESET/ $\overline{\text{RESET}}$	Open-drain output type for active-low; push-pull output type for active-high or active -low. This pin will be asserted when OV/UV fault is detected, the BIST fails, or the $\overline{\text{MR}}$ pin is asserted low. If the open-drain output type is in use, connect it to the desired pull-up voltage with a pull-up resistor. On the other hand, if the push-pull output type is in use, no external pull-up resistor is needed.
5	GND	Ground pin.
6	$\overline{\text{MR}}$	Manual reset pin. If this pin is pulled low, the RESET/$\overline{\text{RESET}}$ output will be asserted. After the $\overline{\text{MR}}$ pin is de-asserted, the output will go high or low after the reset recovery time delay (t_D) expires. It can be left floating when not in use.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VDD, SENSE, RESET/$\overline{\text{RESET}}$, $\overline{\text{MR}}$, CT ---------- –0.3V to 6V
- $I_{RESET/\overline{RESET}}$ ---------- ±20mA
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 4)

- Supply Voltage, V_{DD} ---------- 1.7V to 5.5V
- Sense Voltage, V_{SENSE} ---------- 0.5V to 5V
- Output Voltage, $V_{RESET/\overline{RESET}}$ ---------- 0V to 5.5V
- $\overline{\text{MR}}$ Voltage, $V_{\overline{MR}}$ ---------- 0V to 5.5V
- CT Voltage, V_{CT} ---------- Follow to V_{DD}
- $I_{RESET/\overline{RESET}}$ ---------- –5mA to 5mA
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

12 Thermal Information

(Note 5)

Thermal Parameter		WDFN-6L 1.5x1.5 (COL)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	169.67	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	217.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	42.4	°C/W
θ_{JB}	Junction-to-board thermal resistance	71.9	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

13 Electrical Characteristics

(T_A = T_J = –40°C to 125°C, $V_{\overline{RESET}}$ = 10kΩ to V_{DD}, the CT and $\overline{MR}$ pins are open, Reset load = 10pF. Typical condition is V_{DD} = 3.3V, VDD ramp rate ≤ 6V/μs with ΔV = 1V (Note 6), unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		1.7	--	5.5	V
Supply Current	I_{DD}	1.7V ≤ V_{DD} ≤ 5.5V	--	3.5	7	μA
Power-On Reset Voltage (Note 7)	V_{POR}	$V_{OL(max)}$ = 250mV, I_{OUT} = 15μA	--	--	1	V
Undervoltage-Lockout (Note 8)	$UVLO_F$		1.548	1.62	1.65	V
	$UVLO_R$		1.6	1.65	1.7	
Sensing Current	I_{SENSE}	V_{SENSE} = 5V	--	1	1.5	μA
Positive-Going Threshold Voltage Accuracy	V_{ACC_P}		–0.78	±0.25	0.78	%
Negative-Going Threshold Voltage Accuracy	V_{ACC_N}		–0.78	±0.25	0.78	%
Triggered Threshold Range	$V_{TH(OV)}$		4	--	9	%
	$V_{TH(UV)}$		–9	--	–4	
Hysteresis Voltage (Note 9)	V_{HYS}		0.3	0.5	0.8	%
Low Level Output Voltage	V_{OL}	V_{DD} = 1.7V, I_{OUT} = 0.4mA	--	--	350	mV
		V_{DD} = 2V, I_{OUT} = 3mA	--	--	350	
		V_{DD} = 5V, I_{OUT} = 5mA	--	--	350	
High Level Output Voltage	V_{OH}	V_{DD} = 1.7V, I_{OUT} = –0.4mA	0.8 x V_{DD}	--	--	V
		V_{DD} = 2V, I_{OUT} = –3mA	0.8 x V_{DD}	--	--	
		V_{DD} = 5V, I_{OUT} = –5mA	0.8 x V_{DD}	--	--	
Output Leakage Current	I_{LEAK}	V_{DD} = $V_{\overline{RESET}}$ = 5.5V (Open-Drain Type)	--	--	300	nA
Comparator Threshold Voltage of the CT Pin	V_{CT_TH}		1.14	1.21	1.28	V
High Level Voltage of the CT Pin	V_{CT_H}		1.4	--	--	V
Charging Current of the CT Pin	I_{CT}		320	400	495	nA
$\overline{MR}$ Logic-Low Input	$V_{\overline{MR}\_L}$		--	--	0.3	V
$\overline{MR}$ Logic-High Input	$V_{\overline{MR}\_H}$		1.4	--	--	V
Internal Pull-Up Resistance of the $\overline{MR}$ Pin	$R_{\overline{MR}}$		--	100	--	kΩ
Timing Requirements						
Reset Recovery Time Delay (A, E)	t_D	CT = Floating	35	50	65	μs
		CT = 10kΩ to V_{DD}	140	200	260	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reset Recovery Time Delay (B, F)	t_D	CT = Floating	0.7	1	1.3	ms
		CT = 10kΩ to V_{DD}	14	20	26	
Reset Recovery Time Delay (C, G)	t_D	CT = Floating	3.5	5	6.5	ms
		CT = 10kΩ to V_{DD}	70	100	130	
Reset Recovery Time Delay (D, H)	t_D	CT = Floating	7	10	13	ms
		CT = 10kΩ to V_{DD}	140	200	260	
Deglitch Time for Undervoltage $V_{TH(UV)}$, (5% Overdrive) (Note 10)	$t_{DG(VTH-)}$		--	3	--	µs
Deglitch Time for Overvoltage $V_{TH(OV)}$, (5% Overdrive) (Note 10)	$t_{DG(VTH+)}$		--	3	--	µs
Output Rising Time (Open-Drain Type) (Note 10) (Note 11)	t_R		--	300	--	ns
Output Rising Time (Push-Pull Type) (Note 10) (Note 11)	t_R		--	--	25	ns
Output Falling Time (Note 10) (Note 11)	t_F		--	--	25	ns
Propagation Time Delay (Note 10) (Note 12)	t_{PD}		--	17	45	µs
Deglitch Time for the $\overline{MR}$ Pin Low	$t_{DG(\overline{MR}\_L)}$		0.45	--	3.8	µs
Propagation Time Delay from the $\overline{MR}$ Pin Low to Assert RESET/$\overline{RESET}$	$t_{PD(\overline{MR})}$		--	1.6	4.3	µs
Pulse Low Width Duration Time of the $\overline{MR}$ Pin Low to Assert RESET/$\overline{RESET}$	$t_{PWD(\overline{MR})}$		4.5	--	--	µs
$\overline{MR}$ Release Recovery Time Delay	$t_{D(\overline{MR})}$		--	t_{BIST} + t_D	--	ms
BIST Time (Note 13)	t_{BIST}		0.7	1	1.3	ms
Startup Time Delay (Note 14)	t_{SD}	Starts up when V_{DD} > $UVLO_R$	--	150	--	µs

Note 6. The voltage on the SENSE pin remains within a ±1% range.

Note 7. V_{POR} is the minimum V_{DD} voltage level required for a controlled output state.

Note 8. The RESET/$\overline{RESET}$ pin is driven low when V_{DD} falls below $UVLO_F$.

Note 9. V_{HYS} is defined with respect to the triggered points of $V_{TH(OV)}$ and $V_{TH(UV)}$.

Note 10. 5% overdrive from threshold voltage. Overdrive (%) = $|(V_{SENSE} / V_{NOMINAL}) \times 100\% | - |V_{TH(OV\ or\ UV)}|$, where the $V_{NOMINAL}$ is the nominal setting of the sense target.

Note 11. The RESET/$\overline{RESET}$ output transitions from V_{OH} x 90% to V_{OL} for falling time, and from V_{OL} to V_{OH} x 90% for rising time.

Note 12. t_{PD} is measured from the triggered point $V_{TH(OV)}$ or $V_{TH(UV)}$ until RESET/$\overline{RESET}$ is asserted.

Note 13. Built-in self-test is initiated once V_{DD} rises above $UVLO_R$ and reaches $V_{DD(min)}$ or after the $\overline{MR}$ pin state changes from asserted to de-asserted.

Note 14. During the power-on sequence, V_{DD} must be at or above $V_{DD(min)}$ for a duration of t_{SD} + t_{BIST} + t_D before the output reaches the correct state.

Note 15. If the $\overline{MR}$ is driven to a voltage less than V_{DD}, additional current will flow into V_{DD} and out of $\overline{MR}$.

Note 16. When the CT pin is connected to the VDD pin, a pull-up resistor is required; a 10kΩ is recommended.

14 Typical Application Circuit

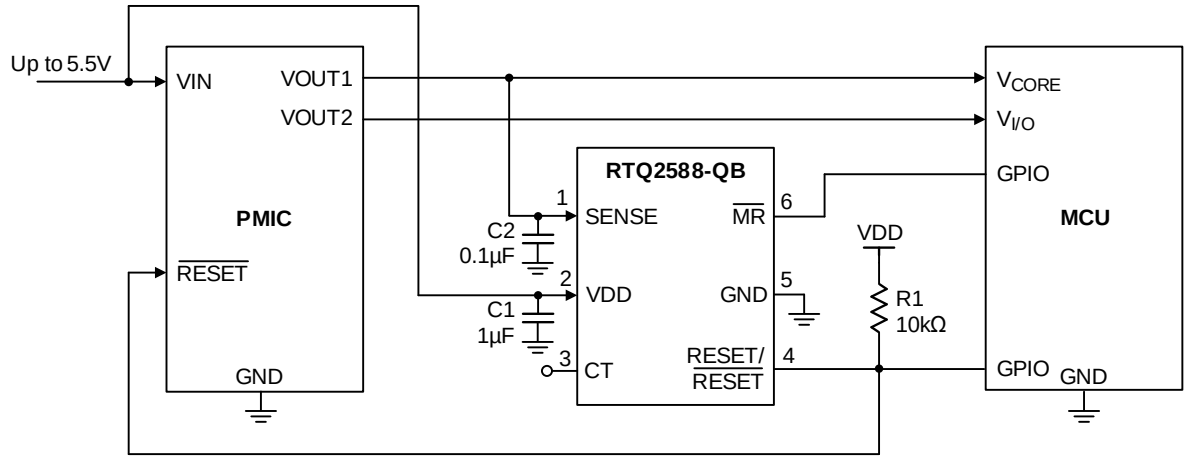
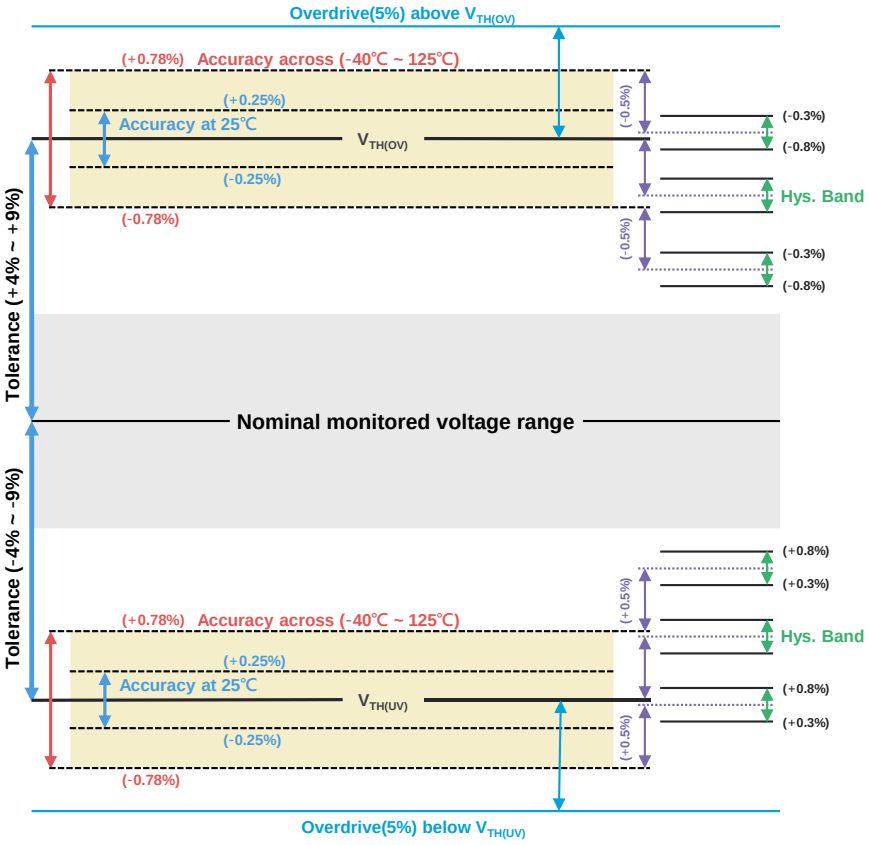
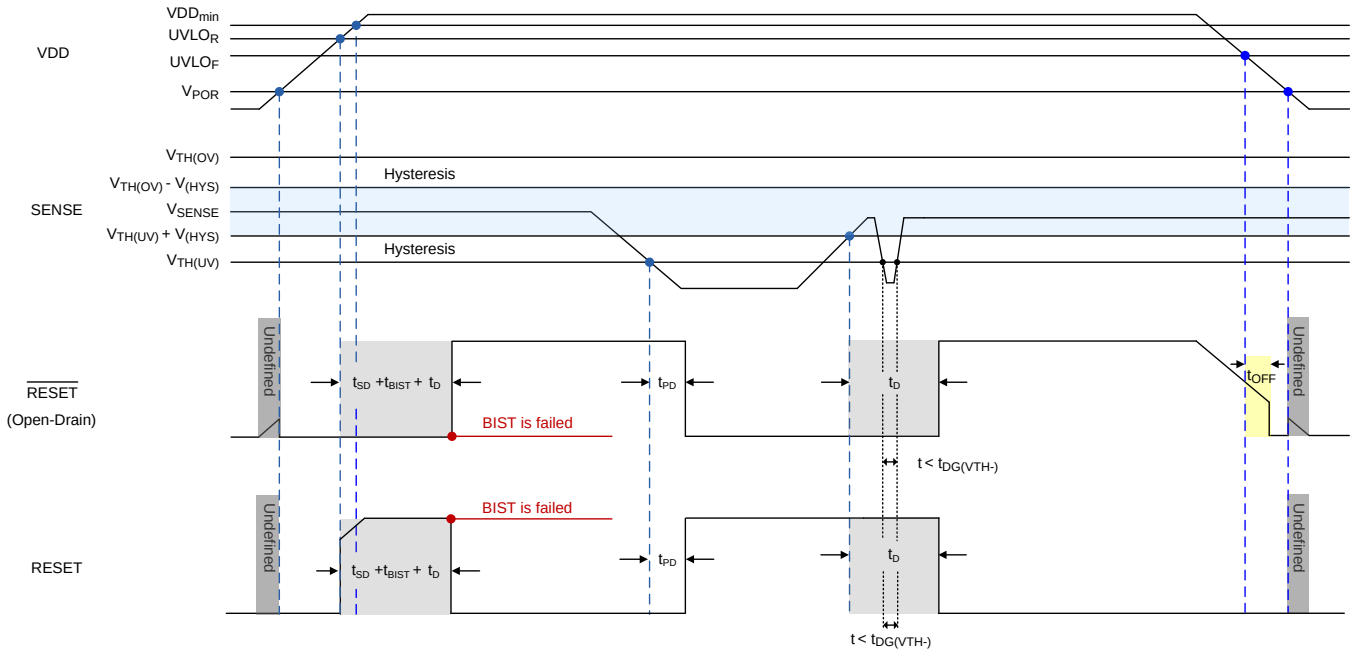


Table 1. Component List for Evaluation Board

Reference	Qty	Part Number	Description	Package	Manufacturer
C1	1	GCM155C71A105KE38	1.0µF/10V/X7S	0402	MURATA
C2	1	GCM155R71A104KA01	0.1µF/10V/X7R	0402	MURATA
R1	1	MR02X1002FAL	10kΩ/1%	0201	WALSIN

15 Timing Diagram

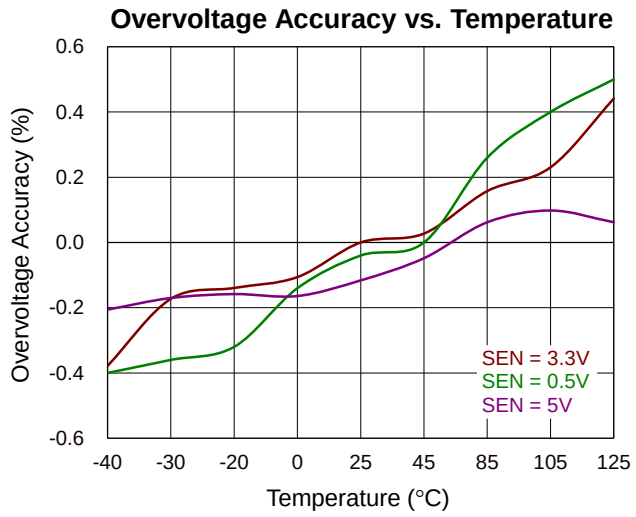


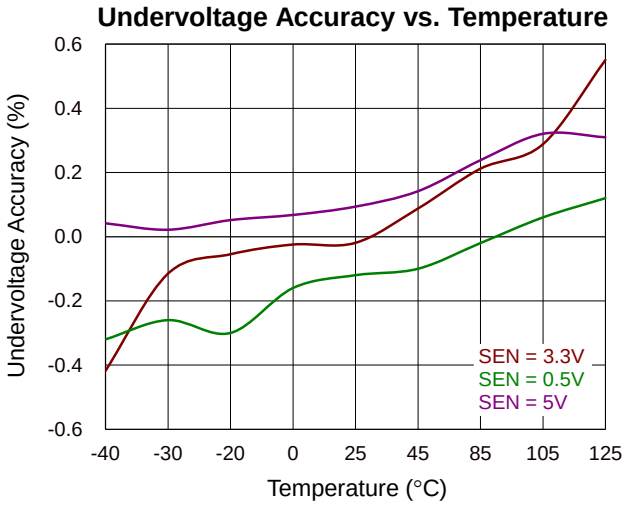


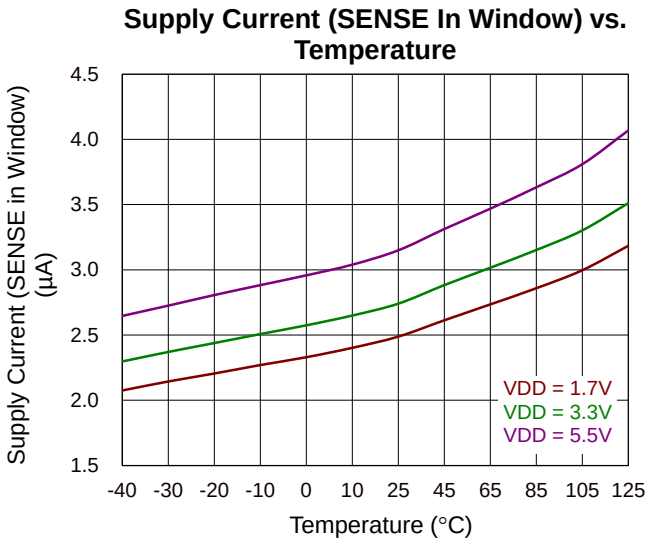
Note 17.

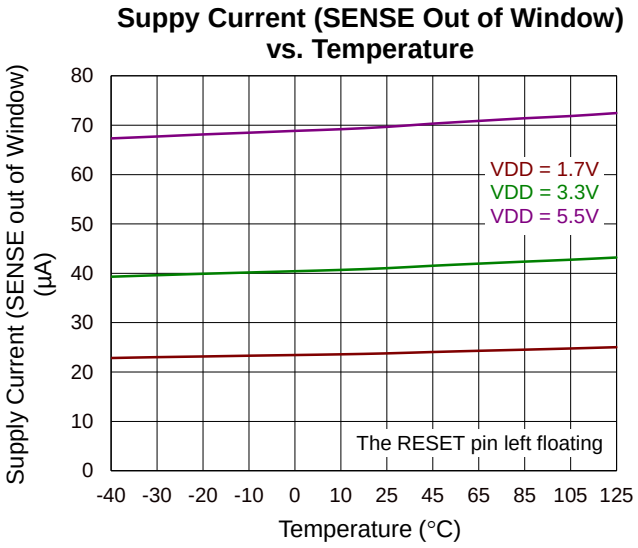
- In open-drain timing diagram, the $\overline{\text{RESET}}$ pin is connected to V_{DD} via an external pull-up resistor.
- Advised that the V_{DD} falling and rising time are much longer than the propagation time delay (t_{PD}) time.
- The typical turn-off time is 10μs when V_{DD} goes below the $UVLO_F$ threshold.

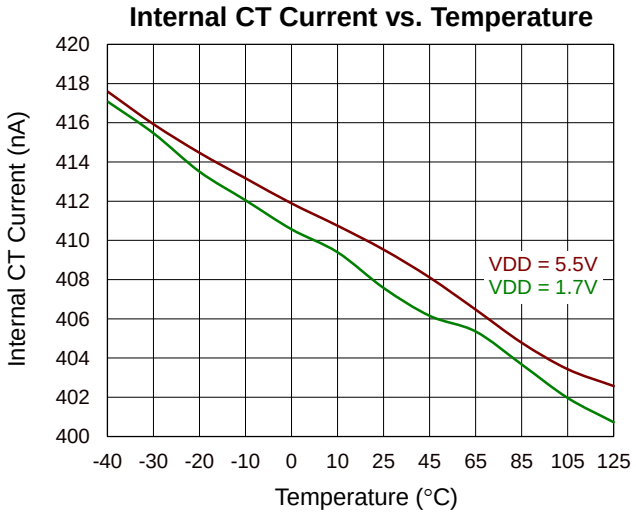
16 Typical Operating Characteristics

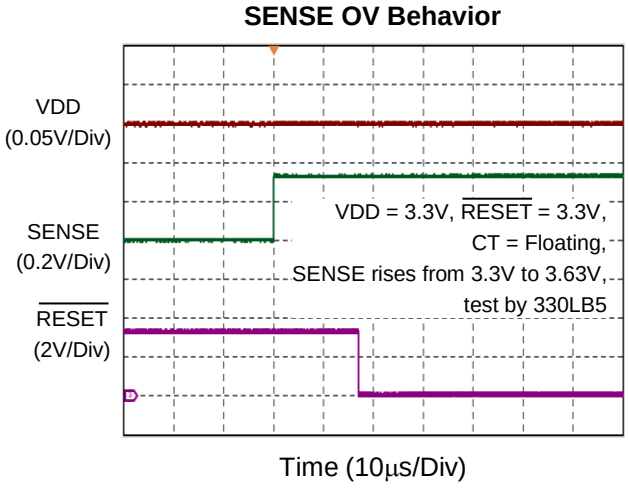




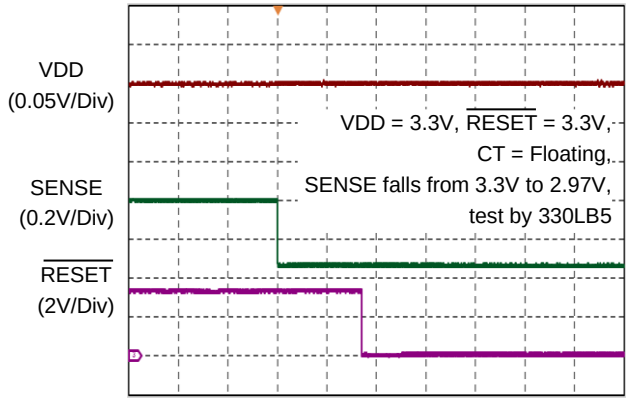






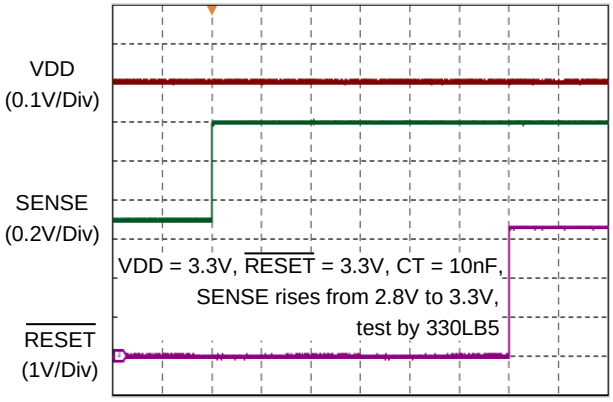


SENSE UV Behavior



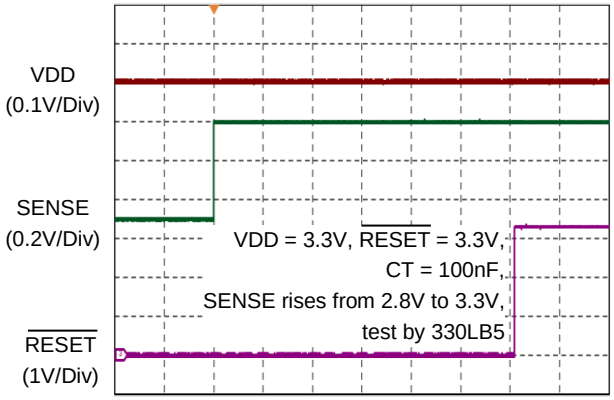
Time (10μs/Div)

RESET Recovery Time Delay, 10nF



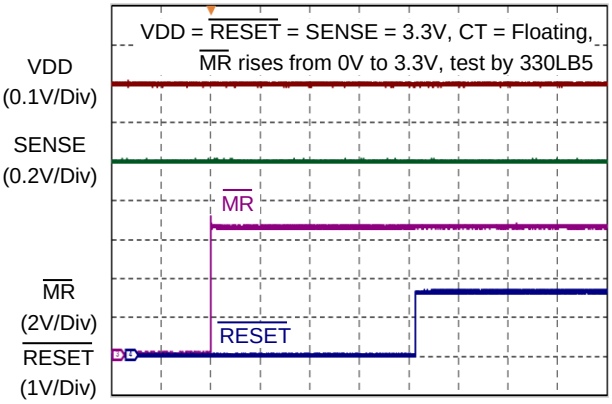
Time (5ms/Div)

RESET Recovery Time Delay, 100nF



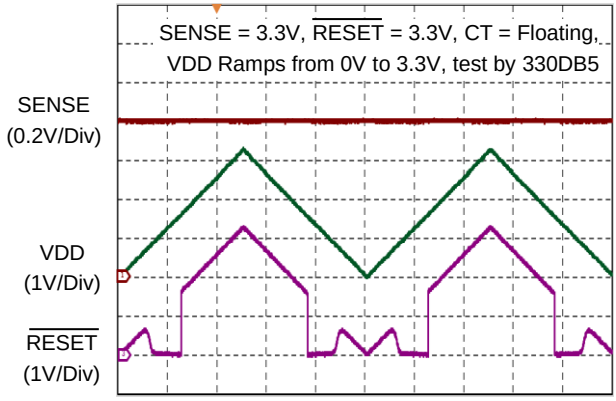
Time (50ms/Div)

MR Recovery Time Delay with BIST



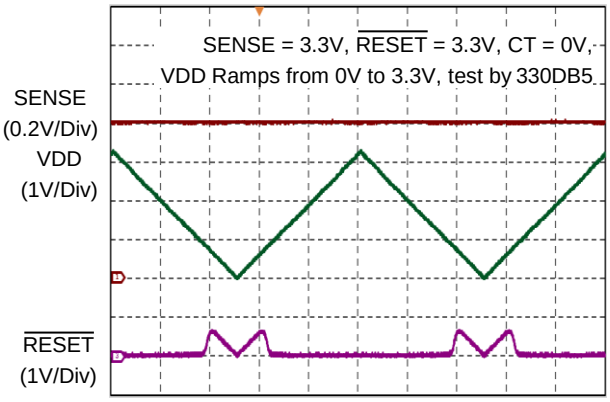
Time (0.5ms/Div)

VDD Ramp Behavior



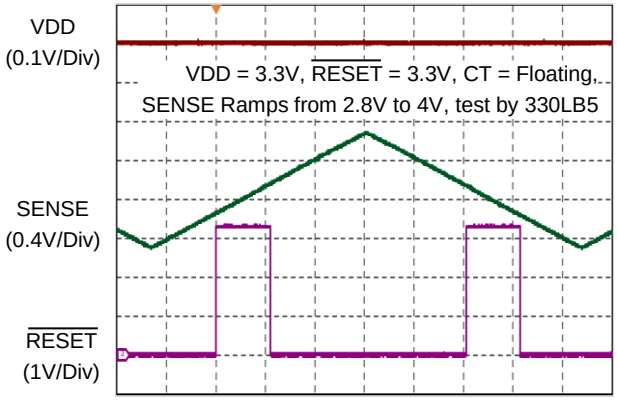
Time (2000ms/Div)

VDD Ramp Latch Behavior



Time (2000ms/Div)

SENSE Ramp OV and UV Behavior



17 Operation

The RTQ2588-QB features an internal window comparator that accurately monitors overvoltage and undervoltage conditions within a maximum tolerance of ±0.78%. It supports a variety of sensing voltage targets without requiring external voltage divider resistors, offering protection threshold options to facilitate easy integration for system designers.

The device provides four reset recovery time settings: each setting offers a different fixed recovery time when the CT pin is left floating, or connected to VDD through a resistor, and supports programmable recovery time when the CT pin is connected to GND through a capacitor.

System designers can choose between two output types: open-drain and push-pull, depending on the application requirements.

For automotive functional safety, the RTQ2588-QB includes a Built-In Self-Test (BIST) function that serves as a safety mechanism to improve the system's latent point fault metrics (LPFM) scores.

17.1 SENSE

The RTQ2588-QB equips with precision-trimmed voltage-divider resistors and a high-accuracy reference voltage, making the internal window comparator ideal for high-precision applications. To enhance noise immunity, despite the inherent hysteresis band of the comparator, it is recommended to place a bypass MLCC capacitor ranging from 10nF to 100nF at the SENSE pin to reduce the impact of transient voltages on the monitored signal.

17.2 Capacitor Time (CT)

The RTQ2588-QB offers four factory-trimmed settings, allowing system designers to select the appropriate reset recovery time delay for their applications. For added flexibility, the CT pin can be left floating, connected to VDD via a resistor, or grounded through a capacitor, with each configuration yielding a different reset recovery time delay.

The reset recovery time delay is re-evaluated each time the monitored voltage enters from outside to inside the window ($V_{TH(UV)}$ < V_{SENSE} / $V_{NOMINAL}$ (%) < $V_{TH(OV)}$). This assessment is managed by an internal state machine that determines the setting based on the CT pin configuration.

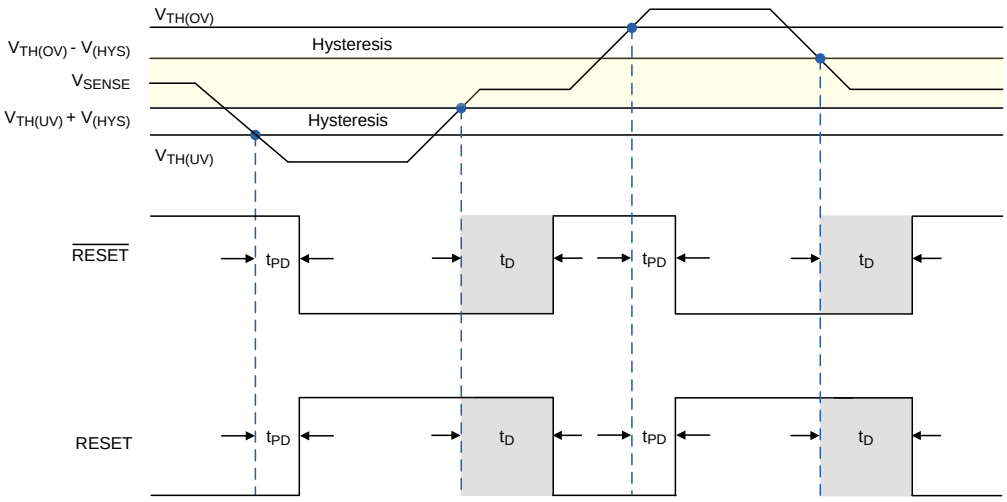
If the CT pin is required to be pulled up to VDD, a 10kΩ pull-up resistor is recommended.

17.3 RESET/$\overline{\text{RESET}}$

The RTQ2588-QB provides two factory-trimmed output type options to suit application needs, allowing selection of the appropriate output asserted behavior for overvoltage (OV) or undervoltage (UV) conditions.

For the open-drain output type, a pull-up resistor is required to connect to the appropriate voltage rail, with a 10kΩ resistor being the recommended value. Normally, the output remains high by default and is driven low when a fault is detected or $\overline{\text{MR}}$ is asserted.

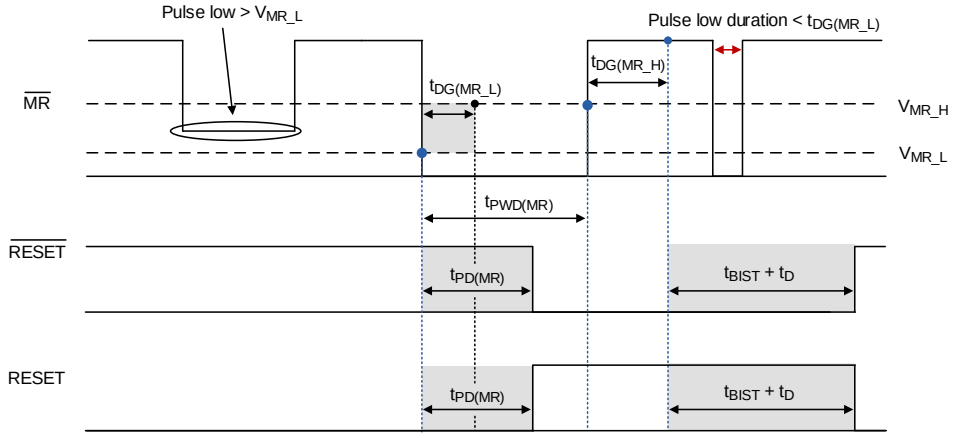
Conversely, the push-pull output type eliminates the need for a pull-up resistor and offers two asserted behaviors: active-low and active-high, accommodating different design requirements.



17.4 Manual Reset ($\overline{MR}$)

The manual reset ($\overline{MR}$) input pin can be utilized by a processor or other logic circuits to initiate a hard reset.

A logic-low control input will assert the reset output; a logic-high control input, combined with the monitored voltage on the SENSE pin being within the window ($V_{TH(UV)}$ < V_{SENSE} / $V_{NOMINAL}$ (%) < $V_{TH(OV)}$), will deassert the reset output after the reset recovery time delay (t_D) and built-in self-test (BIST) time (t_{BIST}). If the $\overline{MR}$ pin is not in use, it can either be left floating or connected to V_{DD}.



a. The monitored voltage on SENSE is within the window.

b. Following the “a”, $\overline{MR}$ must be at or above $V_{\overline{MR}\_H}$ for the time reset counter to be initiated.

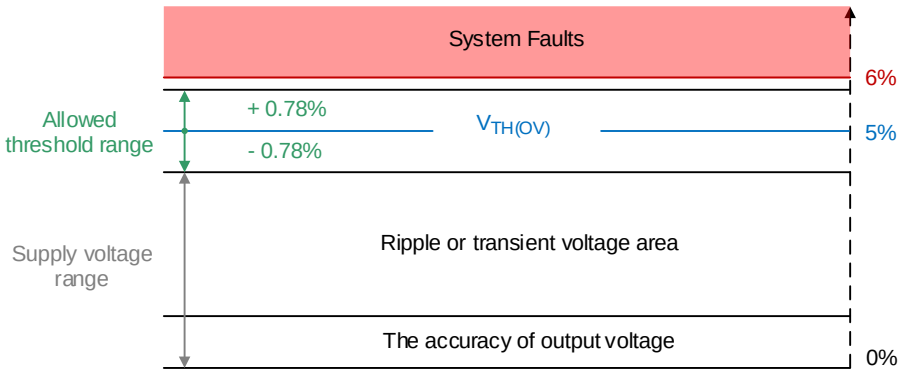
c. $\overline{MR}$ is ignored while the reset output is asserted.

18 Application Information

(Note 18)

18.1 Voltage Protection Threshold Accuracy

The RTQ2588-QB features high voltage accuracy, making it suitable for loose power supply designs. This flexibility allows system designers to use the smaller passive components (for example, capacitors or inductors) for tight voltage margin applications.



18.2 Reset Recovery Time Delay Determination

The RTQ2588-QB offers factory-set timing options with high-precision reset recovery delay timing, providing system designers with reliable settings. The recommended settings are shown below.

Option	RESET/$\overline{\text{RESET}}$ Recovery Time Delay (t_D)			Unit
	CT = Floating	CT = 10kΩ to V_{DD}	CT = Capacitor	
A, E	50	200	N/A	μs
B, F	1	20	Depends on cap. value	ms
C, G	5	100	Depends on cap. value	ms
D, H	10	200	Depends on cap. value	ms

In addition, the RTQ2588-QB reset recovery time delay can be programed by using the internal current source (I_{CT}) to charge external capacitor, and through the internal comparator to compare and determine. The ideal capacitor value can be calculated using Equation 1 to determine the reset recovery time delay, where the external capacitor is in nanofarad (nF) and t_D is in millisecond (ms):

$$t_{D(Typ)}\ (ms) = 1.21\ (V) \times C\ (nF) / 0.4\ (\mu A) \qquad (1)$$

When the faults/manual reset conditions are cleared, the internal current source is enabled to charge the external capacitor on the CT pin until V_{CT_TH} = 1.21V (typical) and RESET/$\overline{\text{RESET}}$ is deasserted.

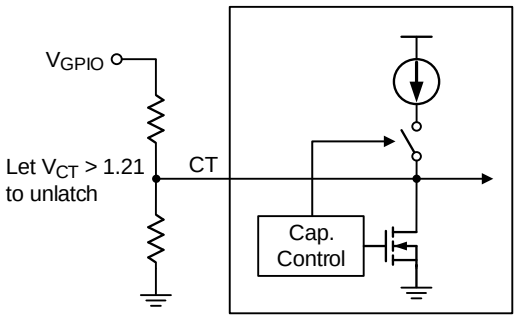
Note that it is suggested to use a X7R, or C0G capacitor and minimize the board parasitic capacitance on the CT pin to achieve precise reset recovery time delay.

Capacitor on the CT Pin	Reset Recovery Time Delay (Typical)
660pF	2ms
1nF	3ms
3.3nF	10ms
100nF	302.5ms
1μF	3025ms

The selection of the minimum capacitor value is constrained by the preset time of the floating state in different reset recovery time delay options.

18.3 Latch Mode on the RESET/$\overline{\text{RESET}}$ Pin

The RTQ2588-QB features a latch mode on the RESET/$\overline{\text{RESET}}$ pin when the CT pin is pulled low to ground. In this mode, the RESET/$\overline{\text{RESET}}$ pin remains in an asserted state regardless of V_{SENSE} being within the in-window range, until a voltage exceeding V_{CT_TH} is applied to the CT pin. This action immediately releases the latch, causing the RESET/$\overline{\text{RESET}}$ pin to go to a deasserted state with no delay. For effective unlatching, apply a voltage greater than 1.21V to the CT pin, using a series voltage-divider resistor to limit the current.



18.4 Functional Safety Support Capable

Aiming to enhance the latent point fault metric (LPFM) score of function safety systems, the RTQ2588-QB features the built-in self-test (BIST) function to diagnose the internal OV/UV function and ensure they maintain normal functionality. This safety mechanism will be enabled and perform a one-time BIST (typical 1ms duration) when VDD rises above $UVLO_R$ or manual reset ($\overline{MR}$) is cleared by an external device. If BIST fails, the RESET/$\overline{\text{RESET}}$ pin will remain in an asserted state.

Furthermore, to improve product reliability, the RTQ2588-QB incorporates a redundant, parallel push-pull structure with multiple sets.

18.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-6L 1.5x1.5 (COL) package, the thermal resistance, θ_{JA}, is 169.67°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (169.67°C/W) = 0.59W for a WDFN-6L 1.5x1.5 (COL) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

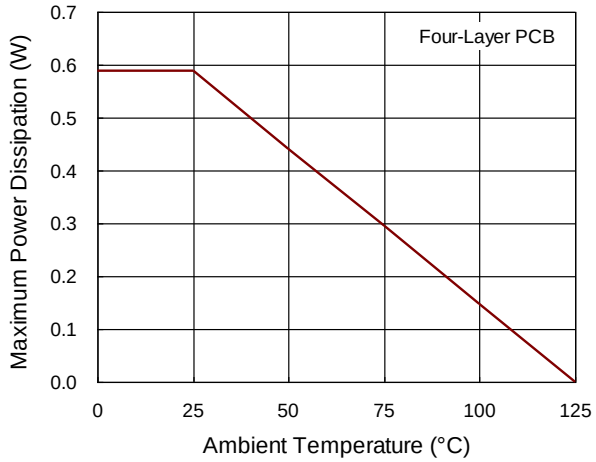


Figure 1. Derating Curve of Maximum Power Dissipation

18.6 Layout Considerations

To ensure accurate voltage monitoring, adhere to the following PCB layout guidelines:

- Keep the trace from the sensing target as short as possible to minimize the effects of parasitic resistance and inductance.
- Position the capacitors near the VDD, SENSE, and CT pins to enhance noise immunity and achieve precise programmable reset recovery time delays.
- Do not place the RTQ2588-QB above layers with high-speed switching traces; it should be separated by a ground layer.
- Ensure the SENSE trace is as far away from high-speed signal traces as possible to avoid interference.

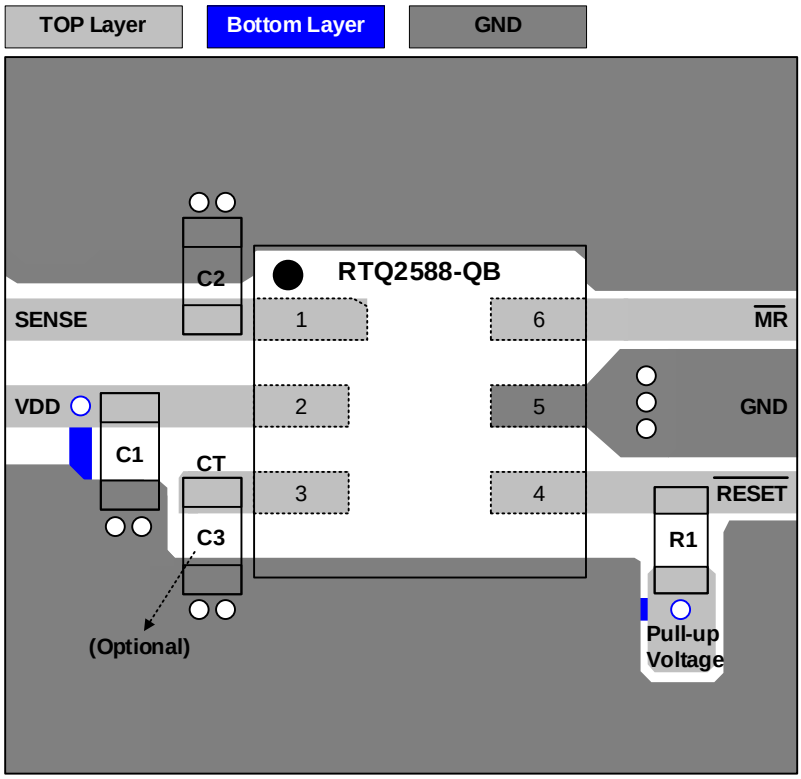
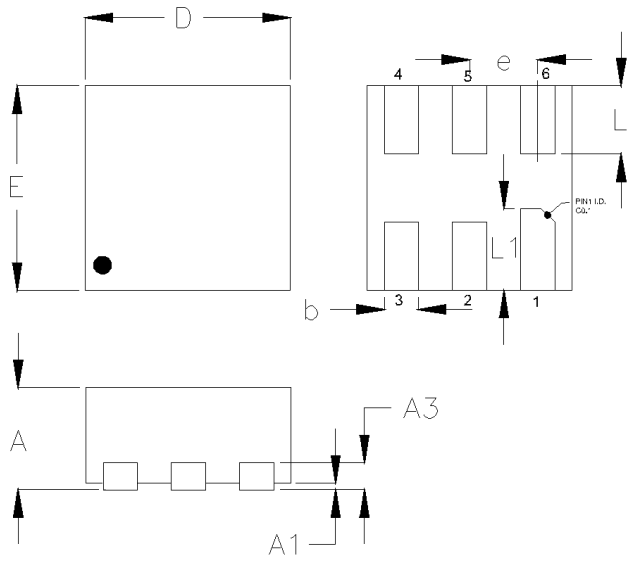


Figure 2. Layout Guide

Note 18. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

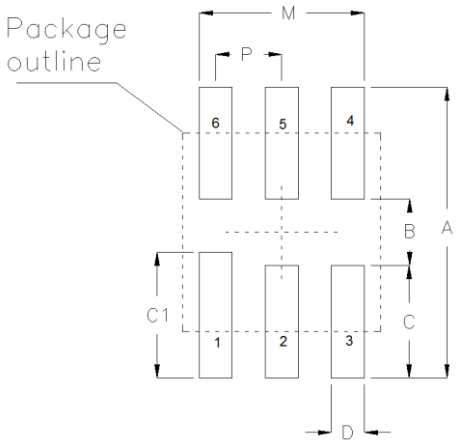
19 Outline Dimension



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A3	0.175	0.203	0.250	0.007	0.008	0.010
b	0.200	0.250	0.300	0.008	0.010	0.012
D	1.450	1.500	1.550	0.057	0.059	0.061
E	1.450	1.500	1.550	0.057	0.059	0.061
e	0.500			0.020		
L	0.450	0.500	0.550	0.018	0.020	0.022
L1	0.550	0.600	0.650	0.022	0.024	0.026

W-Type 6L DFN 1.5x1.5 Package (COL)

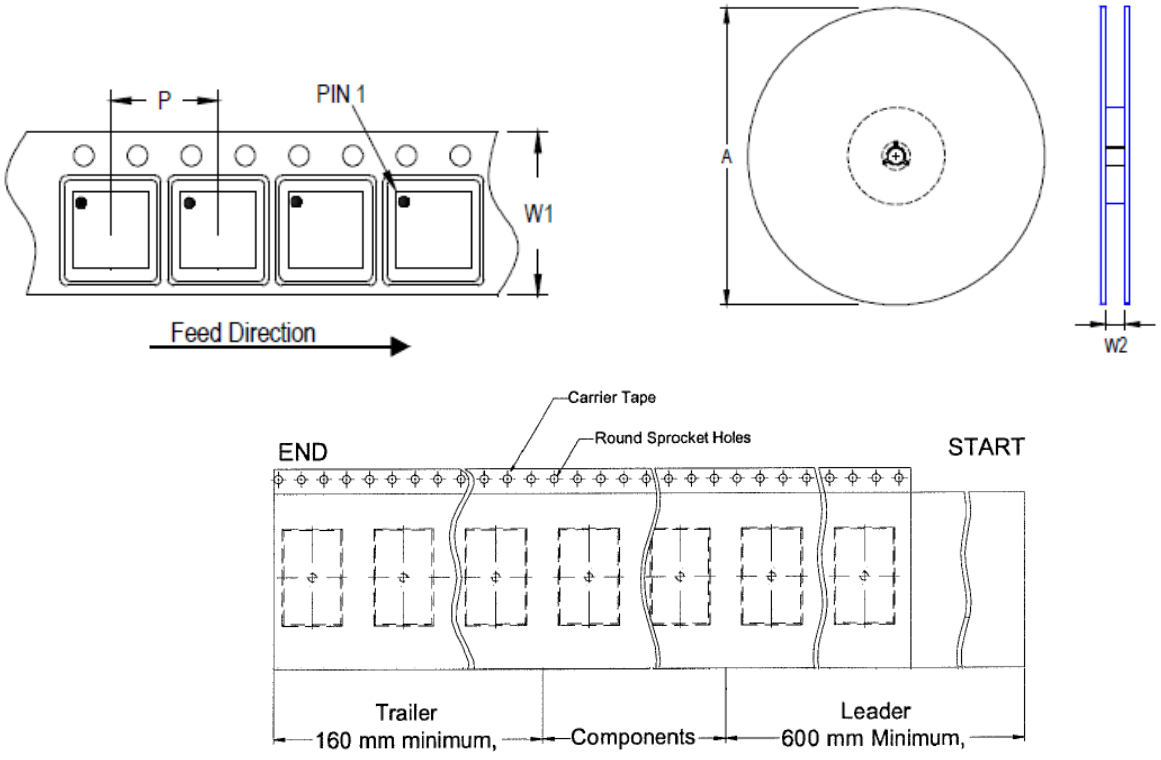
20 Footprint Information



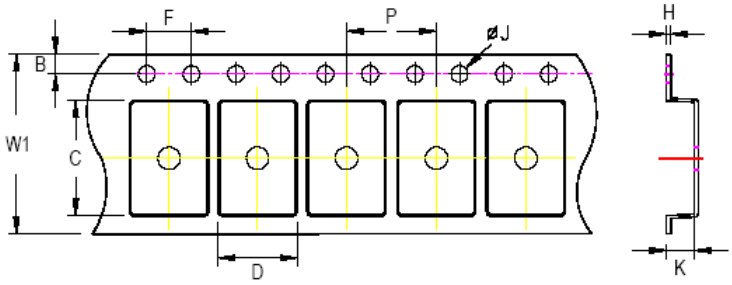
Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P	A	B	C	C1	D	M	
V/W/U/XDFN1.5x1.5-6(COL)	6	0.50	2.20	0.50	0.85	0.95	0.25	1.25	±0.05

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 1.5x1.5	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 1.5x1.5	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/29	Final	Title on P1 Ordering Information on P2 Functional Block Diagram on P6 Electrical Characteristics on P8 Note 10 on P9 Typical Operating Characteristics on P14 Operation on P16, 17 Application Information on P19