RICHTEK®

RTQ2104-QA

36V$_{IN}$, 3A, High Efficiency, 2.1MHz, Synchronous Buck Converter with Low Quiescent Current

1 General Description

The RTQ2104-QA is a 3A, high-efficiency, current mode synchronous buck converter, which is optimized for automotive applications. The device operates with input voltages from 4V to 36V and is protected from load dump transients up to 42V, eases input surge protection design. The device can program the output voltage between 0.8V to V_{IN}. The low quiescent current design with the integrated low $R_{DS(ON)}$ power MOSFETs achieves high efficiency over the wide load range. The peak current mode control with simple internal compensation allows the use of small inductors and results in fast transient response and good loop stability.

The ultra-low minimum on-time enable constant-frequency operation even at very high step-down ratios. The build-in spread spectrum frequency modulation further helping systems designers with better EMC management.

The RTQ2104-QA provides complete protection functions such as input undervoltage-lockout, output undervoltage protection, overcurrent protection, and over-temperature protection. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RTQ2104-QA is available in SOP-8 (Exposed Pad) package. The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

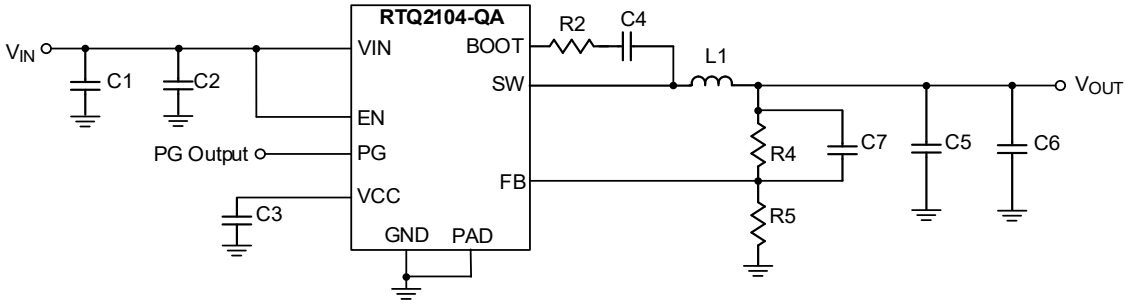
2 Features

- **AEC-Q100 Grade 1 Qualified**
- **Wide Input Voltage Range**
  - **4V to 36V**
- **Wide Output Voltage Range: 0.8V to V_{IN}**
- **Maximum Output Current: 3A**
- **Peak Current Mode Control**
- **Integrated 80mΩ Switch and 80mΩ Synchronous Rectifier**
- **Low Quiescent Current: 40μA**
- **Fast 60ns Minimum Switch On-Time**
- **Ultra-Short 65ns Minimum Switch Off-Time**
- **Fixed Switching Frequency: 2.1MHz**
- **PSM/FPWM at Light Load by Part Number Option**
- **Built-In Spread Spectrum Frequency Modulation for Low EMI**
- **Power-Good Indication**
- **Enable Control**
- **0.8V ±1.5% Reference Accuracy**
- **Adjacent Pin-Short Protection**
- **Built-In UVLO, OCP, UVP, OTP**

3 Applications

- Automotive Systems
- Car Camera Module and Car Cockpit Systems
- Connected Car Systems
- Point of Load Regulator in Distributed Power Systems
- Digital Set-Top Boxes
- Broadband Communication Equipment

4 Simplified Application Circuit



5 Ordering Information

RTQ2104 □□□-QA

Grade
QA : AEC-Q100 Qualified and Screened by High Temperature

Package Type(1)
SP : SOP-8 (Exposed Pad)
(Exposed Pad-Option 2)

Lead Plating System
G: Richtek Green Policy Compliant(2)

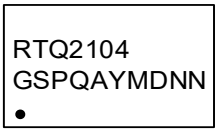
PWM Operation Mode
Default : Automatic PSM
B : Forced PWM

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

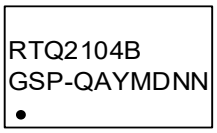
6 Marking Information

RTQ2104GSP-QA



RTQ2104GSPQA : Product Code
YMDNN : Date Code

RTQ2104BGSP-QA

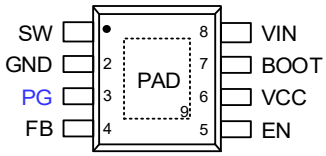


RTQ2104BGSP-QA : Product Code
YMDNN : Date Code

Table of Contents

7 Pin Configuration

(TOP VIEW)

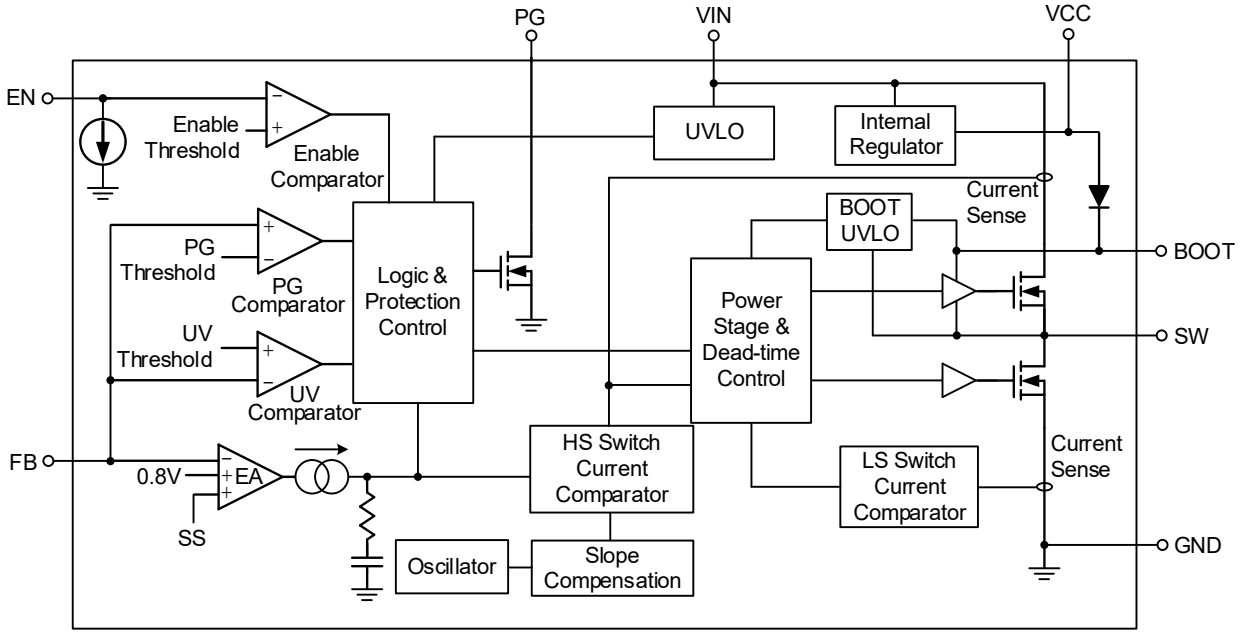


SOP-8 (Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch node. SW is the switching node that supplies power to the output and connect the output LC filter from SW to the output load.
2	GND	Ground. Provide the ground return path for the control circuitry and low-side power MOSFET. Connect this pin to the negative terminals of the input capacitor and output capacitor.
3	PG	Open-drain power-good indication output. Once soft-start is finished, PG will be pulled low to ground if any internal protection is triggered.
4	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at a feedback reference voltage, typically 0.8V.
5	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
6	VCC	Linear regulator output. VCC is the output of the internal 5V linear regulator powered by VIN. Decouple with a 1μF, X7R ceramic capacitor from VCC to ground for normal operation.
7	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF, X7R ceramic capacitor in series with a 10Ω resistance between this pin and SW pin.
8	VIN	Power input. The input voltage range is from 4V to 36V after soft-start is finished. Connect input capacitors between this pin and GND. It is recommended to use a 4.7μF, X7R and a 0.1μF, X7R capacitors.
9 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the device.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 42V
- Switch Voltage, SW ---------- –0.3V to 42V

  <50ns ---------- –5V to 46.3V
- BOOT Voltage, V_{BOOT} ---------- –0.3V to 48V
- BOOT to SW, $V_{BOOT} - V_{SW}$ ---------- –0.3V to 6V
- EN, Voltage ---------- –0.3V to 42V
- PWM Input, V_{PWM} ---------- –0.3V to 6.8V
- Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 4V to 36V
- Output Voltage ---------- 0.8V to VIN*

  VIN*: $0.99 \times (V_{IN} - I_{OUT}(max) \times R_{DSON(max)})$
- Junction Temperature Range ---------- –40°C to 150°C
- Ambient Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		SOP-8	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	36.7	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	51.8	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	1.63	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	26.07	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	2.87	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.81	°C/W

Note 5. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 100mm, four-layer PCB with 2 oz. Cu on the outer layers and 1 oz. Cu on the inner layers. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

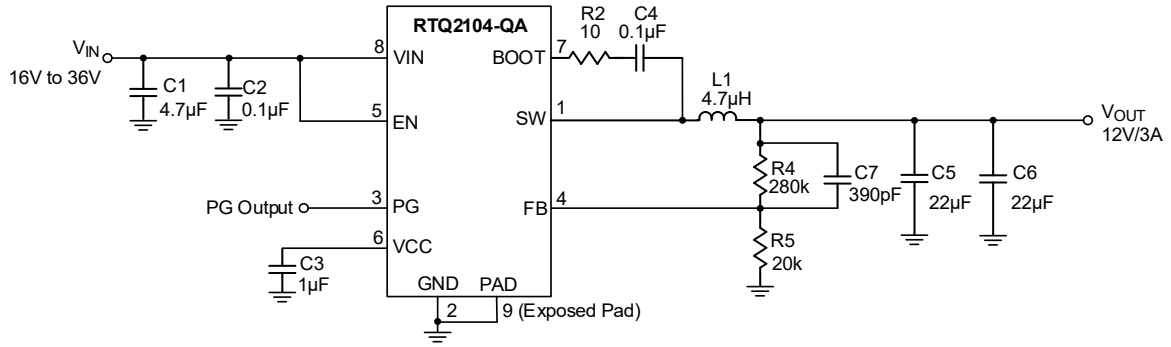
(V_{IN} = 12V, T_A = T_J = –40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Voltage	V_{IN}		4	--	36	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	3.6	3.8	4	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}	V_{IN} falling	2.7	2.85	3	
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
RTQ2104-QA Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.82V, not switching, PSM	--	40	50	μA
RTQ2104-QAB Quiescent Current		V_{EN} = 2V, V_{FB} = 0.82V, not switching, FPWM	--	1.2	--	mA
Output Voltage						
Reference Voltage	V_{REF}	4V < V_{IN} < 36V, PWM T_A = T_J = 25°C	0.792	0.8	0.808	V
		4V < V_{IN} < 36V, PWM T_A = T_J = –40°C to 125°C	0.788	0.8	0.812	
Enable Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}	V_{EN} rising	1.15	1.25	1.35	V
EN Input Voltage Falling Threshold	V_{EN_F}	V_{EN} falling	0.9	1.05	1.15	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	V_{BOOT} – V_{SW} = 4.8V Min. Duty Cycle	4.25	5	5.75	A
Negative Inductor Peak Current Limit	$I_{LIM\_PEAK\_NEG}$	From drain to source	--	2	--	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching						
Switching Frequency	f_{SW}		1.89	2.1	2.31	MHz
Minimum On-Time	t_{ON_MIN}		--	60	80	ns
Minimum Off-Time	t_{OFF_MIN}		--	65	80	ns
Internal MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	80	150	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	80	150	mΩ
High-Side Switch Leakage Current	I_{LK_H}	V_{EN} = 0V, V_{SW} = 0V	--	--	1	μA
Soft-Start						
Soft-Start Period	t_{SS}	10% to 90%	1.4	2	2.6	ms
Power-Good						
Power-Good Voltage Threshold	V_{TH_PGLH1}	V_{FB} rising, % of V_{REF}, PG from low to high	85	90	95	%
	V_{TH_PGHL1}	V_{FB} rising, % of V_{REF}, PG from high to low	--	120	--	
	V_{TH_PGHL2}	V_{FB} falling, % of V_{REF}, PG from high to low	80	85	90	%
	V_{TH_PGLH2}	V_{FB} falling, % of V_{REF}, PG from low to high	--	117	--	
Power-Good Leakage Current	I_{LK_PG}	PG signal good, V_{FB} = V_{REF}, V_{PG} = 5.5V	--	--	0.5	μA
Power-Good Sink Current Capability	I_{SK_PG}	PG signal fault, I_{PG} sinks 2mA	--	--	0.3	V
Spread Spectrum						
Spread Spectrum Range	f_{SS}		--	6	--	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	175	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C
Output Undervoltage Protection						
Output Undervoltage Protection Threshold	V_{UVP}	UVP detect	0.35	0.4	0.45	V

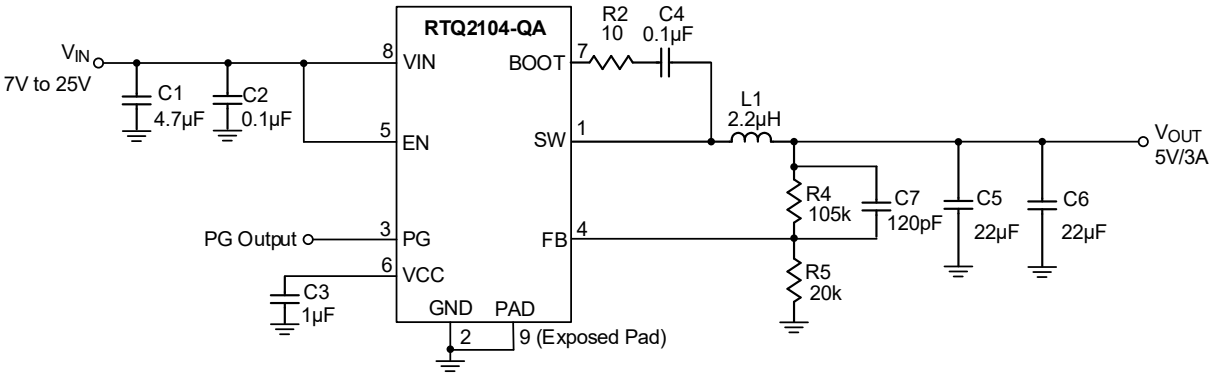
15 Typical Application Circuit

15.1 12V, 3A Buck Converter



L1 = WE-78439346047 / Cyntec-VCHA075D-4R7MS6
C5/C6 = GCM32EC71E226KE36L
C1 = GRM31CR71H475KA12L

15.2 5V, 3A Buck Converter

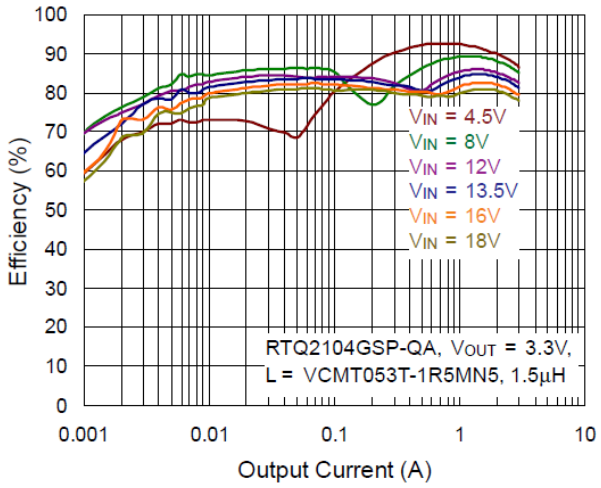


L1 = WE-78439344022 / Cyntec-VCMT063T-2R2MN5
C5/C6 = GRM31CR71A226KE15L
C1 = GRM31CR71H475KA12L

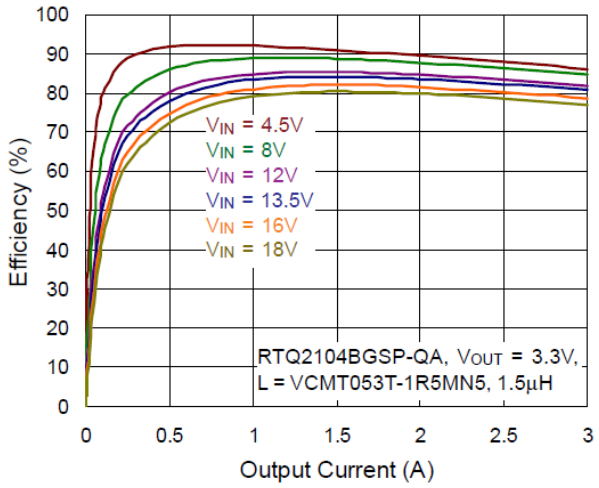
16 Typical Operating Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C. Specified temperatures are ambient.

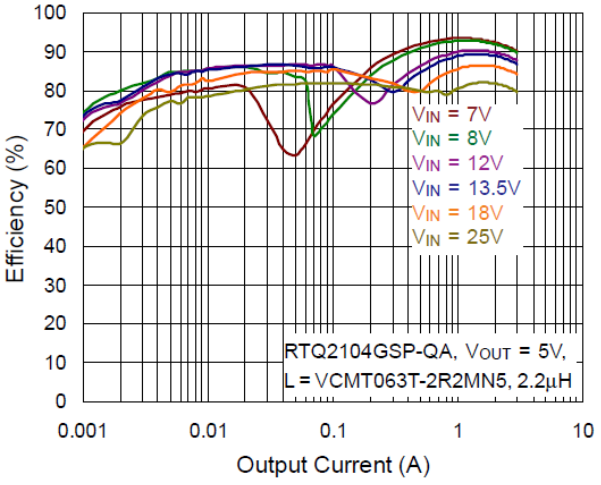
Efficiency vs. Output Current



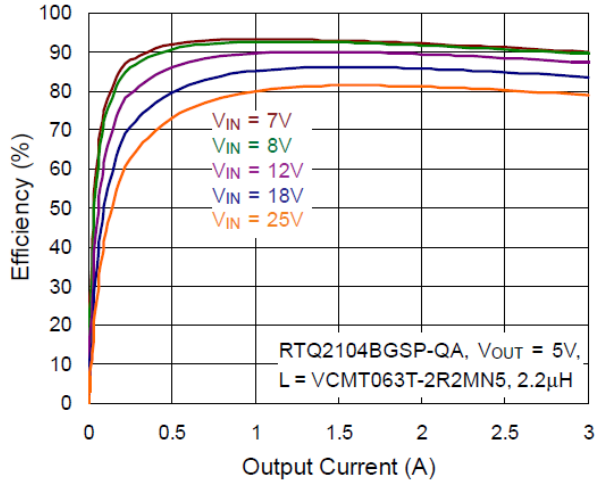
Efficiency vs. Output Current



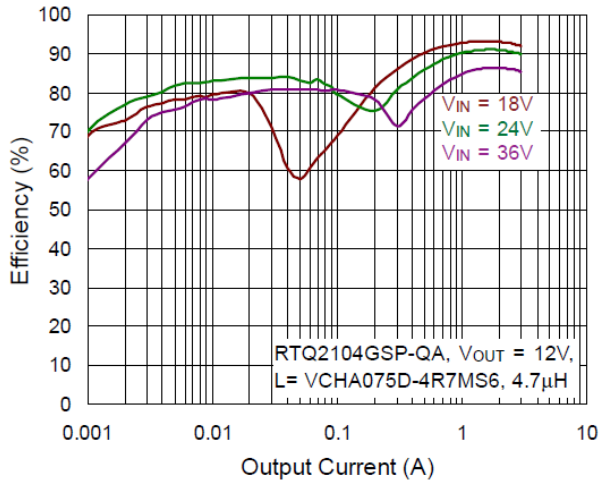
Efficiency vs. Output Current



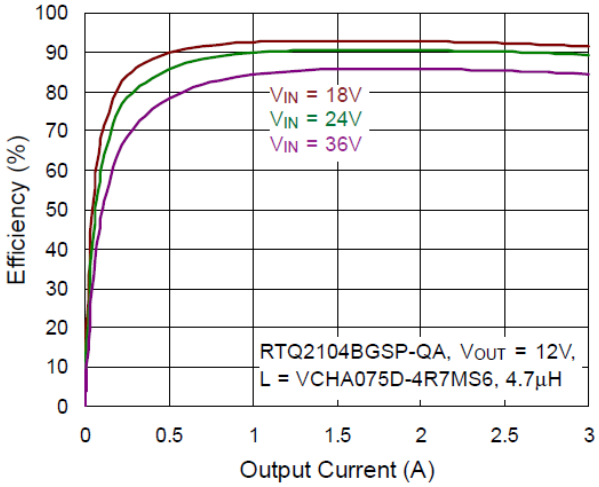
Efficiency vs. Output Current



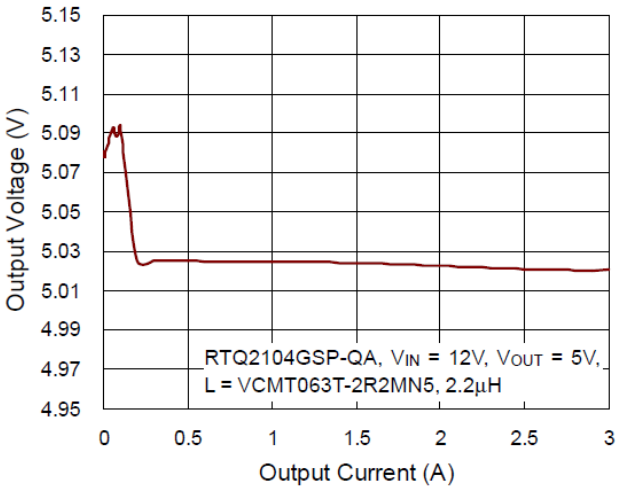
Efficiency vs. Output Current



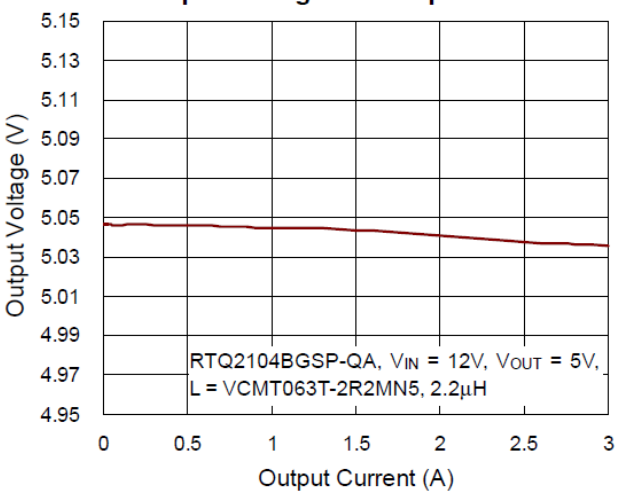
Efficiency vs. Output Current



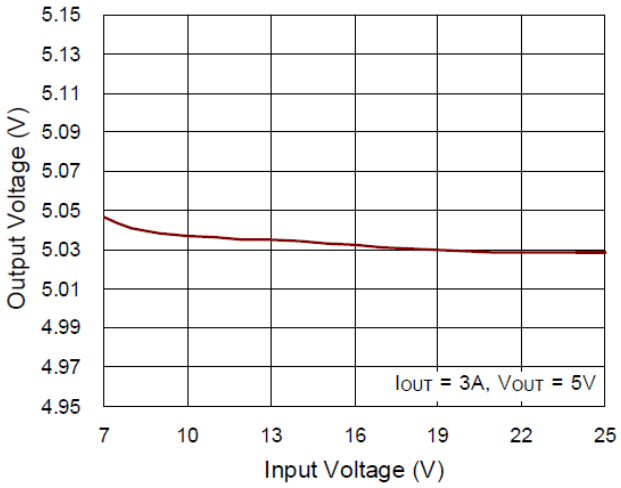
Output Voltage vs. Output Current



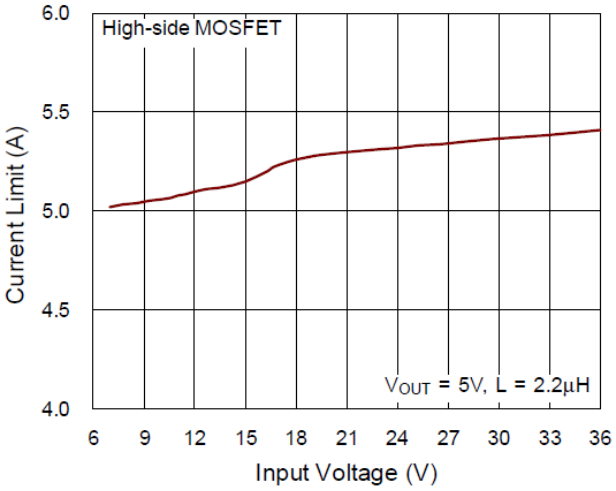
Output Voltage vs. Output Current



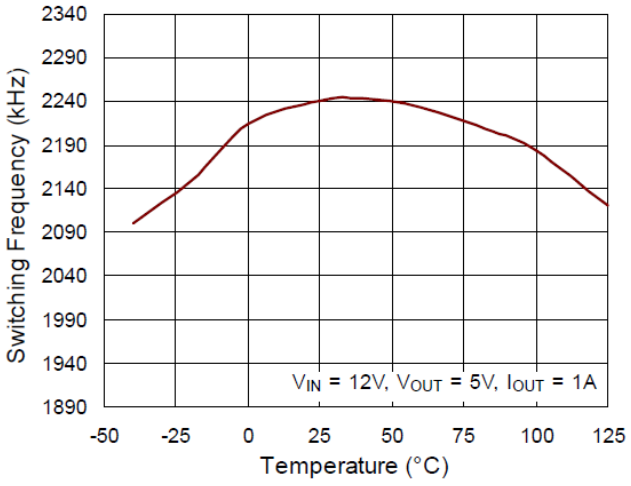
Output Voltage vs. Input Voltage



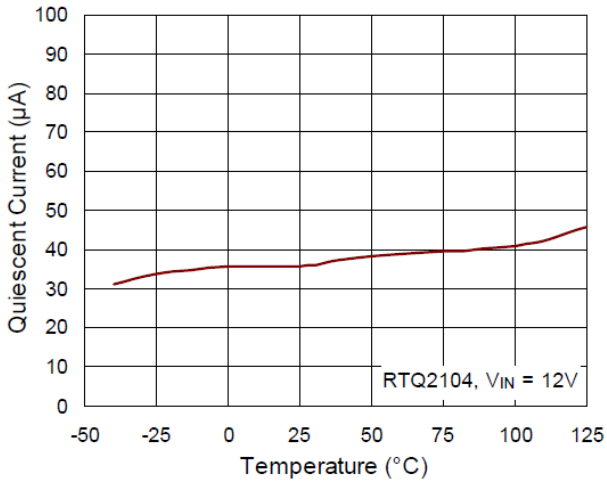
Current Limit vs. Input Voltage



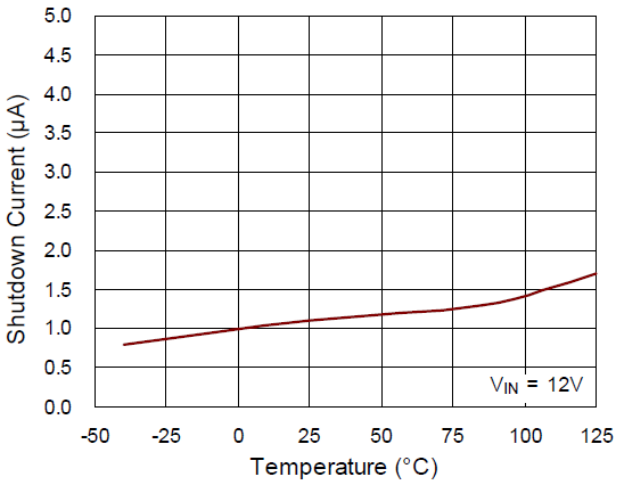
Switching Frequency vs. Temperature



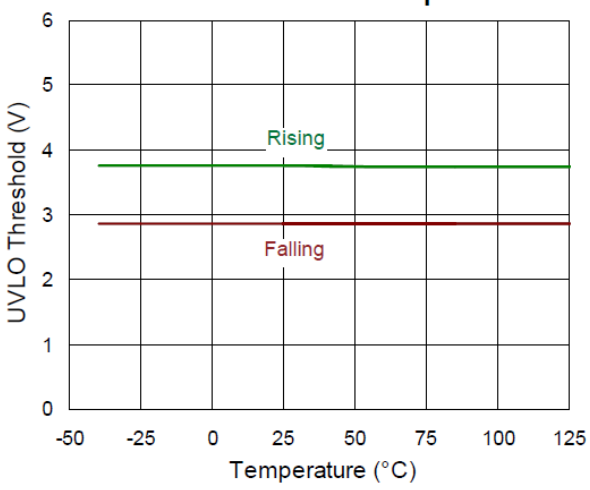
Quiescent Current vs. Temperature



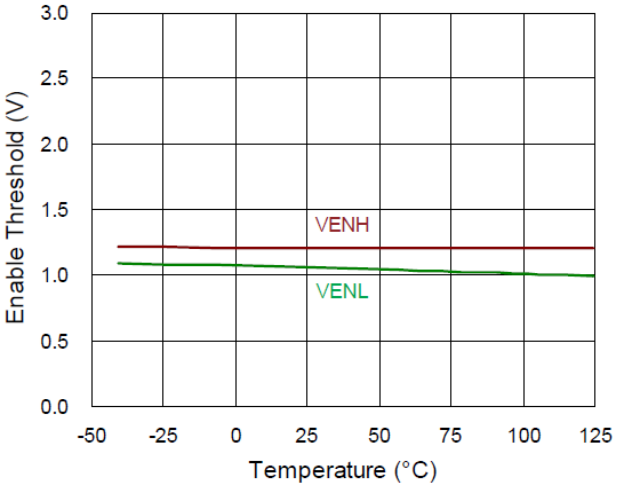
Shutdown Current vs. Temperature



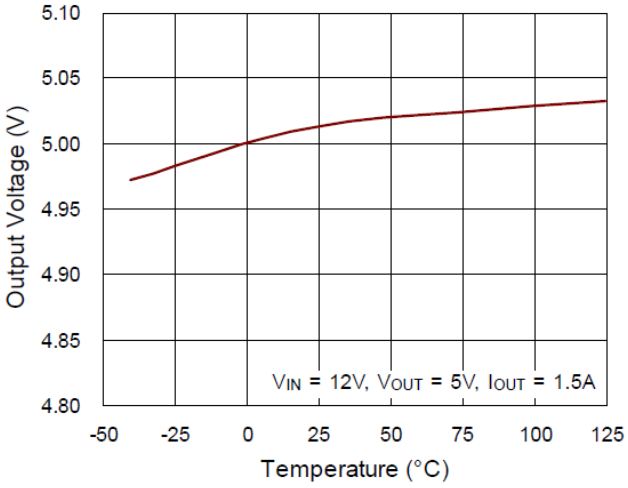
UVLO Threshold vs. Temperature



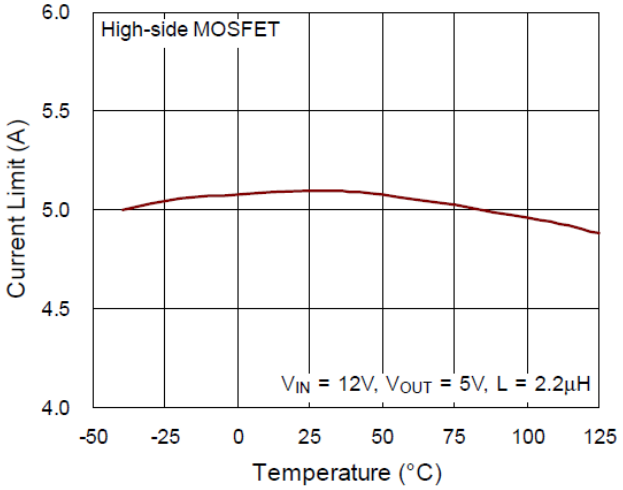
Enable Threshold vs. Temperature



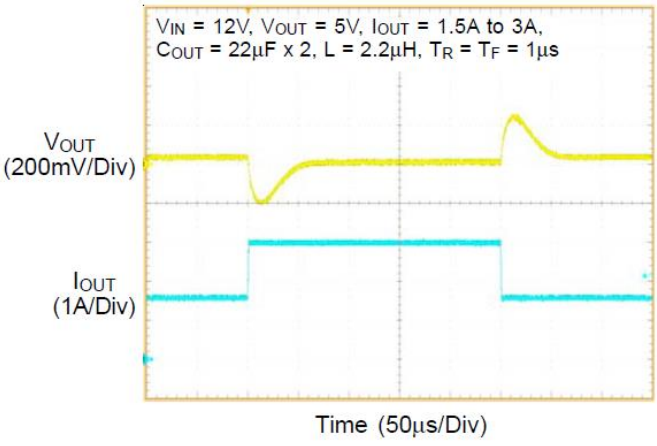
Output Voltage vs. Temperature



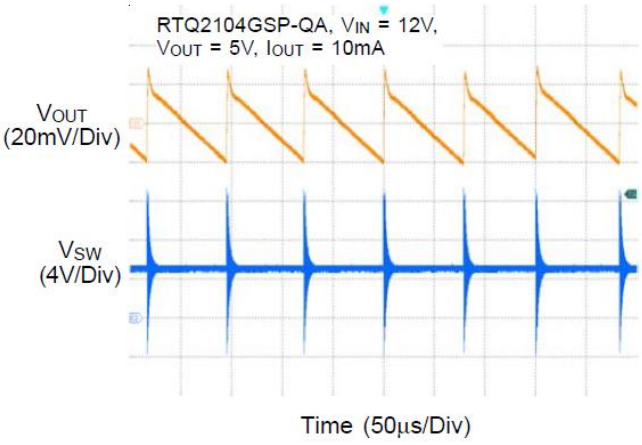
Current Limit vs. Temperature



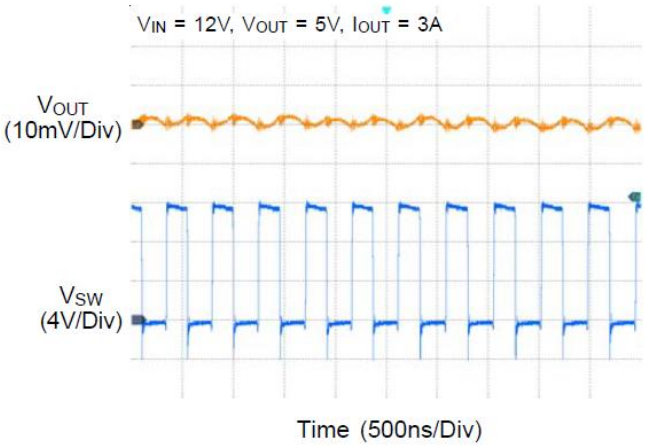
Load Transient Response



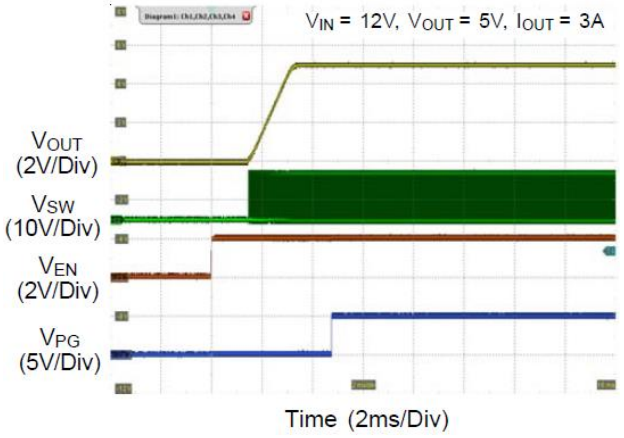
Output Ripple Voltage



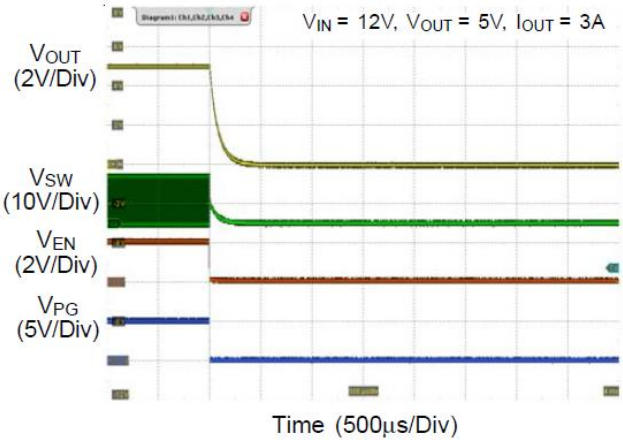
Output Ripple Voltage



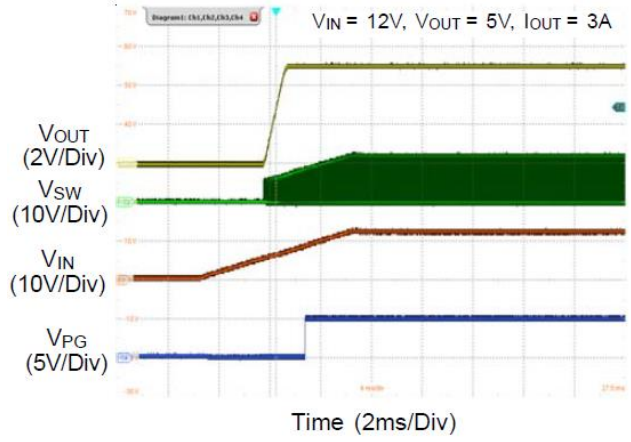
Power On from EN



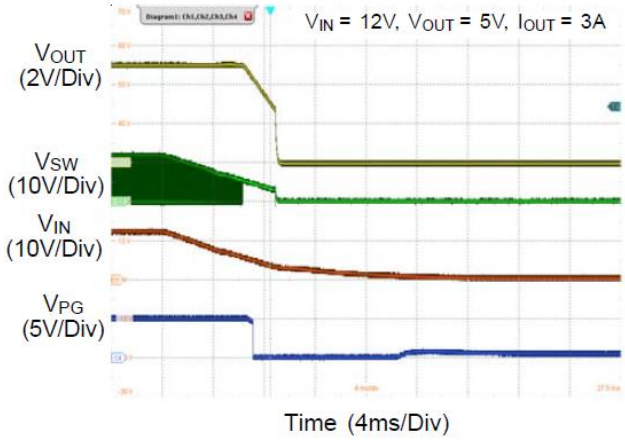
Power Off from EN



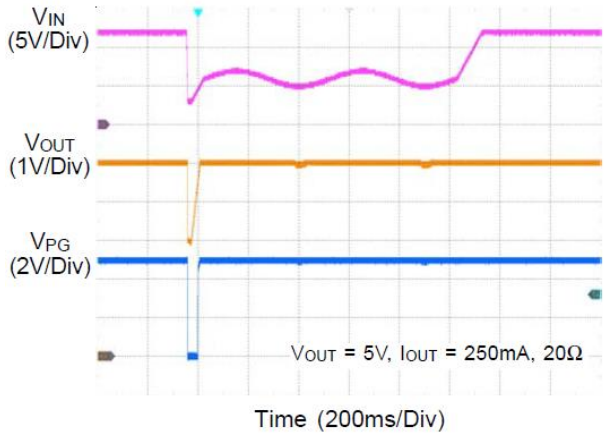
Power On from VIN



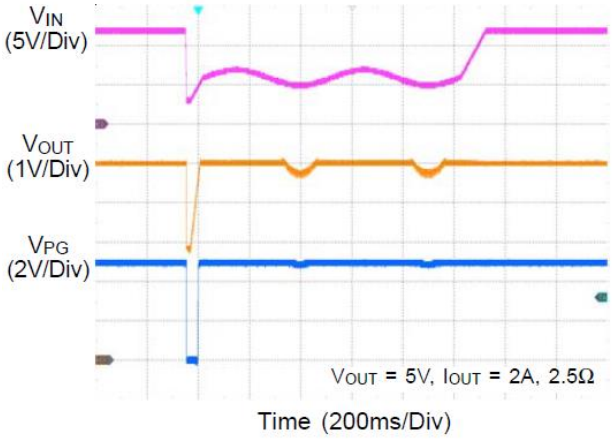
Power Off from VIN



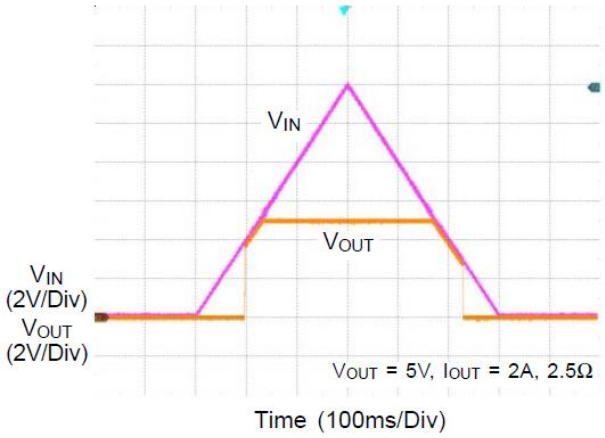
Level III of Starting Profile (ISO16750-2)



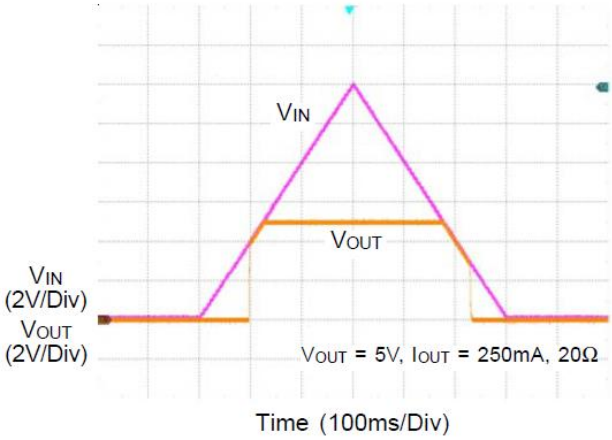
Level III of Starting Profile (ISO16750-2)



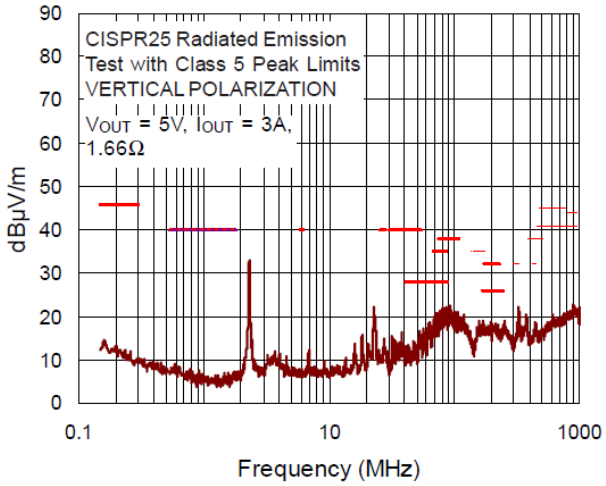
Start-Up Dropout Performance



Start-Up Dropout Performance



Radiated EMI Performance



17 Operation

17.1 Control Loop

The RTQ2104-QA is a high efficiency, buck converter that utilizes the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. The inductor current is internally monitored during each switching cycle. The output voltage is sensed on the FB pin via the resistor divider, R1 and R2, and compared with the internal reference voltage (VREF) to generate a compensation signal (VCOMP). A control signal derived from the inductor current is compared to the VCOMP, derived from the feedback voltage. When the inductor current reaches its threshold, the high-side MOSFET switch is turned off and the inductor current ramps down. While the high-side MOSFET switch is off, the inductor current is supplied through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, the duty-cycle and output voltage are controlled by regulating inductor current.

17.2 Light Load Operation

The RTQ2104GSP-QA operates in power saving mode (PSM) at light load and offers higher light load efficiency. In power saving mode (PSM) at low load current, the inductor current can drop to zero. This is detected by the internal zero-current detection circuitry, which utilizes the low-side MOSFET switch $R_{DS(ON)\_L}$ to sense the inductor current. The low-side MOSFET switch is turned off when the inductor current drops to zero, resulting in discontinuous inductor current operation (DCM). Both power MOSFETs will remain off with the output capacitor supplying the load current until the V_{FB} is lower than the PSM threshold (V_{REF} x 1.005, typical). DCM operation maintains high efficiency at light load and most of the internal circuit is shut down, and the supply current drops to quiescent current (typically, 40mA) to reduce the quiescent power consumption during non-switching period. In PSM, the IC starts to switch when V_{FB} is lower than the PSM threshold (V_{REF} x 1.005, typical) and stops switching when V_{FB} is high enough. The IC detects the peak inductor current (I_{L_PEAK}) and keeps high-side MOSFET switch on until the IL reaches its minimum peak current level (1A at V_{IN} = 12V, typical) to ensure that the IC can provide sufficiency output current with each switching pulse. If the tight voltage regulation accuracy requirement is necessary, the RTQ2104BGSP-QA is offered to operate in Forced-PWM Mode (F_{PWM}). The inductor current maintains in continuous operation (CCM) even at light load. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. Furthermore, this feature ensures that the switching frequency stays away from the AM frequency band, while operating between the minimum and maximum duty cycle limits.

17.3 Input Voltage Range

The minimum on-time, t_{ON_MIN}, is the smallest duration which the high-side MOSFET switch can be in its “on” state. Considering the minimum on-time, the allowed maximum input voltage, V_{IN_MAX}, is calculated by:

$$V_{IN\_MAX} \leq \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW}}$$

where the minimum on-time of the RTQ2104-QA is 60ns (typical); f_{SW} is the maximum operating frequency. The maximum operating frequency of the RTQ2104-QA is 2.45MHz, considering the built-in spread-spectrum frequency modulation. In contrast, the minimum off-time determines the allowed minimum operating input voltage, V_{IN_MIN}, to maintain fixed frequency operation. The minimum off-time, t_{OFF_MIN}, is the smallest amount of time that the RTQ2104-QA is capable of turning on the low-side MOSFET switch, tripping the current comparator and turning the MOSFET switch back off. The following equation shows the minimum off-time calculation that considers the loss terms,

$$V_{IN\_MIN} \geq \left[\frac{V_{OUT} + I_{OUT\_MAX} \times \left(R_{DS(ON)\_L} + DCR\right)}{1 - t_{OFF\_MIN} \times f_{SW}} \right] + I_{OUT\_MAX} \times \left(R_{DS(ON)\_H} - R_{DS(ON)\_L}\right)$$

where the minimum off-time of the RTQ2104-QA is 65ns (typical); $R_{DS(ON)\_H}$ is the on resistance of the high-side MOSFET switch; $R_{DS(ON)\_L}$ is the on resistance of the low-side MOSFET switch; DCR is the DC resistance of inductor.

17.4 Maximum Duty Cycle Operation

The RTQ2104-QA is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than the minimum off-time, the RTQ2104-QA starts to enable the skip off-time function and keeps high-side MOSFET switch on continuously. The RTQ2104-QA implements the skip off-time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

Note that achieving an actual 100% output will only be possible under no-load conditions. In practical scenarios, the ideal maximum output voltage will be equal to the input voltage minus the product of the output current and the maximum high-side MOSFET on-resistance. Additionally, when considering a low boot voltage condition, the low-side MOSFET may be turned on for a certain duration. In this case, the actual VOUT can be expressed as V_{OUT} = 0.99 x (V_{IN} – $I_{OUT(max)}$ x $R_{DSON(max)}$). Therefore, it is advisable to allocate a sufficient design margin to ensure that the target output is maintained under all possible loading current scenarios during the system's operation.

17.5 BOOT UVLO

The BOOT UVLO circuit is implemented to ensure a sufficient voltage of the BOOT capacitor for turning on the high-side MOSFET switch at any condition. The BOOT UVLO usually actives at extremely high conversion ratio or the higher VOUT application operates at very light load. For extremely high conversion ratio condition after soft-start is finished or higher VOUT application operates at very light load and PSM, the low-side MOSFET switch may not have sufficient turn-on time to charge the BOOT capacitor. The device monitors BOOT pin capacitor voltage and force to turn on the low-side MOSFET switch when the BOOT to SW voltage falls below $V_{BOOT\_UVLO\_L}$ (typical, 2.3V). Meanwhile, the minimum off-time is extended to 150ns (typical) hence prolong the BOOT capacitor charging time. The BOOT UVLO is sustained until the $V_{BOOT-SW}$ is higher than $V_{BOOT\_UVLO\_H}$ (typically, 2.4V).

17.6 Internal Regulator

The device integrates a 5V linear regulator (V_{CC}) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when V_{IN} is below 5V. The V_{CC} can be used as the PG pull-up supply but it is "NOT" allowed to power other devices or circuitry. The VCC pin must be bypassed to ground with a 1μF, X7R capacitor and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

17.7 Enable Control

The RTQ2104-QA provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{EN_F}), switching is inhibited even if the VIN voltage is above the VIN

undervoltage-lockout threshold (V_{UVLO_R}). If V_{EN} is held below 0.4V, the converter will enter shutdown mode, that is, the converter is disabled. During shutdown mode, the supply current can be reduced to I_{SHDN} (5μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{EN_R}) while the VIN voltage is higher than V_{UVLO_R}, the device will be turned on, that is, switching being enabled and the soft-start sequence being initiated. The current source of EN typically sinks 1.2μA.

17.8 Soft-Start

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RTQ2104-QA provides an internal soft-start feature for inrush currents control. During the start-up sequence, the internal soft-start capacitor is charged by an internal current source (I_{SS}) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. If the output is for some reasons pre-biased to a certain voltage during start-up, the device will not start switching until the voltage difference between internal soft-start voltage and the FB pin is larger than 400mV (i.e., $V_{SS} - V_{FB} > 400mV$, typical). And only when the internal soft-start ramp voltage is higher than the feedback voltage V_{FB}, the switching will be resumed. The output voltage can then ramp up smoothly to its targeted regulation voltage, and the converter can have a monotonic smooth start-up. The PG pin will be in high impedance and V_{PG} will be held high in the 1.6ms (typical). The typical start-up waveform shown in Figure 1 indicates the sequence and timing between the output voltage and related voltage.

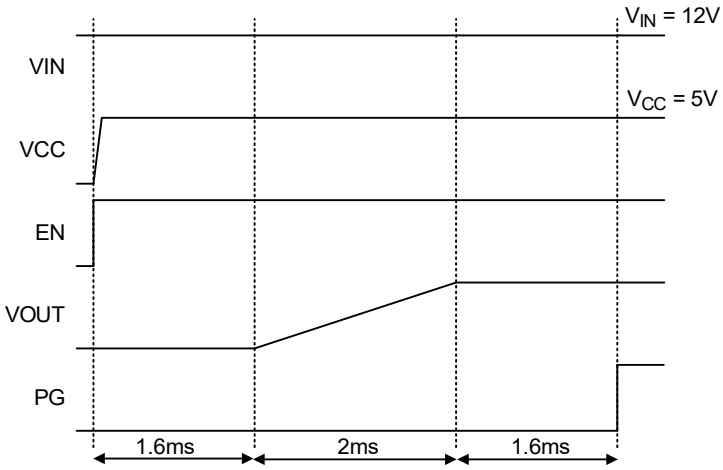


Figure 1. Start-Up Sequence

17.9 Power-Good Indication

The RTQ2104-QA features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to V_{CC} or an external voltage below 5.5V. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH1}) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high after a certain delay elapsed. When V_{FB} exceeds V_{TH_PGHL1} (typically 120% of the reference voltage), the PG pin will be pulled low, moreover, the IC turns off the high-side MOSFET switch and turns on the low-side MOSFET switch until the inductor current reaches I_{SK_L} if the MODE pin is set high. If the V_{FB} is still higher than V_{TH_PGHL1}, the high-side MOSFET switch remains prohibited and the low-side MOSFET switch will turn-on again at next cycle. If the MODE pin is set low, the IC turns off the low-side MOSFET switch once the inductor current reaches zero current unless $V_{BOOT-SW}$ is too low. For V_{FB} higher than V_{TH_PGHL1}, V_{PG} can

be pulled high again if V_{FB} drops back by a power-good high threshold (V_{TH_PGLH2}) (typically 117% of the reference voltage). When V_{FB} fall short of power-good low threshold (V_{TH_PGHL2}) (typically 85% of the reference voltage), the PG pin will be pulled low. Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device (10Ω, typically) will pull the PG pin low. The power good indication-profile is shown in Figure 2.

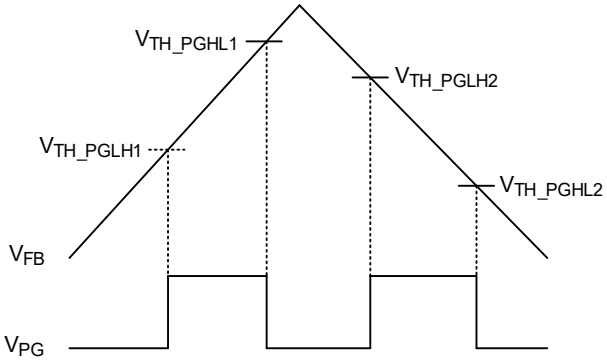


Figure 2. The Logic of PG

17.10 Spread Spectrum Operation

Due to the periodicity of the switching signals, the energy concentrates in one particular frequency and also in its harmonics. These levels or energy is radiated and therefore this is where a potential EMI issue arises. The RTQ2104-QA build-in spread spectrum frequency modulation further helping systems designers with better EMC management. The spread spectrum can be active when soft-start is finished and zero-current is not detected. The spread spectrum is implemented by a pseudo random sequence and uses +6% spread of the switching frequency, that is, the frequency will vary from 2.1MHz to 2.226MHz. Therefore, the RTQ2104-QA still guarantees that the 2.1MHz switching frequency does not drop into the AM band limit of 1.8MHz.

17.11 Input Undervoltage-Lockout

In addition to the EN pin, the RTQ2104-QA also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO_R}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the VIN voltage goes below the UVLO falling threshold voltage (V_{UVLO_F}), this switching will be inhibited; if the VIN voltage rises above the UVLO rising threshold (V_{UVLO_R}), the device will resume switching. Note that V_{IN} = 3V is only designed for cold crank requirement, normal input voltage should be larger than VUVLO_R.

17.12 High-Side Switch Peak Current-Limit Protection

The RTQ2104-QA includes a cycle-by-cycle high-side switch peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. The high-side MOSFET switch peak current limit of the RTQ2104-QA is 5A (typically). The inductor current through the high-side MOSFET switch will be measured after a certain amount of delay when the high-side MOSFET switch being turned on. If an overcurrent condition occurs, the converter will immediately turn off the high-side MOSFET switch and turn on the low-side MOSFET switch to prevent the inductor current exceeding the high-side MOSFET switch peak current limit (I_{LIM_H}).

17.13 Low-Side Switch Current-Limit Protection

The RTQ2104GSP-QA not only implements the high-side MOSFET switch peak current limit but also provides the sourcing current limit for low-side MOSFET switch. Besides, the RTQ2104BGSP-QA further provides sinking current limit for low-side MOSFET switch. With these current protections, the IC can easily control inductor current at both side MOSFET switch and avoid current runaway for short-circuit condition.

For the low-side MOSFET switch sourcing current limit, there is a specific comparator in internal circuitry to compare the low-side MOSFET switch sourcing current to the low-side MOSFET switch sourcing current limit at the end of every clock cycle. When the low-side MOSFET switch sourcing current is higher than the low-side MOSFET switch sourcing current limit which is high-side MOSFET switch current limit (I_{LIM_H}) multiplied by 0.95 (typical), the new switching cycle is not initiated until inductor current drops below the low-side MOSFET switch sourcing current limit.

For the low-side MOSFET switch sinking current-limit protection, it is implemented by detecting the voltage across the low-side MOSFET switch. If the low-side MOSFET switch sinking current exceeds the low-side MOSFET switch sinking current limit (I_{SK_L}) (typical, 2A), the converter will immediately turn off the low-side MOSFET switch and turn on the high-side MOSFET switch.

17.14 Output Undervoltage Protection

The RTQ2104-QA includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage (V_{FB}). If V_{FB} drops below the undervoltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off the high-side MOSFET switch and then turn off the low-side MOSFET switch when the inductor current drop to zero. If the output undervoltage condition continues for a period of time, the RTQ2104-QA enters output undervoltage protection with hiccup mode and discharges the internal V_{SS}. During hiccup mode, the device remains shut down. After the internal V_{SS} is discharged to less than 150mV (typically), the RT2104 attempts to re-start up again. The high-side MOSFET switch will start switching when voltage difference between internal V_{SS} and V_{FB} is larger than 400mV (i.e., $V_{SS} - V_{FB} > 400mV$, typical). If the fault condition is not removed, the high-side MOSFET switch stop switching when the voltage difference between internal V_{SS} and V_{FB} is 700mV (i.e., $V_{SS} - V_{FB} = 700mV$, typically). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. A short circuit protection and recovery profile is shown in Figure 3.

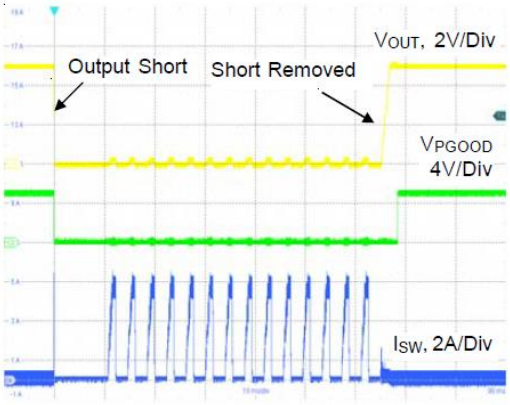


Figure 3. Short Circuit Protection and Recovery

17.15 Over-Temperature Protection

The RTQ2104-QA includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds an over-temperature protection threshold T_{OTP}. Once the junction temperature cools down by an over-temperature protection hysteresis (T_{OTP_HYS}), the IC will resume normal operation with a complete soft-start.

17.16 Pin-Short Protection

The RTQ2104-QA provides pin-short protection for neighbor pins. The internal protection fuse will be burned out to prevent IC smoke, fire, and spark when the BOOT pin is shorted to the VIN pin. The hiccup mode protection will be triggered to avoid IC burn-out when the SW pin is shorted to ground during internal high-side MOSFET turns on.

18 Application Information

(Note 7)

A general the RTQ2104-QA application circuit is shown in the Typical Application Circuit section. External component selection is largely driven by the load requirement. Next, the inductor L is chosen and then the input capacitor C_{IN}, the output capacitor C_{OUT}. Next, feedback resistors and compensation circuit are selected to set the desired output voltage and crossover frequency. Next, the internal regulator capacitor C_{VCC}, the bootstrap resistor R_{BOOT}, and the bootstrap capacitor C_{BOOT} can be selected. Finally, the remaining optional external components can be selected for functions such as the EN and PG.

18.1 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). A good compromise between size and loss is a 30% peak-to-peak ripple current to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. This result in additional phase lag in the loop and reduce the crossover frequency. As the ratio of the slope-compensation ramp to the sensed-current ramp increases, the current-mode system tilts towards voltage-mode control. Lower inductance values allow for smaller case size, but the increased ripple lowers the effective current-limit threshold, increases the AC losses in the inductor and may trigger low-side switch sinking current limit at FPWM. It also causes insufficient slope compensation and ultimately loop instability as duty cycle approaches or exceeds 50%. A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) with about 10% to 50% of the maximum rated output current (3A).

To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load-current value at which DCM/CCM switchover occurs. The inductor selected should have a saturation current rating greater than the peak current limit of the device. The core must be large enough not to saturate at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the high-side switch peak current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the high-side switch peak current limit rather than the peak inductor current. It is recommended to use shielded inductors for good EMI performance.

18.2 Input Capacitor Selection

The input capacitor, C_{IN}, is needed to filter the pulsating current at the drain of the high-side MOSFET switch. C_{IN} should be sized to do this without causing a large variation in the input voltage. The peak-to-peak voltage ripple on the input capacitor can be estimated using the following equation:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + ESR \times I_{OUT}$$

Where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

Figure 4 shows the C_{IN} ripple current flowing through the input capacitors and the resulting voltage ripple across the capacitors. For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple caused by ESR can be ignored, and the minimum value of effective input capacitance can be estimated using the following equation:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where $\Delta V_{CIN\_MAX} \leq 200mV$

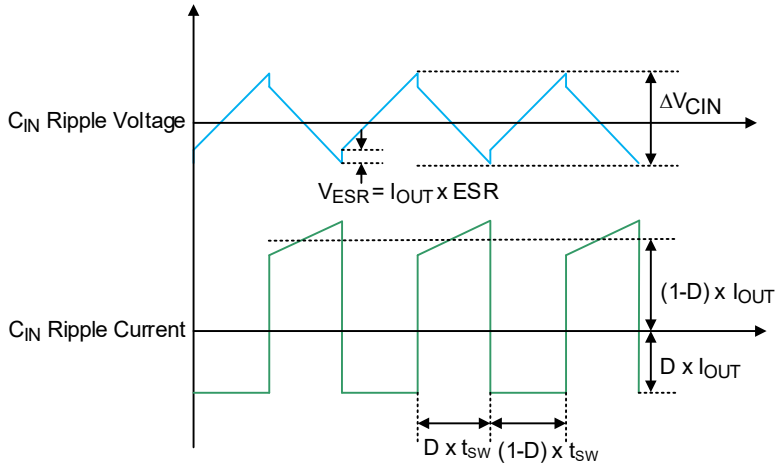


Figure 4. CIN Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current. The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) using the following equation:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at the maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. The maximum ripple voltage usually occurs at 50% duty cycle, that is, V_{IN} = 2 x V_{OUT}. It is commonly to use the worse $I_{RMS} \cong 0.5 \times I_{OUT\_MAX}$ at V_{IN} = 2 x V_{OUT} for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size, height, and thermal

requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Ceramic capacitors are ideal for switching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RTQ2104-QA circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing. The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the GND of the IC. It is recommended to connect a 4.7μF, X7R capacitor between the VIN pin to the GND pin. For filtering high frequency noise, additional small capacitor 0.1μF should be placed close to the part and the capacitor should be 0402 or 0603 in size. X7R capacitors are recommended for best performance across temperature and input voltage variations.

18.3 Output Capacitor Selection

The selection of C_{OUT} is determined by considering to satisfy the voltage ripple and the transient loads. The peak-to- peak output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right)$$

Where the ΔI_L is the peak-to-peak inductor ripple current. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Regarding to the transient loads, the VSAG and VSOAR requirement should be taken into consideration for choosing the effective output capacitance value. The amount of output sag/soar is a function of the crossover frequency factor at PWM, which can be calculated as shown below.

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. The recommended dielectric type of the capacitor is X7R best performance across temperature and input voltage variations. The variation of the capacitance value with temperature, DC bias voltage, and switching frequency needs to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Transient performance can be improved with a higher value of output capacitor. Increasing the output capacitance will also decrease the output voltage ripple. In some applications, for example those with large amounts of output capacitance, the output voltage will probably not be regulated to its setting since C_{OUT} does not be fully charged when soft-start period is end. In this case, the device detects UVP and enters hiccup operation. Determine the output capacitance appropriately to ensure the C_{OUT} is fully charged before the soft-start period is finished.

18.4 Output Voltage Programming

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 5. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where the reference voltage, V_{REF}, is 0.8V (typical).

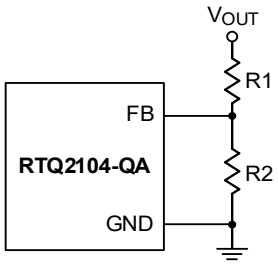


Figure 5. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is not larger than 170kΩ for noise immunity consideration. The resistance of R1 can then be obtained as below:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

18.5 Feed-Forward Capacitor Design

The purpose of loop compensation is to ensure stable operation while maximizing the dynamic performance. An undercompensated system may result in unstable operations. Typical symptoms of an unstable power supply include: audible noise from the magnetic components or ceramic capacitors, jittering in the switching waveforms, oscillation of output voltage, overheating of power MOSFETs and so on.

The RTQ2104-QA integrates simple internal compensation and the performance of a current mode synchronous buck converter can be optimized by adding one feed-forward capacitor (C_{FF}) to boost the crossover frequency (f_C) and phase margin while it can improve output voltage ripple at PSM and transient response, as shown in Figure 6. The C_{FF} and resistive divider of output voltage generates one more zero, and forms one pole in the system, which can optimize either higher bandwidth or greater phase margin to meet specific performance requirements. In general, larger values of C_{FF} provide greater bandwidth improvements. However, if C_{FF} is too large, it causes the high crossover frequency (f_C) but the phase margin is insufficient, resulting in unacceptable phase margin or instability. The method presented here is easy to calculate and design. It is always necessary to make a measurement before releasing the design for final production to take full account of circuit parasitic and component nonlinearity, such as the ESR variations of output capacitors, the nonlinearity of inductors and capacitors, etc. Also, circuit PCB noise and limited measurement accuracy may also cause measurement errors. A Bode plot is ideally measured with a network analyzer while Richtek application note AN038 provides an alternative way to check the stability quickly and easily. Generally, follow the following steps to calculate the compensation components:

1. Check the crossover frequency without feed-forward capacitor (C_{FF}), $f_{C\_ORIGINAL}$. The $f_{C\_ORIGINAL}$ can be measured by using a network analyzer. For stability purposes, our target is to have a loop gain slope that is −20dB/decade from a very low frequency to beyond the crossover frequency. Do “NOT” design the crossover

frequency over 80kHz with the RTQ2104-QA. For dynamic purposes, the higher the bandwidth, the faster load transient response. The downside to high bandwidth is that it increases the regulators susceptibility to board noise which ultimately leads to excessive falling edge jitter of the switch node voltage.

2. Feedforward capacitor (C_{FF}) selection. The feedforward capacitor (C_{FF}) can be determined by calculating the geometric mean of the zero and pole frequencies to boost the crossover frequency (f_C) and phase margin. Setting the geometric mean frequency equal to the converter crossover frequency without C_{FF} to boost the maximum phase.

$$f_{mean} = f_{C\_ORIGINAL} = \sqrt{f_Z \times f_P}$$

where

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}}$$

$$f_P = \frac{1}{2\pi \times \left(\frac{R1 \times R2}{R1 + R2}\right) \times C_{FF}}$$

The C_{FF} can be determined by following equation:

$$C_{FF} = \frac{1}{2\pi \times f_{C\_ORIGINAL}} \times \sqrt{\frac{R1 + R2}{R1 \times (R1 \times R2)}}$$

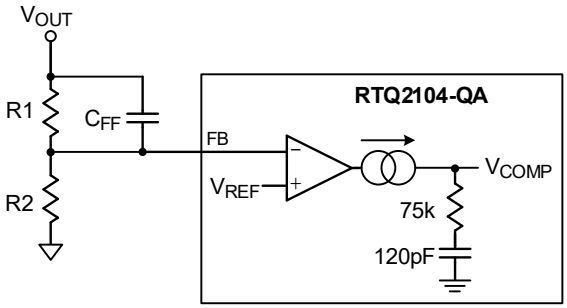


Figure 6. Compensation Network with Feedforward Capacitor

18.6 Internal Regulator

The device integrates a 5V linear regulator (VCC) that is supplied by VIN and provides power to the internal circuitry. The internal regulator operates in low dropout mode when the VIN voltage is below 5V. The VCC can be used as the PG pull-up supply but it is "NOT" allowed to power other devices or circuitry. The VCC pin must be bypassed to ground with a 1μF X7R capacitor and it needs to be placed as close as possible to the VCC pin. Be careful to account for the voltage coefficient of ceramic capacitors when choosing the value and case size. Many ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

18.7 Bootstrap Driver Supply

The bootstrap capacitor (C_{BOOT}) and bootstrap resistor (R_{BOOT}) between the BOOT pin and the SW pin are used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the bootstrap capacitor is charged through an internal diode to a voltage equal to approximately V_{VCC} each time the low-side switch is turned on. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. For most applications, a 0.1μF, 0603 ceramic capacitor with X7R is recommended and the capacitor should have a 6.3V or

higher voltage rating. The R_{BOOT} must be 10 ohms and it can be 0402 or 0603 in size, the recommended application circuit is shown in Figure 7.

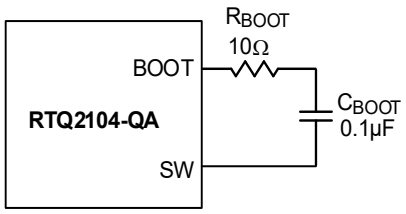


Figure 7. Bootstrap Driver Supply

18.8 External Bootstrap Diode (Optional)

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve the enhancement of the high-side switch and improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 with AEC-Q101 standard qualified. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RTQ2104-QA. Note that the $V_{BOOT-SW}$ must be lower than 5.5V. The recommended application circuit is shown in Figure 8, which includes an external bootstrap diode for charging the bootstrap capacitor, and a bootstrap resistor R_{BOOT} placed between the BOOT pin and the capacitor/diode connection. Figure 9 shows an efficiency comparison with and without Bootstrap Diode.

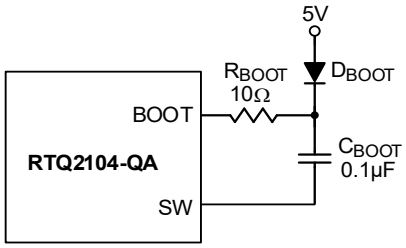


Figure 8. External Bootstrap Diode and Resistor at the BOOT Pin

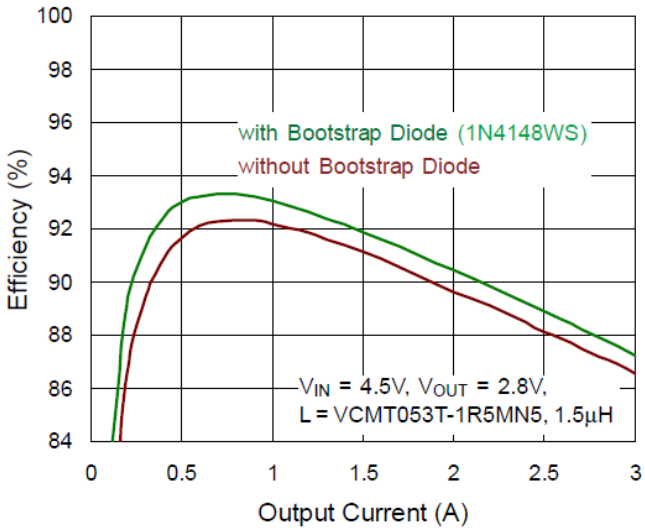


Figure 9. Efficiency Comparison with and without Bootstrap Diode

18.9 EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply VIN directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 11, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins (typically 1.25V). An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 12. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when VIN is smaller than the VOUT target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage-lockout threshold, as shown in Figure 13.

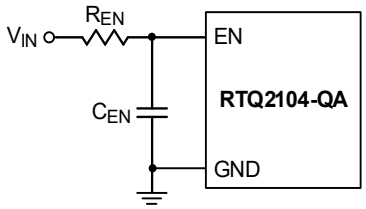


Figure 10. Enable Timing Control

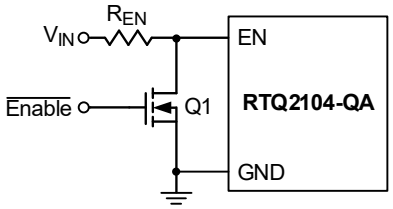


Figure 11. Logic Control for the EN Pin

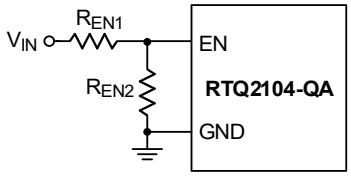


Figure 12. Resistive Divider for Undervoltage-Lockout Threshold Setting

18.10 Power-Good Output

The PG pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor. The external voltage source can be an external voltage supply below 5.5V, VCC or the output of the RTQ2104-QA if the output voltage is regulated under 5.5V. It is recommended to connect a 100kΩ between external voltage source to the PG pin.

18.11 Thermal Consideration

In many applications, the RTQ2104-QA does not generate much heat due to its high efficiency and low thermal resistance of its SOP-8 (Exposed Pad) package. However, in applications in which the RTQ2104-QA is running at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed

the maximum junction temperature of the part. The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, as listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 175°C, the RTQ2104-QA will stop switching the power MOSFETs until the temperature drops by 15°C.

The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum allowed junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient operating temperature, θ_{JA} is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system. The device thermal resistance depends strongly on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance. Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the $\theta_{JA(EVB)}$ is reasonable to obtain the allowed $P_{D(MAX)}$. As an example, consider the case when the RTQ2104-QA is used in applications where V_{IN} = 12V, I_{OUT} = 3A, V_{OUT} = 5V. The efficiency at 5V, 3A is 90% by using Cyntec- VCMT063T-2R2MN5 (2.2µH, 15mΩ DCR) as the inductor and measured at room temperature. The core loss can be obtained from its website of 37.1mW in this case. In this case, the power dissipation of the RTQ2104-QA is

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.495W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 28.68°C/W, using the RTQ2104-QA evaluation board with 4 layers with 2 oz. copper thickness on the outer layers and 1 oz. copper thickness on the inner layers copper thickness, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

T_J = 1.495W x 28.68°C /W + 25°C = 67.88°C

Figure 13 shows the RTQ2104-QA $R_{DS(ON)}$ versus different junction temperature. If the application calls for a higher ambient temperature, we might recalculate the device power dissipation and the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Using 65°C ambient temperature as an example, the change of the equivalent $R_{DS(ON)}$ can be obtained from Figure 13 and yields a new power dissipation of 1.7W.

Therefore, the estimated new junction temperature is

T_J' = 1.7W x 28.68°C/W + 65°C = 113.76°C

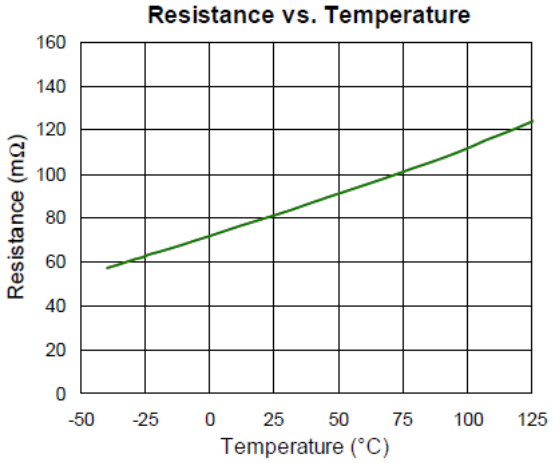


Figure 13. RTQ2104-QA $R_{DS(ON)}$ vs. Temperature

If the application calls for a higher ambient temperature and may exceed the recommended maximum junction temperature of 150°C, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary failsafe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18.12 Layout Guideline

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the RTQ2104-QA:

- Four-layer or six-layer PCB with maximum ground plane is strongly recommended for good thermal performance.
- Keep the traces of the main current paths wide and short.
- Place high frequency decoupling capacitor C_{IN2} as close as possible to the IC to reduce the loop impedance and minimize switch node ringing.
- Place the VCC decoupling capacitor, C_{VCC}, as close to the VCC pin as possible.
- Place bootstrap capacitor, C_{BST}, as close to IC as possible. Routing the trace with width of 20mil or wider.
- Place multiple vias under the device near VIN and GND and near input capacitors to reduce parasitic inductance and improve thermal performance. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the RTQ2104-QA to additional ground planes within the circuit board and on the bottom side.
- The high frequency switching nodes, SW and BOOT, should be as small as possible. Keep analog components away from the SW and BOOT nodes.
- Reducing the area size of the SW exposed copper to reduce the electrically coupling from this voltage.
- Connect the feedback sense network behind via of the output capacitor.
- Place the feedback components R_{FB1}/R_{FB2}/C_{FF} near the IC.

Figure 14 is the layout example which uses 70mm x 100mm, four-layer PCB with 2 oz. Cu on the outer layers and 1 oz. Cu on the inner layers.

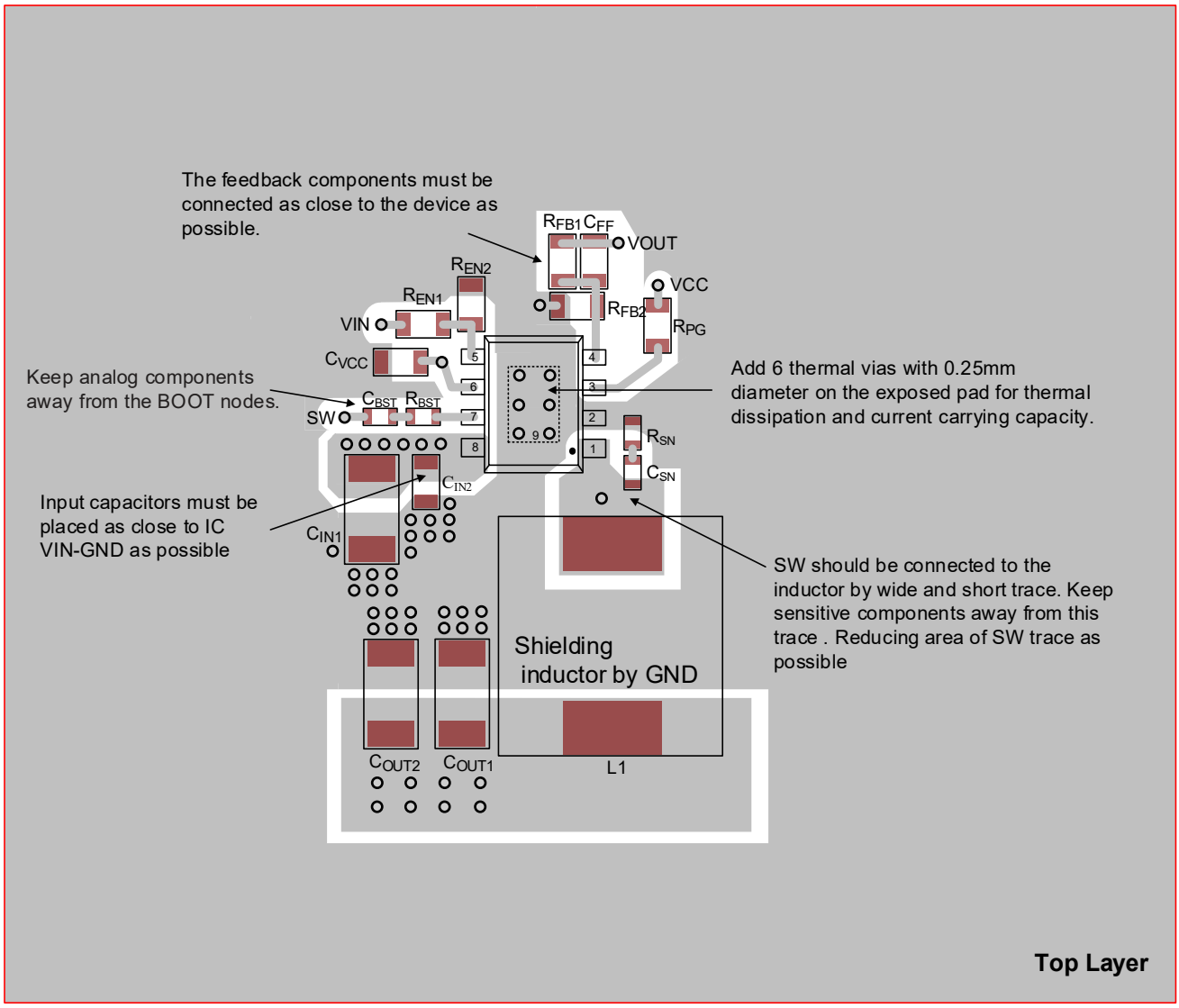
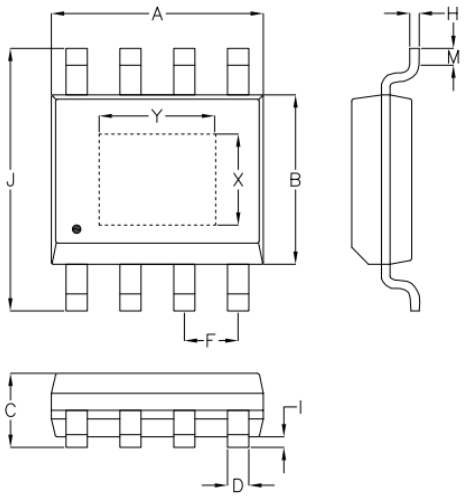


Figure 14. Layout Guide (Top Layer)

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Outline Dimension

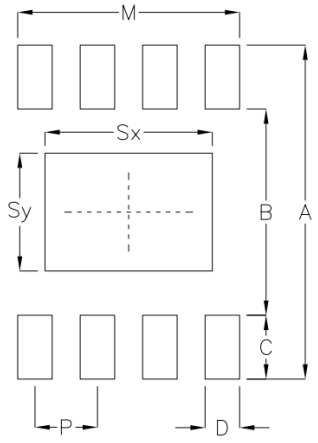


Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 8. The package of the RTQ2104-QA uses Option 2.

20 Footprint Information

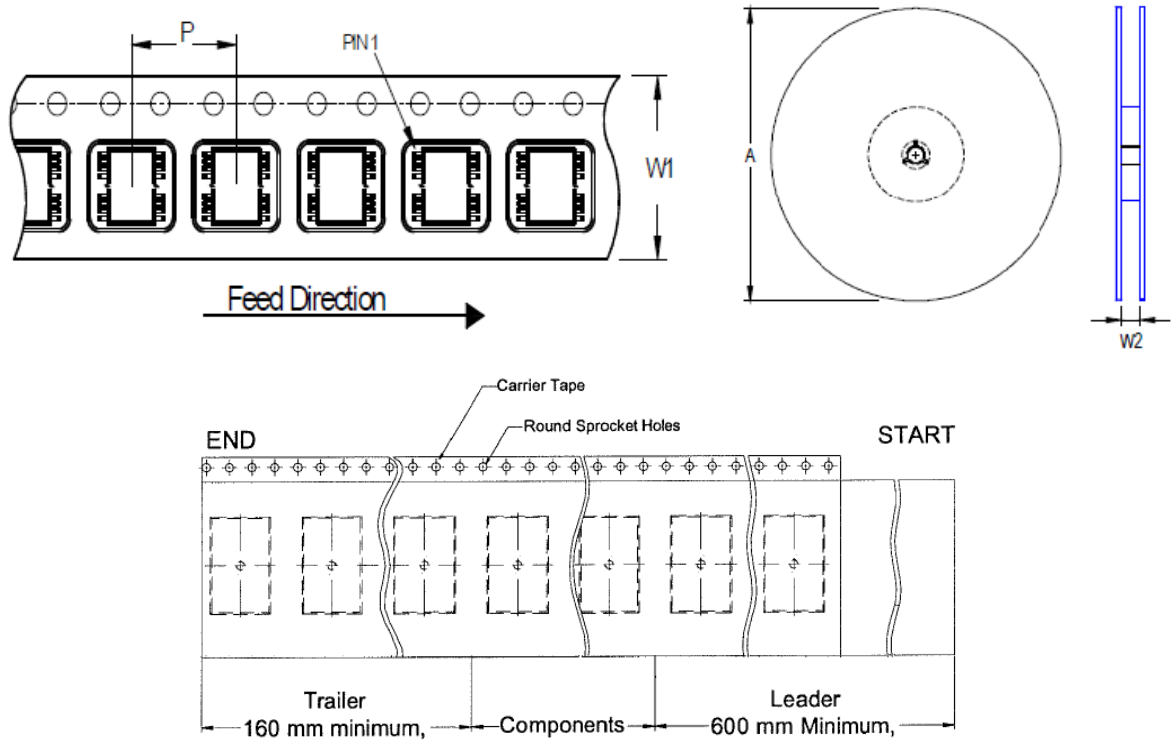


Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

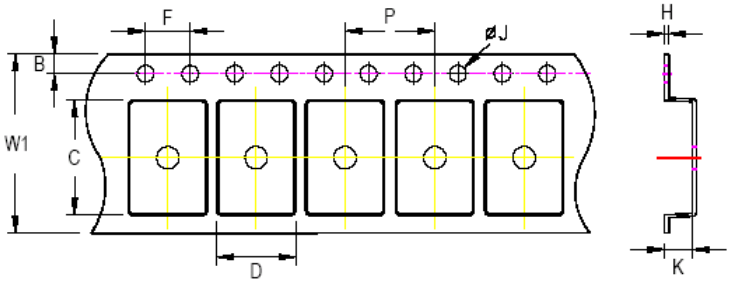
Note 9. The package of the RTQ2104-QA uses Option 2.

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description
03	2025/5/13	General Description Features Ordering Information ESD Ratings Recommended Operating Conditions Thermal Information Electrical Characteristics Operation Application Information Packing Information - Added packing information