RICHTEK®

RTQ2082-QT

Automotive CIS/CCM PMIC for Ultra Compact Camera and High Image Quality System

1 General Description

The RTQ2082-QT is a highly integrated PMIC designed for automotive camera applications. It includes three step-down converters and one high PSRR low-dropout (LDO) regulator. The high-voltage step-down converter operates with an input voltage range of up to 18.5V, suitable for Power Over Coax (POC) connections. Two low-voltage step-down converters provide a constant output voltage. All step-down converters operate in a forced fixed-frequency PWM mode. The LDO output voltage can be easily set via an external resistor. For added flexibility, the RTQ2082-QT supports 10 power sequences, configurable through a resistor. The IC is available in a WETD-VQFN-16L 3x3 package with dimple lead type wettable flanks.

The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 125°C.

2 Applications

- Automotive Camera Modules
  - Surround View Cameras
  - Front View Cameras
  - Rear View Cameras
  - Dash Cam DVR
  - Driver Monitoring Systems
  - Cabin Monitors
  - E-mirrors

3 Features

- **AEC-Q100 Grade 1 Qualified**
- **FMEA Compliant Pin Placement and Protection Mechanisms**
- **Three Step-Down Converters (HVBuck1, LVBuck2, and LVBuck3)**
  - **Peak Current Mode PWM Operation**
  - **Fixed Switching Frequency at 2.1MHz**
  - **EMI Reduction Features including Spread Spectrum and Phase-Shift Operation**
  - **HVBuck1 Supports Input Voltage from 4V to 18.5V, Adjustable Output Voltage, and up to 1.5A Output Current**
  - **LVBuck2 Supports Input Voltage from 2.7V to 5V, Fixed Output Voltage and 1.5A Output Current**
  - **LVBuck3 Supports Input Voltage from 2.7V to 5V, Fixed Output Voltage and 750mA Output Current**
  - **Pins Related to LVBuck2/LVBuck3 Can Float if the Channel is Unused**
- **Low Dropout Regulator (LDO)**
  - **Input Voltage from 2.7V to 5V and 300mA Output Current**
  - **10 Adjustable Output Voltage Settings via the RSET Pin**
  - **High PSRR: 60dB at 100kHz, 40dB at 1MHz**
- **10 Flexible Power Sequence Settings via the SEQ Pin**
- **Small Form Factor WETD-VQFN-16L 3x3 Wettable Flanks Package**
- **Ambient Temperature Range: –40°C to 125°C**
- **Junction Temperature Range: –40°C to 150°C**

4 Ordering Information

RTQ2082□□□-QT-□□□

- **Packing**
- **LVBuck3 Output Voltage**
  None: Default 1.8V
  □□□: Special Request(1)
- **LVBuck2 Output Voltage**
  11: 1.1V (Default)
  Special Request(2)
- **Grade**
  QT: AEC-Q100 Qualified
- **Package Type**(3)
  TN: WETD-VQFN-16L 3x3 (V-Type)
- **UVLO_H**
  A: 3.8V
- **Output Function**
  B: PG

Note 1.

- Marked with (1) indicated: Special Request: For example, 095 means 0.95V.
- Marked with (2) indicated: Special Request: Available voltage between 0.6V to 2.1V with 100mV steps under specific business agreement.
- Richtek products are Richtek Green Policy compliant and marked with (3) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit

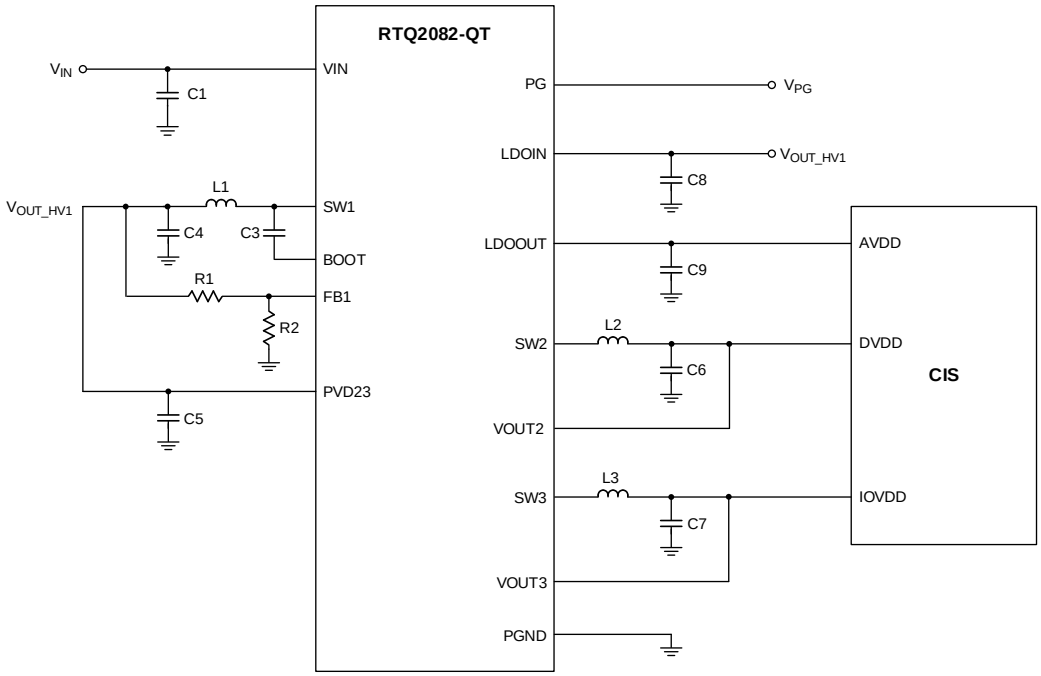
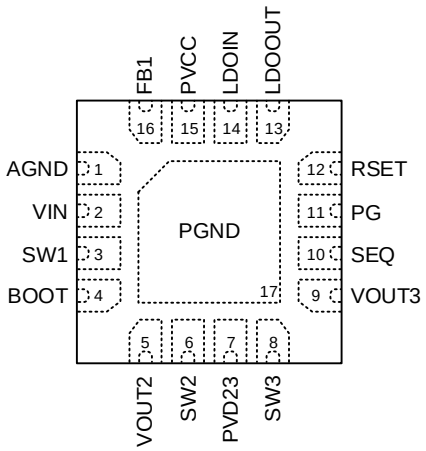


Table of Contents

7 Pin Configuration

(TOP VIEW)



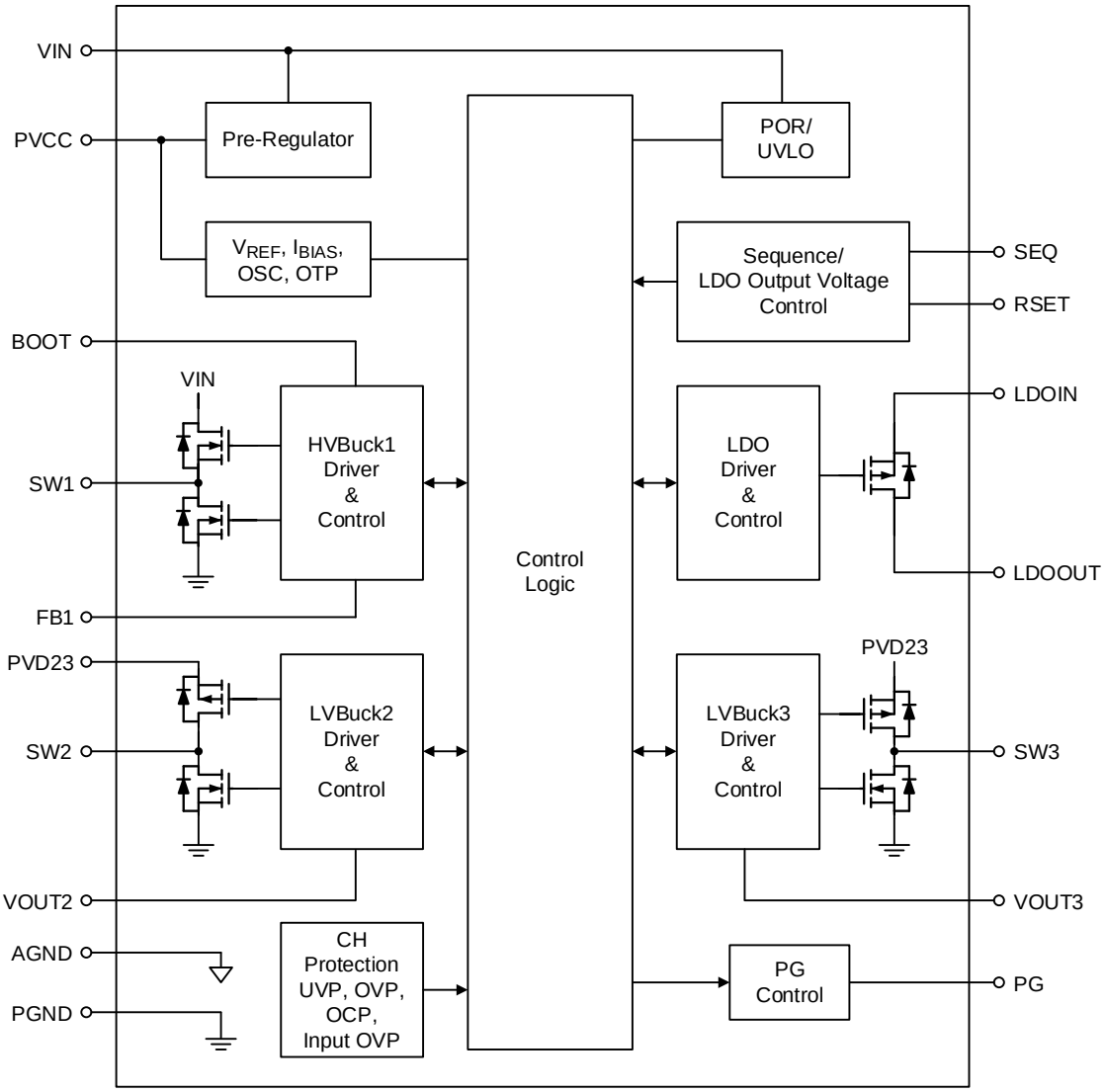
WETD-VQFN-16L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	AGND	Analog ground.
2	VIN	Supply voltage input of HVBuck1. Connect a 4.7μF or larger decouple ceramic capacitor between this pin and ground.
3	SW1	HVBuck1 switch node.
4	BOOT	Bootstrap capacitor connection pin for HVBuck1. Connect a 0.1μF ceramic capacitor between this pin and SW1.
5	VOUT2	Output voltage feedback input of LVBuck2. Directly connect the output capacitor node to this pin for better regulation.
6	SW2	LVBuck2 switch node.
7	PVD23	Supply voltage input of LVBuck2 and LVBuck3. Connect a 4.7μF or larger decouple ceramic capacitor between this pin and ground.
8	SW3	LVBuck3 switch node.
9	VOUT3	Output voltage feedback input of LVBuck3. Directly connect the output capacitor node to this pin for better regulation.
10	SEQ	Power sequence selection.
11	PG	Power status indication pin with open drain structure for HVBuck1, LVBuck2, LVBuck3 and LDO. PG at high state indicates all outputs work well.
12	RSET	LDO output voltage selection.
13	LDOOUT	LDO output. Connect a 2.2μF ceramic decouple capacitor between this pin and ground.
14	LDOIN	Supply voltage input of LDO. Connect a 2.2μF or larger decouple ceramic capacitor between this pin and ground.
15	PVCC	Internal analog power output. Connect a 1μF ceramic decouple capacitor between this pin and ground. Note additional external loading on this pin is forbidden.
16	FB1	Output voltage feedback input of HVBuck1.

Pin No.	Pin Name	Pin Function
17 (Exposed Pad)	PGND	IC thermal pad and power ground. It must connect to main ground plane for proper operation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN ---------- –0.3V to 24V
- SW1 ---------- –0.3V to 24V
- BOOT ---------- –0.3V to 28V
- BOOT to SW1 ---------- –0.3V to 5V
- VOUT2, PVD23, VOUT3, SEQ, PG,
  RSET, LDOOUT, LDOIN, PVCC, FB1 ---------- –0.3V to 6.5V
- SW2, SW3 ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WETD-VQFN-16L 3x3 ---------- 4.16W
- Package Thermal Resistance (Note 3)
  WETD-VQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WETD-VQFN-16L 3x3, θ_{JC} ---------- 4.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Voltage, V_{IN} ---------- 4V to 18.5V
- Supply Voltage, V_{PVD23}, V_{LDOIN} ---------- 2.7V to 5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Undervoltage Lockout Threshold	UVLO_H	V_{IN} rising	3.6	3.8	4	V
	UVLO_L	V_{IN} falling	3.15	3.3	3.45	
Input Overvoltage Protection	V_{IN_OV}		18.6	20	21.5	V
CH1 HVBuck1						
Input Voltage Range	V_{IN}		4	--	18.5	V
Output Voltage Range	V_{OUT_HV1}	Buck mode operation. Switching frequency, minimum on-time and minimum off-time need to be considered.	2.7	--	5	V
Output Feedback Voltage Accuracy	V_{FB1}		0.788	0.8	0.812	V
Switching Frequency	f_{SW_HV1}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	SS_{HV1}		--	6	--	%
Switching Minimum On-Time	$t_{ON\_MIN\_HV1}$		--	--	55	ns
Switching Minimum Off-Time	$t_{OFF\_MIN\_HV1}$		--	--	50	ns
High-Side MOSFET On-Resistance	$R_{ON\_HS\_HV1}$	From VIN pin to SW1 pin	115	210	340	mΩ
Low-Side MOSFET On-Resistance	$R_{ON\_LS\_HV1}$	From SW1 pin to PGND pin	40	110	200	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_HV1}$		2.4	3	3.6	A
Inductor Valley Current Limit	$I_{CL\_VL\_HV1}$		--	2.7	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_HV1}$		1	2.5	4	A
Output Discharge Resistor	R_{DIS_HV1}		220	270	360	Ω
Output Undervoltage Falling Threshold	UVP_{F_HV1}		40	50	60	%
Output Feedback Overvoltage Rising Threshold	OVP_{R_HV1}		--	110	--	%
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT_LV2}		--	1.1	--	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV2}$		–1.5	--	1.5	%
Switching Frequency	f_{SW_LV2}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{\_LV2}$		--	6	--	%
Switching Minimum On-Time	$t_{ON\_MIN\_LV2}$		--	--	44	ns
High-Side MOSFET On-Resistance	$R_{ON\_HS\_LV2}$	From PVD23 pin to SW2 pin	110	150	215	mΩ
Low-Side MOSFET On-Resistance	$R_{ON\_LS\_LV2}$	From SW2 pin to PGND pin	60	90	145	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_LV2}$		1.8	2.2	2.6	A
Inductor Valley Current Limit	$I_{CL\_VL\_LV2}$		--	1.8	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV2}$		0.7	1.7	2.9	A
Output Discharge Resistor	R_{DIS_LV2}		6	9	14	Ω
Output Undervoltage Falling Threshold	$UVP_{\_F\_LV2}$		40	50	60	%
Output Overvoltage Rising Threshold	$OVP_{\_R\_LV2}$		--	120	--	%
Output Overvoltage Falling Threshold	$OVP_{\_F\_LV2}$		--	110	--	%
Input Overvoltage Rising Threshold	$OVP_{\_IN\_R\_LV2}$		5.35	5.8	6.25	V
Input Overvoltage Hysteresis	$OVP_{\_IN\_HYS\_LV2}$	V_{IN_PVD23} falling	--	580	--	mV
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V
Output Voltage	V_{OUT_LV3}		--	1.8	--	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV3}$		–1.5	--	1.5	%
Switching Frequency	f_{SW_LV3}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{\_LV3}$		--	6	--	%
Switching Minimum On-Time	$t_{ON\_MIN\_LV3}$		--	--	44	ns
High-Side MOSFET On-Resistance	$R_{ON\_HS\_LV3}$	From PVD23 pin to SW3 pin	240	310	440	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-Side MOSFET On-Resistance	$R_{ON\_LS\_LV3}$	From SW3 pin to PGND pin	170	230	360	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_LV3}$		0.96	1.2	1.44	A
Inductor Valley Current Limit	$I_{CL\_VL\_LV3}$		--	1.08	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV3}$		0.7	1.7	2.9	A
Output Discharge Resistor	R_{DIS_LV3}		7	10	15	Ω
Output Undervoltage Falling Threshold	$UVP_{\_F\_LV3}$		40	50	60	%
Output Overvoltage Rising Threshold	$OVP_{\_R\_LV3}$		--	120	--	%
Output Overvoltage Falling Threshold	$OVP_{\_F\_LV3}$		--	110	--	%
Input Overvoltage Rising Threshold	$OVP_{\_IN\_R\_LV3}$		5.35	5.8	6.25	V
Input Overvoltage Hysteresis	$OVP_{\_IN\_HYS\_LV3}$	V_{IN_PVD23} falling	--	580	--	mV
CH4 LDO (V_{IN_LDO} = 3.6V)						
Input Voltage Range	V_{IN_LDO}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO}	V_{OUT_LDO} setting via RSET	1.8	--	3.5	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LDO}$	V_{IN_LDO} - V_{OUT_LDO} > 0.3V, I_{OUT_LDO} = 0mA to 300mA	–1.5	--	1.5	%
Maximum Output Current	$I_{OUT\_MAX\_LDO}$		300	--	--	mA
Dropout Voltage	$V_{DROP\_300\_LDO}$	I_{OUT_LDO} = 300mA (Note 6)	--	--	300	mV
	$V_{DROP\_150\_LDO}$	I_{OUT_LDO} = 150mA (Note 6)	--	--	150	
Output Current Limit	I_{CL_LDO}	(Note 7)	345	450	555	mA
Output Discharge Resistor	R_{DIS_LDO}		48	76	104	Ω
Output Undervoltage Falling Threshold	$UVP_{\_F\_LDO}$		30	40	50	%
Output Overvoltage Rising Threshold	$OVP_{\_R\_LDO}$		--	125	--	%
Output Overvoltage Falling Threshold	$OVP_{\_F\_LDO}$		--	110	--	%
Input Overvoltage Rising Threshold	$OVP_{\_IN\_R\_LDO}$		5.35	5.8	6.25	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Overvoltage Hysteresis	$V_{OVP\_IN\_HYS\_LDO}$	V_{IN_LDO} falling	--	500	--	mV
PVCC (Note 8)						
Internal Regulator Output Voltage	V_{OUT_PVCC}		4.33	4.58	4.83	V
Overcurrent Limit	I_{CL_PVCC}		150	--	300	mA
Power-Good						
Pull-Down Voltage	$V_{OUT\_L\_PG}$	Current into the PG pin is equal to 5mA	--	--	200	mV
Input Leakage Current	I_{LEAK_PG}	1.8V is applied to the PG pin	--	--	1	μA
Timing						
Soft-Start Time	t_{SS_HV1}	Time from V_{OUT_HV1} 0% rise to 90% of target value, no load	500	1000	1500	μs
	t_{SS_LV2}	Time from V_{OUT_LV2} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LV3}	Time from V_{OUT_LV3} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LDO}	Time from the previous turn on channel's output voltage reaching 90% of target value to V_{OUT_LDO} rise to 90% of target value. (Note 9)	200	700	1100	
PG Delay Time	t_{DLY_PG}		9	10	11	ms

12.1 System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. (T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Over-Temperature Protection	OTP		--	160	--	°C
Over-Temperature Protection Hysteresis	OTP_H		--	20	--	°C
CH1 HVBuck1						
Maximum Output Current	$I_{OUT\_MAX\_HV1}$		1.5	--	--	A
Load Regulation	$V_{LOAD\_REG\_HV1}$	I_{OUT_HV1} = 0A to 1.5A	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_HV1}$	V_{IN} = 5V to 18.5V, I_{OUT_HV1} = 1.5A	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_HV1}$	I_{OUT_HV1} = 10mA to 500mA to 10mA, 1μs	–150	--	150	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Transient	$V_{LINE\_TRAIN\_HV1}$	V_{IN} = 5V to 18.5V to 5V, 100μs, I_{OUT_HV1} = 10mA/500mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_HV1}	Peak to peak in one switching cycle	--	--	20	mVpp
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT\_MAX\_LV2}$		1.5	--	--	A
Load Regulation	$V_{LOAD\_REG\_LV2}$	I_{OUT_LV2} = 0A to 1.5A	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_LV2}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV2} = 1.5A	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_LV2}$	I_{OUT_LV2} = 10mA to 500mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE\_TRAIN\_LV2}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV2} = 10mA/1A	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV2}	Peak to peak in one switching cycle	--	--	10	mVpp
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT\_MAX\_LV3}$		750	--	--	mA
Load Regulation	$V_{LOAD\_REG\_LV3}$	I_{OUT_LV3} = 0A to 750mA	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_LV3}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV3} = 750mA	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_LV3}$	I_{OUT_LV3} = 10mA to 300mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE\_TRAIN\_LV3}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV3} = 10mA/300mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV3}	Peak to peak in one switching cycle	--	--	10	mVpp
CH4 LDO (V_{IN_LDO} = 3.6V)						
Power Supply Rejection Ratio	$PSRR_{\_LDO}$	I_{OUT_LDO} = 100mA, f = 100kHz	--	60	--	dB
		I_{OUT_LDO} = 100mA, f = 1MHz	--	40	--	
Output Noise Voltage	$eN_{\_LDO}$	I_{OUT_LDO} = 100mA, f = 100Hz to 100kHz	--	60	--	μV
Load Transient	$V_{LOAD\_TRAIN\_LDO}$	I_{OUT_LDO} = 10mA to 200mA to 10mA, 1μs	–25	--	25	mV
Line Transient	$V_{LINE\_TRAIN\_LDO}$	All V_{OUT_LDO}, V_{IN_LDO} step 600mV, LDO not in dropout condition, 10μs, I_{OUT_LDO} = 1mA/300mA	–25	--	25	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Component Requirement (Note 5)						
Effective Input Capacitance	C_{IN_HV1}		1.5	4.7	10	µF
	C_{IN_PVD23}		1.5	4.7	10	
	C_{IN_LDO}		0.7	2.2	4	
Effective Output Capacitance	C_{OUT_HV1}		3.3	10	14	µF
	C_{OUT_LV2}		4.5	10	14	
	C_{OUT_LV3}		4.5	10	14	
	C_{OUT_LDO}		0.7	2.2	4	
Output Inductance	L_{HV1}		1	1.5	2	µH
	L_{LV2}		0.68	1	1.2	
	L_{LV3}		0.68	1	1.2	
Effective Boot Capacitance	C_{BOOT}		0.07	0.1	0.13	µF
Effective PVCC Capacitance	C_{PVCC}		0.3	1	1.4	µF

Note 6. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Note 7. The LDO only supports loading smaller than 150mA (typical) to power up successfully. The current limit changes back to 450mA 8ms after the LDO rail is enabled.

Note 8. PVCC is the pre-regulator output voltage only for internal circuitry. External loading on the PVCC pin is forbidden.

Note 9. The t_{SS_LDO} depends on the total output capacitance of the LDO. The soft-start time without loading can be calculated using the following formula: $t_{SS\_LDO} = (C_{OUT\_LDO} \times V_{OUT\_LDO}) / 0.15$.

13 Typical Application Circuit

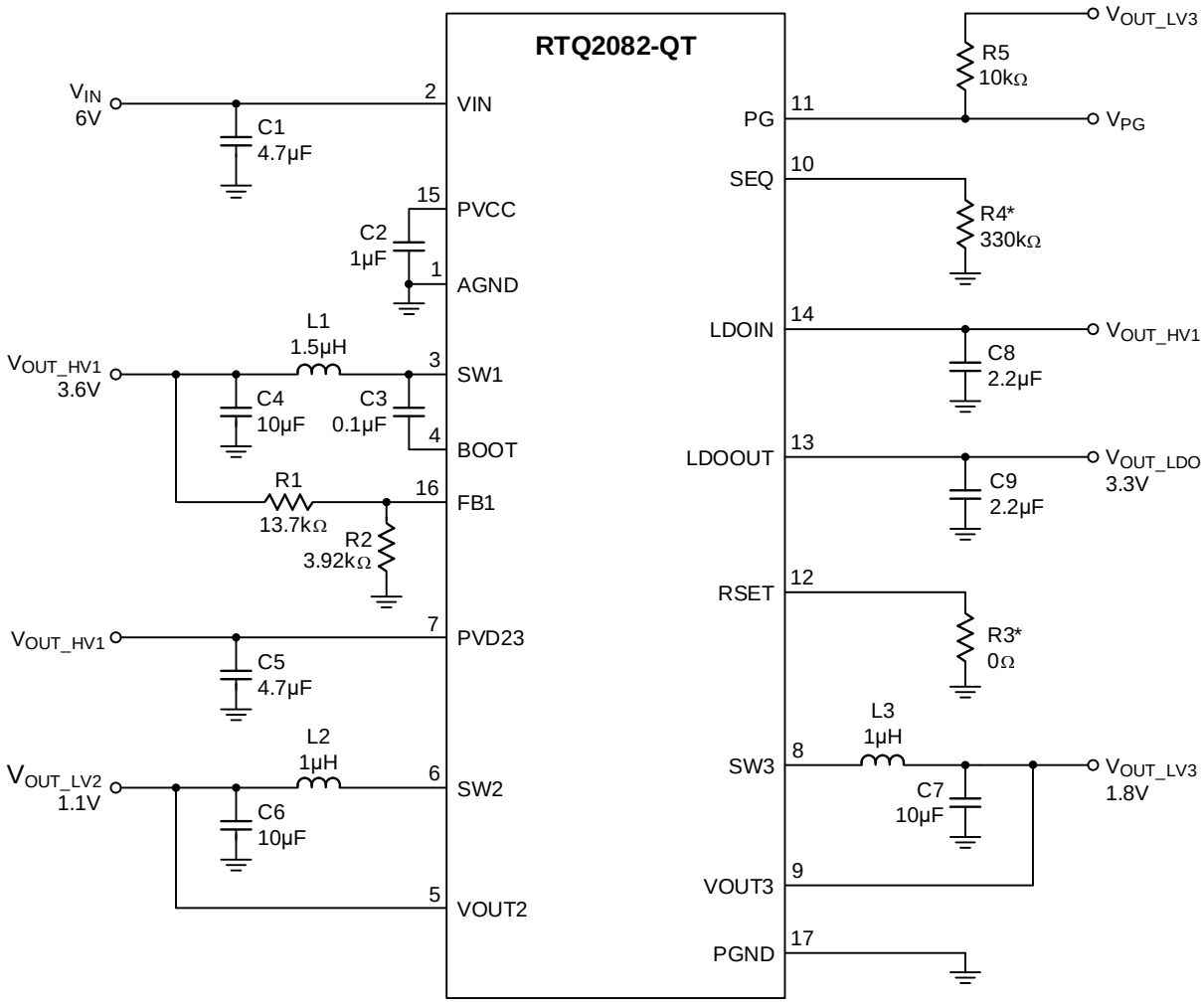


Table 1. Component List of Evaluation Board

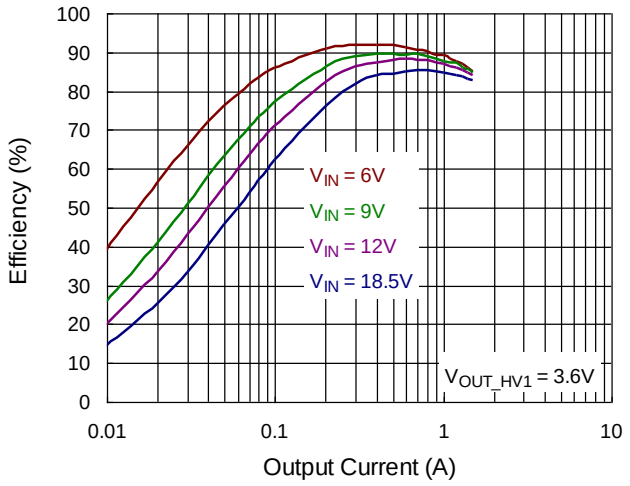
Reference	Qty	Part Number	Description	Package	Manufacturer
C1	1	GCJ31CR71E475KA12	4.7μF/25V/X7R	1206	MURATA
C2	1	GRT155C81A105KE01	1μF/10V/X6S	0402	MURATA
C3	1	GRT155R71C104KE01	0.1μF/16V/X7R	0402	MURATA
C4, C6, C7	1	GRT188C81A106ME13	10μF/10V/X6S	0603	MURATA
C5	1	GRT188C81C475KE13	4.7μF/16V/X6S	0603	MURATA
C8, C9	1	GRT155C81A225KE13	2.2μF/10V/X6S	0402	MURATA
L1	1	TFM201610ALMA1R5MTAA	1.5μH/3.1A/85mΩ	0806	TDK
L2, L3	1	TFM201610ALMA1R0MTAA	1μH/3.7A/50mΩ	0806	TDK
R1	1	MR02X1372FAL	13.7kΩ/1%	0201	WALSIN
R2	1	MR02X3921FAL	3.92kΩ/1%	0201	WALSIN
R3 (Note 10)	1	MR02X000 PAL	0Ω/Jumper	0201	WALISN
R4 (Note 11)	1	MR02X3303FAL	330kΩ/1%	0201	WALSIN
R5	1	MR02X1002FAL	10kΩ/1%	0201	WALSIN

Note 10. Resistor is adjustable with different LDO output voltages.

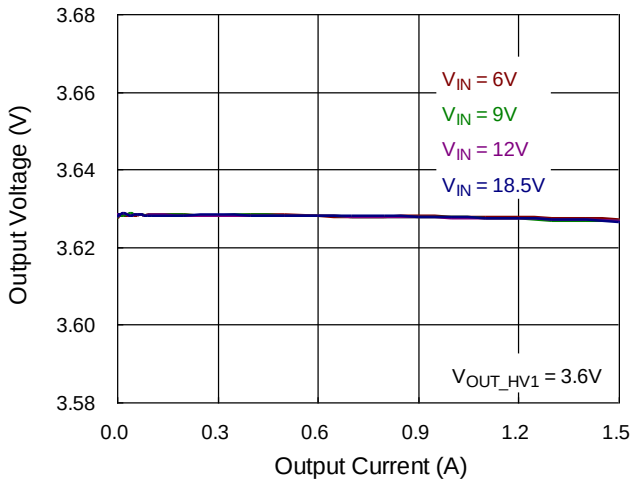
Note 11. Resistor is adjustable with different power-on sequences.

14 Typical Operating Characteristics

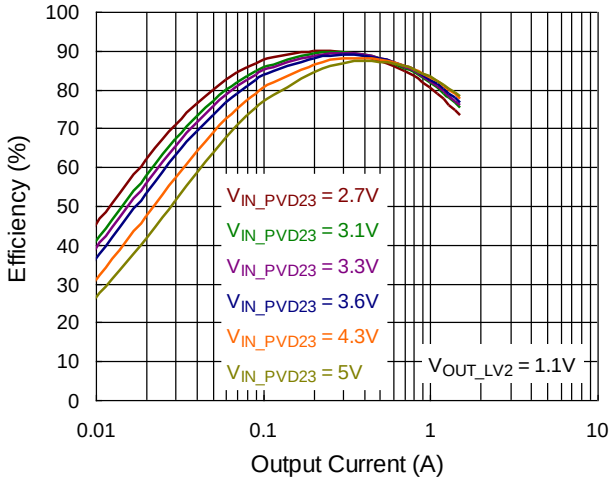
HVBuck1 Efficiency



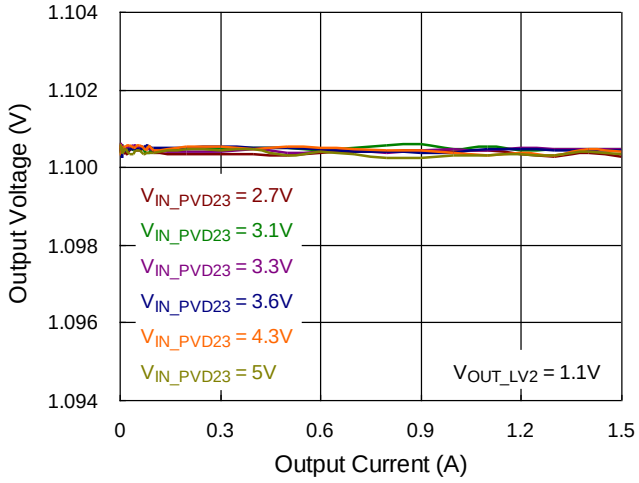
HVBuck1 Load Regulation



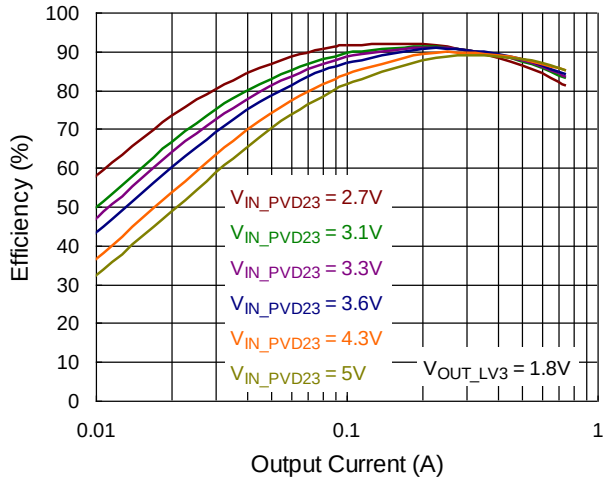
LVBuck2 Efficiency



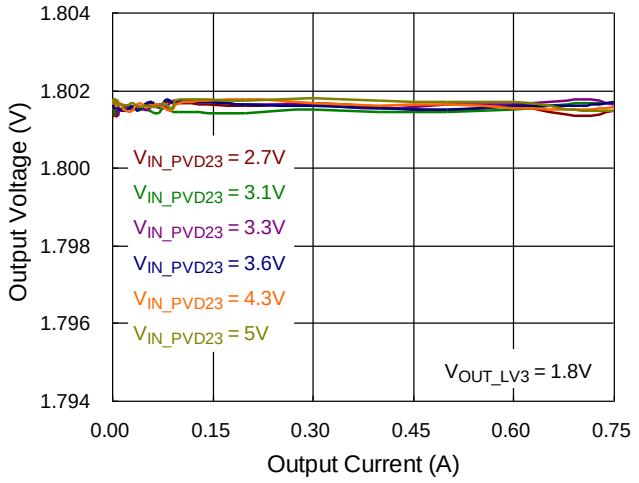
LVBuck2 Load Regulation



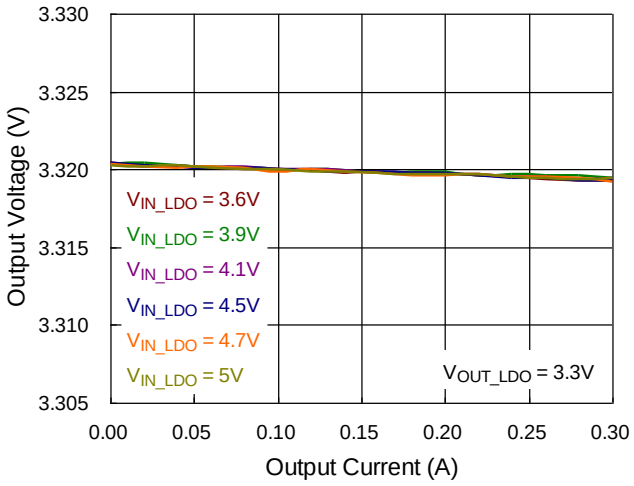
LVBuck3 Efficiency



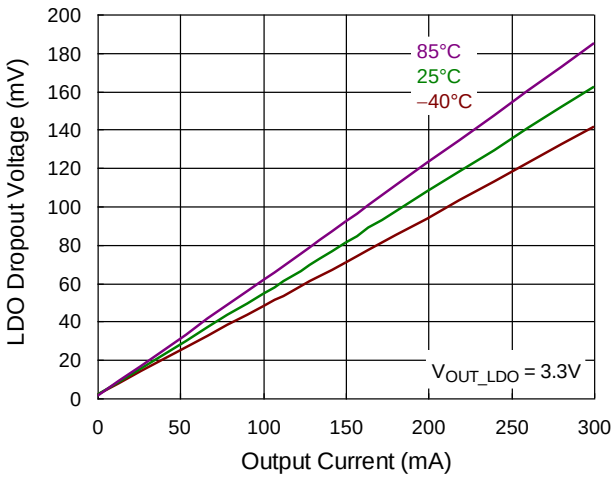
LVBuck3 Load Regulation



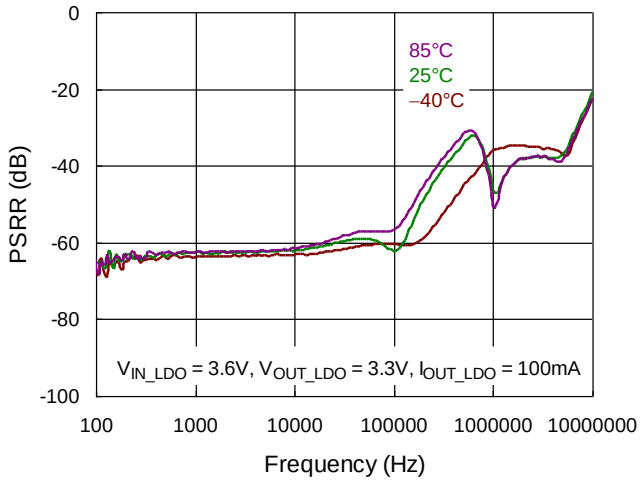
LDO Load Regulation



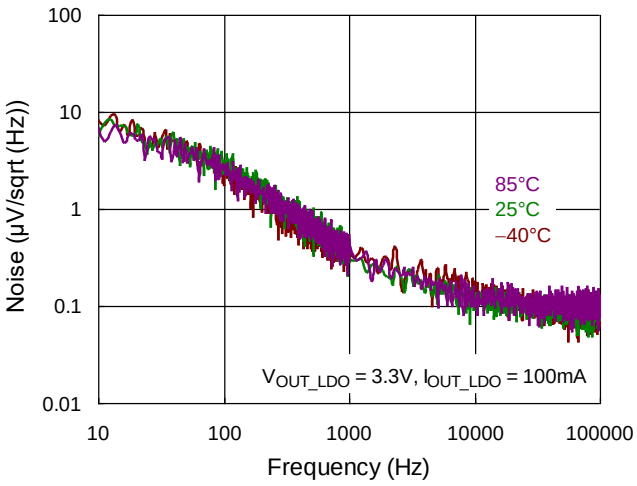
LDO Dropout Voltage vs. Output Current



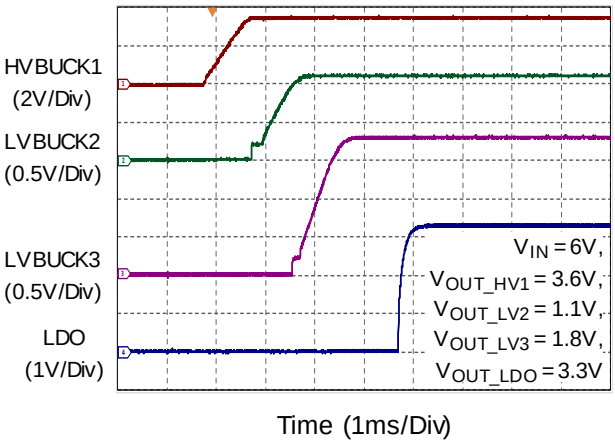
LDO PSRR



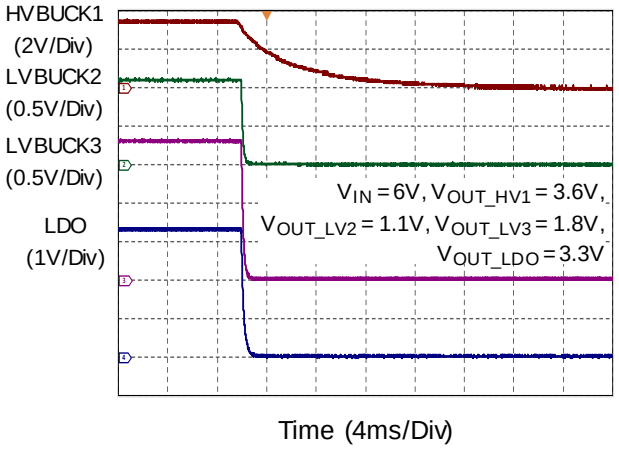
LDO Output Noise



SEQ9 Power On



SEQ9 Power Off



15 Operation

The RTQ2082-QT is a highly integrated power management integrated circuit (PMIC) for automotive camera systems. It includes three step-down converters (CH1 HVBuck1, CH2 LVBuck2, and CH3 LVBuck3) and one generic LDO (CH4 LDO).

15.1 System Undervoltage Protection and Overvoltage Protection

The RTQ2082-QT stops operating if the V_{IN} voltage falls below the Undervoltage Lockout level (UVLO_L). A typical 500mV hysteresis is implemented to avoid unstable on/off behaviors. The shift values of UVLO_H and UVLO_L both move in the same direction (either positive or negative at the same time). The device is initialized to its default state after the V_{IN} voltage recovers from UVLO_H. When the V_{IN} voltage reaches the overvoltage protection level, the step-down converters and LDO are disabled immediately. The IC then enters a latch-off state and can only be r-started by toggling the V_{IN} power. Meanwhile, the PG status will be set to 0V to indicate an IC fault condition.

15.2 Over-Temperature Protection

The RTQ2082-QT features over-temperature protection (OTP). When the junction temperature exceeds the typical threshold of 160°C, OTP is activated, disabling all outputs as the device enters a latch-off state. Once the RTQ2082-QT recovers from OTP, the device can only be restarted by toggling the V_{IN} power.

15.3 Pre-Regulator

The device integrates a 4.45V linear regulator (PVCC) supplied by V_{IN} to provide power to the internal circuitry. The PVCC can be used as the pull-up supply for the RSET and SEQ pins, but it is “NOT” allowed to power any other device or circuitry. A 1μF decoupling capacitor must be connected between PVCC and AGND to filter noise, and it should be placed as close as possible to the PVCC pin.

15.4 Peak Current Mode Control

The three step-down converters utilize peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. By comparing the inductor peak current signal during the high-side MOSFET switch on interval with the internal compensation signal derived from the sensed feedback voltage and reference voltage, the high-side MOSFET switch is turned off and the inductor current continues to flow through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, the regulated inductor current controls duty cycle and output voltage of the converter.

15.5 Spread-Spectrum Operation

Due to the periodicity of the switching signal, energy tends to concentrate at the fundamental frequency and its N-order harmonics. This concentration of energy can result in radiation that may cause EMI issues. The RTQ2082-QT is equipped with a spread-spectrum function to meet CISPR and automotive EMI compliance standards. The spread-spectrum function is implemented using a pseudo-random sequence and applies a +6% spread to the switching frequency. For example, with a 2.1MHz typical switching frequency, the actual frequency will randomly oscillate between 2.1MHz and 2.226MHz. As a result, the RTQ2082-QT effectively prevents the switching frequency from interfering with the 1.8MHz AM band limit.

15.6 Phase-Shifted Operation

The RTQ2082-QT supports phase-shift operation to prevent all step-down converters from switching simultaneously, thereby further reducing the radiation energy. The phase-shift difference in the clock between each step-down converter automatically adjusts based on the numbers of enabled channels. For example, when two step-down converters are in use, the initial turn-on time between two high-side MOSFETs has a 180-degree phase difference. Likewise, there is a 120-degree phase difference when three step-down converters are in use.

15.7 Channel Floating Allowable

To save PCB layout space and reduce material costs, the unused low-voltage step-down converters (CH2/CH3) can be left with floating pins (SW2/SW3), eliminating the need for inductors and output capacitors. The PVD23 pin must be connected to a fixed voltage for floating detection, and it is permissible to omit the capacitor placement. The RTQ2082-QT automatically detects the pin status during the power-on procedure to determine whether the channel is used. After this detection, any malfunction in an unused channel will not impact the device's operation.

15.8 Power-Good Indication

The RTQ2082 features an open-drain power-good output (PG) to monitor the output voltage status. Connect a pull-up resistor from the PG pin to an external voltage. Note that it is forbidden to use PVCC as the pulled-up voltage for the PG pin. When the last channel in the power-on sequence reaches 90% of its target output voltage, the PG signal is pulled high to indicate a "Power-Good" status after a 10ms delay, until the device is disabled, or any other protection is triggered.

Table 2. Unused Channel Pin Connection

Unused Channel	Unused Pin Number	Unused Pin Name	Pin Configuration
LVBuck2	5	VOUT2	Floating
	6	SW2	Floating
	7	PVD23	Connect to a stable voltage
LVBuck3	7	PVD23	Connect to a stable voltage
	8	SW3	Floating
	9	VOUT3	Floating

16 Application Information

(Note 12)

16.1 Power Sequence Control

The RTQ2082 supports 10 power-on sequences for the step-down converters and LDO via the dedicated resistor on the SEQ pin. The SEQ pin must not be left floating, and resistance selected out of range is not guaranteed to result in the correct power-on sequence. In addition, there is only simultaneous power-off for all outputs. Ensure the resistor selection on the SEQ pin is fixed before enabling the device. Any change during the power-on procedure is not guaranteed to result in the correct power-on sequence. The table below shows the power-on sequence with its corresponding resistance.

Table 3. Power-On Sequence Control

SEQ No.	Resistance on SEQ (Ω)			Sequence				
	Min	Typ	Max					
SEQ0	1.07M	1.1M	1.13M	CH1	CH4	CH3	CH2	1ms
SEQ1	319k	330k	341k	CH1	CH2	CH3	1ms	CH4
SEQ2	164k	169k	174k	CH1	CH2	1ms	CH3	CH4
SEQ3	81.6k	84.5k	87.4k	CH1	1ms	CH2	CH4	CH3
SEQ4	45.4k	47k	48.6k	CH1	CH2, CH3, CH4			
SEQ5	26.1k	27k	27.9k	CH1, CH2, CH3, CH4				
SEQ6	14.5k	15k	15.5k	CH1	CH3	CH2	CH4	1ms
SEQ7	7.78k	8.06k	8.34k	CH1	CH3	CH4	CH2	1ms
SEQ8	Short to PVCC			CH1	1ms	CH2	CH3	CH4
SEQ9	Short to PGND			CH1	CH2	CH3	CH4	1ms

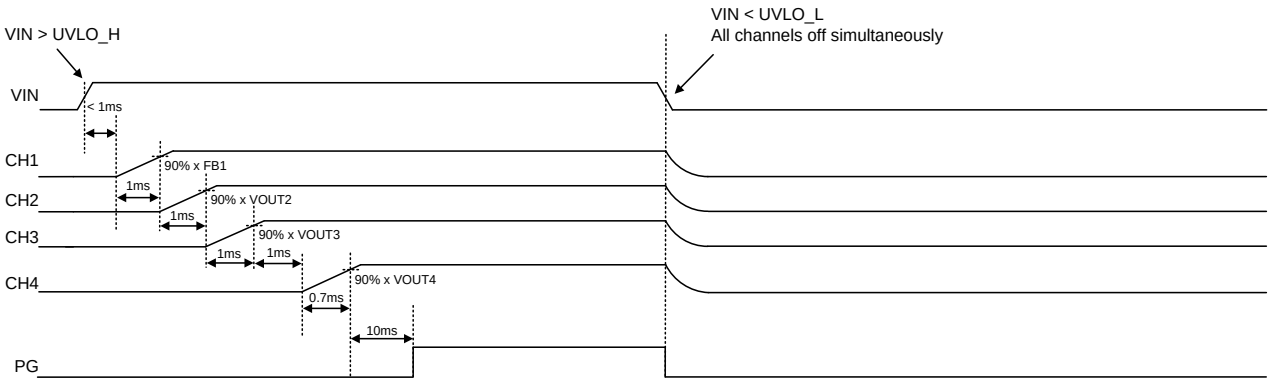


Figure 1. Example SEQ1

16.2 Output Voltage Setting

16.2.1 HVBuck1

The output voltage set by external feedback resistors is expressed in the following equation:

$$V_{OUT\_HV1} = \left(1 + \frac{R1}{R2}\right) \times V_{FB1}$$

where the reference voltage V_{FB1} is 0.8V (typical)

The placement of the resistive divider should be as close as possible to the FB1 pin. For better output voltage accuracy, the divider resistors with ±1% tolerance or better should be used. The recommended resistance ranges from a few kΩ to hundreds of kΩ.

16.2.2 LVBuck2 and LVBuck3

The output voltage of LVBuck2 is fixed 1.1V.

The output voltage of LVBuck3 is fixed 1.8V.

16.2.3 LDO

The LDO output voltage is controlled by setting the dedicated resistor on the RSET pin. The RSET pin must not be left floating, and resistance selected out of range is not guaranteed to result in the correct output voltage. Changing the output voltage in real-time is not recommended. Ensure the resistor selection on RSET pin is fixed before enabling the device.

Table 4. LDO Output Voltage

RSET No.	Resistor on REST (Ω)			Voltage (V)
	Min	Typ	Max	
RSET0	1.07M	1.1M	1.13M	3.5
RSET1	319k	330k	341k	3.4
RSET2	164k	169k	174k	3.2
RSET3	81.6k	84.5k	87.4k	3.1
RSET4	45.4k	47k	48.6k	3.0
RSET5	26.1k	27k	27.9k	2.8
RSET6	14.5k	15k	15.5k	2.7
RSET7	7.78k	8.06k	8.34k	1.8
RSET8	Short to PVCC			2.9
RSET9	Short to PGND			3.3

16.3 Channel Protection Features

The RTQ2082 is equipped with protections to prevent the device from being damaged by abnormal operations or fault conditions (For example, overload, short-circuit, soldering issues, etc.).

16.3.1 Undervoltage Protection (UVP)

16.3.1.1 HVBuck1, LVBuck2, LVBuck3, and LDO

The device disables all channels and enters the latch-off state if a step-down converter or LDO output

undervoltage fault is detected continuously over the deglitch time. The device can only be restarted by toggling the V_{IN} power.

16.3.2 Overvoltage Protection (OVP)

16.3.2.1 HVBuck1

When an overvoltage fault is detected at the FB1 pin, the high-side and low-side MOSFETs turn off immediately and auto-recover to switch until the FB1 pin's voltage decreases to the reset level.

16.3.2.2 LVBuck2, LVBuck3, and LDO

The device disables all channels when a step-down converter or LDO output overvoltage fault is detected continuously over the deglitch time. When the fault is cleared, the device auto-restarts all channels in sequence.

16.3.3 Overcurrent Protection (OCP)

16.3.3.1 HVBuck1, LVBuck2, and LVBuck3

The step-down converter includes a cycle-by-cycle high-side MOSFET overcurrent protection against the condition where the inductor current increases abnormally, even over the inductor saturation current rating. If an overcurrent condition occurs, the controller will immediately turn off the high-side MOSFET and turn on the low-side MOSFET to prevent the inductor current from exceeding the peak current limit level. After the inductor current decreases below the valley current limit, the high-side MOSFET resumes switching on. If an overcurrent fault is further detected continuously over the deglitch time, the device disables all channels and enters the latch-off state. The device can only be restarted by toggling the V_{IN} power.

16.3.3.2 LDO

When the load reaches the current-limit threshold, the current sent to the output will be kept at current limit level. If overcurrent fault detected continuously over the deglitch time, the device disables all channels and enters the latch off state and the device only can re-start with V_{IN} ON/OFF.

16.3.4 Input Overvoltage Protection (OVP)

16.3.4.1 LVBuck2, LVBuck3, and LDO

If the input voltage of the step-down converters (LVBuck2, LVBuck3) or LDO reaches the overvoltage protection level, the device disables all channels. After the fault is removed, it auto-restarts all channels in sequence.

Table 5. Protection Behavior

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Protection	Reset and Threshold (Typical)
System	UVLO	$V_{IN} \leq 3.3V$	32µs	Disable all channels	$V_{IN} \geq 3.8V$
	OVP	$V_{IN} \geq 20V$	5ms	Disable all channels and then enter latch-off protection	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	OTP	$T_J \geq 160°C$	5µs	Disable all channels and then enter latch-off protection	$T_J \leq 140°C$ and $V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Protection	Reset and Threshold (Typical)
CH1 HVBuck1	UVP	$V_{FB1} \leq 0.8V \times 50\%$	5µs	Disable all channels and then enter latch-off protection.	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	OVP	$V_{FB1} \geq 0.8V \times 110\%$	NA	High/Low-side MOSFETs off, low-side MOSFET conditionally ON to charge the BOOT capacitor for driving high-side MOSFET.	$V_{FB1} < 0.8V \times 110\%$
	OCP	$I_{L1\_peak} \geq 3A$	10ms	Cycle-by-cycle detection. If the condition persists for10ms, disable all channels and then enter latch-off protection.	If Buck1 enters latch-off protection, $V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
CH2 LVBuck2	UVP	$V_{OUT\_LV2} \leq 1.1V \times 50\%$	5µs	Disable all channels and then enter latch-off protection.	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	OVP	$V_{OUT\_LV2} \geq 1.1V \times 120\%$	5ms	Disable all channels	$V_{OUT2} \leq 1.1V \times 110\%$ with deglitch 5ms
	OCP	$I_{L2\_peak} \geq 2A$	10ms	Cycle-by-cycle detection. If the condition persists for10ms, disable all channels and then enter latch-off protection.	If Buck2 enters latch-off protection, $V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	Input OVP	$V_{IN\_PVD23} \geq 5.8V$	5µs	Disable all channels	$V_{IN\_PVD23} \leq 5.22V$ with deglitch 5µs
CH3 LVBuck3	UVP	$V_{OUT\_LV3} \leq 1.8V \times 50\%$	5µs	Disable all channels then latch-off protection.	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	OVP	$V_{OUT\_LV3} \geq 1.8V \times 120\%$	5ms	Disable all channels	$V_{OUT3} \leq 1.8V \times 110\%$ with deglitch 5ms
	OCP	$I_{L3\_peak} \geq 1.2A$	10ms	Cycle-by-cycle detection. If the condition persists for10ms, disable all channels and then enter latch-off protection.	If Buck3 enters latch-off protection, $V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$
	Input OVP	$V_{IN\_PVD23} \geq 5.8V$	5µs	Disable all channels	$V_{IN\_PVD23} \leq 5.22V$ with deglitch 5µs

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Protection	Reset and Threshold (Typical)
CH4 LDO	UVP	$V_{OUT\_LDO} \leq$ V_{OUT_LDO} setting x 40%	5µs	Disable all channels and then enter latch-off protection.	$V_{IN} \leq$ 3.3V, then $V_{IN} \geq$ 3.8V
	OVP	$V_{OUT\_LDO} \geq$ V_{OUT_LDO} x 125%	5ms	Disable all channels	$V_{OUT\_LDO} \leq$ V_{OUT_LDO} x 110% with deglitch 5ms
	OCP	$I_{OUT\_LDO} \geq$ 450mA	10ms	Disable all channels and then enter latch-off protection.	$V_{IN} \leq$ 3.3V, then $V_{IN} \geq$ 3.8V
	Input OVP	$V_{IN\_LDO} \geq$ 5.8V	5µs	Disable all channels	$V_{IN\_LDO} \leq$ 5.3V with deglitch 5µs

16.4 Input and Output Capacitor Selection

16.4.1 HVBuck1, LVBuck2, and LVBuck3

It is recommended to use at least a 4.7µF input capacitor with a 10µF output capacitor for step-down converters. The ripple voltage is an important parameter when choosing the output capacitor. This portion consists of two parts. One is the product of the ripple current and the ESR of the output capacitor; the other is generated by the charging and discharging cycles of the output capacitor. The output ripple voltage can be calculated using the following formula:

$$\Delta V_{OUTRipple} = \Delta V_{ESR} + \Delta V_{OUT} = \Delta V_{ESR} + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

16.4.2 LDO

Proper selection of external capacitors is crucial for the stability and performance of any LDO. A 2.2µF capacitor is generally suitable for both the input and output of the LDO. Additional capacitors in parallel on the output can enhance noise suppression, but it may also result in increased inrush current during the LDO's power-up sequence. This potential trade-off should be carefully evaluated.

16.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WETD-VQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be

calculated as below:

$P_{D(MAX)}$ = (150°C – 25°C) / (30°C/W) = 4.16W for a WETD-VQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

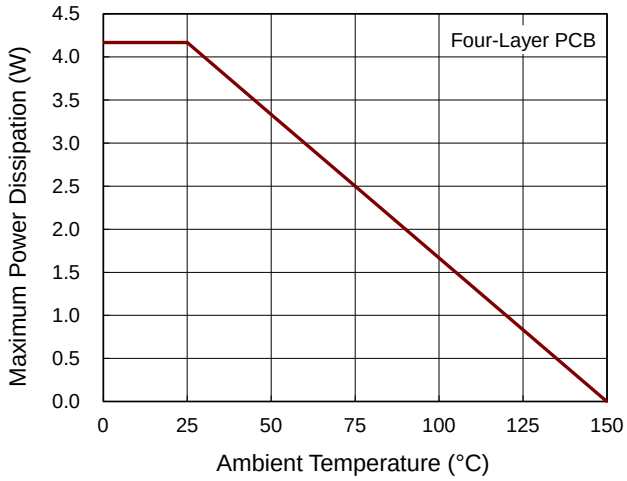


Figure 2. Derating Curve of Maximum Power Dissipation

16.6 Layout Considerations

The PCB layout is an important factor in maintaining the high performance of the RTQ2082-QT. Special attention must be given to the high current paths and fast-switching nodes in the PCB layout to ensure the robustness of the RTQ2082-QT. An improper layout can result in issues such as poor line or load regulation, shifts in ground and output voltage, stability problems, unsatisfactory EMI performance, or reduced efficiency. To optimize the performance of the RTQ2082-QT, the following PCB layout guidelines must be strictly followed:

- The trace from the switching node to the inductor should be kept as short as possible to minimize the switching loop, which will help to improve EMI characteristics.
- Place the input and output capacitors as close as possible to their respective pins to ensure effective filtering.
- Keep the main power traces as wide and short as possible.
- Connect the AGND and PGND to a solid ground plane to enhance thermal dissipation and provide noise immunity.
- Directly connect the step-down converter’s output capacitor to the feedback network to avoid voltage deviations caused by parasitic resistance and inductance in the PCB traces.

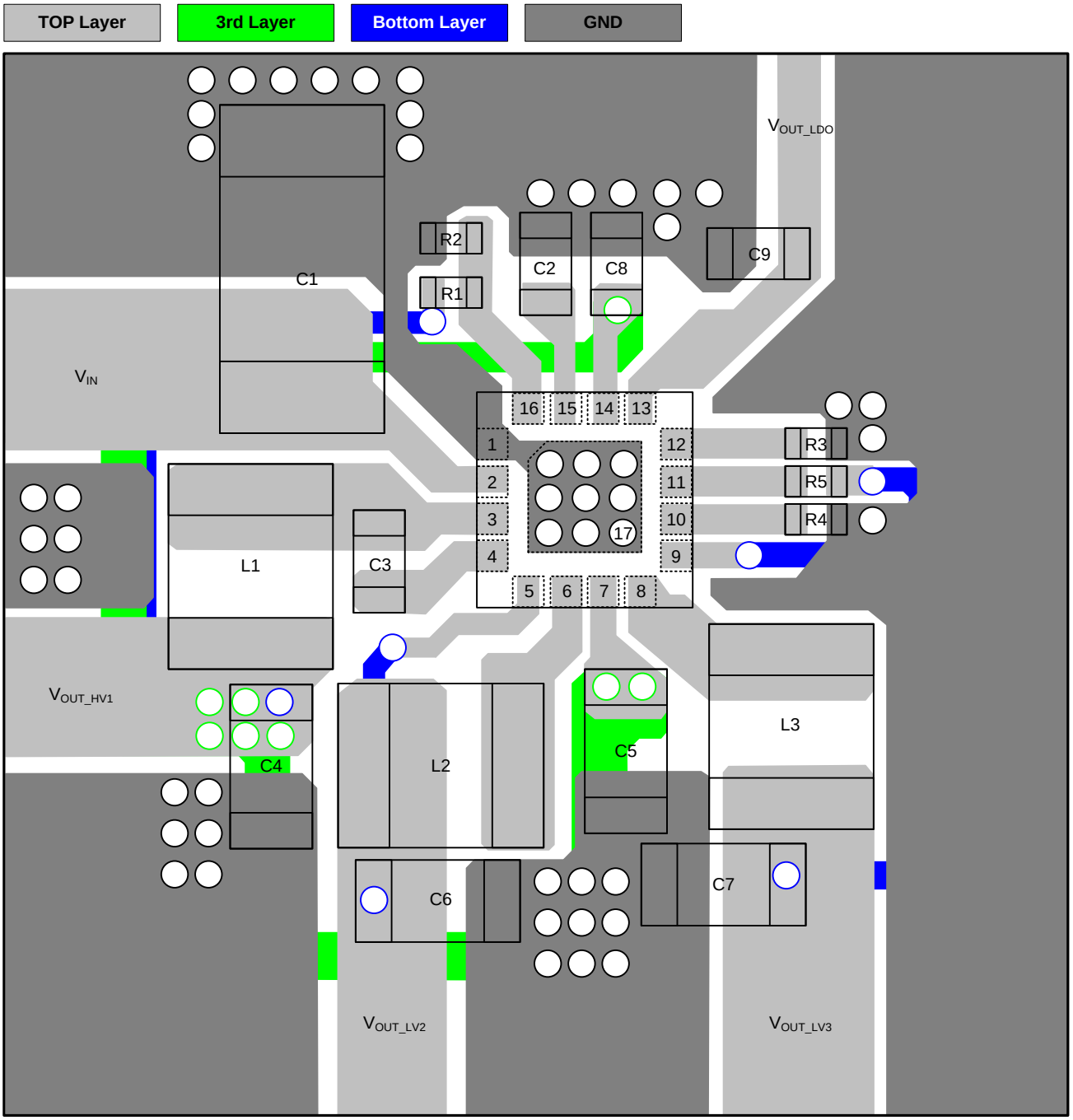
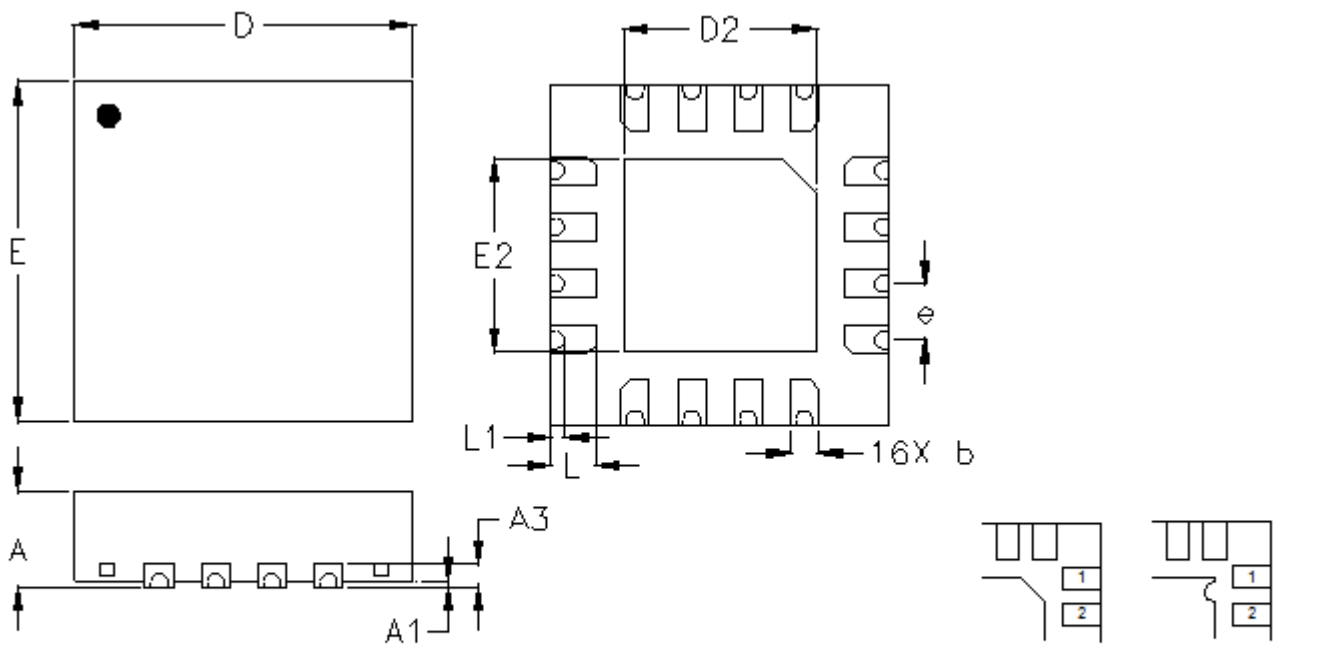


Figure 3. PCB Layout Guide

Note 12. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension



DETAIL A

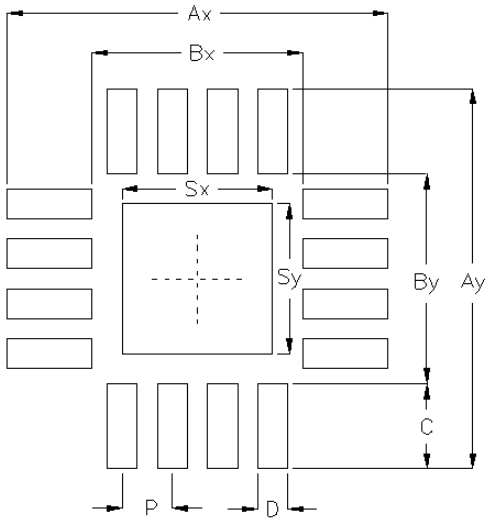
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.650	1.750	0.065	0.069
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.075	0.175	0.003	0.007

WETD V-Type 16L QFN 3x3 Package

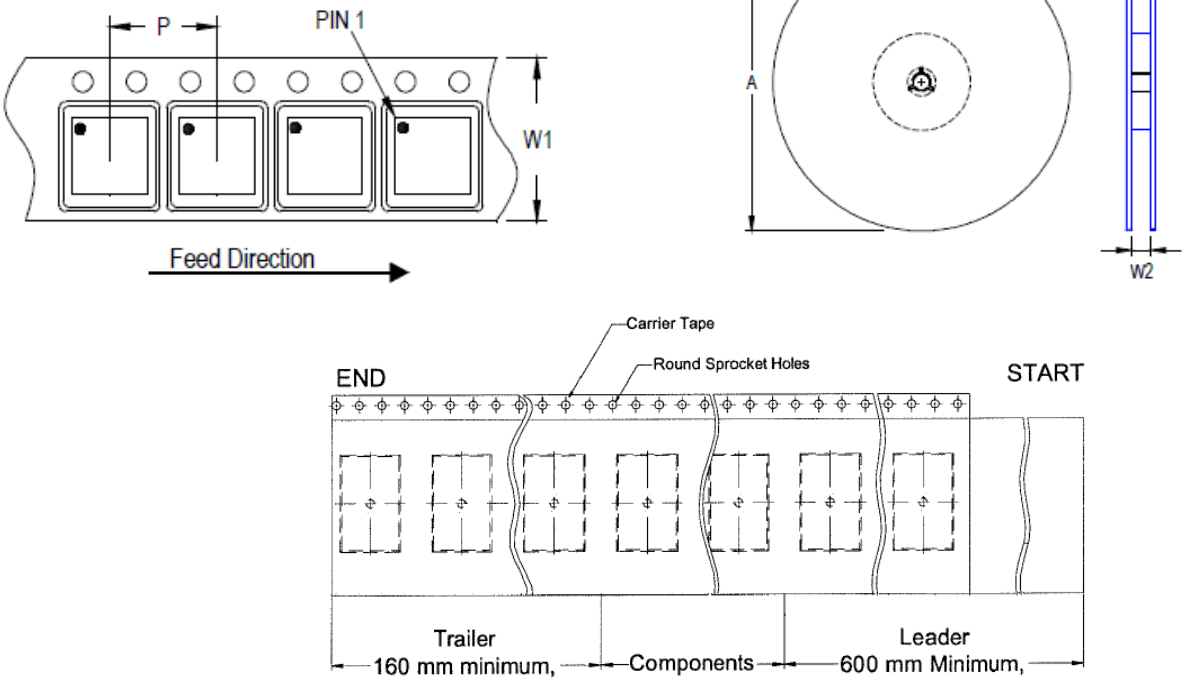
18 Footprint Information



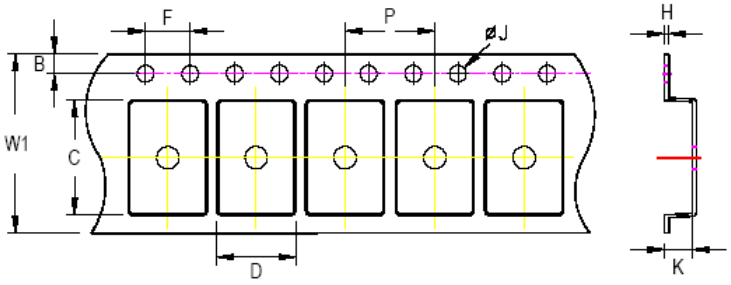
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WETD-V/W/U/XQFN3x3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

20 Datasheet Revision History

Version	Date	Description	Item
00	2024/8/7	Final	Absolute Maximum Ratings on P7 Electrical Characteristics on P8, 10, 11, 13 Application Information on P24, 25