RICHTEK®

RTQ2079-QF

Functional Safety PMIC for Automotive Camera Sensors/ Modules

1 General Description

The RTQ2079-QF is a highly integrated PMIC designed for automotive camera applications. It includes three step-down converters, one high PSRR low-dropout (LDO) regulator, and one general low-dropout (LDO) regulator.

The high-voltage step-down converter operates with an input voltage range of up to 24V and is capable of sustaining a 36V load dump. It is suitable for a direct connection to a 12V battery or Power Over Coaxial (PoC) connection.

The RTQ2079-QF offers overvoltage and undervoltage monitors, two error input receivers, one error output indicator, and fault status reported by I^2C for system fault reporting purpose.

The device offers system design flexibility with I^2C or factory-trimmed configurable functions, including adjustable output voltage for each channel, customizable power-on sequencing, and overvoltage (OV) or undervoltage (UV) monitor threshold voltage. The RTQ2079-QF is available in a WET-WQFN-24AL 4x4 package with wettable flanks.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 125°C.

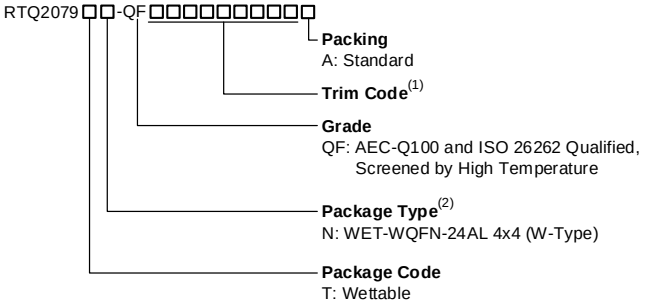
2 Applications

- Function Safety Related Automotive Camera Modules
  - Surround View Cameras
  - Front View Cameras
  - Rear View Cameras
  - Dash Cams
  - Driver Monitoring Systems
  - Cabin Monitors
  - eMirrors

3 Features

- **AEC-Q100 Grade 1 Qualified**
- **Compliance with ISO 26262 ASIL B**
- **Power-On Built-In Self-Test (BIST) for OV/UV Monitors, I^2C Cyclic Redundancy Check (CRC), and OTP Register CRC Protection**
- **Three Step-Down Converters (HVBuck1, LVBuck2, and LVBuck3) with Peak-Current Mode PWM Operation and PSM Mode for Sentry Mode via I^2C Setting**
  - **Fixed Switching Frequency at 2.1MHz**
  - **EMI Reduction Features including Spread Spectrum and Phase-Shift Operation**
  - **HVBuck1 Supports Input Voltage from 4V to 24V with Load Dump Protection (36V for ≤ 400ms Transient), Adjustable Output Voltage, and up to 1.5A Output Current**
  - **LVBuck2 and LVBuck3 Support Input Voltage from 2.7V to 5V, Adjustable Output Voltage, and up to 1.5A Output Current**
  - **Pins Related to LVBuck2/LVBuck3 Can Float if the Channel is Unused**
- **Two Low-Dropout Regulators (LDO1 and LDO2)**
  - **LDO1 with 2.7V to 5V Input Voltage, Adjustable Output Voltage, up to 0.3A Output Current, and High PSRR with 0.1A Output Current (60dB at 100kHz, 40dB at 1MHz)**
  - **LDO2 with 2.7V to 5V Input Voltage, Adjustable Output Voltage, and up to 0.4A Output Current**
- **Input and Output Functions**
  - **Sequence Control for External IC via SEQOUT**
  - **Power Status Indication via PGOOD**
  - **Error Status Indication via ERROUT**
  - **Two Error Signal Receivers via ERRIN1/ERRIN2**
  - **External Voltage Monitor via VMONIN**
- **Small Form Factor**
  - **Wettable WET-WQFN-24AL 4x4 Package with Compact BOM**
- **Junction Temperature Range: –40°C to 125°C**
- **Ambient Temperature Range: –40°C to 125°C**

4 Ordering Information



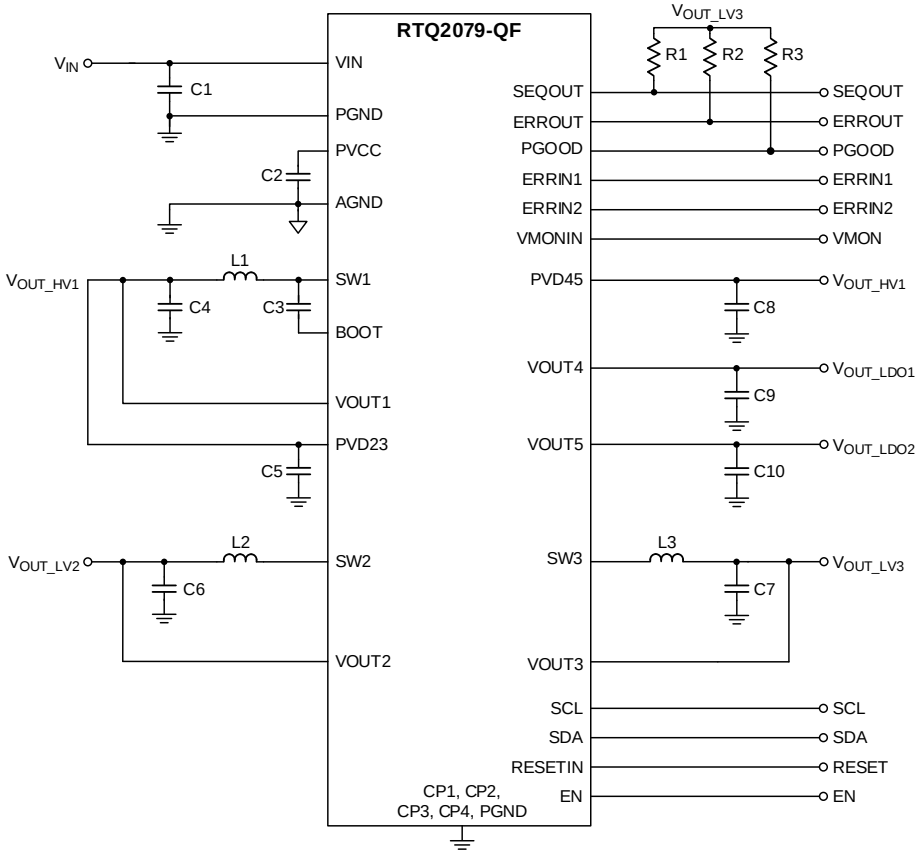
Note 1.

- Marked with (1) indicated: The trim code for UVLO, POWER_ON_SEQ, ON_Td, OFF_Td + UV_SD, HVBUCK1 VOUT, LVBUCK2 VOUT, LVBUCK3 VOUT, LDO1 VOUT, and LDO2 VOUT settings has various combinations. For more details, contact our sales representative directly or through a Richtek distributor in your area.
- Richtek products are Richtek Green Policy compliant and marked with (2) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit



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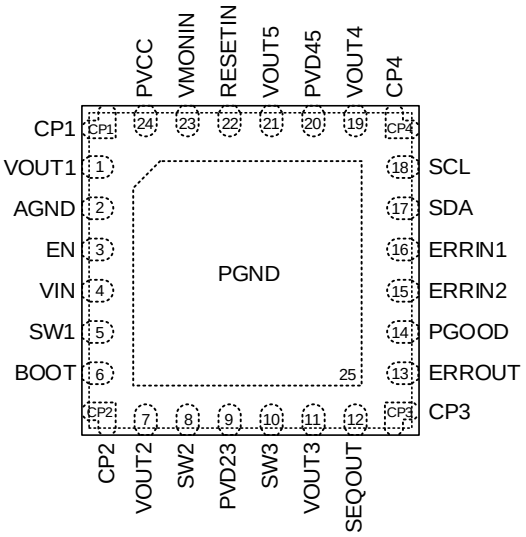
7 Pin Configuration

(TOP VIEW)



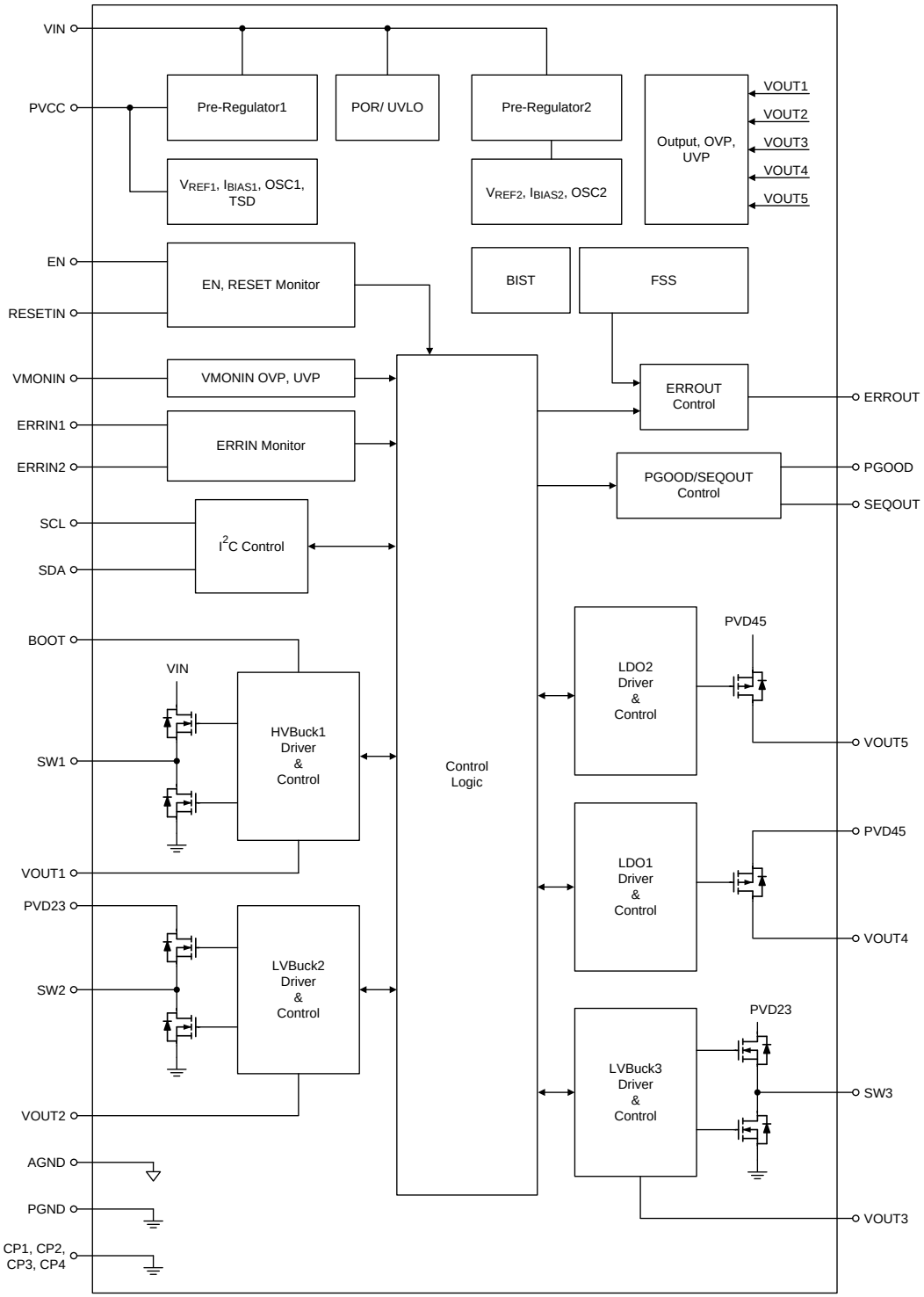
WET-WQFN-24AL 4x4

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUT1	HVBuck1 output voltage feedback. It is recommended to directly connect the output capacitor node to this pin for better regulation.
2	AGND	Analog ground for the PMIC analog circuit.
3	EN	Chip hardware enable input pin. When the EN = High, the I^2C read/write function is enabled.
4	VIN	HVBuck1 and PMIC system input source power.
5	SW1	HVBuck1 switch node.
6	BOOT	HVBuck1 BOOT pin.
7	VOUT2	LVBuck2 output voltage feedback. It is recommended to directly connect the output capacitor node to this pin for better regulation.
8	SW2	LVBuck2 switch node.
9	PVD23	LVBuck2/3 input source power. Assume that PVD23 connects to the HVbuck1 output.
10	SW3	LVBuck3 switch node.
11	VOUT3	LVBuck3 output voltage feedback. It is recommended to directly connect the output capacitor node to this pin for better regulation.
12	SEQOUT	Open-drain output. Use this pin to enable an external device for the desired system ON/OFF sequence.
13	ERROUT	Open-drain output. ERROUT changes the output status until the PMIC detects faults for indication.
14	PGOOD	Open-drain output, PMIC power status for indication. When PGOOD is in a high state, it indicates that all outputs are functioning normally.
15	ERRIN2	Error input monitor 2 for external system fault detection. This pin can be set to active high or active low by register.

Pin No.	Pin Name	Pin Function
16	ERRIN1	Error input monitor 1 for external system fault detection. This pin can be set to active high or active low by register.
17	SDA	I^2C interface serial data pin, open-drain. Connect to an external pull-up resistor is required.
18	SCL	I^2C interface serial clock input pin, open-drain. Connect to an external pull-up resistor is required.
19	VOUT4	LDO1 output pin. It is recommended to directly connect the output capacitor node to this pin for better regulation.
20	PVD45	LDO1/2 input source power. Assume that PVD45 connects to the HVbuck1 output.
21	VOUT5	LDO2 output pin. It is recommended to directly connect the output capacitor node to this pin for better regulation.
22	RESETIN	Chip external reset input pin.
23	VMONIN	Built-in OV/UV voltage monitor for external voltage detection.
24	PVCC	Internal analog power output. Connect a 1μF ceramic decoupling capacitor between this pin and ground. Additional external loading to this pin is forbidden.
25 (Exposed Pad)	PGND	IC thermal pad and power ground. It must be connected to the main ground plane for proper operation.
CP1	CP1	Corner Pins for package reliability improvement. There pins are internally connected to the Exposed Pad.
CP2	CP2	
CP3	CP3	
CP4	CP4	

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN, EN, SW1 ---------- –0.3V to 36V
- BOOT ---------- –0.3V to 36V
- BOOT to SW1 ---------- –0.3V to 5V
- VOUT1, VOUT2, SW2, PVD23, SW3, VOUT3, SEQOUT, ERROUT, PGOOD, ERRIN2, ERRIN1, SDA, SCL, VOUT4, PVD45, VOUT5, RESETIN, VMONIN, PVCC ---------- –0.3V to 6.5V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Rating

(Note 3)

- ESD Susceptibility

  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Voltage, VIN ---------- 4V to 24V
- Supply Voltage, VPVD23, VPVD45 ---------- 2.7V to 5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5)

Thermal Parameter		WET-WQFN-24AL 4x4	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	37	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	34.8	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	0.48	°C/W
θ_{JB}	Junction-to-board thermal resistance	9.72	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

14 Electrical Characteristics

(T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3}= 1.8V, V_{OUT_LDO1} = 3.3V, V_{OUT_LDO2} = 1.8V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Shutdown Current of VIN	$I_{SHUTDOWN}$	EN = L, V_{IN} ≤ 12V, V_{OUT_HV1} ties to PVD23 and PVD45	0	--	10	μA
VIN Undervoltage Lockout Falling	V_{UVLO_F}		3.1	3.3	3.465	V
			3.56	3.8	3.99	
			4.085	4.3	4.515	
			6.46	6.8	7.14	
VIN Undervoltage Lockout Rising	V_{UVLO_R}		3.55	3.8	3.99	V
			4.23	4.5	4.725	
			4.71	5	5.25	
			6.935	7.3	7.665	
VIN Overvoltage Rising Threshold	$V_{OVP\_R\_VIN}$		24.735	25.5	26.265	V
VIN Overvoltage Hysteresis	$V_{OVP\_HYS\_VIN}$		5	6	7	V
Pre-Regulator (Note 6)						
PVCC Voltage Range	V_{PVCC}		4.26	4.58	4.92	V
CH1_HVBuck1						
Input Voltage Range	V_{IN_HV1}	V_{IN_HV1} = VIN	4	--	24	V
Output Voltage Range	V_{OUT_HV1}	V_{IN_HV1} = 4V to 24V	2.7	--	5	V
Output Voltage Accuracy	$V_{OUT\_ACC\_HV1\_FPWM}$	V_{OUT_HV1} = 2.7V to 5V, V_{IN_HV1} = 6V, 9V, 12V, I_{OUT_HV1} = 0 to 1.5A, FPWM	–1.5	--	1.5	%
Soft-Start Time	t_{SS_HV1}	Time for V_{OUT_HV1} to rise from 10% to 90% of the target value, no load	500	1000	1500	μs
Switching Frequency	f_{SW_HV1}		1.89	2.1	2.31	MHz
Spread Spectrum Range	f_{SSP_HV1}		--	12	--	%
High-Side MOSFET On-Resistance	$R_{ON\_UG\_HV1}$		--	220	--	mΩ
Low-Side MOSFET On-Resistance	$R_{ON\_LG\_HV1}$		--	120	--	mΩ
Minimum On-Time	$t_{MIN\_ON\_HV1}$		--	--	40	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Off-Time	$t_{MIN\_OFF\_HV1}$		--	--	50	ns
Positive Inductor Peak Current Limit	$I_{CL\_PK\_HV1}$		1.9	2.5	3.1	A
Positive Inductor Valley Current Limit	$I_{CL\_VALLEY\_HV1}$		--	1.6	--	A
Negative Inductor Peak Current Limit	$I_{CL\_N\_PK\_HV1}$	HVBuck1 in FPWM	1.3	1.8	2.3	A
Output Discharge Resistor	R_{DIS_HV1}		20	50	80	Ω
HVBuck1 Output Undervoltage Falling Threshold Detection	V_{UVP_HV1}		--	80	--	%
HVBuck1 Output Undervoltage Falling Threshold Detection Accuracy	$V_{UVP\_ACC\_HV1}$		–1.3	--	1.3	%
HVBuck1 Output Overvoltage Rising Threshold Detection	V_{OVP_HV1}		--	110	--	%
HVBuck1 Output Overvoltage Rising Threshold Detection Accuracy	$V_{OVP\_ACC\_HV1}$		–1.3	--	1.3	%
CH2_LVBuck2						
Input Voltage Range	V_{IN_LV2}		2.7	--	5	V
Output Voltage Range	V_{OUT_LV2}		0.6	1.1	1.9	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV2\_FPWM}$	V_{OUT_LV2} = 0.6V to 1.9V, V_{IN_LV2} = 3.6V, I_{OUT_LV2} = 0A to 1.5A, FPWM	–1.5	--	1.5	%
Soft-Start Time	t_{SS_LV2}	Time for V_{OUT_LV2} to rise from 10% to 90% of the target value, no load	600	1200	1800	µs
Switching Frequency	f_{SW_LV2}		1.89	2.1	2.31	MHz
Spread Spectrum Range	f_{SSP_LV2}		--	12	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Side MOSFET On-Resistance	$R_{ON\_UG\_LV2}$		--	90	--	mΩ
Low-Side MOSFET On-Resistance	$R_{ON\_LG\_LV2}$		--	35	--	mΩ
Minimum On-Time	$t_{MIN\_ON\_LV2}$		--	--	44	ns
Positive Inductor Peak Current Limit	$I_{CL\_PK\_LV2}$		2.1	2.5	2.9	A
Positive Inductor Valley Current Limit	$I_{CL\_VALLEY\_LV2}$		--	1.8	--	A
Negative Inductor Peak Current Limit	$I_{CL\_N\_PK\_LV2}$	LVBuck2 in FPWM	0.7	1.7	2.9	A
Output Discharge Resistor	R_{DIS_LV2}		6	9	14	Ω
LVBuck2 Output Undervoltage Falling Threshold Detection	V_{UVP_LV2}		--	95	--	%
LVBuck2 Output Undervoltage Falling Threshold Detection Accuracy	$V_{UVP\_ACC\_LV2}$		–1.3	--	1.3	%
LVBuck2 Output Overvoltage Rising Threshold Detection	V_{OVP_LV2}		--	105	--	%
LVBuck2 Output Overvoltage Rising Threshold Detection Accuracy	$V_{OVP\_ACC\_LV2}$		–1.3	--	1.3	%
PVD23 Overvoltage Rising Protection	V_{OVP_PVD23}		5.35	5.8	6.25	V
PVD23 Overvoltage Hysteresis	$V_{OVP\_HYS\_PVD23}$		--	580	--	mV
CH3_LVBuck3						
Input Voltage Range	V_{IN_LV3}		2.7	--	5	V
Output Voltage Range	V_{OUT_LV3}		0.6	1.8	1.9	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy	$V_{OUT\_ACC\_LV3\_FPWM}$	V_{OUT_LV3} = 0.6V to 1.9V, V_{IN_LV3} = 3.6V, I_{OUT_LV3} = 0A to 1.5A, FPWM	–1.5	--	1.5	%
Soft-Start Time	t_{SS_LV3}	Time for V_{OUT_LV3} to rise from 10% to 90% of the target value, no load	600	1200	1800	μs
Switching Frequency	f_{SW_LV3}		1.89	2.1	2.31	MHz
Spread Spectrum Range	f_{SSP_LV3}		--	12	--	%
High-Side MOSFET On-Resistance	$R_{ON\_UG\_LV3}$		--	90	--	mΩ
Low-Side MOSFET On-Resistance	$R_{ON\_LG\_LV3}$		--	42	--	mΩ
Minimum On-Time	$t_{MIN\_ON\_LV3}$		--	--	44	ns
Positive Inductor Peak Current Limit	$I_{CL\_PK\_LV3}$		2.1	2.5	2.9	A
Positive Inductor Valley Current Limit	$I_{CL\_VALLEY\_LV3}$		--	1.8	--	A
Negative Inductor Peak Current Limit	$I_{CL\_N\_PK\_LV3}$	LVBuck3 in FPWM	0.7	1.7	2.9	A
Output Discharge Resistor	R_{DIS_LV3}		6	9	14	Ω
LVBuck3 Output Undervoltage Falling Threshold Detection	V_{UVP_LV3}		--	95	--	%
LVBuck3 Output Undervoltage Falling Threshold Detection Accuracy	$V_{UVP\_ACC\_LV3}$		–1.3	--	1.3	%
LVBuck3 Output Overvoltage Rising Threshold Detection	V_{OVP_LV3}		--	105	--	%
LVBuck3 Output Overvoltage Rising Threshold Detection Accuracy	$V_{OVP\_ACC\_LV3}$		–1.3	--	1.3	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PVD23 Overvoltage Rising Protection	V_{OVP_PVD23}		5.35	5.8	6.25	V
PVD23 Overvoltage Hysteresis	$V_{OVP\_HYS\_PVD23}$		--	580	--	mV
CH4_LDO1						
Input Voltage Range	V_{IN_LDO1}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO1}		1.8	3.3	3.5	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LDO1}$	V_{OUT_LDO1} = 1.8V to 3.5V, (V_{IN_LDO1} - V_{OUT_LDO1}) ≥ 0.3V, I_{OUT_LDO1} = 0mA to 300mA	–1.5	--	1.5	%
Soft-Start Time	t_{SS_LDO1}	Time for V_{OUT_LDO1} to rise from 10% to 90% of target value, no load	200	700	1100	µs
Dropout Voltage (Note 7)	$V_{DROP\_300\_LDO1}$	I_{OUT_LDO1} = 300mA	--	--	300	mV
	$V_{DROP\_150\_LDO1}$	I_{OUT_LDO1} = 150mA	--	--	150	
Maximum Output Current	$I_{OUT\_MAX\_LDO1}$		300	--	--	mA
Output Current Limit	I_{CL_LDO1}		345	450	555	mA
Output Discharge Resistor	R_{DIS_LDO1}		32	60	88	Ω
LDO1 Output Undervoltage Falling Threshold Detection	V_{UVP_LDO1}		--	95	--	%
LDO1 Output Undervoltage Falling Threshold Detection Accuracy	$V_{UVP\_ACC\_LDO1}$		–1.3	--	1.3	%
LDO1 Output Overvoltage Rising Threshold Detection	V_{OVP_LDO1}		--	105	--	%
LDO1 Output Overvoltage Rising Threshold Detection Accuracy	$V_{OVP\_ACC\_LDO1}$		–1.3	--	1.3	%
PVD45 Overvoltage Rising Protection	V_{OVP_PVD45}		5.35	5.8	6.25	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PVD45 Overvoltage Hysteresis	$V_{OVP\_HYS\_PVD45}$		--	500	--	mV
CH5_LDO2						
Input Voltage Range	V_{IN_LDO2}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO2}		1.8	1.8	3.3	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LDO2}$	V_{OUT_LDO2} = 1.8V to 3.5V, (V_{IN_LDO2} - V_{OUT_LDO2}) ≥ 0.4V, I_{OUT_LDO2} = 0mA to 400mA	–1.5	--	1.5	%
Soft-Start Time	t_{SS_LDO2}	Time for V_{OUT_LDO2} to rise from 10% to 90% of target value, no load	344	410	472	μs
Dropout Voltage (Note 7)	$V_{DROP\_400\_LDO2}$	I_{OUT_LDO2} = 400mA	--	--	400	mV
	$V_{DROP\_150\_LDO2}$	I_{OUT_LDO2} = 150mA	--	--	150	
Maximum Output Current	$I_{OUT\_MAX\_LDO2}$		400	--	--	mA
Output Current Limit	I_{CL_LDO2}		450	600	750	mA
Output Discharge Resistor	R_{DIS_LDO2}		32	60	88	Ω
LDO2 Output Undervoltage Falling Threshold Detection	V_{UVP_LDO2}		--	95	--	%
LDO2 Output Undervoltage Falling Threshold Detection Accuracy	$V_{UVP\_ACC\_LDO2}$		–1.3	--	1.3	%
LDO2 Output Overvoltage Rising Threshold Detection	V_{OVP_LDO2}		--	105	--	%
LDO2 Output Overvoltage Rising Threshold Detection Accuracy	$V_{OVP\_ACC\_LDO2}$		–1.3	--	1.3	%
PVD45 Overvoltage Rising Protection	V_{OVP_PVD45}		5.35	5.8	6.25	V
PVD45 Overvoltage Hysteresis	$V_{OVP\_HYS\_PVD45}$		--	500	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I/O Control						
SEQOUT Low-Level Output Voltage	V_{OL_SEQOUT}	The current into the SEQOUT pin is equal to 5mA	--	--	200	mV
SEQOUT Input Leakage Current	I_{LEAK_SEQOUT}	1.8V is applied on the SEQOUT pin	--	--	1	μA
PGOOD Low-Level Output Voltage	V_{OL_PGOOD}	The current into the PGOOD pin is equal to 5mA	--	--	200	mV
PGOOD Input Leakage Current	I_{LEAK_PGOOD}	1.8V applied on the PGOOD pin	--	--	1	μA
PGOOD Delay Time	t_{PGOOD_DLY}	Time interval between the completion of the soft-start process for the last channel and the subsequent assertion of the PGOOD signal	8.3	9.4	10.5	ms
EN Low-Level Input Voltage	V_{IL_EN}		--	--	0.4	V
EN High-Level Input Voltage	V_{IH_EN}		1.2	--	--	V
EN Pull-Down Current	I_{PD_EN}		1	--	11	μA
RESETIN Low-Level Input Voltage	$V_{IL\_RESETIN}$		--	--	0.4	V
RESETIN High-Level Input Voltage	$V_{IH\_RESETIN}$		1.2	--	--	V
RESETIN Pull-Down Resistance	$R_{PD\_RESETIN}$		--	300	--	kΩ
Safety I/O Control						
ERROUT Low-Level Output Voltage	V_{OL_ERROUT}	The current into ERROUT is equal to 5mA	--	--	200	mV
ERROUT Input Leakage Current	I_{LEAK_ERROUT}	1.8V is applied on the ERROUT pin	--	--	1	μA
ERRIN1/2 Low-Level Input Voltage	$V_{IL\_ERRIN1/2}$		--	--	0.4	V
ERRIN1/2 High-Level Input Voltage	$V_{IH\_ERRIN1/2}$		1.2	--	--	V
ERRIN1/2 Pull-Down Resistance	$R_{PD\_ERRIN1/2}$		--	300	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VMONIN						
VMONIN Monitor High-Voltage Range	V_{MONIN_H}	Default: 1.28V	0.938	0.96	0.982	V
			1.162	1.18	1.198	
			1.261	1.28	1.299	
			1.31	1.33	1.35	
VMONIN Monitor Low-Voltage Range	V_{MONIN_L}	Default: 1.14V	0.821	0.84	0.859	V
			1.005	1.02	1.035	
			1.123	1.14	1.157	
			1.075	1.09	1.106	

Note 6. PVCC is the pre-regulator output voltage only for internal circuitry. External loading on the PVCC pin is forbidden.

Note 7. Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100mV below its nominal value.

14.1 System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. ($T_A = T_J$ = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3}= 1.8V, V_{OUT_LDO1} = 3.3V, V_{OUT_LDO2} = 1.8V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Quiescent Current of VIN	I_{Q_ON}	EN = H, $V_{UVLO\_R} \leq V_{IN} \leq$ 24V, V_{OUT_HV1} ties to PVD23 and PVD45, all channels are ON, no load	--	20	--	mA
Quiescent Current of VIN	I_{Q_OFF}	EN = H, $V_{UVLO\_R} \leq V_{IN} \leq$ 24V, V_{OUT_HV1} ties to PVD23 and PVD45, all channels are OFF	--	3	--	mA
Over-Temperature Protection	T_{TSD}		--	170	--	°C
Over-Temperature Protection Hysteresis	T_{TSD_H}		--	20	--	°C
Over-Temperature Warning	T_{OTW}		--	130	--	°C
Over-Temperature Warning Hysteresis	T_{OTW_H}		--	20	--	°C
CH1_HVBuck1						
Maximum Output Current	$I_{OUT\_MAX\_HV1}$	Depends on the input voltage and the output voltage	1.5	--	--	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Transient	$V_{LOAD\_TRAN\_HV1\_FPWM}$	V_{OUT_HV1} = 3.6V, V_{IN_HV1} = 6V/9V/12V, I_{OUT_HV1} = 10mA to 0.5A to 10mA, 1μs, FPWM	–150	--	150	mV
Line Transient	$V_{LINE\_TRAN\_HV1\_FPWM}$	V_{OUT_HV1} = 3.6V, V_{IN_HV1} = 5V to 18.5V to 5V, 100μs, I_{OUT_HV1} = 0.5A, FPWM	–50	--	50	mV
Load Regulation	$V_{LOAD\_REG\_HV1}$	V_{OUT_HV1} = 3.6V, V_{IN_HV1} = 6V/9V/12V, ΔI_{OUT_HV1} = 1.5A, FPWM	--	--	0.15	%
Line Regulation	$V_{LINE\_REG\_HV1}$	V_{OUT_HV1} = 3.6V, V_{IN_HV1} = 5V to 18.5V, I_{OUT_HV1} = 1.5A	--	--	1	%
Output Ripple Voltage	$V_{RIPPLE\_HV1\_FPWM}$	Peak to peak in one switching cycle, FPWM, SSP_EN bit = 0	--	--	20	mVpp
CH2_LVBuck2						
Maximum Output Current	$I_{OUT\_MAX\_LV2}$		1.5	--	--	A
Load Transient	$V_{LOAD\_TRAN\_LV2\_FPWM}$	V_{OUT_LV2} = 1.1V, V_{IN_LV2} = 3.6V, I_{OUT_LV2} = 100mA to 0.5A to 100mA, 1μs, FPWM	–50	--	50	mV
Line Transient	$V_{LINE\_TRAN\_LV2\_FPWM}$	V_{OUT_LV2} = 1.1V, V_{IN_LV2} = 3V to 5V to 3V, 50μs, I_{OUT_LV2} = 10mA/0.75A/1.5A, FPWM	–50	--	50	mV
Load Regulation	$V_{LOAD\_REG\_LV2}$	V_{OUT_LV2} = 1.1V, V_{IN_LV2} = 3.6V, ΔI_{OUT_LV2} = 1.5A, FPWM	--	--	0.15	%
Line Regulation	$V_{LINE\_REG\_LV2}$	V_{OUT_LV2} = 1.1V, V_{IN_LV2} = 2.7V to 5V, I_{OUT_LV2} = 1.5A	--	--	1	%
Output Ripple Voltage	$V_{RIPPLE\_LV2\_FPWM}$	Peak to peak in one switching cycle, FPWM, SSP_EN bit = 0	--	10	15	mVpp
CH3_LVBuck3						
Maximum Output Current	$I_{OUT\_MAX\_LV3}$		1.5	--	--	A
Load Transient	$V_{LOAD\_TRAN\_LV3\_FPWM}$	V_{OUT_LV3} = 1.8V, V_{IN_LV3} = 3.6V, I_{OUT_LV3} = 100mA to 0.5A to 100mA, 1μs, FPWM	–50	--	50	mV
Line Transient	$V_{LINE\_TRAN\_LV3\_FPWM}$	V_{OUT_LV3} = 1.8V, V_{IN_LV3} = 3V to 5V to 3V, 50μs, I_{OUT_LV3} = 10mA/0.75A/1.5A, FPWM	–50	--	50	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Regulation	$V_{LOAD\_REG\_LV3}$	V_{OUT_LV3} = 1.8V, V_{IN_LV3} = 3.6V, ΔI_{OUT_LV3} = 1.5A, FPWM	--	--	0.15	%
Line Regulation	$V_{LINE\_REG\_LV3}$	V_{OUT_LV3} = 1.8V, V_{IN_LV3} = 2.7V to 5V, I_{OUT_LV3} = 1.5A	--	--	1	%
Output Ripple Voltage	$V_{RIPPLE\_LV3\_FPWM}$	Peak to peak in one switching cycle, FPWM, SSP_EN bit = 0	--	10	15	mVpp
CH4_LDO1						
Power Supply Rejection Ratio	PSRR_LDO1	V_{OUT_LDO1} = 3.3V, $V_{IN\_LDO1} \geq$ 3.6V, I_{OUT_LDO1} = 100mA, f = 100kHz Disturbing signal = 100mV	--	60	--	dB
		V_{OUT_LDO1} = 3.3V, $V_{IN\_LDO1} \geq$ 3.6V, I_{OUT_LDO1} = 100mA, f = 100kHz to 1MHz Disturbing signal = 100mV	--	40	--	dB
Load Transient	$V_{LOAD\_TRAN\_LDO1}$	V_{OUT_LDO1} = 3.3V, V_{IN_LDO1} = 3.6V, I_{OUT_LDO1} = 10mA to 0.2A to 10mA, 1μs, C_{O_LDO1} = 2.2μF	–25	--	25	mV
Line Transient	$V_{LINE\_TRAN\_LDO1}$	V_{OUT_LDO1} = 3.3V, V_{IN_LDO1} step 600mV, 10μs, the LDO1 is not in dropout condition, I_{OUT_LDO1} = 1mA/ 0.3A	–25	--	25	mV
CH5_LDO2						
Power Supply Rejection Ratio	PSRR_LDO2	V_{OUT_LDO2} = 3.3V, $V_{IN\_LDO2} \geq$ 3.7V, I_{OUT_LDO2} = 100mA, f = 100kHz Disturbing signal = 100mV	--	20	--	dB
		V_{OUT_LDO2} = 3.3V, $V_{IN\_LDO2} \geq$ 3.7V, I_{OUT_LDO2} = 100mA, f = 100kHz to 1MHz Disturbing signal = 100mV	--	15	--	dB
Load Transient	$V_{LOAD\_TRAN\_LDO2}$	V_{OUT_LDO2} = 1.8V, V_{IN_LDO2} = 3.6V, I_{OUT_LDO2} = 10mA to 0.2A to 10mA, 1μs, C_{O_LDO2} = 2.2μF	–50	--	50	mV
Line Transient	$V_{LINE\_TRAN\_LDO2}$	V_{OUT_LDO2} = 1.8V, V_{IN_LDO2} step 600mV, 10μs, the LDO2 is not in dropout condition, I_{OUT_LDO2} = 1mA/ 0.4A	–25	--	25	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C						
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.2	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{SCL}		--	--	1000	kHz
(Repeated) Start Hold Time	$t_{HD;STA}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	0.26	--	--	µs
SCL Clock Low Time	t_{LOW}		0.5	--	--	µs
SCL Clock High Time	t_{HIGH}		0.26	--	--	µs
(Repeated) Start Setup Time	$t_{SU;STA}$	Set-up time for a repeated START condition	0.26	--	--	µs
SDA Data Hold Time	$t_{HD;DAT}$		0	--	--	ns
SDA Set-Up Time	$t_{SU;DAT}$		50	--	--	ns
STOP Condition Setup Time	$t_{SU;STO}$		0.26	--	--	µs
Bus Free Time between Stop and Start Condition	t_{BUF}		0.5	--	--	µs
Rising Time of Both SDA and SCL Signals	t_R		--	--	120	ns
Falling Time of Both SDA and SCL Signals	t_F		--	--	120	ns
SDA Output Low Sink Current	I_{OL_I2C}	SDA voltage = 0.4V	2	--	--	mA
SDA Valid Acknowledge Time	$t_{VD;ACK}$		--	--	0.45	µs
I/O Time Deglitch						
EN Rising Deglitch Time	$t_{EN\_R\_DEG}$		--	5	--	µs
EN Falling Deglitch Time	$t_{EN\_F\_DEG}$		--	50	--	µs

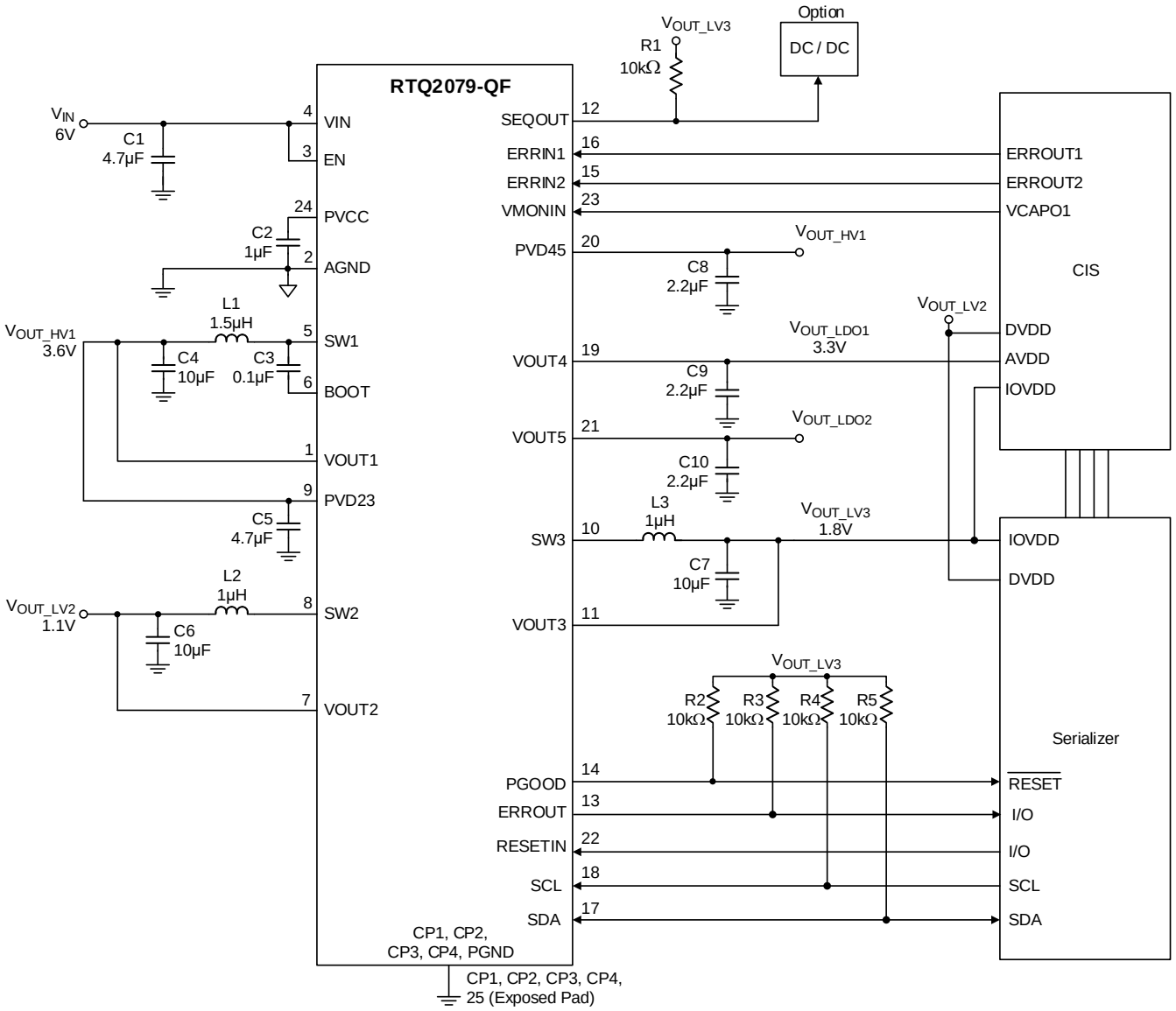
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RESETIN Detection Delay Time	$t_{RESETIN\_DET\_DLY}$	Delay time starts detecting RESETIN after PGOOD normal state is ready	--	100	--	µs
RSETIN Rising Deglitch Time	$t_{RSETIN\_R\_DEG}$		--	50	--	µs
RSETIN Falling Deglitch Time	$t_{RSETIN\_F\_DEG}$		--	5	--	µs
Safety I/O Time Deglitch						
ERRIN1/2 Detection Delay Time	$t_{ERRIN1/2\_DET\_DLY}$	Delay time starts detecting ERRIN1/2 after PGOOD normal state is ready	--	100	--	µs
ERRIN1/2 Rising Deglitch Time	$t_{ERRIN1/2\_R\_DEG}$		--	50	--	µs
ERRIN1/2 Falling Deglitch Time	$t_{ERRIN1/2\_F\_DEG}$		--	50	--	µs
VMONIN Time Deglitch						
VMONIN Monitor Voltage Detection Delay Time	$t_{VMONIN\_DET\_DLY}$	Delay time starts detecting VMONIN after PGOOD normal state is ready	--	100	--	µs
VMONIN Monitor Voltage Deglitch Time	t_{VMONIN_DEG}		--	50	--	µs
Protection Time Deglitch						
HVBuck1 Output UVP Deglitch Time	$t_{UVP\_DEG\_HV1}$		--	50	--	µs
LVBuck2 Output UVP Deglitch Time	$t_{UVP\_DEG\_LV2}$		--	50	--	µs
LVBuck3 Output UVP Deglitch Time	$t_{UVP\_DEG\_LV3}$		--	50	--	µs
LDO1 Output UVP Deglitch Time	$t_{UVP\_DEG\_LDO1}$		--	50	--	µs
LDO2 Output UVP Deglitch Time	$t_{UVP\_DEG\_LDO2}$		--	50	--	µs
HVBuck1 Output OVP Deglitch Time	$t_{OVP\_DEG\_HV1}$		--	50	--	µs
LVBuck2 Output OVP Deglitch Time	$t_{OVP\_DEG\_LV2}$		--	50	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LVBuck3 Output OVP Deglitch Time	$t_{OVP\_DEG\_LV3}$		--	50	--	μs
LDO1 Output OVP Deglitch Time	$t_{OVP\_DEG\_LDO1}$		--	50	--	μs
LDO2 Output OVP Deglitch Time	$t_{OVP\_DEG\_LDO2}$		--	50	--	μs
PVD23 OVP Rising Deglitch Time	$t_{OVP\_R\_DEG\_PVD23}$	ΔV = 700mV	--	5	6	μs
PVD23 OVP Falling Deglitch Time	$t_{OVP\_F\_DEG\_PVD23}$	ΔV = 700mV	--	5	6	μs
PVD45 OVP Rising Deglitch Time	$t_{OVP\_R\_DEG\_PVD45}$		--	5	--	μs
PVD45 OVP Falling Deglitch Time	$t_{OVP\_F\_DEG\_PVD45}$		--	5	--	μs
HVBuck1 OCP Deglitch Time	$t_{OCP\_DEG\_HV1}$		--	1	--	ms
LVBuck2 OCP Deglitch Time	$t_{OCP\_DEG\_LV2}$		--	1	--	ms
LVBuck3 OCP Deglitch Time	$t_{OCP\_DEG\_LV3}$		--	1	--	ms
LDO1 OCP Deglitch Time	$t_{OCP\_DEG\_LDO1}$		--	1	--	ms
LDO2 OCP Deglitch Time	$t_{OCP\_DEG\_LDO2}$		--	1	--	ms
Component Constraint						
Effective Output Inductance	L_{HV1}		1	1.5	2	μH
	L_{LV2}		0.68	1	1.2	
	L_{LV3}		0.68	1	1.2	
Effective Boot Capacitance	C_{BOOT}		0.07	0.1	0.13	μF
Effective PVCC Capacitance	C_{PVCC}		0.3	1	1.4	μF
Effective Input Capacitance	C_{IN_HV1}		1.5	4.7	10	μF
	C_{IN_PVD23}		1.5	4.7	10	
	C_{IN_PVD45}		0.7	2.2	4	

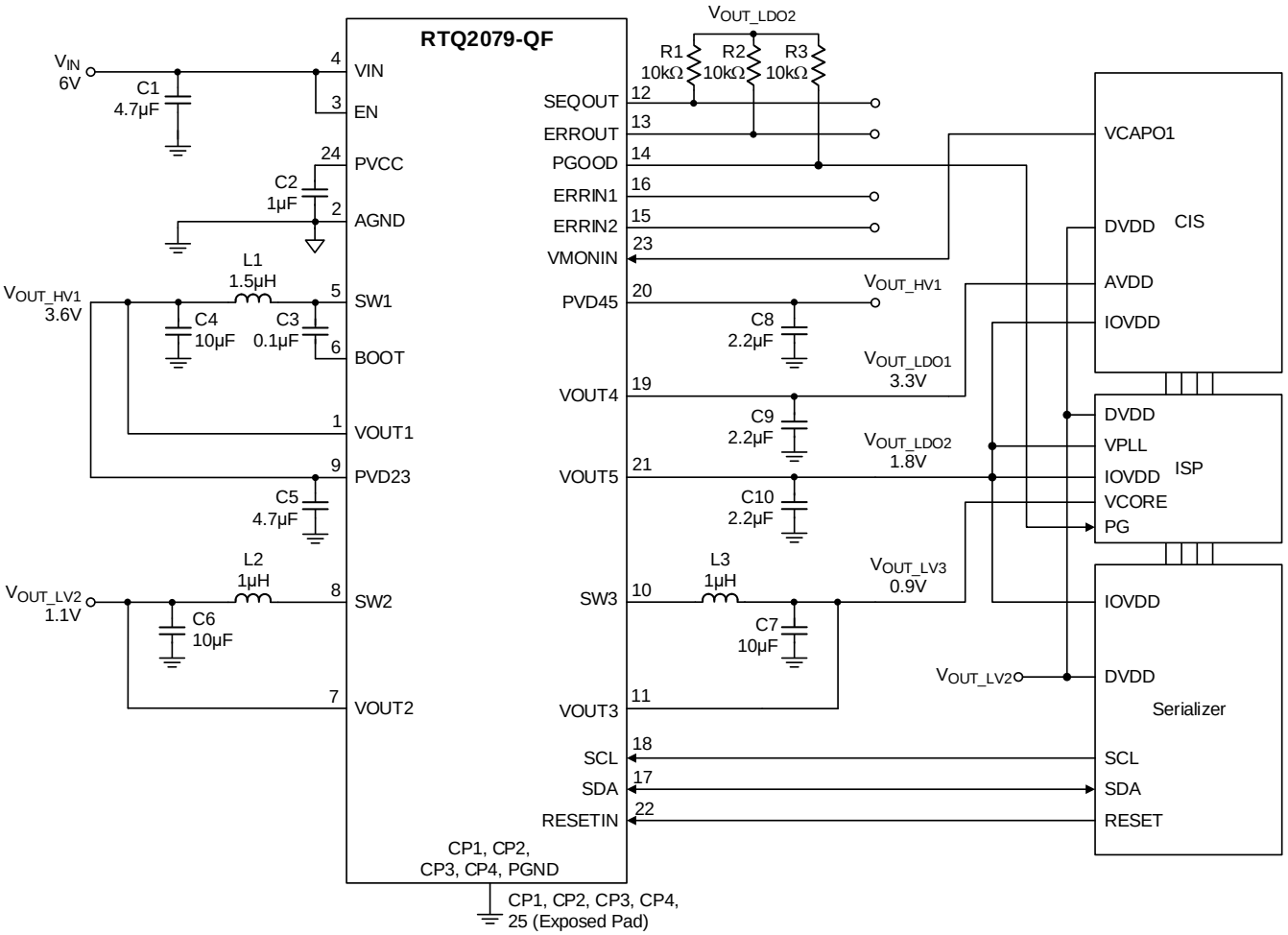
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Effective Output Capacitance	C_{O_HV1}		3.3	10	14	μF
	C_{O_LV2}		4.5	10	14	
	C_{O_LV3}		4.5	10	14	
	C_{O_LDO1}		0.7	2.2	33	
	C_{O_LDO2}		0.7	2.2	22	
Output Capacitance ESR for HVBuck1, LVBuck2, LVBuck3, LDO1, and LDO2	C_{O_ESR}		--	10	20	mΩ

15 Typical Application Circuit

15.1 General CIS Application



15.2 General CIS with ISP Application



15.3 General CIS Application with Battery Input

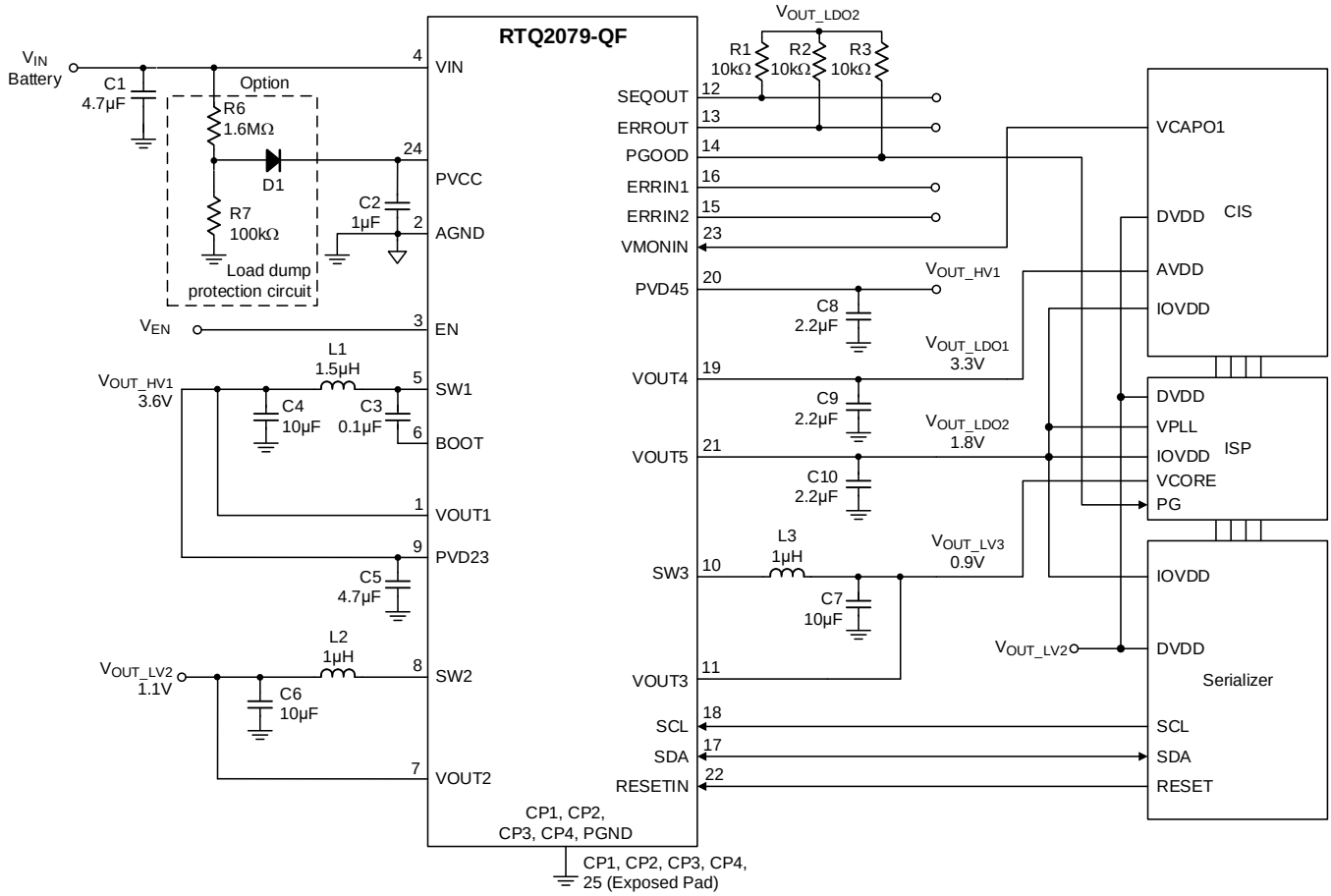


Table 1. Recommended Component List for Evaluation Board

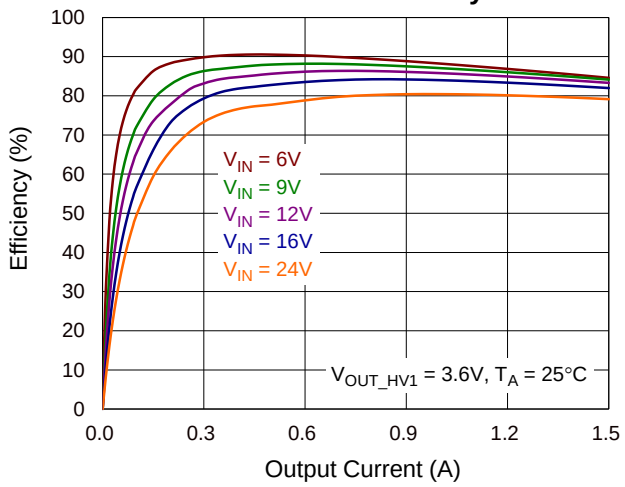
Reference	Qty	Part Number	Description	Package	Manufacturer
C1	1	GCJ31CC71H475KA01	4.7μF/50V/X7S	1206	MURATA
C2	1	GRT155C81A105KE01	1μF/10V/X6S	0402	MURATA
C3	1	GRT155R71C104KE01	0.1μF/16V/X7R	0402	MURATA
C4, C6, C7	1	GRT188C81A106ME13	10μF/10V/X6S	0603	MURATA
C5	1	GRT188C81C475KE13	4.7μF/16V/X6S	0603	MURATA
C8, C9, C10	1	GRT155C81A225KE13	2.2μF/10V/X6S	0402	MURATA
L1	1	TFM201610ALMA1R5MTAA	1.5μH/3.1A/85mΩ	0806	TDK
L2, L3	1	TFM201610ALMA1R0MTAA	1μH/3.7A/50mΩ	0806	TDK
R1, R2, R3, R4, R5	1	MR02X1002FAL	10kΩ/1%	0201	WALSIN

Table 2. Recommended Component List for Load Dump Protection Circuit

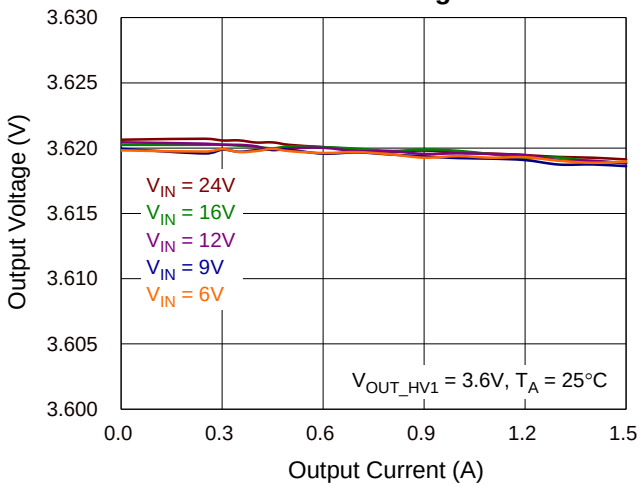
Reference	Qty	Part Number	Description	Package	Manufacturer
R6	1	MR04W1604FTL	1.6MΩ/1%	0402	WALSIN
R7	1	MR04X1003FTL	100kΩ/1%	0402	WALSIN
D1	1	BAS316	Diode	SOD323	NEXPERIA

16 Typical Operating Characteristics

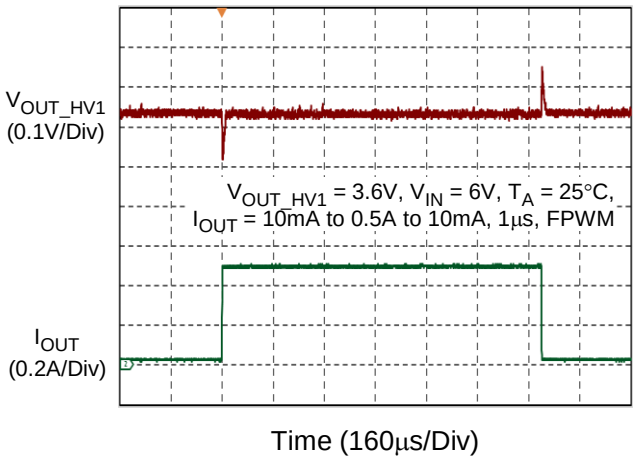
HVBuck1 Efficiency



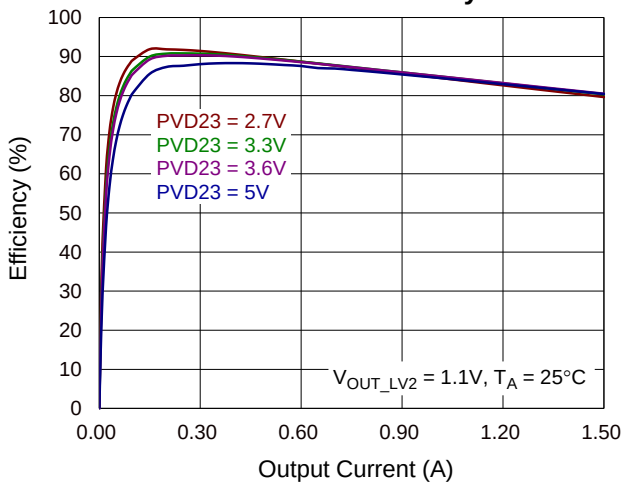
HVBuck1 Load Regulation



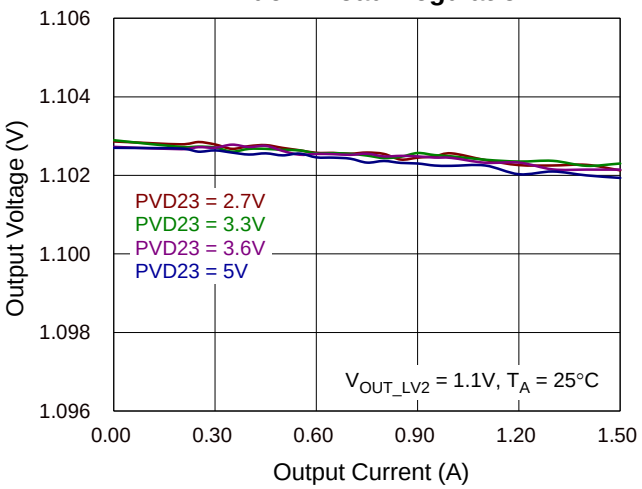
HVBuck1 Load Transient



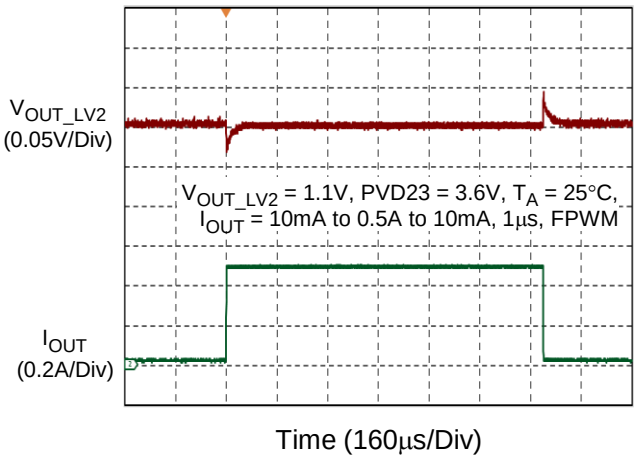
LVBuck2 Efficiency



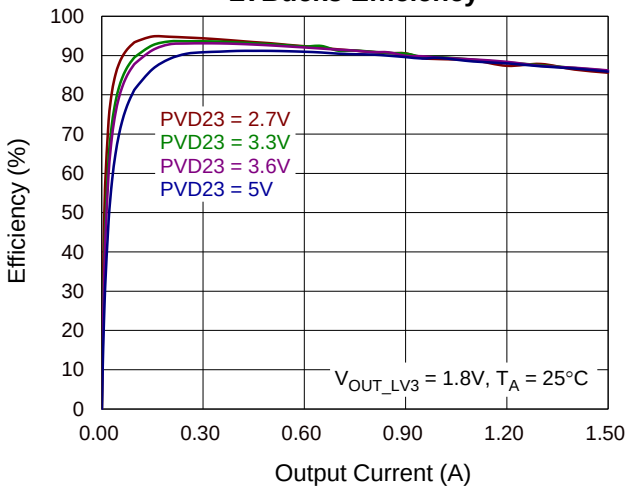
LVBuck2 Load Regulation



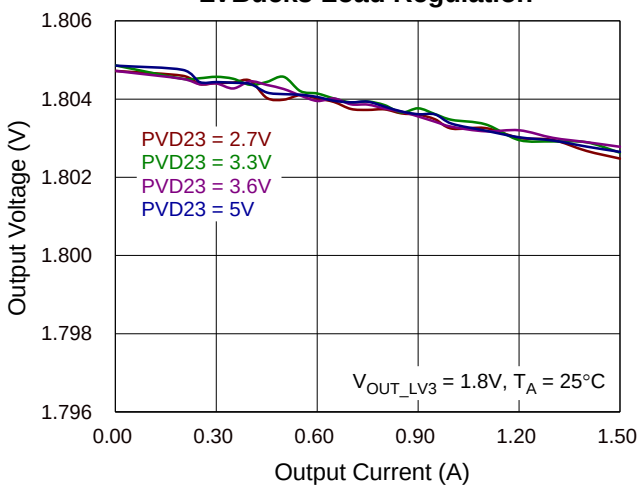
LVBuck2 Load Transient



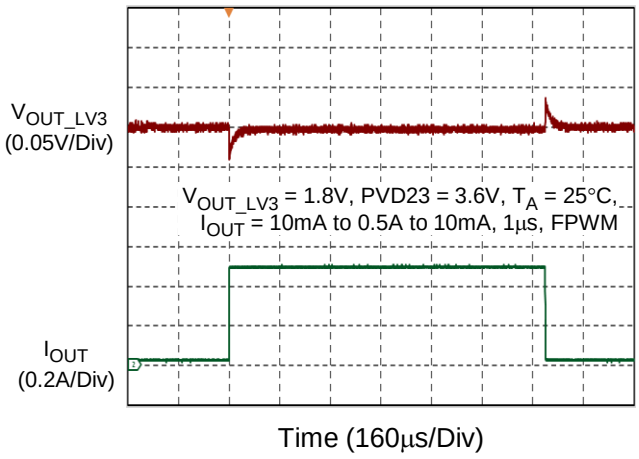
LVBuck3 Efficiency



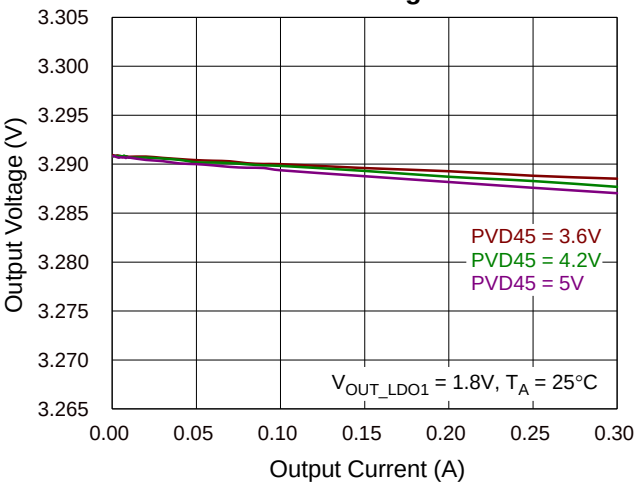
LVBuck3 Load Regulation



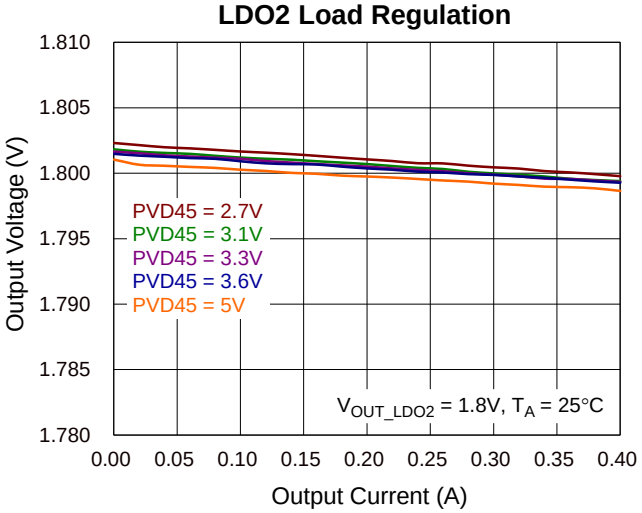
LVBuck3 Load Transient



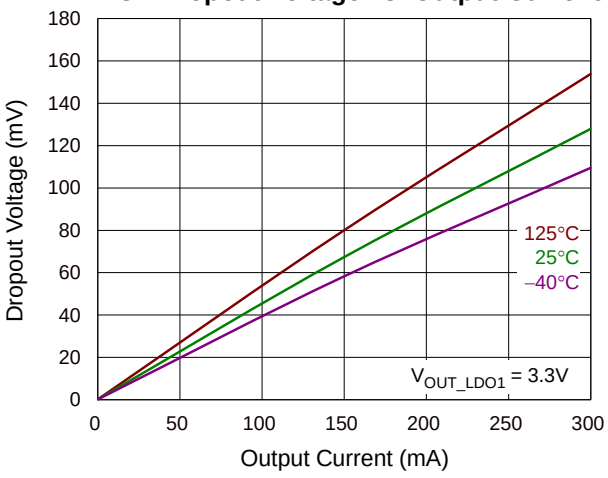
LDO1 Load Regulation



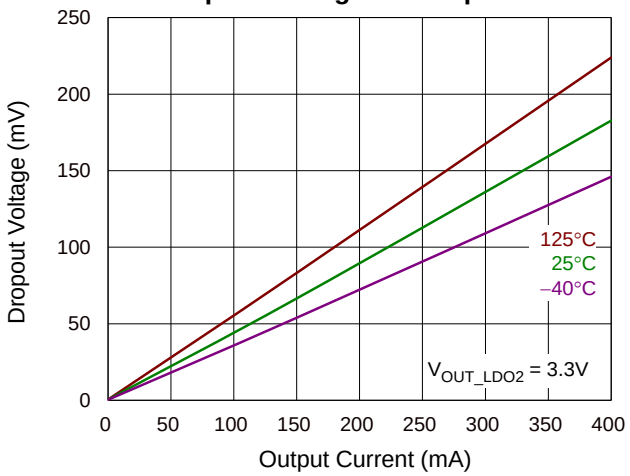
LDO2 Load Regulation



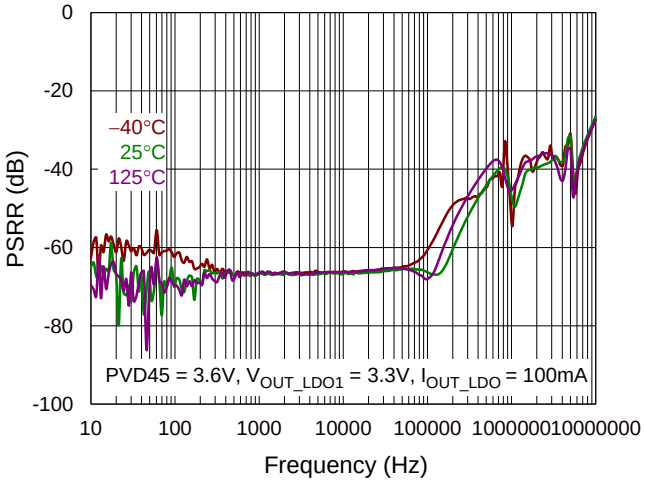
LDO1 Dropout Voltage vs. Output Current



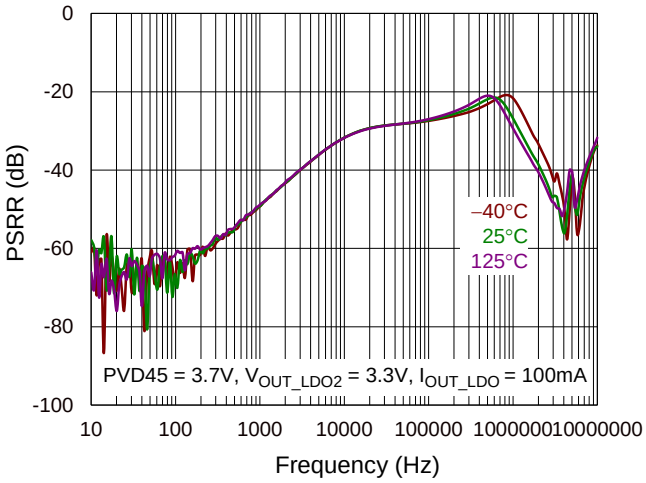
LDO2 Dropout Voltage vs. Output Current



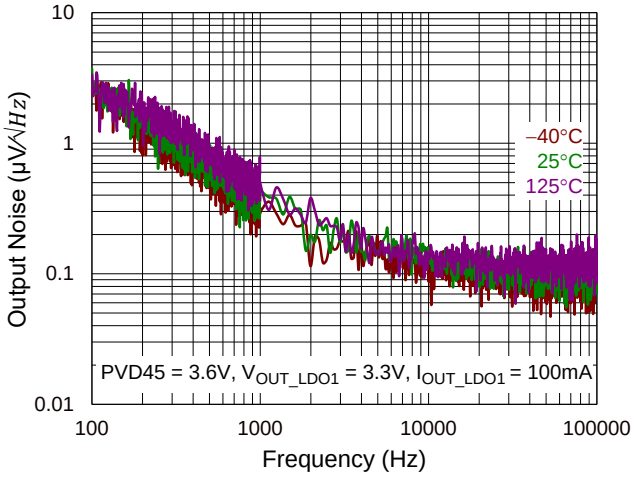
LDO1 PSRR



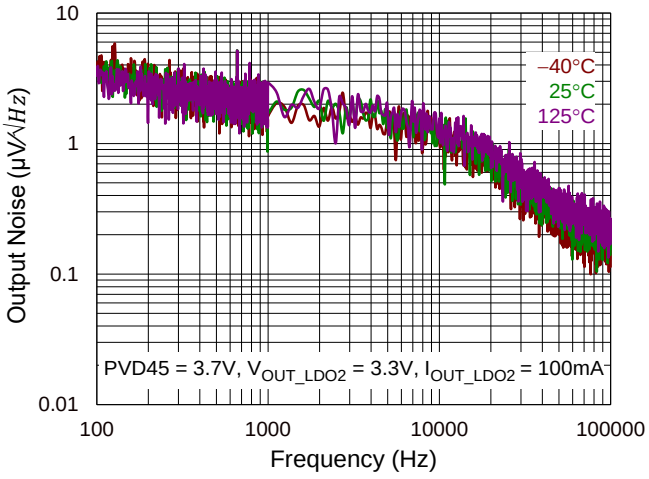
LDO2 PSRR



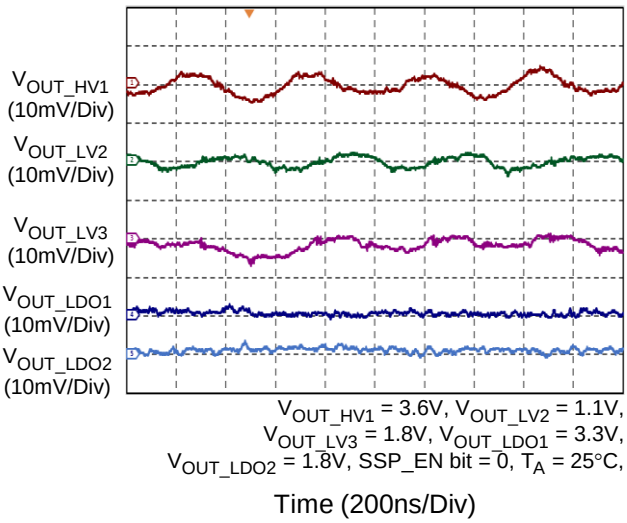
LDO1 Output Noise



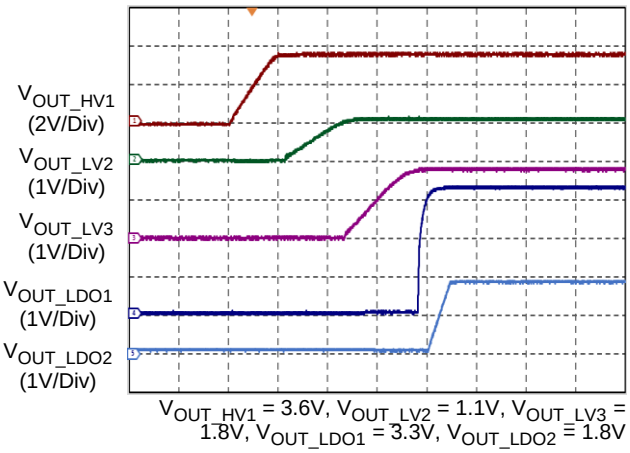
LDO2 Output Noise



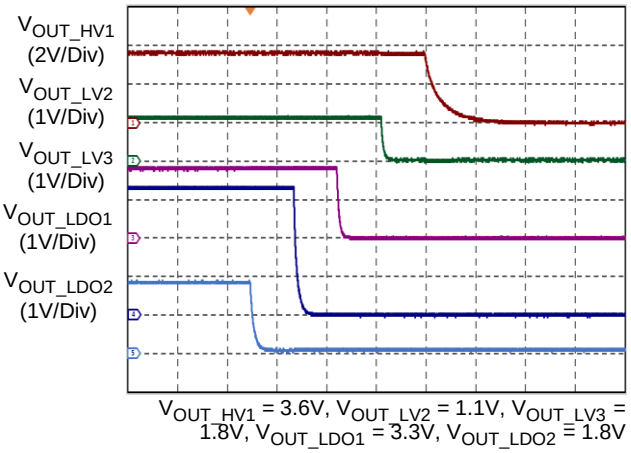
Output Voltage Ripple (Full Load)



SEQ4 Power-On



SEQ4 Power-Off



17 Operation

The RTQ2079-QF is a highly integrated power management integrated circuit (PMIC) for automotive camera system. It includes three step-down converters (HVBuck1, LVBuck2, and LVBuck3) and two generic LDOs (LDO1 and LDO2).

17.1 System Undervoltage and Overvoltage Protection

The RTQ2079-QF disables all channels if the V_{IN} voltage falls below the undervoltage-lockout level (V_{UVLO_F}) and the duration time is longer than 32μs. The device initializes in its default state after the V_{IN} voltage recovers from V_{UVLO_R}.

When the V_{IN} voltage reaches the overvoltage protection level ($V_{OVP\_R\_VIN}$), the step-down converters, LDOs, and SEQOUT are disabled immediately. Then the IC enters the “Regulator-Off” state and PGOOD and ERROUT changes from "H" to "L" to indicate the IC is in a fault status. When V_{IN} falls below 19.5V and the duration time is longer than 5μs, then the RTQ2079-QF resumes operation automatically.

17.2 Over-Temperature Protection

The RTQ2079-QF features over-temperature warning (OTW) and over-temperature protection (TSD). When the junction temperature exceeds the typical value of 130°C, the OTW function is activated, and the ERROUT status changes from "H" to "L" state for indication, but all outputs continue to operate. When the junction temperature exceeds the typical value of 170°C, the TSD function is activated, resulting in the disabling all outputs and the device enters the "Regulator-Off" state. Meanwhile, the PGOOD status also changes from "H" to "L" state to indicate the IC is in a fault status. The RTQ2079-QF will automatically resume normal operation once the junction temperature falls below the TSD threshold with a 20°C hysteresis band.

17.3 Pre-Regulator

The device integrates a 4.58V linear regulator (PVCC) supplied by V_{IN} to provide power to the internal circuitry. The PVCC is “NOT” allowed to power any other device or circuitry. A 1μF decoupling capacitor must be connected between PVCC and AGND to filter the noise, and it needs to be placed as close as possible to the PVCC pin.

17.4 Peak Current Mode Control

The three step-down converters utilize peak current mode control. At the beginning of each clock cycle, the internal high-side MOSFET turns on, allowing the current to ramp up in the inductor. By comparing the inductor peak current signal with the internal compensation signal derived from the feedback voltage, the turn-on time of high-side and low-side MOSFETs in every switching cycle are determined. In other words, the inductor current is used to control the duty-cycle and output voltage regulation of the converter.

17.5 Spread Spectrum Operation

Due to the periodicity of the switching signal, energy tends to concentrate at the fundamental frequency and its N-order harmonics. This concentration of energy can result in radiation that may cause the EMI issues. To address this, the RTQ2079-QF is equipped with a spread spectrum function designed to reduce EMI and ensure compliance with automotive EMC standards (CISPR 25). The spread spectrum function employs a pseudo-random sequence to modulate the switching frequency, allowing it to vary randomly within a range of 0% to 12%. For example, with a 2.1MHz typical switching frequency, the actual frequency will randomly oscillate between 2.1MHz and 2.352MHz. As a result, the RTQ2079-QF effectively prevents the switching frequency from interfering with the 1.8MHz AM band, which is a critical requirement of CISPR 25.

17.6 Phase-Shift Operation

The RTQ2079-QF supports phase-shift operation to prevent all step-down converters from switching simultaneously, further reducing the radiation quantity of energy. The phase-shift difference in the clock between each step-down converter automatically changes based on the numbers of enabled channels. For example, when two step-down converters are in use, the initial turn-on time between two high-side MOSFETs has a 180-degree phase difference. Likewise, there is a 120-degree phase difference when three step-down converters are in use.

17.7 Channel Floating Allowable

To save PCB layout space and reduce material costs, the unused low-voltage step-down converters (CH2/CH3) can be left with floating pins, eliminating the need of inductors and output capacitors. The RTQ2079-QF automatically detects the pin status during the power-on procedure to determine whether the channel is used or not. After that, any malfunction in an unused channel will not impact the device operation.

17.8 Reboot Operation

If the register bit 0x00[1] is set to 1, the device will disable all channels upon detecting a fault event. It will then exit the Fail-Safe state and reboot, while preserve the record of the fault event. Conversely, if the register bit at 0x00[1] is set to 0, the IC remains in the Fail-Safe state.

17.9 Power-Good Indication

The RTQ2079-QF features an open-drain output pin named PGOOD (Power-Good) to indicate the output voltage status of all channels. Connect a pull-up resistor from the PGOOD pin to an external voltage. When the last channel in the power-on sequence reaches 90% of its target output voltage, the PGOOD signal will be pulled high to indicate a "Power-Good" status after a 10ms delay.

Table 3. Unused Channel Pin Connection

Unused Channel	Unused Pin Number	Unused Pin Name	Pin Configuration
LVBuck2	7	VOUT2	Floating
	8	SW2	Floating
	9	PVD23	Connect to a fixed stable voltage
LVBuck3	9	PVD23	Connect to a fixed stable voltage
	10	SW3	Floating
	11	VOUT3	Floating
LDO1	19	VOUT4	Floating with minimum effective output capacitance
	20	PVD45	Connect to a fixed stable voltage
LDO2	20	PVD45	Connect to a fixed stable voltage
	21	VOUT5	Floating with minimum effective output capacitance
ERROUT	13	ERROUT	Connect to a fixed stable voltage via pull-up resistor
PGOOD	14	PGOOD	Floating

Unused Channel	Unused Pin Number	Unused Pin Name	Pin Configuration
ERRIN1	16	ERRIN1	• Floating (0x0E[3] = 0) • Connect to ground (0x0E[3] = 1, 0x0E[1] = 1) • Connect to a fixed stable voltage (0x0E[3] = 1, 0x0E[1] = 0)
ERRIN2	15	ERRIN2	• Floating (0x0E[2] = 0) • Connect to ground (0x0E[2] = 1, 0x0E[0] = 1) • Connect to a fixed stable voltage (0x0E[2] = 1, 0x0E[0] = 0)
I^2C	17	SDA	Connect to ground
	18	SCL	Connect to ground
RESETIN	22	RESETIN	Connect to ground
VMONIN	23	VMONIN	Floating (0x0C[4] = 0)

18 Application Information

(Note 8)

18.1 Load Dump Protection

In automotive systems, a load dump event is triggered when the alternator is charging the battery and the battery connection is suddenly removed. The RTQ2079-QF is capable of sustaining a 36V load dump. By paralleling additional voltage-dividing resistors to PVCC at the input, it is ensured that when EN is set to low, all output rails are turned off.

18.2 Device and Channel Enable Control

There is a hardware enable pin, EN, to control the RTQ2079-QF. When the supply voltage V_{IN} reaches the power-on reset level of 2.7V (typical) and EN is in a high state, the device is enabled and ready to receive I^2C commands for configuration. When V_{IN} rises above the UVLO rising voltage and the SEQ_CTRL register at 0x00[0] is set to 1, the power-on sequence starts. The channels are sequenced to power off if the EN state changes to low or the SEQ_CTRL register at 0x00[0] is set to 0. All channels shut down immediately without any sequence once V_{IN} falls below the UVLO falling voltage.

18.3 Device Register Configuration Control

Write access to the registers or bits marked as "CFG_LOCK (Configured Lock)" is restricted via the TM_PASS_CODE registers at 0x20 and 0x21. Before the configuration of the registers can be changed, the correct password must be written to enter guest mode to unlock the control registers. To exit guest mode and lock the control registers, thereby preventing unexpected operations, an incorrect password must be entered once changes are finalized.

18.4 Device State Machine

There are seven main states listed in the Table 4.

Table 4. Device State

State	Description	Entry	Exit
Power-Off	The device is in non-operation state.	• $V_{IN} \leq$ 2.5V (typical) From Regulator-Off • EN = L	• $V_{IN} \geq$ 2.7V (typical) AND EN = H
Regulator-Off	The device loads the OTP default setting and passes the OTP CRC checksum value comparison. All channels remains disabled, and the PGOOD/ERROUT signals are driven to a low state.	From Power-Off • Pass OTP CRC checksum value comparison From Standby/Power-On • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • Fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD) • RESET behavior (RESETIN, RESET bit) From Active/Alarm • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • Fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD)	To Power-Off • $V_{IN} \leq$ 2.5V (typical) • EN = L To BIST • $V_{IN} \geq V_{UVLO\_R}$, EN = H and no fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD).

State	Description	Entry	Exit
		• RESET behavior (RESETIN, RESET bit) • SEQ_CTRL_bit 0x00[0] = 0 From Fail-Safe • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • RESET behavior (RESETIN, RESET bit) • REBOOT_ACT 0x00[1] = 1	
Standby	The device passes the built-in self-test (BIST) and waits for an I^2C command to enable all channels.	BIST pass	To Regulator-Off • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • Fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD) To Power-On • SEQ_CTRL 0x00[0] = 1 and no RESET behavior (RESETIN, RESET bit)
Power-On	Channel power-on procedure starts.	From Standby SEQ_CTRL 0x00[0] = 1 and no RESET behavior (RESETIN, RESET bit)	To Regulator-Off • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • Fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD) To Active • The output voltages of all enable channels rise to 90% of the target values To Fail-Safe • Fault event (CH V_O UVP, CH V_O OVP) if the register 0x0F = 1Fh, 0x10 = 1Fh • Fault event (CH OCP)

State	Description	Entry	Exit
Active	The output voltages of all enabled channels rise to 90% of their target values. The PGOOD and ERROUT signals change to a high state to indicate the power status and any fault events. The ERRIN1, ERRIN2, VMONIN, and RESEIN functions are activated after the PGOOD signal changes to a high state.	From Power-On The output voltages of all enabled channels rise to 90% of the target values. From Alarm • All fault registers (0x11 to 0x15) event = 0	To Regulator-Off • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • Fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD) • RESET behavior (RESETIN, RESET bit) • SEQ_CTRL 0x00[0] = 0 To Alarm • Fault event (CH V_O UVP, CH V_O OVP) if register 0x0F = 00h, 0x10 = 00h • Fault event (ERRIN1, ERRIN2, V_{MON} UVP, V_{MON} OVP) • Fault event (OTW) • Any fault register (0x11 to 0x15, except 0x12[6]) event = 1 To Fail-Safe • Fault event (CH V_O UVP, CH V_O OVP) if register 0x0F = 1Fh, 0x10 = 1Fh • Fault event (CH OCP)
Alarm	When a fault event is detected but the channel is not turned off, the PGOOD signal remains in a high state, and ERROUT changes to a low state as a warning.	From Active • Fault event (CH V_O UVP, CH V_O OVP) if register 0x0F = 00h, 0x10 = 00h • Fault event (ERRIN1, ERRIN2, V_{MON} UVP, V_{MON} OVP) • Fault event (OTW) • Any fault register (0x11 to 0x15, except 0x12[6]) event = 1	To Regulator-Off • EN = L • $V_{IN} \leq V_{UVLO\_F}$ • Fault event (V_{IN} OVP, V_{PVD23} OVP, V_{PVD45} OVP, TSD) • RESET behavior (RESETIN, RESET bit) • SEQ_CTRL 0x00[0] = 0 To Active • All fault registers (0x11 to 0x15) event = 0 To Fail-Safe • Fault event (CH VO UVP, CH VO OVP) if register 0x0F = 1Fh, 0x10 = 1Fh • Fault event (CH OCP)

State	Description	Entry	Exit
Fail-Safe	When a fault event is detected and all channels are turned off, the PGOOD signal changes to a low state to indicate the power status. The ERROUT signal also changes to a low state to indicate a fault has been detected.	• BIST failure • Fault event (CH V_O UVP, CH V_O OVP) if register 0x0F = 1Fh, 0x10 = 1Fh • Fault event (CH OCP)	To Regulator-Off • $V_{IN} \leq V_{UVLO\_F}$ • EN = L • RESET behavior (RESETIN, RESET bit) • REBOOT_ACT 0x00[1] = 1

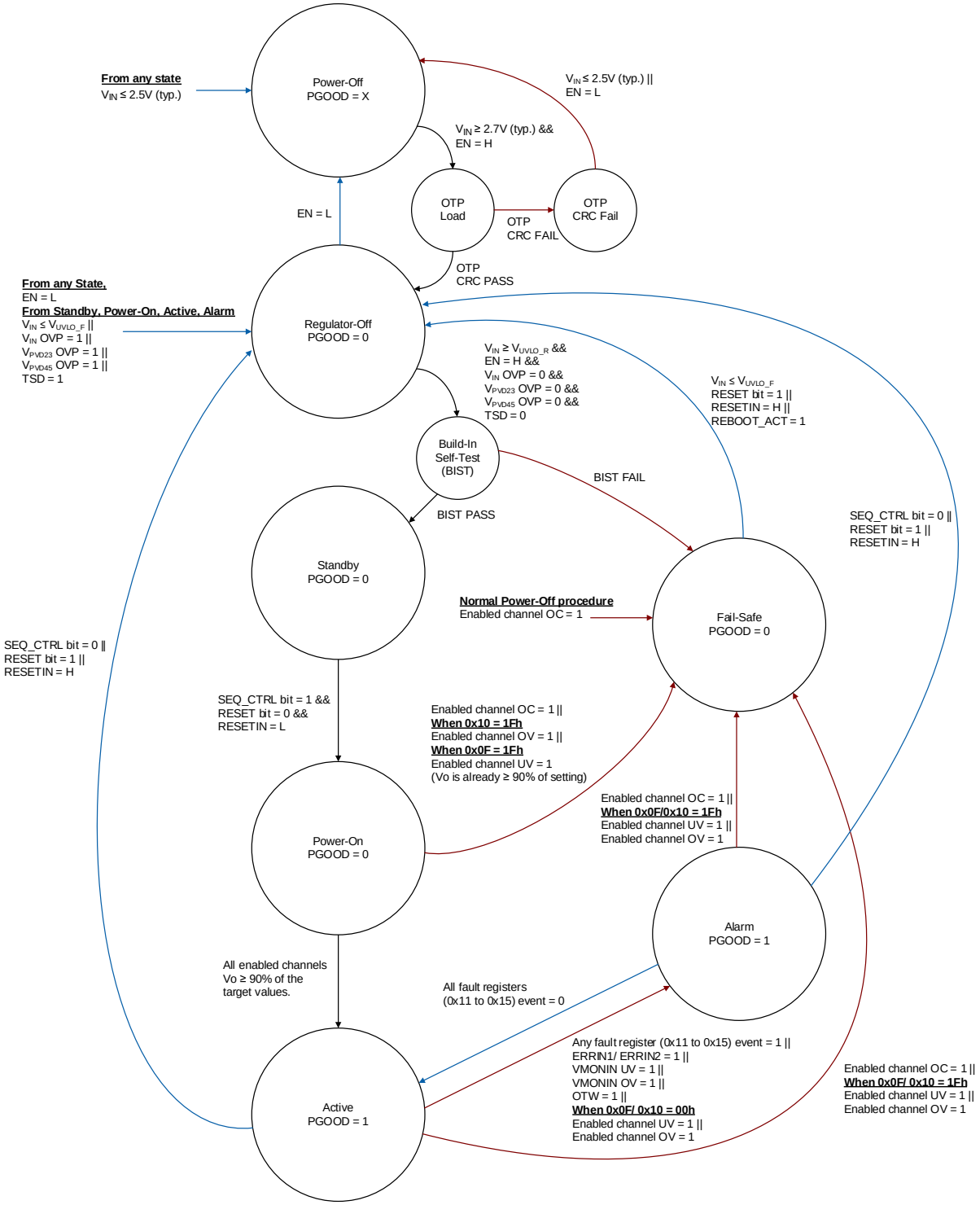


Figure 1. State Diagram

18.5 Power Sequence and Interval Time Setting

The RTQ2079-QF supports eight power-on sequences, as shown in Table 5. Only when the SEQ_CTRL register at 0x00[0] is set to 0, the power sequence register at 0x02[2:0] and the interval time register at 0x02[6:3] between adjacent channels can be configured by I^2C. The new settings will be applied at the next power-up. The RTQ2079-QF is also equipped with the OTP36 register at 0xE4[6:0] to provide One-Time Programmable (OTP) settings of the power sequence and interval time to establish factory default settings.

Table 5. Power-On Sequence

SEQ No.	Sequence					
SEQ0	CH1	CH2	CH3	CH4	SEQOUT	
SEQ1	CH1	CH4	CH3	CH2	SEQOUT	
SEQ2	CH1	CH4	SEQOUT	CH3	CH2	
SEQ3	CH1	CH2, CH3, CH4, SEQOUT				
SEQ4	CH1	CH2	CH3	CH4	CH5	SEQOUT
SEQ5	CH1	CH4	CH3	CH5	CH2	SEQOUT
SEQ6	CH1	CH4	SEQOUT	CH5	CH2	CH3
SEQ7	CH1	CH4	SEQOUT	CH3	CH2	CH5

18.6 Power-On/Off Control

There are methods using V_{UVLO}, the EN pin, the SEQ_CERT register bit at 0x00[0] or the RESETIN pin to flexibly control the RTQ2079-QF power sequence for different requirements and applications. The power-off sequence is the reverse order of the power-on sequence.

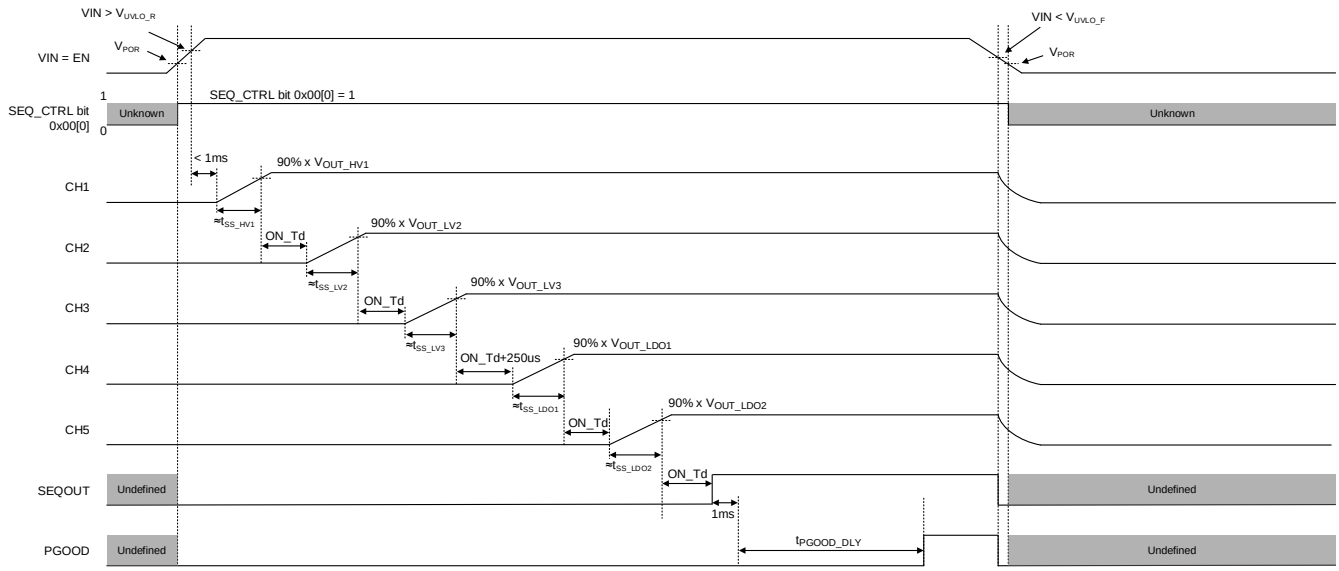


Figure 2. Example of SEQ4 Power Sequence Triggered by V_{UVLO} (VIN = EN)

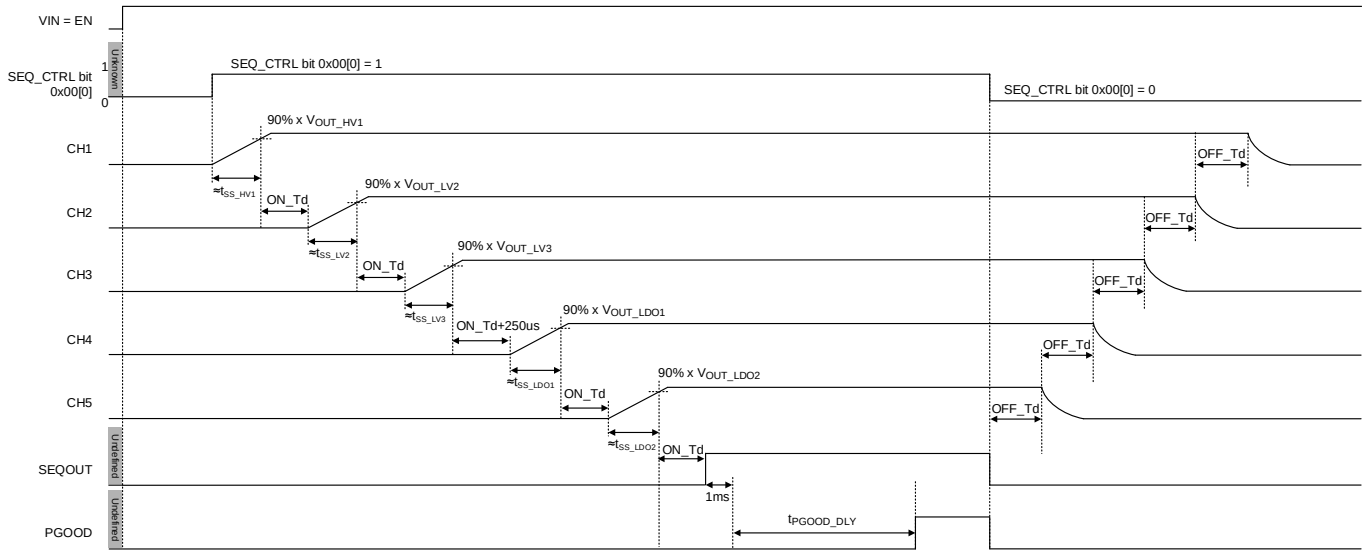


Figure 3. Example 1 of SEQ4 Power Sequence Triggered by SEQ_CTRL

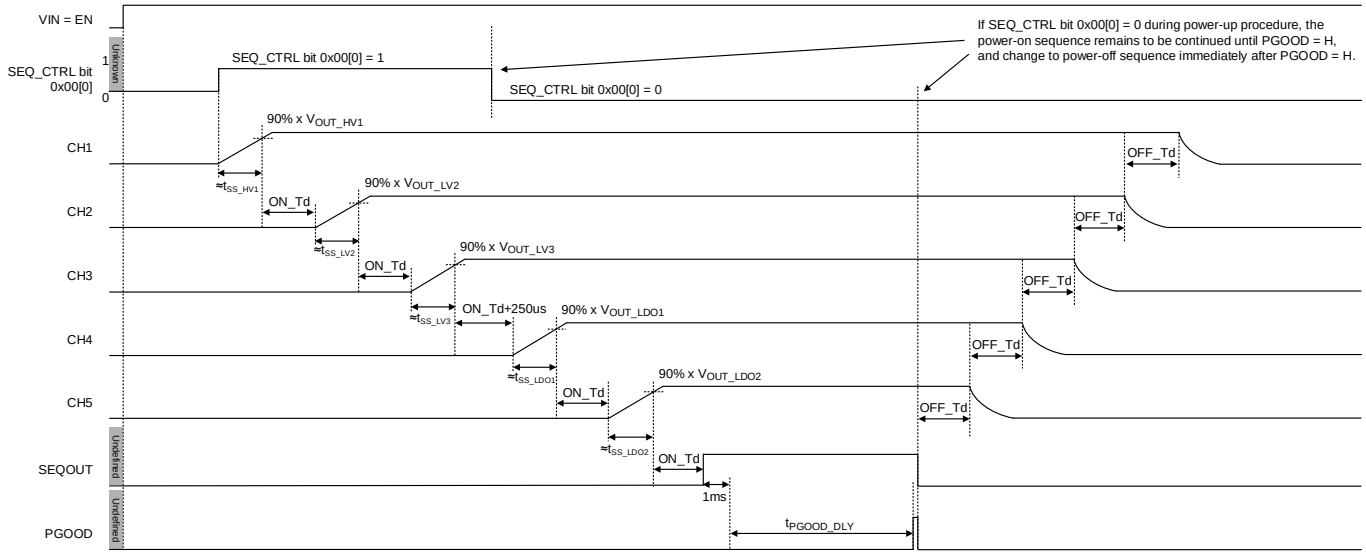


Figure 4. Example 2 of SEQ4 Power Sequence Triggered by SEQ_CTRL

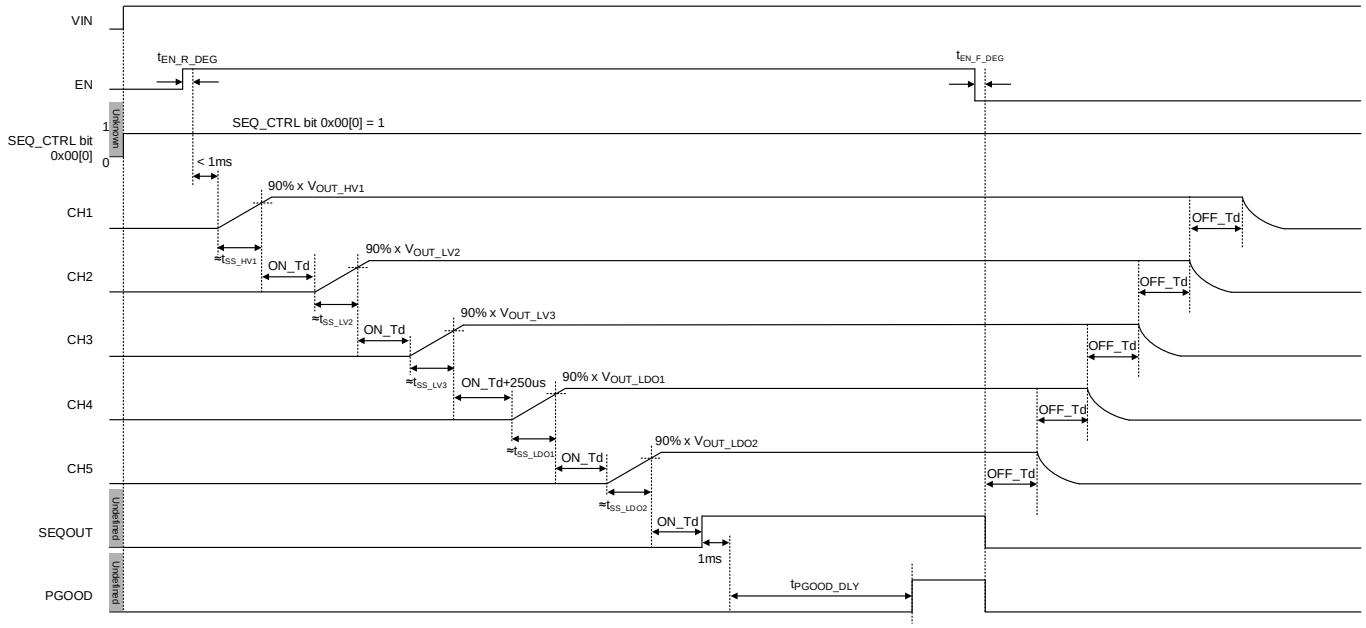


Figure 5. Example 1 of SEQ4 Power Sequence Triggered by EN

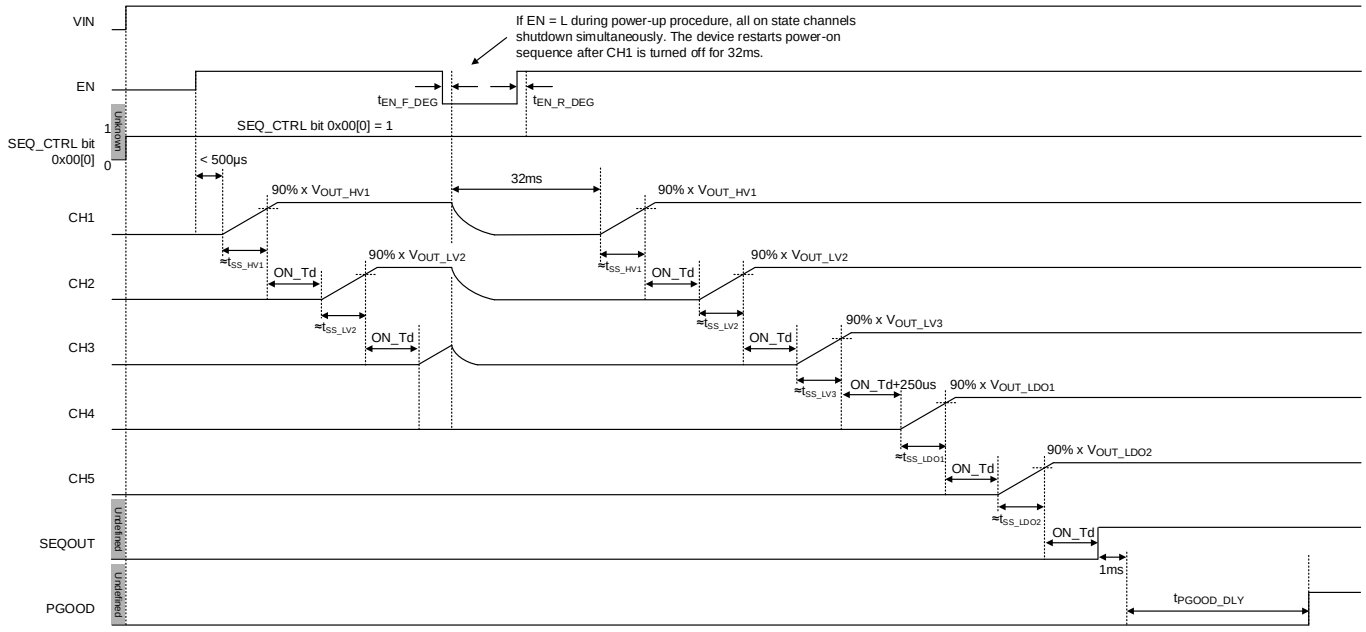


Figure 6. Example 2 of SEQ4 Power Sequence Triggered by EN

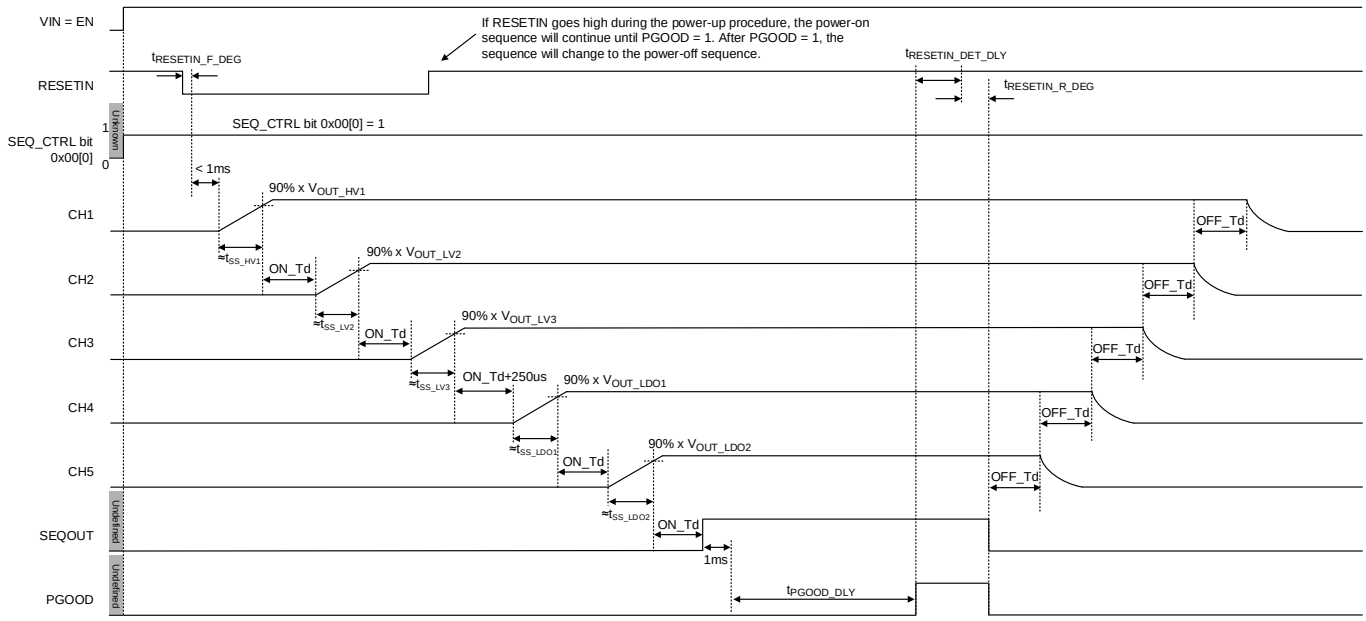


Figure 7. Example of SEQ4 Power Sequence Triggered by RESETIN

18.7 Output Voltage Setting

The output voltage settings of all rails are controlled through I^2C by configuring the relevant registers. The RTQ2079-QF is also equipped with OTP37 to OTP39 registers, ranging from 0xE5 to 0xE7[7:6], to enable one-time programmable settings for the corresponding output voltages, establishing them as the factory default settings.

18.7.1 HVBuck1, LVBuck2, and LVBuck3

HVBuck1 output voltage can be set via the register at 0x03[3:0] from 2.7V to 5V, and the default voltage is 3.6V.

LVBuck2 output voltage can be set via the register at 0x04[4:0] from 0.6V to 1.9V, and the default voltage is 1.1V.

LVBuck3 output voltage can be set via the register at 0x05[4:0] from 0.6V to 1.9V, and the default voltage is 1.8V.

18.7.2 LDO1 and LDO2

LDO1 output voltage can be set via the register at 0x06[4:0] from 1.8V to 3.5V. The default voltage is set at 3.3V.

LDO2 output voltage can be set via the register at 0x07[3:0] from 1.8V to 3.3V. The default voltage is set at 1.8V.

18.8 External Voltage Monitoring (VMONIN)

The RTQ2079-QF provides an independent pin, VMONIN, to support external device voltage monitoring. When the VMONIN configuration register bit at 0x0C[4] is set to 1, the device monitors the voltage 100μs after the PGOOD signal asserts high. If the external voltage is out of the monitoring range, the device enters an Alarm state. The ERROUT signal changes from a high to a low state as a warning, without disabling any channels. The ECU can configure different thresholds for monitoring voltage via the register at 0x0C[3:0]. This function is disabled by default and can be enabled through the register at 0x0C[4]. The RTQ2079-QF also includes OTP39 registers at 0xE7[5:1], providing one-time programmable settings for VMONIN protection thresholds, deglitch time, and EN status as the factory default settings.

18.9 External Error Monitoring (ERRIN1, ERRIN2)

The RTQ2079-QF includes two error-monitoring pins, ERRIN1 and ERRIN2, to monitor external device error signals. When the ERRIN configuration register bit at 0x0E[3] or 0x0E[2] is set to 1, the device monitors the error signal 100μs after the PGOOD signal asserts high. If an external error signal is detected through ERRIN1 or ERRIN2, the device enters an Alarm state. The ERROUT signal changes from a high to a low state as a warning, without disabling any channels. The ECU can configure different signal triggering directions via the register at 0x0E[1:0]. This function is enabled by default with a high active direction and can be configured through the register at 0x0E[3:2].

18.10 Reset Function

The RTQ2079-QF is equipped with an external hardware reset pin, RESETIN, and a RESET register at 0x0D[4] to reset the device. The device activates the RESET function 100μs after the PGOOD signal asserts high.

The RESET_ACT register bit at 0x0D[3] offers two configuration options:

- If the register bit 0x0D[3] is set to 0, all registers except for the sequence control related registers at 0x02[4:0], the external error monitoring related register at 0x0E[3:0], and the fault event indication registers at 0x11 to 0x15 are reset to their default values. The device follows the sequence settings to disable output rails. The fault event log remains stored in the corresponding registers and can be accessed by the ECU after reset.
- If the register bit 0x0D[3] is set to 1, all registers except for the sequence control related register at 0x02[4:0] and external error monitoring related register at 0x0E[3:0] are reset to their default values. The device follows the sequence settings to disable output rails.

18.11 Protection Features

The RTQ2079-QF is equipped with multiple protections to safeguard the device from damage caused by abnormal operations or fault conditions, including overload, short-circuit, soldering issues, and more.

18.11.1 Channel Output Undervoltage Protection (UVP)

There are four configurable UVP thresholds via the registers at 0x08 and 0x09[5:4]. The output UVP deglitch time is adjustable through the registers at 0x09[3:0]. When any of the bits at 0x0F[4:0] is configured to 1, the device disables all channels simultaneously and enters a Fail-Safe state once a UV fault is detected on any channel. Conversely, if all bits at 0x0F[4:0] are configured to 0 when a UV fault is detected, the device does not disable any channels but enters an Alarm state instead. The registers at 0x13[4:0] indicate that a UV fault event occurred on the corresponding channel, independent of the setting at 0x0F[4:0]. The RTQ2079-QF also includes OTP35 at registers 0xE3[1], providing one-time programmable settings of the channel output UVP behavior to be set as the factory default. Based on various states, there are different methods to reset the device, as shown in Table 4.

18.11.2 Channel Output Overvoltage Protection (OVP)

There are four configurable OVP thresholds via the registers at 0x0A and 0x0B[5:4]. The output OVP deglitch time is adjustable through the registers at 0x0B[3:0]. When any of the bits at 0x10[4:0] is configured to 1, the device disables all channels simultaneously and enters a Fail-Safe state once an OV fault is detected on any channel. Conversely, if all bits at 0x10[4:0] are configured to 0 when an OV fault is detected, the device does not disable any channels but enters an Alarm state instead. The registers at 0x14[4:0] indicate that the OV fault event occurred on the corresponding channel, independent of the settings at 0x10[4:0]. The RTQ2079-QF also includes OTP35 at registers 0xE3[2], providing one-time programmable settings of the channel output OVP behavior to be set as the factory default. Based on various states, there are different methods to reset the device, as shown in Table 4.

18.11.3 Channel Overcurrent Protection (OCP)

This section describes overcurrent protection function of HVBuck1, LVBuck2, LVBuck3, LDO1, and LDO2.

18.11.3.1 HVBuck1, LVBuck2, and LVBuck3

The step-down converter includes a cycle-by-cycle peak current limit for the high-side MOSFET, safeguarding against abnormal increases in inductor current, including those beyond the inductor's saturation current rating. In the event of an overcurrent, the controller immediately turns off the high-side MOSFET and turns on the low-side MOSFET to keep the inductor current within the peak current limit. After the inductor current decreases to below the valley current limit, the high-side MOSFET resumes switching. If an overcurrent fault is continuously detected for a duration longer than the deglitch time, the device disables all channels simultaneously and enters a Fail-Safe state. There are different methods to reset the device, as shown in Table 4.

18.11.3.2 LDO1 and LDO2

When the load exceeds the current-limit threshold, the output current is regulated to stay at this limit. If the overcurrent condition persists beyond the deglitch time, the device will disable all channels simultaneously and enter the Fail-Safe state. The device can be reset using various methods, as specified in Table 4.

18.11.4 Channel Input Overvoltage Protection (OVP)

If the input voltage of the step-down converters (LVBuck2 and LVBuck3), or LDO1 and LDO2 reaches the overvoltage protection threshold, the device disables all channels simultaneously and enters a Regulator-Off state. The device then automatically restarts and powers back on once the input voltage falls below the overvoltage threshold minus the hysteresis value.

18.11.5 Built-In Self-Test Protection

The RTQ2079-QF features a Built-In Self-Test (BIST) to ensure design integrity and enhance reliability. It conducts internal circuit tests before starting the rail power-on procedure The device enters a Fail-Safe state without activating the rails if the BIST fails, and the BIST_FAULT_EVT register at 0x11[6] is set to 1 to indicate a BIST failure.

18.11.6 ERROUT Protection

The ERROUT signal output is designed for error indication. The ERROUT pin is an open-drain design, and a pull-up resistor is needed. The ERROUT signal is pulled low if the RTQ2079-QF detects any fault in the Active state. The RTQ2079-QF implements an ERROUT monitor to detect the open-drain logic faults. The fault will be recorded by the register bit at 0x12[6].

18.11.7 OTP Register CRC (Cyclic Redundancy Check) Protection

When EN changes to a high state and the supply voltage V_{IN} exceeds the power-on reset level of 2.7V (typical), the device loads OTP data to reset all registers to default values. The CRC controller then begins to perform a CRC to verify the integrity of the OTP registers. The CRC controller calculates the checksum value of the OTP registers and compares it against the stored checksum value in OTP40. If a checksum error is detected, the device remains in the Power-Off state and sets the OTP_CRC_EVT register at 0x11[5] to 1 as an indication.

18.11.8 Device Configuration Register CRC Protection

When the ECU changes the registers to apply new settings, the CRC controller executes a CRC check to validate the integrity of the affected registers. If a checksum mismatch occurs, the device remains the current settings without reconfiguration. The CRC controller uses the standard CRC-8 polynomial, $X^8 + X^2 + X+1$, to calculate the checksum,

and it evaluates the CRC across an 8-bit string.

Table 6. Protection List

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Channel Behavior	Reset and Threshold (Typical)
Base	BIST	NA	NA	All channels stay disabled	Refer to Table 4. (Fail-Safe state)
	OTP CRC	NA	NA	All channels stay disabled	$V_{IN} \leq 2.5V$ or EN = L
System	UVLO	$V_{IN} \leq 3.3V$ (after IC operation)	32µs	Disable all channels	$V_{IN} \geq 3.8V$
	OVP	$V_{IN} \geq 25.5V$	5µs	Disable all channels	$V_{IN} \leq 19.5V$, Auto-recovery
	OTW	$T_J \geq 130°C$	5µs	Keep all channels in operation	Refer to Table 4. (Alarm state)
	TSD	$T_J \geq 170°C$	5µs	Disable all channels	$T_J \leq 150°C$, Auto-recovery
	VMONIN_OVP	$V_{MONIN} \geq 1.28V$	50µs	Keep all channels in operation	Refer to Table 4. (Alarm state)
	VMONIN_UVP	$V_{MONIN} \leq 1.14V$	50µs	Keep all channels in operation	Refer to Table 4. (Alarm state)
	ERRIN1	ERRIN1 = H or L (Depends on 0x0E[1])	50µs	Keep all channels in operation	Refer to Table 4. (Alarm state)
	ERRIN2	ERRIN2 = H or L (Depends on 0x0E[0])	50µs	Keep all channels in operation	Refer to Table 4. (Alarm state)
	ERROUT	ERROUT open-drain logic error	NA	Keep all channels in operation	Refer to Table 4. (Alarm state)
	I^2C CRC	NA	NA	Keep all channels in operation	NA
CH1 HVBuck1	UVP	$V_{OUT\_HV1} \leq V_{OUT\_HV1}$ x 80%	50µs	If 0x0F[4] = 0, keep all channels in operation	If 0x0F[4] = 0, refer to Table 4. (Alarm state)
				If 0x0F[4] = 1, disable all channels and latch off	If 0x0F[4] = 1, refer to Table 4. (Fail-Safe state)
	OVP	$V_{OUT\_HV1} \geq V_{OUT\_HV1}$ x 110%	50µs	If 0x10[4] = 0, keep all channels in operation	If 0x10[4] = 0, refer to Table 4. (Alarm state)
				If 0x10[4] = 1, disable all channels and latch off	If 0x10[4] = 1, refer to Table 4. (Fail-Safe state)
	OCP	$I_{L1\_peak} \geq 2.5A$	1ms	Cycle-by-cycle detection. If keeps for 1ms, disable all channels and latch off	Refer to Table 4. (Fail-Safe state)

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Channel Behavior	Reset and Threshold (Typical)
CH2 LVBuck2	UVP	$V_{OUT\_LV2} \leq V_{OUT\_LV2}$ x 95%	50µs	If 0x0F[3] = 0, keep all channels in operation	If 0x0F[3] = 0, refer to Table 4. (Alarm state)
				If 0x0F[3] = 1, disable all channels and latch-off	If 0x0F[3] = 1, refer to Table 4. (Fail-Safe state)
	OVP	$V_{OUT\_LV2} \geq V_{OUT\_LV2}$ x 105%	50µs	If 0x10[3] = 0, keep all channels operation	If 0x10[3] = 0, refer to Table 4. (Alarm state)
				If 0x10[3] = 1, disable all channels and latch off	If 0x10[3] = 1, refer to Table 4. (Fail-Safe state)
	OCP	$I_{L2\_peak} \geq 2.5A$	1ms	Cycle-by-cycle detection. If keeps for 1ms, disable all channels and latch off	Refer to Table 4. (Fail-Safe state)
	Input OVP	$V_{IN\_LV2} \geq 5.8V$	5µs	Disable all channels	$V_{IN\_LV2} \leq 5.22V$, Auto-recovery
CH3 LVBuck3	UVP	$V_{OUT\_LV3} \leq V_{OUT\_LV3}$ x 95%	50µs	If 0x0F[2] = 0, keep all channels in operation	If 0x0F[2] = 0, refer to Table 4. (Alarm state)
				If 0x0F[2] = 1, disable all channels and latch off	If 0x0F[2] = 1, refer to Table 4. (Fail-Safe state)
	OVP	$V_{OUT\_LV3} \geq V_{OUT\_LV3}$ x 105%	50µs	If 0x10[2] = 0, keep all channels in operation	If 0x10[2] = 0, refer to Table 4. (Alarm state)
				If 0x10[2] = 1, disable all channels and latch-off	If 0x10[2] = 1, refer to Table 4. (Fail-Safe state)
	OCP	$I_{L3\_peak} \geq 2.5A$	1ms	Cycle-by-cycle detection. If keeps for 1ms, disable all channels and latch off	Refer to Table 4. (Fail-Safe state)
	Input OVP	$V_{IN\_LV3} \geq 5.8V$	5µs	Disable all channels	$V_{IN\_LV3} \leq 5.22V$, Auto-recovery

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Channel Behavior	Reset and Threshold (Typical)
CH4 LDO1	UVP	$V_{OUT\_LDO1} \leq V_{OUT\_LDO1}$ x 95%	50µs	If 0x0F[1] = 0, keep all channels in operation	If 0x0F[1] = 0, refer to Table 4. (Alarm state)
				If 0x0F[1] = 1, disable all channels and latch off	If 0x0F[1] = 1, refer to Table 4. (Fail-Safe state)
	OVP	$V_{OUT\_LDO1} \geq V_{OUT\_LDO1}$ x 105%	50µs	If 0x10[1] = 0, keep all channels in operation	If 0x10[1] = 0, refer to Table 4. (Alarm state)
				If 0x10[1] = 1, disable all channels and latch off	If 0x10[1] = 1, refer to Table 4. (Fail-Safe state)
	OCP	$I_{OUT\_LDO1} \geq$ 450mA	1ms	Disable all channels and latch off	Refer to Table 4. (Fail-Safe state)
	Input OVP	$V_{IN\_LDO1} \geq$ 5.8V	5µs	Disable all channels	$V_{IN\_LDO1} \leq$ 5.3V, Auto-recovery
CH5 LDO2	UVP	$V_{OUT\_LDO2} \leq V_{OUT\_LDO2}$ x 95%	50µs	If 0x0F[0] = 0, keep all channels in operation	If 0x0F[0] = 0, refer to Table 4. (Alarm state)
				If 0x0F[0] = 1, disable all channels and latch-off	If 0x0F[0] = 1, refer to Table 4. (Fail-Safe state)
	OVP	$V_{OUT\_LDO2} \geq V_{OUT\_LDO2}$ x 105%	50µs	If 0x10[0] = 0, keep all channels in operation	If 0x10[0] = 0, refer to Table 4. (Alarm state)
				If 0x10[0] = 1, disable all channels and latch off	If 0x10[0] = 1, refer to Table 4. (Fail-Safe state)
	OCP	$I_{OUT\_LDO2} \geq$ 600mA	1ms	Disable all channels and latch off	Refer to Table 4. (Fail-Safe state)
	Input OVP	$V_{IN\_LDO2} \geq$ 5.8V	5µs	Disable all channels	$V_{IN\_LDO2} \leq$ 5.3V, Auto-recovery

Table 7. Fault Status and Event Log

Channel	Type	PGOOD	ERROUT	Event
Base	BIST	L	L	BIST_FAULT_EVT (0x11[6] = 1)
	OTP CRC	L	L	OTP_CRC_EVT (0x11[5] = 1)
System	UVLO	L	L	NA
	OVP	L	L	VIN_OV_EVT (0x11[2] = 1)
	OTW	H	L	TWARN_EVT (0x11[4] = 1)
	TSD	L	L	TSD_EVT (0x11[3] = 1)
	VMONIN_OVP	H	L	VMONIN_OV_EVT (0x12[3] = 1)
	VMONIN_UVP	H	L	VMONIN_UV_EVT (0x12[2] = 1)
	ERRIN1	H	L	ERRIN1_EVT (0x12[1] = 1)
	ERRIN2	H	L	ERRIN2_EVT (0x12[0] = 1)
	ERROUT	H	H	ERROUT_ALARM_EVT (0x12[6] = 1)
	I^2C CRC	H	H	NA
CH1 HVBuck1	UVP	H (0x0F[4] = 0)	L	HVBUCK1_UV_EVT (0x13[4] = 1)
		L (0x0F[4] = 1)		
	OVP	H (0x10[4] = 0)	L	HVBUCK1_OV_EVT (0x14[4] = 1)
		L (0x10[4] = 1)		
	OCP	L	L	HVBUCK1_OC_EVT (0x15[4] = 1)
CH2 LVBuck2	UVP	H (0x0F[3] = 0)	L	LVBUCK2_UV_EVT (0x13[3] = 1)
		L (0x0F[3] = 1)		
	OVP	H (0x10[3] = 0)	L	LVBUCK2_OV_EVT (0x14[3] = 1)
		L (0x10[3] = 1)		
	OCP	L	L	LVBUCK2_OC_EVT (0x15[3] = 1)
	Input OVP	L	L	PVD23_OV_EVT (0x11[1] = 1)

Channel	Type	PGOOD	ERROUT	Event
CH3 LVBuck3	UVP	H (0x0F[2] = 0)	L	LVBUCK3_UV_EVT (0x13[2] = 1)
		L (0x0F[2] = 1)		
	OVP	H (0x10[2] = 0)	L	LVBUCK3_OV_EVT (0x14[2] = 1)
		L (0x10[2] = 1)		
	OCP	L	L	LVBUCK3_OC_EVT (0x15[2] = 1)
	Input OVP	L	L	PVD23_OV_EVT (0x11[1] = 1)
CH4 LDO1	UVP	H (0x0F[1] = 0)	L	LDO1_UV_EVT (0x13[1] = 1)
		L (0x0F[1] = 1)		
	OVP	H (0x10[1] = 0)	L	LDO1_OV_EVT (0x14[1] = 1)
		L (0x10[1] = 1)		
	OCP	L	L	LDO1_OC_EVT (0x15[1] = 1)
	Input OVP	L	L	PVD45_OV_EVT (0x11[0] = 1)
CH5 LDO2	UVP	H (0x0F[0] = 0)	L	LDO2_UV_EVT (0x13[0] = 1)
		L (0x0F[0] = 1)		
	OVP	H (0x10[0] = 0)	L	LDO2_OV_EVT (0x14[0] = 1)
		L (0x10[0] = 1)		
	OCP	L	L	LDO2_OC_EVT (0x15[0] = 1)
	Input OVP	L	L	PVD45_OV_EVT (0x11[0] = 1)

18.12 Inductor Selection

18.12.1 HVBuck1, LVBuck2, and LVBuck3

Based on the following equations, the maximum inductor current for various load conditions can be determined. It is recommended that the inductor's saturation current rating exceed the calculated maximum current. To achieve optimal performance and efficiency, an inductor with a low Direct Current Resistance (DCR) should be chosen. The recommended nominal inductance is 1.5μH for HVBuck1 and 1μH for LVBuck2/LVBuck3.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_peak} = I_{OUT} + \frac{1}{2} \times \Delta I_L$$

18.13 Input and Output Capacitor Selection

18.13.1 HVBuck1, LVBuck2, and LVBuck3

It is recommended to use at least a 4.7μF input capacitor with a 10μF output capacitor for step-down converters. The ripple voltage is an important parameter when choosing output capacitor. This portion consists of two parts. One is the product of the ripple current and the ESR of the output capacitor; the other is generated by the charging and discharging cycles of the output capacitor. The output ripple voltage can be calculated using the following formula:

$$\Delta V_{OUTRipple} = \Delta V_{ESR} + \Delta V_{OUT} = \Delta V_{ESR} + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

18.13.2 LDO1 and LDO2

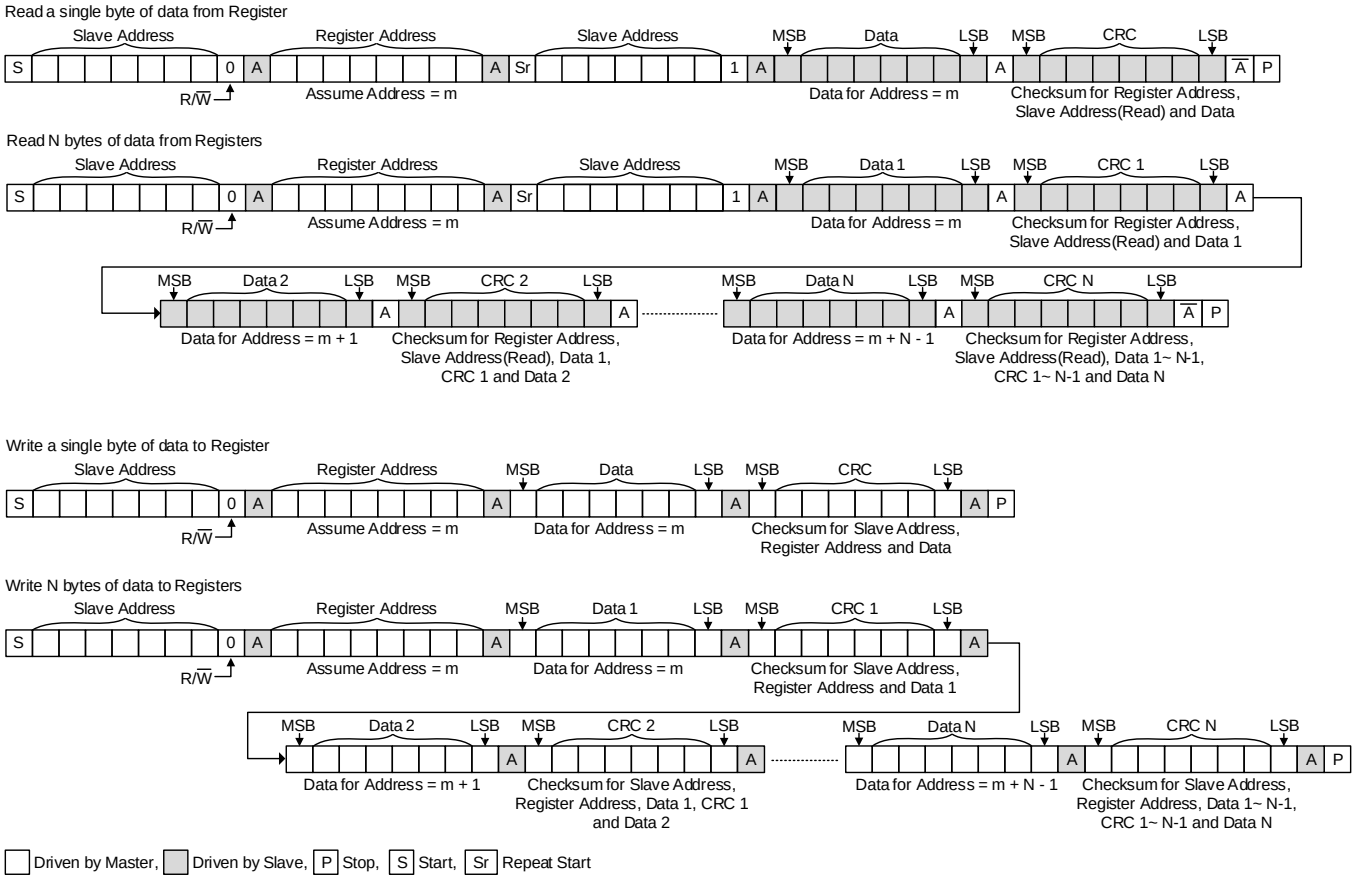
Proper selection of external capacitors is crucial for stability and performance of any LDO. A 2.2μF capacitor is generally suitable for both input and output of the LDO. Additional capacitors in parallel on the output can enhance noise suppression, it may also result in increased inrush current during the LDO's power-up sequence. This potential trade-off should be carefully evaluated.

18.14 I²C Interface

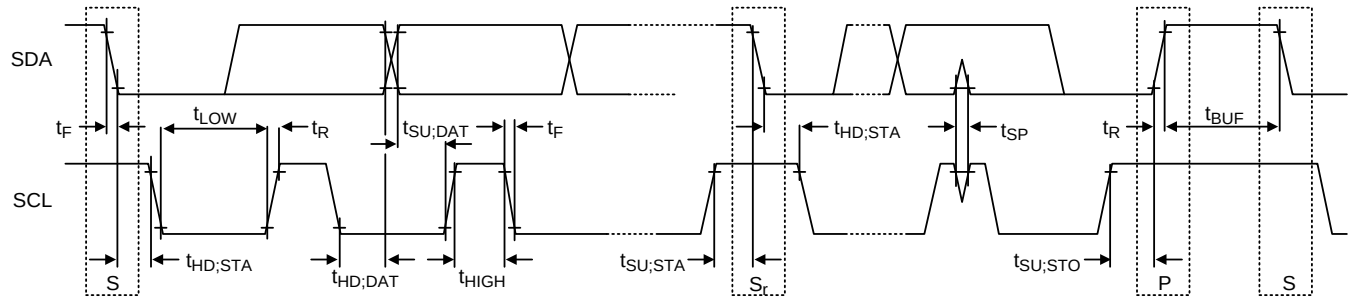
18.14.1 Slave Address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 = LSB
1	1	1	0	1	0	1	R/$\overline{W}$

18.14.2 Read and Write Function



18.14.3 I²C Waveform Information



18.15 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For WET-WQFN-24AL 4x4 package, the thermal resistance, θ_{JA}, is 37°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C - 25°C) / (37°C/W) = 2.7W for a WET-WQFN-24AL 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

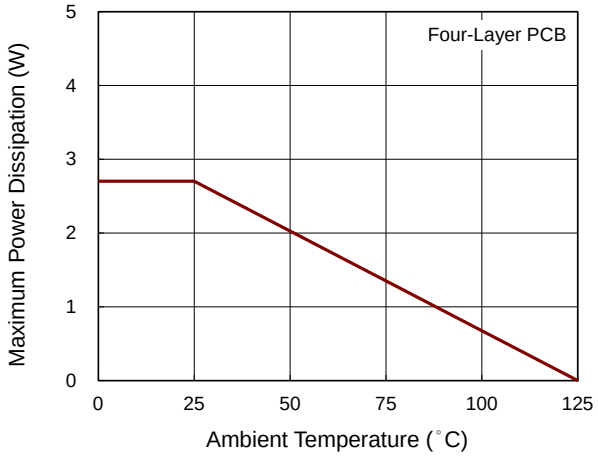


Figure 8. Derating Curve of Maximum Power Dissipation

18.16 Layout Considerations

The PCB layout is an important factor in maintaining the high performance of the RTQ2079-QF. Special attention must be given to the high current paths and fast-switching nodes in the PCB layout to ensure the robustness of the RTQ2079-QF. An improper layout can result in issues such as poor line or load regulation, shifts in ground and output voltage, stability problems, unsatisfactory EMI performance, or reduced efficiency. To optimize the performance of the RTQ2079-QF, the following PCB layout guidelines must be strictly followed:

- The trace from the switching node to the inductor should be kept as short as possible to minimize the switching loop, which will help to improve EMI characteristics.
- Place the input and output capacitors as close as possible to their respective pins to ensure effective filtering.
- Keep the main power traces as wide and short as possible.

- Connect the AGND and PGND to a solid ground plane to enhance thermal dissipation and provide noise immunity.
- Directly connect the step-sown converter's output capacitor to the feedback network to avoid voltage deviations caused by parasitic resistance and inductance in the PCB traces.

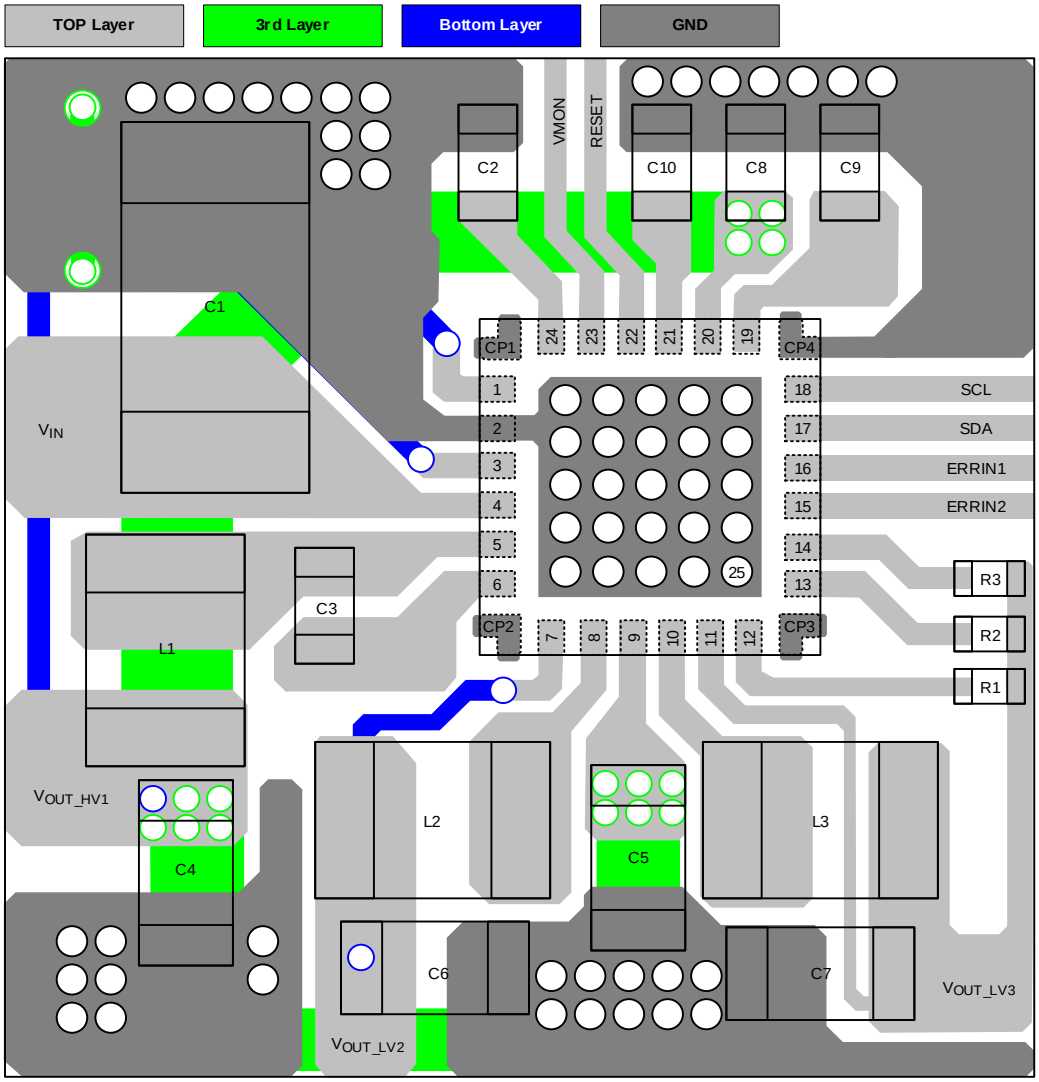


Figure 9. PCB Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Functional Register Description

R: Read Only

R/W: Read and Write

W1C: Write Clear (Write '1' then automatic clears to '0' after procedure finish)

Table 8.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOP_CFG	0x00	Meaning	Reserved	Reserved	Reserved	UVLO		UVLO_DEG	REBOOT_ACT	SEQ_CTRL
		Default	0	0	0	0	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
UVLO (CFG_LOCK)			VIN UVLO (Falling/Rising) voltage setting							
			00: 3.3V/3.8V (default) 01: 3.8V/4.5V 10: 4.3V/5.0V 11: 6.8V/7.3V							
UVLO_DEG (CFG_LOCK)			UVLO falling deglitch time setting							
			0: 32μs (default) 1: 64μs							
REBOOT_ACT (CFG_LOCK)			IC auto-reboot behavior selection when the PMIC enters a Fail-Safe State							
			0: Auto-reboot is disabled. (default) 1: Auto-reboot is enabled (register keep)							
SEQ_CTRL			Sequence ON and OFF control							
			0: Sequence OFF 1: Sequence ON (default)							

Table 9.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_CFG	0x01	Meaning	PGOOD_DLY		BUCK_MODE	HVBUCK1_DIS	LVBUCK2_DIS	LVBUCK3_DIS	LDO1_DIS	LDO2_DIS
		Default	0	1	1	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PGOOD_DLY (CFG_LOCK)	Time interval between the completion of the soft-start process for the last channel and the announcement of the Power-Good status.
	00: 4.7ms 01: 9.4ms (default) 10: 14.1ms 11: 18.8ms
BUCK_MODE (CFG_LOCK)	LVBuck2 and LVBuck3 operation mode
	0: PSM 1: FPWM (default)
HVBUCK1_DIS (CFG_LOCK)	HVBuck1 active output discharge
	0: Enable (default) 1: Disable
LVBUCK2_DIS (CFG_LOCK)	LVBuck2 active output discharge
	0: Enable (default) 1: Disable
LVBUCK3_DIS (CFG_LOCK)	LVBuck3 active output discharge
	0: Enable (default) 1: Disable
LDO1_DIS (CFG_LOCK)	LDO1 active output discharge
	0: Enable (default) 1: Disable
LDO2_DIS (CFG_LOCK)	LDO2 active output discharge
	0: Enable (default) 1: Disable

Table 10.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SEQ_ON_CFG	0x02	Meaning	Reserved	ON_Td		OFF_Td		POWER_ON_SEQ		
		Default	0	0	0	1	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ON_Td (CFG_LOCK)			Delay time between power-on channel and its next channel							
			00: 0ms (default) 01: 0.5ms 10: 1ms 11: 2ms							
OFF_Td (CFG_LOCK)			Delay time between power-off channel and its next channel							
			00: 1ms 01: 1.5ms 10: 2ms (default) 11: 3ms							
POWER_ON_SEQ (CFG_LOCK)			Power-on sequence setting							
			000: SEQ0 001: SEQ1 (default) 010: SEQ2 011: SEQ3 100: SEQ4 101: SEQ5 110: SEQ6 111: SEQ7							

Table 11.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HVBUCK1_OUT_CFG	0x03	Meaning	Reserved	Reserved	Reserved	Reserved	HVBUCK1_VOUT			
		Default	0	0	0	0	1	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVBUCK1_VOUT (CFG_LOCK)			HVBuck1 output voltage can be set from 2.7V to 4V (100mV/step), 4.5V, and 5.0V							
			0000: 2.7V 0001: 2.8V 0010: 2.9V 0011: 3.0V 0100: 3.1V 0101: 3.2V 0110: 3.3V 0111: 3.4V 1000: 3.5V 1001: 3.6V (default) 1010: 3.7V 1011: 3.8V 1100: 3.9V 1101: 4.0V 1110: 4.5V 1111: 5.0V							

Table 12.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVBUCK2_OUT_CFG	0x04	Meaning	Reserved	Reserved	Reserved	LVBUCK2_VOUT				
		Default	0	0	0	0	1	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LVBUCK2_VOUT (CFG_LOCK)			LVBuck2 output voltage can be set from 0.6V to 1.4V (50mV/step) and 1.4V to 1.9V (100mV/step)							
			00000: 0.60V 00001: 0.65V 00010: 0.70V 00011: 0.75V 00100: 0.80V 00101: 0.85V 00110: 0.90V 00111: 0.95V 01000: 1.00V 01001: 1.05V 01010: 1.10V (default) 01011: 1.15V 01100: 1.20V 01101: 1.25V 01110: 1.30V 01111: 1.35V 10000: 1.40V 10001: 1.50V 10010: 1.60V 10011: 1.70V 10100: 1.80V 10101: 1.90V 10110: 1.90V 10111: 1.90V 11000: 1.90V 11001: 1.90V 11010: 1.90V 11011: 1.90V 11100: 1.90V 11101: 1.90V 11110: 1.90V 11111: 1.90V							

Table 13.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVBUCK3_OUT_CFG	0x05	Meaning	Reserved	Reserved	Reserved	LVBUCK3_VOUT				
		Default	0	0	0	1	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LVBUCK3_VOUT (CFG_LOCK)			LVBuck3 output voltage can be set from 0.6V to 1.4V (50mV/step) and 1.4V to 1.9V (100mV/step)							
			00000: 0.60V 00001: 0.65V 00010: 0.70V 00011: 0.75V 00100: 0.80V 00101: 0.85V 00110: 0.90V 00111: 0.95V 01000: 1.00V 01001: 1.05V 01010: 1.10V 01011: 1.15V 01100: 1.20V 01101: 1.25V 01110: 1.30V 01111: 1.35V 10000: 1.40V 10001: 1.50V 10010: 1.60V 10011: 1.70V 10100: 1.80V (default) 10101: 1.90V 10110: 1.90V 10111: 1.90V 11000: 1.90V 11001: 1.90V 11010: 1.90V 11011: 1.90V 11100: 1.90V 11101: 1.90V 11110: 1.90V 11111: 1.90V							

Table 14.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LDO1_OUT_CFG	0x06	Meaning	Reserved	LDO1_IOUT_OC_SS		LDO1_VOUT				
		Default	0	1	1	1	0	0	1	1
		Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
LDO1_IOUT_OC_SS			LDO1 output current limit at soft-start duration							
			00: 450mA 01: 450mA 10: 50mA 11: 150mA (default)							
LDO1_VOUT (CFG_LOCK)			LDO1 output voltage can be set from 1.8V to 1.9V (50mV/step) and 2.5V to 3.5V (50mV/step)							
			00000: 1.80V 00001: 1.85V 00010: 1.90V 00011: 2.50V 00100: 2.55V 00101: 2.60V 00110: 2.65V 00111: 2.70V 01000: 2.75V 01001: 2.80V 01010: 2.85V 01011: 2.90V 01100: 2.95V 01101: 3.00V 01110: 3.05V 01111: 3.10V 10000: 3.15V 10001: 3.20V 10010: 3.25V 10011: 3.30V (default) 10100: 3.35V 10101: 3.40V 10110: 3.45V 10111: 3.50V							

Table 15.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LDO2_OUT_CFG	0x07	Meaning	Reserved	Reserved	Reserved	Reserved	LDO2_VOUT			
		Default	0	0	0	1	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LDO2_VOUT (CFG_LOCK)			LDO2 output voltage can be set from 1.8V to 3.3V(100mV/step)							
			0000: 1.8V (default) 0001: 1.9V 0010: 2.0V 0011: 2.1V 0100: 2.2V 0101: 2.3V 0110: 2.4V 0111: 2.5V 1000: 2.6V 1001: 2.7V 1010: 2.8V 1011: 2.9V 1100: 3.0V 1101: 3.1V 1110: 3.2V 1111: 3.3V							

Table 16.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_ UVP1_ CFG	0x08	Meaning	HVBUCK1_UV		LVBUCK2_UV		LVBUCK3_UV		LDO1_UV	
		Default	1	1	0	1	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVBUCK1_UV (CFG_LOCK)			HVBuck1 UV detection threshold with respect to the target voltage							
			00: 95% 01: 90% 10: 85% 11: 80% (default)							
LVBUCK2_UV (CFG_LOCK)			LVBuck2 UV detection threshold with respect to the target voltage							
			00: 96.5% 01: 95% (default) 10: 94% 11: 90%							
LVBUCK3_UV (CFG_LOCK)			LVBuck3 UV detection threshold with respect to the target voltage							
			00: 96.5% 01: 95% (default) 10: 94% 11: 90%							
LDO1_UV (CFG_LOCK)			LDO1 UV detection threshold with respect to the target voltage							
			00: 96.5% 01: 95% (default) 10: 94% 11: 90%							

Table 17.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_ UVP2_ CFG	0x09	Meaning	Reserved	Reserved	LDO2_UV		HVBUCK1_UV_DEG		LVCH_UV_DEG	
		Default	0	0	0	1	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LDO2_UV (CFG_LOCK)			LDO2 UV detection threshold with respect to the target voltage							
			00: 96.5% 01: 95% (default) 10: 94% 11: 90%							
HVBUCK1_UV_DEG (CFG_LOCK)			HVBuck1 UV detection deglitch time selection							
			00: Reserved 01: 50µs (default) 10: 75µs 11: 100µs							
LVCH_UV_DEG (CFG_LOCK)			LVBuck2, LVBuck3, LDO1, and LDO2 UV detection deglitch time selection							
			00: Reserved 01: 50µs (default) 10: 75µs 11: 100µs							

Table 18.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_ OVP1_ CFG	0x0A	Meaning	HVBUCK1_OV		LVBUCK2_OV		LVBUCK3_OV		LDO1_OV	
		Default	0	1	0	1	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVBUCK1_OV (CFG_LOCK)			HVBuck1 OV detection threshold with respect to the target voltage							
			00: 105% 01: 110% (default) 10: 115% 11: 120%							
LVBUCK2_OV (CFG_LOCK)			LVBuck2 OV detection threshold with respect to the target voltage							
			00: 103.5% 01: 105% (default) 10: 106% 11: 110%							
LVBUCK3_OV (CFG_LOCK)			LVBuck3 OV detection threshold with respect to the target voltage							
			00: 103.5% 01: 105% (default) 10: 106% 11: 110%							
LDO1_OV (CFG_LOCK)			LDO1 OV detection threshold with respect to the target voltage							
			00: 103.5% 01: 105% (default) 10: 106% 11: 110%							

Table 19.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_ OVP2_ CFG	0x0B	Meaning	Reserved	Reserved	LDO2_OV		HVBUCK1_OV_DEG		LVCH_OV_DEG	
		Default	0	0	0	1	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LDO2_OV (CFG_LOCK)			LDO2 OV detection threshold with respect to the target voltage							
			00: 103.5% 01: 105% (default) 10: 106% 11: 110%							
HVBUCK1_OV_DEG (CFG_LOCK)			HVBuck1 OV detection deglitch time selection							
			00: Reserved 01: 50µs (default) 10: 75µs 11: 100µs							
LVCH_OV_DEG (CFG_LOCK)			LVBuck2, LVBuck3, LDO1 and LDO2 OV detection deglitch time selection							
			00: Reserved 01: 50µs (default) 10: 75µs 11: 100µs							

Table 20.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VMON_CFG	0x0C	Meaning	Reserved	VMON_DEG		VMON_EN	VMON_H		VMON_L	
		Default	0	1	1	0	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VMON_DEG (CFG_LOCK)			VMONIN deglitch time							
			00: 10μs 01: 15μs 10: 25μs 11: 50μs (default)							
VMON_EN (CFG_LOCK)			VMONIN function							
			0: Disable (default) 1: Enable							
VMON_H (CFG_LOCK)			VMON sensed voltage high level can be set from 0.96V to 1.33V.							
			00: 1.33V 01: 1.28V (default) 10: 1.18V 11: 0.96V							
VMON_L (CFG_LOCK)			VMON sensed voltage low level can be set from 0.84V to 1.14V.							
			00: 1.09V 01: 1.14V (default) 10: 1.02V 11: 0.84V							

Table 21.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FUNC1_CFG	0x0D	Meaning	Reserved	Reserved	Reserved	RESET	RESET_ACT	FAULT_MASK	PHASE_EN	SSP_EN
		Default	0	0	0	0	0	0	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RESET	SW reset and reset behavior follows 0x0D[3], RESET_ACT
	0: None (default) 1: SW Reset
RESET_ACT (CFG_LOCK)	RESET triggered registers behavior selection
	0: Reset all registers to default value, with the exception of the fault event registers (default) 1: Reset all registers to default value
FAULT_MASK (CFG_LOCK)	All faults event mask
	0: Unmask (default) 1: Mask
PHASE_EN (CFG_LOCK)	Bucks' switching phase shift function
	0: Disable 1: Enable (default)
SSP_EN (CFG_LOCK)	Bucks' switching frequency spread spectrum function
	0: Disable 1: Enable (default)

Table 22.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FUNC2_CFG	0x0E	Meaning	Reserved	Reserved	Reserved	Reserved	ERRIN1_EN	ERRIN2_EN	ERRIN1_ACTL	ERRIN2_ACTL
		Default	0	0	0	0	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ERRIN1_EN	ERRIN1 function
	0: Disable 1: Enable (default)
ERRIN2_EN	ERRIN2 function
	0: Disable 1: Enable (default)
ERRIN1_ACTL	ERRIN1 pin level to act selection
	0: Low to act 1: High to act (default)
ERRIN2_ACTL	ERRIN2 pin level to act selection
	0: Low to act 1: High to act (default)

Table 23.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PROTEC1_CFG	0x0F	Meaning	Reserved	Reserved	Reserved	HVBUCK1_UV_SD	LVBUCK2_UV_SD	LVBUCK3_UV_SD	LDO1_UV_SD	LDO2_UV_SD
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVBUCK1_UV_SD (CFG_LOCK)			HVBuck1 undervoltage protection behavior selection							
			0: Only inform ECU of fault events (default) 1: Channel latch-off and inform ECU of fault events							
LVBUCK2_UV_SD (CFG_LOCK)			LVBuck2 undervoltage protection behavior selection							
			0: Only inform ECU of fault events (default) 1: Channel latch-off and inform ECU of fault events							
LVBUCK3_UV_SD (CFG_LOCK)			LVBuck3 undervoltage protection behavior selection							
			0: Only inform ECU of fault events (default) 1: Channel latch-off and inform ECU of fault events							
LDO1_UV_SD (CFG_LOCK)			LDO1 undervoltage protection behavior selection							
			0: Only inform ECU of fault events (default) 1: Channel latch-off and inform ECU of fault events							
LDO2_UV_SD (CFG_LOCK)			LDO2 undervoltage protection behavior selection							
			0: Only inform ECU of fault events (default) 1: Channel latch-off and inform ECU of fault events							

Table 24.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PROTEC2_CFG	0x10	Meaning	Reserved	Reserved	Reserved	HVBUCK1_OV_SD	LVBUCK2_OV_SD	LVBUCK3_OV_SD	LDO1_OV_SD	LDO2_OV_SD
		Default	0	0	0	1	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

HVBUCK1_OV_SD (CFG_LOCK)	HVBuck1 overvoltage protection behavior selection
	0: Only inform ECU of fault events 1: Channel latch-off and inform ECU of fault events (default)
LVBUCK2_OV_SD (CFG_LOCK)	LVBuck2 overvoltage protection behavior selection
	0: Only inform ECU of fault events 1: Channel latch-off and inform ECU of fault events (default)
LVBUCK3_OV_SD (CFG_LOCK)	LVBuck3 overvoltage protection behavior selection
	0: Only inform ECU of fault events 1: Channel latch-off and inform ECU of fault events (default)
LDO1_OV_SD (CFG_LOCK)	LDO1 overvoltage protection behavior selection
	0: Only inform ECU of fault events 1: Channel latch-off and inform ECU of fault events (default)
LDO2_OV_SD (CFG_LOCK)	LDO2 overvoltage protection behavior selection
	0: Only inform ECU of fault events 1: Channel latch-off and inform ECU of fault events (default)

Table 25.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BASE1_EVT	0x11	Meaning	Reserved	BIST_FAULT_EVT	OTP_CRC_EVT	TWARN_EVT	TSD_EVT	VIN_OV_EVT	PVD23_OV_EVT	PVD45_OV_EVT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	W1C	W1C	W1C	W1C	W1C	W1C	W1C

BIST_FAULT_EVT	BIST fault acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
OTP_CRC_EVT	Internal OTP CRC checking fault acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
TWARN_EVT	Thermal warning event acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
TSD_EVT	Thermal shutdown event acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
VIN_OV_EVT	VIN overvoltage threshold event acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
PVD23_OV_EVT	PVD23 overvoltage threshold event acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
PVD45_OV_EVT	PVD45 overvoltage threshold event acknowledgement
	0: No faults are detected, or faults are masked (default) 1: Fault is detected

Table 26.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BASE2_EVT	0x12	Meaning	Reserved	ERROUT_ALARM_EVT	Reserved	Reserved	VMONIN_OV_EVT	VMONIN_UV_EVT	ERRIN1_EVT	ERRIN2_EVT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	W1C	R/W	R/W	W1C	W1C	W1C	W1C
ERROUT_ALARM_EVT			ERROUT logic fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
VMONIN_OV_EVT			VMONIN overvoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
VMONIN_UV_EVT			VMONIN undervoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
ERRIN1_EVT			ERRIN1 fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
ERRIN2_EVT			ERRIN2 fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							

Table 27.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_UV_EVT	0x13	Meaning	Reserved	Reserved	Reserved	HVBUCK1_UV_EVT	LVBUCK2_UV_EVT	LVBUCK3_UV_EVT	LDO1_UV_EVT	LDO2_UV_EVT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	W1C	W1C	W1C	W1C	W1C
HVBUCK1_UV_EVT			HVBuck1 undervoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LVBUCK2_UV_EVT			LVBuck2 undervoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LVBUCK3_UV_EVT			LVBuck3 undervoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LDO1_UV_EVT			LDO1 undervoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LDO2_UV_EVT			LDO2 undervoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							

Table 28.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_OV_EVT	0x14	Meaning	Reserved	Reserved	Reserved	HVBUCK1_OV_EVT	LVBUCK2_OV_EVT	LVBUCK3_OV_EVT	LDO1_OV_EVT	LDO2_OV_EVT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	W1C	W1C	W1C	W1C	W1C
HVBUCK1_OV_EVT			HVBuck1 overvoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LVBUCK2_OV_EVT			LVBuck2 overvoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LVBUCK3_OV_EVT			LVBuck3 overvoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LDO1_OV_EVT			LDO1 overvoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							
LDO2_OV_EVT			LDO2 overvoltage fault event							
			0: No faults are detected, or faults are masked (default) 1: Fault is detected							

Table 29.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH_OC_EVT	0x15	Meaning	Reserved	Reserved	Reserved	HVBUCK1_OC_EVT	LVBUCK2_OC_EVT	LVBUCK3_OC_EVT	LDO1_OC_EVT	LDO2_OC_EVT
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	W1C	W1C	W1C	W1C	W1C

HVBUCK1_OC_EVT	HVBuck1 overcurrent fault event
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
LVBUCK2_OC_EVT	LVBuck2 overcurrent fault event
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
LVBUCK3_OC_EVT	LVBuck3 overcurrent fault event
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
LDO1_OC_EVT	LDO1 overcurrent fault event
	0: No faults are detected, or faults are masked (default) 1: Fault is detected
LDO2_OC_EVT	LDO2 overcurrent fault event
	0: No faults are detected, or faults are masked (default) 1: Fault is detected

Table 30.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEV_STAT	0x16	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	DEV_STATE		
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
DEV_STATE			Indicates the PMIC present state							
			000: Regulator-Off state or BIST state (default) 001: Standby state 010: Power-On state 011: Active state 100: Alarm state 101: Fail-Safe state							

Table 31.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_CRC_1	0x18	Meaning	CRC_START	CRC_FAIL	CRC_DONE	CRC_EN	Reserved	Reserved	Reserved	Reserved
		Default	0	0	0	1	0	0	0	0
		Read/Write	R/W	R	R	R/W	R/W	R/W	R/W	R/W
CRC_START			For OTP CRC value calculation, the calculated value is displayed at 0x19							
			0: None (default) 1: Enable							
CRC_FAIL			OTP CRC comparison result							
			0: None or CRC pass (default) 1: CRC fail							
CRC_DONE			OTP CRC calculation process							
			0: None or calculating (default) 1: Calculation completed							
CRC_EN			OTP CRC function							
			0: Disable 1: Enable (default)							

Table 32.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP_CRC_2	0x19	Meaning	OTP_CRC_RESULT							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
OTP_CRC_RESULT			OTP CRC calculation value							

Table 33.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM_PASS_CODE1	0x20	Meaning	TM_PASS_CODE1							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TM_PASS_CODE1			To enter guest mode, set 0x20 = 8'h69 and 0x21 = 8'h96 sequentially To leave guest mode, set 0x20 ≠ 8'h69 or 0x21 ≠ 8'h96							

Table 34.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM_PASS_CODE2	0x21	Meaning	TM_PASS_CODE2							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TM_PASS_CODE2			To enter guest mode, set 0x20 = 8'h69 and 0x21 = 8'h96 sequentially To leave guest mode, set 0x20 ≠ 8'h69 or 0x21 ≠ 8'h96							

Table 35.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP34	0xE2	Meaning	UV_LVCH		OV_LVCH		UV_DEG_LVCH		OV_DEG_LVCH	
		Default	0	1	0	1	0	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
UV_LVCH (Not in RTK P/N Options)			LVBuck2, LVBuck3, LDO1, and LDO2 UV detection threshold with respect to target voltage							
			00: 96.5% 01: 95% (default) 10: 94% 11: 90%							
OV_LVCH (Not in RTK P/N Options)			LVBuck2, LVBuck3, LDO1, and LDO2 OV detection threshold with respect to target voltage							
			00: 103.5% 01: 105% (default) 10: 106% 11: 110%							
UV_DEG_LVCH (Not in RTK P/N Options)			LVBuck2, LVBuck3, LDO1, and LDO2 UV detection deglitch time selection							
			00: Reserved 01: 50μs (default) 10: 75μs 11: 100μs							
OV_DEG_LVCH (Not in RTK P/N Options)			LVBuck2, LVBuck3, LDO1, and LDO2 OV detection deglitch time selection							
			00: Reserved 01: 50μs (default) 10: 75μs 11: 100μs							

Table 36.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP35	0xE3	Meaning	OV_HVCH		UVLO		UVLO_DEG	CH_OV_SD	CH_UV_SD	REBOOT
		Default	0	1	0	0	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OV_HVCH (Not in RTK P/N Options)			HVBuck1 OV detection threshold with respect to the target voltage							
			00: 105% 01: 110% (default) 10: 115% 11: 120%							
UVLO			VIN UVLO (falling/rising) voltage setting							
			00: 3.3V/3.8V (default) 01: 3.8V/4.5V 10: 4.3V/5.0V 11: 6.8V/7.3V							
UVLO_DEG (Not in RTK P/N Options)			UVLO falling deglitch time setting							
			0: 32μs (default) 1: 64μs							
CH_OV_SD (Not in RTK P/N Options)			HVBuck1, LVBuck2, LVBuck3, LDO1, and LDO2 overvoltage protection behavior selection							
			0: Only inform ECU of fault events 1: Channel latch-off and inform ECU of fault events (default)							
CH_UV_SD			HVBuck1, LVBuck2, LVBuck3, LDO1, and LDO2 undervoltage protection behavior selection							
			0: Only inform ECU of fault events (default) 1: Channel latch-off and inform ECU of fault events							
REBOOT (Not in RTK P/N Options)			IC auto-reboot behavior selection when the PMIC enters a Fail-Safe state							
			0: Auto-reboot is disabled (default) 1: Auto-reboot is enabled (register keep)							

Table 37.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP36	0xE4	Meaning	SEQ_ CTRL	ON_Td		OFF_Td		POWER_ON_SEQ		
		Default	1	0	0	1	0	0	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SEQ_CTRL (Not in RTK P/N Options)			Sequence on and off control							
			0: Sequence off 1: Sequence on (default)							
ON_Td			Delay time between power-on channel and its next channel							
			00: 0ms (default) 01: 0.5ms 10: 1ms 11: 2ms							
OFF_Td			Delay time between power-off channel and its next channel							
			00: 1ms 01: 1.5ms 10: 2ms (default) 11: 3ms							
POWER_ON_SEQ			Power-on sequence setting							
			000: SEQ0 001: SEQ1 (default) 010: SEQ2 011: SEQ3 100: SEQ4 101: SEQ5 110: SEQ6 111: SEQ7							

Table 38.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP37	0xE5	Meaning	HVBUCK1_VOUT				LVBUCK2_VOUT			
		Default	1	0	0	1	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVBUCK1_VOUT			HVBuck1 output voltage can be set from 2.7V to 4V (100mV/step), 4.5V, and 5.0V 0000: 2.7V 0001: 2.8V 0010: 2.9V 0011: 3.0V 0100: 3.1V 0101: 3.2V 0110: 3.3V 0111: 3.4V 1000: 3.5V 1001: 3.6V (default) 1010: 3.7V 1011: 3.8V 1100: 3.9V 1101: 4.0V 1110: 4.5V 1111: 5.0V							
LVBUCK2_VOUT			LVBuck2 output voltage can be set from 0.9V to 1.4V (50mV/step) and 1.4V to 1.9V (100mV/step) 0000: 0.90V 0001: 0.95V 0010: 1.00V 0011: 1.05V 0100: 1.10V (default) 0101: 1.15V 0110: 1.20V 0111: 1.25V 1000: 1.30V 1001: 1.35V 1010: 1.40V 1011: 1.50V 1100: 1.60V 1101: 1.70V 1110: 1.80V 1111: 1.90V							

Table 39.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP38	0xE6	Meaning	LVBUCK3_VOUT				LDO1_VOUT			
		Default	1	1	1	0	1	1	0	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LVBUCK3_VOUT			LVBuck3 output voltage can be set from 0.9V to 1.4V (50mV/step) and 1.4V to 1.9V (100mV/step)							
			0000: 0.90V 0001: 0.95V 0010: 1.00V 0011: 1.05V 0100: 1.10V 0101: 1.15V 0110: 1.20V 0111: 1.25V 1000: 1.30V 1001: 1.35V 1010: 1.40V 1011: 1.50V 1100: 1.60V 1101: 1.70V 1110: 1.80V (default) 1111: 1.90V							
LDO1_VOUT			LDO1 output voltage can be set from 1.8V and 2.7V to 3.4V (50mV/step)							
			0000: 1.80V 0001: 2.70V 0010: 2.75V 0011: 2.80V 0100: 2.85V 0101: 2.90V 0110: 2.95V 0111: 3.00V 1000: 3.05V 1001: 3.10V 1010: 3.15V 1011: 3.20V 1100: 3.25V 1101: 3.30V (default) 1110: 3.35V 1111: 3.40V							

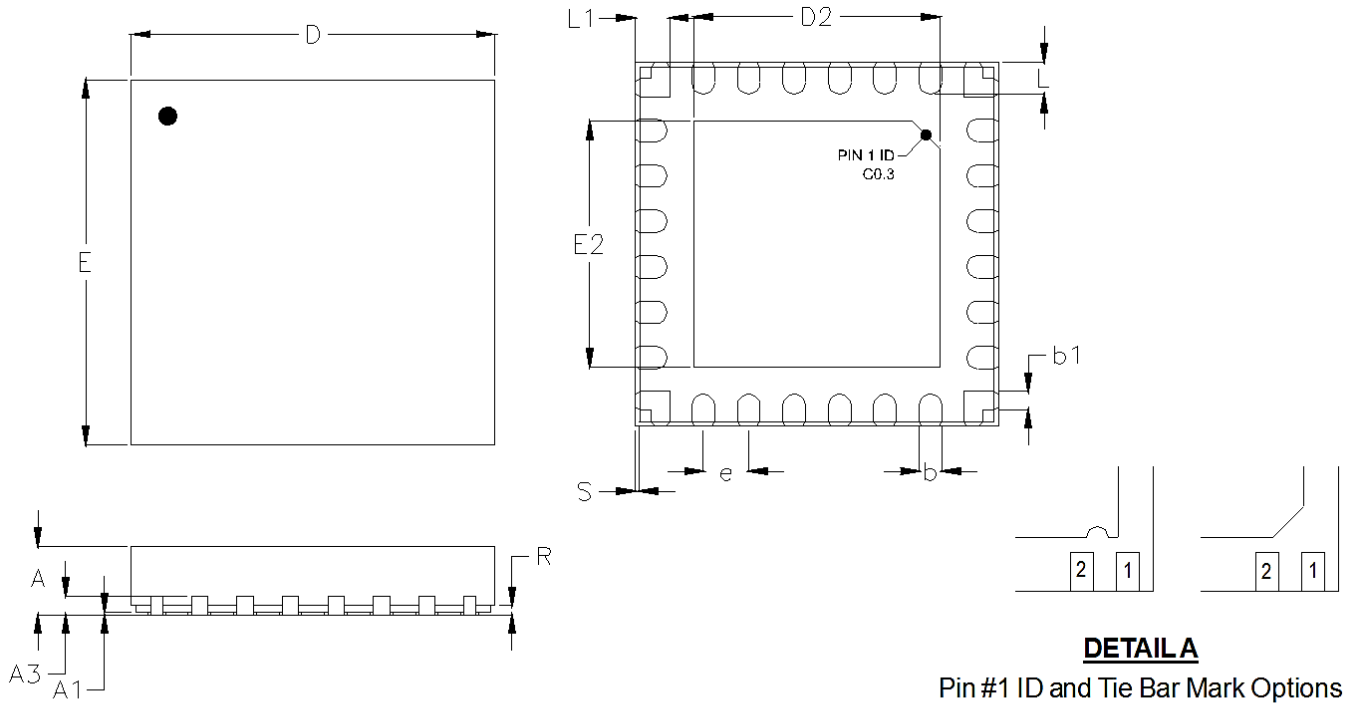
Table 40.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP39	0xE7	Meaning	LDO2_VOUT		VMON_DEG		VMON_LEVEL		VMON_EN	ADR
		Default	0	0	1	1	0	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LDO2_VOUT			LDO2 output voltage can be set from 1.8V, 2.5V, 2.9V and 3.3V							
			00: 1.8V (default) 01: 2.5V 10: 2.9V 11: 3.3V							
VMON_DEG (Not in RTK P/N Options)			VMONIN deglitch time							
			00: 10μs 01: 15μs 10: 25μs 11: 50μs (default)							
VMON_LEVEL (Not in RTK P/N Options)			VMON sensed voltage level can be set as follows							
			00: VMON_H/VMON_L = 1.33V/1.09V 01: VMON_H/VMON_L = 1.28V/1.14V (default) 10: VMON_H/VMON_L = 1.18V/1.02V 11: VMON_H/VMON_L = 0.96V/0.84V							
VMON_EN (Not in RTK P/N Options)			VMONIN function							
			0: Disable (default) 1: Enable							
ADR (Not in RTK P/N Options)			PMIC slave address							
			0: 75h (7bit) (default) 1: 76h (7bit)							

Table 41.

Address Name	Register Address	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OTP40	0xE8	Meaning	CRC_B7	CRC_B6	CRC_B5	CRC_B4	CRC_B3	CRC_B2	CRC_B1	CRC_B0
		Default	0	1	0	0	0	1	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CRC_CODE			After modifying the settings of OTP34 to OTP40, write the register 0x18[7] = 1. This action triggers the PMIC to automatically calculate a new CRC which is shown in the register 0x19. Enter the new CRC value into OTP40 to complete the PMIC BIST process successfully.							

20 Outline Dimension



DETAIL A

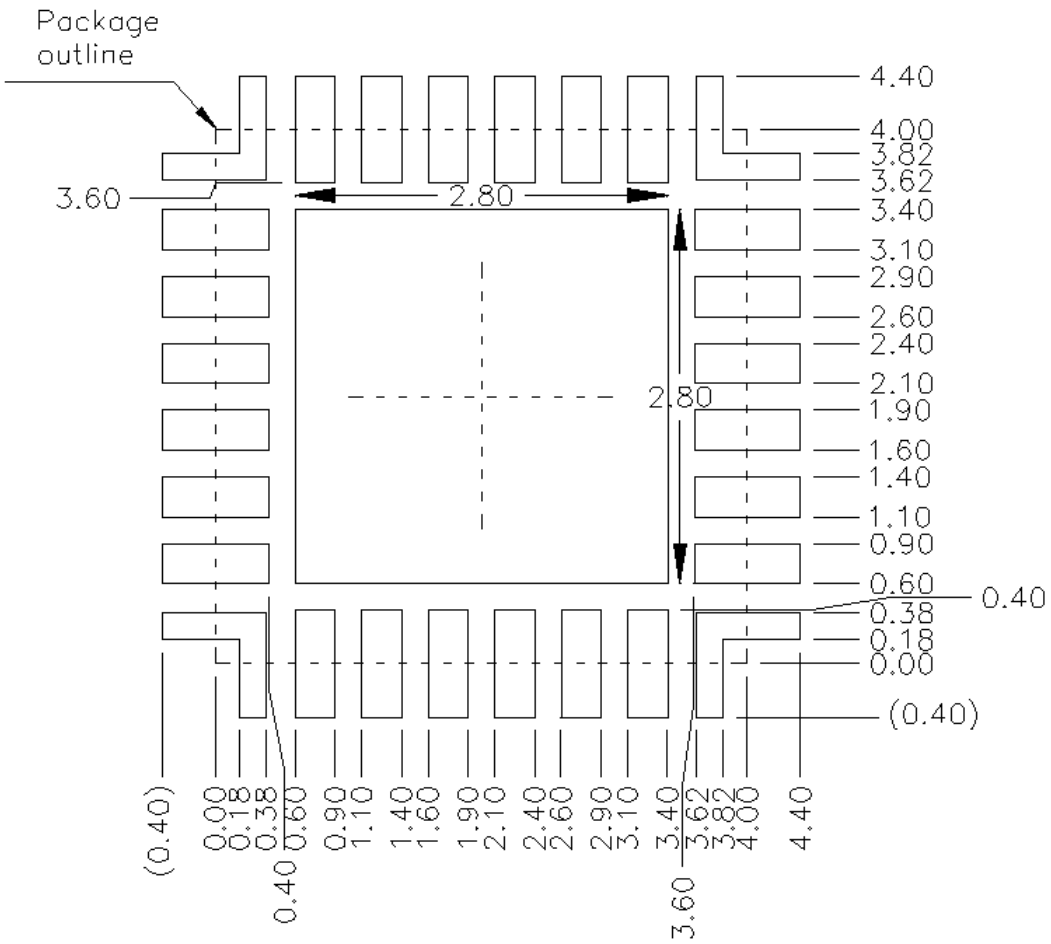
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
b1	0.150	0.250	0.006	0.010
D	3.900	4.100	0.154	0.161
D2	2.650	2.750	0.104	0.108
E	3.900	4.100	0.154	0.161
E2	2.650	2.750	0.104	0.108
e	0.500		0.020	
L	0.300	0.400	0.012	0.016
L1	0.330	0.430	0.013	0.017
R	0.050	0.150	0.002	0.006
S	0.001	0.090	0.000	0.004

WET W-Type 24AL QFN 4x4 Package

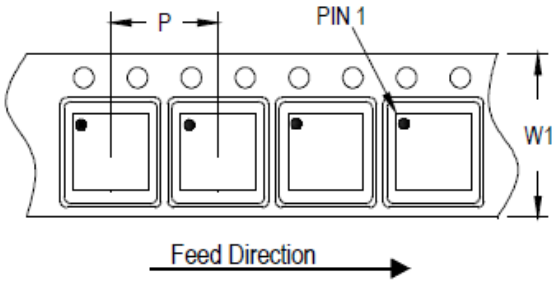
21 Footprint Information

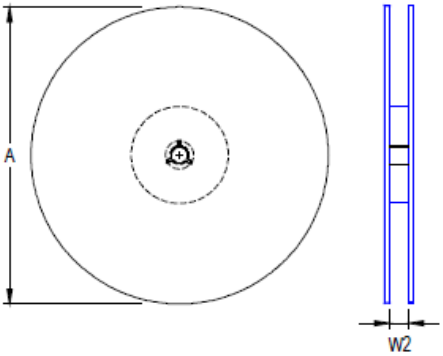


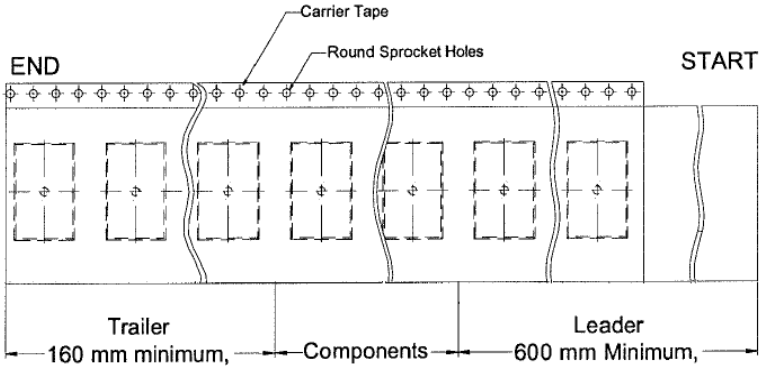
Tolerance (mm)
±0.050

22 Packing Information

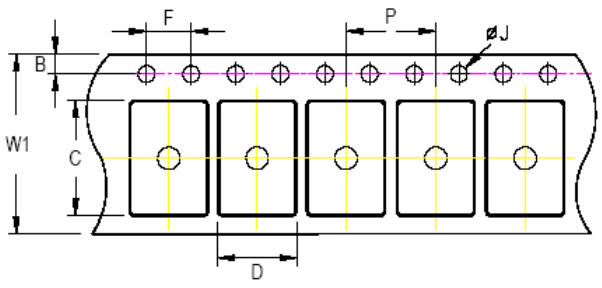
22.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

22.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

22.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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23 Datasheet Revision History

Version	Date	Description	Item
00	2024/10/9	Final	*Packing Information on page 80* - Updated Tape and Reel Data