Micro-Power Voltage Detector with Manual Reset

General Description

The RT9834 is a micro-power voltage detector with deglitched manual reset input supervising the power supply voltage level for microprocessors (µP) or digital systems. It provides internally fixed threshold levels with 0.1V per step ranging from 1.2V to 5V, which covers most digital applications. It features low supply current of 3µA. The RT9834 performs supervisory function by sending out a reset signal whenever the V_{DD} voltage falls below a preset threshold level. This reset signal will last the whole period before V_{DD} recovering. Once V_{DD} recovered upcrossing the threshold level, the reset signal will be released after a certain delay time. To pull reset signal low manually, just pull the manual reset input (MR) below the specified V_{IL} level. The RT9834 is available in the SC-82 and SOT-143 packages.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

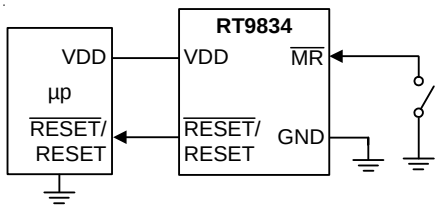
Features

- **Internally Fixed Threshold 1.2V to 5V in 0.1V Step**
- **High Accuracy ±1.5%**
- **Low Supply Current 3µA**
- **No External Components Required**
- **Quick Reset within 20µs**
- **Built-in Recovery Delay : 0ms, 55ms, 220ms, 450ms Options**
- **Low Functional Supply Voltage 0.9V**
- **CMOS Push-Pull Output**
- **Small SC-82 and SOT-143 Packages**
- **RoHS Compliant and Halogen Free**

Applications

- Computers
- Controllers
- Intelligent Instruments
- Critical µP and µC Power Monitoring
- Portable/Battery-Powered Equipment

Simplified Application Circuit



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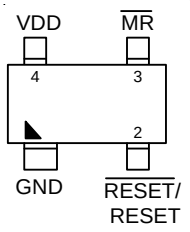
Ordering Information

RT9834 □-□□□□

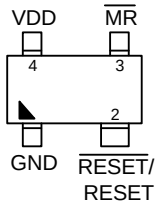
- Package Type
  - H : SOT-143
  - Y : SC-82
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- Threshold Voltage
  - 12 : 1.2V
  - 13 : 1.3V
  - :
  - 49 : 4.9V
  - 50 : 5.0V
- Reset Active Timeout Period
  - A = 0ms ($\overline{\text{RESET}}$)
  - B = 55ms ($\overline{\text{RESET}}$)
  - C = 220ms ($\overline{\text{RESET}}$)
  - D = 450ms ($\overline{\text{RESET}}$)
  - E = 0ms (RESET)
  - F = 55ms (RESET)
  - G = 220ms (RESET)
  - H = 450ms (RESET)

Pin Configuration

(TOP VIEW)



SOT-143



SC-82

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Part Status

Part No.	Status	Package Type	Lead Plating System
RT9834A-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834B-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834C-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834D-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834E-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834F-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834G-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)
RT9834H-XXGH	Lifebuy	SOT-143	G : Green (Halogen Free and Pb Free)

The part status values are defined as below :

Active : Device is in production and is recommended for new designs.

Lifebuy : The device will be discontinued, and a lifetime-buy period is in effect.

NRND : Not recommended for new designs.

Preview : Device has been announced but is not in production.

EOL : Richtek has discontinued the production of the device.

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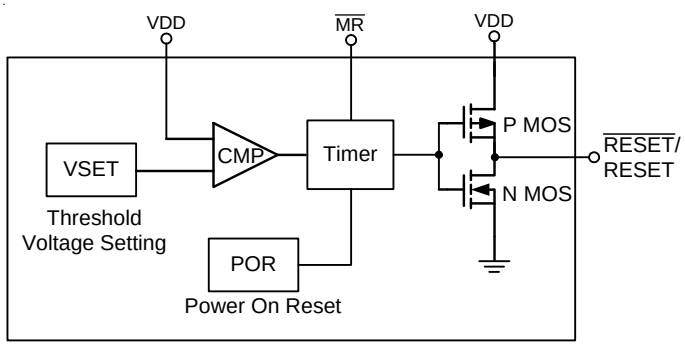
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground.
2	$\overline{\text{RESET}}$	Active Low Push-Pull Reset Output.
	RESET	Active High Push-Pull Reset Output.
3	$\overline{\text{MR}}$	Manual Reset.
4	VDD	Power.

Functional Block Diagram



Operation

When VDD is lower than threshold voltage set by VSET circuit, the RESET output becomes high. If VDD remains higher than the threshold voltage with a hysteresis voltage, Timer will be active. After a specific delay time, the RESET output becomes low. There is an internal pull-high resistor connected to the $\overline{\text{MR}}$ pin. $\overline{\text{MR}}$ resets the RT9834 only when it is pulled low. When $\overline{\text{MR}}$ releases and waits for a delay time, output returns to its normal state related to VDD. The RESET pin is a Pull-Push output, and it will pull the output high to VDD, low to Ground. Adding a pull-high resistor tied to any power which higher than VDD is forbidden.

Timer

The Timer provides four kinds of delay time options including 0ms, 55ms, 220ms, and 450ms.

VSET

The VSET generates a fixed threshold voltage.

CMP

Voltage Comparator which compares the voltage difference between threshold voltage and VDD.

POR

Power on reset. It will set all digital logic to the right state when power on.

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Absolute Maximum Ratings (Note 1)

- Terminal Voltage (with Respect to GND)
  V_{DD} ---------- –0.3V to 6V
- All Other Inputs ---------- –0.3V to (V_{DD} + 0 .3V)
- Input Current, I_{VDD} ---------- 20mA
- Power Dissipation, P_D @ T_A = 25°C
  SOT-143 ---------- 0.44W
  SC-82 ---------- 0.29W
- Package Thermal Resistance (Note 2)
  SOT-143, θ_{JA} ---------- 228.1°C/W
  SC-82, θ_{JA} ---------- 345.6°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 125°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating V_{DD} (V_{OUT}) Range		V_{DD}	RT9834A/B/C/D	0.9	--	6	V
			RT9834E/F/G/H	1.1	--	6	
Supply Current		I_{DD}	V_{TH} = 3V, V_{DD} = 4.5V	--	3	8	μA
Reset Threshold		V_{TH}		--	1.2 to 5	--	V
Threshold Voltage Accuracy		ΔV_{TH}		–1.5	--	1.5	%
Threshold Voltage Hysteresis		V_{HYS}		--	0.01 V_{TH}	--	V
V_{DD} Drop to Reset Delay		t_{RD}	Drop = V_{TH} –125mV	--	20	--	μs
Reset Active Timeout Period	RT9834A/E	t_{RP}	$V_{DD} \geq 1.02 \times V_{TH}$	--	0	--	ms
	RT9834B/F			35	55	75	
	RT9834C/G			143	220	297	
	RT9834D/H			292	450	608	
$\overline{\text{RESET}}$ Output Voltage Low		V_{OL}	$V_{DD} < V_{TH(MIN)}$, I_{SINK} = 3.5mA, $V_{TH} \geq$ 3V	--	--	0.4	V
			$V_{DD} < V_{TH(MIN)}$, I_{SINK} = 1.2mA, $V_{TH} \geq$ 1.8V	--	--	0.3	
			$V_{TH(MIN)} > V_{DD} >$ 1V, I_{SINK} = 0.5mA	--	--	0.3	

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ Output Voltage High		V_{OH}	$V_{DD} > V_{TH(MAX)}$, I_{SOURCE} = 800μA, $V_{TH} \geq 3V$	V_{DD} – 1.5	--	--	V
			$V_{DD} > V_{TH(MAX)}$, I_{SOURCE} = 500μA, $V_{TH} \geq 1.8V$	0.8 V_{DD}	--	--	
			$V_{DD} > V_{TH(MAX)}$, I_{SOURCE} = 200μA, $V_{TH} \geq 1.1V$	0.8 V_{DD}	--	--	
RESET Output Voltage Low		V_{OL}	$V_{DD} > V_{TH(MAX)}$, I_{SINK} = 3.5mA, $V_{TH} \geq 3V$	--	--	0.4	V
			$V_{DD} > V_{TH(MAX)}$, I_{SINK} = 1.2mA, $V_{TH} \geq 1.8V$	--	--	0.3	
			$V_{DD} > V_{TH(MAX)}$, I_{SINK} = 0.5mA, $V_{TH} \geq 1.2V$	--	--	0.3	
RESET Output Voltage High		V_{OH}	1.1V < V_{DD} < $V_{TH(MIN)}$, I_{SOURCE} = 200μA	0.8 V_{DD}	--	--	V
			1.8V < V_{DD} < $V_{TH(MIN)}$, I_{SOURCE} = 500μA	0.8 V_{DD}	--	--	
			3V < V_{DD} < $V_{TH(MIN)}$, I_{SOURCE} = 800μA	V_{DD} – 1.5	--	--	
$\overline{\text{MR}}$ Active Timeout Period	RT9834A/E	$t_{\overline{MR}}$		--	0	--	ms
	RT9834B/F			35	55	75	
	RT9834C/G			143	220	297	
	RT9834D/H			292	450	608	
$\overline{\text{MR}}$ Input Voltage Threshold	Logic-High	$V_{\overline{MR}\_H}$	$V_{DD} > V_{TH(MAX)}$	0.75 x V_{DD}	--	V_{DD}	V
	Logic-Low	$V_{\overline{MR}\_L}$	$V_{DD} > V_{TH(MAX)}$	--	--	0.25 x V_{DD}	

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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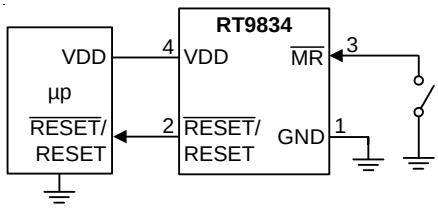
Typical Application Circuit



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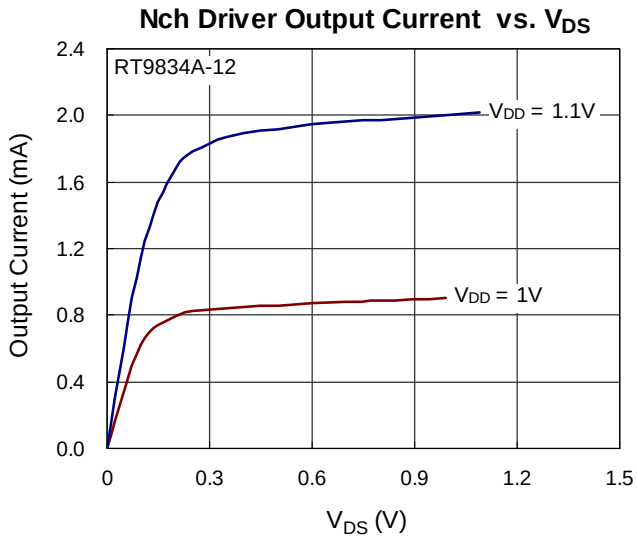
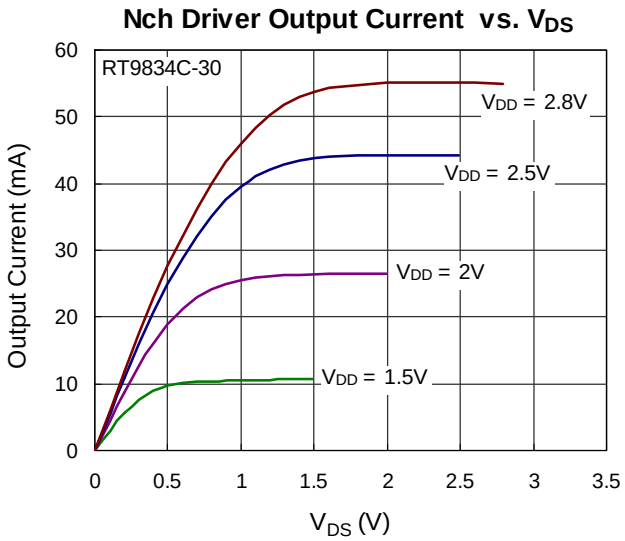
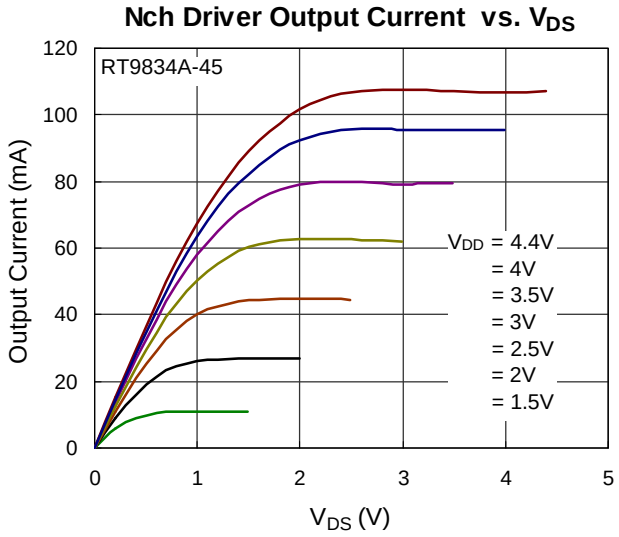
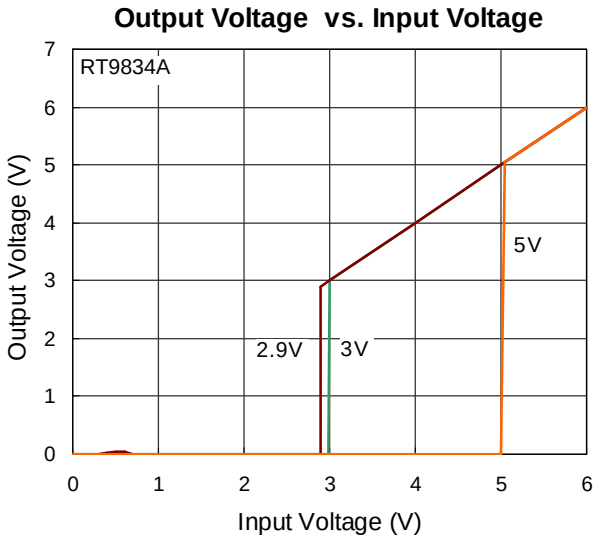
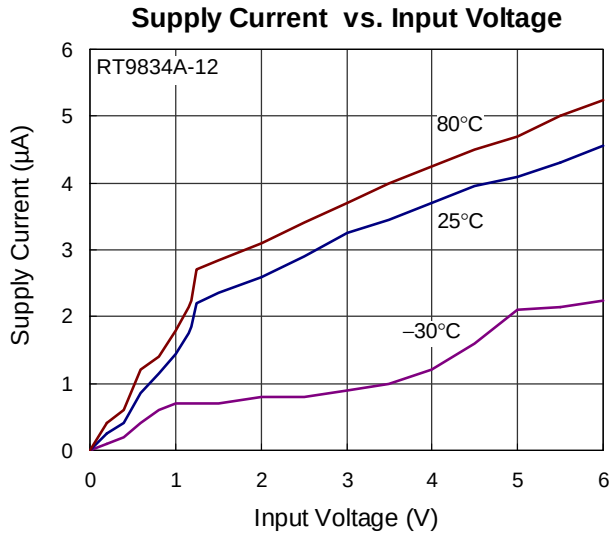
Typical Operating Characteristics

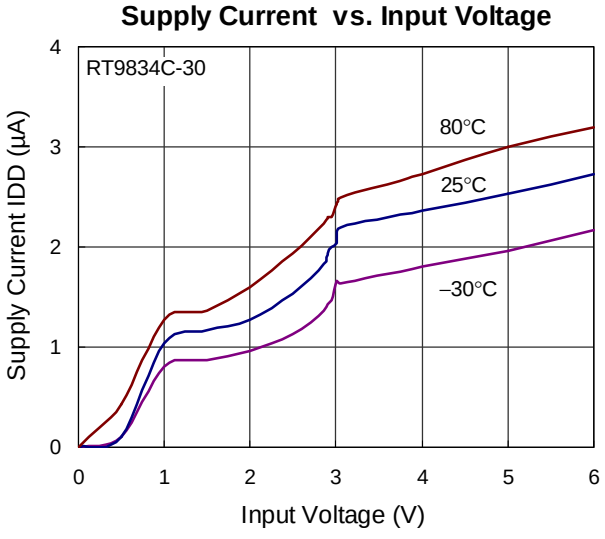












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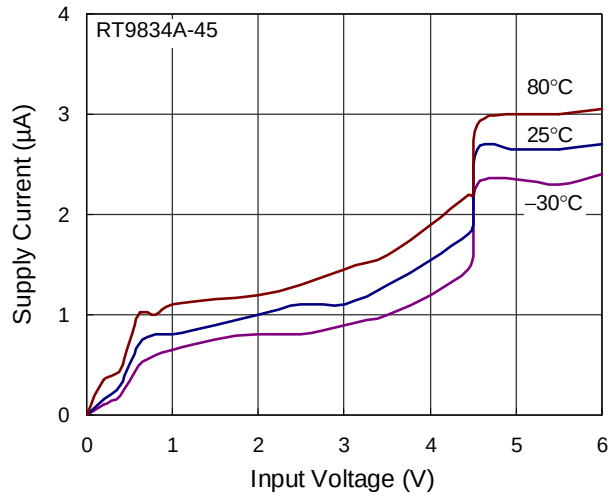
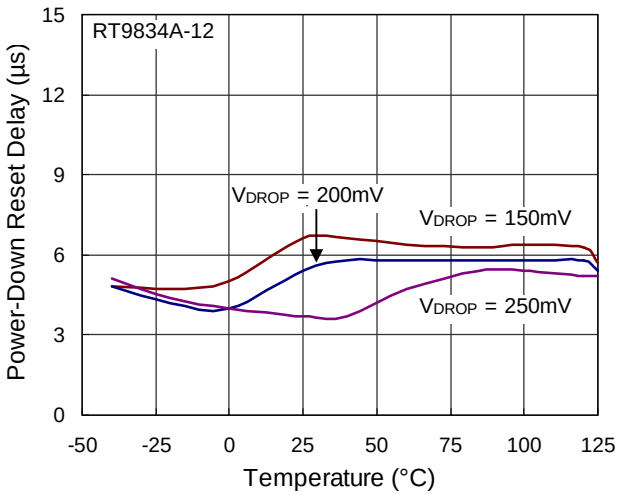
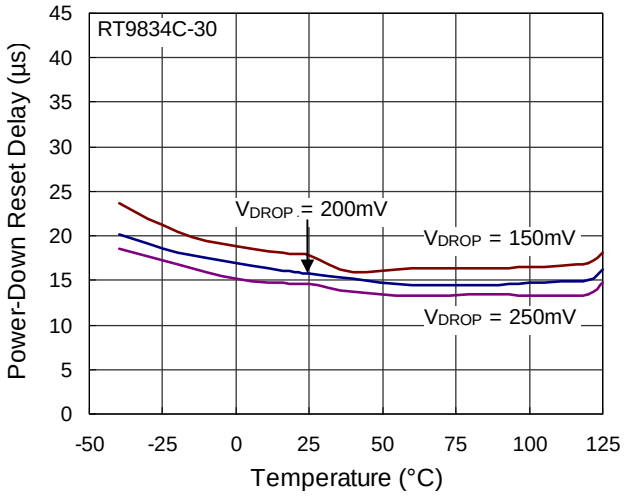
Supply Current vs. Input Voltage



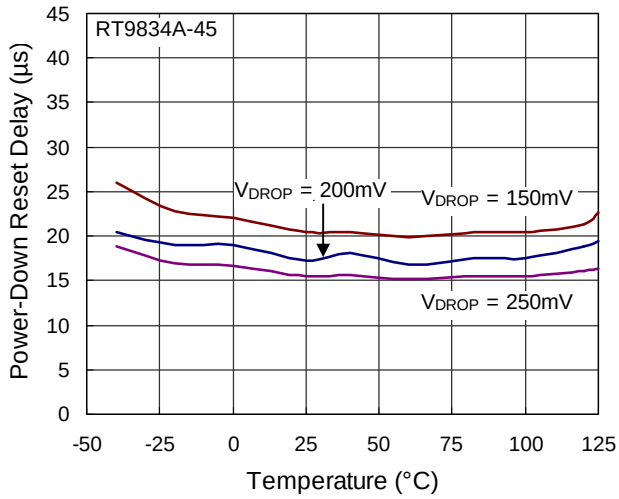
Power-Down Reset Delay vs. Temperature



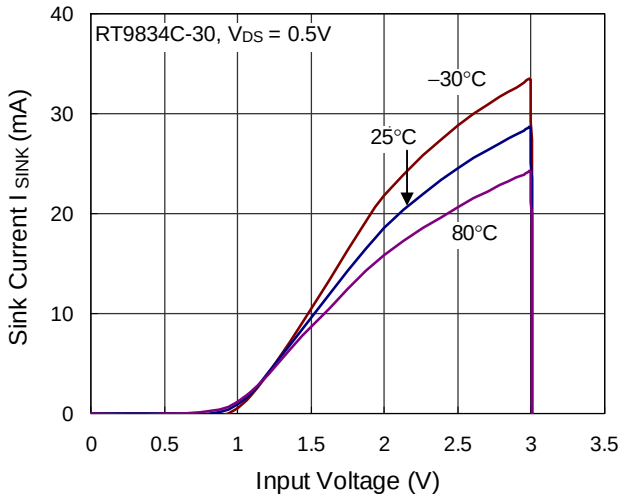
Power-Down Reset Delay vs. Temperature



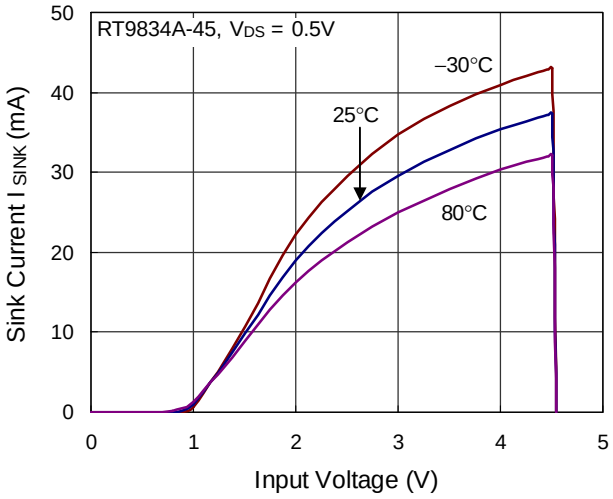
Power-Down Reset Delay vs. Temperature



Nch Driver Sink Current vs. Input Voltage



Nch Driver Sink Current vs. Input Voltage



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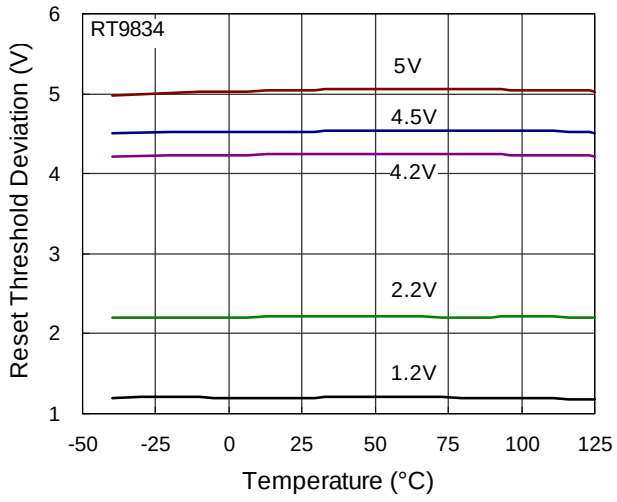
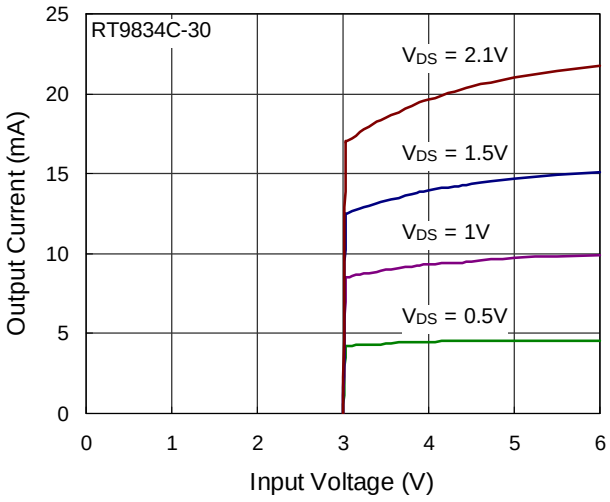
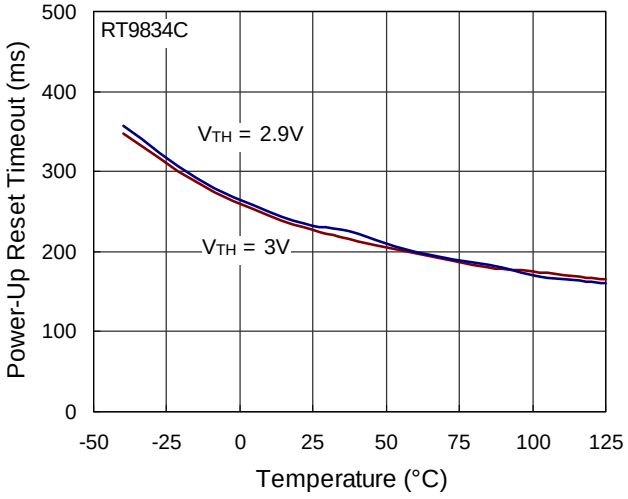
Reset Threshold Deviation vs. Temperature



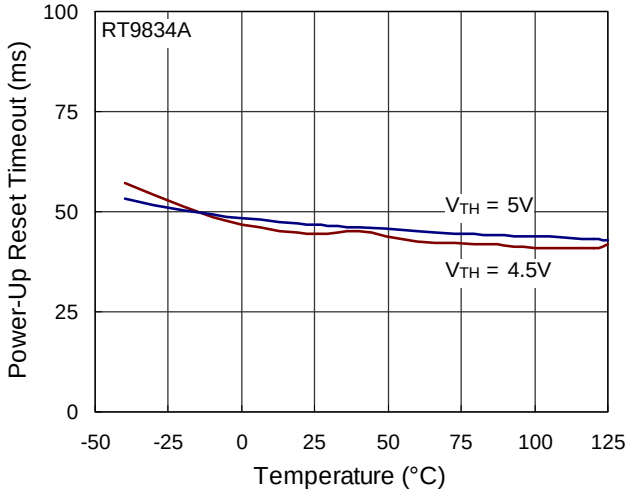
Pch Driver Output Current vs. Input Voltage



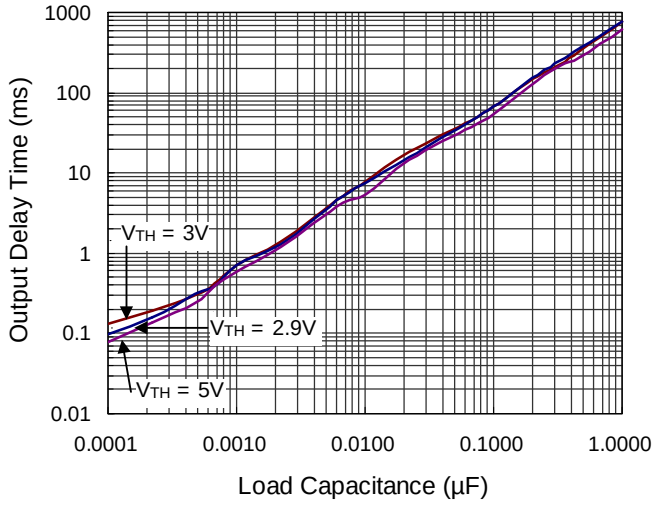
Power-Up Reset Timeout vs. Temperature



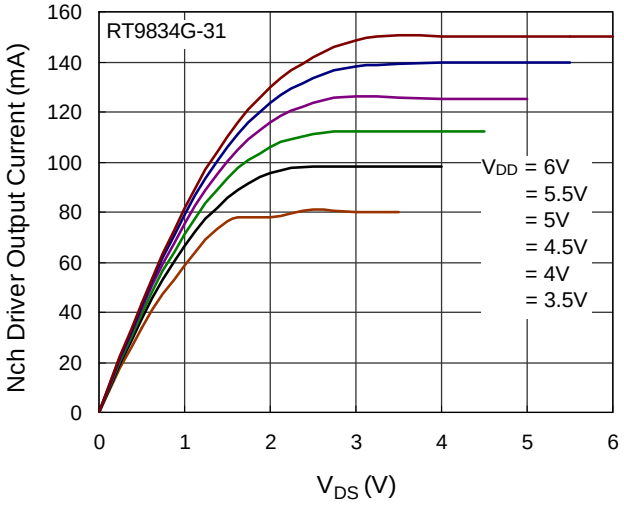
Power-Up Reset Timeout vs. Temperature



Output Delay Time vs. Load Capacitance



Nch Driver Output Current vs. V_{DS}



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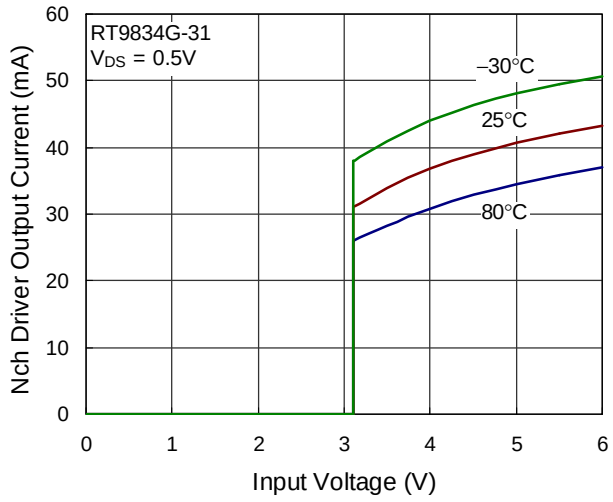
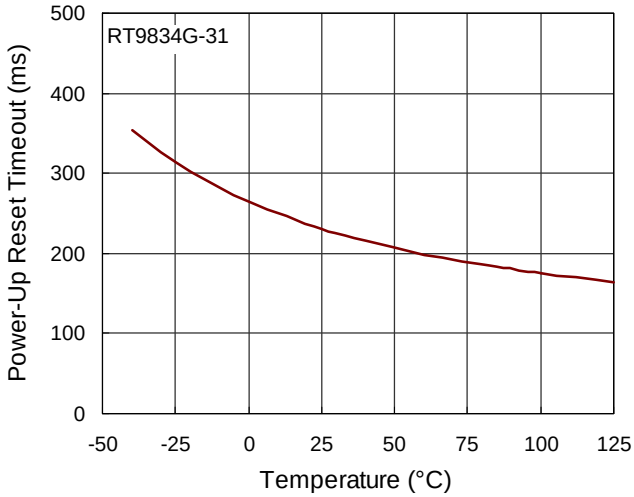
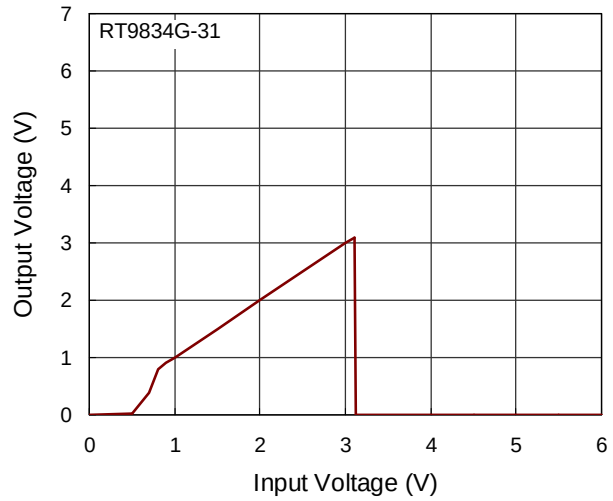
Nch Driver Output Current vs. Input Voltage



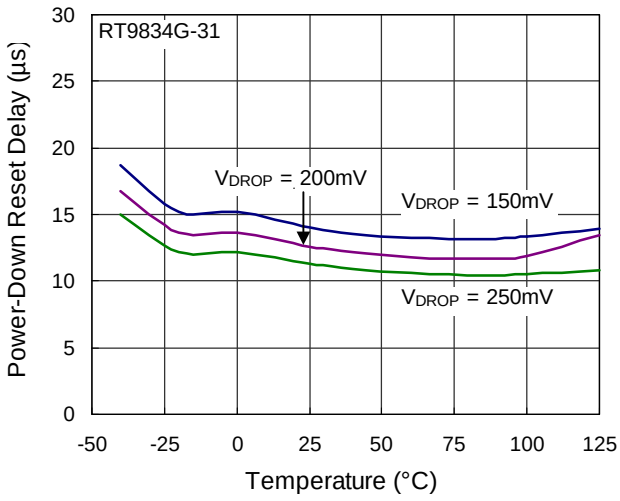
Power-Up Reset Timeout vs. Temperature



Output Voltage vs. Input Voltage



Power-Down Reset Delay vs. Temperature



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Application Information

Operation Timing Diagram

The VDD and $\overline{\text{RESET}}$ voltage rising and falling of the IC can be explained in five steps as Figure 1.

1. $\overline{\text{RESET}}$ voltage is pulled up to VDD voltage.
2. When the VDD voltage is down to the detector threshold voltage (Point A), $\overline{\text{RESET}}$ voltage becomes low level.
3. When the VDD voltage is lower than the minimum operating voltage, the $\overline{\text{RESET}}$ voltage is indefinite. In this case, the $\overline{\text{RESET}}$ voltage will stay at low level.
4. $\overline{\text{RESET}}$ voltage keeps in low level.
5. When the VDD voltage exceeds the threshold voltage (Point B). The $\overline{\text{RESET}}$ voltage will go high after a delay time.

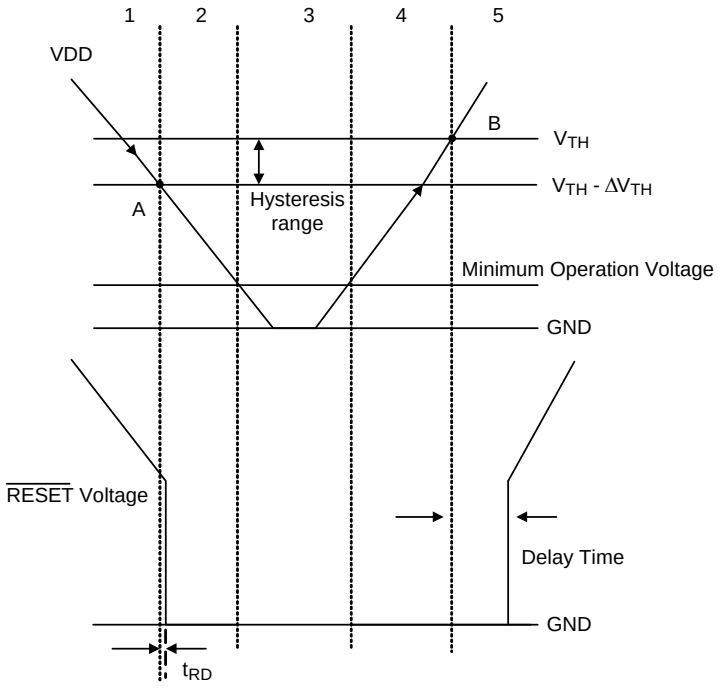

Figure 1. Operation Timing Diagram

Manual Reset Control

Many processor based products require manual reset capability, allowing the user or external logic circuitry to initiate a reset. A logic low on MR asserts reset. Reset remains asserted while MR is low and for the reset timeout period after MR returns high. Connect a normally open momentary switch from MR to ground to create a manual reset function.

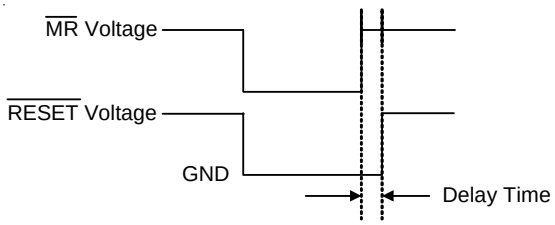

Figure 2. Manual Reset Control

Benefits of Highly Accurate Reset Threshold

Most µP supervisor ICs have reset threshold voltages between 1% and 1.5% below the value of nominal supply voltages. This ensures a reset will not occur within 1% of the nominal supply, but will occur when the supply is 1.5% below nominal.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-143 package, the thermal resistance, θ_{JA}, is 228.1°C/W on a standard JEDEC 51-7 four-layer thermal test board.

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SC-82 package, the thermal resistance, θ_{JA}, is 345.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (228.1°C/W) = 0.44W for SOT-143 package

$P_{D(MAX)}$ = (125°C – 25°C) / (345.6°C/W) = 0.29W for SC-82 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

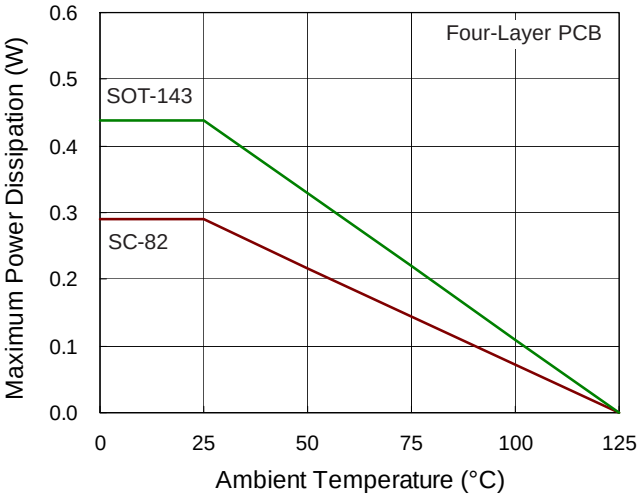

Figure 3. Derating Curve of Maximum Power Dissipation

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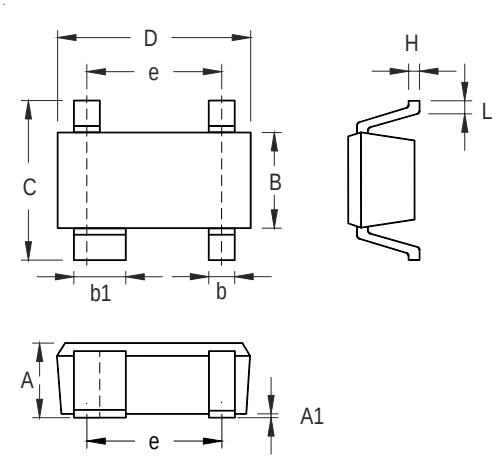
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.050	0.150	0.002	0.006
B	1.200	1.400	0.047	0.055
b	0.300	0.520	0.012	0.020
b1	0.760	0.920	0.030	0.036
C	2.100	2.640	0.083	0.104
D	2.800	3.040	0.110	0.120
e	1.900		0.075	
H	0.080	0.150	0.003	0.006
L	0.210	0.410	0.008	0.016

SOT-143 Surface Mount Package

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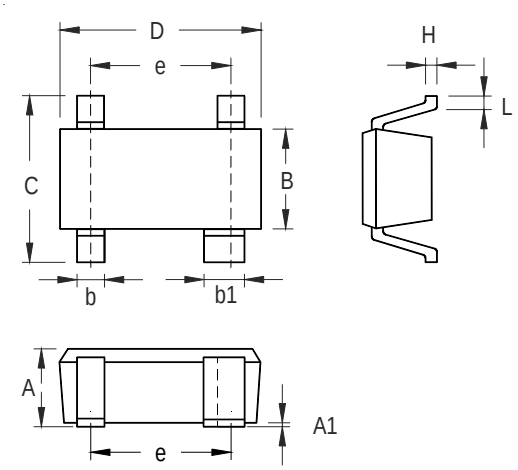

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.043
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.053
b	0.150	0.400	0.006	0.016
b1	0.350	0.500	0.014	0.020
C	1.800	2.450	0.071	0.096
D	1.800	2.200	0.071	0.087
e	1.300		0.051	
H	0.080	0.260	0.003	0.010
L	0.200	0.460	0.008	0.018

SC-82 Surface Mount Package

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Datasheet Revision History

Version	Date	Description	Item
04	2023/6/21	Modify	Part Status on P2

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