PWM Duty Generator with Adjustable Duty Setting

General Description

The RT9832 is a PWM duty generator with adjustable duty setting. The PWM frequency is fixed 0.5Hz typically. The duty cycle can be set by an external resistor between the RSET and GND pins. When the RSET pin is floating, the duty cycle is set at 50% typically. An open drain output is provided and it can be pulled up to a suitable voltage level with a pull-up resistor.

The device operates over a wide input voltage range from 2.8V to 20V. An active-low enable control pin is used to reduce shutdown current to 3.5μA. Input UVLO and thermal shutdown are provided. The RT9832 is available in the WL-CSP-6B 0.8x1.2 (BSC) package.

Ordering Information

RT9832 □

└Package Type

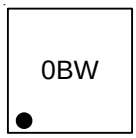
WSC : WL-CSP-6B 0.8x1.2 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



0B : Product Code

W : Date Code

Features

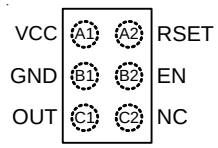
- **Input Voltage Range : 2.8V to 20V**
- **0.5Hz PWM Frequency**
- **EN Pin with Internal Pull-Low Resistor**
- **Open Drain Output**
- **Adjustable PWM Duty from 1% to 100%**
- **Input Under Voltage Lockout**
- **Thermal Shutdown Protection**
- **Shutdown Current : <3.5μA**
- **6-Ball WL-CSP Package**
- **RoHS Compliant and Halogen Free**

Applications

- Cellular Phones
- Digital Cameras
- Probable Instruments

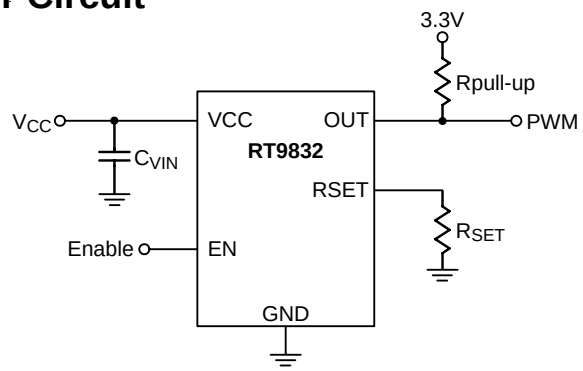
Pin Configurations

(TOP VIEW)



WL-CSP-6B 0.8x1.2 (BSC)

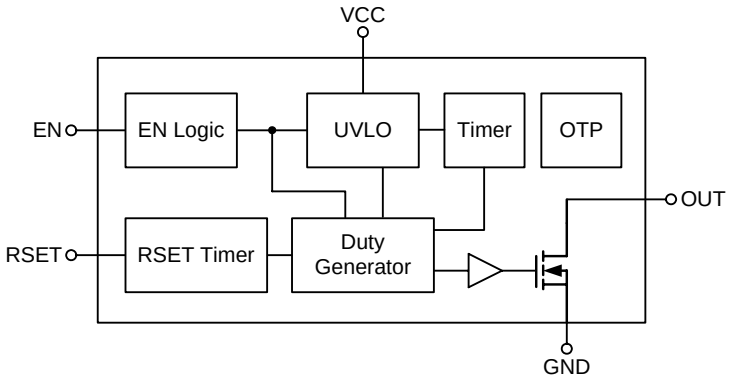
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	VCC	Supply Voltage Input. Connect a 0.47μF or larger ceramic capacitor from VCC to ground as close as possible to the VCC pin.
A2	RSET	Duty Set Pin. Connect an external resistor to set PWM duty. When the RSET pin is floating, the PWM duty cycle is equal to 50% (typ.).
B1	GND	Ground.
B2	EN	Enable Control Input (Active Low).
C1	OUT	Open Drain Output. Connect a pull-up resistor from this pin to VCC or a suitable supply.
C2	NC	No Internal Connection.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 22V
- Output Voltage, OUT ---------- –0.3V to 22V
- EN, RSET ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-6B 0.8x1.2 (BSC) ---------- 0.68W
- Package Thermal Resistance (Note 2)
  WL-CSP-6B 0.8x1.2 (BSC), θ_{JA} ---------- 148°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.8V to 20V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 4V, C_{IN} = 0.47µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Supply Current	I_{VCC}	V_{CC} = 5V, EN = Low, R_{SET} = 500kΩ	--	1	2	mA
UVLO Threshold	V_{UVLO}	V_{CC} Falling	--	2.5	--	V
UVLO Hysteresis	ΔV_{UVLO}		--	100	--	mV
VCC Shutdown Current	I_{SHDN}	V_{CC} = 5V, EN = High	--	3.5	--	µA
Duty Generator						
RSET Voltage	V_{SET}		0.833	0.85	0.867	V
PWM Frequency	f_{PWM}		0.45	0.5	0.55	Hz
Minimum Duty Cycle	D_{MIN}		1	--	--	%
Duty Cycle	Duty		--	R_{SET} / 10k	--	%
Duty Cycle Accuracy	D_{ACC}	R_{SET} = 50kΩ to 1000kΩ	–10	--	10	%
Output						
OUT Current Sink Ability	I_{SINK}	V_{CC} ≥ 4V, V_{OUT} = 0.1V	10	--	40	mA
OUT Leakage Current	I_{LEAK}	V_{CC} = 5V, EN = High, V_{OUT} = 5V	–0.1	--	0.1	µA
Protection Function						
Thermal Shutdown	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Control							
EN Voltage	Logic-High	V_{IH}		1.2	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	
EN Pull Low Resistance		R_{EN}		--	200	--	kΩ

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

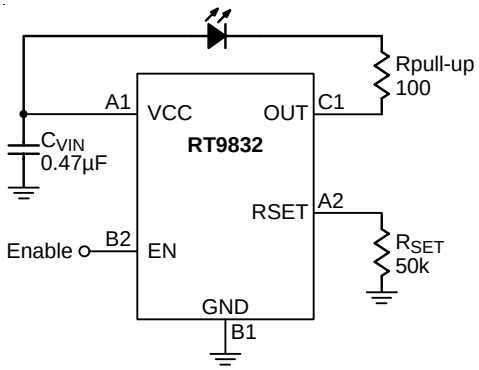
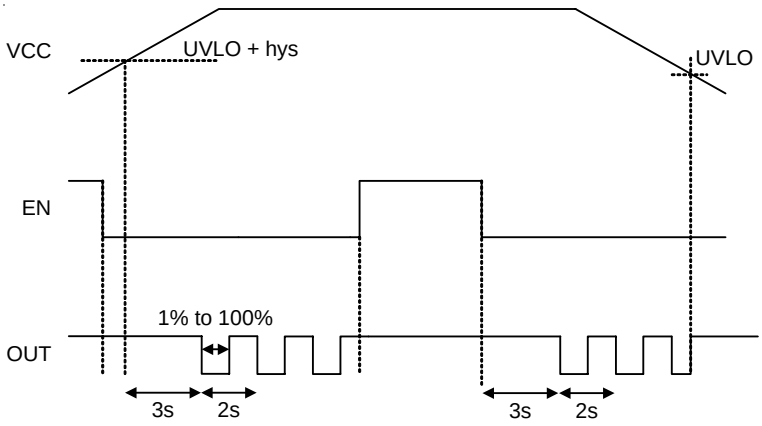


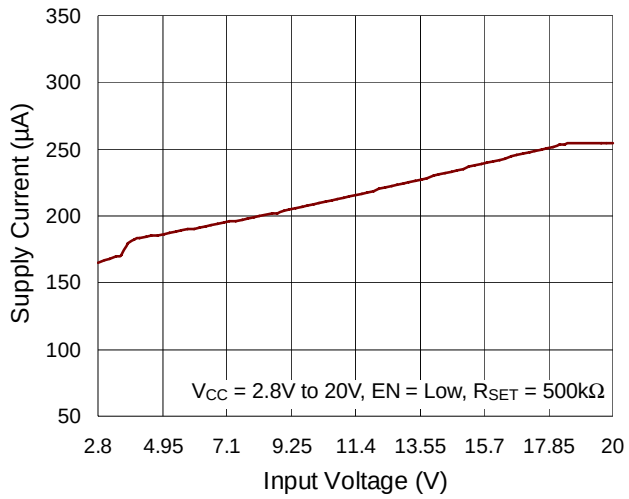
Figure 1. WLED Indicator

Timing Diagram

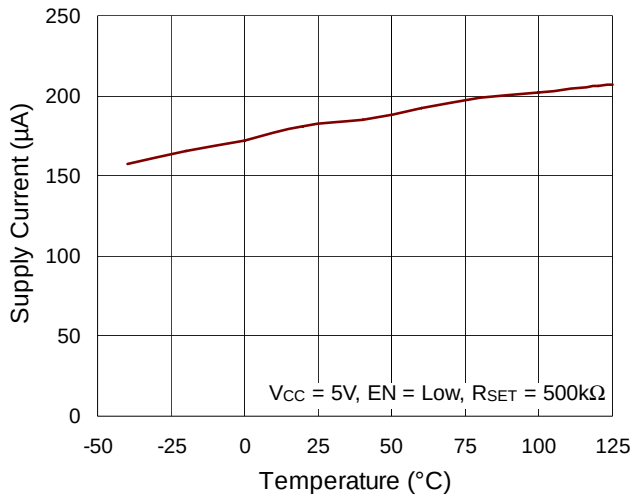


Typical Operating Characteristics

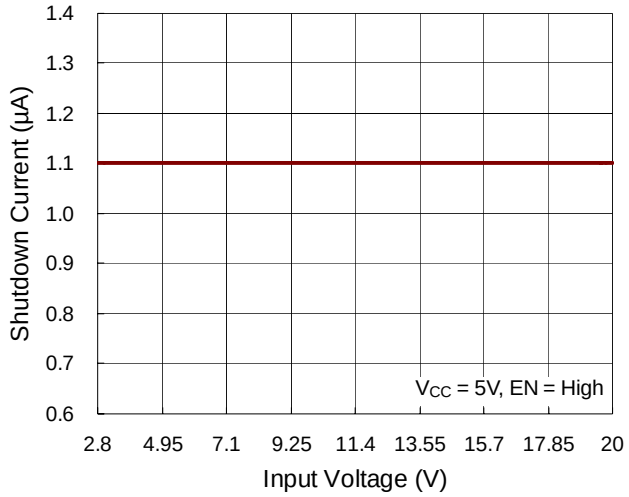
Supply Current vs. Input Voltage



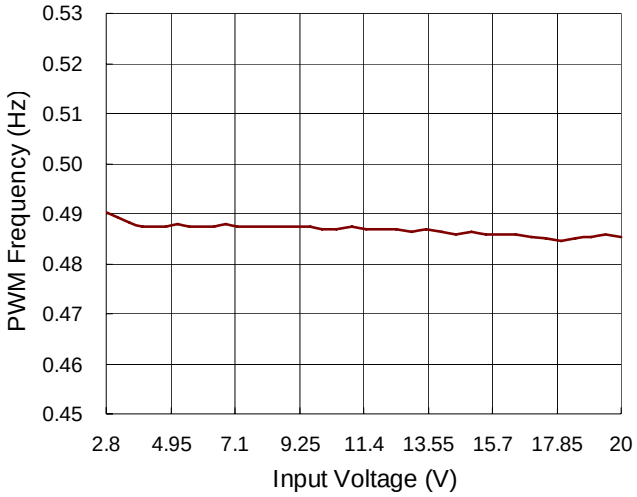
Supply Current vs. Temperature



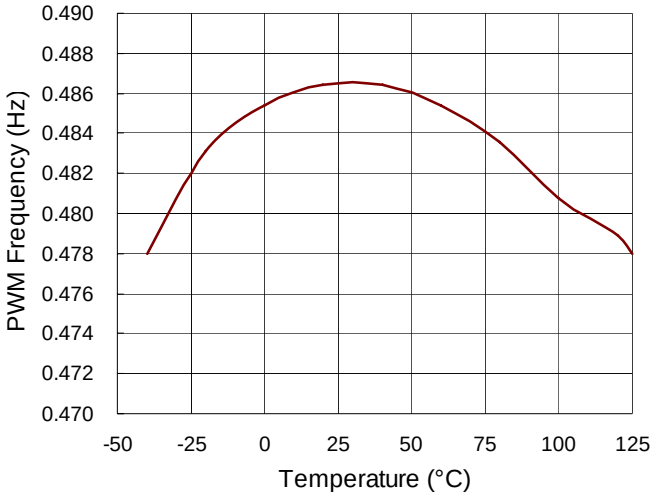
Shutdown Current vs. Input Voltage



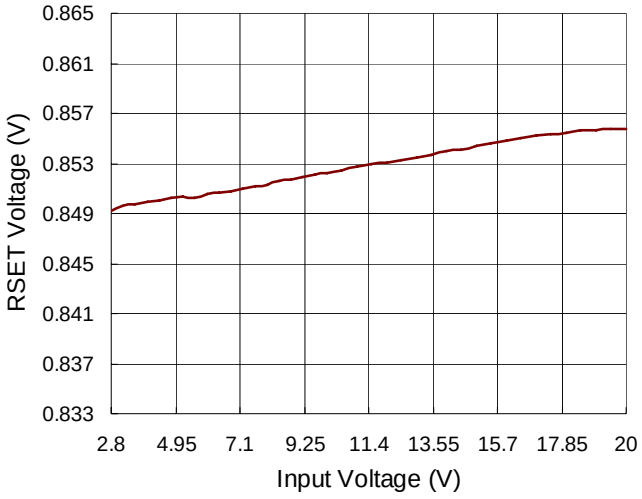
PWM Frequency vs. Input Voltage



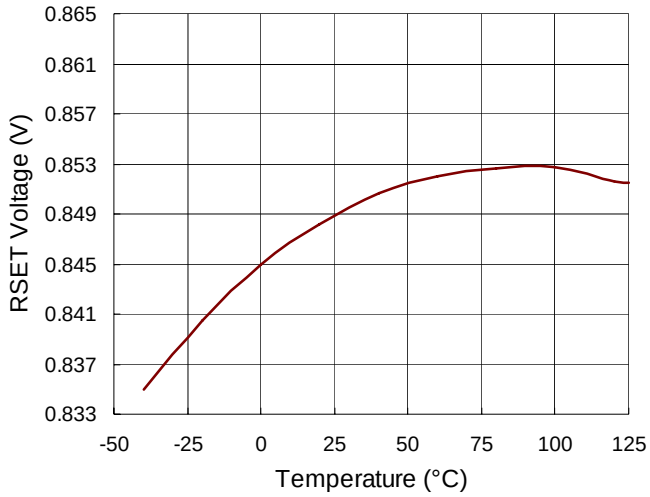
PWM Frequency vs. Temperature



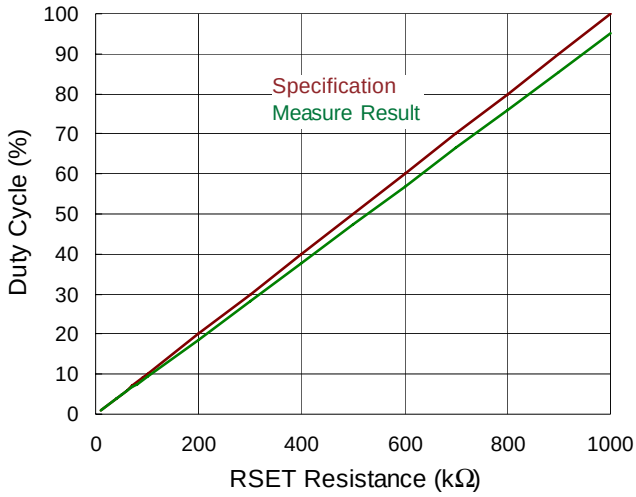
RSET Voltage vs. Input Voltage



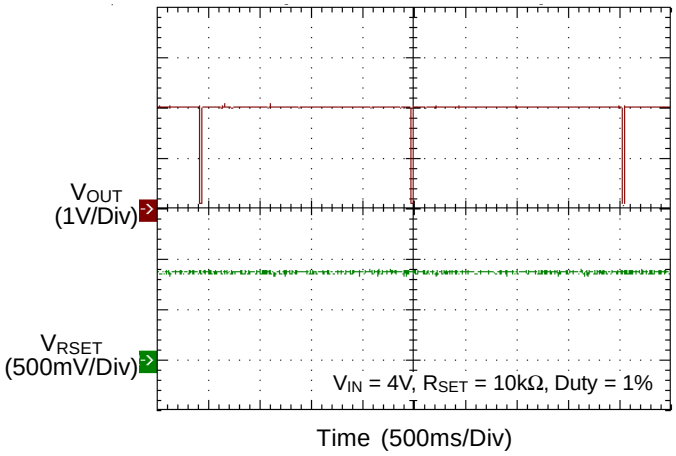
RSET Voltage vs. Temperature



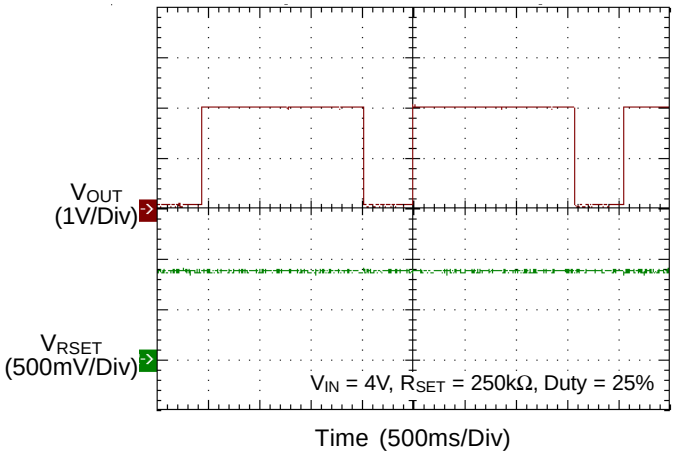
Duty Cycle vs. RSET Resistance



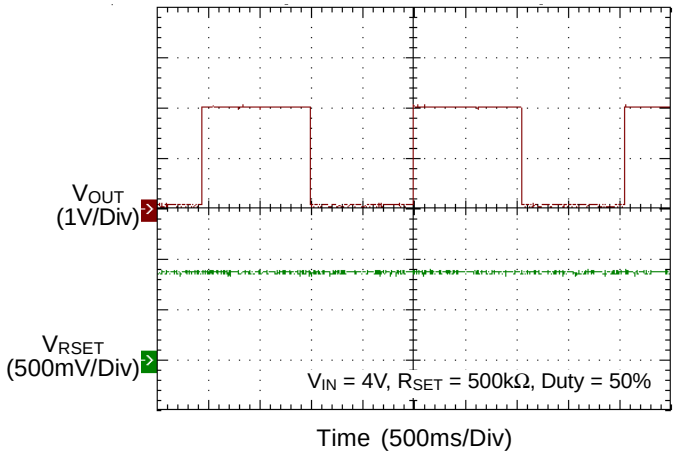
Duty Cycle



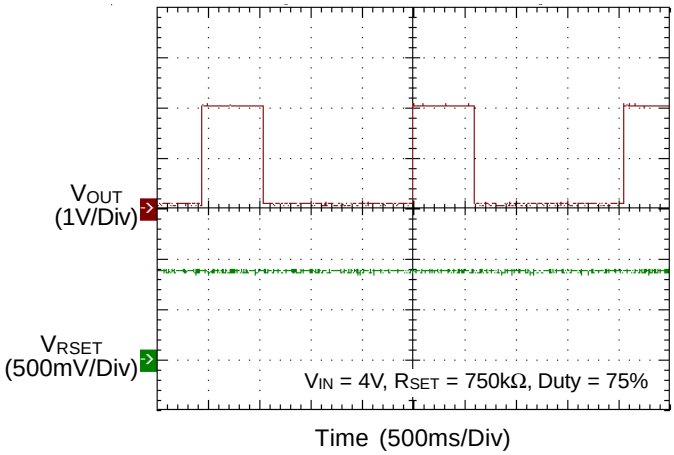
Duty Cycle



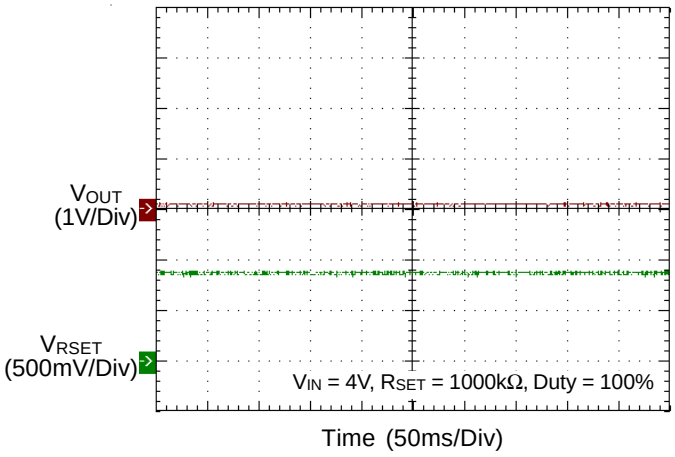
Duty Cycle



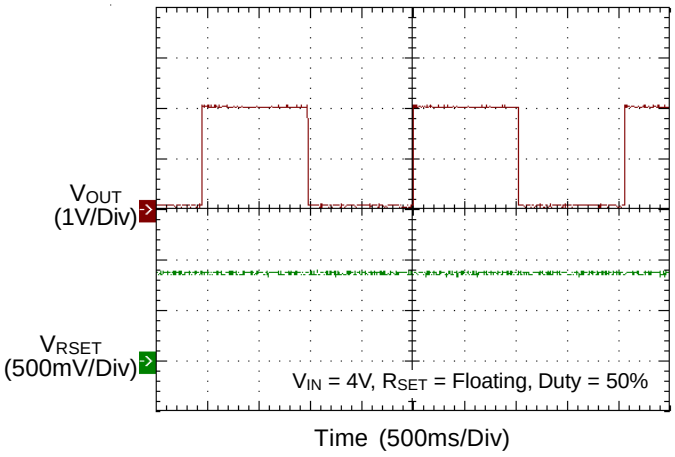
Duty Cycle



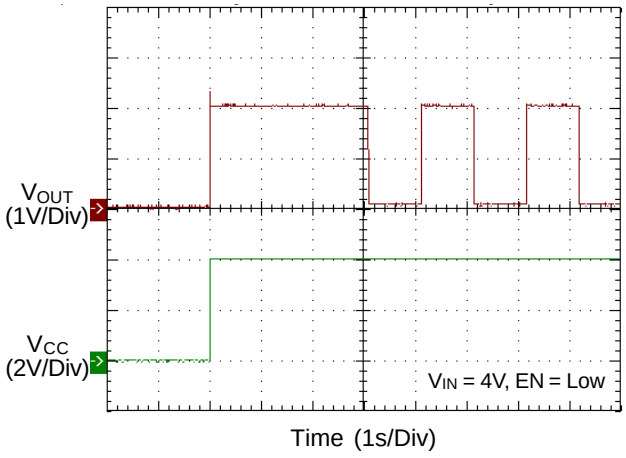
Duty Cycle



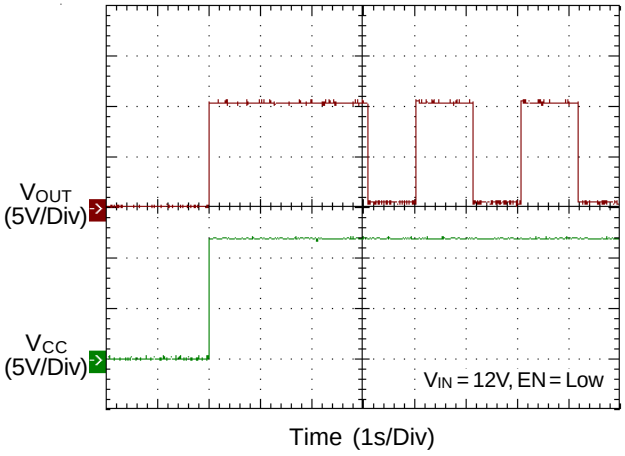
Duty Cycle



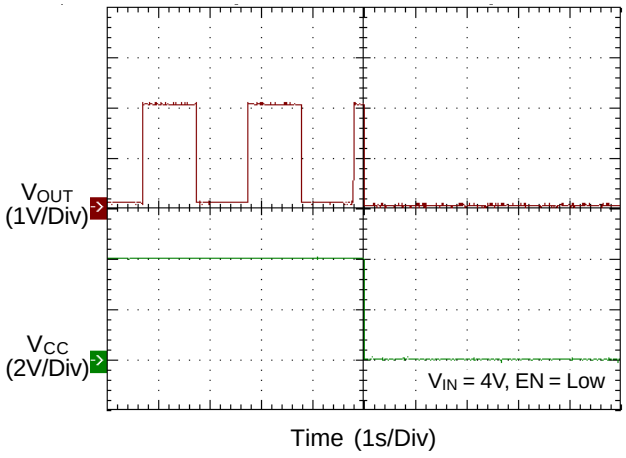
Power On from VCC



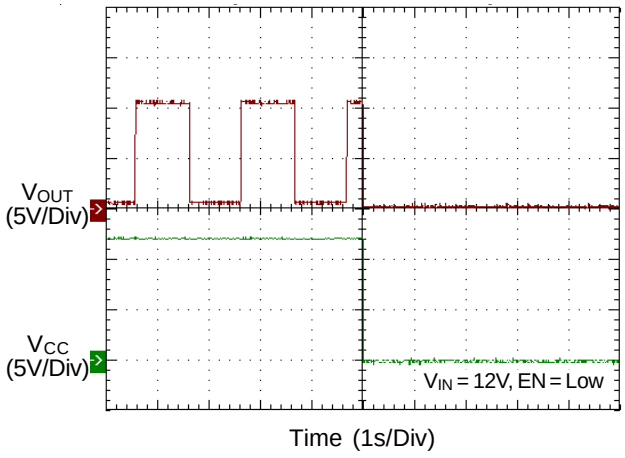
Power On from VCC



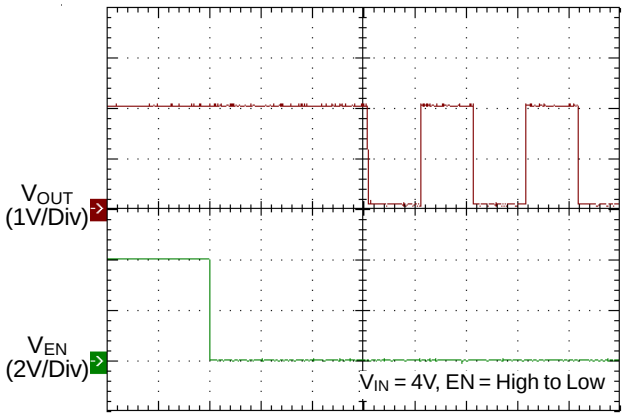
Power Off from VCC



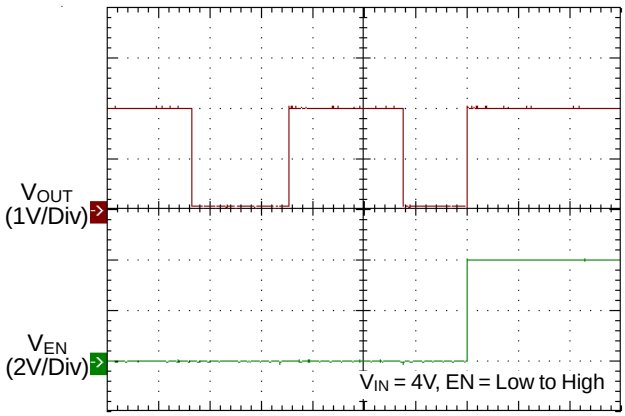
Power Off from VCC



Duty On from EN



Duty Off from EN



Application Information

The RT9832 is a PWM duty generator with adjustable duty setting. The PWM frequency is fixed 0.5Hz typically. The device operates over a wide input voltage range from 2.8V to 20V.

Capacitor Selection

Input ceramic capacitor of 0.47µF is recommended for the RT9832. For better voltage filtering, ceramic capacitors with low ESR are recommended. X5R and X7R types are suitable because of their wider voltage and temperature ranges.

UVLO/OTP

As the input voltage is lower than a specified value, the chip will enter protection mode to prevent abnormal function. As the die temperature is higher then 160°C, the chip will also enter protection mode. The output will be turned off during protection mode to prevent abnormal operation.

Duty Cycle Setting

The duty cycle is set by an external resistor on RSET pin, and the PWM duty is adjustable from 1% to 100%, according to following equation :

$$\text{Duty Cycle} = \frac{R_{SET}}{10k\Omega}$$

When the RSET is floating, the duty cycle is set at 50% typically.

Enable

The RT9832 enable is an active low logic signal control for output. The enable pin is pulled to low with internal resistors. When enable logic is low, a PWM duty will be on; when enable logic is high, a PWM duty will be off.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-6B 0.8x1.2 (BSC) package, the thermal resistance, θ_{JA}, is 148°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (148°C/W) = 0.68W for WL-CSP-6B 0.8x1.2 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

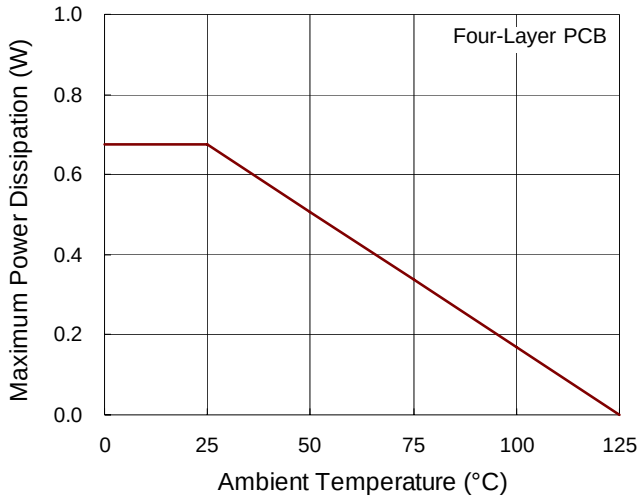


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Consideration

For best performance of the RT9832, the following guidelines must be strictly followed.

- Input capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.
- The GND should be connected to a strong ground plane for heat sinking and noise protection.
- Keep the main current traces as possible as short and wide.

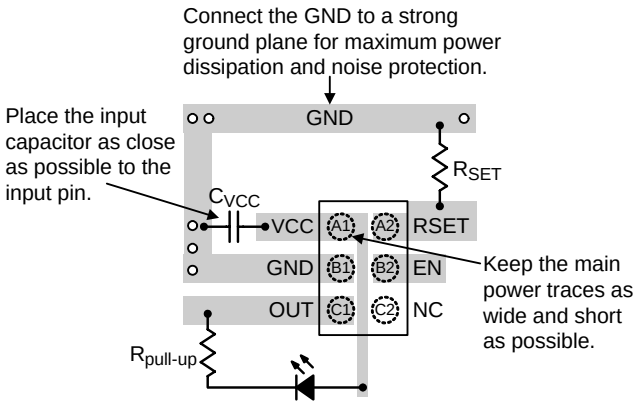
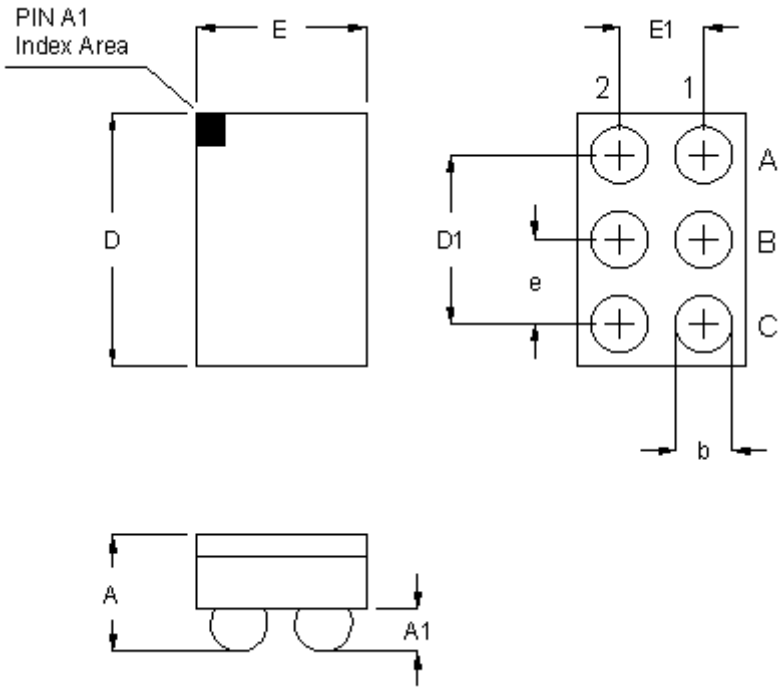


Figure 3. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.150	1.250	0.045	0.049
D1	0.800		0.031	
E	0.750	0.850	0.030	0.033
E1	0.400		0.016	
e	0.400		0.016	

6B WL-CSP 0.8x1.2 Package (BSC)

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