RICHTEK®

RT9758D

High Voltage Cap Divider Converter with Bypass Function

1 General Description

The RT9758D is a high efficiency switching capacitor converter for input >7.4V application. The efficiency is up to 98.1% when V_{OUT} = 10V, I_{OUT} = 2A, switching frequency = 500kHz, dual phase with VBUS input in cap divider mode. The device integrates two phase switching capacitor topology (DIV2 mode), bypass mode, an input reverse blocking MOS and 9-way protections. The default operation mode of the device is DIV2 mode. User can use I^2C to select the device operating in bypass mode or reverse DIV2 mode or reverse bypass mode. The maximum output current is 6A with DIV2 mode or 5A with bypass mode. In present mode ($\overline{EN}$ = H), the host can still issue commands by the I^2C serial interface.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Applications

- Smart Phones
- Tablet
- PC

3 Ordering Information

RT9758D □

└Package Type(1)

WSC: WL-CSP-36B 2.74x2.84 (BSC)

Note 1.

Marked with (1) indicated: Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

4 Marking Information

3M: Product Code
YMDAN: Date Code

5 Features

- **Integrated Bidirectional Bypass Mode and Cap Divider Mode (DIV2 Mode)**
- **Input Reverse Blocking NFET between WRX_IN Pin and VBUS Pin**
  - **Block the Reverse Current**
- **Dual-Phase Charge Pump Core**
  - **6A Output Current Ability with DIV2 Mode and 5A with Bypass Mode**
  - **Efficiency Up to 98.1% when V_{OUT} = 10V, I_{OUT} = 2A, Switching Frequency = 500kHz and Dual Phase with VBUS Input in DIV2 Mode**
  - **300kHz to 1.5MHz Variable Switching Frequency Stay Out of Audio Band**
  - **Spread Spectrum Technology for EMI Reduction**
  - **Adjustable Single-Phase or Dual-Phase for DIV2 Mode**
  - **Programmable Pre-Charge Current and Pre-Charge Timing for Charge Soft-Start**
  - **Support Converter Soft-Start with 500mA Loading**
- **Support Synchronize Function for Parallel Application**
- **Operation Mode Transfer Automatically between Bypass Mode and DIV2 Mode (AT_Function)**
- **I^2C is Available when Device in Present Mode**
- **3-Error Charge Pump Switch Protection**
  - **VBUS Voltage Too Low Error Protection before Switch (VBUS_LOW_ERR)**
  - **CFLY Short Error Protection Before Switch (CFLY_DIAG)**
  - **Converter Overcurrent Protection (CON_OCP)**
- **6-Way System Protection**
  - **VBUS Overvoltage Protection (VBUS_OVP)**
  - **IBUS Overcurrent Protection (IBUS_OCP)**
  - **VOUT Overvoltage Protection (VOUT_OVP)**
  - **WRX Reverse Overcurrent Protection (WRX_IRE_OCP)**
  - **VOUT Short Error Protection Before Charge (VOUT_ERR)**
  - **Junction Over-Temperature Protection (TDIE_OTP)**

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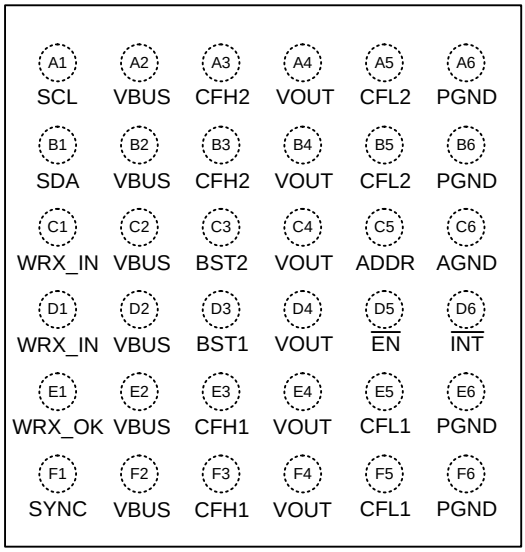
6 Pin Configuration

(TOP VIEW)



WL-CSP-36B 2.74x2.84 (BSC)

7 Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1	SCL	DI	I^2C serial clock line. Connect to 1.8V/3.3V pull-up voltage via 10kΩ pull-up resistor.
A2, B2, C2, D2, E2, F2	VBUS	P	These pins are the input power supply and must be connected together on the PCB. Two 4.7μF capacitors must be connected to VBUS and GND.
A3, B3	CFH2	P	Flying capacitor positive node. Two 22μF capacitors must be connected to CFL2 and CFH2 and placed as close as possible to the device. These pins must be connected together on the PCB.
A4, B4, C4, D4, E4, F4	VOUT	P	Power supply. Connect to positive terminal of the battery pack or the input of the next stage charger IC. Must be connected together on the PCB. One 22μF capacitor must be connected to VOUT and GND.
A5, B5	CFL2	P	Flying capacitor negative node. Two 22μF capacitors must be connected to CFL2 and CFH2 and placed as close as possible to the device. These pins must be connected together on the PCB.
A6, B6, E6, F6	PGND	P	Power ground pin.
B1	SDA	DIO	I^2C serial data line. Connect to 1.8V/3.3V pull-up voltage via 10kΩ pull-up resistor.
C1, D1	WRX_IN	P	Connect to wireless power receiver output. One 2.2μF capacitor must be connected to WRX_IN and GND.
C3	BST2	P	Charge pump for gate drive. Connect a 22nF capacitor between BST2 and CFH2.
C5	ADDR	DI	Provide different voltage level at ADDR and GND to assign address of the device.
C6	AGND	P	Analog ground pin.

Pin No.	Pin Name	I/O	Pin Function
D3	BST1	P	Charge pump for gate drive. Connect a 22nF capacitor between BST1 and CFH1.
D5	$\overline{EN}$	DI	Device enable control pin. Pull high to disable device. I^2C is still available when the $\overline{EN}$ pin is pulled high.
D6	$\overline{INT}$	DO	Open drain interrupt output. Connect to pull-up voltage via 10kΩ pull-up resistor. Normally high, when an event happens, the $\overline{INT}$ pin sends a 256μs low pulse to system.
E1	WRX_OK	P	Push-pull structure. When WRX_IN is higher than WRX_INSERT level, this pin will pull high to inform system.
E3, F3	CFH1	P	Flying capacitor positive node. Two 22μF capacitors must be connected to CFL1 and CFH1 and placed as close as possible to the device. These pins must be connected together on the PCB.
E5, F5	CFL1	P	Flying capacitor negative node. Two 22μF capacitors must be connected to CFL1 and CFH1 and placed as close as possible to the device. These pins must be connected together on the PCB.
F1	SYNC	AIO	Push-pull structure. The sync pin of the master device is connected to the sync pin of the slave device. Leave the pin floating in standalone mode.

8 Typical Application Circuit

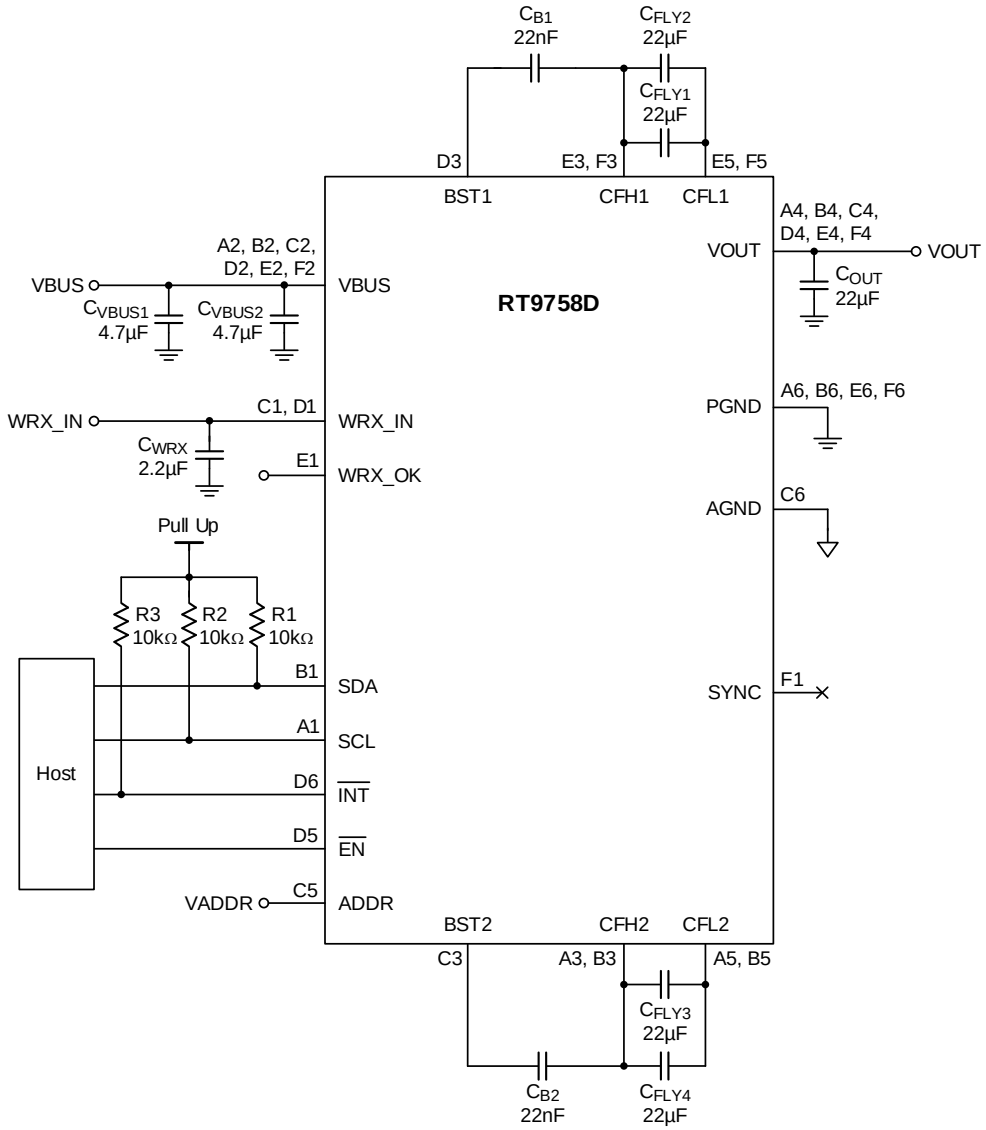
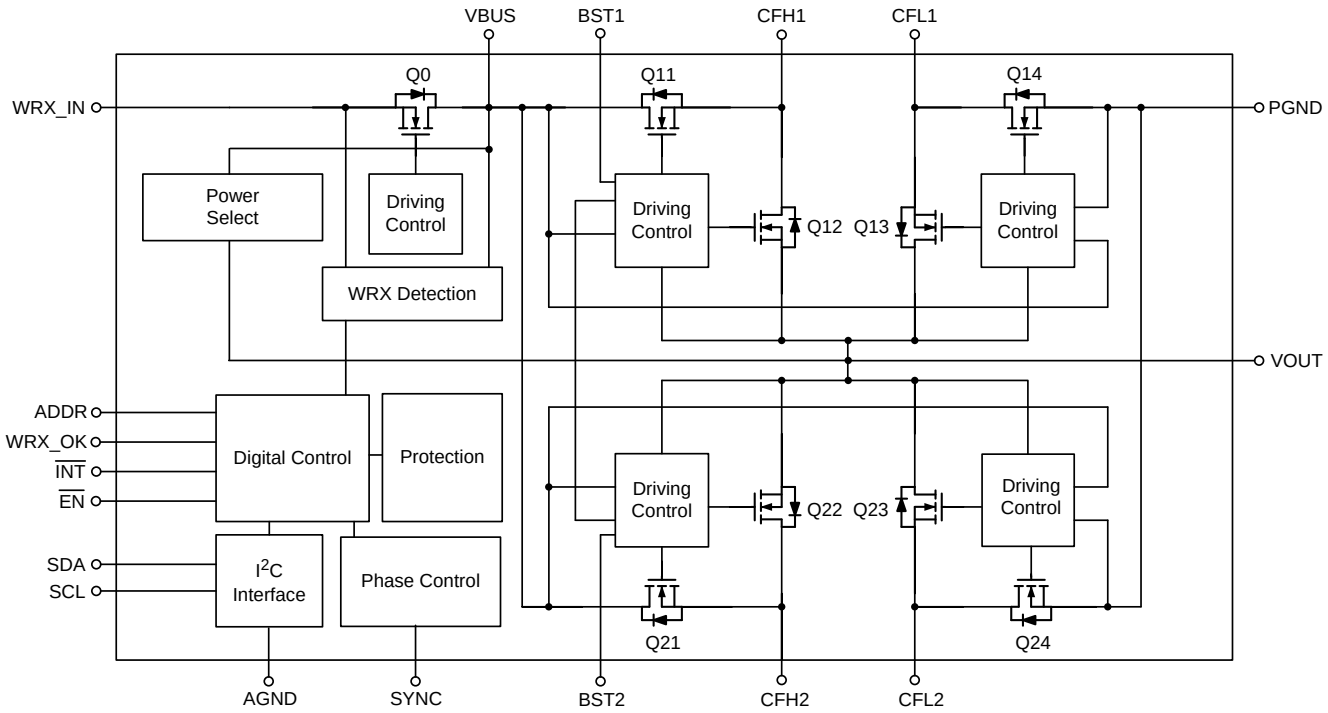


Table 1. BOM List

Name	Part Number	Description	Package	Manufacturer
C_{VBUS1}, C_{VBUS2}	GRM188R6YA475KE15	CAP, CERM, 4.7µF, 35V, ±10%, X5R	0603	MuRata
C_{WRX_IN}	GRM155R6YA225ME11	CAP, CERM, 2.2µF, 35V, ±20%, X5R	0402	MuRata
C_{FLY1}, C_{FLY2}, C_{FLY3}, C_{FLY4},	GRM21BR61E226ME44	CAP, CERM, 22µF, 25V, ±20%, X5R	0805	MuRata
C_{OUT}	GRM21BR61E226ME44	CAP, CERM, 22µF, 25V, ±20%, X5R	0805	MuRata
C_{B1}, C_{B2}	GRM033R61C223KE84	CAP, CERM, 22nF, 16V, ±10%, X5R	0201	MuRata
R1, R2, R3	CRCW040210K0JNED	RES, 10k, 5%, 0.063W	0402	Vishay-Dale

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Pin Voltage, WRX_IN ---------- –1.4V to 28V
- Supply Pin Voltage, VBUS ---------- –1.4V to 28V
- Supply Pin Voltage, VOUT ---------- –1.4V to 16.5V
- Terminal Pin Voltage, BST1, BST2 ---------- –0.3V to 34V
- Terminal Pin Voltage, CFH1, CFH2 ---------- –0.3V to 24V
- Terminal Pin Voltage, CFL1, CFL2 ---------- –0.3V to 16.5V
- Differential Pin Voltage, VBUS to WRX_IN ----------–0.3V to 28V
- Differential Pin Voltage, BST to CFH ----------–1V to 24V
- Terminal Pin Voltage, SDA, SCL, $\overline{INT}$, $\overline{EN}$ ---------- –0.3V to 6V
- Terminal Pin Voltage, ADDR, SYNC, WRX_OK ---------- –0.3V to 6V
- Terminal Pin Current, $\overline{INT}$ ---------- 0mA to 6mA
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-36B 2.74x2.84 (BSC) ---------- 2.88W
- Package Thermal Resistance (Note 3)

  WL-CSP-36B 2.74x2.84 (BSC), θ_{JA} ---------- 34.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model), per ANSI/ESDA/JEDEC JS-001 ---------- ±2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage Range, WRX_IN, VBUS (Bypass Mode) ---------- 4V to 13V
- Supply Input Voltage Range, WRX_IN, VBUS (DIV2 Mode) ---------- 7.4V to 21V
- Output Voltage Range, VOUT (Reverse Bypass Mode) ---------- 4V to 13V
- Output Voltage Range, VOUT (Reverse DIV2 Mode) ---------- 3.7V to 10.5V
- Positive flying capacitor Voltage Range, CFH1, CFH2 ---------- 0V to 21V
- Negative flying capacitor Voltage Range, CFL1, CFL2 ---------- 0V to 10.5V
- Analog Voltage Range, ADDR, SYNC, WRX_OK ---------- 0V to 5V
- I/O Control Voltage Range, SDA, SCL, $\overline{INT}$, $\overline{EN}$ ---------- 0V to 5V

- Charger Current Range, IOUT (DIV2 Mode) ---------- 0A to 6A
- Charger Current Range, IOUT (BYPASS Mode) ---------- 0A to 5A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Select and Source						
VBUS Quiescent Current	$I_{BUS\_IQ\_PRESENT}$	$\overline{EN}$ = 1.8V, VBUS = 5.5V, VOUT = 0V, WRX_IN = 0V, Q0 turn off, all pull-down resistors disable, WDT disable	--	15	22	μA
	$I_{BUS\_IQ\_STANDBY}$	$\overline{EN}$ = 0V, VBUS = 5.5V, VOUT = 0V, WRX_IN = 0V, Q0 turn off, all pull-down resistors disable, WDT disable, CHG_EN = 0	--	--	300	μA
	$I_{BUS\_IQ\_DIV2}$	$\overline{EN}$ = 0V, VBUS = 20V, VOUT = 0V, WRX_IN = 0V, Q0 turn off, all pull-down resistors disable, WDT disable, CHG_EN = 1, in DIV2 mode (Note 6)	--	--	12	mA
	$I_{BUS\_IQ\_BYPASS}$	$\overline{EN}$ = 0V, VBUS = 5.5V, VOUT = 0V, WRX_IN = 0V, Q0 turn off, all pull-down resistors disable, WDT disable, CHG_EN = 1, in bypass mode	--	1.65	--	mA
WRX_IN Quiescent Current	$I_{WRX\_IN\_IQ\_PRESENT}$	$\overline{EN}$ = 1.8V, WRX_IN = 5.5V, VOUT = 0V, Q0 turn on, all of pull-down resistor disable, WDT disable	--	15	22	μA
	$I_{WRX\_IN\_IQ\_STANDBY}$	$\overline{EN}$ = 0V, WRX_IN = 5.5V, VOUT = 0V, Q0 turn on, all pull-down resistors disable, WDT disable, CHG_EN = 0	--	--	450	μA
	$I_{WRX\_IN\_IQ\_DIV2}$	$\overline{EN}$ = 0V, WRX_IN = 20V, VOUT = 0V, Q0 turn on, all pull-down resistors disable, WDT disable, CHG_EN = 1, in DIV2 mode (Note 6)	-	--	12	mA
	$I_{WRX\_IN\_IQ\_BYPASS}$	$\overline{EN}$ = 0V, WRX_IN = 5.5V, VOUT = 0V, Q0 turn on, all pull-down resistors disable, WDT disable, CHG_EN = 1, in Bypass mode	--	1.65	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Quiescent Current	$I_{OUT\_IQ\_PRESENT}$	$\overline{EN}$ = 1.8V, VOUT = 7.4V, WRX_IN = 0V, Q0 turn off, all pull-down resistors disable, WDT disable	--	15	22	μA
	$I_{OUT\_IQ\_STANDBY}$	$\overline{EN}$ = 0V, VOUT = 7.4V, WRX_IN = 0V, Q0 turn off, all pull-down resistors disable, WDT disable, CHG_EN = 0	--	--	300	μA
VDDA UVLO Threshold	$V_{DDA\_UVLO\_TH}$	V_{DDA} rising, $\overline{EN}$ = 0V	--	2.6	--	V
VDDA UVLO Hysteresis	$V_{DDA\_UVLO\_HY}$	V_{DDA} falling, $\overline{EN}$ = 0V	--	0.6	--	V
WRX_IN Insert Threshold	$V_{WRX\_IN\_INSERT\_TH}$	WRX_IN rising	3	3.1	3.2	V
WRX_IN Insert Threshold Deglitch Time	$t_{WRX\_IN\_INSERT\_DEG}$		--	3	--	μs
WRX_IN Insert Hysteresis	$V_{WRX\_IN\_INSERT\_HY}$	WRX_IN falling	50	150	250	mV
VBUS Insert Threshold	$V_{BUS\_INSERT\_TH}$	V_{BUS} rising	3	3.1	3.2	V
VBUS Insert Threshold Deglitch Time	$t_{VBUS\_INSERT\_DEG}$		--	3	--	μs
VBUS Insert Hysteresis	$V_{BUS\_INSERT\_HY}$	V_{BUS} falling	50	150	250	mV
VOUT Insert Threshold	$V_{OUT\_INSERT\_TH}$	V_{OUT} rising	3.3	3.5	3.7	V
VOUT Insert Threshold Deglitch Time	$t_{VOUT\_INSERT\_DEG}$		--	3	--	μs
VOUT Insert Hysteresis	$V_{OUT\_INSERT\_HY}$	V_{OUT} falling	180	200	235	mV
Cap Divider and Bypass Mode On-Resistance						
Q0 RON	R_{Q0}	WRX_IN = 3.1V to 21V, Charge enable	--	25	35	mΩ
Q11, Q21 RON	R_{Q11}, R_{Q21}	VOUT = 3.5V to 10.5V, in DIV2 mode	--	35	49	mΩ
Q12, Q22 RON	R_{Q12}, R_{Q22}	VOUT = 3.5V to 10.5V, in DIV2 mode	--	25	35	mΩ
Q13, Q23 RON	R_{Q13}, R_{Q23}	VOUT = 3.5V to 10.5V, in DIV2 mode	--	25	35	mΩ
Q14, Q24 RON	R_{Q14}, R_{Q24}	VOUT = 3.5V to 10.5V, in DIV2 mode	--	25	35	mΩ
Bypass RON	(R_{Q11} + R_{Q12}), (R_{Q21} + R_{Q22})	VOUT = 3.5V to 14V, in Bypass mode	--	30	40	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Frequency						
Charge Switch Frequency	f_{SW}	Select by register 0x0F[5:3] = 111	1350	1500	1650	kHz
		Select by register 0x0F[5:3] = 110 (Note 6)	900	1000	1100	
		Select by register 0x0F[5:3] = 011	765	900	1035	
		Select by register 0x0F[5:3] = 101 (Note 6)	675	750	825	
		Select by register 0x0F[5:3] = 010 (Note 6)	510	600	690	
		Select by register 0x0F[5:3] = 100, default	450	500	550	
		Select by register 0x0F[5:3] = 001 (Note 6)	382.5	450	517.5	
		Select by register 0x0F[5:3] = 000	255	300	345	
Protection						
VOUT OVP Range	$V_{OUT\_OVP\_RAN}$	Rising	7	--	14	V
VOUT OVP Step Size	$V_{OUT\_OVP\_SIZE}$		--	1	--	V
VOUT OVP Accuracy	$V_{OUT\_OVP\_ACC}$		–1.5	--	1.5	%
VOUT OVP Deglitch Time	$t_{VOUT\_OVP\_DEG}$		--	4	--	µs
WRX_IRE OCP Range	$I_{WRX\_IRE\_OCP\_RAN}$	Rising	1	--	6	A
WRX_IRE OCP Step Size	$I_{WRX\_IRE\_OCP\_SIZE}$		--	500	--	mA
WRX_IRE OCP Accuracy	$I_{WRX\_IRE\_OCP\_ACC}$	$I_{WRX\_IRE\_OCP}$ = 1A to 4A	–5	--	5	%
		$I_{WRX\_IRE\_OCP}$ = 4.5A to 6A (Note 6)	–10	--	10	
WRX_IRE OCP Deglitch Time	$t_{WRX\_IRE\_OCP\_DEG}$		--	50	--	µs
VBUS OVP Range	$V_{BUS\_OVP\_RAN}$	Rising	7.25	--	22	V
VBUS OVP Step Size	$V_{BUS\_OVP\_SIZE}$		--	250	--	mV
VBUS OVP Accuracy	$V_{BUS\_OVP\_ACC}$	V_{BUS_OVP} = 9V to 22V	–2	--	2	%
VBUS OVP Hysteresis	$V_{BUS\_OVP\_HYS}$		--	400	--	mV
VBUS OVP Reaction Time	$t_{VBUS\_OVP\_RE}$	During between VBUS over VBUS_OVP threshold and device start to turn off charger, VBUS_OVP set 1.1 times the level of VBUS (Note 6)	--	75	--	ns
IBUS OCP Range	$I_{BUS\_OCP\_RAN}$	Rising	2	--	6	A
IBUS OCP Step Size	$I_{BUS\_OCP\_SIZE}$		--	500	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBUS OCP Accuracy	$I_{BUS\_OCP\_ACC}$	In bypass mode	–10	--	10	%
		In DIV2 mode, f_{SW} = 500kHz, I_{BUS_OCP} = 2A to 3A	–15	--	15	
IBUS OCP Deglitch	$t_{IBUS\_OCP\_DEG}$		--	--	100	µs
VOUT_ERR Detect Level	t_{VOUT_ERR}	V_{BUS} = 5V, in Bypass or DIV2 mode	0.8	1	1.2	V
VOUT_ERR Off Time	$t_{VOUT\_ERR\_OFF\_TIME}$	Only active in Bypass mode, select by register 0x11[1] = 0, default	36	40	44	ms
		Only active in Bypass mode, select by register 0x11[1] = 1	72	80	88	
CFLY_DIAG Detect Level	V_{CFLY_DIAG}	Detect CFL pin voltage when CFLY pre-charge is finished in DIV2 mode or reverse DIV2 mode.	0.8	1	1.2	V
Thermal Shutdown Threshold	$T_{DIE\_OTP\_TH}$	(Note 6)	--	140	--	°C
Thermal Shutdown Hysteresis	$T_{DIE\_OTP\_HYS}$	(Note 6)	--	20	--	°C
Thermal Shutdown Deglitch Time	t_{TDIE_DEG}	Rising	--	10	--	ms
		Falling	--	160	--	
VBUS_LOW_ERR Accuracy	$V_{BUS\_LOW\_ERR\_ACC}$	$V_{BUS\_LOW\_ERR}$ = VBUS/VOUT, falling threshold for device can start reverse DIV2 mode but cannot start DIV2 mode.	1.95	1.975	2	V/V
		$V_{BUS\_LOW\_ERR}$ = VBUS/VOUT, falling threshold for device can start reverse bypass mode but cannot start bypass mode	0.98	0.99	1	
VBUS_LOW_ERR Hysteresis	$V_{BUS\_LOW\_ERR\_HYS}$	$V_{BUS\_LOW\_ERR}$ rising hysteresis for device can start DIV2 mode but cannot start reverse DIV2 mode.	--	--	0.025	V/V
		$V_{BUS\_LOW\_ERR}$ rising hysteresis for device can start bypass mode but cannot start reverse bypass mode.	--	--	0.018	
VBUS LOW ERR Deglitch	$t_{VBUS\_LOW\_ERR\_DEG}$		--	--	15	µs
Converter OCP Threshold	$I_{CON\_OCP\_TH}$	f_{SW} = 500kHz, VBUS = 10V	10.8	12	13.2	A
Function Threshold and Accuracy						
VOUT Pre-Charge Current Range	$I_{OUT\_PRE\_CHG\_RAN}$	Default = 660mA per phase	330	--	660	mA
VOUT Pre-Charge Current Accuracy	$I_{OUT\_PRE\_CHG\_ACC}$	V_{BUS} = 9.5V, in DIV2 single phase mode, PRECHARGE_ CURRENT = 660mA	–20	--	20	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Pre-Charge Timing	$t_{VOUT\_PRE\_CHG}$	Select by register 0x11[3:2] = 00	--	0.5	--	ms
		Select by register 0x11[3:2] = 01	--	1	--	
		Select by register 0x11[3:2] = 10	--	2	--	
		Select by register 0x11[3:2] = 11 (Default)	--	4	--	
CFLY Pre-Charge Current Range	$I_{CFLY\_PRE\_CHG\_RAN}$	Default = 660mA per phase	330	--	660	mA
CFLY Pre-Charge Current Accuracy	$I_{CFLY\_PRE\_CHG\_ACC}$	V_{BUS} = 9.5V, in DIV2 single phase mode, PRECHARGE_CURRENT = 660mA	–20	--	20	%
CFLY Pre-Charge Timing	$t_{CFLY\_PRE\_CHG}$	Select by register 0x11[7:6] = 00	--	0.5	--	ms
		Select by register 0x11[7:6] = 01	--	1	--	
		Select by register 0x11[7:6] = 10	--	2	--	
		Select by register 0x11[7:6] = 11 (Default)	--	4	--	
AT Function Threshold Range	$V_{AT\_FUNCTION\_RAN}$		9	--	12	V
AT Function Threshold Step Size	$V_{AT\_FUNCTION\_SIZE}$		--	0.5	--	V
AT Function Threshold Accuracy	$V_{AT\_FUNCTION\_ACC}$	Rising	–150	--	200	mV
AT Function Hysteresis	$V_{AT\_FUNCTION\_HYS}$	Falling	--	400	--	mV
AT Function Deglitch	$t_{AT\_FUNCTION\_DEG}$		8	10	12	ms
Synchronize Function						
SYNC Output High Level	V_{OH_SYNC}	VBUS = 5V to 21V, synchronize function enable, master mode	--	4.2	--	V
SYNC Output Low Level	V_{OL_SYNC}	VBUS = 5V to 21V, synchronize function enable, master mode	–0.3	--	0.3	V
SYNC Duty Cycle	D_{MAX_SYNC}	DIV2 mode, synchronize function enable, master mode (Note 6)	--	--	50	%
SYNC Frequency	f_{SW_SYNC}	f_{SW} = 500kHz, synchronize frequency is twice as switching frequency (Note 6)	900	1000	1100	kHz
SYNC Output Current Limit	I_{LIM_SYNC}	SYNC pin short, WRX_IN = 10V	--	--	42	mA
Pull Down Resistor						
VBUS Pull Down	R_{VBUS_PD}	VBUS = 5V to 12V	--	0.75	--	kΩ
WRX_IN Pull Down	$R_{WRX\_IN\_PD}$	WRX_IN = 5V to 12V	--	1	--	kΩ
VOUT Pull Down	R_{VOUT_PD}	VOUT = 5V to 12V	--	0.75	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Watchdog Time Out						
Watchdog Time Out	WDT	No I^2C communication for 3.75s, set by Register 0x0E[6:4] = 000	3	3.75	4.5	sec
		No I^2C communication for 7.5s, set by Register 0x0E[6:4] = 001	6	7.5	9	
		No I^2C communication for 11.25s, set by Register 0x0E[6:4] = 010	9	11.25	13.5	
		No I^2C communication for 15s, set by Register 0x0E[6:4] = 011	12	15	18	
		No I^2C communication for 30s, set by Register 0x0E[6:4] = 100, default	24	30	36	
		No I^2C communication for 60s, set by Register 0x0E[6:4] = 101	48	60	72	
		No I^2C communication for 90s, set by Register 0x0E[6:4] = 110	72	90	108	
		No I^2C communication for 120s, set by Register 0x0E[6:4] = 111	96	120	144	
Control Input Pin ($\overline{EN}$)						
Input High Threshold Voltage	V_{IH_EN}		1.3	--	--	V
Input Low Threshold Voltage	V_{IL_EN}		--	--	0.4	V
Input Floating Threshold Voltage	$V_{IH\_EN\_FLOATING}$	The $\overline{EN}$ pin is floating	--	1.7	--	V
Logic Output Pin ($\overline{INT}$)						
$\overline{INT}$ Pin Pull Low Time	$t_{INT\_PULL\_LOW}$		--	256	--	μs
Logic Output Pin (WRX_OK)						
WRX_OK Output High Level	$V_{OH\_WRX\_OK}$	WRX_IN > 5V, Q0 turn on	4.8	5	5.2	V
WRX_OK Output Low Level	$V_{OL\_WRX\_OK}$	WRX_IN < WRX_INSERT	–0.3	--	0.3	V
WRX_OK Output Current Limit	$I_{LIM\_WRX\_OK}$	WRX_OK pin short	--	--	42	mA
Address Detection						
Input Low Threshold for Slave Address = 0x50	$V_{IL\_ADDRESS}$		--	--	0.4	V
Input Floating Threshold for Slave Address = 0x51	$V_{IM\_ADDRESS}$	The ADDR pin is floating	--	0.9	--	V
Input High Threshold for Slave Address = 0x52	$V_{IH\_ADDRESS}$		1.3	--	--	V
Input Leakage Current	$I_{LKG\_ADDRESS}$	The ADDR pin = 0V or 1.8V	--	--	5	μA

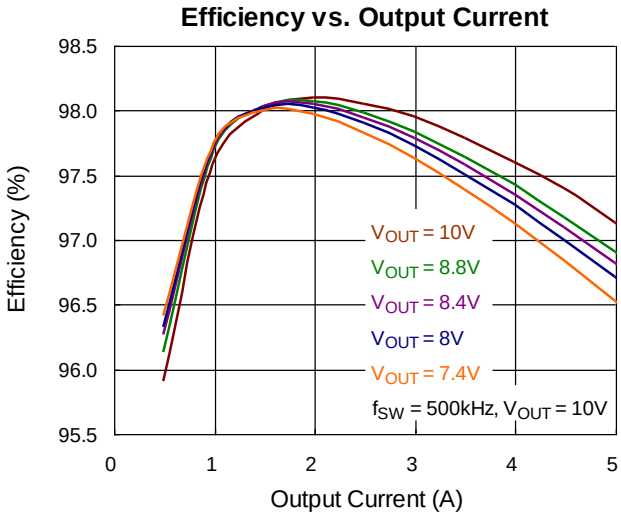
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Timing						
Device Wake Up Time	t_{WAKE_UP}	Duration time between V_{DDA} > V_{DDA_UVLO} and device can start I^2C communication	--	500	--	μs
Device into Standby Mode Time	$t_{STANDBY\_DELAY}$	Duration time from Present mode to Standby mode	--	300	--	μs
Soft-Start Time for Bypass Mode	t_{SS_BYPASS}	Timing about VOUT pre-charge to VBUS and Bypass RON fully turn on when Bypass mode is enabled with no load, Pre-charge current = 660mA, $V_{OUT\_ERR\_ON\_TIME}$ = 4msec, C_{OUT} = 22μF x 1, V_{BUS} = 5V	--	4	--	ms
Soft-Start Time for DIV2 Mode	t_{SS_DIV2}	Timing about CFLY and VOUT pre-charge to (VBUS/2) and start switching when DIV2 mode is enabled with no load, Pre-charge current = 660mA, $C_{FLY\_DIAG\_TIME}$ = 4msec, $V_{OUT\_ERR\_ON\_TIME}$ = 4msec, C_{FLY} = 22μF x 2 each phase, C_{OUT} = 22μF x 1, V_{BUS} = 10V	--	9	--	ms
Soft-Start Time for Reverse Bypass Mode	$t_{SS\_REVERSE\_BYPASS}$	Timing about Bypass RON fully turn on when Reverse Bypass mode is enabled with no load, Pre-charge current = 660mA, $V_{OUT\_ERR\_ON\_TIME}$ = 4msec, V_{OUT} = 5V	--	4	--	ms
Soft-Start Time for Reverse DIV2 Mode	$t_{SS\_REVERSE\_DIV2}$	Timing about CFLY from 0V to 5V and start switching when reverse DIV2 mode is enabled with no load, Pre-charge current = 660mA, $C_{FLY\_DIAG\_TIME}$ = 4msec, C_{FLY} = 22μF x 2 each phase, V_{OUT} = 5V	--	5	--	ms
Turn on Q0 Delay Time	t_{Q0_DELAY}	0x0D[1:0] = 10, Duration time between WRX_IN > WRX_INSERT and Q0 start to turn on	--	2	--	ms
OVP Recovery Time	$t_{OVP\_RECOVERY}$	Only active in Bypass mode with register 0x0E[7] = 1, Select by register 0x0F[7] = 0	17	21	25	ms
		Only active in Bypass mode with register 0x0E[7] = 1, Select by register 0x0F[7] = 1	80	100	120	
WRX_OK Pull Up Time	$t_{WRX\_OK\_PULL\_UP}$	VBUS > 5V, in standby mode, WRX_OK pin is floating, Duration time between WRX_IN > WRX_INSERT and WRX_OK pull to high level	--	16	--	μs

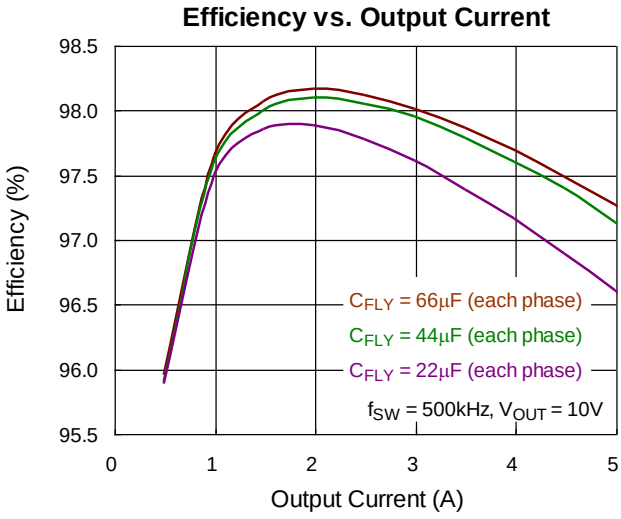
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Watchdog Reset Wait Time	t_{WDT_WAIT}		--	32	--	ms
I^2C Characteristics						
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.5	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{CLK}	Standard-mode	--	--	100	kHz
		Fast-mode	--	--	400	
		Fast-mode plus	--	--	1000	
		High-speed mode Cb = 400pF	--	--	1.7	MHz
		High-speed mode Cb = 100pF	--	--	3.4	
Bus Free Time between Stop and Start Condition	t_{BUF}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	
		High-speed mode Cb = 100pF	160	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard-mode	4.7	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Plus	0.26	--	--	
		High-speed mode Cb = 400 pF	160	--	--	ns
		High-speed mode Cb = 100 pF	160	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard-mode	0.1	--	--	ns
		Fast-mode	0.1	--	--	
		Fast-mode plus	0.1	--	--	
		High-speed mode Cb = 400pF	0.1	--	150	
		High-speed mode Cb = 100pF	0.1	--	70	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard-mode	--	--	3.45	µs
		Fast-mode	--	--	0.9	
		Fast-mode plus	--	--	0.45	

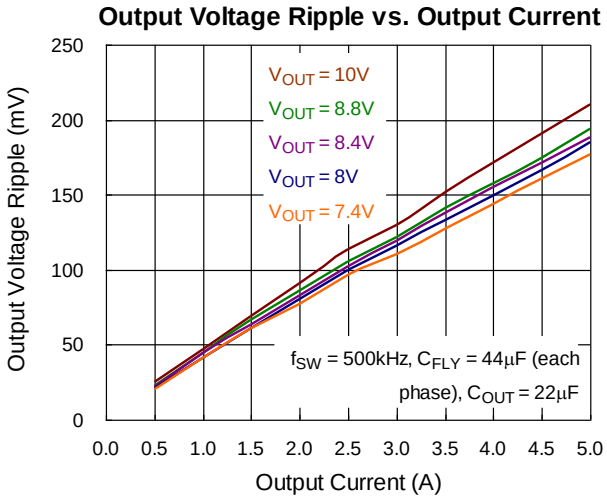
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SDA Setup Time	$t_{SU;DAT}$	Standard-mode	250	--	--	ns
		Fast-mode	100	--	--	
		Fast-mode plus	50	--	--	
		High-speed mode Cb = 400pF	10	--	--	
		High-speed mode Cb = 100pF	10	--	--	
SCL Clock Low Time	t_{LOW}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode plus	0.5	--	--	
		High-speed mode Cb = 400pF	320	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SCL Clock High Time	t_{HIGH}	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode plus	0.26	--	--	
		High-speed mode Cb = 400pF	120	--	--	ns
		High-speed mode Cb = 100pF	60	--	--	

Note 6. Specification is guaranteed by design and/or correlation with statistical process control.

13 Typical Operating Characteristics







14 Application Information

(Note 13)

14.1 Operation Principle

The cap divider topology relies on a smart wall adapter to control the voltage and current of input in order to charge. Based on the cap divider topology, the 4 MOSFETs (Q1 to Q4) are used to charge and discharge flying capacitor (CFLY) alternately. The simplified circuit of cap divider is shown in Figure 1.

In period 1: When Q1 and Q3 are turned on and Q2 and Q4 are turned off, the CFLY and COUT are in series with VBUS. The BUS current is supplied to COUT directly. During this period, the voltage of CFLY can be expressed as equation 1:

VCFLY = VBUS - VOUT ---- (1)

In period 2: When Q1 and Q3 are turned off and Q2 and Q4 are turned on, the CFLY and COUT are in parallel. The current of COUT is only supplied by CFLY. During this period, the voltage of CFLY can be expressed as equation 2:

VCFLY = VOUT ---- (2)

If the equation 2 is substituted into equation 1, the equation 1 can be expressed as equation 3:

VOUT = VBUS/2 ---- (3)

If the power dissipation of topology is ignored, the output power can be expressed as equation 4:

VOUT x IOUT = VBUS x IBUS ---- (4)

If the equation 3 is substituted into equation 4, the IOUT can be expressed as equation 5:

IOUT = 2 x IBUS ---- (5)

According to the equations above, the output voltage is half of the input voltage, and the output current is twice the input current in cap divider topology. For the efficiency and output ripple improvement in application, the dual phase cap divider topology with phase shift 180 degrees between phases are built in the RT9758D.

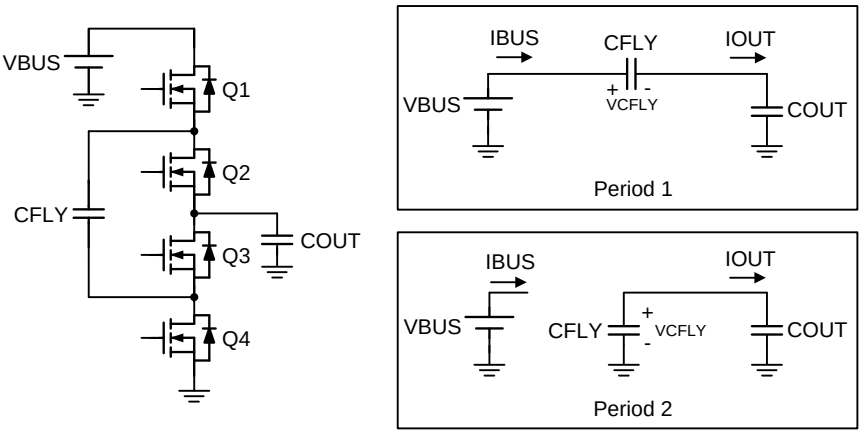


Figure 1. Simplified Circuit of Cap Divider

While the RT9758D is charging, host needs to communicate with smart wall adapter or wireless power device to control the charging current provided by the RT9758D. The communication flow between smart wall adapter, wireless power device and charge system is shown in Figure 2. In order to prevent abnormal events when charging, the RT9758D is established with many adjustable protections. All protection behaviors in each operation mode are shown in Table 3, Table 4, Table 5, and Table 6.

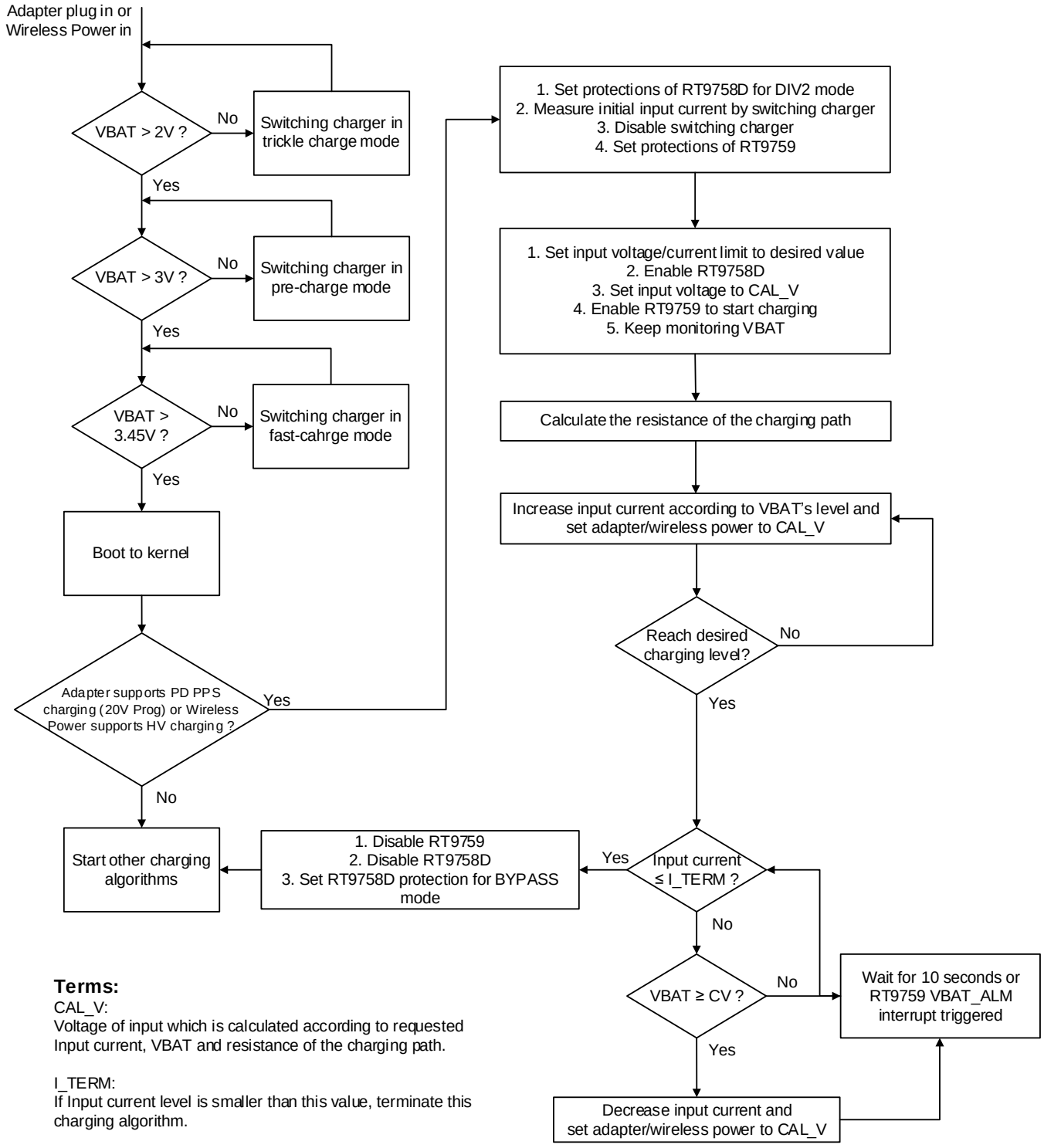


Figure 2. System Control Flow Chart

14.2 Device Power Up

The device is powered by VDDA. When VDDA voltage is higher than VDDA_UVLO threshold, the device will start working. The VDDA voltage can be powered by either VBUS or VOUT and that is dominated by the higher voltage level.

Once the RT9758D is powered, the device will activate the address detection mechanism to assign the slave address of device and configuration mode. The slave address of device is determined by voltage level at ADDR pin. The criteria of address detection threshold are shown in electrical characteristics list. After address detection is finished, the host can communicate with the RT9758D by I^2C serial interface. Furthermore, the reaction time during VDDA > VDDA_UVLO to I^2C release (t_{WAKE_UP}) is around 500μsec.

The RT9758D includes a watchdog timer that is disabled by default. When the watchdog timer expired, WDT_STAT and WDT_FLAG turn to high and the $\overline{INT}$ pin is pulsed ($t_{INT\_PULL\_LOW}$) 256μsec to interrupt the host. After resetting wait time (t_{WDT_WAIT}) 32msec, the related registers are reset to default values. (Refer to Register Descriptions for detail). If the device stays in watchdog timeout status, host can read or write any register to return counting.

Figure 3 shows the device power on flow with protections, insert and indictor function activation list in each state. In order to reduce quiescent current when charge system is unused, the RT9758D is established with low quiescent current mode that is called present mode. If the $\overline{EN}$ pin is pulled high or floating, the RT9758D will enter present mode for power saving. In present mode, most of sensing circuit inside the RT9758D will be turned off. In other words, all of protection and insert function are inactivated. However, if the user desires WRX_OK function to be active in present mode, users can set both WRX_OK_PSM bit and WRX_OK_EN bit to 1 to activate it.

If the $\overline{EN}$ pin is pulled low and set CHG_EN bit to 0, this condition is called standby mode. In standby mode, the AP can catch interrupt by the $\overline{INT}$ pin if specific protection or insert is triggered. Before start charging, the AP still can set the register values by I^2C protocol in present mode and standby mode.

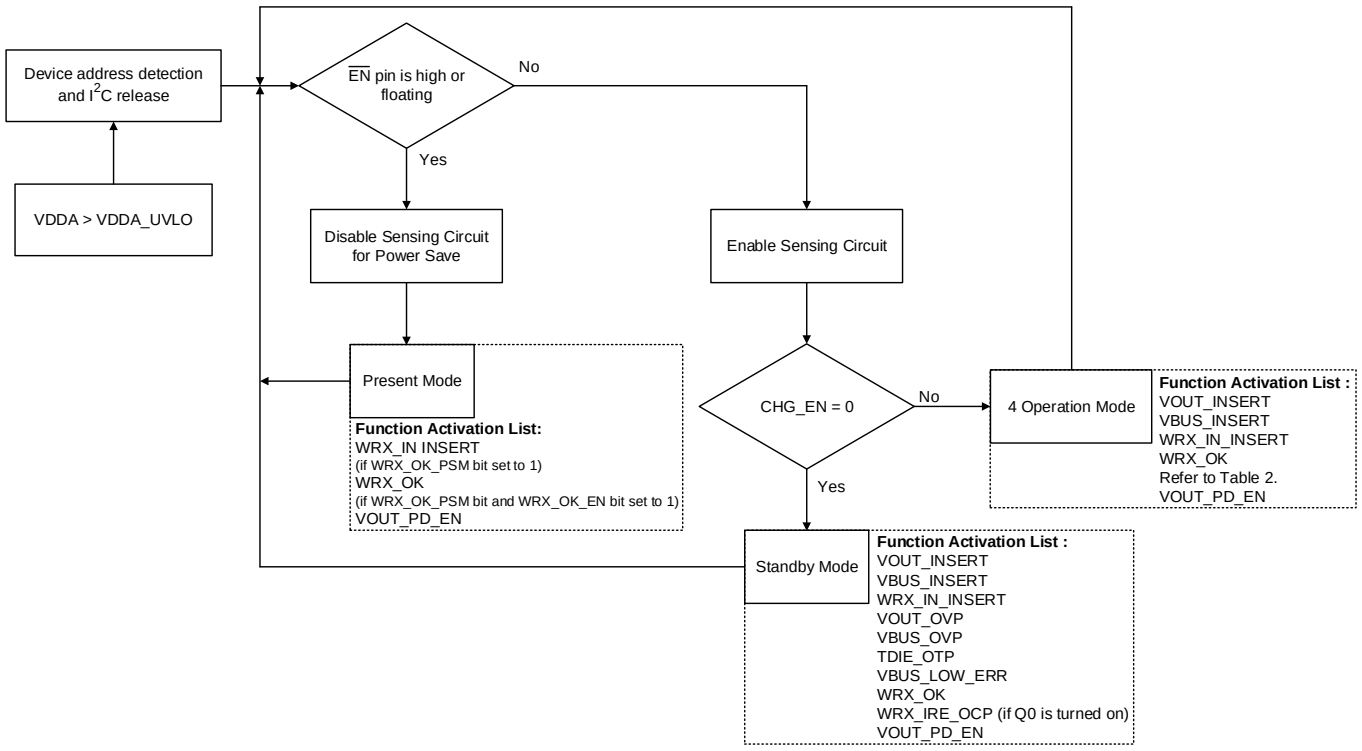


Figure 3. Device Power On Flow with Protections, Insert and Indicator Function Activation List

14.3 Protection Feature

The RT9758D integrates 9 protections to protect device operating in unexpected condition. These protections are established in bypass mode, reverse bypass mode, DIV2 mode and reverse DIV2 mode. Table 2 shows the related configuration of 4 operation modes. For example, only let the $\overline{EN}$ pin pull to high or floating, the RT9758D will operate in present mode for low quiescent current application. If let the $\overline{EN}$ pin pull to GND and set CHG_EN bit to 0, the RT9758D will enter standby mode. And if the $\overline{EN}$ pin pull to GND and set CHG_EN bit to 1, the operation mode is decided by OPERATION_MODE_SELECTION bit and REVERSE_MODE_EN bit setting.

About protections established in the RT9758D, Table 3, Table 4, Table 5, and Table 6 show the protect function activation list in each mode. In Table 3 and Table 5, "Stop bypass and Stop switching" means the device will stop charge but the CHG_EN bit still keeps 1, so the device will soft-start again immediately if VBUS_LOW_ERR status meets the rule and VBUS exists.

Table 2. Configuration of 4 Operation Modes

Mode	$\overline{EN}$ Pin	CHG_EN bit	OPERATION_MODE_SELECTION bit	REVERSE_MODE_EN bit
Present	H/Floating	X	X	X
Standby	L	0	X	X
Bypass	L	1	0	0
Reverse Bypass	L	1	0	1
DIV2 mode	L	1	1	0
Reverse DIV2	L	1	1	1

Table 3. Protection Function Activation List in Bypass Mode

Protection Function	Protection Method
VOUT_OVP (Note 7)	1. Stop bypass until fault release over 21m/100msec deglitch time (Default) 2. Reset CHG_EN = 0
VBUS_OVP (Note 7)	1. Stop bypass until fault release over 21m/100msec deglitch time (Default) 2. Reset CHG_EN = 0
IBUS_OCP	Stop bypass
WRX_IRE_OCP	Set Q0_CONTROL = 00 (Note 8)
VOUT_ERR	Hiccup (Note 9)
TDIE_OTP	Reset CHG_EN = 0
CFLY_DIAG	Not active
CON_OCP	Stop bypass
VBUS_LOW_ERR	Cannot do soft-start until VBUS_LOW_ERR = 0 (Note 10)

Note 7. Protection Method depends on AUTO_RECOVERY_EN bit and IN_VALID_RECOVERY_DEGLITCH bit.

Note 8. The WRX_IRE_OCP is active only when Q0 is turned on.

Note 9. Hiccup off time depends on VOUT_ERR_OFF_TIME bit.

Note 10. VBUS_LOW_ERR is active only before converter soft-start.

Table 4. Protection Function Activation List in Reverse Bypass Mode

Protection Function	Protection Method
VOUT_OVP	Reset CHG_EN = 0
VBUS_OVP	Reset CHG_EN = 0
IBUS_OCP	Reset CHG_EN = 0 and REVERSE_MODE_EN = 0
WRX_IRE_OCP	Set Q0_CONTROL = 00
VOUT_ERR	Not active
TDIE_OTP	Reset CHG_EN = 0 and REVERSE_MODE_EN = 0
CFLY_DIAG	Not active
CON_OCP	Reset CHG_EN = 0 and REVERSE_MODE_EN = 0
VBUS_LOW_ERR	Cannot do soft-start until VBUS_LOW_ERR = 1 (Note 10)

Table 5. Protection Function Activation List in DIV2 Mode

Protection Function	Protection Method
VOUT_OVP	Stop switching
VBUS_OVP	Stop switching
IBUS_OCP	Reset CHG_EN = 0
WRX_IRE_OCP	Set Q0_CONTROL = 00
VOUT_ERR	Reset CHG_EN = 0
TDIE_OTP	Stop switching until fault release over 160msec deglitch time
CFLY_DIAG	Reset CHG_EN = 0
CON_OCP	Stop switching
VBUS_LOW_ERR	Cannot do soft-start until VBUS_LOW_ERR = 0 (Note 10)

Table 6. Protection Function Activation List in Reverse DIV2 Mode

Protection Function	Protection Method
VOUT_OVP	Reset CHG_EN = 0
VBUS_OVP	Reset CHG_EN = 0
IBUS_OCP	Reset CHG_EN = 0 and REVERSE_MODE_EN = 0
WRX_IRE_OCP	Set Q0_CONTROL = 00
VOUT_ERR	Not active
TDIE_OTP	Reset CHG_EN = 0 and REVERSE_MODE_EN = 0
CFLY_DIAG	Reset CHG_EN = 0
CON_OCP	Reset CHG_EN = 0 and REVERSE_MODE_EN = 0
VBUS_LOW_ERR	Cannot do soft-start until VBUS_LOW_ERR = 1 (Note 10)

14.3.1 Input and Output Overvoltage Protection (VBUS_OVP, VOUT_OVP)

The device integrates VBUS_OVP and VOUT_OVP function to monitor input and output voltage by VBUS pin and VOUT pin, respectively. When the device is in standby mode or 4 operation modes, if the VBUS voltage is higher than VBUS_OVP threshold or the VOUT voltage is higher than VOUT_OVP threshold, the device will start to turn off charger in $t_{VBUS\_OVP\_RE}$ time or $t_{VOUT\_OVP\_DEG}$ time, respectively.

There are two register bits related to OVP protection which are AUTO_RECOVERY_EN and IN_VALID_RECOVERY_DEGLITCH. According to different two of register setting, the device shows different protection method in bypass mode. For example, in bypass mode with default setting (AUTO_RECOVERY_EN = 1 and IN_VALID_RECOVERY_DEGLITCH = 0), the device stops charge while OVP is triggered. And if OVP fault is released, the device will count 21msec deglitch time ($t_{OVP\_RECOVERY}$) to make sure OVP fault is released actually. After deglitch counting is finished, the device can re-start in bypass mode again. And in DIV2 mode, depending on the protection conditions, the device stops charge while OVP is triggered, if OVP fault is released the device can re-start immediately again or set CHG_EN = 0 when OVP is triggered in Table 5. In other two operation modes, regardless of two of bit setting, the device will set CHG_EN = 0 when OVP is triggered. About OVP protection behavior, Table 7 shows relational behavior in each mode. Users can adjust the threshold of VBUS_OVP and VOUT_OVP via register setting. For safety charging, the OVP level must be set to 1.1 times the level of operating voltage. And make sure the input and output voltage are not higher than absolute maximum rating of the VBUS, WRX_IN and VOUT pin. (Prevented by external TVS or OVP IC, etc.).

Table 7. OVP Protection Behavior in Each Mode

Bypass Mode		
AUTO_RECOVERY_EN	**IN_VALID_RECOVERY_DEGLITCH**	**OVP Protection Behavior**
0	X	Reset CHG_EN = 0
1	0	Stop bypass until fault release over 21msec deglitch time
1	1	Stop bypass until fault release over 100msec deglitch time
DIV2 Mode		
X	X	Stop switching until fault release or reset CHG_EN = 0
Reverse Bypass Mode and Reverse DIV2 Mode		
X	X	Reset CHG_EN = 0

14.3.2 VBUS Charge Voltage Protection (VBUS_LOW_ERR)

The device integrates VBUS_LOW_ERR to prevent users from adjusting wrong VBUS for charge. In standby mode, if VBUS is lower than VBUS_LOW_ERR falling threshold, the VBUS_LOW_ERR flag and status bit will set to 1. If VBUS is higher than VBUS_LOW_ERR rising threshold, the VBUS _LOW_ERR status bit will set to 0. The VBUS_LOW_ERR threshold depends on OPERATION_MODE_SELECTION bit, if OPERATION_MODE_SELECTION set to 0, the VBUS_LOW_ERR typical falling threshold is 0.99V/V. If OPERATION_MODE_SELECTION set to 1, the VBUS_LOW_ERR typical threshold is 1.975V/V. Before start charging in 4 operation modes, users should follow the rule of VBUS_LOW_ERR shown in Table 8. If VBUS_LOW_ERR condition does not meet the rule, the device will not enter charging process. In above case, the device will keep similarly to standby mode until the VBUS_LOW_ERR condition is met. For recommended setup process before start charging,

set the device into standby mode (CHG_EN = 0) and then make sure VBUS_LOW_ERR status, OPERATION_MODE_SELECTION bit and REVERSE_MODE_EN bit are ready. After the device starts charging, the VBUS_LOW_ERR function will be disabled.

Table 8. Rule of VBUS_LOW_ERR before Start Charging Process in 4 Operation Modes

Operation Mode	VBUS_LOW_ERR STAT	OPERATION_MODE_SELECTION bit	REVERSE_MODE_EN bit
Bypass	0	0	0
Reverse Bypass	1	0	1
DIV2	0	1	0
Reverse DIV2	1	1	1

14.3.3 WRX Reverse Overcurrent Protection (WRX_IRE_OCP)

The WRX_IRE_OCP function monitors reverse input current from VBUS to WRX_IN via Q0. And it is active only while Q0 is turned on. If Q0_CONTROL bit set 10 or 11, the Q0 will turn on and WRX_IRE_OCP will start detecting reverse input current. If the reverse input current is larger than WRX_IRE_OCP threshold in $t_{WRX\_IRE\_OCP\_DEG}$ time, the device will only reset Q0_CONTROL bit to 00 in order to disable Q0 immediately. Users can adjust the WRX_IRE_OCP threshold via register setting.

14.3.4 IBUS Overcurrent Protection (IBUS_OCP)

The device integrates bidirectional IBUS_OCP function to detect input current in 4 operation modes. In reverse DIV2 mode and reverse bypass mode, if IBUS current from VOUT to VBUS is larger than IBUS_OCP threshold in $t_{IBUS\_OCP\_DEG}$ time, the device will stop charging and reset CHG_EN bit and REVERSE_MODE_EN bit to 0.

In DIV2 mode, if IBUS current from VBUS to VOUT is larger than IBUS_OCP threshold in $t_{IBUS\_OCP\_DEG}$ time, the device will stop charging and reset CHG_EN bit to 0.

In bypass mode, if IBUS current from VBUS to VOUT is larger than IBUS_OCP threshold in $t_{IBUS\_OCP\_DEG}$ time, the device will stop charging and still keep CHG_EN bit to 1. Users can adjust the IBUS_OCP threshold via register setting.

14.3.5 Converter Overcurrent Protection (CON_OCP)

The device integrates CON_OCP function to prevent huge abnormal converter operating current in 4 operation modes. In reverse DIV2 mode and reverse bypass mode, if the converter operating current is larger than CON_OCP threshold, the device will stop charging and reset CHG_EN bit and REVERSE_ MODE_EN bit to 0.

In DIV2 mode and bypass mode, if the converter operating current is larger than CON_OCP threshold, the device will stop charging and still keep CHG_EN bit to 1.

14.3.6 Device Thermal Shutdown (TDIE_OTP)

The device integrates TDIE_OTP to prevent system charging in over-temperature condition. The TDIE_ OTP function monitors die temperature. When the device is in standby mode or bypass mode, if the die temperature is higher than TDIE_ OTP threshold in t_{TDIE_DEG} time, the device will stop charging and reset CHG_EN bit to 0.

In DIV2 mode, if the die temperature is higher than TDIE_ OTP threshold in t_{TDIE_DEG} time, the device will stop charging and until fault release over 160m seconds deglitch time. And the device will re-start again if start-up conditions are met.

When the device is in reverse bypass mode or reverse DIV2 mode, if the die temperature is higher than TDIE_OTP threshold, the device will stop charging and reset CHG_EN bit and REVERSE_MODE_EN bit both to 0.

After TDIE_OTP is triggered, the TDIE_OTP_EXIT_ FLAG will turn to high when die temperature is lower than TDIE_OTP release threshold. For safety, the device should only enable charge again after TDIE_OTP_STAT is set to 0 and TDIE_OTP_EXIT_ FLAG is set to 1.

14.3.7 Flying Capacitor Diagnose (CFLY_DIAG)

The device integrates CFLY_DIAG function to diagnose the health of flying capacitors before charging. The CFLY_DIAG function only active in soft-start process of DIV2 mode and reverse DIV2 mode. After CHG_EN is enabled, the device starts soft-start process with corresponding soft-start time (t_{SS_DIV2}, or $t_{SS\_REVERSE\_DIV2}$) in DIV2 or reverse DIV2 mode. In soft-start process, the CFLY_DIAG function will diagnose the CFL pin level in each phase. If the CFL level is higher than CFLY_DIAG detect level (V_{CFLY_DIAG}), the device will stop soft-start process and reset CHG_EN bit to 0. The CFLY_DIAG function will stop activating after the device charge successfully. In normal charging case, If the flying capacitor is short while charging, the device can be protected by other protections (e.g., IBUS_OCP, VBUS_OVP, VOUT_OVP or CON_OCP).

14.3.8 Output Pin Error Detection (VOUT_ERR)

The device integrates VOUT_ERR function to prevent output pin abnormal short before charging. The VOUT_ERR function is active only soft-start process of bypass mode and DIV2 mode. After CHG_EN is enabled, the device starts soft-start process with corresponding soft-start time (t_{SS_BYPASS} and t_{SS_DIV2}) in bypass or DIV2 mode. In soft-start process of DIV2 mode, the VOUT_ERR function will detect the VOUT pin level. If the VOUT level cannot over than VOUT_ERR detect level (VOUT_ERR), the device will stop soft-start process and reset CHG_EN bit to 0.

In soft-start process of bypass mode, If VOUT_ERR function is triggered, the device will stop soft-start process and still keep CHG_EN bit to 1. And the device will re-start again if start-up conditions are met. At bypass mode case, the device operates like Hiccup mode if VOUT pin short abnormally. The VOUT_ERR function will stop activating after the device charge successfully.

14.4 Auto Transition Function Feature (AT_Function)

For more flexible mode change application between bypass mode and DIV2 mode, the auto transition function (AT_Function) is established in the RT9758D to make converter mode change automatically by adjusting VBUS voltage. In register map, the AT_FUNCTION_EN bit is used to enable this function and the AT_FUNCTION bit is used to set the threshold of mode transition. When the AT_Function is active in bypass mode, if VBUS is higher than AT_Function threshold in $t_{AT\_FUNCTION\_DEG}$ time, the device will stop charging, set OPERATION_MODE_ SELECTION bit to 1 and then start DIV2 charging process if the start-up conditions are met. In another case, if VBUS is lower than AT_Function threshold when the device operates in DIV2 mode, it will stop charging, set OPERATION_MODE_ SELECTION bit to 0 and then start bypass charging process if the start-up conditions are met. Figure 4 is the recommended operation flow for using auto transition function, users should follow step 1-4 to use auto transition function. Especially, if the user desires device be transited from bypass mode to DIV mode by using AT_Function, be sure to enable VOUT_PD bit to 1 before increasing VBUS voltage.

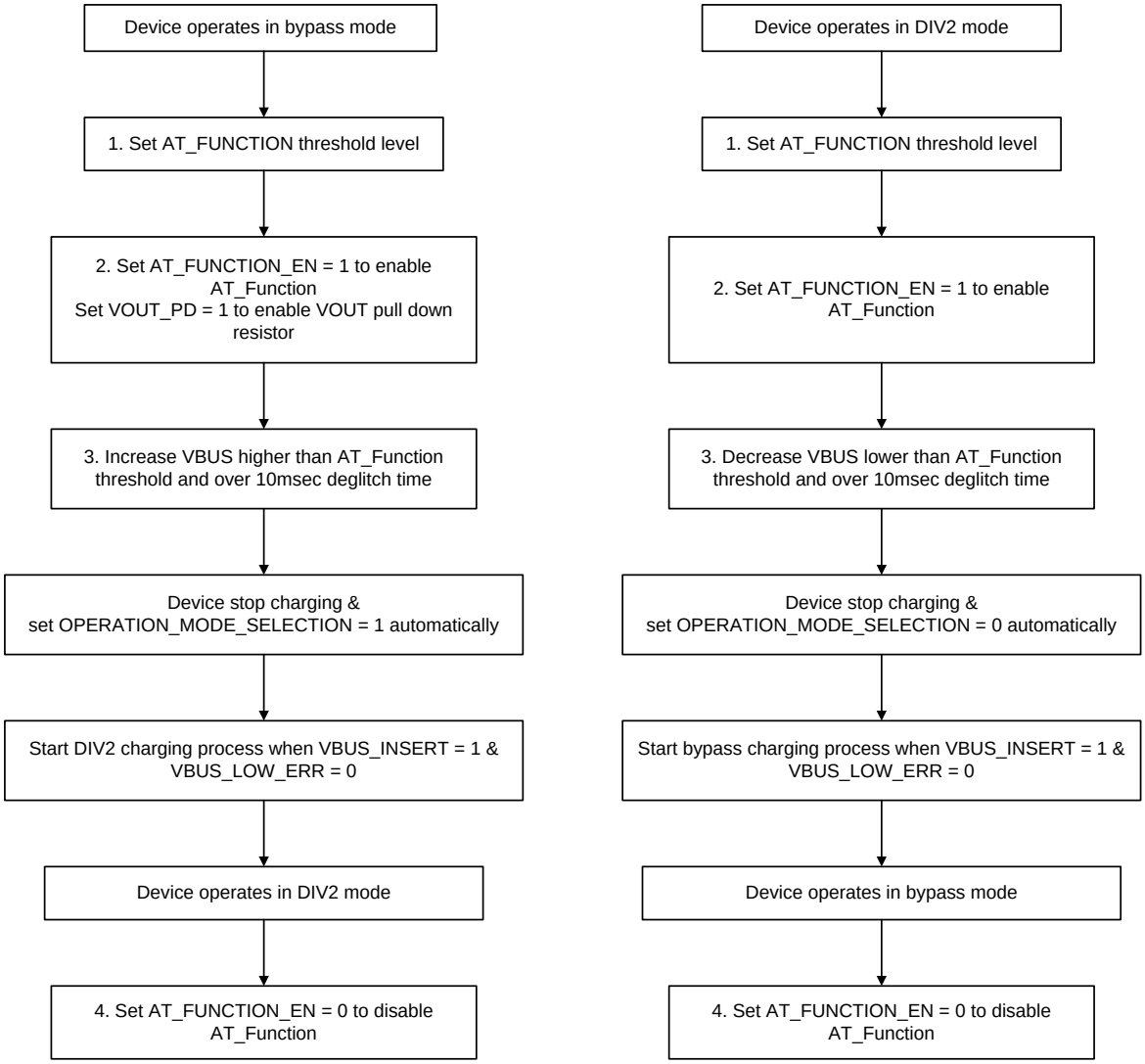


Figure 4. Operation Flow for Using Auto Transition Function

14.5 Watchdog Timer (WDT)

When the device is controlled by host, all of the registers can be programmed by host. The host has to read or write any register to reset watchdog counter before watchdog timeout and it can also disable WDT function by setting WDT_EN bits to 0. When the watchdog timer expired in standby mode and 4 operation mode, WDT_STAT and WDT_FLAG turn to high and $\overline{INT}$ pin is pulsed to interrupt the host. After watchdog reset wait time (t_{WDT_WAIT}), the different related registers are reset to default values (Refer to Register Descriptions for detail) according to operation mode and the BEHAVIOR_AFTER_WDT bit setting. Figure 5 shows the WDT flow chart. For example, when the watchdog timer expired in bypass mode and the BEHAVIOR_AFTER_WDT bit is 1, the OVP, OCP and OTP registers are reset to default value but the CHG_EN bit and Q0_CONTROL bit will keep as same as before. In other case, when the watchdog timer is expired, the OVP, OCP and OTP registers are reset to default value and the CHG_EN bit and Q0_CONTROL bit will also reset to 0 and 00, separately. If the device stays in watchdog timer suspend status, host can read or write any registers to return counting. To decrease quiescent current in present mode, the WDT timer will force disable.

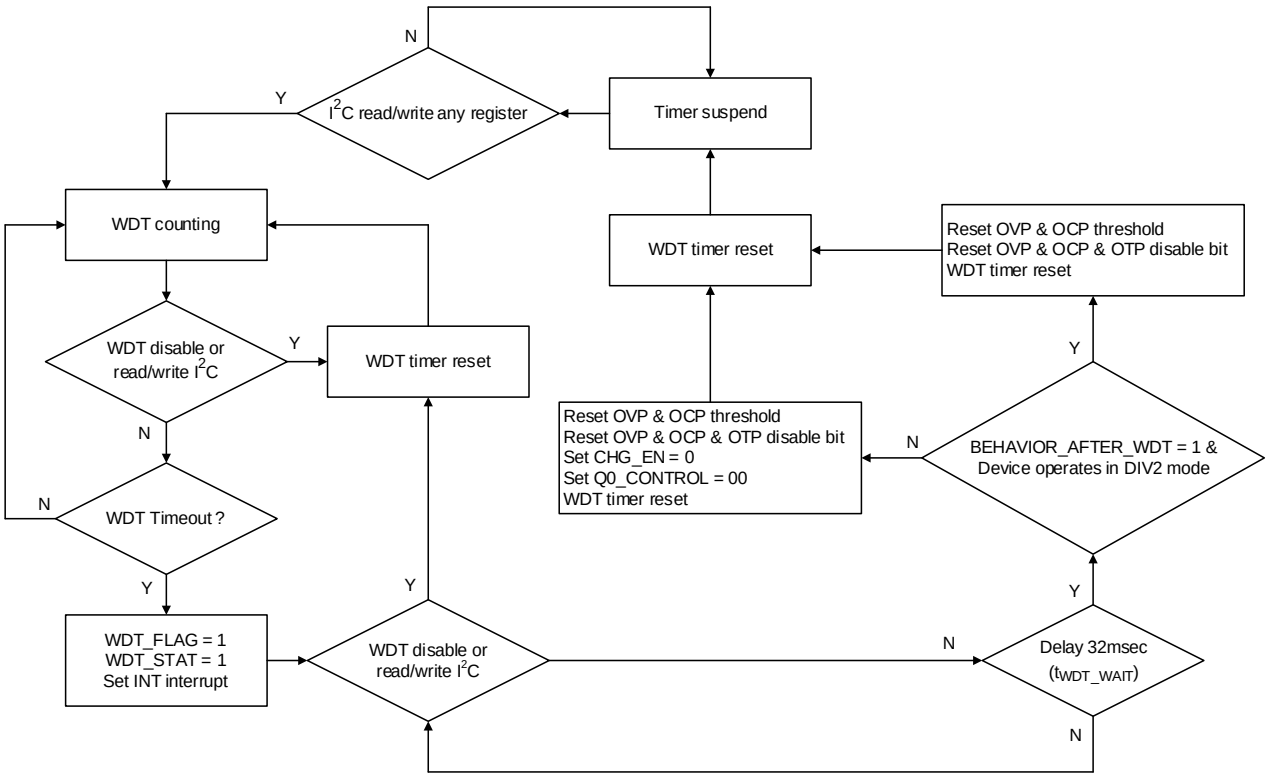


Figure 5. WDT Flow Chart

14.6 Pre-Charge Mechanism

To avoid the inrush current caused by the voltage difference between capacitors and the voltage source, the device establishes a pre-charge mechanism to charge the CFLY capacitors and the COUT capacitor before charging the battery. The device begins to charge the battery if the pre-charge time is timeout and no fault occurs during the pre-charge period. The pre-charge time depends on the setting of registers CFLY_DIAG_TIME and VOUT_ERR_ON_TIME. Each pre-charge time and pre-charged capacitors for 4 operation modes are indicated in Table 9. In the case of the DIV2 mode, the pre-charge time is CFLY_DIAG_TIME plus VOUT_ERR_ON_TIME, and the CFLY and COUT capacitors are pre-charged at the same time.

Table 9. Pre-charge Time in 4 Operation Modes

Operation Mode	Pre-charge Time	Pre-charged Capacitor
Bypass	VOUT_ERR_ON_TIME	COUT
Reverse Bypass	NA	NA
DIV2	CFLY_DIAG_TIME + VOUT_ERR_ON_TIME	CFLY and COUT
Reverse DIV2	CFLY_DIAG_TIME	CFLY

14.7 Operation Mode Diagram

The RT9758D includes 4 operation modes, users can control device to enter each mode by related register bits. Figure 6 shows the setting step between each mode. Users need to follow the recommended step to control device. For example, the device can be transferred between bypass mode and DIV2 mode by two operation ways. The first way is using AT_FUNCTION, and the second way is controlling by register setting. If the user controls device by register, the recommended operation flow is as below: The first step is to set CHG_EN bit to 0 to make device enter standby mode. The second step is to set OPERATION_MODE_SELECTION bit and REVERSE_MODE_EN bit, then the last step is to set CHG_EN bit to 1 to start charging. Based on above description, the OPERATION_MODE_SELECTION bit and REVERSE_MODE_EN bit can be changed only while the device stays in standby mode or present mode.

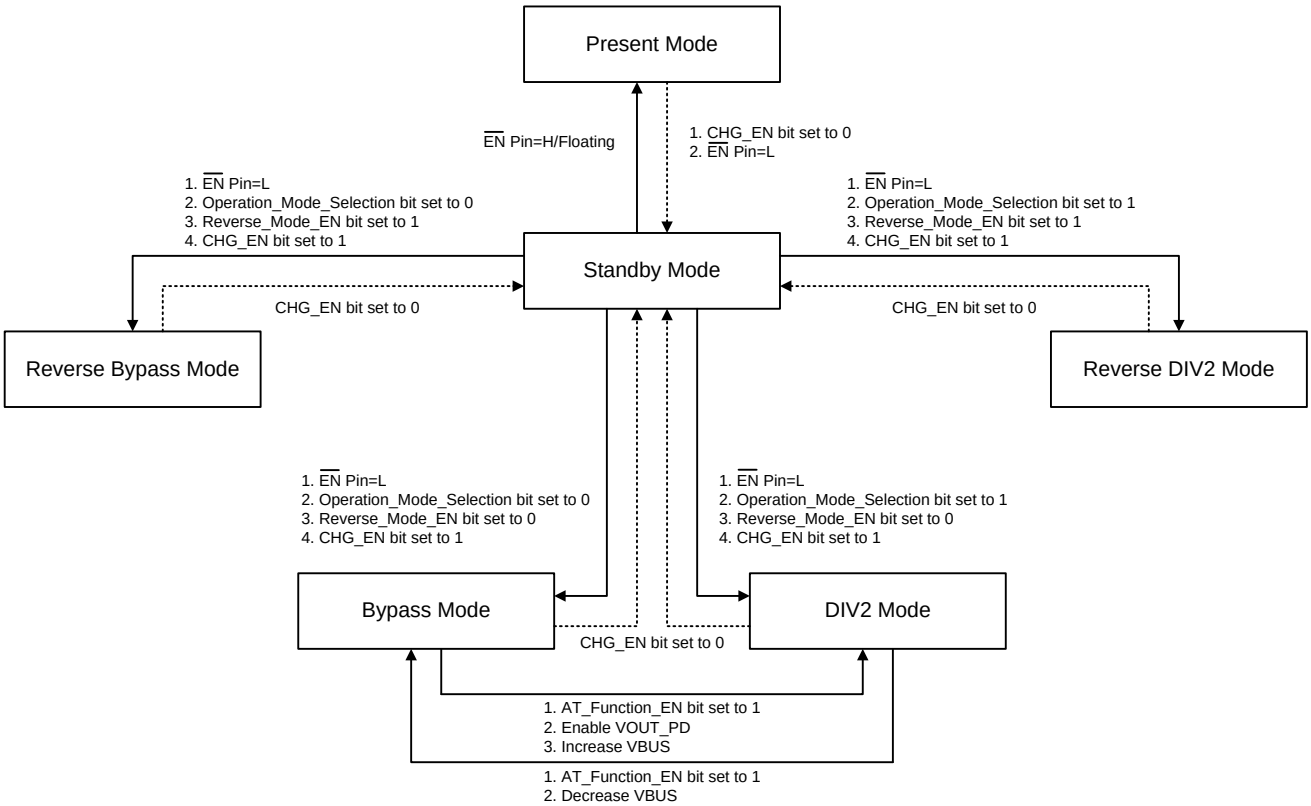


Figure 6. Operation Mode Diagram

14.8 WRX_OK Function (WRX_OK)

The RT9758D includes WRX_OK pin function to inform system. In standby mode and 4 operation mode with default setting, if WRX_IN voltage is higher than WRX_INSERT level, WRX_OK pin will pull high. Users can change status of WRX_OK pin from high to low while WRX_INSERT is detected by using OVERRIDE_WRX_OK_PIN_LOW bit. If OVERRIDE_WRX_OK_PIN_LOW bit is set to 1, the status of WRX_OK pin pulls to low while WRX_INSERT is detected. If the user desires WRX_OK function to be active in present mode, users can set WRX_OK_PSM bit and WRX_OK_EN bit both to 1 to activate it. In addition, users can disable WRX_OK function by WRX_OK_EN bit in each mode.

14.9 Q0 MOSFET Control (Q0_CONTROL)

The RT9758D includes Q0 MOSFET to prevent reverse voltage from VBUS pin. It can be controlled by Q0_CONTROL bit. If Q0_CONTROL bit set to 10, Q0 will turn on after 2msec delay time (t_{Q0_DELAY}) when WRX_INSERT is detected and without VBUS OVP fault. In 2msec delay time (t_{Q0_DELAY}), WRX_IN pull down resistor will be active. If Q0_CONTROL bit set to 11, Q0 will turn on immediately when VBUS_INSERT is detected. If users desire to turn off Q0 MOSFET, just set Q0_CONTROL bit to 00 or 10.

14.10 I²C Serial Interface

The RT9758D integrates I²C interface for host to program charging parameter and monitor device status. The interface requires a serial clock line (SCL) and a serial data line (SDA). The host should initiate a data transfer on the bus and generates the clock signals to permit that transfer. The device operates with address 50H, 51H or 52H to receive control input from the host. The SCL and SDA pin are open drain structures. Users should connect a supply voltage via a current source or pull-up resistors on SCL and SDA. Figure 7 shows the I²C waveform information, the data line must be stable during the high period of SCL line. The high or low state of SDA can change only when SCL line is low.

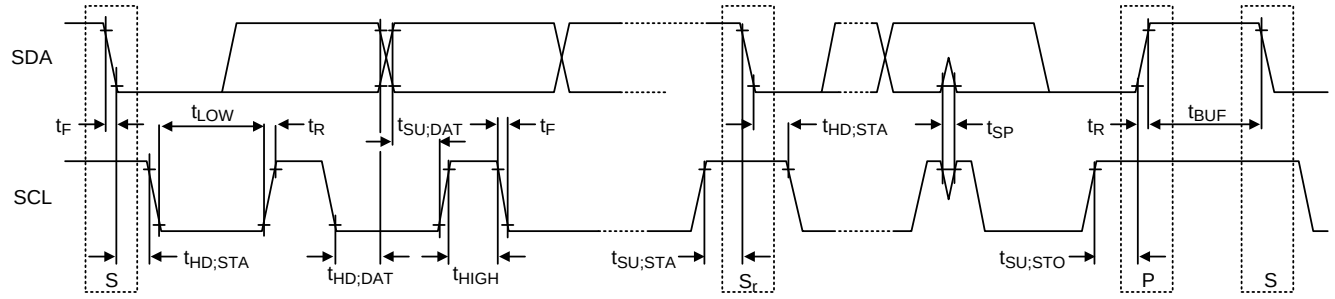


Figure 7. I²C Waveform Information

The RT9758D operates as an I²C slave device with address 50H, 51H or 52H (depends on voltage condition of ADDR pin). Every byte on SDA line must be 8-bit long. Figure 8 shows the byte format of SDA and SCL line. All of transactions begin with a START pattern and can be terminated with a STOP pattern. After START, the master should send a slave address. The slave address is 7-bit long followed by the eighth bit as a data direction bit (R/W). The direction bit setting to 0 indicates a transmission and 1 indicates a request for data. The master should take an acknowledge bit after every byte. The master should release SDA line during the acknowledge clock pulse so the slave device can pull low the SDA line to signal the master that the byte was successfully received. The RT9758D supports multi read/write and SCL line can be up to 3.4MHz.

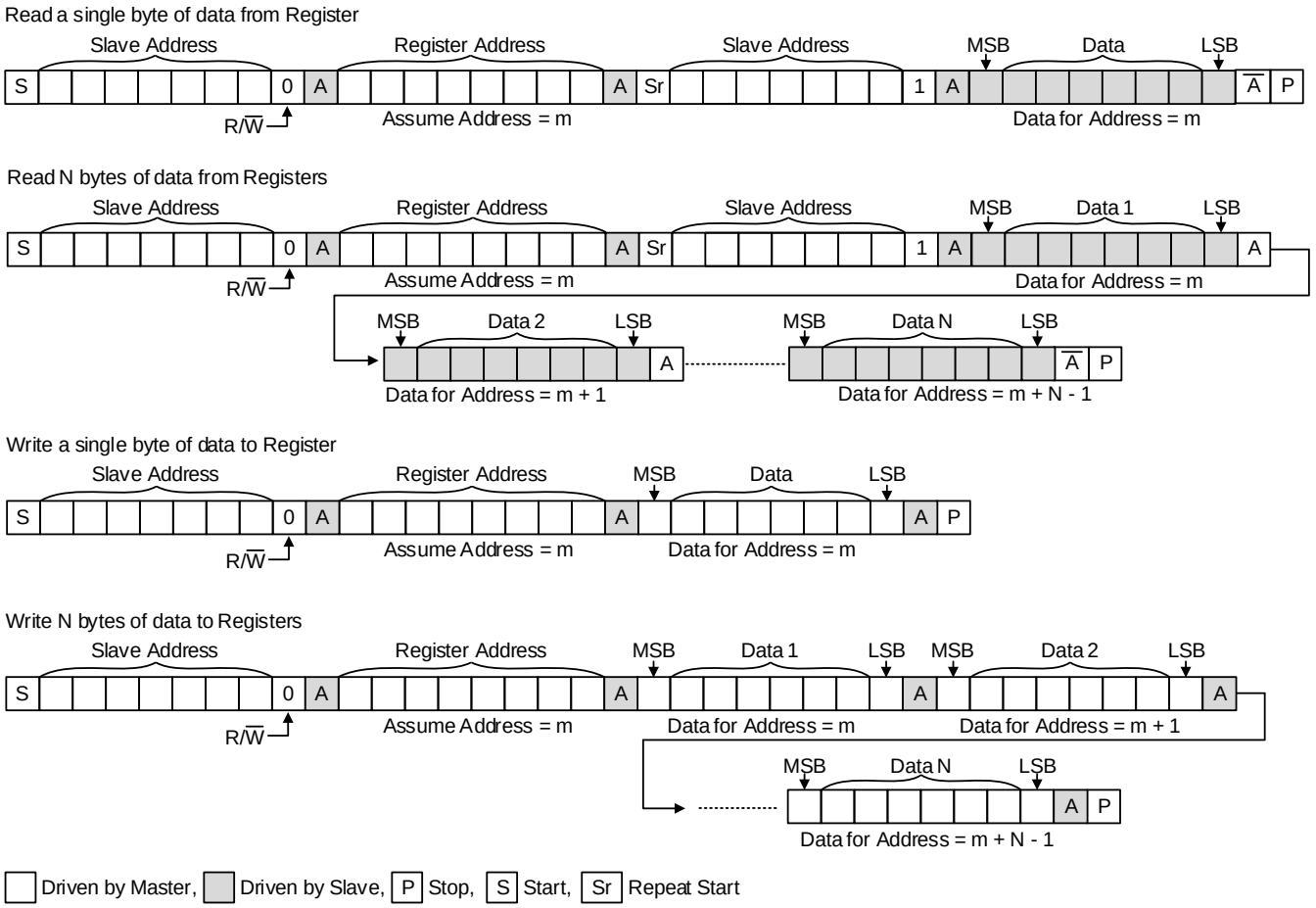


Figure 8. Read and Write Function

14.11 Interrupt ($\overline{INT}$), STAT, FLAG, and MASK

The $\overline{INT}$ pin is an open drain structure; users should connect a supply voltage via a current source or pull-up resistors on the pin. When the device triggers an event, the $\overline{INT}$ pin will pull low for $t_{INT\_PULL\_LOW}$ to notify host. The register map shows all state, flag, and control bit of the device.

When the device triggers the event with FLAG, it will send an $\overline{INT}$ signal to host and set the FLAG bit to 1. The FLAG bit can be cleared after read. The device will not send another $\overline{INT}$ signal until the FLAG is cleared and a new event occurs again. The MASK bit can disable the $\overline{INT}$ pin to send a signal to host. The STAT and FLAG bit are still updated even though the MASK bit is set to 1.

The STAT bits show current statue of the device and are updated as the status change. All of STAT bits will not send $\overline{INT}$ signal to system when the STAT bit is triggered.

14.12 Spread Spectrum

The device integrated spread spectrum function for users to optimize the EMI influence on system design. The device switching frequency is decided by 0x0F[5:3] bit. The spectral density will concentrate on the switching frequency. Users can enable the spread spectrum function by setting 0x0F[6] bit. After the spread spectrum function is enabled, the device will modulate the switching frequency for ±6% to reduce the spectral density.

14.13 Parallel Application

For higher charging current application, it is available to use two RT9758D in parallel architecture. The advantages of using parallel architecture are reducing cable losses, improving efficiency of charge system and cutting down charging period. The high power solution that uses two RT9758D is shown in Figure 9. The slave address of RT9758D can be configured by setting ADDR pin while device power up. In order to avoid unstable ripple issue while charging with parallel architecture, the RT9758D is established with synchronization function at SYNC pin. If the RT9758D is configured to master mode (SYNC_SLAVE_EN bit = 0) and synchronization function is active (SYNC_FUNCTION_ EN bit = 1), the SYNC pin provides synchronization pulses with frequency equal to twice switching frequency and 50% duty cycle. If the RT9758D is configured to slave mode (SYNC_SLAVE_EN bit = 1) and synchronization function is active (SYNC_FUNCTION_EN bit = 1), the device works only while SYNC pin receives synchronization pulses. For using the synchronization function, the SYNC pins of the two devices should be connected to each other. The configuration mode and synchronization function can be configured by 0x0D[3] bit and 0x0D[2] bit, respectively.

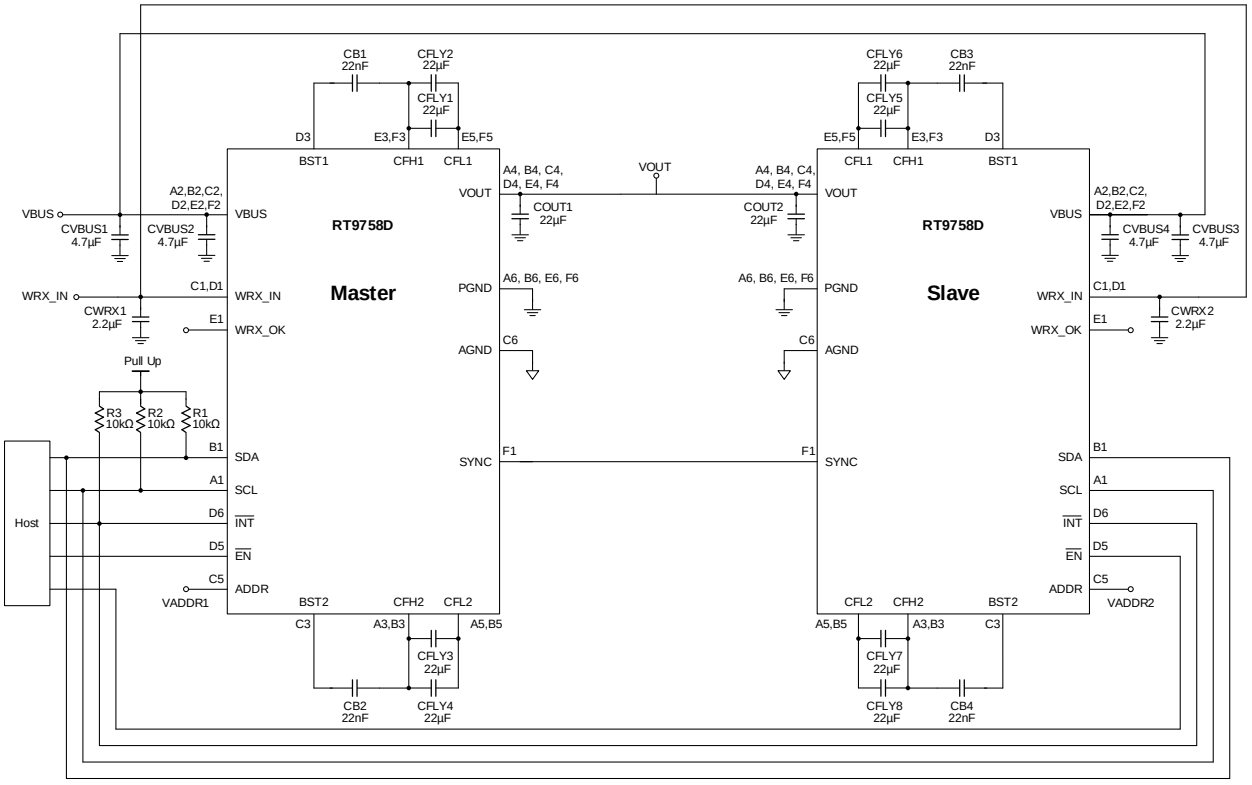


Figure 9. Parallel Application Circuit

In DIV2 mode and reverse DIV2 mode, all of phase angle in the device need to be defined correctly for optimized output ripple and charging efficiency, especially parallel application. Table 10 shows the recommended phase angle in 4 operation modes with different configuration. For example, in DIV2 mode parallel application, the A phase between master and slave device should be shifted 90 degrees, the A and B phase in the same device should be shifted 180 degrees. It is strongly prohibited to change PHASE_A_ANGLE bit and PHASE_B_ANGLE bit during charging.

If parallel architecture is used, the start-up sequence should be compiled with the rules below. The RT9758D set as slave (RT9758D_S) should be enabled before host enables the RT9758D set as master (RT9758D_M) in order to achieve parallel application. The RT9758D_S will not switch until the SYNC pin receives synchronization pulses

provided by the RT9758D_M. The communication flow between smart wall adapter, wireless power device and parallel charge system is shown in Figure 10.

Table 10. Phase Angle in 4 Operation Modes with Different Configuration

Operation Mode	Configuration	Phase_A_ANGLE	Phase_B_ANGLE
DIV2 mode	Standalone	0°	180°
DIV2 mode	Master	0°	180°
DIV2 mode	Slave	90°	270°
Reverse DIV2 mode	Standalone	0°	180°
Reverse DIV2 mode	Master	0°	180°
Reverse DIV2 mode	Slave	90°	270°
Bypass mode	NA	Don't care	Don't care
Reverse Bypass mode	NA	Don't care	Don't care

Table 11 shows the related configuration of 4 operation modes in parallel application. The users must follow the rule before normal operation. For example, the SYNC_SLAVE_EN bit set to 0, OPERATION_MODE_SELECTION bit set to 1 and REVERSE_MODE_EN bit set to 0 in DIV2 mode with master configuration is required. Especially in reverse DIV2 mode with salve configuration, the REVERSE_MODE_EN bit should be set to 0 for normal soft-start sequence.

Table 11. Configuration of 4 Operation Modes in Parallel Application (Note 11)

Mode	Configuration	SYNC_SLAVE_EN bit	OPERATION_MODE_SELECTION bit	REVERSE_MODE_EN bit
Bypass	**Master**	0	0	0
	Slave	1	0	0
Reverse Bypass	**Master**	0	0	1
	Slave	1	0	1
DIV2 mode	**Master**	0	1	0
	Slave	1	1	0
Reverse DIV2	**Master**	0	1	1
	Slave	1	1	0 (Note 12)

Note 11. In parallel application, SYNC_FUNCTION_EN bit must be set to 1.

Note 12. In case of reverse DIV2 mode with slave configuration, the REVERSE_MODE_EN bit will be forced to 0 when SYNC_FUNCTION_EN bit = 1 and the SYNC pin receives synchronization pulses from master device.

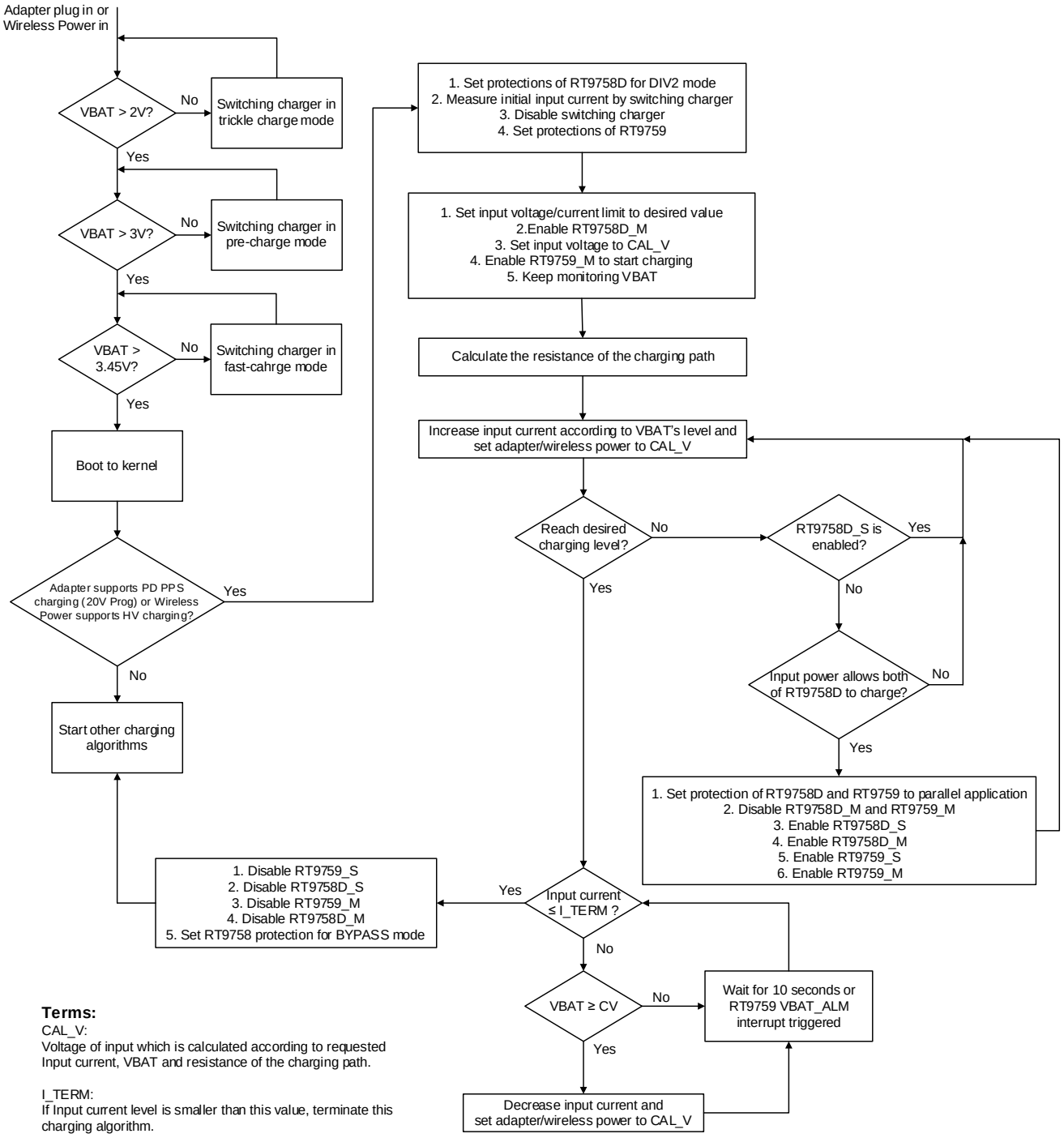


Figure 10. System Control Flow Chart with Parallel Charge System

14.14 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-36B 2.74x2.84 (BSC) package, the thermal resistance, θ_{JA}, is 34.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (34.7°C/W) = 2.88W for a WL-CSP-36B 2.74x2.84 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

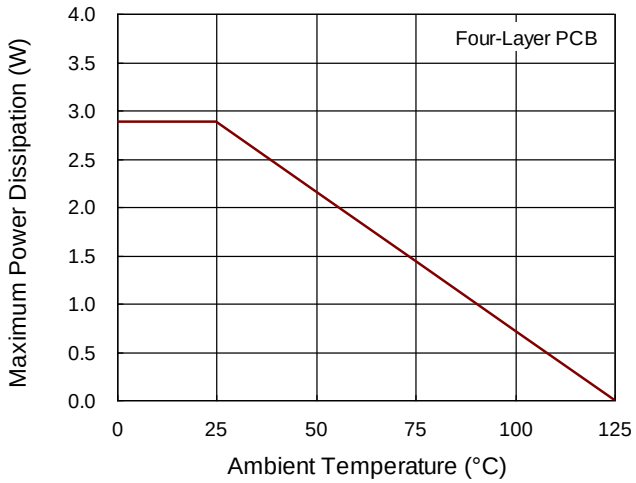


Figure 11. Derating Curve of Maximum Power Dissipation

14.15 Layout Considerations

The RT9758D layout guidelines are recommended as below:

- Place low ESR bypass capacitor to GND for the WRX_IN/VBUS/VOUT pin. The bypass capacitor needs to be placed as close as possible to the RT9758D.
- The capacitor of BST/CFH should be placed as close as possible to the RT9758D.
- Place flying caps with the RT9758D on same layer. The flying caps should be placed as close as possible to the RT9758D. The path of flying caps should be as small as possible.

The WRX_IN, VBUS, and VOUT traces should be as wide as possible to accommodate high charge current.

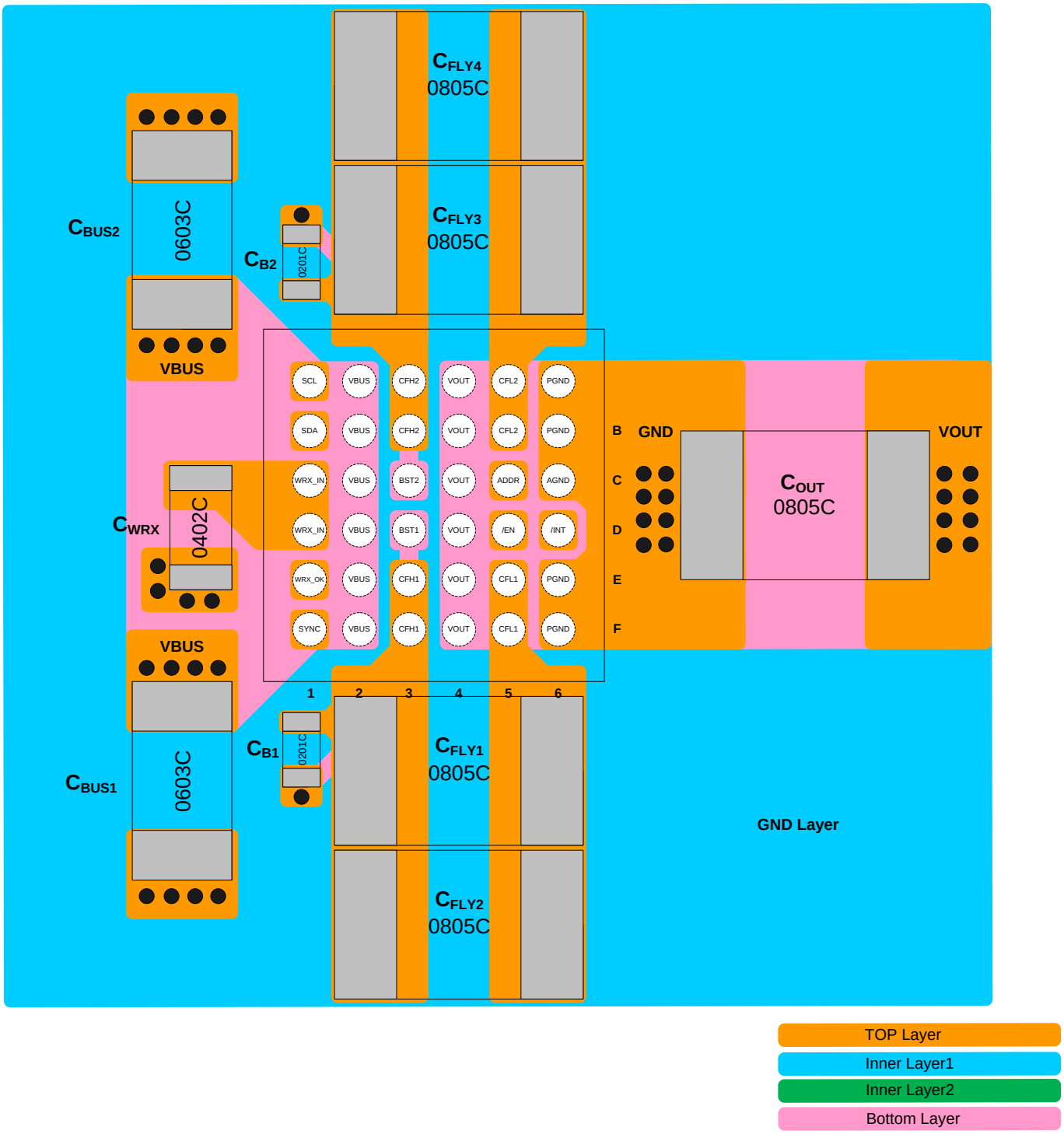


Figure 12. PCB Layout Guide

Note 13. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

15 Functional Register Description

15.1 Register Map Summary

Function Name	STAT	FLAG	MASK	Threshold	Enable	Deglitch
VOUT_OVP	0x09[6]	0x02[6]	0x06[6]	0x0A[2:0]	0x12[7]	--
VBUS_OVP	0x09[7]	0x02[7]	0x06[7]	0x0B[5:0]	0x12[6]	--
IBUS_OCP	0x09[3]	0x03[7]	0x07[7]	0x0C[7:4]	0x12[4]	--
WRX_IRE_OCP	0x09[2]	0x03[6]	0x07[6]	0x0C[3:0]	0x12[3]	--
CON_OCP	--	0x01[7]	0x05[7]	--	--	--
TDIE_OTP	0x09[1]	0x02[1]	0x06[1]	--	0x12[5]	--
TDIE_OTP_EXIT	--	0x02[2]	0x06[2]	--	--	--
VBUS_LOW_ERR	0x08[3]	0x01[4]	0x05[4]	--	--	--
CFLY_DIAG	--	0x01[6]	0x05[6]	--	--	--
VOUT_ERR	--	0x01[3]	0x05[3]	--	--	--
WRX_INSERT	0x08[2]	0x01[2]	0x05[2]	--	--	--
VBUS_INSERT	0x08[0]	0x01[0]	0x05[0]	--	--	--
VOUT_INSERT	0x08[4]	0x01[5]	0x05[5]	--	--	--
WDT	0x09[0]	0x02[0]	0x06[0]	0x0E[6:4]	0x0E[3]	--
SWITCHING_ENABLED	0x08[1]	0x01[1]	0x05[1]	--	--	--
IN_VALID_RECOVERY_DEGLITCH	--	--	--	--	--	0x0F[7]
CFLY_DIAG_TIME	--	--	--	--	--	0x11[7:6]
VOUT_ERR_ON_TIME	--	--	--	--	--	0x11[3:2]
VOUT_ERR_OFF_TIME	--	--	--	--	--	0x11[1]
AT_FUNCTION	--	--	--	0x10[2:0]	0x10[3]	--
SINGLE_PHASE_MODE_EN	--	--	--	0x0D[5:4]	--	--
FSW	--	--	--	0x0F[5:3]	--	--
OPERATION_MODE_SELECTION	--	--	--	0x0F[0]	--	--
PHASE_A_ANGLE	--	--	--	0x10[7:6]	--	--
PHASE_B_ANGLE	--	--	--	0x10[5:4]	--	--
PRECHARGE_CURRENT	--	--	--	0x11[5:4]	--	--
REG_RST	--	--	--	0x12[2]	--	--
BEHAVIOR_AFTER_WDT	--	--	--	--	0x11[0]	--
SPREAD_SPECTRUM	--	--	--	--	0x0F[6]	--
CHG_EN	--	--	--	--	0x0F[2]	--
REVERE_MODE_EN	--	--	--	--	0x0F[1]	--
AUTO_RECOVERY_EN	--	--	--	--	0x0E[7]	--
OVERRIDE_WRX_OK_PIN_LOW	--	--	--	--	0x0E[2]	--
WRX_OK_EN	--	--	--	--	0x0E[1]	--
WRX_OK_PSM	--	--	--	--	0x0E[0]	--

VBUS_PD_EN	--	--	--	--	0x0D[7]	--
WRX_PD_EN	--	--	--	--	0x0D[6]	--
VOUT_PD_EN	--	--	--	--	0x13[1]	--
SYNC_SLAVE_EN	--	--	--	--	0x0D[3]	--
SYNC_FUNCTION_EN	--	--	--	--	0x0D[2]	--
Q0_CONTROL	--	--	--	--	0x0D[1:0]	--
IC_STAT	0x04[2:0]	--	--	--	--	--

15.2 Register Description

R: Read only

RC: Read and clear

RW: Read and write

RWSC: Read and write, also automatically set/clear by particular condition

Table 12. DEVICE_INFO

Address: 0x00 **Description:** DEVICE_INFO								
Bit	7	6	5	4	3	2	1	0
Field	DEVICE REVISION				Device ID			
Default	X	X	X	X	0	0	1	1
Type	R				R			

Bit	Name	WDT Reset	Reg Reset	Description
7:4	DEVICE REVISION	N	N	Device Revision
3:0	Device ID	N	N	Device ID 0011 = RT9758D

Table 13. FLAG_1

Address: 0x01 **Description:** FLAG_1								
Bit	7	6	5	4	3	2	1	0
Field	CON_OCP _FLAG	CFLY_ DIAG_ FLAG	VOUT_ INSERT_ FLAG	VBUS_ LOW_ ERR_ FLAG	VOUT_ ERR_ FLAG	WRX_ INSERT_ FALG	SWITCHING _ENABLED_ FLAG	VBUS_ INSERT _FLAG
Default	0	0	0	0	0	0	0	0
Type	RC	RC	RC	RC	RC	RC	RC	RC

Bit	Name	WDT Reset	Reg Reset	Description
7	CON_OCP_ FLAG	N	N	Set 1 and send an $\overline{INT}$ when converter current over than CON_OCP threshold. Clear upon read. 0: Normal 1: CON_OCP has occurred.
6	CFLY_DIAG_ FLAG	N	N	Set 1 and send an $\overline{INT}$ when CFLY short during converter soft-start in DIV2 or reverse DIV2 mode. Clear upon read. 0: Normal 1: CFLY_DIAG has occurred.
5	VOUT_ INSERT_FLAG	N	N	Set 1 and send an $\overline{INT}$ when VOUT voltage over than VOUT_INSERT threshold. Clear upon read. 0: Normal 1: VOUT_INSERT has occurred.
4	VBUS_LOW_ ERR_FLAG	N	N	Set 1 and send an $\overline{INT}$ when VBUS voltage lower than VBUS_LOW_ERR threshold. Clear upon read. 0: Normal 1: VBUS_LOW_ERR has occurred.
3	VOUT_ERR_ FLAG	N	N	Set 1 and send an $\overline{INT}$ when VOUT short during converter soft-start in DIV2 mode or bypass mode. Clear upon read. 0: Normal 1: VOUT_ERR has occurred.
2	WRX_ INSERT_FALG	N	N	Set 1 and send an $\overline{INT}$ when WRX_IN voltage over than WRX_INSERT threshold. Clear upon read. 0: Normal 1: WRX_INSERT has occurred.
1	SWITCHING_ENABLED_ FLAG	N	N	Set 1 and send an $\overline{INT}$ when the converter start working. Clear upon read. 0: Normal 1: Converter start switching.
0	VBUS_ INSERT_FLAG	N	Y	Set 1 and send an $\overline{INT}$ when VBUS voltage over than VBUS_INSERT threshold. Clear upon read. 0: Normal 1: VBUS_INSERT has occurred.

Table 14. FLAG_2

Address: 0x02 **Description:** FLAG_2								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_FLAG	VOUT_OVP_FLAG	Reserved			TDIE_OTP_EXIT_FLAG	TDIE_OTP_FLAG	WDT_FLAG
Default	0	0	0	0	0	0	0	0
Type	RC	RC	NA			RC	RC	RC

Bit	Name	WDT Reset	Reg Reset	Description
7	VBUS_OVP_FLAG	N	N	Set 1 and send an $\overline{INT}$ when VBUS voltage over than VBUS_OVP threshold. Clear upon read. 0: Normal 1: VBUS_OVP has occurred.
6	VOUT_OVP_FLAG	N	N	Set 1 and send an $\overline{INT}$ when VOUT voltage over than VOUT_OVP threshold. Clear upon read. 0: Normal 1: VOUT_OVP has occurred.
5:3	Reserved	NA	NA	Reserved
2	TDIE_OTP_EXIT_FLAG	N	N	Set 1 and send an $\overline{INT}$ when die temperature lower than TDIE_OTP release threshold after TDIE_OTP is triggered. Clear upon read. 0: Normal 1: TDIE_OTP_EXIT has occurred.
1	TDIE_OTP_FLAG	N	N	Set 1 and send an $\overline{INT}$ when die temperature over than TDIE threshold. Clear upon read. 0: Normal 1: TDIE_OTP has occurred.
0	WDT_FLAG	N	N	Set 1 and send an $\overline{INT}$ when watchdog timeout happen. Clear upon read. 0: Normal 1: WDT has occurred.

Table 15. FLAG_3

Address: 0x03 **Description:** FLAG_3								
Bit	7	6	5	4	3	2	1	0
Field	IBUS_OCP_FLAG	WRX_IRE_OCP_FLAG	Reserved					
Default	0	0	0	0	0	0	0	0
Type	RC	RC	NA					

Bit	Name	WDT Reset	Reg Reset	Description
7	IBUS_OCP_FLAG	N	N	Set 1 and send an $\overline{INT}$ when IBUS current over than IBUS_OCP threshold. Clear upon read. 0: Normal 1: IBUS_OCP has occurred.
6	WRX_IRE_OCP_FLAG	N	N	Set 1 and send an $\overline{INT}$ when current that from VBUS to WRX_IN over than WRX_IRE_OCP threshold. Clear upon read. 0: Normal 1: WRX_IRE_OCP has occurred.
5:0	Reserved	NA	NA	Reserved

Table 16. IC_STAT

Address: 0x04 **Description:** IC_STAT								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					IC_STAT		
Default	0	0	0	0	0	0	0	0
Type	NA					R		

Bit	Name	WDT Reset	Reg Reset	Description
7:3	Reserved	NA	NA	Reserved
2:0	IC_STAT	N	Y	Indicate converter operation status 000: Present mode (Default) 001: Standby mode 010: Forward DIV2 mode 011: Forward bypass mode 100: Reverse DIV2 mode 101: Reverse bypass mode 110: Charge Fault 111: Reserved

Table 17. MASK_1

Address: 0x05 **Description:** MASK_1								
Bit	7	6	5	4	3	2	1	0
Field	CON_OCP_MASK	CFLY_DIAG_MASK	VOUT_INSERT_MASK	VBUS_LOW_ERR_MASK	VOUT_ERR_MASK	WRX_INSERT_MASK	SWITCHING_ENABLED_MASK	VBUS_INSERT_MASK
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit	Name	WDT Reset	Reg Reset	Description
7	CON_OCP_MASK	N	Y	CON_OCP mask. 0: Not mask IRQ of CON_OCP_FLAG (Default) 1: Mask IRQ of CON_OCP_FLAG
6	CFLY_DIAG_MASK	N	Y	CFLY_DIAG mask. 0: Not mask IRQ of CFLY_DIAG_FLAG (Default) 1: Mask IRQ of CFLY_DIAG_FLAG
5	VOUT_INSERT_MASK	N	Y	VOUT_INSERT mask. 0: Not mask IRQ of VOUT_INSERT_FLAG (Default) 1: Mask IRQ of VOUT_INSERT_FLAG
4	VBUS_LOW_ERR_MASK	N	Y	VBUS_LOW_ERR mask. 0: Not mask IRQ of VBUS_LOW_ERR_FLAG (Default) 1: Mask IRQ of VBUS_LOW_ERR_FLAG
3	VOUT_ERR_MASK	N	Y	VOUT_ERR mask. 0: Not mask IRQ of VOUT_ERR_FLAG (Default) 1: Mask IRQ of VOUT_ERR_FLAG
2	WRX_INSERT_MASK	N	Y	WRX_INSERT mask. 0: Not mask IRQ of WRX_INSERT_FLAG (Default) 1: Mask IRQ of WRX_INSERT_FLAG
1	SWITCHING_ENABLED_MASK	N	Y	SWITCHING_ENABLED mask. 0: Not mask IRQ of SWITCHING_ENABLED_FLAG (Default) 1: Mask IRQ of SWITCHING_ENABLED_FLAG
0	VBUS_INSERT_MASK	N	Y	VBUS_INSERT mask. 0: Not mask IRQ of VBUS_INSERT_FLAG (Default) 1: Mask IRQ of VBUS_INSERT_FLAG

Table 18. MASK_2

Address: 0x06 **Description:** MASK_2								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_MASK	VOUT_OVP_MASK	Reserved			TDIE_OTP_EXIT_MASK	TDIE_OTP_MASK	WDT_MASK
Default	0	0	1	1	1	0	0	0
Type	RW	RW	NA			RW	RW	RW

Bit	Name	WDT Reset	Reg Reset	Description
7	VBUS_OVP_MASK	N	Y	VBUS_OVP mask. 0: Not mask IRQ of VBUS_OVP_FLAG (Default) 1: Mask IRQ of VBUS_OVP_FLAG
6	VOUT_OVP_MASK	N	Y	VOUT_OVP mask. 0: Not mask IRQ of VOUT_OVP_FLAG (Default) 1: Mask IRQ of VOUT_OVP_FLAG
5:3	Reserved	NA	NA	Reserved
2	TDIE_OTP_EXIT_MASK	N	Y	TDIE_OTP_EXIT mask. 0: Not mask IRQ of TDIE_OTP_EXIT_FLAG (Default) 1: Mask IRQ of TDIE_OTP_EXIT_FLAG
1	TDIE_OTP_MASK	N	Y	TDIE_OTP mask. 0: Not mask IRQ of TDIE_OTP_FLAG (Default) 1: Mask IRQ of TDIE_OTP_FLAG
0	WDT_MASK	N	Y	Watchdog timeout mask. 0: Not mask IRQ of WDT_FLAG (Default) 1: Mask IRQ of WDT_FLAG

Table 19. MASK_3

Address: 0x07 **Description:** MASK_3								
Bit	7	6	5	4	3	2	1	0
Field	IBUS_OCP_MASK	WRX_IRE_OCP_MASK	Reserved					
Default	0	0	1	1	1	1	1	1
Type	RW	RW	NA					

Bit	Name	WDT Reset	Reg Reset	Description
7	IBUS_OCP_MASK	N	Y	IBUS_OCP mask. 0: Not mask IRQ of IBUS_OCP_FLAG (Default) 1: Mask IRQ of IBUS_OCP_FLAG
6	WRX_IRE_OCP_MASK	N	Y	WRX_IRE_OCP mask. 0: Not mask IRQ of WRX_IRE_OCP_FLAG (Default) 1: Mask IRQ of WRX_IRE_OCP_FLAG
5:0	Reserved	NA	NA	Reserved

Table 20. STAT_1

Address: 0x08
Description: STAT_1

Bit	7	6	5	4	3	2	1	0
Field	Reserved			VOUT_INSERT_STAT	VBUS_LOW_ERR_STAT	WRX_INSERT_STAT	SWITCHING_ENABLED_STAT	VBUS_INSERT_STAT
Default	0	0	0	0	0	0	0	0
Type	NA			R	R	R	R	R

Bit	Name	WDT Reset	Reg Reset	Description
7:5	Reserved	NA	NA	Reserved
4	VOUT_INSERT_STAT	N	N	Set 1 when VOUT voltage above the VOUT_INSERT threshold. Persists until condition is no longer valid. 0: Normal 1: VOUT_INSERT is occurring.
3	VBUS_LOW_ERR_STAT	N	N	Set 1 when VBUS voltage below the VBUS_LOW_ERR threshold. Persists until condition is no longer valid. 0: Normal 1: VBUS_LOW_ERR is occurring.
2	WRX_INSERT_STAT	N	N	Set 1 when WRX_IN voltage above the WRX_INSERT threshold. Persists until condition is no longer valid. 0: Normal 1: WRX_INSERT is occurring.
1	SWITCHING_ENABLED_STAT	N	N	Set 1 and send an $\overline{INT}$ when the converter start working. Only one $\overline{INT}$ is sent when switching starts. Persists until condition is no longer valid. 0: Normal 1: SWITCHING is occurring.
0	VBUS_INSERT_STAT	N	N	Set 1 when VBUS voltage above the VBUS_INSERT threshold. Persists until condition is no longer valid. 0: Normal 1: VBUS_INSERT is occurring.

Table 21. STAT_2

Address: 0x09 **Description:** STAT_2								
Bit	7	6	5	4	3	2	1	0
Field	VBUS_OVP_STAT	VOUT_OVP_STAT	Reserved		IBUS_OCP_STAT	WRX_IRE_OCP_STAT	TDIE_OTP_STAT	WDT_STAT
Default	0	0	0	0	0	0	0	0
Type	R	R	NA		R	R	R	R

Bit	Name	WDT Reset	Reg Reset	Description
7	VBUS_OVP_STAT	N	N	Set 1 when VBUS voltage above the VBUS_OVP threshold. Persists until condition is no longer valid. 0: Normal 1: VBUS_OVP is occurring.
6	VOUT_OVP_STAT	N	N	Set 1 when VOUT voltage above the VOUT_OVP threshold. Persists until condition is no longer valid. 0: Normal 1: VOUT_OVP is occurring.
5:4	Reserved	NA	NA	Reserved
3	IBUS_OCP_STAT	N	N	Set 1 when IBUS current above the IBUS_OCP threshold. Persists until condition is no longer valid. 0: Normal 1: IBUS_OCP is occurring.
2	WRX_IRE_OCP_STAT	N	N	Set 1 when current that from VBUS to WRX_IN above the WRX_IRE_OCP threshold. Persists until condition is no longer valid. 0: Normal 1: WRX_IRE_OCP is occurring.
1	TDIE_OTP_STAT	N	N	Set 1 when die temperature over than TDIE_OTP threshold. Persists until condition is no longer valid. 0: Normal 1: TDIE_OTP is occurring.
0	WDT_STAT	N	N	0: WDT is counting. 1: WDT reset will occur after 32ms.

Table 22. CTRL_1

Address: 0x0A **Description:** CTRL_1								
Bit	7	6	5	4	3	2	1	0
Field	Reserved					VOUT_OVP		
Default	0	0	0	0	0	1	1	1
Type	NA					RW		

Bit	Name	WDT Reset	Reg Reset	Description
7:3	Reserved	NA	NA	Reserved
2:0	VOUT_OVP	Y	Y	VOUT overvoltage protection threshold. 000: 7V 001: 8V 010: 9V 011: 10V 100: 11V 101: 12V 110: 13V 111: 14V (Default)

Table 23. CTRL_2

Address: 0x0B **Description:** CTRL_2								
Bit	7	6	5	4	3	2	1	0
Field	Reserved		VBUS_OVP					
Default	0	0	1	1	1	0	1	1
Type	NA		RW					

Bit	Name	WDT Reset	Reg Reset	Description
7:6	Reserved	NA	NA	Reserved
5:0	VBUS_OVP	Y	Y	VBUS overvoltage protection threshold. VBUS_OVP = 7.25V + VBUS_OVP[5:0] x LSB LSB = 250mV Default = 22V (111011b)

Table 24. CTRL_3

Address: 0x0C **Description:** CTRL_3								
Bit	7	6	5	4	3	2	1	0
Field	IBUS_OCP				WRX_IRE_OCP			
Default	0	1	1	0	0	0	1	0
Type	RW				RW			

Bit	Name	WDT Reset	Reg Reset	Description
7:4	IBUS_OCP	Y	Y	IBUS overcurrent protection threshold. This current protection is bidirectional. 0000: Reserved 0001: Reserved 0010: 2A 0011: 2.5A 0100: 3A 0101: 3.5A 0110: 4A (Default) 0111: 4.5A 1000: 5A 1001: 5.5A 1010: 6A 1011: 6A 1100: 6A 1101: 6A 1110: 6A 1111: 6A
3:0	WRX_IRE_OCP	Y	Y	WRX reverse overcurrent protection threshold. 0000: 1A 0001: 1.5A 0010: 2A (Default) 0011: 2.5A 0100: 3A 0101: 3.5A 0110: 4A 0111: 4.5A 1000: 5A 1001: 5.5A 1010: 6A 1011: 6A 1100: 6A 1101: 6A 1110: 6A 1111: 6A

Table 25. CTRL_4

Address: 0x0D
Description: CTRL_4

Bit	7	6	5	4	3	2	1	0
Field	VBUS_PD_EN	WRX_PD_EN	SINGLE_PHASE_MODE_EN		SYNC_SLAVE_EN	SYNC_FUNCTION_EN	Q0_CONTROL	
Default	0	0	1	1	0	0	1	0
Type	RW	RW	RW		RW	RW	RW	

Bit	Name	WDT Reset	Reg Reset	Description
7	VBUS_PD_EN	N	Y	VBUS pull down resistor enable bit. 0: Pull down disable (Default) 1: Pull down enable
6	WRX_PD_EN	N	Y	WRX_IN pull down resistor enable bit. 0: Pull down disable (Default) 1: Pull down enable
5:4	SINGLE_PHASE_MODE_EN	N	Y	Select phase operation mode only in DIV2 or reverse DIV2 mode. It is strongly prohibited during operation. shall be determined before CHG_EN set 1. 00: Both A, B operating in synchronization 01: only Phase A operating 10: only Phase B operating 11: Both A, B operating in synchronization (Default)
3	SYNC_SLAVE_EN	N	Y	This bit is only effective in SYNC_FUNCTION_EN bit = 1. 0: Master (Default) 1: Slave
2	SYNC_FUNCTION_EN	N	Y	Enable or disable synchronization function. 0: Disable (Default) 1: Enable
1:0	Q0_CONTROL	Y/N	Y	Enable or disable Q0 MOSFET. If this bit set 10, Q0 turn on function is only valid in following conditions: WRX_IN voltage over than WRX_INSERT threshold and not exceed VBUS_OVP threshold with the $\overline{EN}$ pin pull low If this bit set 11, Q0 turn on function is only valid in following conditions: VBUS voltage over than VBUS_INSERT threshold with the $\overline{EN}$ pin pull low. If the device operates in bypass mode with BEHAVIOR_AFTER_WDT bit is 1, this bit will not be reset by WDT. 00: Disable (Q0 turn off) 01: Disable (Q0 turn off) 10: Enable (Q0 turn on) (default) 11: Enable (Q0 force turn on)

Table 26. CTRL_5

Address: 0x0E
Description: CTRL_5

Bit	7	6	5	4	3	2	1	0
Field	AUTO_ RECOVERY _EN	WDT			WDT_EN	OVERRIDE _WRX_OK _PIN_LOW	WRX_OK _EN	WRX_ OK_PSM
Default	1	1	0	0	0	0	1	0
Type	RW	RW			RW	RW	RW	RW

Bit	Name	WDT Reset	Reg Reset	Description
7	AUTO_RECOVERY_ EN	N	Y	Enable or disable auto recovery after OVP status be released. This bit is only effective in bypass mode. 0: Force standby mode 1: Enable AUTO_RECOVERY when the fault condition has been released. (Default)
6:4	WDT	N	Y	Watchdog timer setting. 000: 3.75s 001: 7.5s 010: 11.25s 011: 15s 100: 30s (Default) 101: 60s 110: 90s 111: 120s
3	WDT_EN	N	Y	Watchdog enable. 0: Disable (Default) 1: Enable
2	OVERRIDE_WRX_ OK_PIN_LOW	N	Y	Enable or disable override function to change status of WRX_OK pin from high to low or from low to high as long as WRX_IN > WRX_INSERT and WRX_OK_EN = 1. 0: Disable (Status of WRX_OK pin changes from low to high once the bit is rest to 0 from 1.) (Default) 1: Enable override (The status of WRX_OK pin is changed from high to low manually.)
1	WRX_OK_EN	N	Y	Enable or disable WRX_OK pin function. 0: Disable 1: Enable (Default)
0	WRX_OK_PSM	N	Y	Enable or disable WRX_OK pin function in present mode. 0: Disable (Default) 1: Enable

Table 27. CTRL_6

Address: 0x0F
Description: CTRL_6

Bit	7	6	5	4	3	2	1	0
Field	IN_VALID_ RECOVERY _DEGLITCH	SPREAD_ SPECTRUM	FSW			CHG_ EN	REVERSE _MODE_ EN	OPERATION _MODE_ SELECTION
Default	0	0	1	0	0	1	0	1
Type	RW	RW	RW			RW	RW	RW

Bit	Name	WDT Reset	Reg Reset	Description
7	IN_VALID_ RECOVERY_DEGLITCH	N	Y	This bit only sets the deglitch time of fault recovery from the OVP event in bypass mode. 0: 21ms (Default) 1: 100ms
6	SPREAD_SPECTRUM	N	Y	Adjust switching frequency for EMI reduction. 0: Normal (Default) 1: Enable spread spectrum
5:3	FSW	N	Y	Set switching frequency in DIV2 and reverse DIV2 mode. 000: 300kHz 001: 450kHz 010: 600kHz 011: 900kHz 100: 500kHz (Default) 101: 750kHz 110: 1000kHz 111: 1500kHz
2	CHG_EN	Y/N	Y	Enable converter (default = 1). If this bit is 0, converter in standby mode. If the device operates in bypass mode with BEHAVIOR_AFTER_WDT bit is 1, this bit will not be reset by WDT. 0: Disable 1: Enable (Default)
1	REVERSE_MODE_EN	N	Y	This bit decides converter direction of power delivery. If this set to 1 and OPERATION_MODE_SELECTION set to 1, converter will operate in reverse DIV2 mode. If this set to 1 and OPERATION_MODE_SELECTION set to 0, converter will operate in reverse bypass mode. 0: Converter operate in forward of power delivery (Default) 1: Converter operate in reverse of power delivery
0	OPERATION_MODE_ SELECTION	N	Y	This bit selects converter operation mode. 0: Bypass mode 1: DIV2 mode (Default)

Table 28. CTRL_7

Address: 0x10
Description: CTRL_7

Bit	7	6	5	4	3	2	1	0
Field	PHASE_A_ANGLE		PHASE_B_ANGLE		AT_FUNCTION_EN	AT_FUNCTION		
Default	0	0	1	0	0	1	0	0
Type	RW		RW		RW	RW		

Bit	Name	WDT Reset	Reg Reset	Description
7:6	PHASE_A_ANGLE	N	Y	Select phase A angle in DIV2 or reverse DIV2 mode. It is strongly prohibited during operation. shall be determined before CHG_EN set 1. If the RT9758D operate in single application, recommend this bit set to 00. If the RT9758D operate in parallel application, recommend this bit set to 00 in Master mode. If the RT9758D operate in parallel application, recommend this bit set to 01 in Slave mode. 00: 0 degrees (Default) 01: 90 degrees 10: 180 degrees 11: 270 degrees
5:4	PHASE_B_ANGLE	N	Y	Select phase B angle in DIV2 or reverse DIV2 mode. It is strongly prohibited during operation. shall be determined before CHG_EN set 1. If the RT9758D operate in single application, recommend this bit set to 10. If the RT9758D operate in parallel application, recommend this bit set to 10 in Master mode. If the RT9758D operate in parallel application, recommend this bit set to 11 in Slave mode. 00: 0 degrees 01: 90 degrees 10: 180 degrees (Default) 11: 270 degrees
3	AT_FUNCTION_EN	N	Y	Enable or disable auto transition function that make converter mode change between bypass mode and DIV2 mode automatically. 0: Disable (Default) 1: Enable
2:0	AT_FUNCTION	N	Y	Auto transition function threshold. 000: 9V 001: 9.5V 010: 10V 011: 10.5V 100: 11V (Default) 101: 11.5V 110: 12V 111: 12V

Table 29. CTRL_8

Address: 0x11 **Description:** CTRL_8								
Bit	7	6	5	4	3	2	1	0
Field	CFLY_DIAG_TIME		PRECHARGE_CURRENT		VOUT_ERR_ON_TIME		VOUT_ERR_OFF_TIME	BEHAVIOR_AFTER_WDT
Default	1	1	1	1	1	1	0	1
Type	RW		RW		RW		RW	RW

Bit	Name	WDT Reset	Reg Reset	Description
7:6	CFLY_DIAG_TIME	N	Y	Program pre-charge timing of CFLY in DIV2 mode or reverse DIV2 mode. In DIV2 mode, pre-charge timing of CFLY is sum of CFLY_DIAG_TIME and VOUT_ERR_ON_TIME. In reverse DIV2 mode, pre-charge timing of CFLY depends on CFLY_DIAG_TIME. 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms (Default)
5:4	PRECHARGE_CURRENT	N	Y	Program VOUT or CFLY pre-charge current in soft-start period. 00: Reserved 01: 330mA 10: 500mA 11: 660mA (Default)
3:2	VOUT_ERR_ON_TIME	N	Y	Program pre-charge timing of VOUT in bypass mode and DIV2 mode. In DIV2 mode, pre-charge timing of VOUT is sum of CFLY_DIAG_TIME and VOUT_ERR_ON_TIME. In bypass mode, pre-charge timing of VOUT depends on VOUT_ERR_ON_TIM. 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms (Default)
1	VOUT_ERR_OFF_TIME	N	Y	Program a turn off timing after VOUT_ERR is triggered in bypass mode. 0: 40ms (Default) 1: 80ms
0	BEHAVIOR_AFTER_WDT	N	Y	Select the converter behavior of converter after trigger watchdog timeout event. 0: Converter will enter standby mode and Q0_CONTROL set to 00 after WDT is triggered 1: Only when in bypass mode, the converter will keep the same mode as before, after WDT is triggered. (Default)

Table 30. CTRL_9

Address: 0x12 **Description:** CTRL_9								
Bit	7	6	5	4	3	2	1	0
Field	DISABLE_ VOUT_ OVP	DISABLE_ VBUS_ OVP	DISABLE_ TDIE_ OTP	DISABLE_ IBUS_ OCP	DISABLE_ WRX_IRE_ OCP	REG_ RST	Reserved	
Default	0	0	0	0	0	0	0	0
Type	RW	RW	RW	RW	RW	RWSC	NA	

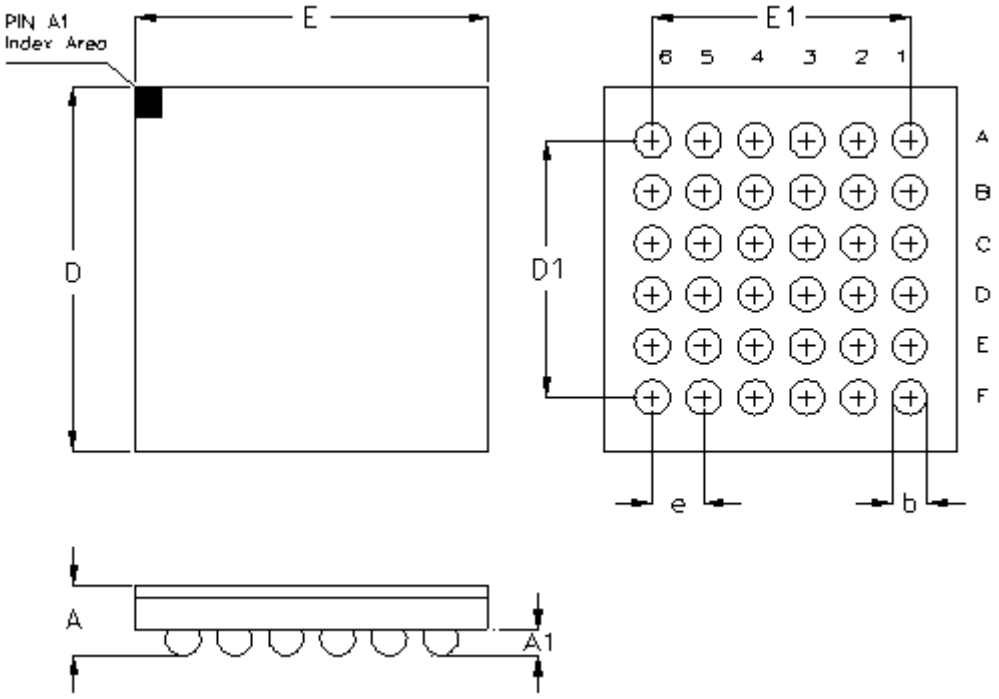
Bit	Name	WDT Reset	Reg Reset	Description
7	DISABLE_ VOUT_OVP	Y	Y	Enable or disable VOUT_OVP function. 0: Enable (Default) 1: Disable
6	DISABLE_ VBUS_OVP	Y	Y	Enable or disable VBUS_OVP function. 0: Enable (Default) 1: Disable
5	DISABLE_ TDIE_OTP	Y	Y	Enable or disable TDIE_OTP function. 0: Enable (Default) 1: Disable
4	DISABLE_ IBUS_OCP	Y	Y	Enable or disable IBUS_OCP function. 0: Enable (Default) 1: Disable
3	DISABLE_ WRX_IRE_ OCP	Y	Y	Enable or disable WRX_IRE_OCP function. 0: Enable (Default) 1: Disable
2	REG_RST	N	Y	Register reset 0: No action (Default) 1: Reset register (Notice: Back to 0 after register reset)
1:0	Reserved	NA	NA	Reserved

Table 31. CTRL_10

Address: 0x13 **Description:** CTRL_10								
Bit	7	6	5	4	3	2	1	0
Field	Reserved						VOUT_PD_EN	Reserved
Default	0	0	0	0	0	0	0	0
Type	NA						RW	NA

Bit	Name	WDT Reset	Reg Reset	Description
7:2	Reserved	NA	NA	Reserved
1	VOUT_PD_EN	N	Y	Once VOUT_PD_EN = 1 is set, the Enable state remains valid until the user changes it to 0 (Disable) or changes REG_RST 0x12[2] or the IC is reset even if CHG_EN = 0. Enable pull-down resistor for discharge VOUT voltage. 0: Not discharge (Default) 1: Enable discharge
0	Reserved	NA	NA	Reserved

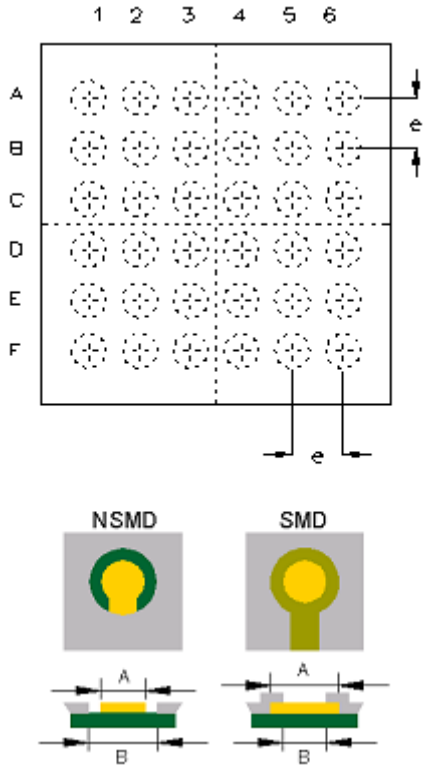
16 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.800	2.880	0.110	0.113
D1	2.000		0.079	
E	2.700	2.780	0.106	0.109
E1	2.000		0.079	
e	0.400		0.016	

36B WL-CSP 2.74x2.84 Package (BSC)

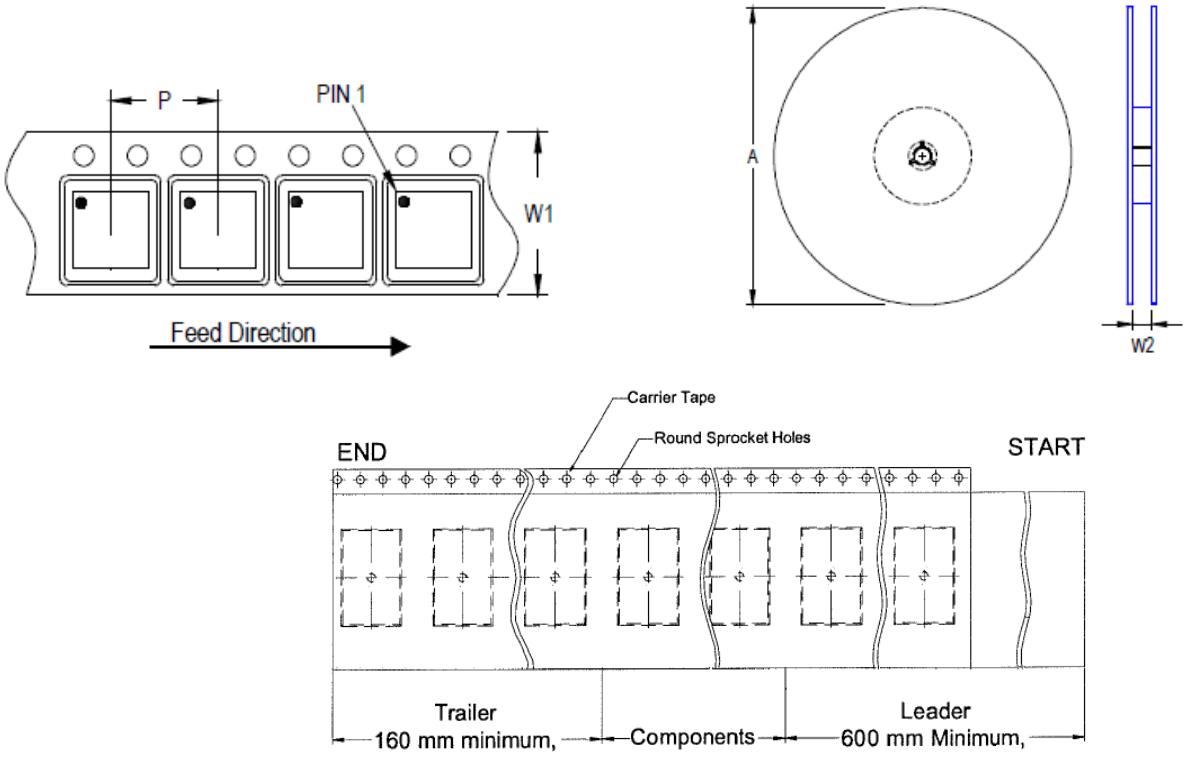
17 Footprint Information



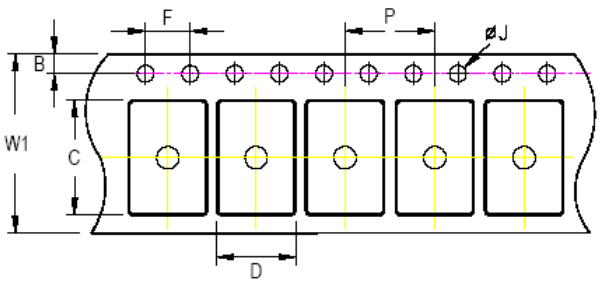
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.74x2.84-36(BSC)	36	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

18 Packing Information

18.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.74x2.84	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.74x2.84	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/3	Final	Marking Information on P1