8A Single Cell Smart Cap Divider and Direct Charge Charger with 8-Channel ADC, USB BC 1.2 Detection

1 General Description

The RT9756A is a high-efficiency and high charge current charger. The efficiency is up to 98.2% when V_{BAT} = 4V, I_{BAT} = 2A with a maximum charge current of up to 8A in DIV2 mode. In bypass mode, the efficiency is up to 99.1% when V_{BAT} = 4V and I_{BAT} = 1A, with a maximum charger current of up to 5A. The device integrates smart cap divider topology, direct charging mode, external overvoltage protection control, an input reverse blocking N-MOSFET and 2-way regulation, a dual-phase charge pump core, 14-way protection, 9-way system alarm, 8-channel high-speed analog-to-digital converter and USB BC 1.2 detection. The high-speed analog-to-digital converter provides input and output voltage, current, and temperature information to the host, which can be monitored via the I^2C serial interface.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Applications

- Smart Phones
- Tablets

3 Ordering Information

RT9756A □□

Pin 1 Orientation
Empty: Quadrant 1
(2): Quadrant 2, Follow EIA-481

Package Type(1)
WSC: WL-CSP-36B 2.8x2.8 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

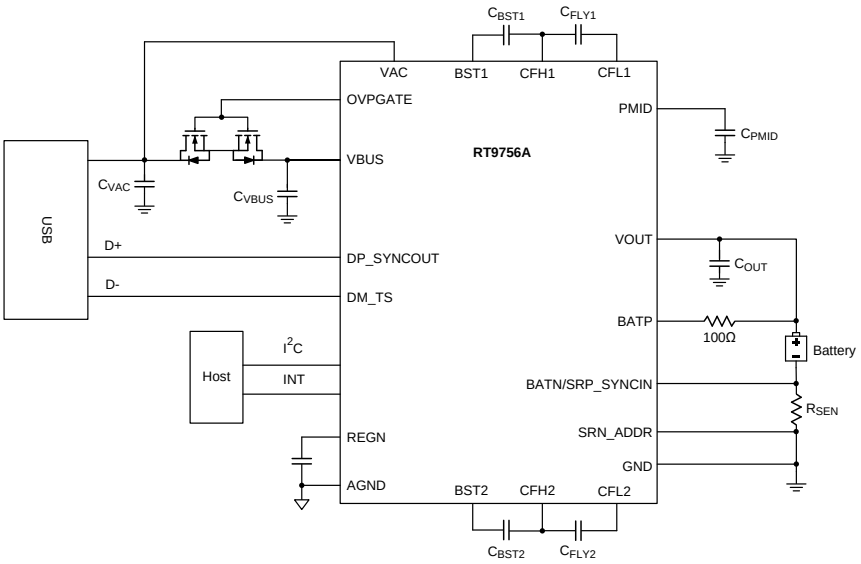
4 Features

- **Integrate Cap Divider Mode (DIV2 Mode) and Direct Charging Mode (Bypass Mode)**
- **Support USB BC1.2**
- **External OVP MOS Control and Regulation**
  - **High Absolute Maximum Rating of 37V**
  - **100ns Fast Reaction Time and 100ns Fast Turn-Off Time**
  - **VBAT Voltage Regulation (VBAT REG)**
  - **IBAT Current Regulation (IBAT REG)**
- **Dual-Phase Charge Pump Core**
  - **8A Output Current Capability**
  - **Efficiency up to 98.2% when V_{BAT} = 4V, I_{BAT} = 2A (DIV2 Mode)**
  - **Efficiency Up to 99.1% when V_{BAT} = 4V, I_{BAT} = 1A (Bypass Mode)**
  - **100kHz to 1000kHz Variable Switching Frequency Stay Out of Audio Band**
  - **Spread Spectrum Technology for EMI Reduction**
- **8-Channel 12-bit ADC**
  - **High Speed Data Rate for 128 Times Average Per Channel**
  - **8-Channel (VBUS, IBUS, VOUT, VBAT, IBAT, TDIE, DP, DM) for Voltage/Current/Temperature Measurement**
- **Input Reverse Blocking N-MOSFET**
  - **Block the Reverse Current**
- **3-Error Charge Pump Switch Protection**
- **11-Way System Protection**
- **9-Way System Alarm**

5 Marking Information

31: Product Code
XXYY: Wafer ID with Check Sum
CCC-RRR: IC Coordinate (X, Y)
YMDNN: Date Code

6 Simplified Application Circuit



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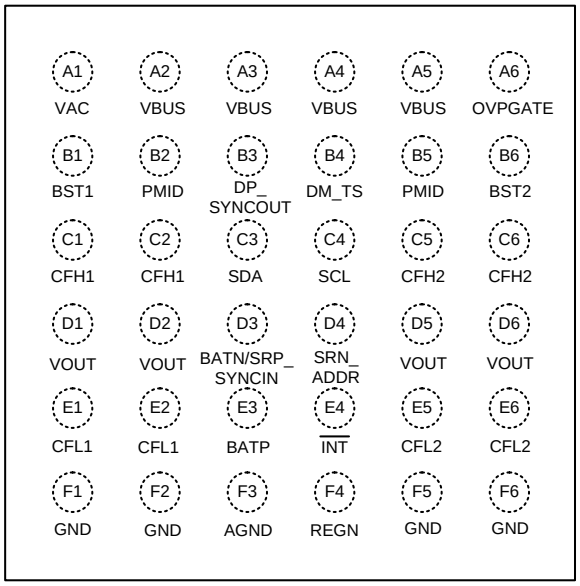
7 Pin Configuration

(TOP VIEW)



WL-CSP-36B 2.8x2.8 (BSC)

8 Functional Pin Description

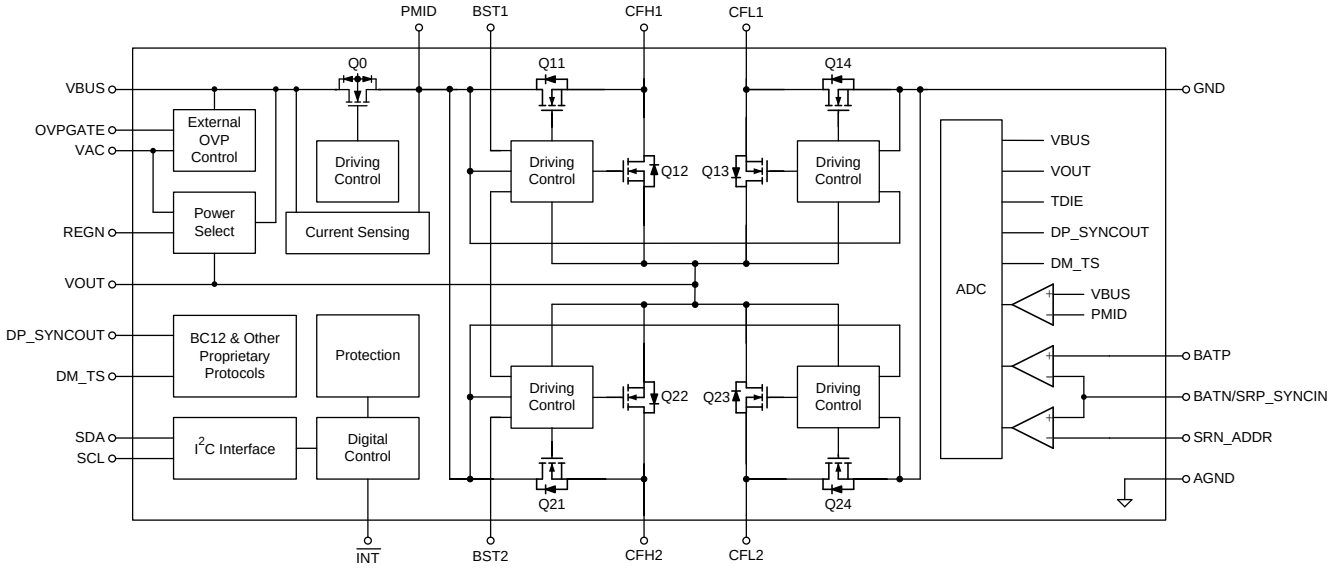
Pin No.	Pin Name	I/O	Pin Function
A1	VAC	AI	Input voltage sense pin. Connect to VBUS if the external N-MOSFET is not used.
A2, A3, A4, A5	VBUS	P	These pins are the input power supply and must be connected on the PCB. A 2.2μF capacitor must be connected from VBUS to GND and placed close to these pins.
A6	OVPGATE	AO	External N-MOSFET control pin. Connect to the gate of the external N-MOSFET.
B1	BST1	P	The high-side MOSFET driver positive supply. A 0.1μF capacitor must be connected from BST1 to CFH1 and placed as close as possible to the device.
B2, B5	PMID	P	Connected to the drain of the reverse blocking N-MOSFET. A 10μF capacitor must be connected from PMID to GND and placed as close as possible to the device.
B3	DP_ SYNCOUT	AIO	Positive line of the USB data line pair. Support DP/DM-based USB host and charging port detection. In a parallel configuration, connect this pin to the BATN/SRP_SYNCIN pin of the slave.
B4	DM_TS	AIO	Negative line of the USB data line pair. Support DP/DM-based USB host and charging port detection. This pin also functions as a temperature sensing input, requiring an external NTC thermistor, resistor divider and voltage reference.
B6	BST2	P	Positive supply for the high-side MOSFET driver. A 0.1μF capacitor must be connected from BST2 to CFH2 and placed as close as possible to the device.
C1, C2	CFH1	P	Flying capacitor positive node. Three 22μF capacitors must be connected from CFL1 to CFH1 and placed as close as possible to the device. These pins must be connected on the PCB.

Pin No.	Pin Name	I/O	Pin Function
C3	SDA	DIO	I^2C serial data line. Connect to the pull-up voltage via a 10kΩ pull-up resistor.
C4	SCL	DI	I^2C serial clock line. Connect to the pull-up voltage via a 10kΩ pull-up resistor.
C5, C6	CFH2	P	Flying capacitor positive node. Three 22μF capacitors must be connected from CFL2 to CFH2 and placed as close as possible to the device. These pins must be connected on the PCB.
D1, D2, D5, D6	VOUT	P	Power supply. Connect to the positive terminal of the battery pack. These pins must be connected on the PCB. Two 10μF capacitors must be connected from VOUT to GND and placed as close as possible to the device.
D3	BATN/SRP_SYNCIN	AI	Negative input for battery voltage sensing and positive input for battery current sensing. Place a 5mΩ or 2mΩ resistor between BATN/SRP_SYNCIN and SRN_ADDR. If battery current sensing is not used, connect a 100Ω resistor in series with the negative terminal of the battery pack. In a parallel configuration, connect this pin to the DP_SYNCOUT pin of the master.
D4	SRN_ADDR	AI	Negative input for battery current sensing. Place a 5mΩ or 2mΩ resistor between SRN_ADDR and BATN/SRP_SYNCIN. Connect SRN_ADDR to GND to set the slave address to 0x6F, or float SRN_ADDR to set slave address to 0x6E. To set slave address to 0x6E, the parasitic capacitance of the SRN_ADDR pin must be less than 100pF.
E1, E2	CFL1	P	Flying capacitor negative node. Three 22μF capacitors must be connected from CFL1 to CFH1 and placed as close as possible to the device. These pins must be connected on the PCB.
E3	BATP	AI	Positive input for battery voltage sensing. Connect a 100Ω resistor in series with the positive terminal of the battery pack.
E4	$\overline{INT}$	DO	Open-drain interrupt output. Connect to the pull-up voltage via a 10kΩ pull-up resistor. Normally high, when an event occurs, the $\overline{INT}$ pin sends a 256μs low pulse to the system.
E5, E6	CFL2	P	Flying capacitor negative node. Three 22μF capacitors must be connected from CFL2 to CFH2 and placed as close as possible to the device. These pins must be connected on the PCB.
F1, F2, F5, F6	GND	P	Power ground.
F3	AGND	AI	Analog ground.
F4	REGN	AO	Internal LDO output. This pin is the internal power supply VDDA. A 4.7μF capacitor must be connected from REGN to AGND and placed as close as possible to the device. Do not use this pin for other function.

8.1 I/O Type Definition

- DIO: Digital Input/Output Pin
- DI: Digital Input Pin
- DO: Digital Output Pin
- AIO: Analog Input/Output Pin
- AI: Analog Input Pin
- AO: Analog Output Pin
- P: Power Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Pin Voltage, VAC ---------- –0.3V to 37V
- Supply Pin Voltage, VBUS ---------- –0.3V to 22V
- Supply Pin Voltage, VOUT ---------- –0.3V to 6V
- Control Pin Voltage, OVPGATE (Note 3) ---------- –0.3V to 37V
- Terminal Pin Voltage, OVPGATE to VBUS ---------- –22V to 14V
- Terminal Pin Voltage, PMID ---------- –0.3V to 14V
- Terminal Pin Voltage, DP_SYNCOUT, DM_TS ---------- –0.3V to 6V
- Terminal Pin Voltage, BST1, BST2 ---------- –0.3V to 18V
- Terminal Pin Voltage, BST1 to CFH1, BST2 to CFH2 ---------- –0.3V to 14V
- Terminal Pin Voltage, CFH1, CFH2 ---------- –0.3V to 12V
- Terminal Pin Voltage, CFL1, CFL2 ---------- –0.3V to 6V
- Terminal Pin Voltage, PMID to CFH1, PMID to CFH2 ---------- –0.3V to 6V
- Terminal Pin Voltage, CFH1 to VOUT, CFH2 to VOUT ---------- –0.3V to 6V
- Terminal Pin Voltage, CFH1 to CFL1, CFH2 to CFL2 ---------- –0.3V to 6V
- Terminal Pin Voltage, VOUT to CFL1, VOUT to CFL2 ---------- –0.3V to 6V
- Terminal Pin Voltage, $\overline{INT}$, SDA, SCL, REGN ---------- –0.3V to 6V
- Terminal Pin Voltage, BATP, BATN/SRP_SYNCIN ---------- –0.3V to 6V
- Terminal Pin Voltage, SRN_ADDR ---------- –0.3V to 6V
- Terminal Pin Voltage, BATN/SRP_SYNCIN to SRN_ADDR ---------- –0.5V to 0.5V
- Terminal Pin Voltage, GND to AGND ---------- –0.5V to 0.5V
- Terminal Pin Current, $\overline{INT}$ ---------- 0mA to 6mA
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-36B 2.8x2.8 (BSC) ---------- 3.42W
- Package Thermal Resistance (Note 4)

  WL-CSP-36B 2.8x2.8 (BSC), θ_{JA} ---------- 29.26°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model), per ANSI/ESDA/JEDEC JS-001 ---------- ±2kV

  CDM (Charged Device Model), per JEDEC Specification JESD22-C101 ---------- ±500V

  Latch-Up ---------- ±100mA

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. For testing the absolute maximum rating of the OVPGATE pin, the VBUS pin should initially be powered on with 20V. After VBUS has maintained 20V for 25.6ms, the OVPGATE can be biased.

Note 4. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- Supply Pin Voltage Range, VAC ---------- 3V to 17V
- Supply Pin Voltage Range (Device in Operating Mode), VAC ---------- 3V to 12V
- Supply Input Voltage Range (Device in DIV2 Mode), VBUS, ---------- 6V to 11V
- Supply Input Voltage Range (Device in Bypass Mode), VBUS ---------- 3V to 5V
- Output Voltage Range, VOUT---------- 3V to 5V
- Positive Flying Capacitor Voltage Range, CFH1, CFH2---------- 0V to 11V
- Negative Flying Capacitor Voltage Range, CFL1, CFL2 ---------- 0V to 5V
- Voltage Range Across Q11 and Q21, PMID to CFH1, PMID to CFH2---------- 0V to 5V
- Voltage Range Across Q12 and Q22, CFH1 to VOUT, CFH2 to VOUT ---------- 0V to 5V
- Voltage Range Across Q13 and Q23, VOUT to CFL1, VOUT to CFL2 ---------- 0V to 5V
- Analog Sense Voltage Range, BATP ---------- 0V to 5V
- Analog Sense Voltage Range, BATN/SRP_SYNCIN, SRN_ADDR ---------- 0V to 0.04V
- Battery Positive and Negative Voltage Sense Range, BATP to BATN/SRP_SYNCIN---------- 0V to 5V
- I/O Control Voltage Range, SDA, SCL, $\overline{INT}$ ---------- 0V to 5V
- I/O Control Voltage Range, DP_SYNCOUT, DM_TS ---------- 0V to 3.3V
- Input Current Range (Device in DIV2 Mode), IBUS---------- 0A to 4A
- Input Current Range (Device in Bypass Mode), IBUS ---------- 0A to 5A
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 6. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
External OVP Control						
OVPGATE Voltage	$V_{OVPGATE}$	Operation voltage $V_{OVPGATE}$ – V_{BUS}. V_{AC} = 3V to 3.5V or V_{BUS} = 3V to 3.5V. Set by Register 0x0004[0] = 1.	7	10	11	V
		Operation voltage $V_{OVPGATE}$ – V_{BUS}. V_{AC} = 3.5V to 9V or V_{BUS} = 3.5V to 9V. Set by Register 0x0004[0] = 1.	9	10	11	
		Operation voltage $V_{OVPGATE}$ – V_{BUS}. V_{AC} = 3V to 9V or V_{BUS} = 3V to 9V. Set by Register 0x0004[0] = 0.	4.5	4.8	5.1	
VAC Insert Threshold	V_{AC_INSERT}	V_{AC} rising threshold to turn on external MOS	2.6	2.8	3	V
VAC Insert Threshold Rising Deglitch Time	$t_{VAC\_INSERT\_RIS\_DEG}$	Deglitch between V_{AC} over V_{AC_INSERT} threshold and sent an $\overline{INT}$.	--	1	--	ms
VAC Insert Hysteresis	$V_{AC\_INSERT\_HYS}$	V_{AC} falling hysteresis to turn off external MOS	250	500	750	mV
VBUS Insert Threshold	V_{BUS_INSERT}	V_{BUS} rising threshold to turn on external MOS	2.65	2.8	2.95	V
VBUS Insert Threshold Rising Deglitch Time	$t_{DEGLITCH\_VBUS\_INSERT\_R}$		--	17	--	µs
VBUS Insert Hysteresis	$V_{BUS\_INSERT\_HYS}$	V_{BUS} falling hysteresis to turn off external MOS	50	150	250	mV
VAC Insert Deglitch Time	$t_{DEGLITCH\_VAC\_INSERT}$	V_{OUT} < V_{OUT_INSERT}. Deglitch time between V_{AC} higher than V_{AC_INSERT} threshold and start to turn on external MOS. (Note 7)	22	25	28	ms
		V_{OUT} > V_{OUT_INSERT}. Deglitch time between V_{AC} higher than V_{AC_INSERT} threshold and start to turn on external MOS. (Note 7)	20	22	24	
VAC OVP Range	$V_{AC\_OVP\_RAN}$	I^2C programmable, 3-bit DAC, 6.5V, 11V to 17V (Note 8)	6.5	--	17	V
VAC OVP Accuracy	$V_{AC\_OVP\_ACC}$	V_{AC_OVP} threshold accuracy	–2	--	2	%
VAC OVP Hysteresis	$V_{AC\_OVP\_HYS}$	V_{AC} falling to turn on the external MOS after VAC OVP occurs.	250	500	750	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVPGATE Reaction Time	$t_{VAC\_OVP\_RE}$	Duration between V_{AC} exceeding the V_{AC_OVP} threshold and OVPGATE starting to turn off the external MOSFET. V_{AC_OVP} is set to 17V with a V_{AC} slew rate = 12V/μs, and V_{AC} rises from 5V to 22V. (Note 7)	--	100	--	ns
OVPGATE Turn-Off Time	$t_{VAC\_OVP\_OFF}$	Duration between OVPGATE starting to turn off the external MOSFET and the external MOSFET being fully turned off, with C_{GS} = 4nF. (Note 7)	--	100	--	ns
Regulation Time Out	$t_{REG\_TIMEOUT}$	If device is in regulation and no VDR_OVP occurs during this time, the device will stop charge.	585	650	715	ms
Power Select and Source						
VBUS Quiescent Current	I_{Q_VBUS}	ADC disable, charge disable, OVPGATE disable, VBUS and VAC are open, VOUT no present, no VBUS_OVP happen. Measure quiescent current on VBUS. V_{BUS} = 3V to 12V.	--	250	300	μA
VAC Quiescent Current	I_{Q_VAC}	ADC disable, charge disable, OVPGATE disable, VOUT no present. Measure quiescent current on VAC. V_{AC} = 12V, V_{BUS} = 0V.	--	250	300	μA
		ADC disable, charge disable, OVPGATE enable, VOUT no present, no VAC_OVP happen. Measure quiescent current on VAC. V_{AC} = 0V to 12V.	--	650	--	μA
		ADC enable, charge disable, OVPGATE enable, VOUT no present. Measure quiescent current on VAC. V_{AC} = 3V to 12V.	--	3	4	mA
VOUT Quiescent Current	I_{Q_VOUT}	ADC disable, charge disable. VAC no present. EN_I2C_LEVEL_DETECTION = 0, V_{OUT} falling from 4.5V to 0V. Measure quiescent current on VOUT.	--	5	10	μA
		ADC enable, charge disable. VAC no present. Measure quiescent current on VOUT. V_{OUT} = 0V to 4.5V.	--	2	3	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDA UVLO Threshold	V_{DDA_UVLO}	V_{DDA} rising	2.45	2.6	2.75	V
VDDA UVLO Hysteresis	$V_{DDA\_UVLO\_HYS}$	V_{DDA} falling to turn off REGN and stop ADC function.	100	250	400	mV
VDDA UVLO Falling Threshold	$V_{DDA\_UVLO\_F}$	V_{DDA} falling to stop I^2C work.	--	2	--	V
Device Wake Up Time	t_{WAKE_UP}	Duration time between V_{DDA} > V_{DDA_UVLO} threshold and the device being able to start I^2C communicate.	--	--	2.5	ms
Soft-Start Time	t_{SS}	Duration time between CHG_EN = 1 and the device start switching	--	--	92	ms
VOUT Insert Threshold	V_{OUT_INSERT}	V_{OUT} rising	2.65	2.8	2.95	V
VOUT Insert Threshold Rising Deglitch Time	$t_{DEGLITCH\_VOUT\_INSERT\_R}$		--	17	--	µs
VOUT Insert Hysteresis	$V_{OUT\_INSERT\_HYS}$	V_{OUT} falling	50	150	250	mV
Cap Divider Charger						
Q0 On-Resistance	R_{DSON_Q0}	DIV2 mode, charge enable. V_{BUS} = 9V, V_{OUT} = 4.5V.	--	7.1	11	mΩ
Q11, Q21 On-Resistance	R_{DSON_Q11}, R_{DSON_Q21}	DIV2 mode, charge enable. V_{BUS} = 9V, V_{OUT} = 4.5V.	--	12	19	mΩ
Q12, Q22 On-Resistance	R_{DSON_Q12}, R_{DSON_Q22}	DIV2 mode, charge enable. V_{BUS} = 9V, V_{OUT} = 4.5V.	--	9.5	13	mΩ
Q13, Q23 On-Resistance	R_{DSON_Q13}, R_{DSON_Q23}	DIV2 mode, charge enable. V_{BUS} = 9V, V_{OUT} = 4.5V.	--	12.5	19.5	mΩ
Q14, Q24 On-Resistance	R_{DSON_Q14}, R_{DSON_Q24}	DIV2 mode, charge enable. V_{BUS} = 9V, V_{OUT} = 4.5V.	--	11	17	mΩ
Bypass Mode On-Resistance (VBUS to VOUT)	$R_{DSON\_BYPASS\_MODE}$	Bypass mode, charge enable. V_{OUT} = 4.5V.	--	17.85	27	mΩ
Charge Switch Frequency Range	f_{SW}		100	--	1000	kHz
Charge Switch Frequency Step Size	f_{SW_SIZE}		--	100	--	kHz
Charge Switch Frequency Accuracy	f_{SW_ACC}	f_{SW} = 200kHz to 1000kHz	–10	--	10	%
Protection						
VBAT OVP Range	$V_{BAT\_OVP\_RAN}$	Rising	4.2	--	4.975	V
VBAT OVP Step Size	$V_{BAT\_OVP\_SIZE}$		--	25	--	mV
VBAT OVP Accuracy	$V_{BAT\_OVP\_ACC}$	V_{BAT_OVP} = 4.4V to 4.55V	–1	--	1	%
		V_{BAT_OVP} = 4.2V to 4.65V	–1.5	--	1.5	
VBAT OVP Deglitch Time	$t_{DEGLITCH\_VBAT\_OVP}$		--	3	--	µs
BATP Leakage Current	I_{BATP_LK}		--	--	1.2	µA
BATN Leakage Current	I_{BATN_LK}		--	--	1	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBAT OCP Range	$I_{BAT\_OCP\_RAN}$	Rising	2	--	8.3	A
IBAT OCP Step Size	$I_{BAT\_OCP\_SIZE}$		--	100	--	mA
IBAT OCP Accuracy	$I_{BAT\_OCP\_ACC}$	I_{BAT_OCP} = 3A to 8A, R_{SEN} = 0.002Ω	–200	--	200	mA
IBAT OCP Deglitch Time	$t_{DEGLITCH\_IBAT\_OCP}$		--	50	--	µs
VBUS OVP Range	$V_{BUS\_OVP\_RAN}$	DIV2 mode. V_{BUS} rising.	6	--	12.3	V
		Bypass mode. V_{BUS} rising.	3	--	6.15	
VBUS OVP Step Size	$V_{BUS\_OVP\_SIZE}$	DIV2 mode	--	100	--	mV
		Bypass mode		50		
VBUS OVP Accuracy	$V_{BUS\_OVP\_ACC}$	DIV2 mode, V_{BUS_OVP} = 8.9V to 11.5V	–1	--	1	%
		Bypass mode, V_{BUS_OVP} = 4.2V to 5V	–1	--	1	
VBUS OVP Hysteresis	$V_{BUS\_OVP\_HYS}$	DIV2 mode. V_{BUS} falling.	--	500	--	mV
		Bypass mode. V_{BUS} falling.	--	200	--	
VBUS OVP Rising Reaction Time	$t_{VBUS\_OVP\_R\_RE}$	V_{BUS} rising slope with 10V/µs. ADC enable. Duration between V_{BUS} exceeding the V_{BUS_OVP} threshold and the device starting to turn off the charger and reverse the body diode of Q0. (Note 7)	--	0.1	--	µs
VBUS OVP Falling Reaction Time	$t_{VBUS\_OVP\_F\_RE}$	V_{BUS} rising slope with –10V/µs. ADC enable. During between V_{BUS} under $V_{BUS\_OVP\_HYS}$ threshold and the body diode of Q0 start to be turned forward. (Note 7)	--	0.1	--	µs
IBUS OCP Range	$I_{BUS\_OCP\_RAN}$	Rising	1	--	5.5	A
IBUS OCP Step Size	$I_{BUS\_OCP\_SIZE}$		--	250	--	mA
IBUS OCP Accuracy	$I_{BUS\_OCP\_ACC}$		–100	--	100	mA
IBUS OCP Deglitch	$t_{IBUS\_OCP\_DEG}$		--	50	--	µs
IBUS OCP_H Threshold	$I_{BUS\_OCP\_H}$	Rising (Note 7)	--	6.8	--	A
IBUS OCP_H Reaction Time	$t_{IBUS\_OCP\_H\_RE}$	Duration between IBUS exceeding the IBUS_OVP_H threshold and device starting to turn off charger. (Note 7)	--	2	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBUS UCP Rising Accuracy	$I_{BUS\_UCP\_R\_ACC}$	Rising, IBUS_UCP_R = 300mA, set by Register 0x0007[6] = 0	160	300	420	mA
		Rising, IBUS_UCP_R = 500mA, set by Register 0x0007[6] = 1	400	500	600	
IBUS UCP Rising Deglitch Time	$t_{DEGLITCH\_IBUS\_UCP\_R}$		--	22	--	µs
IBUS UCP Falling Accuracy	$I_{BUS\_UCP\_F\_ACC}$	Falling, $I_{BUS\_UCP\_F}$ = 150mA, set by Register 0x0007[6] = 0	40	150	320	mA
		Falling, $I_{BUS\_UCP\_F}$ = 250mA, set by Register 0x0007[6] = 1	140	250	420	
IBUS UCP Falling Deglitch Time	$t_{DEGLITCH\_IBUS\_UCP\_F}$	$t_{DEGLITCH\_IBUS\_UCP\_F}$ = 22µs, set by Register 0x005D[3] = 0	--	22	--	µs
		$t_{DEGLITCH\_IBUS\_UCP\_F}$ = 5ms, set by Register 0x005D[3] = 1	--	5	--	ms
IBUS UCP Time Out	$t_{IBUS\_UCP\_TIMEOUT}$	$t_{BUS\_UCP\_TIMEOUT}$ = 12.5ms, set by Register 0x005D[7:5] = 001	11.25	12.5	13.75	ms
		$t_{BUS\_UCP\_TIMEOUT}$ = 25ms, set by Register 0x005D [7:5] = 010	22.5	25	27.5	
		$t_{BUS\_UCP\_TIMEOUT}$ = 50ms, set by Register 0x005D [7:5] = 011	45	50	55	
		$t_{BUS\_UCP\_TIMEOUT}$ = 100ms, set by Register 0x005D [7:5] = 100	90	100	110	
		$t_{BUS\_UCP\_TIMEOUT}$ = 400ms, set by Register 0x005D [7:5] = 101	360	400	440	
		$t_{BUS\_UCP\_TIMEOUT}$ = 1.5s, set by Register 0x005D [7:5] = 110	1.35	1.5	1.65	sec
		$t_{BUS\_UCP\_TIMEOUT}$ = 100s, set by Register 0x005D [7:5] = 111	90	100	110	
VDR OVP Accuracy	$V_{DR\_OVP\_ACC}$	Rising, VDR_OVP = 300mV	200	300	400	mV
VDR OVP Deglitch Time	$t_{DEGLITCH\_VDR\_OVP}$	$t_{DEGLITCH\_VDR\_OVP}$ = 8µs, set by Register 0x0005[4] = 0	--	8	--	µs
		$t_{DEGLITCH\_VDR\_OVP}$ = 5ms, set by Register 0x0005[4] = 1	--	5	--	ms
VOUT OVP Accuracy	$V_{OUT\_OVP\_ACC}$	Rising, V_{OUT_OVP} = 4.9V	4.8	4.9	5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT OVP Deglitch Time	$t_{DEGLITCH\_VOUT\_OVP}$		--	3	--	μs
Over-Temperature Protection Threshold	T_{OTP}	Rising	130	140	150	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Falling	--	20	--	°C
Over-Temperature Protection Deglitch Time	$t_{DEGLITCH\_OTP}$		--	3	--	μs
VBUS Voltage Too High Error Protection Accuracy	$V_{BUS\_HIGH\_ERR\_ACC}$	DIV2 mode. V_{BUS} rising. $V_{BUS\_HIGH\_ERR}$ = V_{BUS}/V_{OUT}	2.328	2.4	2.472	V/V
		Bypass mode. V_{BUS} rising. $V_{BUS\_HIGH\_ERR}$ = V_{BUS}/V_{OUT}	1.14	1.2	1.26	
VBUS Voltage Too Low Error Protection Accuracy	$V_{BUS\_LOW\_ERR\_ACC}$	DIV2 mode. V_{BUS} falling. $V_{BUS\_LOW\_ERR}$ = V_{BUS}/V_{OUT}	2	2.04	2.08	V/V
		Bypass mode. V_{BUS} falling. $V_{BUS\_LOW\_ERR}$ = V_{BUS}/V_{OUT}	0.905	0.952	1	
CFLY Short Detect Level	R_{CFLY_DIAG}	In V_{BAT} = 4V, if the device detects that the short resistance of the flying capacitor is smaller than a specified level during the soft-start duration, the device will stop charging.	--	--	16	Ω
Alarm						
VBAT_OVP_ALM Range	$V_{BAT\_OVP\_ALM\_RAN}$	Rising	4.2	--	4.975	V
VBAT_OVP_ALM Step Size	$V_{BAT\_OVP\_ALM\_SIZE}$		--	25	--	mV
VBAT_OVP_ALM Hysteresis	$V_{BAT\_OVP\_ALM\_HYS}$	Falling	--	50	--	mV
VBAT_OVP_ALM Accuracy	$V_{BAT\_OVP\_ALM\_ACC}$	$V_{BAT\_OVP\_ALM}$ = 4.2V to 4.5V	–0.5	--	0.5	%
IBAT_OCP_ALM Range	$I_{BAT\_OCP\_ALM\_RAN}$	Rising	2	--	8.3	A
IBAT_OCP_ALM Step Size	$I_{BAT\_OCP\_ALM\_SIZE}$		--	100	--	mA
IBAT_OCP_ALM Hysteresis	$I_{BAT\_OCP\_ALM\_HYS}$	Falling	--	100	--	mA
IBAT_OCP_ALM Accuracy	$I_{BAT\_OCP\_ALM\_ACC}$	$I_{BAT\_OCP\_ALM}$ = 3A to 6A, R_{SEN} = 0.002Ω	–200	--	200	mA
IBAT_UCP_ALM Range	$I_{BAT\_UCP\_ALM\_RAN}$	Falling	0	--	3.15	A
IBAT_UCP_ALM Step Size	$I_{BAT\_UCP\_ALM\_SIZE}$		--	50	--	mA
IBAT_UCP_ALM Hysteresis	$I_{BAT\_UCP\_ALM\_HYS}$	Rising	--	50	--	mA
IBAT_UCP_ALM Accuracy	$I_{BAT\_UCP\_ALM\_ACC}$	$I_{BAT\_UCP\_ALM}$ = 3A, R_{SEN} = 0.002Ω	–200	--	200	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS_OVP_ALM Range	$V_{BUS\_OVP\_ALM\_RAN}$	DIV2 mode. V_{BUS} rising.	6	--	12.3	V
		Bypass mode. V_{BUS} rising.	3	--	6.15	
VBUS_OVP_ALM Step Size	$V_{BUS\_OVP\_ALM\_SIZE}$	DIV2 mode	--	100	--	mV
		Bypass mode	--	50	--	
VBUS_OVP_ALM Hysteresis	$V_{BUS\_OVP\_ALM\_HYS}$	DIV2 mode. V_{BUS} falling.	--	100	--	mV
		Bypass mode. V_{BUS} falling.	--	50	--	
VBUS_OVP_ALM Accuracy	$V_{BUS\_OVP\_ALM\_ACC}$	Falling, $V_{BUS\_OVP\_ALM}$ = 6V to 9V.	–35	--	35	mV
IBUS_OCP_ALM Range	$I_{BUS\_OCP\_ALM\_RAN}$	Rising	0	--	6	A
IBUS_OCP_ALM Step Size	$I_{BUS\_OCP\_ALM\_SIZE}$		--	100	--	mA
IBUS_OCP_ALM Hysteresis	$I_{BUS\_OCP\_ALM\_HYS}$	Falling	--	100	--	mA
IBUS_OCP_ALM Accuracy	$I_{BUS\_OCP\_ALM\_ACC}$	$I_{BUS\_OCP\_ALM}$ = 1A to 4A	–150	--	150	mA
IBUS_UCP_ALM Range	$I_{BUS\_UCP\_ALM\_RAN}$	Rising	0	--	3.175	A
IBUS_UCP_ALM Step Size	$I_{BUS\_UCP\_ALM\_SIZE}$		--	25	--	mA
IBUS_UCP_ALM Hysteresis	$I_{BUS\_UCP\_ALM\_HYS}$	Falling	--	50	--	mA
IBUS_UCP_ALM Accuracy	$I_{BUS\_UCP\_ALM\_ACC}$	$I_{BUS\_UCP\_ALM}$ = 0.3A to 0.5A	–150	--	150	mA
TDIE_OTP_ALM Range	$T_{DIE\_OTP\_ALM\_RAN}$	Rising	25	--	152.5	°C
TDIE_OTP_ALM Step Size	$T_{DIE\_OTP\_ALM\_SIZE}$		--	1	--	°C
TDIE_OTP_ALM Hysteresis	$T_{DIE\_OTP\_ALM\_HYS}$	Falling	--	10	--	°C
TDIE_OTP_ALM Accuracy	$T_{DIE\_OTP\_ALM\_ACC}$		–4	--	4	°C
DP_OV_ALM Rising Threshold	$V_{DP\_OV\_ALM}$	Rising	--	4.5	--	V
DP_OV_ALM Hysteresis	$V_{DP\_OV\_ALM\_HYS}$	Falling	--	100	--	mV
DP_OV_ALM Accuracy	$V_{DP\_OV\_ALM\_ACC}$		–50	--	50	mV
DM_OV_ALM Rising Threshold	$V_{DM\_OV\_ALM}$	Rising	--	4.5	--	V
DM_OV_ALM Hysteresis	$V_{DM\_OV\_ALM\_HYS}$	Falling	--	100	--	mV
DM_OV_ALM Accuracy	$V_{DM\_OV\_ALM\_ACC}$		–50	--	50	mV
ADC Specification						
ADC Sample Rate	f_{SAMPLE_RATE}		1800	2000	2200	kHz
ADC Data Rate	t_{DATA_ADC}	12bit, 128 averages Report data for each channel	--	1.2	--	ms
VBUS ADC Range	$V_{BUS\_ADC\_RAN}$		0	--	14	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$	V_{BUS} = 6V to 9V	–35	--	35	mV
		V_{BUS} = 3.3V to 11.5V	–2	--	2	%
IBUS ADC Range	$I_{BUS\_ADC\_RAN}$		0	--	6	A
IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$	I_{BUS} = 2A	–5	--	5	%
		I_{BUS} = 0A to 4A	–150	--	150	mA
VOUT ADC Range	$V_{OUT\_ADC\_RAN}$		0	--	5	V
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$	V_{OUT} = 3V to 4.5V	–20	--	20	mV
VBAT ADC Range	$V_{BAT\_ADC\_RAN}$		0	--	5	V
VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$	V_{BAT} = 3V to 4.5V	–0.5	--	0.5	%
		V_{BAT} = 4.45V	–10	--	10	mV
IBAT ADC Range	$I_{BAT\_ADC\_RAN}$		0	--	10	A
IBAT ADC Accuracy	$I_{BAT\_ADC\_ACC}$	I_{BAT} = 3A to 8A, R_{SEN} = 0.002Ω	–200	--	200	mA
		I_{BAT} = 2A, R_{SEN} = 0.002Ω	–5	--	5	%
		I_{BAT} = 7A, R_{SEN} = 0.002Ω	–2	--	2	
TDIE ADC Range	$T_{DIE\_ADC\_RAN}$		–40	--	152.5	°C
TDIE ADC Accuracy	$T_{DIE\_ADC\_ACC}$	T_J = 25°C	–4	--	4	°C
DP_ADC Range	$D_{P\_ADC\_RAN}$		0	--	5	V
DP_ADC Accuracy	$D_{P\_ADC\_ACC}$		–50	--	50	mV
DM_ADC Range	$D_{M\_ADC\_RAN}$		0	--	5	V
DM_ADC Accuracy	$D_{M\_ADC\_ACC}$		–50	--	50	mV
REGN						
REGN LDO Output Voltage	V_{REGN}	ADC enabled, $V_{BUS} \geq$ 5.5V	4.9	5	5.1	V
		ADC enabled, V_{BUS} < 5.5V, Without VAC and VOUT, V_{BUS} > V_{DDA_UVLO} threshold	V_{BUS} – 0.7	V_{BUS}	V_{BUS} + 0.1	
		Without VAC and VOUT, V_{OUT} > V_{DDA_UVLO} threshold	V_{OUT} – 0.1	V_{OUT}	V_{OUT} + 0.1	
Pull-Down						
VAC Pull-Down Resistance	R_{VAC_PD}	V_{AC} < 5V	--	270	--	Ω
		V_{AC} > 5V	--	22	--	mA
VAC Pull-Down Time Out	t_{VAC_PD}		360	400	440	ms
VBUS Pull-Down Resistance	R_{VBUS_PD}	V_{BUS} = 3V to 14V	0.6	1	1.4	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Watchdog Time Out						
Watchdog Time Out	WDT	No I²C communication for 0.5s, set by Register 0x0000[2:0] = 000 (Note 7)	0.45	0.5	0.55	sec
		No I²C communication for 1s, set by Register 0x0000[2:0] = 001 (Note 7)	0.9	1	1.1	
		No I²C communication for 5s, set by Register 0x0000[2:0] = 010 (Note 7)	4.5	5	5.5	
		No I²C communication for 30s, set by Register 0x0000[2:0] = 011 (Note 7)	27	30	33	
		No I²C communication for 40s, set by Register 0x0000[2:0] = 100 (Note 7)	36	40	44	
		No I²C communication for 80s, set by Register 0x0000[2:0] = 101 (Note 7)	72	80	88	
		No I²C communication for 128s, set by Register 0x0000[2:0] = 110 (Note 7)	115.2	128	140.8	
		No I²C communication for 255s, set by Register 0x0000[2:0] = 111 (Note 7)	229.5	255	280.5	
Logic Output Pin ($\overline{INT}$)						
$\overline{INT}$ Output Low Threshold	V_{OL_INT}	Sink current = 100μA	--	--	0.1	V
		Sink current = 2mA	--	--	0.3	
$\overline{INT}$ High Level Leakage Current	I_{INT_LK}	Pull-up rail 1.8V	--	--	1	μA
$\overline{INT}$ Pin Pull-Low Time	$t_{INT\_PULL\_LOW}$		--	256	--	μs
Synchronization Function						
DP_SYNCOUT Output High Threshold	$V_{OH\_DP\_SYNCOUT}$	Register 0x005F[7] = 1	V_{REGN} - 0.4	--	--	V
DP_SYNCOUT Output Low Threshold	$V_{OL\_DP\_SYNCOUT}$	Register 0x005F[7] = 1	--	--	0.2	V
BATN/SRP_SYNCIN Input High Threshold	V_{IH_BATN/SRP_SYNCIN}	Register 0x005F[5] = 1	V_{REGN} x 0.75	--	--	V
BATN/SRP_SYNCIN Input Low Threshold	V_{IL_BATN/SRP_SYNCIN}	Register 0x005F[5] = 1	--	--	V_{REGN} x 0.25	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD of I²C Detection						
VDD Level of I²C Detection Threshold	$V_{TH\_I2C\_level}$	VDD level of I²C = 1.2V when SDA voltage < $V_{TH\_I2C\_level}$. VDD level of I²C = 1.8V when SDA voltage > $V_{TH\_I2C\_level}$. (VDD level of I²C can only change to 1.8V from 1.2V. It cannot change to 1.2V from 1.8V.)	1.3	1.5	1.65	V
V_{SDA} Rising Deglitch Time	t_{I2C_level}		--	17.5	--	μs
DP/DM Detection						
DP Source Voltage	V_{DP_SRC}		0.5	0.6	0.7	V
DM Source Voltage	V_{DM_SRC}		0.5	0.6	0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
Logic Threshold Voltage	V_{LGC_CHG}		0.8	--	2	V
DP Sink Current	I_{DP_SINK}		25	45	65	μA
DM Sink Current	I_{DM_SINK}		25	45	65	μA
Data Contact Detect Current Source	I_{DP_SRC}		7	10	13	μA
DP Pull-Down Resistance	R_{DP_PD}		14.25	20	24.8	kΩ
DM Pull-Down Resistance	R_{DM_PD}		14.25	20	24.8	kΩ
DP Source On-Time	$t_{DP\_SRC\_ON}$		40	64	80	ms
DM Source On-Time	$t_{DM\_SRC\_ON}$		40	64	80	ms
DCD Timeout	$t_{DCD\_TIMEOUT}$	Register 0x0044[6:5] = 01	300	--	900	ms

12.1 I²C Characteristics

(Note 7)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}	I2C_level = 1.8V	1.17	--	--	V
		I2C_level = 1.2V	0.78	--	--	
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}	I2C_level = 1.8V	--	--	0.63	V
		I2C_level = 1.2V			0.42	
SDA Low-Level Output Threshold Voltage	V_{OL_I2C}	Sink current = 3mA, pull-up rail 1.8V	--	--	0.36	V
		Sink current = 3mA, pull-up rail 1.2V	--	--	0.24	

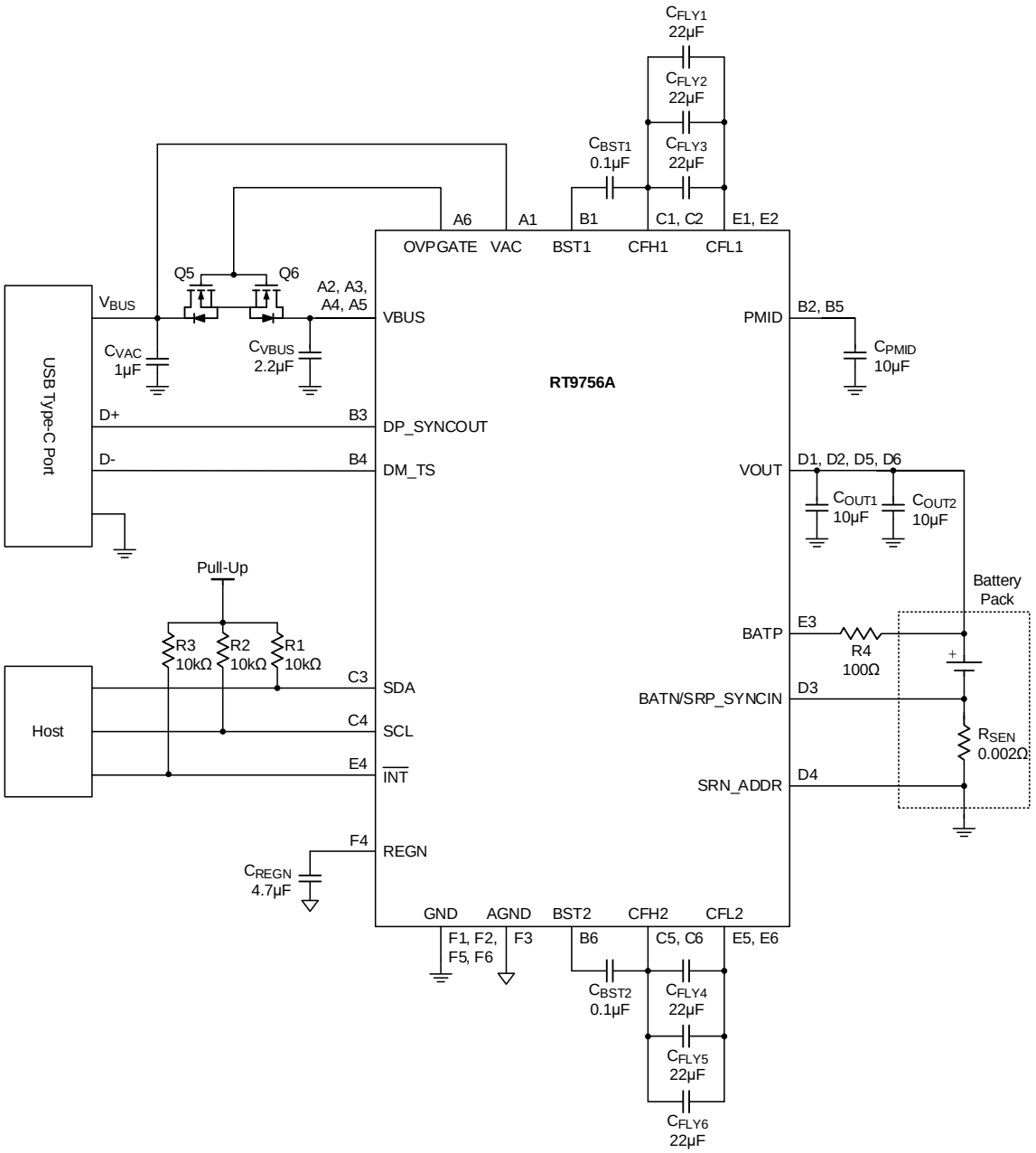
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Clock Frequency	f_{CLK}	Standard-mode	--	--	100	kHz
		Fast-mode	--	--	400	
		Fast-mode plus	--	--	1000	
		High-speed mode Cb = 400pF	--	--	1.7	MHz
		High-speed mode Cb = 100pF	--	--	3.4	
Bus Free Time between Stop and Start Condition	t_{BUF}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode plus	0.5	--	--	
(Repeated) Start Hold Time	$t_{HD;STA}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
(Repeated) Start Setup Time	$t_{SU;STA}$	Standard-mode	4.7	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode plus	0.26	--	--	
		High-speed mode Cb = 400 pF	160	--	--	ns
		High-speed mode Cb = 100 pF	160	--	--	
STOP Condition Setup Time	$t_{SU;STO}$	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode plus	0.26	--	--	
		High-speed mode Cb = 400pF	160	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SDA Data Hold Time	$t_{HD;DAT}$	Standard-mode	0.1	--	--	ns
		Fast-mode	0.1	--	--	
		Fast-mode plus	0.1	--	--	
		High-speed mode Cb = 400pF	0.1	--	150	
		High-speed mode Cb = 100pF	0.1	--	70	
SDA Valid Acknowledge Time	$t_{VD;ACK}$	Standard-mode	--	--	3.45	µs
		Fast-mode	--	--	0.9	
		Fast-mode plus	--	--	0.45	
SDA Setup Time	$t_{SU;DAT}$	Standard-mode	250	--	--	ns
		Fast-mode	100	--	--	
		Fast-mode plus	50	--	--	
		High-speed mode Cb = 400pF	10	--	--	
		High-speed mode Cb = 100pF	10	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCL Clock Low Time	t_{LOW}	Standard-mode	4.7	--	--	µs
		Fast-mode	1.3	--	--	
		Fast-mode plus	0.5	--	--	
		High-speed mode Cb = 400pF	320	--	--	ns
		High-speed mode Cb = 100pF	160	--	--	
SCL Clock High Time	t_{HIGH}	Standard-mode	4	--	--	µs
		Fast-mode	0.6	--	--	
		Fast-mode Pplus	0.26	--	--	
		High-speed mode Cb = 400pF	120	--	--	ns
		High-speed mode Cb = 100pF	60	--	--	

Note 7. The specification is guaranteed by design and/or correlation with statistical process control.

Note 8. When Bypass mode is set, VAC OVP must be 6.5V to handle surge conditions.

13 Typical Application Circuit



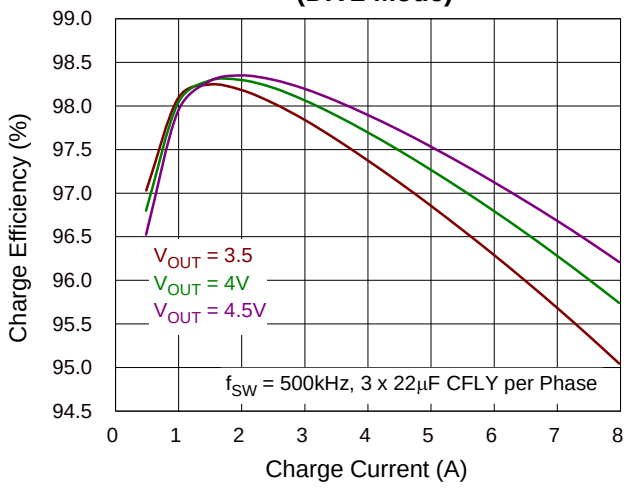
13.1 Recommended Components Information

Table 1. BOM List

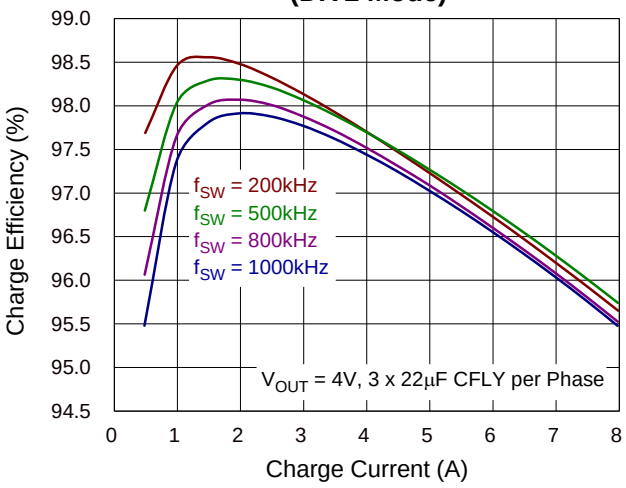
Name	Part Number	Description	Package	Manufacturer
C_{VAC}	GRM155R61H105KE05	CAP, CERM, 1μF, 50V, ±10%, X5R	0402	MuRata
C_{VBUS}	GRM155R61E225KE11	CAP, CERM, 2.2μF, 25V, ±10%, X5R	0402	MuRata
Q5, Q6	PSMN2R4-30MLD	N-Channel 30V, 2.4mΩ logic level MOSFET in LFPAK33, using NextPowerS3 Technology	LFPAK33	Nexperia
C_{FLY1}, C_{FLY2}, C_{FLY3}, C_{FLY4}, C_{FLY5}, C_{FLY6}	GRM187R61A226ME15	CAP, CERM, 22μF, 10V, ±20%, X5R	0603	MuRata
C_{OUT1}, C_{OUT2}	GRM185R60J106ME15	CAP, CERM, 10μF, 6.3V, ±20%, X5R	0603	MuRata
C_{PMID}	GRM188R61E106MA73	CAP, CERM, 10μF, 25V, ±20%, X5R	0603	MuRata
C_{BST1}, C_{BST2}	GRM033R61C104KE14	CAP, CERM, 0.1μF, 16V, ±10%, X5R	0201	MuRata
C_{REGN}	GRM155R61A475MEAAD	CAP, CERM, 4.7μF, 10V, ±20%, X5R	0402	MuRata
R1, R2, R3	WR04X1002FTL	RES, 10k, 1%, 0.0625W	0402	Walsin
R4	CR0402F100RQ10Z	RES, 100Ω, 1%, 0.063W	0402	EVER OHMS
R_{SEN}	CSNL1206FT2L00	RES, 0.002, 1%, 1W	1206	Stackpole Electronics Inc

14 Typical Operating Characteristics

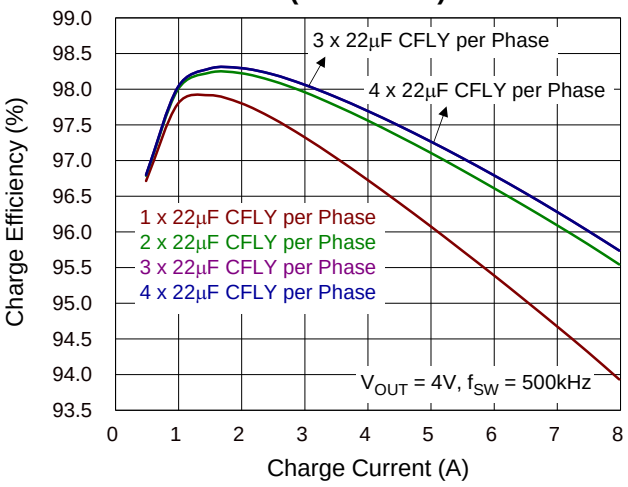
Charge Efficiency vs. Charge Current (DIV2 Mode)



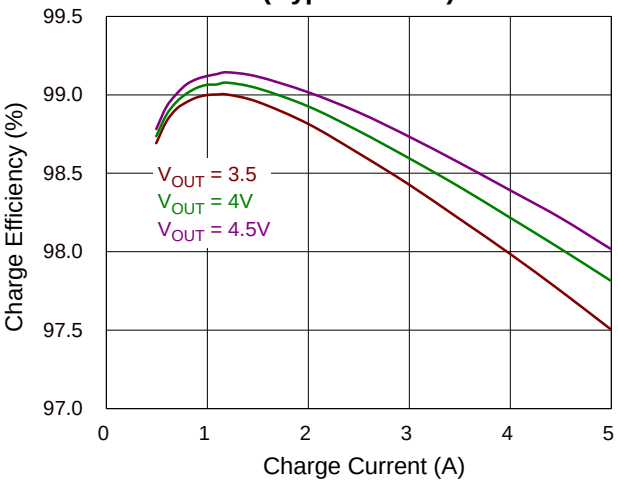
Charge Efficiency vs. Charge Current (DIV2 Mode)



Charge Efficiency vs. Charge Current (DIV2 Mode)



Charge Efficiency vs. Charge Current (Bypass Mode)



15 Application Information

(Note 9)

15.1 Operation Principle

The cap divider topology relies on a smart wall adapter to control the input voltage and current for charging. Based on this topology, four MOSFETs (Q1 to Q4) are used to alternately charge and discharge the flying capacitor (CFLY). The simplified circuit of the capacitor divider is shown in Figure 1(A).

Period 1: When Q1 and Q3 are turned on and Q2 and Q4 are turned off, CFLY and the battery (BAT) are in series with VBUS. The BUS current is supplied directly to COUT and BAT. During this period, the voltage of CFLY can be expressed as equation 1:

$V_{CFLY} = V_{BUS} - V_{BAT}$ ---- (1)

Period 2: When Q1 and Q3 are turned off and Q2 and Q4 are turned on, CFLY and BAT are in parallel. The current of BAT is supplied only by CFLY. During this period, the voltage of CFLY can be expressed as equation 2:

$V_{CFLY} = V_{BAT}$ ---- (2)

If equation 2 is substituted into equation 1, equation 1 can be expressed as equation 3:

$V_{BAT} = V_{BUS} / 2$ ---- (3)

If the power dissipation of the topology is ignored, the output power can be expressed as equation 4:

$V_{BAT} \times I_{BAT} = V_{BUS} \times I_{BUS}$ --- (4)

If equation 3 is substituted into equation 4, I_{BAT} can be expressed as equation 5:

$I_{BAT} = 2 \times I_{BUS}$ --- (5)

According to the equations above, the battery voltage is half of the input voltage and the current flowing into the battery is twice the input current in the cap divider topology. For efficiency and output ripple improvement in applications, the dual-phase cap divider topology with a 180-degree phase shift between phases is built into the RT9756A.

The RT9756A also has a Bypass mode for direct charging. To use Bypass mode, set OPERATION_MODE (0x0000[5]) = 0 before starting charging. In Bypass mode, Q1, Q2 and Q4 turn on continuously as shown in Figure 1(B).

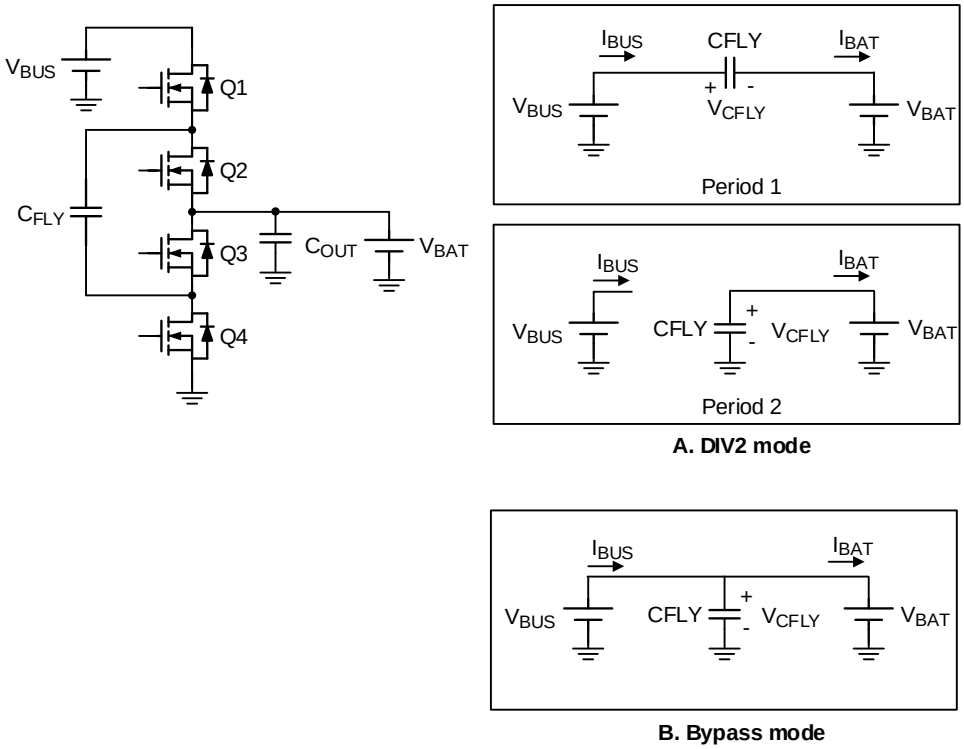


Figure 1. Simplified Circuit of Cap Divider

15.2 Charge System Introduction

The RT9756A is a smart cap divider charger used in slave charger applications. The RT9756A generates high output current using the cap divider topology. Before enabling the RT9756A, the host sets up all protection and alarm functions and disables the main charger in the power solution. The host must monitor the alarms set up in the RT9756A during the high current charging period and communicate with the smart wall adapter to control the charging current flow into the battery.

Figure 2 is the simplified charge system block. In this charge system, the RT9756A is used to detect USB BC1.2 of the adapter, and the PD controller is used to communicate with adapter via the PD protocol. Once the smart wall adapter is detected, the AP will control the switching charger and smart cap divider charger to achieve a high current charging period. These devices can communicate with each other through the I^2C serial interface.

The charge profile of a high-capacity battery using a switching charger and a cap divider charger is shown in Figure 3. To achieve the charge profile, the switching charger is required to dominate the pre-charge, fast charge (when battery voltage is lower than the system startup voltage), constant voltage, and termination periods, respectively. The cap divider charger is used to achieve the fast charge period. To shorten the constant voltage period, the cap divider charger is controlled to reduce the charge current by ramp steps when the battery voltage triggers the VBAT_OVP_ALM.

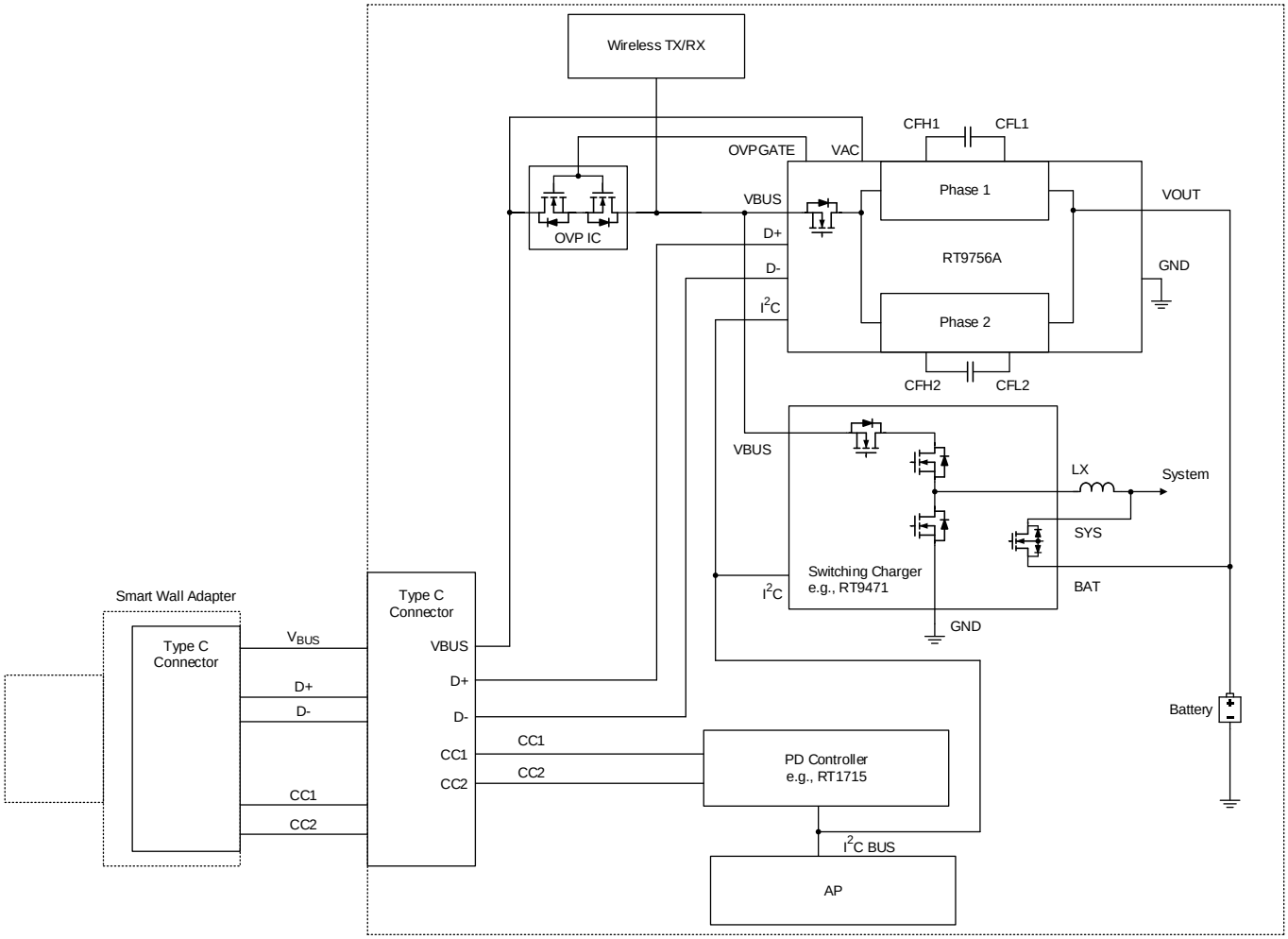


Figure 2. Simplified Charge System

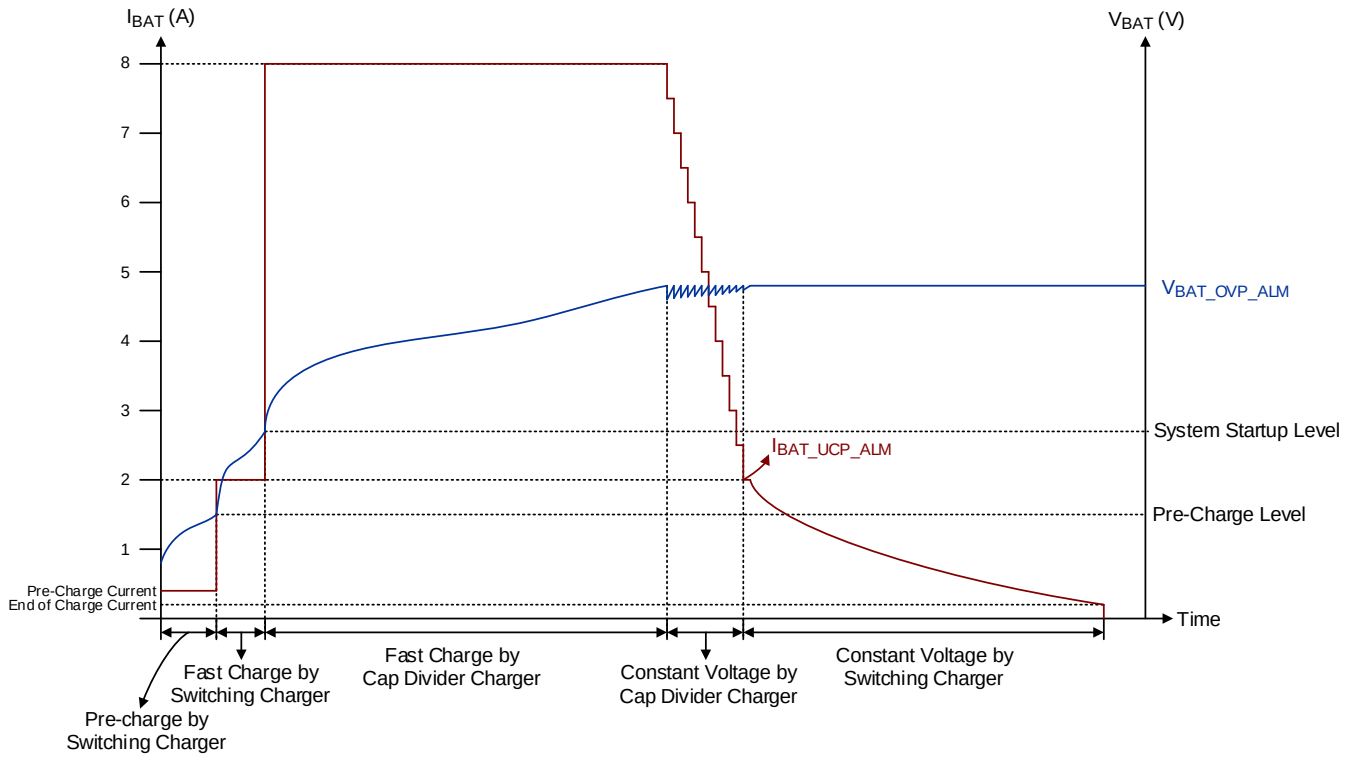


Figure 3. Charge Profile using Switching Charger and Cap Divider Charger

While the RT9756A is charging, the host needs to communicate with the smart wall adapter to control the charging current provided by the RT9756A. The communication flow between the smart wall adapter and charge system is shown in Figure 4. To prevent abnormal events during charging, the RT9756A is equipped with many adjustable protection and alarm functions. All alarms and protections are activated under specific operating conditions, as shown in Table 2 and Table 4, respectively.

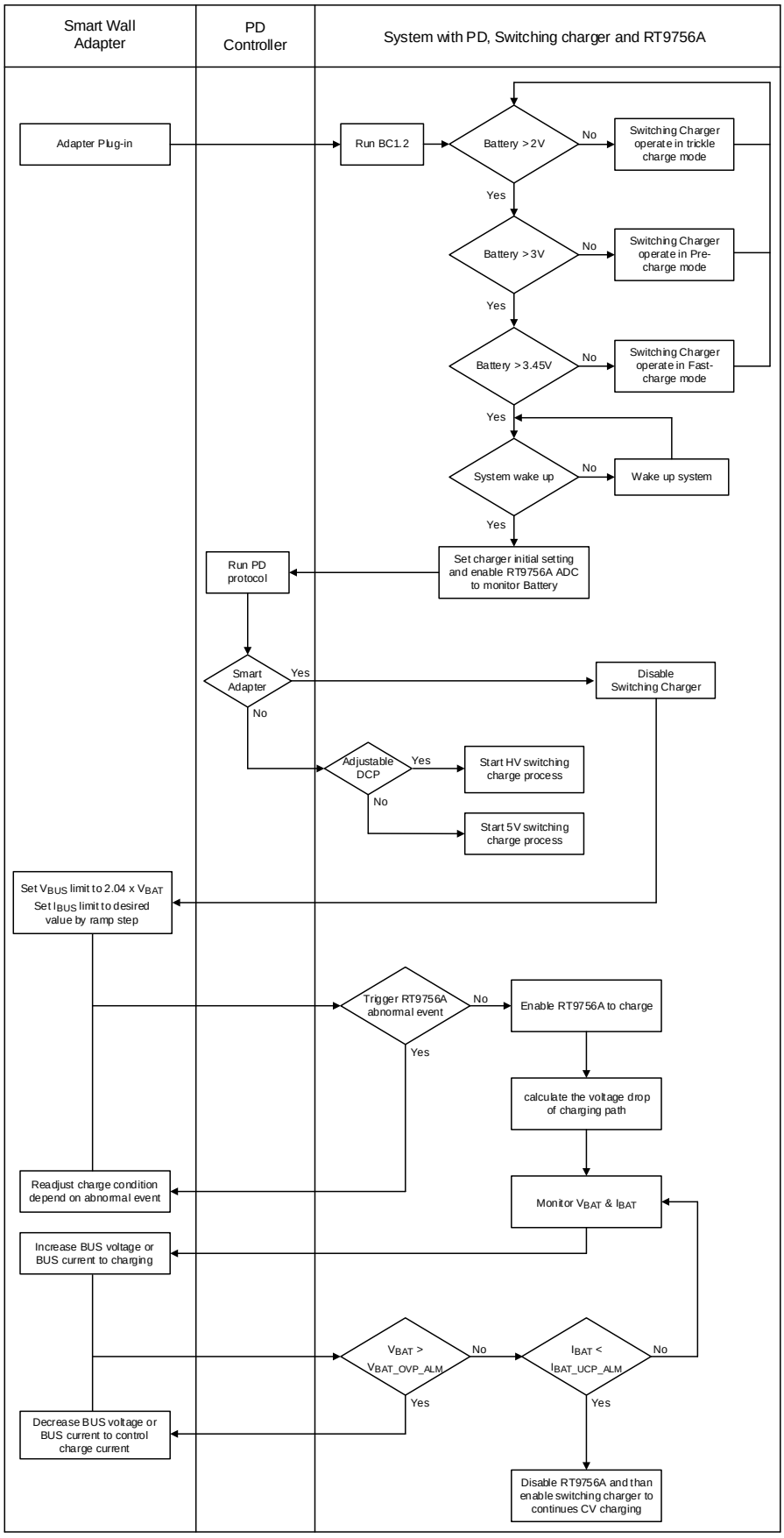


Figure 4. System Control Flow Chart

15.3 Device Power-Up

The device is powered by VDDA, and the VDDA voltage can be measured through the REGN pin. When the V_{DDA} voltage is higher than the V_{DDA_UVLO} threshold, the device will start working. The VDDA voltage can be powered by VAC, VBUS, or VOUT, whichever has the higher voltage level.

Once the RT9756A is powered, the device will activate the address detection mechanism to assign its slave address. The slave address is determined by the state of the SRN_ADDR pin after power-on. Depending on whether the SRN_ADDR pin is shorted to ground or floating, the slave address will be 0x6F or 0x6E , respectively. After address detection is finished, the host can communicate with the RT9756A via I^2C serial interface. Furthermore, the reaction time from $V_{DDA} > V_{DDA\_UVLO}$ to I^2C release (t_{VDDA_START}) is around 400μs.

The RT9756A includes a watchdog timer that is enabled by default. If the device is not read or written to before the watchdog timer times out, the ADC_EN and CHG_EN will be set to their default values. The register table shows which registers are reset by the watchdog. Moreover, the watchdog timeout flag and the $\overline{INT}$ pulse will be triggered to inform the host.

If the V_{OUT} is not higher than the V_{OUT_INSERT} rising threshold, charging cannot be enabled. Once V_{OUT} exceeds the V_{OUT_INSERT} rising threshold, the minimum allowable V_{OUT} to enable charging is the V_{OUT_INSERT} falling threshold. Before charging is enabled, the RT9756A can report ADC information while the ADC is enabled. After charging is enabled, the RT9756A reports ADC information regardless of whether the ADC is enabled or not.

To reduce quiescent current, most of the sensing circuits inside the RT9756A will be turned off after address detection is finished and ADC_EN and CHG_EN are disabled for 500ms. In other words, some protection and insert functions are still activated before the device's sensing circuit are disabled. Figure 5 shows the device power-on flow with the protection and insert function activation list in each state. The VAC_OVP, VBAT_OVP, VOUT_OVP, VBUS_OVP, TDIE_OTP, TS_OTP, VBUS_HIGH_ERR, VBUS_ LOW_ERR, VOUT_INSERT, VBUS_INSERT, and VAC_INSERT functions are still active before sensing circuits are turned off. When the device disables sensing circuits, all protections and INSERT functions are disabled except VAC_INSERT, VAC_OVP, and VBUS_OVP.

15.4 8-Channel Analog to Digital Converter

The RT9756A integrates an 8-channel ADC conversion for users to monitor the input and output status of the device. The ADC function is allowed to operate if $V_{DDA} > V_{DDA\_UVLO}$ threshold. Once V_{DDA} exceeds the V_{DDA_UVLO} rising threshold, the RT9756A will reset ADC_EN to disable if $V_{DDA} < V_{DDA\_UVLO}$ threshold. The ADC function can operate in continuous mode or 1-shot mode. Users can enable the ADC function and select the conversion mode via I^2C serial interface control (0x0011). In continuous mode, the ADC function will convert all ADC channels and report ADC data to related registers continuously. In 1-shot mode, the ADC function will reset the ADC_EN bit to 0 after converting each ADC channel. Each ADC channel can be enabled or disabled. The device uses ADC conversion data to detect all alarm functions, TS_OTP, VBUS_LOW_ERR and VBUS_HIGH_ERR. Due to this feature, the ADC function will be forced to convert each ADC channel in continuous mode and ADC cannot be controlled via the register after charging. Figure 6 shows the ADC function operation flow chart; users can follow the flow chart to control the ADC function. While reading the data of registers, the high byte has to be read first, followed by the low byte. Moreover, the high byte and low byte have to be read using the I^2C multi-byte reading method in one transmission, which is terminated with one STOP condition.

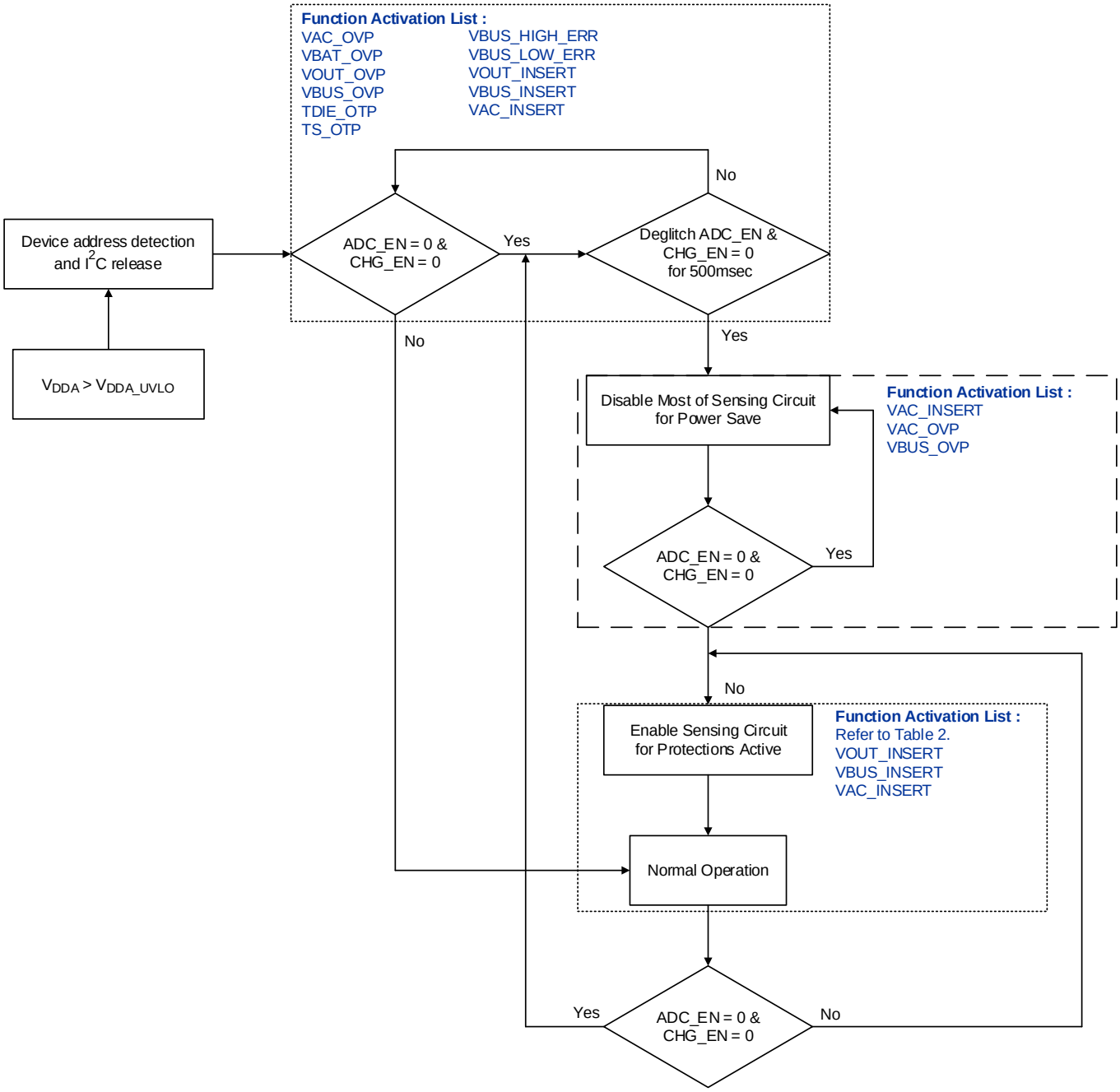


Figure 5. Device Power-On Flow with Protections and Insert Function Activation List

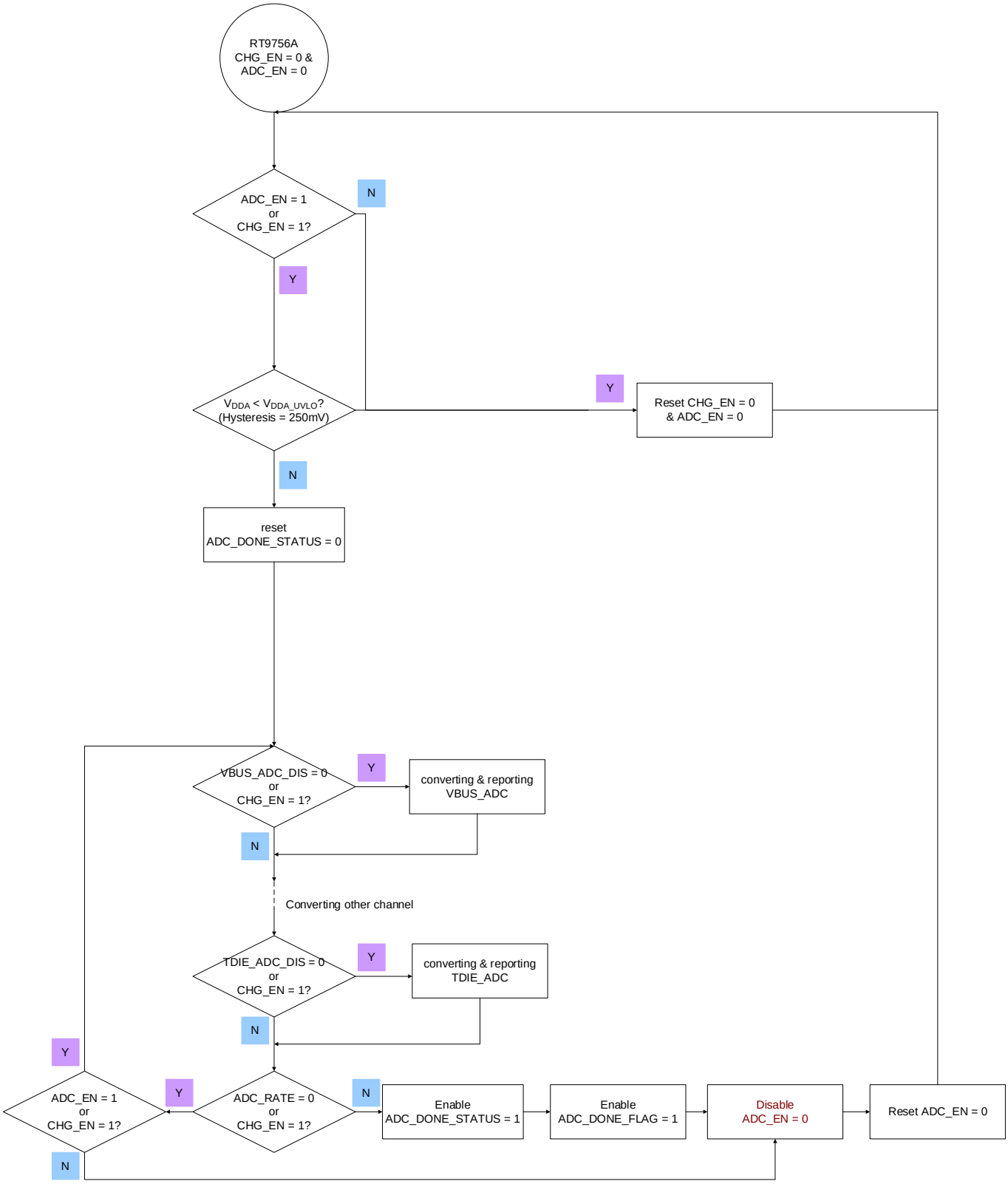


Figure 6. ADC Function Operation Flow Chart

15.5 Protection Feature

The RT9756A integrates 14 protection features to safeguard device charging under unexpected conditions. All protection activations are based on CHG_EN and ADC_EN bits, except for VAC_OVP and VBUS_OVP. Users need to set the CHG_EN or ADC_EN bit to 1 to enable the related protection. Each protection function can be disabled by its respective enable bit. Table 2 shows the enable conditions and protection methods for each protection feature.

Table 2. Protection Trigger Condition and Behavior

Protection Function	Enable Condition	Threshold Refer to Electrical Characteristics	Deglitch Time	Protection Method	Reset Method
VAC_OVP	V_{AC} > V_{AC_INSERT} & OVPMOS_DIS = 0	V_{AC} ≥ 12V (Programmable)	NA	Turn off OVPGATE and Reset CHG_EN = 0	V_{AC} is lower than hysteresis 500mV
VBUS_OVP	V_{DDA} > V_{DDA_UVLO}	V_{BUS} ≥ 8.9V in DIV2 mode V_{BUS} ≥ 4.5V in DIV2 mode (Programmable)	NA	Reset CHG_EN = 0	V_{BUS} < OVP level
VBAT_OVP	CHG_EN = 1 or ADC_EN = 1	V_{BAT} ≥ 4.35V (Programmable)	3μs	Reset CHG_EN = 0	V_{BAT} < OVP level
VOUT_OVP	CHG_EN = 1 or ADC_EN =1	V_{OUT} ≥ 4.9V	3μs	Reset CHG_EN = 0	V_{OUT} < OVP level
IBUS_OCP	CHG_EN = 1	I_{BUS} ≥ 3A (Programmable)	50μs	Reset CHG_EN = 0	NA
IBUS_OCP_H	CHG_EN = 1	I_{BUS} ≥ 6.8A	NA	Reset CHG_EN = 0	NA
IBUS_UCP	CHG_EN = 1	I_{BUS} ≤ 150mA (Programmable)	22μs (Programmable)	Reset CHG_EN = 0	NA
IBAT_OCP	CHG_EN = 1	I_{BAT} ≥ 7.2A (Programmable)	50μs	Reset CHG_EN = 0	NA
TDIE_OTP	CHG_EN = 1 or ADC_EN = 1	T_{DIE} ≥ 150°C	3μs	Reset CHG_EN = 0	T_{DIE} < OTP level
VDR_OVP	CHG_EN = 1	(V_{AC} – V_{BUS}) ≥ 300mV	8μs (Programmable)	Reset CHG_EN = 0	NA
CFLY_DIAG	CHG_EN = 1	R_{CFLY} ≤ 16Ω	NA	Reset CHG_EN = 0	NA
TS_OTP	(CHG_EN = 1 or ADC_EN =1) & DM_ADC_DIS = 0 & DM_TS_CFG = 1	TS pin ≤ 0V (Programmable)	NA	Reset CHG_EN = 0	TS pin > TS_OTP level
VBUS_LOW_ERR	CHG_EN = 1 (before switching) or ADC_EN = 1 (VBUS_ADC and VOUT_ADC must be enabled)	V_{BUS} / V_{OUT} ≤ 2.04	NA	Reset CHG_EN = 0	V_{BUS} / V_{OUT} > 2.04

Protection Function	Enable Condition	Threshold Refer to Electrical Characteristics	Deglitch Time	Protection Method	Reset Method
VBUS_HIGH_ERR	CHG_EN = 1 (before switching) or ADC_EN = 1 (VBUS_ADC and VOUT_ADC must be enabled)	V_{BUS} / V_{OUT} ≥ 2.4	NA	Reset CHG_EN = 0	V_{BUS} / V_{OUT} < 2.4

15.5.1 VAC Pin Overvoltage Protection (VAC_OVP)

The RT9756A integrates a VAC_OVP function to monitor the adaptor voltage via the VAC pin and control the external MOSFET via the OVPGATE pin. The VAC_OVP function is powered by the VAC pin and will be enabled if the V_{AC} voltage is higher than V_{AC_INSERT} and OVPMOS_DIS is set to 0. The device will provide a $V_{OVPGATE}$ voltage to turn on the external MOSFET if V_{AC} is higher than V_{AC_INSERT} for a $t_{DEGLITCH\_VAC\_INSERT}$ time. If the V_{AC} voltage is higher than the V_{AC_OVP} threshold, the device will start to turn off the external MOSFET after a $t_{VAC\_OVP\_RE}$ time and will turn off the external MOSFET within $t_{VAC\_OVP\_OFF}$ time. Figure 7 shows the timing of the VAC_OVP function. Users should ensure that the adaptor voltage does not exceed the absolute maximum rating of the VAC pin and the external MOSFET (prevented by external TVS, etc.).

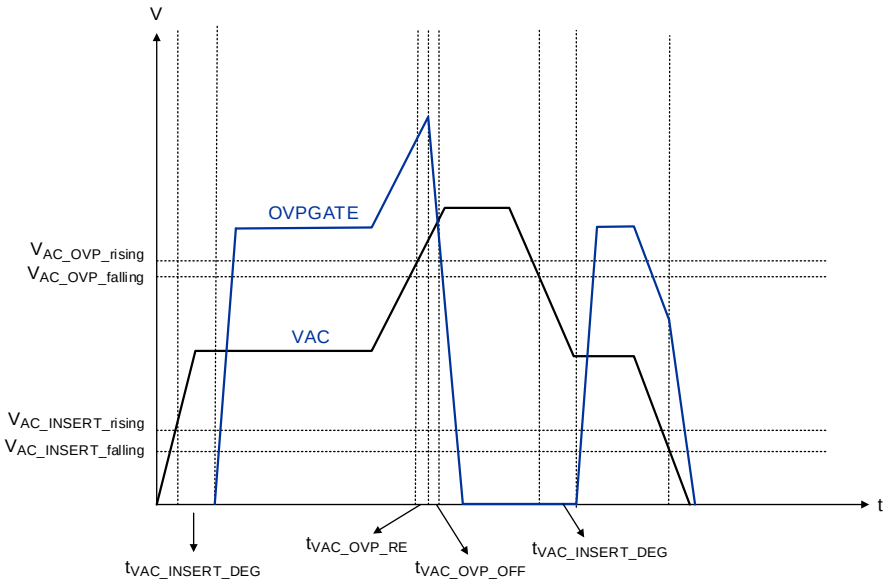


Figure 7. OVPGATE Operation Timing

15.5.2 VBUS Charge Voltage Protection (VBUS_HIGH_ERR and VBUS_LOW_ERR)

The device integrates VBUS_HIGH_ERR and VBUS_LOW_ERR to prevent users from setting an incorrect VBUS for charging. In a no-charge condition, if V_{BUS} is higher than the $V_{BUS\_HIGH\_ERR}$ threshold or lower than the $V_{BUS\_LOW\_ERR}$ threshold, the device will force the CHG_EN bit to disable. Both VBUS_HIGH_ERR and VBUS_LOW_ERR will be disabled after the device successfully starts charging. The device diagnoses VBUS_HIGH_ERR and VBUS_LOW_ERR using VBUS ADC and VOUT ADC values. To use these two functions, enabling VBUS ADC and VOUT ADC conversion is necessary.

15.5.3 Input and Output Overvoltage Protection (VBUS_OVP, VOUT_OVP, VBAT_OVP)

The device has VBUS_OVP, VBAT_OVP, and VOUT_OVP functions to detect input and output charge voltage conditions. If the input and output charge voltage is higher than protection threshold, the device will turn off the charger and reset CHG_EN to disable. The VBUS_OVP function monitors the VBUS voltage via the VBUS pin. The VOUT_OVP function monitors the VOUT voltage via the VOUT pin. In high charging current applications, the system might experience a large voltage drop between the device and the battery pack. For such applications, the device integrates VBAT_OVP to monitor differential voltage between BATP and BATN/SRP_SYNCIN. Users should connect a 100Ω resistor between BATP and the battery pack to achieve remote sensing for the device. Users can adjust the protection levels of VBUS_OVP and VBAT_OVP.

15.5.4 Input and Output Overcurrent Protection (IBUS_OCP, IBUS_OCP_H, IBAT_OCP)

The IBUS_OCP and IBUS_OCP_H functions monitor the input current via Q0. If the CHG_EN bit is enabled, Q0 will turn on and IBUS_OCP will start detecting the input current. If the I_{BUS} exceeds the I_{BUS_OCP} threshold, the device stops charging and resets the CHG_EN bit to disable. If I_{BUS} rises over the $I_{BUS\_OCP\_H}$ level quickly, the device stops charging immediately after the IBUS_OCP_H reaction time and resets the CHG_EN bit to disable. The IBAT_OCP function detects the battery current via the BATN/SRP_SYNCIN and SRN_ADDR pins. Users should connect a 2mΩ resistor in series with the battery pack. The SRN_ADDR and BATN/SRP_SYNCIN should be connected in parallel across the resistor. The internal protector will convert the differential voltage between BATN/SRP_SYNCIN and SRN_ADDR to a current value. The ratio between the differential voltage and current value can be determined by register settings. If the current value exceeds the I_{BAT_OCP} threshold, the device will stop charging and reset CHG_EN to disable. Users can adjust the IBUS_OCP and IBAT_OCP threshold via register settings.

15.5.5 Input Undercurrent Protection (IBUS_UCP)

The device integrates an IBUS_UCP function to prevent reverse current from the battery to VBUS. The IBUS_UCP detects input current via Q0. Figure 8 shows the flow chart of IBUS_UCP, the device enables the IBUS UCP Rising threshold and starts the counting timer after charging begins. Once I_{BUS} exceeds the IBUS UCP Rising threshold, the device will stop the counting timer and enable the IBUS UCP Falling threshold. If the I_{BUS} is smaller than $I_{BUS\_UCP\_R}$ and the timer is already longer than IBUS_ UCP_FALL Falling Deglitch Time ($t_{IBUS\_UCP\_TIMEOUT}$), the device will enable the IBUS UCP Falling threshold. After the device enables the IBUS UCP Falling threshold, if the I_{BUS} is smaller than $I_{BUS\_UCP\_F}$ threshold, the device will stop charging and reset CHG_EN to disable. Figure 9 shows IBUS_UCP behavior in different applications.

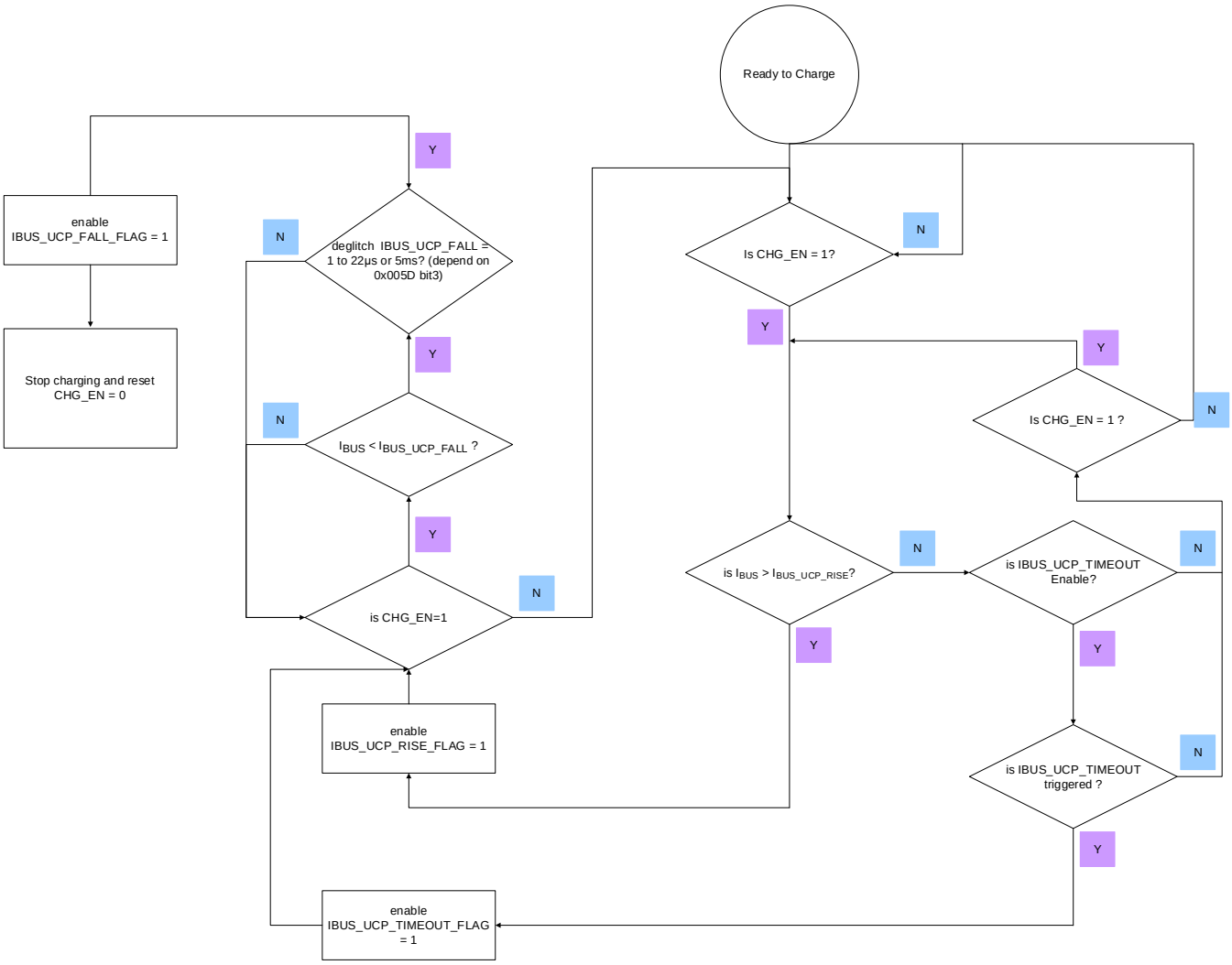


Figure 8. Flow Chart of the IBUS_UCP Function

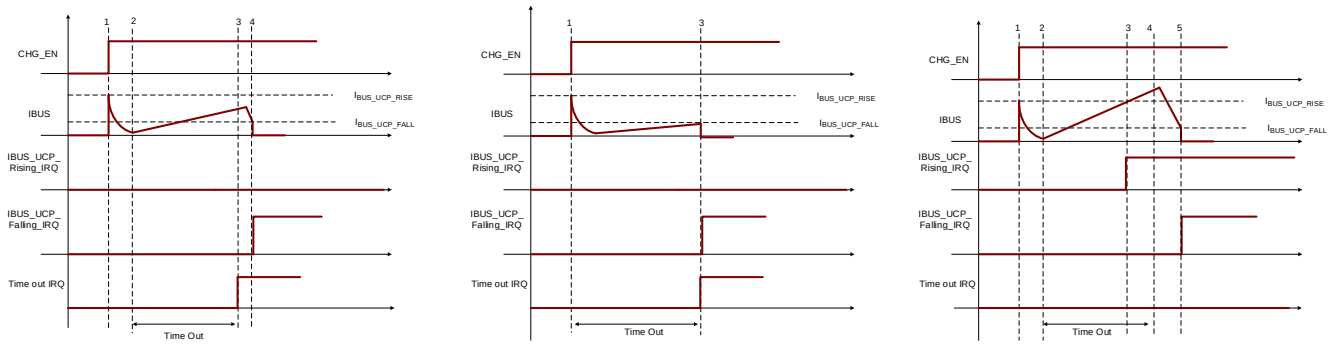


Figure 9. IBUS_UCP Behavior in Different Applications

15.5.6 Device Over-Temperature Protection (TDIE_OTP)

The device integrates a TDIE_OTP to prevent system charging under over-temperature conditions. The TDIE_OTP function monitors the die temperature of the device. If the die temperature exceeds the T_{DIE_OTP} threshold, the device will stop charging and reset the CHG_EN bit to disable.

15.5.7 Flying Capacitor Diagnose (CFLY_DIAG)

The device integrates a CFLY_DIAG function to diagnose the health of flying capacitors. After CHG_EN is enabled, the device starts the soft-start process within t_{SOFT_START}. During the soft-start process, the CFLY_DIAG function will diagnose the resistance between CFL and CFH for each phase. If the resistance is smaller than R_{CFLY_DIAG}, the device will stop the soft-start process and reset CHG_EN to disable. If the device successfully starts charging after the soft-start process, the CFLY_DIAG function will stop activating. If the CFLY shorts after the soft-start, the device can be protected by other protections (e.g., IBUS_OCP, VBAT_OVP, VOUT_OVP, CON_OCP, etc.).

15.5.8 Dropout Voltage Protection (VDR_OVP)

A large voltage drop across the external MOSFET might cause high power loss and significant heat in the system. To prevent this situation, the device integrates a VDR_OVP function to monitor the voltage drop between the VAC and VBUS pins. If the voltage drop exceeds the V_{DR_OVP} threshold, the device will stop charging and reset the CHG_EN bit to disable.

15.5.9 TS Over-Temperature Protection (TS_OTP)

The device integrates a temperature sensing (TS) function to diagnose the external temperature using an NTC thermistor. The voltage on the NTC thermistor varies with different temperatures. Figure 10 shows the DM_TS pin connection for the TS function. The device diagnoses TS_OTP from the DM_TS pin ADC value if DM_TS_CFG(0x005F[6]) is set to 1. If the external sensing voltage is lower than the TS_OTP threshold, the device will stop charging and reset CHG_EN bit to disable. The temperature information is derived from the DM_TS pin ADC value. To use this function, enabling DM ADC conversion is necessary.

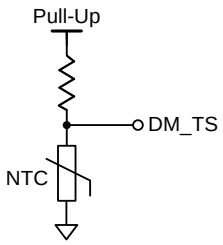


Figure 10. TS Function Connection

15.6 Regulation Feature

The device has VBAT_REG and IBAT_REG regulation functions to manage instant current and voltage changes for the battery. Users can set the regulation thresholds via register settings.

The VBAT_REG function monitors differential voltage between the BATP and BATN/SRP_SYNCIN pins. If the differential voltage exceeds the V_{BAT_REG} threshold, the device will control the OVPGATE voltage to regulate charge current. The IBAT_REG function converts the differential voltage between the SRN_ADDR and BATN/SRP_SYNCIN pins to a current value. If the current value exceeds the I_{BAT_REG} threshold, the device will control the OVPGATE voltage to regulate the charge current. If the regulation functions are triggered and persist for $t_{REG\_TIMEOUT}$, the device will stop charging and reset the CHG_EN bit to disable. When the regulation functions are triggered, the

system should adjust the charging conditions to prevent the device from triggering $t_{REG\_TIMEOUT}$ and VDR_OVP.

15.7 Alarm Feature

The device integrates 9 alarm functions to allow the system to monitor the charging condition. These alarm functions use ADC conversion data to monitor the charging condition. Table 3 shows the relationship between alarm functions and ADC channels; users should ensure that the relevant ADC channel is enabled when using the corresponding alarm functions. If an alarm function is triggered, the device will send an interrupt to the alarm system, but the charger will not stop charging. Table 4 shows the enable conditions for each alarm.

Table 3. Alarm Function with Related ADC Channel

Alarm Function	Related ADC Channel Need Enabled	Sense Node
VBAT_OVP_ALM	VBAT_ADC	BATP and BATN/SRP_SYNCIN pin
IBAT_OCP_ALM	IBAT_ADC	BATN/SRP_SYNCIN and SRN_ADDR pin
IBAT_UCP_ALM	IBAT_ADC	BATN/SRP_SYNCIN and SRN_ADDR pin
VBUS_OVP_ALM	VBUS_ADC	VBUS pin
IBUS_OCP_ALM	IBUS_ADC	Q0
IBUS_UCP_ALM	IBUS_ADC	Q0
TDIE_OTP_ALM	TDIE_ADC	DIE temperature
DP_OV_ALM	DP_ADC	DP pin
DM_OV_ALM	DM_ADC	DM pin

Table 4. Alarm Function Activation List

Alarm Function	Enable Condition
VBUS_OVP_ALM	CHG_EN = 1 or ADC_EN =1
VBAT_OVP_ALM	CHG_EN = 1 or ADC_EN =1
IBUS_OCP_ALM	CHG_EN = 1
IBUS_UCP_ALM	CHG_EN = 1
IBAT_OCP_ALM	CHG_EN = 1
IBAT_UCP_ALM	CHG_EN = 1
TDIE_OTP_ALM	CHG_EN = 1 or ADC_EN =1
DP_OV_ALM	ADC_EN =1 & DP_ADC_DIS=0
DM_OV_ALM	ADC_EN =1 & DM_ADC_DIS=0

15.8 External MOSFET Control by OVPGATE

The RT9756A has an OVPGATE pin to control the external MOSFET. This control can support both single and back-to-back external N-channel MOSFETs. The external MOSFET can be turned on or off by setting the OVPMOS_DIS register. If OVPMOS_DIS is set to 0, the OVPGATE pin will drive external MOSFET to turn on when the VAC voltage is higher than the V_{AC_INSERT} threshold or the VBUS voltage is higher than the V_{BUS_INSERT} threshold for a $t_{DEGLITCH\_VAC\_INSERT}$ time. The OVPGATE pin will drive the external MOSFET to turn off if the V_{AC} voltage is lower than the V_{AC_INSERT} threshold and the V_{BUS} voltage is lower than V_{BUS_INSERT} threshold. If a VAC OVP event occurs, the external MOSFET will also be turned off. This information is detailed in the VAC_OVP function description section. If OVPMOS_DIS is set to 1, the OVPGATE pin will force the external MOSFET to turn off.

The voltage between OVPGATE and VBUS can be set to 10V or 4.8V using OVPGATE(0x0004[0]). If the OVPGATE voltage level needs to be changed, both OVGATE and the charger must be disabled (0x0004[6] = 1 and 0x0000[6] = 0) first, and then the OVPGATE voltage level can be set. After waiting for over 2ms, the OVPGATE can be enabled again. Figure 11 shows the flow of changing the OVPGATE setting. The OVPGATE register control bit cannot be set if OVPMOS_DIS = 0 or CHG_EN = 1.

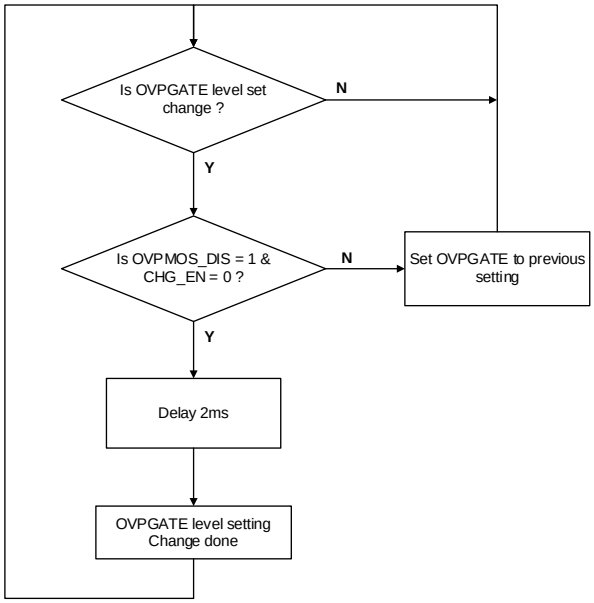


Figure 11. Flow Chart of Changing OVPGATE Setting

15.9 BC1.2 General Description

The BC1.2 detection is performed through the USB2.0 D+ and D- lines upon connection. The BC1.2 specification defines three types of charging ports: Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and Standard Downstream Port (SDP). The detection results are reported in the USB_STATUS register (0x0046[7:5]). When an adapter is plugged in, the device can start BC1.2 detection if BC12_EN is set to 1 (0x0044[7] = 1). The Data Contact Detect timeout can be set using the DCD_TIMEOUT_SET register (0x0044[6:5]). The RT9756A supports both the portable device role (sink role) and the downstream port or charging downstream port (source role). When the device is in the source role, set the HOST_MODE register (0x0044[3:2]) to choose the charging port type. BC12_EN (0x0044[7]), HOST_MODE (0x0044[3:2]), and other protocol functions cannot be enabled at the same time. To change the charging port type, HOST_MODE (0x0044[3:2]) must first be set to 00.

15.10 DP/DM Output Control Mode

The DP/DM output control mode is enabled by setting SET_DPDM_EN (0x0048[7]) to 1. The output is controlled by the programmed values of SET_DP (0x0048[6:4]) and SET_DM (0x0048[3:1]). The device will ignore BC1.2 detection when SET_DPDM_EN is set to 1.

15.11 I^2C Level Selection

The RT9756A supports I^2C VDD levels of 1.2V or 1.8V. When EN_I2C_LEVEL_DETECTION (0x005E[7]) is enabled, the I^2C level can change from 1.2V to 1.8V if the pull-up voltage of the SDA pin is higher than $V_{TH\_I2C\_level}$, and I2C_level (0x005E[6]) will be set to 0. Because the I^2C level detection function is not automatically disabled, users should disable this function after the RT9756A wakes up and the I^2C VDD is ready. If users want to set I2C_level (0x005E[6]), EN_I2C_LEVEL_DETECTION (0x005E[7]) must be disable first. The I^2C level detection function will not change the I^2C level from 1.8V to 1.2V even if the SDA voltage is lower than $V_{TH\_I2C\_level}$. If users want to charge the I^2C level from 1.8V to 1.2V, they must disable EN_I2C_LEVEL_DETECTION (0x005E[7]) first, then set I2C_level (0x005E[6]) to 1.

15.12 Interrupt (INT), STAT, FLAG AND MASK

The $\overline{INT}$ pin is an open-drain structure; users should connect a supply voltage via a current source or pull-up resistors on the pin. When the device triggers an event, the INT pin will pull low for $t_{INT\_PULL\_LOW}$ to notify the host. The register map shows all state, flag, and control bits of the device.

When the device triggers an event with a FLAG, it will send an INT signal to the host and set the FLAG bit to 1. The FLAG bit can be cleared after being read. The device will not send another INT signal until the FLAG is cleared and a new event occurs. The MASK bit can disable the $\overline{INT}$ pin from sending a signal to the host. The STAT and FLAG bits are still updated even if the MASK bit is set to 1.

The STAT bits show the current statue of the device and are updated as the status changes. None of the STAT bits will send an INT signal to the system when triggered, except for SWITCHING_STAT.

15.13 Spread Spectrum

The device integrates a spread spectrum function to help users optimize the EMI influence on system design. The device's switching frequency is determined by the register 0x0001[7:4]. The spectral density will concentrate on the switching frequency. Users can enable the spread spectrum function by setting the register 0x0001[3:2]. Once the spread spectrum function is enabled, the device will modulate the switching frequency by ±10% to reduce the spectral density.

15.14 Parallel Application

For high-capacity battery charging applications, it is possible to use two RT9756A devices in a parallel architecture. The advantages of using a parallel architecture include reducing cable losses, improving the efficiency of the charging system, and shortening the charging period. The high-power solution using two RT9756A devices is shown in Figure 12.

To avoid unstable ripple issues while charging with a parallel architecture, the RT9756A is equipped with a synchronization function at the DP_SYNCOUT pin and the BATN/SRP_SYNCIN pin. These pins are multi-function pins that depend on different configurations. The slave address is configured by the SRN_ADDR pin during power-up, and the configuration mode is set by DP_SYNCOUT_CFG (0x005F[7]) or BATN_SRP_SYNCIN_CFG (0x005F[5]). Table 5 shows the configuration mode settings. When the RT9756A is configured in master mode (RT9756A_M), the DP_SYNCOUT pin provides synchronization pulses with a frequency equal to twice the switching frequency and a 50% duty cycle, so the DP and DM pins cannot implement any protocol functions. When the

RT9756A is configured in slave mode (RT9756A_S), the BATN/SRP_SYNCIN pin is used to receive pulses for synchronization, disabling the VBAT and IBAT sense functions. For synchronization, the DP_SYNCOUT pin of the master device and the BATN/SRP_SYNCIN pin of the slave device should be connected. BATN_SRP_SYNCIN_CFG cannot be set to 1 when the slave address is 0x6F, and DP_SYNCOUT_CFG cannot be set to 1 when the slave address is 0x6E.

In DIV2 mode, all phase angles in the device need to be correctly defined to optimize output ripple and charging efficiency, especially parallel applications. The A phase between the master and slave devices should be shifted by 90 degrees, and the A and B phases in the same device should be shifted by 180 degrees. It is strongly prohibited to change PHASE_A_ANGLE (0x0002[3:2]) and PHASE_B_ANGLE (0x0002[1:0]) during charging.

In parallel applications, only the master device's OVP MOSFET is used. Furthermore, the OVPGATE function should be turned off in the slave device, and the OVPGATE pin should be left floating. Additionally, only the slave device's DP and DM pin can be used. To enable the DPDM protocol function, VAC_INSERT_PROTOCOL_DIS should be set to 1 because all protocol functions are restricted by VAC_INSERT_STAT = 1.

If a parallel architecture is used, the start-up sequence should comply with the following rules. The RT9756A_S should be enabled before the host enables the RT9756A_M to achieve parallel operation. The RT9756A_S will not switch until the BATN/SRP_SYNCIN pin receives synchronization pulses from the RT9756A_M. The communication flow between the smart wall adapter and the parallel charge system is shown in Figure 13.

Table 5. Configuration Mode Setting Description

Slave Address	Register	Configuration
0x6F	DP_SYNCOUT_CFG = 0	Standalone
0x6F	DP_SYNCOUT_CFG = 1	Master
0x6E	BATN_SRP_SYNCIN_CFG = 0	Standalone
0x6E	BATN_SRP_SYNCIN_CFG = 1	Slave

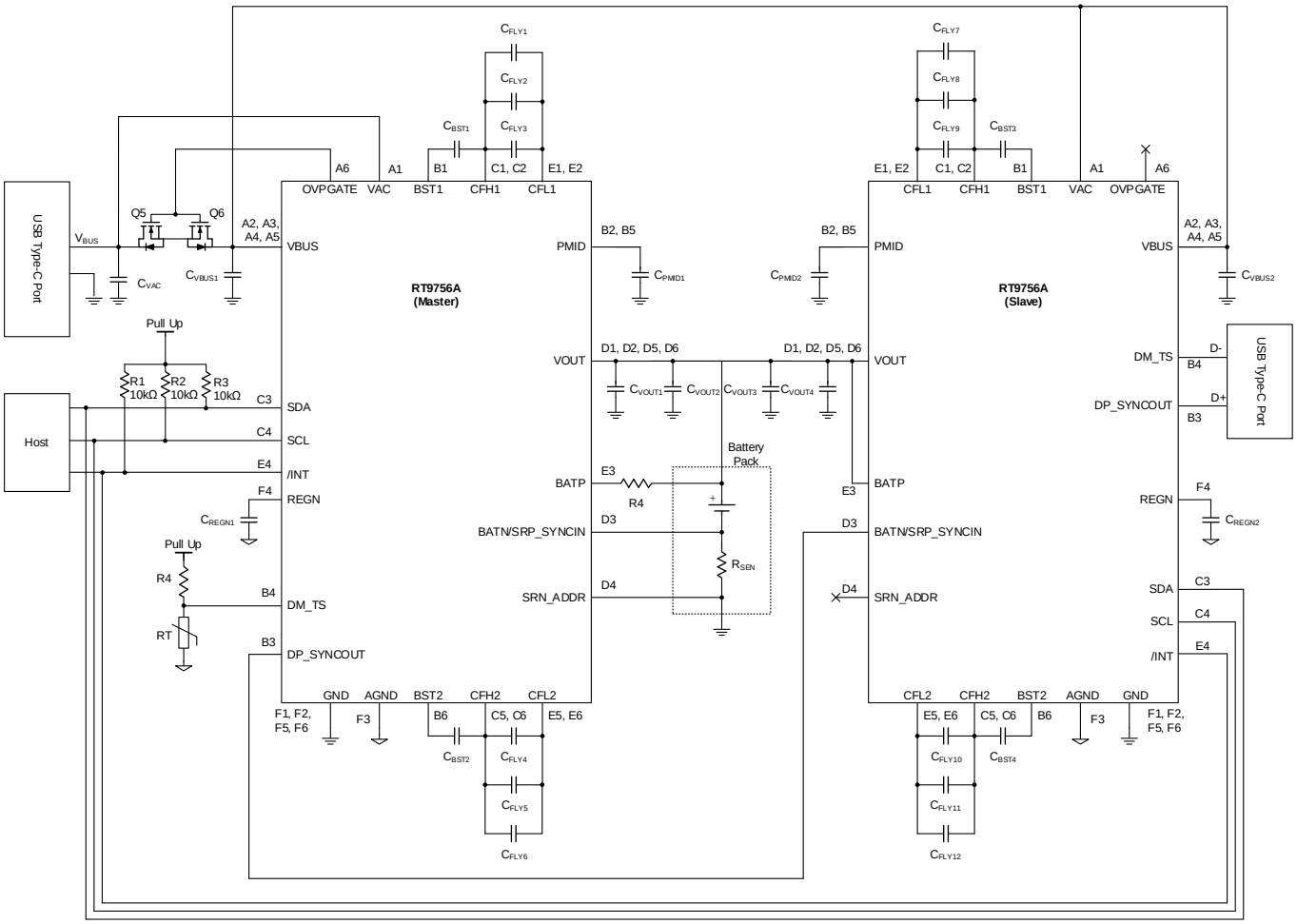


Figure 12. Parallel Application Circuit

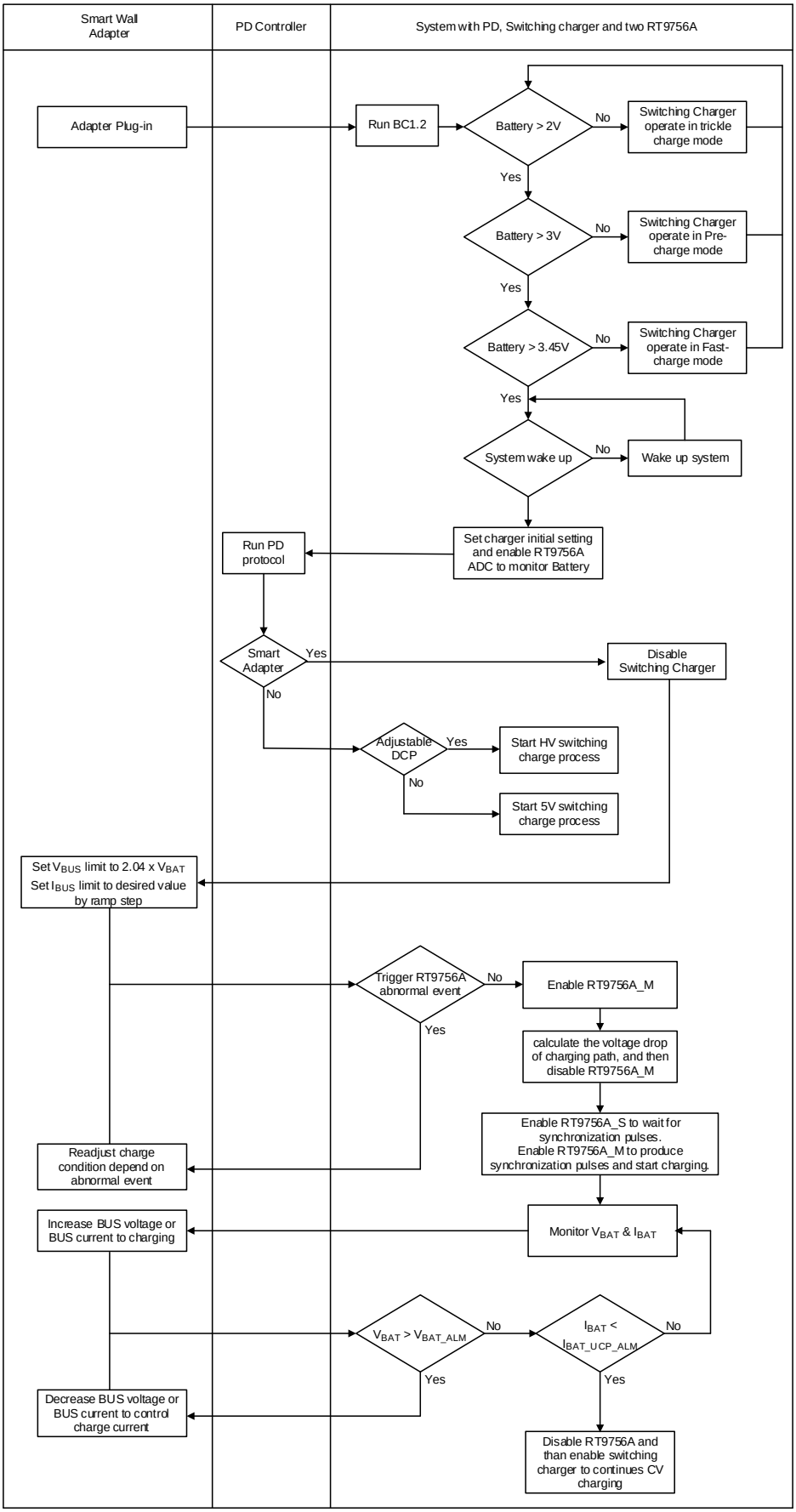


Figure 13. System Control Flow Chart with Parallel Charge System

15.15 I²C Serial Interface

The RT9756A integrates an I²C interface for the host to program charging parameters and monitor device status. The interface requires a serial clock line (SCL) and a serial data line (SDA). The host should initiate a data transfer on the bus and generate the clock signals to permit that transfer. The device operates with an address of 0x6F or 0x6E to receive control input from the host. The SCL and SDA pins are open-drain structures. Users should connect a supply voltage via a current source or pull-up resistors on SCL and SDA. Figure 14 shows the I²C waveform information. The data line must be stable during the high period of the SCL line. The high or low state of SDA can only change when the SCL line is low.

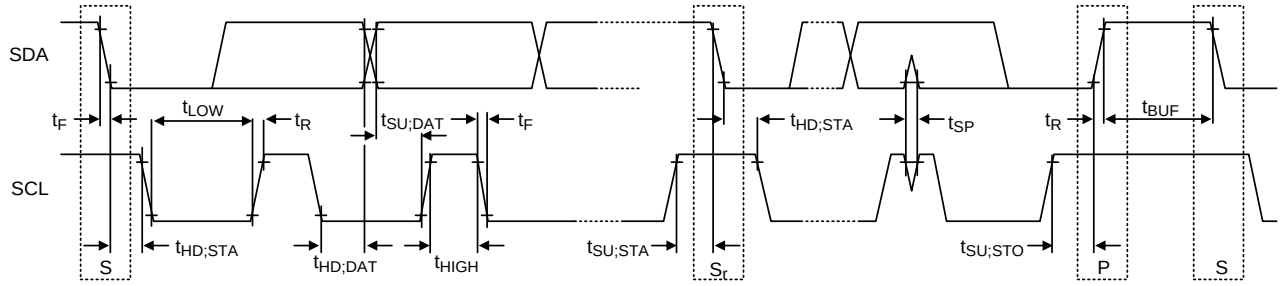


Figure 14. I²C Waveform Information

The RT9756A operates as an I²C slave device with an address of 0x6F or 0x6E (depending on the SRN_ADDR pin). Every byte on SDA line must be 8 bits long. The register address size is two bytes. Send the high byte of the register address first and then the low byte of the register address. Figure 15 shows the byte format. All transactions begin with a START pattern and can be terminated with a STOP pattern. After START, the master should send a slave address. The slave address is 7 bits long followed by the eighth bit as a data direction bit (R/W). Setting the direction bit to 0 indicates a transmission, and setting it to 1 indicates a request for data. The master should take an acknowledge bit after every byte. The master should release the SDA line during the acknowledge clock pulse so the slave device can pull low the SDA line to signal the master that the byte was successfully received. The RT9756A supports multi-read/write operations, and the SCL line can operate at up to 3.4MHz.

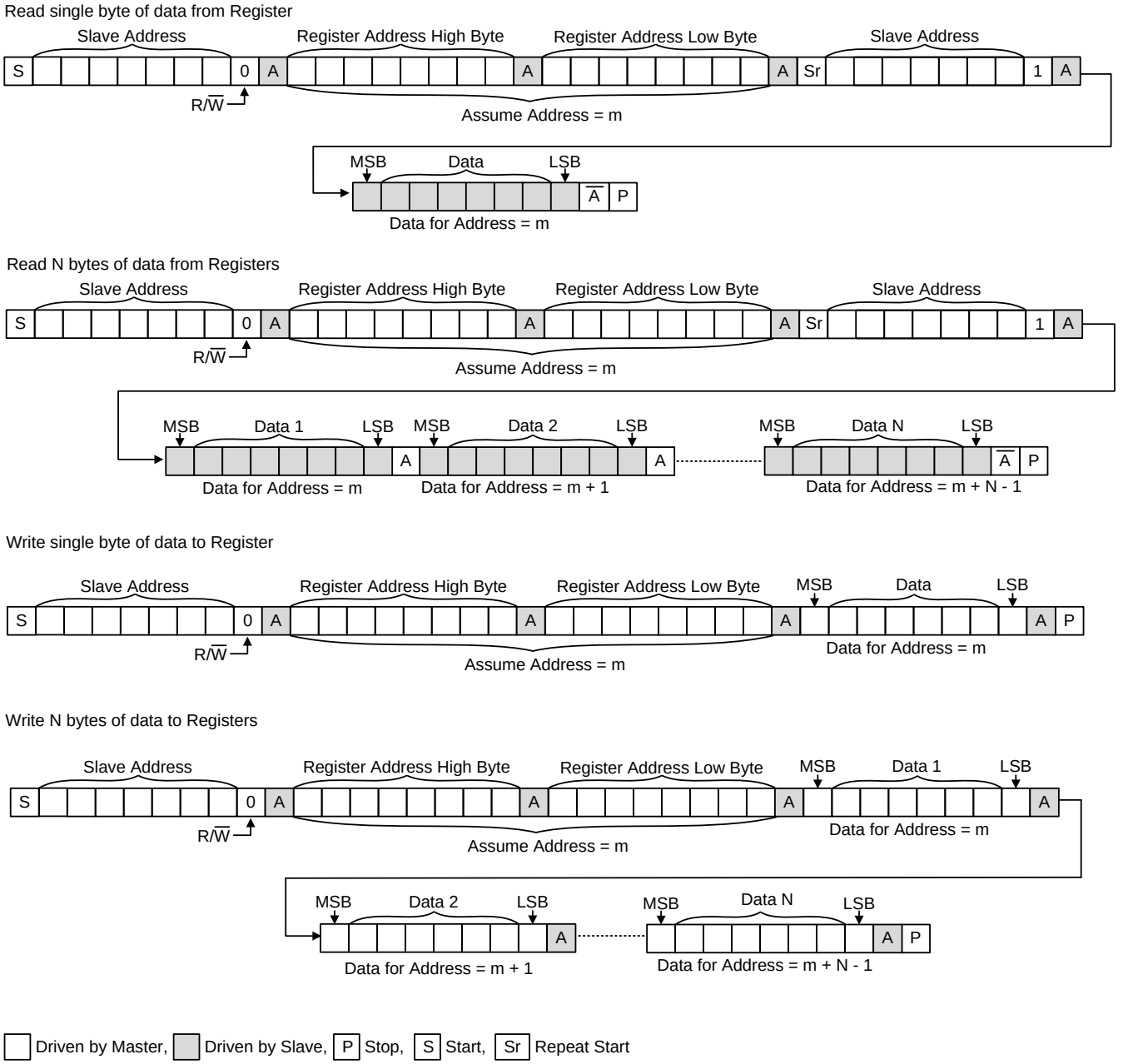


Figure 15. Read and Write Function

15.16 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-36B 2.8 x 2.8 (BSC) package, the thermal resistance, θ_{JA}, is 29.26°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (29.26°C/W) = 3.42W for a WL-CSP-36B 2.8 x 2.8 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 16 allows the designer to inspect the effect of rising ambient temperature on the maximum power dissipation.

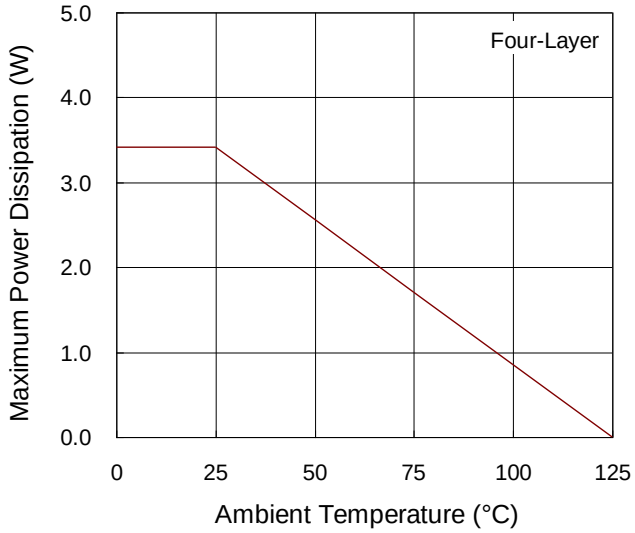


Figure 16. Derating Curve of Maximum Power Dissipation

15.17 Layout Considerations

The following layout guidelines are recommended for the RT9756A:

- Place a low ESR bypass capacitor to GND for the PMID/VOUT/VBUS pin. The bypass capacitor should be placed as close as possible to the RT9756A.
- The capacitor for REGN/BST1/BST2 should be placed as close as possible to the RT9756A.
- Place flying capacitors on the same layer as the RT9756A. The flying capacitors should be placed as close as possible to the RT9756A. The path of the flying capacitors should be as short as possible. The traces and copper pour for the two phases' flying capacitors should be as symmetrical as possible.

- The VBUS and VOUT traces should be as wide as possible to accommodate high charge current.
- Place differential lines for VBATP/VBATN and SRP/SRN. Do not route the differential lines across the power pad, especially near the flying capacitors.

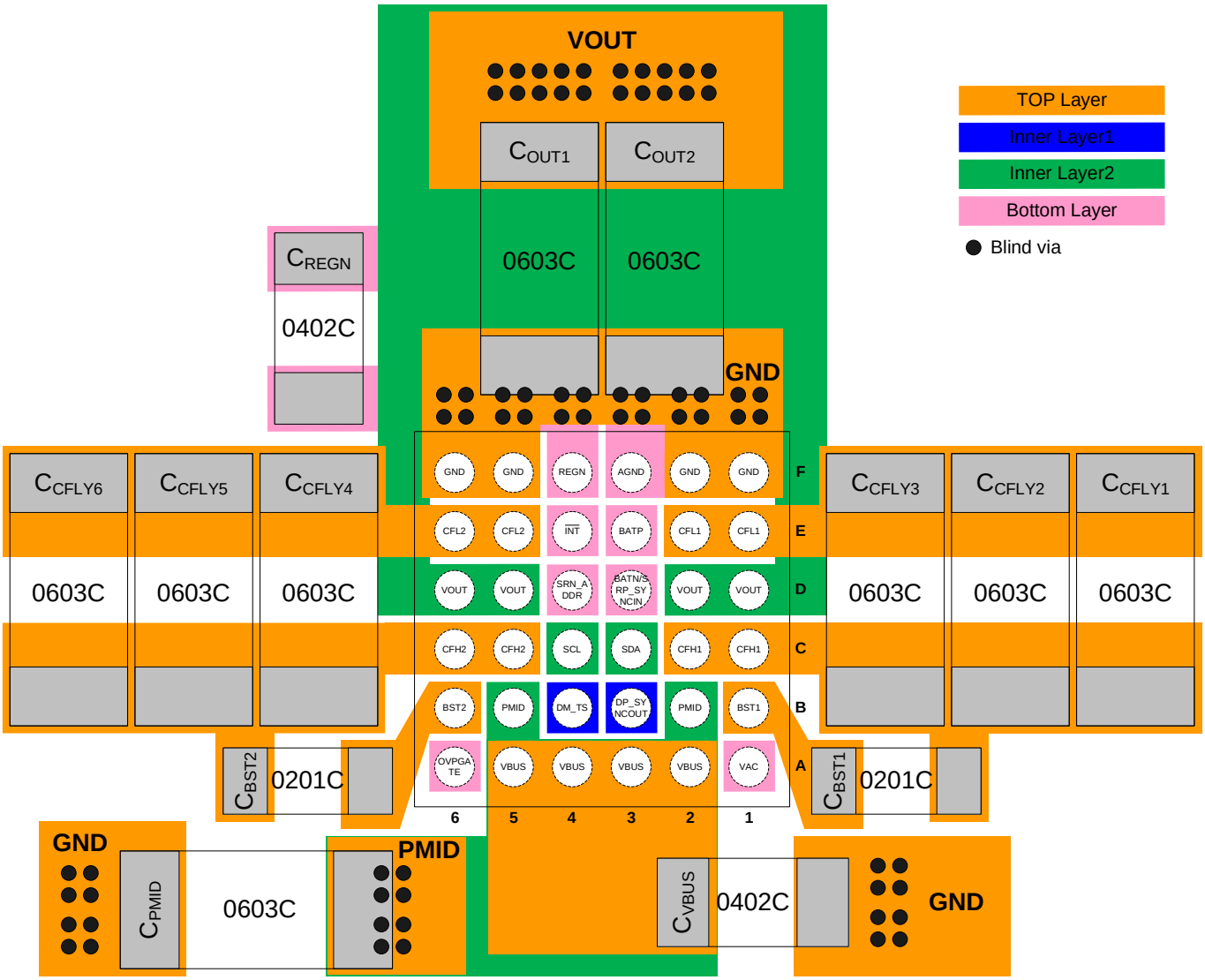


Figure 17. PCB Layout Guide

Note 9. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

16 Functional Register Description

16.1 Register Map

Function Name	STAT	FLAG	MASK	Threshold/ Setting	Enable	Deglitch
REG_RST	--	--	--	--	0x0000[7]	--
CHG_EN	--	--	--	--	0x0000[6]	--
OPERATION_MODE	--	--	--	0x0000[5]	--	--
WDT	--	0x000F[5]	0x0010[5]	0x0000[2:0]	0x0000[3]	--
FSW	--	--	--	0x0001[7:4]	--	--
FSW_SHIFT	--	--	--	0x0001[3:2]	--	--
PHASE_DELAY	--	--	--	0x0001[1:0]	--	--
PHASE_ANGLE	--	--	--	0x0002[3:0]	--	--
OVPGATE	--	--	--	0x0004[0]	0x0004[6]	--
CON_SWITCHING	0x005C[7]	--	0x005C[6]	--	--	--
IC_STAT	0x005C[5:4]	--	--	--	--	--
IBAT_RSEN	--	--	--	0x005E[1:0]	--	--
Pin Configuration	--	--	--	0x005F[7:5]	--	--
VAC_PD	--	0x000B[6]	0x000C[6]	--	0x0005[7]	--
VBUS_PD	--	0x000B[5]	0x000C[5]	--	0x0005[6]	--
CFLY_DIAG	--	0x000F[0]	0x0010[0]	--	0x0002[7]	--
TDIE_OTP	0x004C[3]	0x000D[3]	0x000E[3]	--	0x0002[6]	--
VBUS_LOW_ERR	0x004C[2]	0x000D[2]	0x000E[2]	--	0x0002[5]	--
VBUS_HIGH_ERR	0x004C[1]	0x000D[1]	0x000E[1]	--	0x0002[4]	--
VAC_OVP	0x004B[7]	0x000B[7]	0x000C[7]	0x0004[3:1]	0x0004[4]	--
VDR_OVP	0x004B[4]	0x000B[4]	0x000C[4]	--	0x0005[5]	0x0005[4]
VBUS_OVP	0x004B[3]	0x000B[3]	0x000C[3]	0x0006[5:0]	0x0006[7]	--
IBUS_UCP_RISE	--	0x000B[1]	0x000C[1]	0x0007[6]	0x0007[7]	--
IBUS_UCP_FALL	--	0x000B[0]	0x000C[0]	0x0007[6]	0x0007[7]	0x005D[3]
IBUS_OCP	0x004B[2]	0x000B[2]	0x000C[2]	0x0007[4:0]	0x0007[5]	--
IBUS_OCP_H	--	0x0061[0]	0x0061[1]	--	--	--
VBAT_OVP	0x004C[7]	0x000D[7]	0x000E[7]	0x0008[4:0]	0x0008[7]	--
IBAT_OCP	0x004C[6]	0x000D[6]	0x000E[6]	0x0009[5:0]	0x0009[7]	--
VOUT_OVP	0x004E[0]	0x0049[0]	0x004A[0]	--	0x005E[3]	--
IBAT_REG	0x004C[4]	0x000D[4]	0x000E[4]	0x000A[4:3]	0x000A[5]	--
VBAT_REG	0x004C[5]	0x000D[5]	0x000E[5]	0x000A[1:0]	0x000A[2]	--
VAC_INSERT	0x004C[0]	0x000D[0]	0x000E[0]	--	--	--
VBUS_INSERT	0x004D[7]	0x000F[7]	0x0010[7]	--	--	--
VOUT_INSERT	0x004D[6]	0x000F[6]	0x0010[6]	--	--	--
VAC_UVLO	0x004D[4]	0x000F[4]	0x0010[4]	--	--	--

Function Name	STAT	FLAG	MASK	Threshold/ Setting	Enable	Deglitch
VBUS_UVLO	0x004D[3]	0x000F[3]	0x0010[3]	--	--	--
VDDA_UVLO	--	0x0063[1]	0x0063[0]	--	--	--
IBUS_UCP_TIMEOUT	0x004D[2]	0x000F[2]	0x0010[2]	0x005D[7:5]	--	--
TS_OTP	0x005F[1]	0x005F[3]	0x005F[2]	0x0060[7:0]	0x005F[0]	
ADC	0x004D[1]	0x000F[1]	0x0010[1]	0x0011[6]	0x0011[7]	--
VBUS_ADC	0x0012[5:0] 0x0013[7:0]	--	--	--	0x0011[5]	--
IBUS_ADC	0x0014[5:0] 0x0015[7:0]	--	--	--	0x0011[4]	--
VBAT_ADC	0x0016[5:0] 0x0017[7:0]	--	--	--	0x0011[3]	--
IBAT_ADC	0x0018[5:0] 0x0019[7:0]	--	--	--	0x0011[2]	--
TDIE_ADC	0x001A[7:0]	--	--	--	0x0011[1]	--
VOUT_ADC	0x0056[5:0] 0x0057[7:0]	--	--	--	0x0056[7]	
DP_ADC	0x0058[5:0] 0x0059[7:0]	--	--	--	0x0058[7]	
DM_ADC	0x005A[5:0] 0x005B[7:0]	--	--	--	0x005A[7]	
VBAT_OVP_ALM	0x004E[7]	0x0049[7]	0x004A[7]	0x004F[4:0]	0x004F[7]	--
IBAT_OCP_ALM	0x004E[6]	0x0049[6]	0x004A[6]	0x0050[5:0]	0x0050[7]	--
VBUS_OVP_ALM	0x004E[5]	0x0049[5]	0x004A[5]	0x0051[5:0]	0x0051[7]	--
IBUS_OCP_ALM	0x004E[4]	0x0049[4]	0x004A[4]	0x0052[5:0]	0x0052[7]	--
IBAT_UCP_ALM	0x004E[3]	0x0049[3]	0x004A[3]	0x0053[5:0]	0x0053[7]	--
IBUS_UCP_ALM	0x004E[2]	0x0049[2]	0x004A[2]	0x0054[6:0]	0x0054[7]	--
TDIE_OTP_ALM	0x004E[1]	0x0049[1]	0x004A[1]	0x0055[6:0]	0x0055[7]	--
DP_OV_ALM	0x0061[5]	0x0061[7]	0x0061[3]	--	--	--
DM_OV_ALM	0x0061[4]	0x0061[6]	0x0061[2]	--	--	--
BC1.2	0x0046[7:3] 0x0046[1:0]	0x0045[4:0]	0x0047[4:0]	--	0x0044[7:2]	--
DPDM Manual	--	--	--	0x0048 0x0066 0x006D 0x006E	--	--

16.2 Register Description

I^{2}C Slave Address: 1101111 (6FH) when SRN_ADDR pin is connected to GND

I^{2}C Slave Address: 1101110 (6EH) when SRN_ADDR pin is floating

R: Read only

RC: Read and clear

RW: Read and write

RWC: Read and write, also automatically clear by particular condition

RWSC: Read and write, also automatically set/clear by particular condition

Register Address: 0x0000, Register Name: CHG_CTL1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	REG_RST	0	N	Y	RW	Register reset 0: No register reset (default) 1: Reset registers
6	CHG_EN	0	Y	Y	RW	Charger control bit 0: Disable charge (default) 1: Enable charge
5	OPERATION_ MODE	1	N	N	RW	This bit selects converter operation mode. 0: Bypass mode 1: DIV2 mode (default)
4	Reserved	0	NA	NA	NA	Reserved
3	WDT_DIS	0	N	Y	RW	Disable Watchdog 0: Enable watchdog (default) 1: Disable watchdog
2:0	WDT_TIMER	000	N	Y	RW	Set the watchdog timer. 000: 0.5s (default) 001: 1s 010: 5s 011: 30s 100: 40s 101: 80s 110: 128s 111: 255s

Register Address: 0x0001, Register Name: CHG_CTL2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	FSW_SET	0100	N	Y	RW	Set the switching frequency. 0000 to 1001: 100kHz to 1000kHz in 100kHz steps 1010 to 1111: Reserved 0100: 500kHz (default)
3:2	FREQ_SHIFT	00	N	Y	RW	Adjust switching frequency for EMI. 00: Nominal frequency (default) 01: Nominal frequency + 10% 10: Nominal frequency - 10% 11: Spread spectrum
1:0	PHASE_ DELAY	00	N	Y	RW	Adjust delay time between two phases. It is strongly prohibited during operation. Should be determined before CHG_EN is set to 1. 00: 0ns (default) 01: 15ns 10: 30ns 11: 45ns

Register Address: 0x0002, Register Name: CHG_CTL3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CFLY_DIAG_EN	1	N	Y	RW	Enable CFLY short protection before charge mode is enabled. 0: Disable 1: Enable (default)
6	TDIE_OTP_EN	1	N	Y	RW	Enable TDIE over-temperature protection. 0: Disable 1: Enable (default)
5	VBUS_LOW_ERR_EN	1	N	Y	RW	Enable VBUS voltage too high error protection before charge mode is enabled. 0: Disable 1: Enable (default)
4	VBUS_HIGH_ERR_EN	1	N	Y	RW	Enable VBUS voltage too low error protection before charge mode is enabled. 0: Disable 1: Enable (default)
3:2	PHASE_A_ANGLE	00	N	Y	RW	Select phase A angle in DIV2 mode. It is strongly prohibited during operation. Should be determined before CHG_EN is set to 1. 00: 0 degree (default) 01: 90 degree 10: 180 degree 11: 270 degree (If the RT9756A operates in single application, the bits are recommended to set to 00. If the RT9756A operates in parallel application and enables synchronous function, the bits are recommended to set to 00 in Master mode and 01 in Slave mode.)
1:0	PHASE_B_ANGLE	10	N	Y	RW	Select phase B angle in DIV2 mode. It is strongly prohibited during operation. Should be determined before CHG_EN set 1. 00: 0 degree 01: 90 degree 10: 180 degree (default) 11: 270 degree (If the RT9756A operates in single application, the bits are recommended to set 10. If the RT9756A operates in parallel application and enables synchronous function, the bits are recommended to set 10 in Master mode and 11 in Slave mode.)

Register Address: 0x0003, Register Name: DEVICE_INFO

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	Device Revision	0000	Y	Y	R	Device revision
3:0	Device ID	0111	Y	Y	R	Device ID 0111: RICHTEK product

Register Address: 0x0004, Register Name: VAC_PROTECTION

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	NA	Reserved
6	OVPMOS_DIS	0	Y	Y	RW	Disable OVPGATE. 0: Enable OVPGATE (default) 1: Disable OVPGATE
5	Reserved	0	NA	NA	NA	Reserved
4	VAC_OVP_EN	1	Y	Y	RW	Enable VAC overvoltage protection. 0: Disable 1: Enable (default)
3:1	VAC_OVP	001	N	Y	RW	VAC overvoltage threshold 000-110 is determined by V_{AC_OVP} = 11V + VAC_OVP[2:0] x 1V. Writing all 1 to these bits to set the V_{AC_OVP} to 6.5V. Default = 12V
0	OVPGATE	0	N	N	RW	Select OVPMOS VGS voltage. It is strongly prohibited when OVPMOS is turned on. Should be determined before OVPMOS is turned on. 0: 4.8V (default) 1: 10V

Register Address: 0x0005, Register Name: PD_VDR_OVP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VAC_PD_EN	0	N	N	RW	Enable VAC pull-down resistor. 0: Disable (default) 1: Enable (VAC pull-down resistor is only enabled for 400ms, and then this bit is reset to default.)
6	VBUS_PD_EN	0	N	Y	RW	Enable VBUS pull-down resistor. 0: Disable (default) 1: Enable
5	VDR_OVP_EN	1	N	Y	RW	Enable Dropout overvoltage protection. 0: Disable 1: Enable (default)
4	VDR_OVP_DEGLITCH_SET	0	N	Y	RW	This is the deglitch time after the device reaches the VDR_OVP threshold before the part stops switching. 0: 8μs (default) 1: 5ms
3:0	Reserved	0000	NA	NA	NA	Reserved

Register Address: 0x0006, Register Name: VBUS_OVP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_OVP_EN	1	Y	Y	RW	Enable VBUS overvoltage protection. 0: Disable 1: Enable (default)
6	Reserved	0	NA	NA	NA	Reserved
5:0	VBUS_OVP	011101	N	Y	RW	VBUS overvoltage threshold. The setting is determined by different modes. Device in DIV2 mode: V_{BUS_OVP} = 6V + VBUS_OVP[5:0] X 100mV, Default: 8.9V (b011101) Device in BYPASS mode: V_{BUS_OVP} = 3V + VBUS_OVP[5:0] X 50mV, Default: 4.45V (b011101)

Register Address: 0x0007, Register Name: IBUS_OCP_UCP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBUS_UCP_EN	1	N	Y	RW	Enable IBUS undercurrent protection. 0: Disable 1: Enable (default)
6	IBUS_UCP_THRESHOLD	0	N	Y	RW	This bit sets the IBUS_UCP threshold and it can only be changed prior to enabling switching. The system should control the IBUS current rise to IBUS_UCP_RISE within the IBUS_UCP_TIMEOUT. 0: 300mA rising, 150mA falling (default) 1: 500mA rising, 250mA falling
5	IBUS_OCP_EN	1	N	Y	RW	Enable IBUS overcurrent protection. 0: Disable 1: Enable (default)
4:0	IBUS_OCP	01000	N	Y	RW	IBUS overcurrent threshold. I_{BUS_OCP} = 1A + IBUS_OCP[4:0] x 250mA. 10010 to 11111: I_{BUS_OCP} = 5.5A. Default: 3A (b01000)

Register Address: 0x0008, Register Name: VBAT_OVP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_EN	1	N	Y	RW	Enable VBAT overvoltage protection. 0: Disable 1: Enable (default)
6:5	Reserved	00	NA	NA	NA	Reserved
4:0	VBAT_OVP	00110	N	Y	RW	VBAT overvoltage threshold. V_{BAT_OVP} = 4.2V + VBAT_OVP[4:0] x 25mV Default: 4.35V (b00110)

Register Address: 0x0009, Register Name: IBAT_OCP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_OCP_EN	1	N	Y	RW	Enable IBAT overcurrent protection. 0: Disable 1: Enable (default)
6	Reserved	0	NA	NA	NA	Reserved
5:0	IBAT_OCP	110100	N	Y	RW	IBAT overcurrent threshold I_{BAT_OCP} = 2A + IBAT_OCP[5:0] x 100mA Default: 7.2A (b110100)

Register Address: 0x000A, Register Name: REG_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	NA	Reserved
5	IBAT_REG_EN	0	N	Y	RW	Enable IBAT current regulation. 0: Disable (default) 1: Enable
4:3	IBAT_REG	00	N	Y	RW	These two bits set the threshold below I_{BAT_OCP} at which the part starts regulation. 00: 200mA below I_{BAT_OCP} setting (default) 01: 300mA below I_{BAT_OCP} setting 10: 400mA below I_{BAT_OCP} setting 11: 500mA below I_{BAT_OCP} setting (2A is the minimum level of IBAT_REG.)
2	VBAT_REG_EN	0	N	Y	RW	Enable VBAT voltage regulation. 0: Disable (default) 1: Enable
1:0	VBAT_REG	00	N	Y	RW	These two bits set the threshold below V_{BAT_OVP} at which the part starts regulation. 00: 50mV below V_{BAT_OVP} setting (default) 01: 100mV below V_{BAT_OVP} setting 10: 150mV below V_{BAT_OVP} setting 11: 200mV below V_{BAT_OVP} setting (4.2V is the minimum level of IBAT_REG.)

Register Address: 0x000B, Register Name: INT_FLAG1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VAC_OVP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when a VAC_OVP event occurs. 0: No VAC_OVP fault 1: VAC_OVP fault has occurred (Clear upon read.)
6	VAC_PD_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when a VAC pull-down event occurs. 0: No VAC pull-down 1: VAC pull-down has occurred (Clear upon read.)
5	VBUS_PD_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when a VBUS pull-down event occurs. 0: No VBUS pull=down 1: VBUS pull-down has occurred (Clear upon read.)
4	VDR_OVP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when a VDR_OVP has occurred. 0: No VDR_OVP fault 1: VDR_OVP fault has occurred (Clear upon read.)
3	VBUS_OVP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BUS} exceeds the V_{BUS_OVP} threshold. 0: No VBUS_OVP fault. 1: VBUS_OVP fault has occurred. (Clear upon read.)
2	IBUS_OCP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BUS} exceeds the I_{BUS_OCP} threshold. 0: No IBUS_OCP fault. 1: IBUS_OCP fault has occurred. (Clear upon read.)
1	IBUS_UCP_RISE_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BUS} current exceeds the $I_{BUS\_UCP\_RISE}$ threshold. 0: No IBUS_UCP rising. 1: IBUS_UCP rising has occurred. (Clear upon read.)
0	IBUS_UCP_FALL_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BUS} current is lower than the $I_{BUS\_UCP\_FALL}$ threshold. 0: No IBUS_UCP falling. 1: IBUS_UCP falling has occurred. (Clear upon read.)

Register Address: 0x000C, Register Name: INT_MASK1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VAC_OVP_ MASK	0	N	Y	RW	Mask a VAC_OVP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
6	VAC_PD_ MASK	0	N	Y	RW	Mask a VAC_PD event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
5	VBUS_PD_ MASK	0	N	Y	RW	Mask a VBUS_PD event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
4	VDR_OVP_ MASK	0	N	Y	RW	Mask a VDR_OVP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
3	VBUS_OVP_ MASK	0	N	Y	RW	Mask a VBUS_OVP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
2	IBUS_OCP_ MASK	0	N	Y	RW	Mask a IBUS_OCP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
1	IBUS_UCP_ RISE_MASK	0	N	Y	RW	Mask a IBUS_UCP rising event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
0	IBUS_UCP_ FALL_MASK	0	N	Y	RW	Mask a IBUS_UCP falling event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask

Register Address: 0x000D, Register Name: INT_FLAG2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BAT} exceeds the V_{BAT_OVP} threshold. 0: No VBAT_OVP fault. 1: VBAT_OVP fault has occurred. (Clear upon read.)
6	IBAT_OCP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BAT} exceeds the I_{BAT_OCP} threshold. 0: No IBAT_OCP Fault. 1: IBAT_OCP Fault has occurred. (Clear upon read.)
5	VBAT_REG_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when VBAT_REG has been active. 0: No VBAT_REG. 1: VBAT_REG has occurred. (Clear upon read.)
4	IBAT_REG_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when IBAT_REG has been active. 0: No IBAT_REG. 1: IBAT_REG has occurred. (Clear upon read.)
3	TDIE_OTP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when die temperature exceeds the T_{DIE} threshold. 0: No TDIE_OTP fault. 1: TDIE_OTP fault has occurred. (Clear upon read.)
2	VBUS_LOW_ERR_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BUS} voltage is lower than the $V_{BUS\_LOW\_ERR}$ threshold. 0: No VBUS_LOW_ERR fault. 1: VBUS_LOW_ERR Fault has occurred. (Clear upon read.)
1	VBUS_HIGH_ERR_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BUS} voltage exceeds the $V_{BUS\_HIGH\_ERR}$ threshold. 0: No VBUS_HIGH_ERR fault. 1: VBUS_HIGH_ERR fault has occurred. (Clear upon read.)
0	VAC_INSERT_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{AC} exceeds the V_{AC_INSERT} threshold. 0: No VAC_INSERT. 1: VAC_INSERT has occurred. (Clear upon read.)

Register Address: 0x000E, Register Name: INT_MASK2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_MASK	0	N	Y	RW	Mask a VBAT_OVP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
6	IBAT_OCP_MASK	0	N	Y	RW	Mask a IBAT_OCP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
5	VBAT_REG_MASK	0	N	Y	RW	Mask a VBAT_REG event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
4	IBAT_REG_MASK	0	N	Y	RW	Mask a IBAT_REG event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
3	TDIE_OTP_MASK	0	N	Y	RW	Mask a TDIE_OTP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
2	VBUS_LOW_ERR_MASK	0	N	Y	RW	Mask a VBUS_LOW_ERR event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
1	VBUS_HIGH_ERR_MASK	0	N	Y	RW	Mask a VBUS_HIGH_ERR event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
0	VAC_INSERT_MASK	0	N	Y	RW	Mask a VAC_INSERT event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask

Register Address: 0x000F, Register Name: INT_FLAG3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_ INSERT_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BUS} exceeds the V_{BUS_INSERT} threshold. 0: No VBUS_INSERT. 1: VBUS_INSERT has occurred. (Clear upon read.)
6	VOUT_ INSERT_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{OUT} exceeds the V_{OUT_INSERT} threshold. 0: No VOUT_INSERT. 1: VOUT_INSERT has occurred. (Clear upon read.)
5	WDT_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when a watchdog timeout event occurs. 0: No watchdog time out. 1: Watchdog time out has occurred. (Clear upon read.)
4	VAC_UVLO_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{AC} is lower than the V_{AC_INSERT} threshold. 0: No VAC_UVLO. 1: VAC_UVLO has occurred. (Clear upon read.)
3	VBUS_UVLO_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BUS} is lower than the V_{BUS_INSERT} threshold. 0: No VBUS_UVLO. 1: VBUS_UVLO has occurred. (Clear upon read.)
2	IBUS_UCP_ TIMEOUT_ FLAG	0	N	N	RC	If I_{BUS} does not ramp to the $I_{BUS\_UCP\_RISE}$ threshold within the IBUS_UCP_TIMEOUT period after CHG_EN = 1, the converter will stop switching. Set to 1 and send an $\overline{INT}$ when this event occurs. 0: No IBUS_UCP_TIMEOUT. 1: IBUS_UCP_TIMEOUT has occurred. (Clear upon read.)
1	ADC_DONE_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when ADC conversion is completed in 1-shot mode. 0: No ADC conversion. 1: ADC conversion is completed. (Clear upon read.)
0	CFLY_DIAG_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when CFLY is short during converter's soft-start period. 0: No CFLY short. 1: CFLY short has occurred. (Clear upon read.)

Register Address: 0x0010, Register Name: INT_MASK3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_INSERT_MASK	0	N	Y	RW	Mask a VBUS_INSERT event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
6	VOUT_INSERT_MASK	0	N	Y	RW	Mask a VOUT_INSERT event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
5	WDT_MASK	0	N	Y	RW	Mask a watchdog time out event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
4	VAC_UVLO_MASK	0	N	Y	RW	Mask a VAC_UVLO event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
3	VBUS_UVLO_MASK	0	N	Y	RW	Mask a VBUS_UVLO event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
2	IBUS_UCP_TIMEOUT_MASK	0	N	Y	RW	Mask a IBUS_UCP_TIMEOUT event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
1	ADC_DONE_MASK	0	N	Y	RW	Mask a ADC conversion event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
0	CFLY_DIAG_MASK	0	N	Y	RW	Mask a CFLY short event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask

Register Address: 0x0011, Register Name: ADC_CTRL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ADC_EN	0	Y	Y	RW	Enable ADC conversion. 0: Disable (default) 1: Enable
6	ADC_RATE	0	N	Y	RW	ADC conversion rate 0: Continuous mode (default) 1: 1-shot mode (In 1-shot mode, ADC_EN will be reset to 0 after ADC conversion is completed.)
5	VBUS_ADC_DIS	0	N	Y	RW	Disable VBUS_ADC. 0: Enable Conversion (default) 1: Disable Conversion
4	IBUS_ADC_DIS	0	N	Y	RW	Disable IBUS_ADC. 0: Enable Conversion (default) 1: Disable Conversion
3	VBAT_ADC_DIS	0	N	Y	RW	Disable VBAT_ADC. 0: Enable Conversion (default) 1: Disable Conversion
2	IBAT_ADC_DIS	0	N	Y	RW	Disable IBAT_ADC. 0: Enable Conversion (default) 1: Disable Conversion
1	TDIE_ADC_DIS	0	N	Y	RW	Disable TDIE_ADC. 0: Enable Conversion (default) 1: Disable Conversion
0	Reserved	0	NA	NA	NA	Reserved

Register Address: 0x0012, Register Name: VBUS_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	NA	Reserved
5:0	VBUS_ADC1	000000	N	N	R	VBUS ADC high byte HSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address: 0x0013, Register Name: VBUS_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VBUS_ADC0	00000000	N	N	R	VBUS ADC low byte LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address: 0x0014, Register Name: IBUS_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	NA	Reserved
5:0	IBUS_ADC1	000000	N	N	R	IBUS ADC high byte HSB<5:0>: 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA

Register Address: 0x0015, Register Name: IBUS_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	IBUS_ADC0	00000000	N	N	R	IBUS ADC low byte LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA

Register Address: 0x0016, Register Name: VBAT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	NA	Reserved
5:0	VBAT_ADC1	000000	N	N	R	VBAT ADC high byte HSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address: 0x0017, Register Name: VBAT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VBAT_ADC0	00000000	N	N	R	VBAT ADC low byte LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address: 0x0018, Register Name: IBAT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	NA	Reserved
5:0	IBAT_ADC1	000000	N	N	R	IBAT ADC high byte HSB<5:0>: 8192mA,4096mA, 2048mA, 1024mA, 512mA, 256mA

Register Address: 0x0019, Register Name: IBAT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	IBAT_ADC0	00000000	N	N	R	IBAT ADC low byte LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA

Register Address: 0x001A, Register Name: TDIE_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TDIE_ADC	00000000	N	N	R	TDIE ADC LSB<7:0>: 128°C, 64°C, 32°C, 16°C, 8°C, 4°C, 2°C, 1°C TDIE = –40°C + TDIE_ADC<7:0> x 1°C

Register Address: 0x0044, Register Name: BC12_CTL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	BC12_EN	0	Y	Y	RW	Enable BC1.2 detection. 0: Disable BC1.2 detection (default) 1: Enable BC1.2 detection (BC1.2 detection cannot be enabled if DP_SYNCOUT_CFG = 1, DM_TS_CFG = 1)
6:5	DCD_ TIMEOUT_ SET	01	Y	Y	RW	BC1.2 data contact timer. 00: Disable DCD timeout function 01: Enable 600ms DCD timeout function (default) 10: Enable 900ms DCD timeout function 11: Wait data contact
4	VLGC_OPT	0	Y	Y	RW	Enable primary detection high reference voltage option. 0: Disable (default) 1: Enable
3:2	HOST_MODE	00	Y	Y	RW	Host mode setting in OTG. 00: DPDM floating (default) 01: SDP 10: CDP 11: DCP
1:0	Reserved	00	NA	NA	NA	Reserved

Register Address: 0x0045, Register Name: BC12_FLAG1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	Reserved	0000	NA	NA	NA	Reserved
3	BC12_DONE_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when BC1.2 detection is completed. 0: BC1.2 detection is not ready 1: BC12_DONE_STAT rising detection is completed (Clear upon read.)
2	DCDT_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when data contact detection fails in DCD_TIMEOUT time. 0: DCD Timeout event of BC1.2 detection does not occur 1: DCD Timeout event of BC1.2 detection occurs (Clear upon read.)
1	CDP_DONE_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when CDP flow is completed. 0: No CDP flow 1: CDP flow is completed (This bit will be updated when HOST mode is changed.) (Clear upon read.)
0	CDP_PD_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when CDP primary detection starts. 0: CDP primary detection does not start 1: CDP primary detection starts (This bit will be updated when HOST mode is changed.) (Clear upon read.)

Register Address: 0x0046, Register Name: BC12_STAT1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	USB_STATUS	000	N	Y	R	000: No VBUS 001: VBUS flow is ongoing 010: SDP 011: NSTD 100: DCP 101: CDP 110: Reserved 111: Reserved
4	Reserved	0	NA	NA	NA	Reserved
3	BC12_DONE_STAT	0	N	N	R	USB BC1.2 status bit 0: BC1.2 is not completed 1: BC1.2 is completed
2	Reserved	0	NA	NA	NA	Reserved
1	CDP_DONE_STAT	0	N	N	R	CDP flow status 0: No CDP flow 1: CDP flow is done. (This bit will be updated when HOST mode is changed.)
0	CDP_PD_STAT	0	N	N	R	CDP primary detection start status. 0: CDP primary detection does not start 1: CDP primary detection starts (This bit will be updated when HOST mode is changed.)

Register Address: 0x0047, Register Name: BC12_MASK1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	Reserved	0000	NA	NA	NA	Reserved
3	BC12_DONE_MASK	0	N	Y	RW	Mask a BC12_DONE event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
2	DCDT_MASK	0	N	Y	RW	Mask a DCDT event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
1	CDP_DONE_MASK	0	N	Y	RW	Mask a CDP_DONE event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
0	CDP_PD_MASK	0	N	Y	RW	Mask a CDP_PD event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask

Register Address: 0x0048, Register Name: DPDM_CTL

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	SET_DPDM_EN	0	N	Y	RW	Enable DP, DM voltage setting function. 0: Disable DP, DM set function (default) 1: Enable DP, DM set function
6:4	SET_DP	000	N	Y	RW	DP output voltage selection. 000: Set DP to HZ (default) 001: Set DP to 0 V 010: Set DP to 0.6V 011: Set DP to 1.8V 100: Set DP to 2.8V 101: Set DP to 3.3V 110 to 111: Reserved
3:1	SET_DM	000	N	Y	RW	DM output voltage selection. 000: Set DM to HZ (default) 001: Set DM to 0 V 010: Set DM to 0.6V 011: Set DM to 1.8V 100: Set DM to 2.8V 101: Set DM to 3.3V 110 to 111: Reserved
0	VAC_INSERT_PROTOCOL_DIS	0	N	Y	RW	0: DPDM protocol can be enabled with VAC_INSERT_STATUS = 1 (default) 1: DPDM protocol can be enabled with VAC_INSERT_STATUS = 1 or 0

Register Address: 0x0049, Register Name: INT_FLAG4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BAT} exceeds the $V_{BAT\_OVP\_ALM}$ threshold. 0: No VBAT_OVP_ALM fault 1: VBAT_OVP_ALM fault has occurred (Clear upon read.)
6	IBAT_OCP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BAT} exceeds the $I_{BAT\_OCP\_ALM}$ threshold. 0: No IBAT_OCP_ALM fault 1: IBAT_OCP_ALM fault has occurred (Clear upon read.)
5	VBUS_OVP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{BUS} exceeds the $V_{BUS\_OVP\_ALM}$ threshold. 0: No VBUS_OVP_ALM fault 1: VBUS_OVP_ALM fault has occurred (Clear upon read.)
4	IBUS_OCP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BUS} exceeds the $I_{BUS\_OCP\_ALM}$ threshold. 0: No IBUS_OCP_ALM fault 1: IBUS_OCP_ALM fault has occurred (Clear upon read.)
3	IBAT_UCP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BAT} current is lower than the $I_{BAT\_UCP\_ALM}$ threshold. 0: No IBAT_UCP_ALM rising 1: IBAT_UCP_ALM rising has occurred (Clear upon read.)
2	IBUS_UCP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when I_{BUS} current is lower than $I_{BUS\_UCP\_ALM}$ threshold. 0: No IBUS_UCP_ALM rising 1: IBUS_UCP_ALM rising has occurred (Clear upon read.)
1	TDIE_OTP_ ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when die temperature exceeds the T_{DIE_ALM} threshold. 0: No TDIE_OTP_ALM fault 1: TDIE_OTP_ALM fault has occurred (Clear upon read.)
0	VOUT_OVP_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when V_{OUT} exceeds the V_{OUT_OVP} threshold. 0: No VOUT_OVP fault 1: VOUT_OVP fault has occurred (Clear upon read.)

Register Address: 0x004A, Register Name: INT_MASK4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ ALM_MASK	0	N	Y	RW	Mask a VBAT_OVP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
6	IBAT_OCP_ ALM_MASK	0	N	Y	RW	Mask a IBAT_OCP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
5	VBUS_OVP_ ALM_MASK	0	N	Y	RW	Mask a VBUS_OVP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
4	IBUS_OCP_ ALM_MASK	0	N	Y	RW	Mask a IBUS_OCP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
3	IBAT_UCP_ ALM_MASK	0	N	Y	RW	Mask a IBAT_UCP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
2	IBUS_UCP_ ALM_MASK	0	N	Y	RW	Mask a IBUS_UCP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
1	TDIE_OTP_ ALM_MASK	0	N	Y	RW	Mask a TDIE_OTP_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
0	VOUT_OVP_ MASK	0	N	N	RW	Mask a VOUT_OVP event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask

Register Address: 0x004B, Register Name: INT_STAT1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VAC_OVP_STAT	0	N	N	R	Set to 1 when a VAC_OVP event occurs. Persist until the condition is no longer valid. 0: No VAC_OVP fault 1: VAC_OVP fault has occurred.
6:5	Reserved	00	NA	NA	NA	Reserved
4	VDR_OVP_STAT	0	N	N	R	Set to 1 when a VDR_OVP has occurred. Persist until the condition is no longer valid. 0: No VDR_OVP fault 1: VDR_OVP fault has occurred.
3	VBUS_OVP_STAT	0	N	N	R	Set to 1 when V_{BUS} exceeds the V_{BUS_OVP} threshold. Persist until the condition is no longer valid. 0: No VBUS_OVP fault 1: VBUS_OVP fault has occurred.
2	IBUS_OCP_STAT	0	N	N	R	Set to 1 when I_{BUS} exceeds the I_{BUS_OCP} threshold. Persist until the condition is no longer valid. 0: No IBUS_OCP fault 1: IBUS_OCP fault has occurred.
1:0	Reserved	00	NA	NA	NA	Reserved

Register Address: 0x004C, Register Name: INT_STAT2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_STAT	0	N	N	R	Set to 1 when V_{BAT} exceeds the V_{BAT_OVP} threshold. Persist until the condition is no longer valid. 0: No VBAT_OVP fault. 1: VBAT_OVP fault has occurred.
6	IBAT_OCP_STAT	0	N	N	R	Set to 1 when I_{BAT} exceeds the I_{BAT_OCP} threshold. Persist until the condition is no longer valid. 0: No IBAT_OCP fault. 1: IBAT_OCP fault has occurred.
5	VBAT_REG_STAT	0	N	N	R	Set to 1 when VBAT_REG has been active. Persist until the condition is no longer valid. 0: No VBAT_REG. 1: VBAT_REG has occurred.
4	IBAT_REG_STAT	0	N	N	R	Set to 1 when IBAT_REG has been active. Persist until the condition is no longer valid. 0: No IBAT_REG. 1: IBAT_REG has occurred.
3	TDIE_OTP_STAT	0	N	N	R	Set to 1 when die temperature exceeds the T_{DIE} threshold. Persist until the condition is no longer valid. 0: No TDIE_OTP Fault. 1: TDIE_OTP Fault has occurred.
2	VBUS_LOW_ERR_STAT	0	N	N	R	Set to 1 when V_{BUS} voltage is lower $V_{BUS\_LOW\_ERR}$ threshold. Persist until the condition is no longer valid. 0: No VBUS_LOW_ERR Fault 1: VBUS_LOW_ERR Fault has occurred.
1	VBUS_HIGH_ERR_STAT	0	N	N	R	Set to 1 when V_{BUS} voltage exceeds the $V_{BUS\_HIGH\_ERR}$ threshold. Persist until the condition is no longer valid. 0: No VBUS_HIGH_ERR Fault. 1: VBUS_HIGH_ERR Fault has occurred.
0	VAC_INSERT_STAT	0	N	N	R	Set to 1 when V_{AC} exceeds the V_{AC_INSERT} threshold. Persist until the condition is no longer valid. 0: No VAC_INSERT. 1: VAC_INSERT has occurred.

Register Address: 0x004D, Register Name: INT_STAT3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_ INSERT_STAT	0	N	N	R	Set to 1 when V_{BUS} exceeds the V_{BUS_INSERT} threshold. Persist until the condition is no longer valid. 0: No VBUS_INSERT. 1: VBUS_INSERT has occurred.
6	VOUT_ INSERT_STAT	0	N	N	R	Set to 1 when V_{OUT} exceeds the V_{OUT_INSERT} threshold. Persist until the condition is no longer valid. 0: No VOUT_INSERT 1: VOUT_INSERT has occurred.
5	Reserved	0	NA	NA	NA	Reserved
4	VAC_UVLO_ STAT	0	N	N	R	Set to 1 when V_{AC} is lower than the V_{AC_INSERT} threshold. Persist until the condition is no longer valid. 0: No VAC_UVLO. 1: VAC_UVLO has occurred.
3	VBUS_UVLO_ STAT	0	N	N	R	Set to 1 when V_{BUS} is lower than the V_{BUS_INSERT} threshold. Persist until the condition is no longer valid. 0: No VBUS_UVLO. 1: VBUS_UVLO has occurred.
2	IBUS_UCP_ TIMEOUT_ STAT	0	N	N	R	Set to 1 when IBUS_UCP_TIMEOUT event occurs. Persist until the condition is no longer valid. 0: No IBUS_UCP_TIMEOUT. 1: IBUS_UCP_TIMEOUT is occurring.
1	ADC_DONE_ STAT	0	N	N	R	Set to 1 when the ADC conversion is completed in 1-shot mode. This bit will change to '0' when an ADC conversion is requested in 1-shot mode, and it will change back to '1' when the conversion is completed. During continuous conversion mode, this bit will be '0' 0: Conversion not complete. 1: Conversion complete.
0	Reserved	0	NA	NA	NA	Reserved

Register Address: 0x004E, Register Name: INT_STAT4

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ ALM_STAT	0	N	N	R	Set to 1 when V_{BAT} exceeds the $V_{BAT\_OVP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No VBAT_OVP_ALM fault 1: VBAT_OVP_ALM fault has occurred.
6	IBAT_OCP_ ALM_STAT	0	N	N	R	Set to 1 when I_{BAT} exceeds the $I_{BAT\_OCP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No IBAT_OCP_ALM fault 1: IBAT_OCP_ALM fault has occurred.
5	VBUS_OVP_ ALM_STAT	0	N	N	R	Set to 1 when V_{BUS} exceeds the $V_{BUS\_OVP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No VBUS_OVP_ALM fault 1: VBUS_OVP_ALM fault has occurred.
4	IBUS_OCP_ ALM_STAT	0	N	N	R	Set to 1 when I_{BUS} exceeds the $I_{BUS\_OCP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No IBUS_OCP_ALM fault 1: IBUS_OCP_ALM fault has occurred.
3	IBAT_UCP_ ALM_STAT	0	N	N	R	Set to 1 when I_{BAT} current is lower than the $I_{BAT\_UCP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No IBAT_UCP_ALM rising 1: IBAT_UCP_ALM rising has occurred.
2	IBUS_UCP_ ALM_STAT	0	N	N	R	Set to 1 when I_{BUS} current is lower than the $I_{BUS\_UCP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No IBUS_UCP_ALM rising 1: IBUS_UCP_ALM rising has occurred.
1	TDIE_OTP_ ALM_STAT	0	N	N	R	Set to 1 when die temperature exceeds the $T_{DIE\_OTP\_ALM}$ threshold. Persist until the condition is no longer valid. 0: No TDIE_OTP_ALM Fault 1: TDIE_OTP_ALM Fault has occurred.
0	VOUT_OVP_ STAT	0	N	N	R	Set to 1 when V_{OUT} exceeds the V_{OUT_OVP} threshold. Persist until the condition is no longer valid. 0: No VOUT_OVP fault 1: VOUT_OVP fault has occurred.

Register Address: 0x004F, Register Name: VBAT_OVP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBAT_OVP_ALM_DIS	0	N	Y	RW	Disable VBAT_OVP_ALM. 0: Enable (default) 1: Disable
6:5	Reserved	00	NA	NA	NA	Reserved
4:0	VBAT_OVP_ALM	00000	N	Y	RW	Battery overvoltage alarm threshold. $V_{BAT\_OVP\_ALM}$ = 4.2V + VBAT_OVP_ALM[4:0] x 25mV Default: 4.2V (b00000)

Register Address: 0x0050, Register Name: IBAT_OCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_OCP_ALM_DIS	0	N	Y	RW	Disable IBAT_OCP_ALM. 0: Enable (default) 1: Disable
6	Reserved	0	NA	NA	NA	Reserved
5:0	IBAT_OCP_ALM	110010	N	Y	RW	Battery overcurrent alarm threshold. $I_{BAT\_OCP\_ALM}$ = 2A + IBAT_OCP_ALM[5:0] X 100mA Default: 7A (b110010)

Register Address: 0x0051, Register Name: VBUS_OVP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VBUS_OVP_ALM_DIS	0	N	Y	RW	Disable VBUS_OVP_ALM. 0: Enable (default) 1: Disable
6	Reserved	0	NA	NA	NA	Reserved
5:0	VBUS_OVP_ALM	011100	N	Y	RW	VBUS overvoltage alarm threshold. The setting is determined by different modes. Device in DIV2 mode: V_{BUS_OVP} = 6V + VBUS_OVP[5:0] x 100mV, Default: 8.8V (b011100) Device in BYPASS mode: V_{BUS_OVP} = 3V + VBUS_OVP[5:0] x 50mV, Default: 4.4V (b011100)

Register Address: 0x0052, Register Name: IBUS_OCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBUS_OCP_ALM_DIS	0	N	Y	RW	Disable IBUS_OCP_ALM. 0: Enable (default) 1: Disable
6	Reserved	0	NA	NA	NA	Reserved
5:0	IBUS_OCP_ALM	011100	N	Y	RW	IBUS overcurrent alarm threshold. The setting is determined by $I_{BUS\_OCP\_ALM}$ = IBUS_OCP_ALM[5:0] x 100mA. Default: 2.8A (b011100)

Register Address: 0x0053, Register Name: IBAT_UCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBAT_UCP_ALM_DIS	0	N	Y	RW	Disable IBAT_UCP_ALM. 0: Enable (default) 1: Disable
6	Reserved	0	NA	NA	NA	Reserved
5:0	IBAT_UCP_ALM	101000	N	Y	RW	IBAT undercurrent alarm threshold. $I_{BAT\_UCP\_ALM}$ = IBAT_UCP_ALM [5:0] x 50mA Default: 2A (b101000)

Register Address: 0x0054, Register Name: IBUS_UCP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	IBUS_UCP_ALM_DIS	0	N	Y	RW	Disable IBUS_UCP_ALM. 0: Enable (default) 1: Disable
6:0	IBUS_UCP_ALM	0101000	N	Y	RW	IBUS undercurrent alarm threshold. $I_{BUS\_UCP\_ALM}$ = IBUS_UCP_ALM [6:0] x 25mA Default: 1A (b0101000)

Register Address: 0x0055, Register Name: TDIE_OTP_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	TDIE_OTP_ALM_DIS	0	N	Y	RW	Disable TDIE_OTP_ALM. 0: Enable (default) 1: Disable
6:0	TDIE_OTP_ALM	1100100	N	Y	RW	TDIE alarm threshold. T_{DIE_ALM} = 25°C + TDIE_ALM[6:0] x 1°C Default: 125°C (b1100100)

Register Address: 0x0056, Register Name: VOUT_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VOUT_ADC_DIS	0	N	Y	RW	Disable VOUT_ADC. 0: Enable conversion (default) 1: Disable conversion
6	Reserved	0	NA	NA	NA	Reserved
5:0	VOUT_ADC1	000000	N	N	R	VOUT ADC high byte HSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address: 0x0057, Register Name: VOUT_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	VOUT_ADC0	00000000	N	N	R	VOUT ADC low byte LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address: 0x0058, Register Name: DP_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DP_ADC_DIS	1	N	Y	RW	Disable DP ADC. 0: Enable 1: Disable (default)
6	Reserved	0	NA	NA	NA	Reserved
5:0	DP_ADC1	000000	N	Y	R	DP ADC high byte HSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address: 0x0059, Register Name: DP_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	DP_ADC0	00000000	N	Y	R	DP ADC LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address: 0x005A, Register Name: DM_ADC1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DM_ADC_DIS	1	N	Y	RW	Disable DM ADC. 0: Enable 1: Disable (default)
6	Reserved	0	NA	NA	NA	Reserved
5:0	DM_ADC1	000000	N	Y	R	DM ADC high byte HSB<5:0>: 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV

Register Address: 0x005B, Register Name: DM_ADC0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	DM_ADC0	00000000	N	Y	R	DM ADC low byte LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV

Register Address: 0x005C, Register Name: CON_STAT

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CON_ SWITCHING_ STAT	0	N	N	R	Set to 1 and send an $\overline{INT}$ when the converter starts switching and IBUS_UCP_TIMEOUT timer starts. Only one $\overline{INT}$ is sent when switching starts. Persist until the condition is no longer valid. 0: No CON_SWITCHING 1: SWITCHING occurs.
6	CON_ SWITCHING_ MASK	0	N	N	RW	Mask a CON_SWITCHING event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
5:4	IC_STAT	00	N	N	R	Indicate converter operation status. 00: Standby mode 01: Bypass mode 10: Forward DIV2 mode 11: Reserved
3:0	Reserved	0000	NA	NA	NA	Reserved

Register Address: 0x005D, Register Name: IBUS_UCP_TIMEOUT

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:5	IBUS_UCP_ TIMEOUT	111	N	Y	RW	Adjustable timeout for I_{BUS} to rise to the $I_{BUS\_UCP\_RISE}$ threshold. 000: Timeout disabled 001: 12.5ms 010: 25ms 011: 50ms 100: 100ms 101: 400ms 110: 1.5s 111: 100s (default)
4	Reserved	0	NA	NA	NA	Reserved
3	IBUS_UCP_ FALL_ DEGLITCH_ SET	0	N	Y	RW	This bit sets the deglitch time for VBUS_UCP_FALL. 0: 22μs (default) 1: 5ms
2:0	Reserved	000	NA	NA	NA	Reserved

Register Address: 0x005E, Register Name: other1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	EN_I2C_ LEVEL_ DETECTION	1	NA	NA	RW	0: Disable 1: Enable (default)
6	I2C_level	1	NA	NA	RW	0: 1.8V 1: 1.2V (default)
5:4	Reserved	00	NA	NA	NA	Reserved
3	VOUT_OVP_ EN	1	N	Y	RW	Enable VOUT overvoltage protection. 0: Disable 1: Enable (default)
2	Reserved	1	NA	NA	NA	Reserved
1:0	IBAT_RSEN	01	N	N	RW	This bit selects the external battery current sense resistor value. 00: 1mΩ 01: 2mΩ (default) 10: 5mΩ 11: 10mΩ

Register Address: 0x005F, Register Name: other2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DP_SYNCOUT_CFG	0	N	N	RW	DP_SYNCOUT pin configuration. 0: DP_SYNCOUT pin is configured as DP pin. (default) 1: DP_SYNCOUT pin is configured as SYNCOUT pin. (All DP pin functions are invalid when DP_SYNCOUT = 1.)
6	DM_TS_CFG	0	N	N	RW	DM_TS pin configuration. 0: DM_TS pin is configured as DM pin. (default) 1: DM_TS pin is configured as TS pin. (All TS functions are invalid when DM_TS = 0. All DM pin functions are invalid when DM_TS = 1.)
5	BATN_SRP_SYNCIN_CFG	0	N	N	RW	BATN/SRP_SYNCIN pin configuration 0: BATN/SRP_SYNCIN pin is configured as BATN/SRP pin. (default) 1: BATN/SRP_SYNCIN pin is configured as SYNCIN pin. (All sensing and protection of VBAT and IBAT are invalid when BATN/SRP_SYNCIN = 1.)
4	Reserved	0	NA	NA	NA	Reserved
3	TS_OTP_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when TS ADC is lower than the TS_OTP threshold. 0: No TS_OTP 1: TS_OTP occurs. (Clear upon read.)
2	TS_OTP_MASK	0	N	Y	RW	Mask a TS_OTP event to send an $\overline{INT}$ 0: Unmask (default) 1: Mask
1	TS_OTP_STAT	0	N	N	R	Set to 1 when TS ADC is lower than TS_OTP threshold. Persist until the condition is no longer valid. 0: No TS_OTP 1: TS_OTP occurs.
0	TS_OTP_EN	0	N	Y	RW	Enable TS_OTP. 0: Disable (default) 1: Enable

Register Address: 0x0060, Register Name: TS_OTP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:0	TS_OTP	00000000	N	Y	RW	TS_OTP Threshold TS_OTP = TS_OTP[7:0] x 7mV Default: 0V (b00000000)

Register Address: 0x0061, Register Name: DPDM_OV_ALM

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DP_OV_ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when DP_ADC exceeds 4.5V. 0: No DP_OV_ALM fault 1: DP_OV_ALM fault has occurred. (Clear upon read.)
6	DM_OV_ALM_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$ when DM_ADC exceeds 4.5V. 0: No DM_OV_ALM fault 1: DM_OV_ALM fault has occurred. (Clear upon read.)
5	DP_OV_ALM_STAT	0	N	N	R	DP_OV_ALM status when DP_ADC exceeds 4.5V. Persist until the condition is no longer valid. 0: No DP_OV_ALM fault 1: DP_OV_ALM fault has occurred.
4	DM_OV_ALM_STAT	0	N	N	R	DM_OV_ALM status when DM_ADC exceeds 4.5V. Persist until the condition is no longer valid. 0: No DM_OV_ALM fault 1: DM_OV_ALM fault has occurred.
3	DP_OV_ALM_MASK	0	N	Y	RW	Mask a DP_OV_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
2	DM_OV_ALM_MASK	0	N	Y	RW	Mask a DM_OV_ALM event to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
1	IBUS_OCP_H_MASK	0	N	Y	RW	Mask a IBUS_OCP_H to send an $\overline{INT}$. 0: Unmask (default) 1: Mask
0	IBUS_OCP_H_FLAG	0	N	N	RC	Set to 1 and send an $\overline{INT}$, when IBUS_OCP_H trigger. 0: No IBUS_OCP_H fault. 1: IBUS_OCP_H fault has occurred. (Clear upon read)

Register Address: 0x0062, Register Name: REVISION

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:2	Reserved	000000	NA	NA	NA	Reserved
1:0	PRODUCT_ID	01	N	N	RO	01: RT9756A

Register Address: 0x0063, Register Name: other3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:3	Reserved	00000	NA	NA	NA	Reserved
2	CHIP_RESET_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{\text{INT}}$ when power-on is ready. 0: No power-on ready fault. 1: Power-on ready has occurred. (Clear upon read.)
1	VDDA_UVLO_ FLAG	0	N	N	RC	Set to 1 and send an $\overline{\text{INT}}$ when VDDA_UVLO is triggered. 0: No VDDA_UVLO fault. 1: VDDA_UVLO fault occurs. (Clear upon read.)
0	VDDA_UVLO_ MASK	0	N	Y	RW	Mask a VDDA_UVLO to send an $\overline{\text{INT}}$. 0: Unmask (default) 1: Mask

Register Address: 0x0066, Register Name: DPDM_SEL1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	DP_DISCHG_SEL	11	N	Y	RW	DP discharge level selection when SET_DPDM_EN = 1. 00: Bypass 01: 20kΩ 10: 45μA 11: 60μA (default)
5:4	DM_DISCHG_SEL	11	N	Y	RW	DM discharge level selection when SET_DPDM_EN = 1. 00: Bypass 01: 20kΩ 10: 45μA 11: 60μA (default)
3:2	DP_PULL_SEL	11	N	Y	RW	DP pull-up resistor level selection when SET_DPDM_EN = 1. 00: 1.2kΩ 01: 2.7kΩ 10: 15kΩ 11: Bypass (default)
1:0	DM_PULL_SEL	11	N	Y	RW	DM pull-up resistor level selection when SET_DPDM_EN = 1. 00: 1.2kΩ 01: 2.7kΩ 10: 15kΩ 11: Bypass (default)

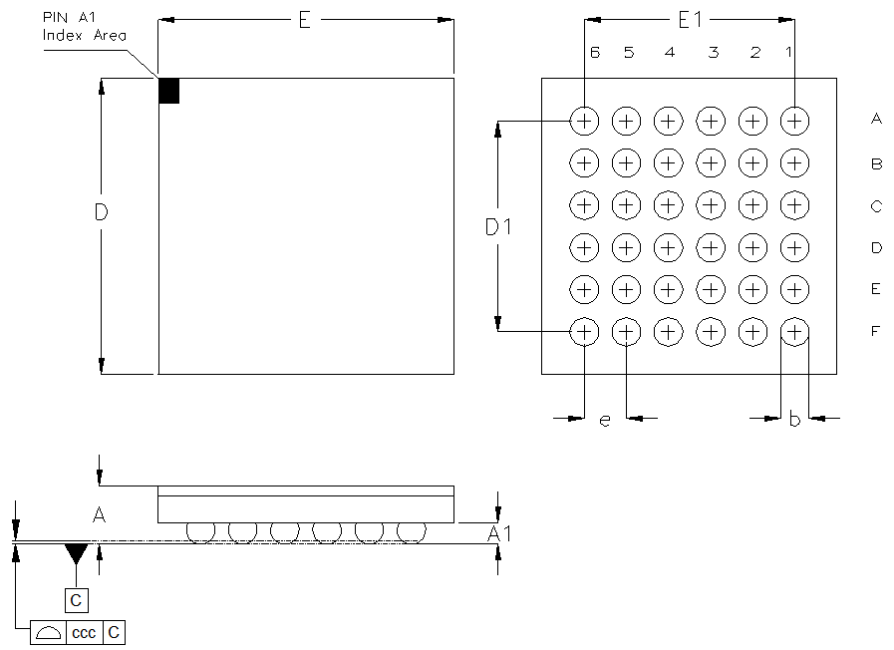
Register Address: 0x006D, Register Name: DPDM_CON5

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DP_DISCHG_EN	0	N	Y	RW	DP discharge current or resistor enable control when SET_DPDM_EN = 1. 0: Disable (default) 1: Enable
6:4	Reserved	110	NA	NA	NA	Reserved
3	DM_DISCHG_EN	0	N	Y	RW	DM discharge current or resistor enable control when SET_DPDM_EN = 1. 0: Disable (default) 1: Enable
2:0	Reserved	110	NA	NA	NA	Reserved

Register Address: 0x006E, Register Name: DPDM_CON6

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	DP_PULL_IEN	0	N	Y	RW	DP pull-up current source enable control when SET_DPDM_EN = 1. 0: Disable (default) 1: Enable (10μA)
6	DP_PULL_REN	0	N	Y	RW	DP pull-up resistor enable control when SET_DPDM_EN = 1. 0: Disable (default) 1: Enable
5:4	Reserved	11	NA	NA	NA	Reserved
3	DM_PULL_IEN	0	N	Y	RW	DM pull-up current source enable control when SET_DPDM_EN = 1. 0: Disable (default) 1: Enable (10μA)
2	DM_PULL_REN	0	N	Y	RW	DM pull-up resistor enable control when SET_DPDM_EN = 1. 0: Disable (default) 1: Enable
1:0	Reserved	110	NA	NA	NA	Reserved

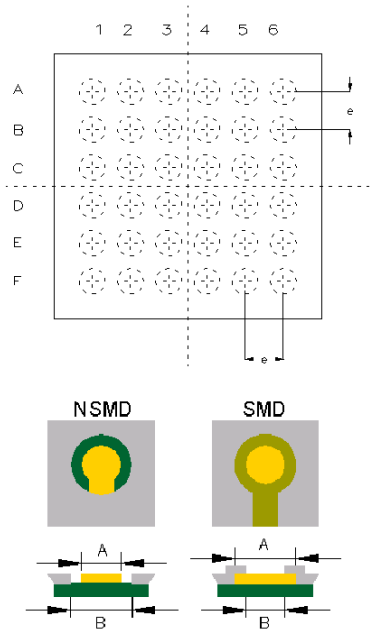
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.765	2.835	0.109	0.112
D1	2.000		0.079	
E	2.765	2.835	0.109	0.112
E1	2.000		0.079	
e	0.400		0.016	
ccc	0.020		0.001	

36B WL-CSP 2.8x2.8 Package (BSC)

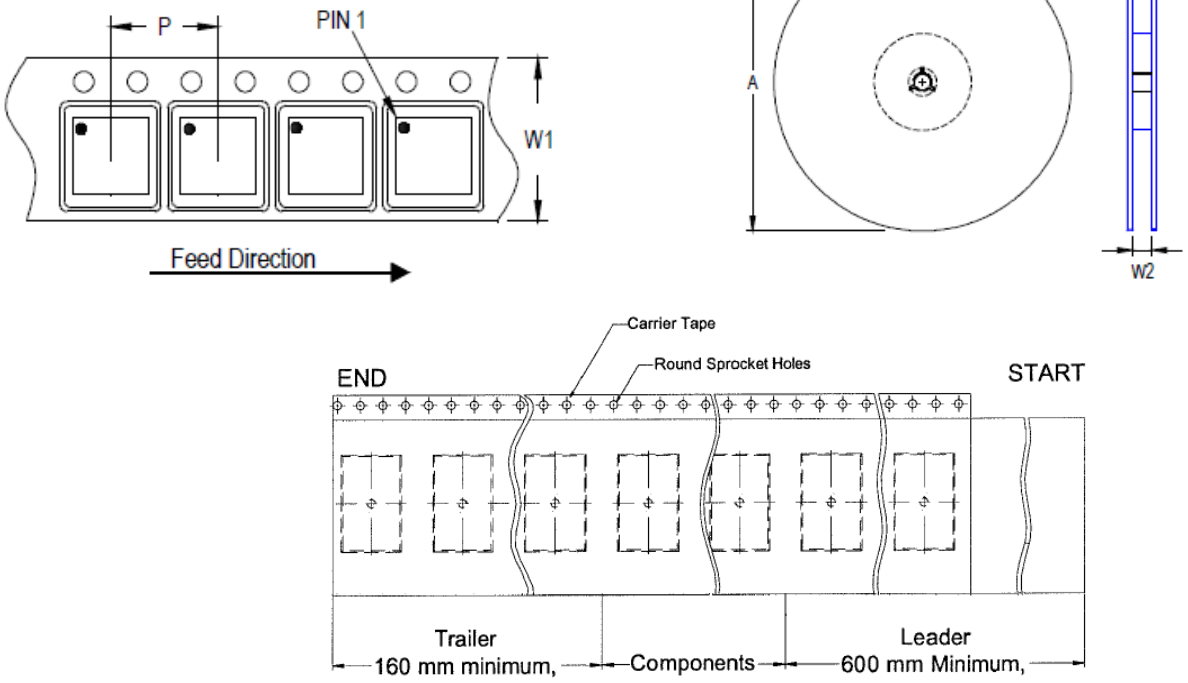
18 Footprint Information



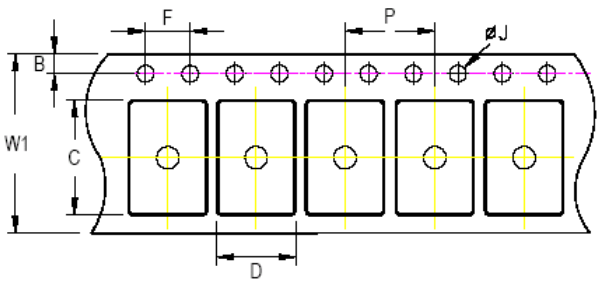
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.8x2.8-36(BSC)	36	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

19 Packing Information

19.1 RT9756AWSC Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.8x2.8	8	4	180	7	3,000	160	600	8.4/9.9



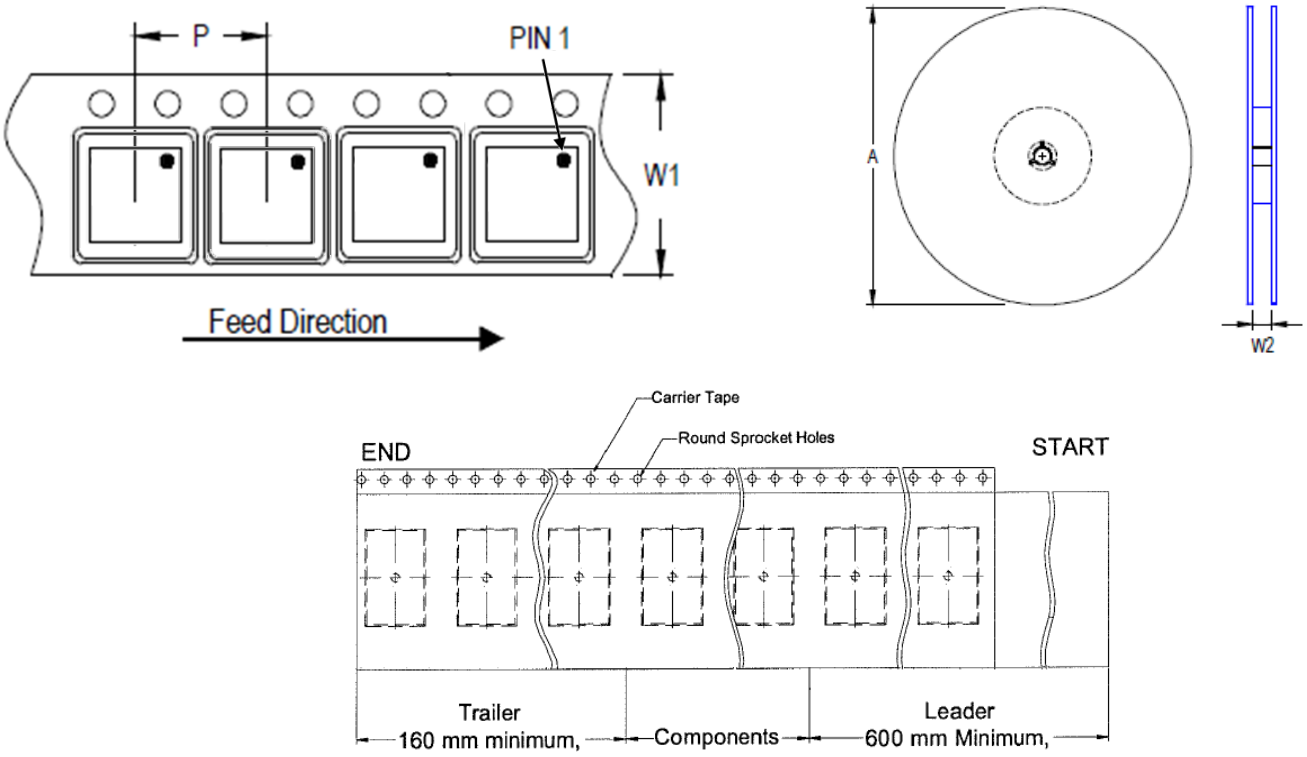
C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

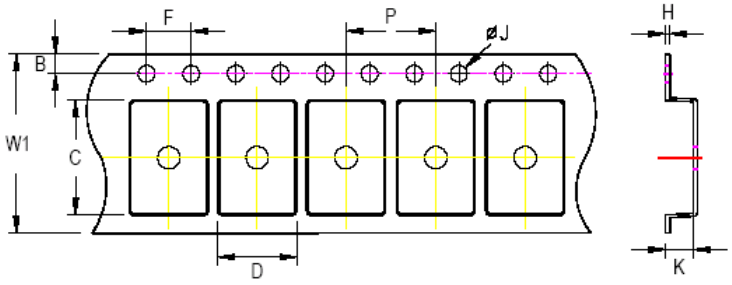
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 RT9756AWSC(2) Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.8x2.8	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.3 RT9756AWSC Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.8x2.8	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.4 RT9756AWSC(2) Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.8x2.8	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.5 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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20 Datasheet Revision History

Version	Date	Description	Item
00	2023/7/7	Modify	Features on P1, 2 Ordering Information on P2 Functional Pin Description on P3, 4 Absolute Maximum Ratings on P5 Electrical Characteristics on P6 to 16 Typical Application Circuit on P20 Typical Operating Characteristics on P21 Register Description on P22, 23, 24, 25, 26, 28, 39, 42, 51 Application Information on P59, 60, 73, 74, 75, 76, 77
01	2024/1/18	Modify	General Description on P1 Ordering Information on P2 Recommended Operating Conditions on P6 Electrical Characteristics on P10 Packing Information on P83, 84, 85, 86
02	2024/10/18	Modify	*Ordering Information on page 2* - Updated ordering information and added note *Application Information on page 46* - Updated declaration *Packing Information on page 86, 87, 88, 89* - Updated packing information