# 5V Capable Low-Voltage DPDT Analog Switch

## General Description

RT9737 is a 5V high quality low-voltage double-pole double-throw (DPDT) analog switch. RT9737 supply voltage is designed to operate from 2.5V to 5.5V. Supply voltage can be smaller than input voltage while keeping 5V input range. With 70mΩ turn-on resistance, power-loss and signal distortion can be minimized. RT9737 is ideal for switching audio signal from outputs of audio amplifiers. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another for audio applications.

## Features

- **Maximum Input Signal Range 0 to 5.5V**
- **70mΩ Turn-On Resistance**
- **2.5V to 5.5V Supply Voltage**
- **40μA Quiescent Current**
- **Break-Before-Make Between Channel Transition**
- **Available in 9Ball WL-CSP Package**

## Applications

- Smartphone
- Tablet

## Pin Configurations

(TOP VIEW)
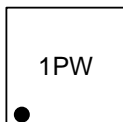


WL-CSP-9B 1.24x1.24 (BSC)

## Ordering Information

RT9737☐

Package Type
WSC : WL-CSP-9B 1.24x1.24 (BSC)

Note :

Richtek products are :

▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
▶ Suitable for use in SnPb or Pb-free soldering processes

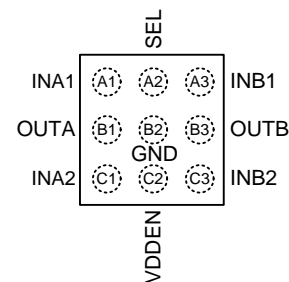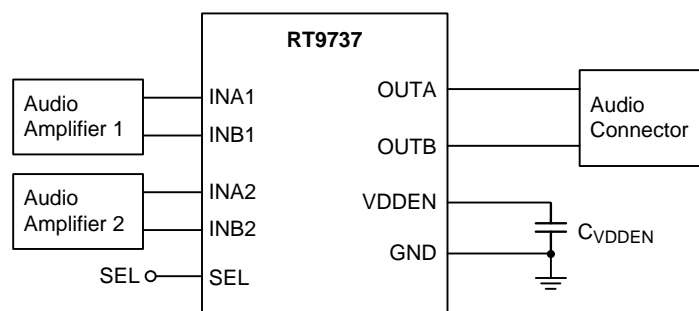## Marking Information



1P : Product Code

W : Date Code

## Simplified Application Circuit



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# RT9737

**RICHTEK**

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| A1 | INA1 | Input 1 of Channel A. |
| A2 | SEL | Selection for Input 1or 2. |
| A3 | INB1 | Input 1 of Channel B. |
| B1 | OUTA | Output of Channel A. |
| B2 | GND | Ground. |
| B3 | OUTB | Output of Channel B. |
| C1 | INA2 | Input 2 of Channel A. |
| C2 | VDDEN | Supply Voltage. |
| C3 | INB2 | Input 2 of Channel B. |

## Function Block Diagram
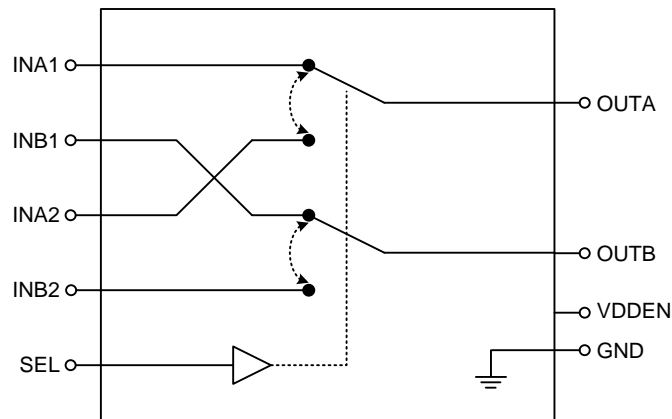


## Operation

The switches are fully specified to operate from a single 2.5V to 5.5V power supply. RT9737 via internal design, be able to handle when the input signal is greater than the supply voltage range and don't cause the signal distortion. RT9737 control the switches with a control pin, SEL. When SEL voltage under low level, internal switch is thrown to position 1. Audio signal are via INA1 and INB1 to IC OUTA and OUTB. And then OUTA, OUTB output to the load and Audio connector. When SEL voltage above high level, internal switch is thrown to position 2. When the supply voltage VDDEN under operation range, the switches impedance are risen and all analog signal ports can keep out signals from 0V to 5.5V.

## Absolute Maximum Ratings    (Note 1)

- VDDEN, INA1, INA2, INB1, INB2, OUTA, OUTB, SEL-------------------------------------------- −0.3 to 6V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C

  WL-CSP-9B 1.24x1.24 (BSC)-------------------------------------------------------------------------- 1.28W
- Package Thermal Resistance    (Note 2)

  WL-CSP-9B 1.24x1.24 (BSC), $\theta_{JA}$ ------------------------------------------------------------- 78.1°C/W
- Lead Temperature (Soldering, 10 sec.) ------------------------------------------------------------- 260°C
- Junction Temperature -------------------------------------------------------------------------------- 150°C
- Storage Temperature Range -------------------------------------------------------------------- −65°C to 150°C
- ESD Susceptibility    (Note 3)

  HBM (Human Body Model) ------------------------------------------------------------------------- 2kV

  MM (Machine Model)-------------------------------------------------------------------------------- 200V

## Recommended Operating Conditions    (Note 4)

- Supply Input Voltage, VDDEN------------------------------------------------------------------------- 2.5V to 5.5V
- Junction Temperature Range--------------------------------------------------------------------------- −40°C to 125°C
- Ambient Temperature Range--------------------------------------------------------------------------- −40°C to 85°C

## Electrical Characteristics

($V_{VDDEN}$ = 2.5V, $C_{VDDEN}$ = 0.1μF, $T_A$= 25°C, for each LDO unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Power Supply Range | $V_{DDEN}$ | | 2.5 | -- | 5.5 | V |
| Power Supply Rejection Ratio | PSRR | Vp-p = 200mV, f = 20kHz, $R_L$ = 32Ω    (Note 5) | -- | 80 | -- | dB |
| Quiescent Current | $I_Q$ | VDDEN = 2.5V to 5.5V | -- | 40 | 60 | μA |
| **Analog Switch** | | | | | | |
| Input Signal Range | | | 0 | -- | 5.5 | V |
| Turn-On Resistance | $R_{DS(ON)}$ | VDDEN = 2.5V, OUT = 0V, $I_{OUT}$ =100mA | -- | 90 | 125 | mΩ |
| | | VDDEN = 3.6V, OUT = 0V, $I_{OUT}$= 100mA | -- | 70 | 100 | mΩ |
| Off-State Leakage Current | | INA, INB, OUTA, OUTB, VDDEN = 5.5V | -- | 1.2 | 1.5 | μA |
| | | INA, INB, OUTA, OUTB = 5.5V, VDDEN = 0V | | 0.12 | 0.2 | μA |
| Turn-On Time | $t_{ON}$ | INA, INB = 0V | -- | 5 | 10 | ms |
| Turn-Off Time | $t_{OFF}$ | INA, INB = 0V    (Note 5) | -- | -- | 100 | μs |
| Break-Before-Make Time | $t_{BBM}$ | INA, INB = 0V | -- | 5 | 10 | ms |
| Off-Isolation    (Note 5) | | VDDEN = 0V, $R_L$ = 50Ω, INA/INB = 0.5Vpp, 20kHz | -- | −50 | -- | dB |
| Crosstalk    (Note 5) | | $R_L$ = 50Ω, INA/INB = 0.5Vpp, 20kHz | -- | −80 | -- | dB |
| THD+N    (Note 5) | | $R_L$ = 50Ω, INA/INB = 0.5Vpp, 1kHz, DC bias = 0.25V | -- | 0.001 | -- | % |
| -3dB Bandwidth    (Note 5) | | $R_L$ = 50Ω | -- | 2 | -- | MHz |
| INA/INB Capacitance | | INA /INB = 0.5$V_{P-P}$, f = 1MHz (Note 5) | -- | 70 | -- | pF |
| OUTA/OUTB Capacitance | | INA /INB = 0.5$V_{P-P}$, f = 1MHz (Note 5) | -- | 120 | -- | pF |

# RT9737

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital I/O** | | | | | | |
| Input Logic-Hi Threshold | $V_{IH}$ | | 1.4 | -- | -- | V |
| Input Logic-Low Threshold | $V_{IL}$ | | -- | -- | 0.4 | V |
| Input Leakage Current | | SEL = 0V or VDDEN | −0.1 | -- | 0.1 | μA |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Guarantee by design.

## Typical Application Circuit
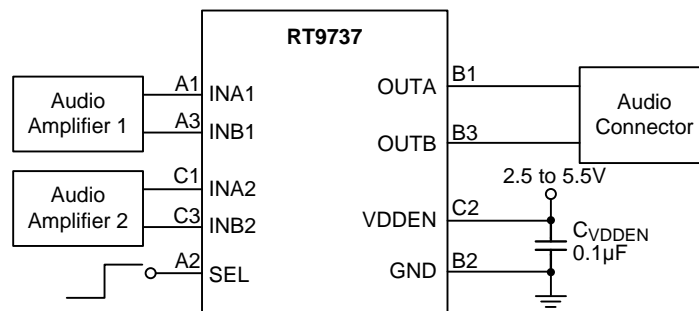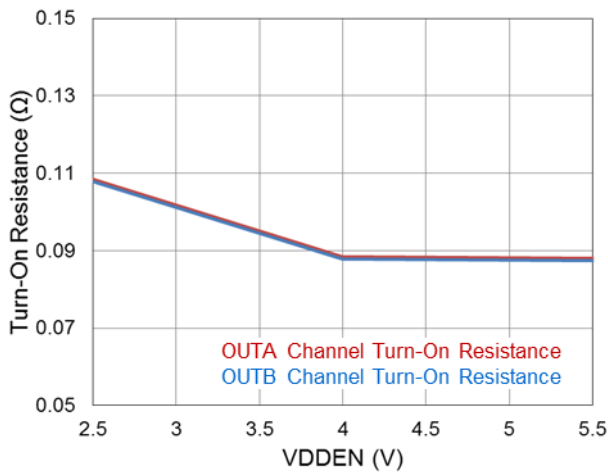
## Typical Operating Characteristics

**Quiescent Current vs. VDDEN**
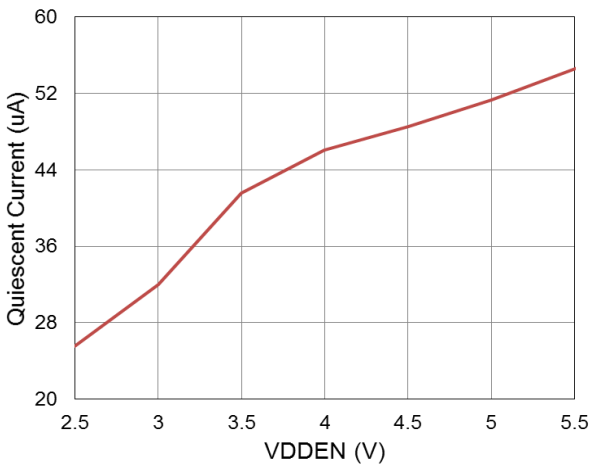


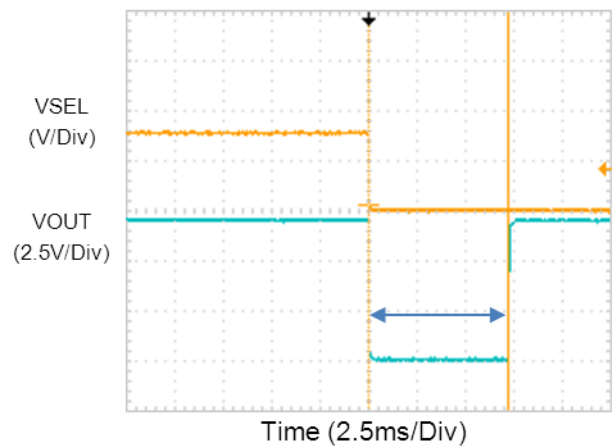**SEL Leakage Current vs. V<sub>SEL</sub>**
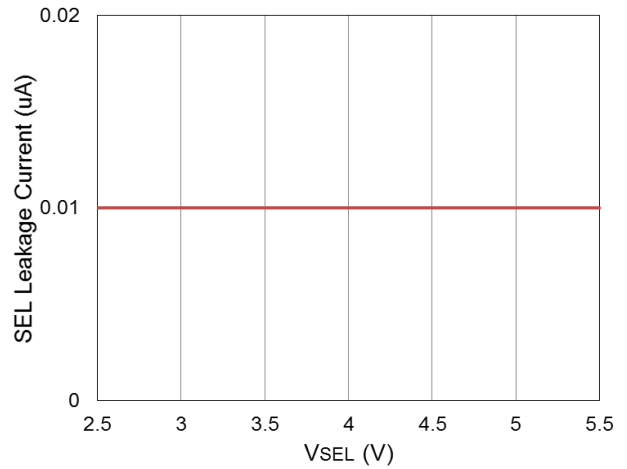


**Turn-On Resistance vs. VDDEN**



OUTA Channel Turn-On Resistance
OUTB Channel Turn-On Resistance

**t<sub>BBM</sub> V<sub>SEL</sub> High to Low**



**t<sub>BBM</sub> V<sub>SEL</sub> Low to High**
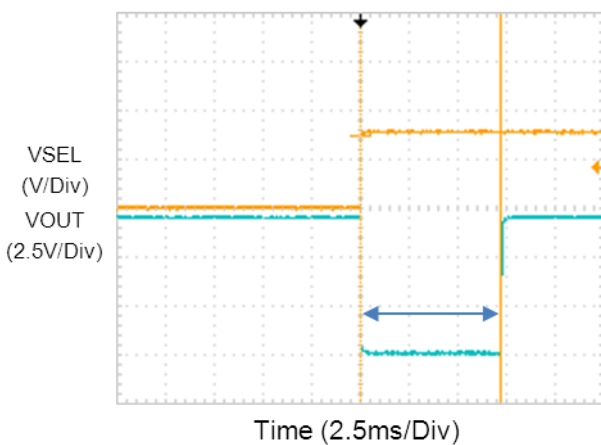


**Cross talk vs. Frequency**



VDDEN= 2.5V
VDDEN=3.6V
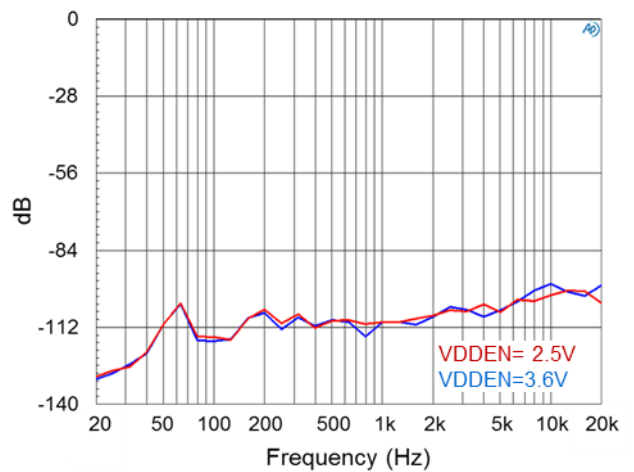
## Application Information

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### Analog Input

RT9737 internal topology design for input and output voltage level can greater than supply voltage.

Low turn-on resistance and excellent channel to channel matching are ideal for audio applications.

### Switch Logic Control

RT9737 can use SEL pin to control internal switches position for another audio source application. SEL pin input current is very low.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For WL-CSP-9B 1.24x1.24 (BSC) packages, the thermal resistance, $\theta_{JA}$, is 78.1°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$$P_{D(MAX)} = (125°C - 25°C) / (78.1°C/W) = 1.28W \text{ for}$$

WL-CSP-9B 1.24x1.24 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.



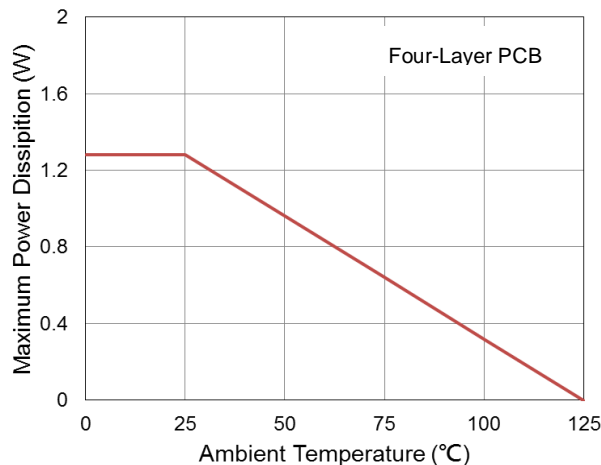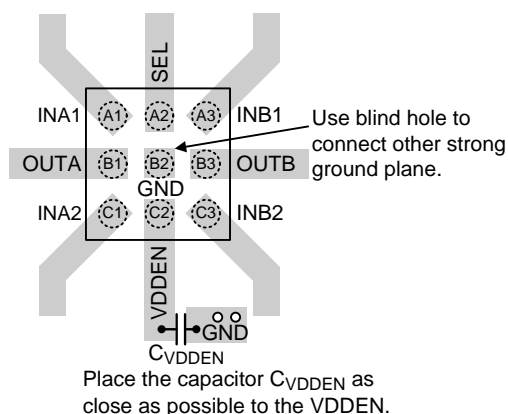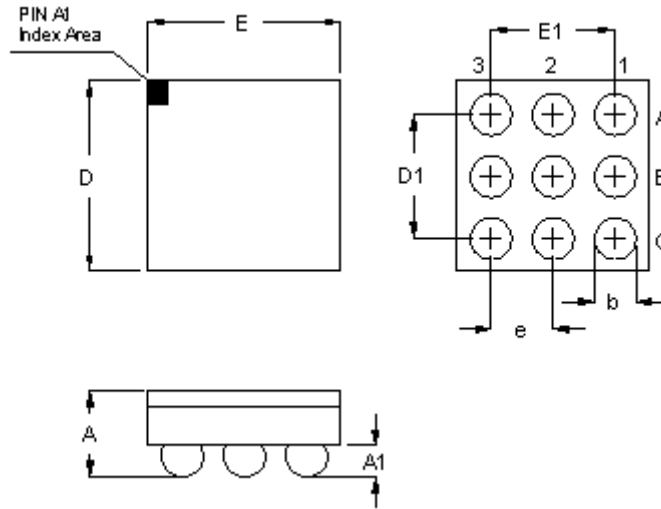Figure 1. Derating Curve of Maximum Power Dissipation



Figure 2. PCB Layout Guide

## Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|:---:|:---:|:---:|:---:|:---:|
| | Min. | Max. | Min. | Max. |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.170 | 0.230 | 0.007 | 0.009 |
| b | 0.240 | 0.300 | 0.009 | 0.012 |
| D | 1.190 | 1.290 | 0.047 | 0.051 |
| D1 | 0.800 | | 0.031 | |
| E | 1.190 | 1.290 | 0.047 | 0.051 |
| E1 | 0.800 | | 0.031 | |
| e | 0.400 | | 0.016 | |

**WL-CSP-9B 1.24x1.24 (BSC) Package**

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