RICHTEK®

RT9728A

120mΩ, 1.3A Power Switch with Programmable Current Limit

1 General Description

The RT9728A is a cost-effective, low-voltage, single P-MOSFET high-side power switch IC for USB applications with a programmable current limit feature. This IC features a low switch-on resistance (typically 120mΩ) and a low supply current (typically 120μA). The RT9728A offers a programmable current-limit threshold ranging from 75mA to 1.3A (typical) via an external resistor, With a ±10% current limit accuracy across all current limit settings. In addition, a flag output is available to indicate fault conditions to the local USB controller. Furthermore, the IC also integrates an embedded delay function to prevent mis-operation due to high inrush current. The RT9728A is an ideal solution for USB power supply and can support flexible applications since it is functional for various current limit requirements. It is available in SOT-23-6 and WDFN-6L 2x2 packages. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

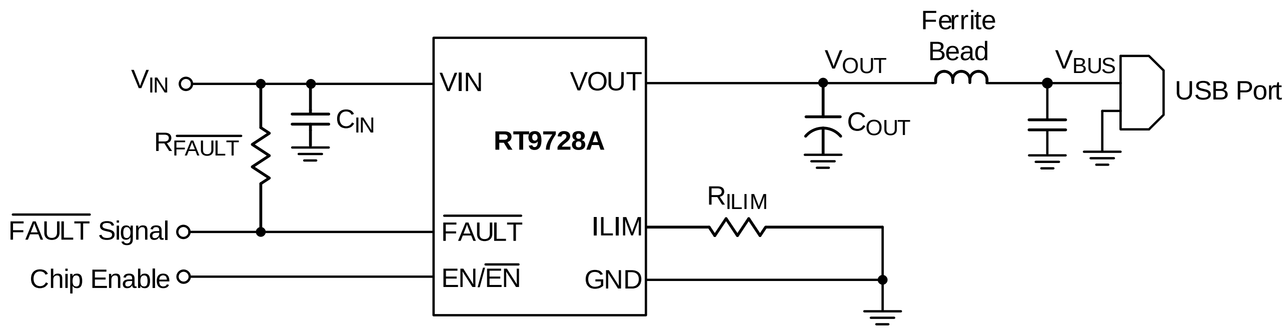
2 Features

- **±10% Current Limit Accuracy @ 1.3A**
- **Adjustable Current Limit: 75mA to 1.3A (Typical)**
- **Meet USB Current Limiting Requirements**
- **Operating Voltage Range: 2.5V to 5.5V**
- **Reverse Input-Output Voltage Protection**
- **Built-In Soft-Start**
- **120mΩ High-Side MOSFET**
- **120μA Supply Current**
- **15kV ESD Protection per IEC 61000-4-2 (With External Capacitance)**
- **Nemko Approved IEC62368-1**
- **UL Approved-E219878**

3 Applications

- USB Bus/Self-Powered Hubs
- USB Peripheral Ports
- ACPI Power Distribution
- Battery-Powered Equipment
- 3G/3.5G Data Cards and Set-Top Boxes

4 Simplified Application Circuit



5 Ordering Information

RT9728A □□□

Package Type(1)
E: SOT-23-6
QW: WDFN-6L 2x2

Lead Plating System
G: Richtek Green Policy Compliant(2)
Z: ECO (Ecological Element with Halogen Free and Pb free) (for WDFN-6L 2x2 Only)

H: Chip Enable High
L: Chip Enable Low

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information

RT9728AHGE

01=DNN

01= : Product Code
DNN : Date Code

RT9728ALGE

02=DNN

02= : Product Code
DNN : Date Code

RT9728AHGQW

17W

17 : Product Code
W : Date Code

RT9728ALGQW

19W

19 : Product Code
W : Date Code

RT9728AHZQW

17W

17 : Product Code
W : Date Code

RT9728ALZQW

19W

19 : Product Code
W : Date Code

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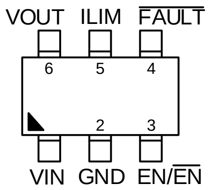
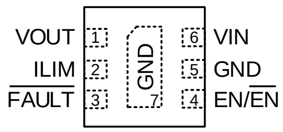
7 Pin Configuration

(TOP VIEW)



SOT-23-6

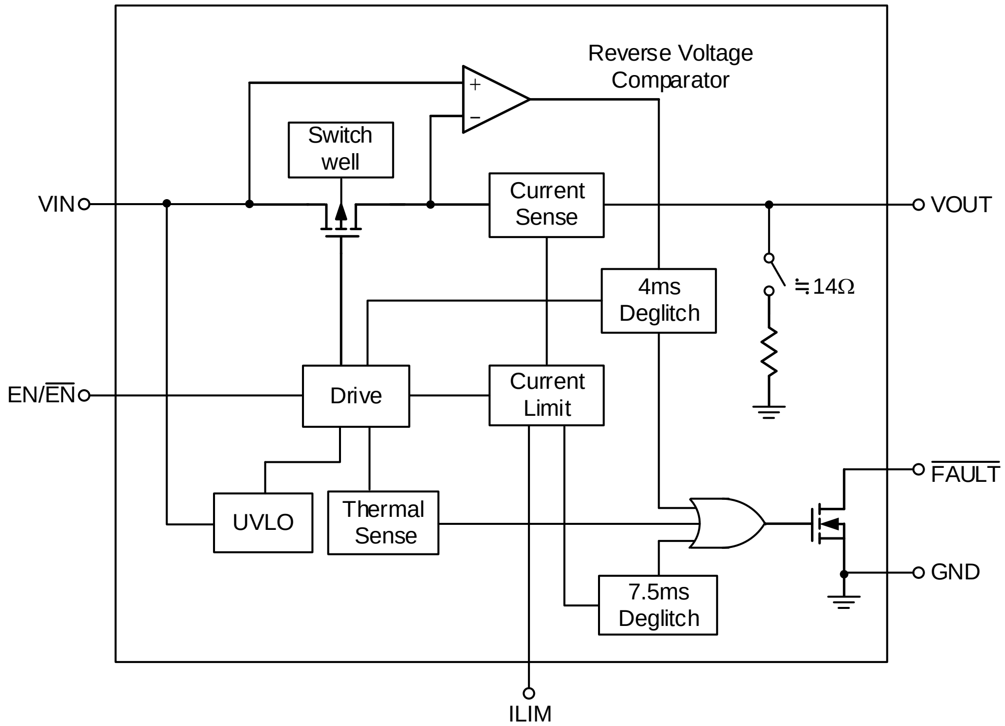


WDFN-6L 2x2

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
SOT-23-6	WDFN-6L 2x2		
1	6	VIN	Power input. The input voltage range is from 2.5V to 5.5V. Connect a suitable input capacitor between this pin and GND; typically, a 10μF capacitor is used.
2	5, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	4	EN/$\overline{\text{EN}}$	Enable Control Pin with Internal Pull-Up Current Source (EN): Leaving the pin floating or applying a logic-high voltage (≥ 1.1V, typical) will enable the converter. Applying a logic-low voltage will force the device into shutdown mode. Connecting the EN pin to ground will force the converter into shutdown state, which is particularly relevant for cases where the enable pin is marked as /EN (active-low).
4	3	$\overline{\text{FAULT}}$	Active-Low Open-Drain Output: This output is asserted during overcurrent, over-temperature, or reverse-voltage conditions. It is recommended to connect a 100kΩ resistor to VIN.
5	2	ILIM	Current limit set pin. An external resistor sets the current-limit threshold, with a recommended range of 19.1kΩ to 232kΩ.
6	1	VOUT	Power switch output pins. A ceramic capacitor of 10μF is required for stability. The output capacitor should be placed as close to the device as possible, and the impedance between the VOUT pin and the load should be minimized.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage -- –0.3V to 6V
- Other Pin Voltage -- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  SOT-23-6 -- 0.4W

  WDFN-6L 2x2 -- 0.606W
- Package Thermal Resistance (Note 3)

  SOT-23-6, θ_{JA} -- 250°C/W

  WDFN-6L 2x2, θ_{JA} -- 165°C/W

  WDFN-6L 2x2, θ_{JC} -- 7°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range -- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

11 ESD Ratings

(Note 4)

- HBM (Human Body Model) --2kV

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN -- 2.5V to 5.5V
- Junction Temperature Range -- –40°C to 125°C
- Ambient Temperature Range -- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

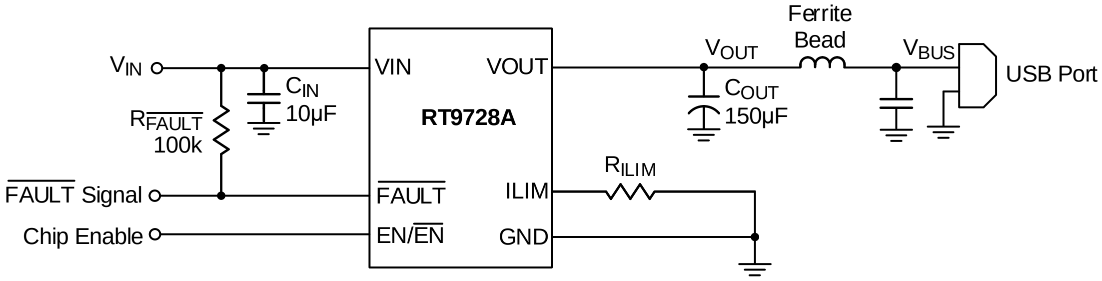
13 Electrical Characteristics

(V_{IN} = 3.6V, 19.1kΩ ≤ R_{ILIM} ≤ 232kΩ, T_A = T_J = 25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
EN Input Voltage Rising Threshold	V_{EN_R}			1.1	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}			--	--	0.66	V
Current-limit threshold Resistor Range	R_{ILIM}	(nominal 1%) from ILIM to GND		19.1	--	232	kΩ
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}			--	2.3	--	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}			--	2.1	--	V
Shutdown Current	I_{SHDN}	V_{IN} = 5.5V, no load on V_{OUT}, V_{EN} = 0V		--	1	3	μA
Quiescent Current	I_Q	V_{IN} = 5.5V, no load on V_{OUT}	R_{ILIM} = 20kΩ	--	120	170	μA
			R_{ILIM} = 210kΩ	--	120	170	
Reverse Leakage Current	I_{REV}	V_{OUT} = 5.5V, V_{IN} = 0V		--	1	3	μA
Static Drain-Source On-State Resistance	R_{DS}	I_{SW} = 0.2A		--	120	--	mΩ
Current Limit	I_{LIM}	R_{ILIM} = 20kΩ		1190	1295	1400	mA
		R_{ILIM} = 49.9kΩ		468	520	572	
		R_{ILIM} = 210kΩ		110	130	150	
		ILIM shorted to VIN		50	75	100	
Reverse Voltage Comparator Trip Point (V_{OUT} – V_{IN})				--	135	--	mV
$\overline{\text{FAULT}}$ Output Low Voltage	V_{OL}	$\overline{\text{FAULT}}$ = 1mA		--	180	--	mV
$\overline{\text{FAULT}}$ Off State Leakage		V_{FAULT} = 5.5V		--	1	--	μA
$\overline{\text{FAULT}}$ Deglitch		$\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition		5	7.5	10	ms
		$\overline{\text{FAULT}}$ assertion or de-assertion due to reverse voltage condition		2	4	6	
$\overline{\text{FAULT}}$ Flag Assertion Offset	$V_{\overline{FAULT}\_OFS}$	Offset between fault flag assertion level versus ILIM trigger level (Note 6)		–100	--	0	mA
Over-Temperature Protection Threshold	T_{OTP}	(Note 6)		--	160	--	°C

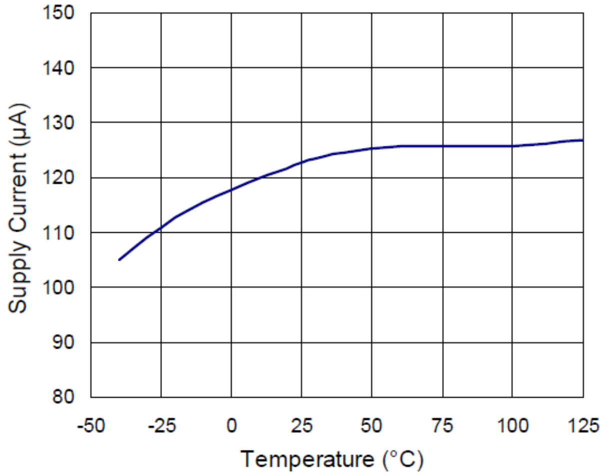
Note 6. Guarantee by design.

14 Typical Application Circuit

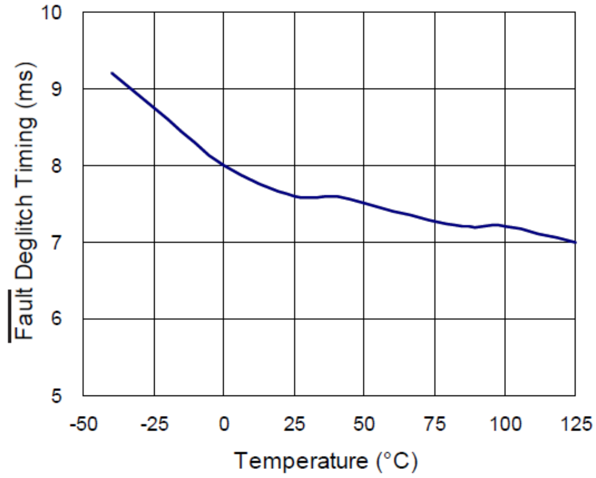


15 Typical Operating Characteristics

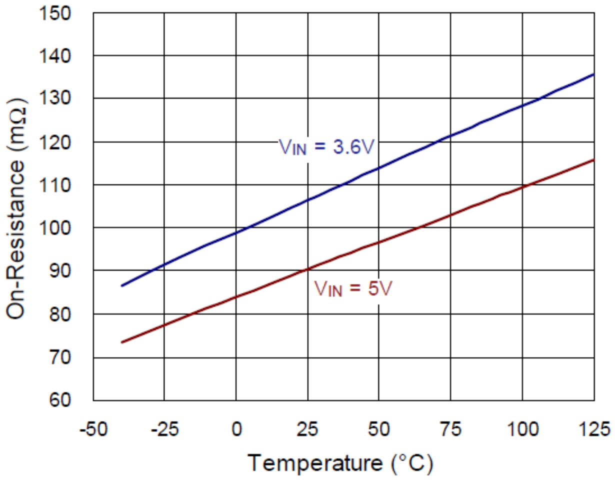
Supply Current vs. Temperature



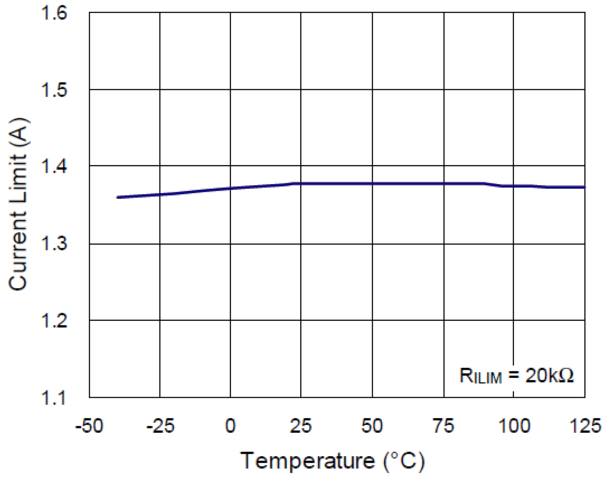
$\overline{\text{Fault}}$ Deglitch Timing vs. Temperature



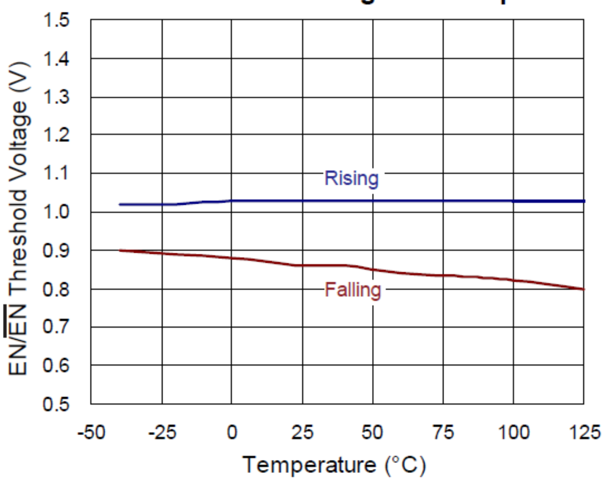
On- Resistance vs. Temperature



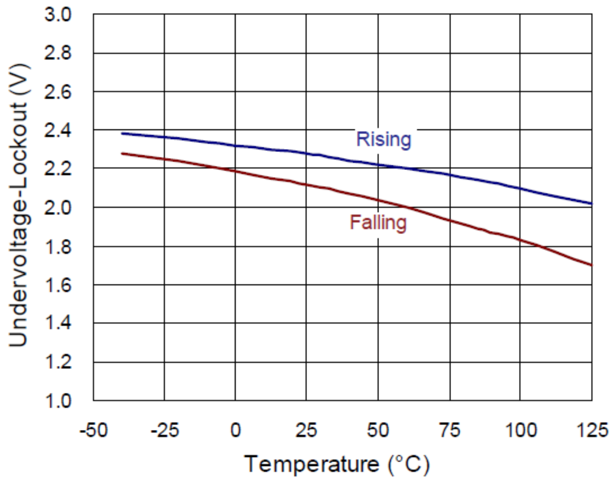
Current Limit vs. Temperature



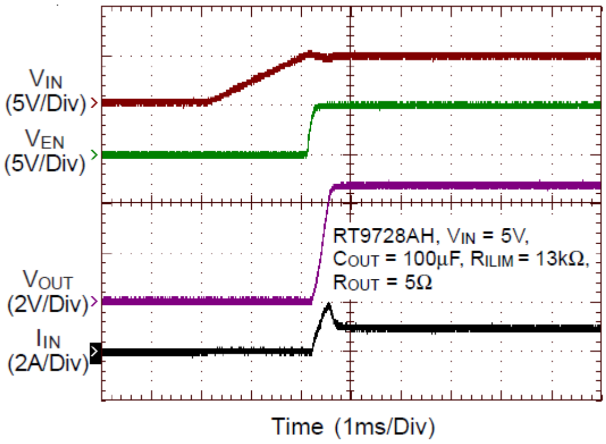
EN/$\overline{\text{EN}}$ Threshold Voltage vs. Temperature



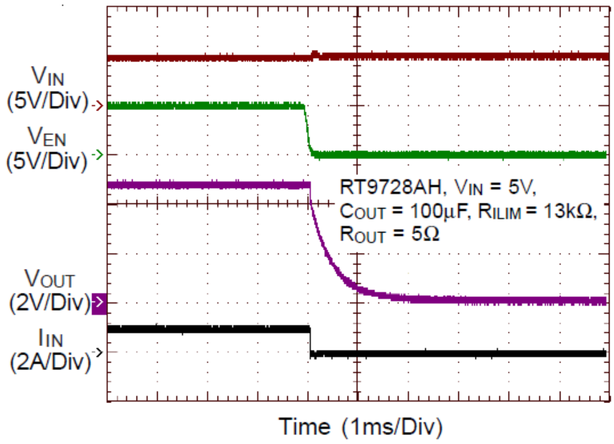
Undervoltage-Lockout vs. Temperature



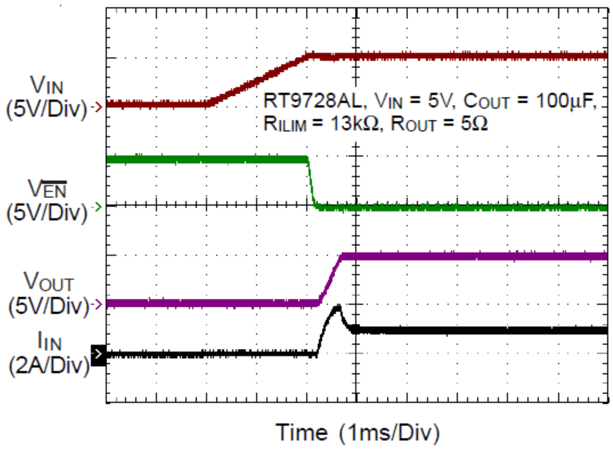
Power On from EN



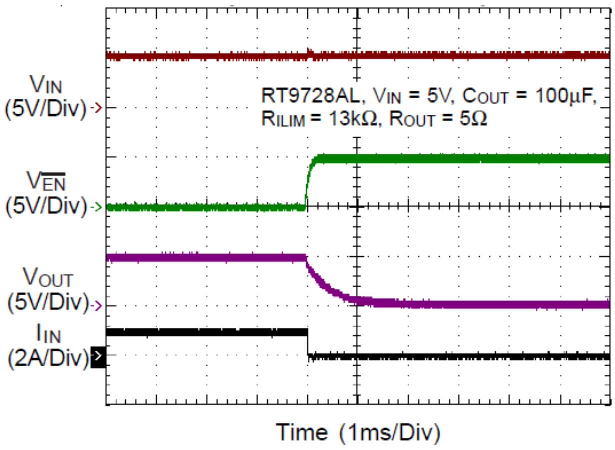
Power Off from EN



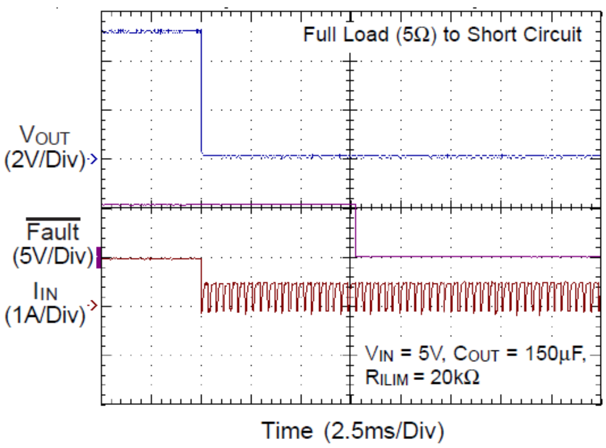
Power On from $\overline{EN}$



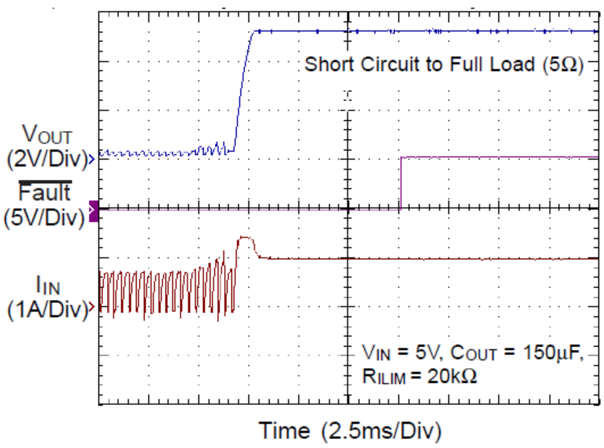
Power Off from $\overline{EN}$

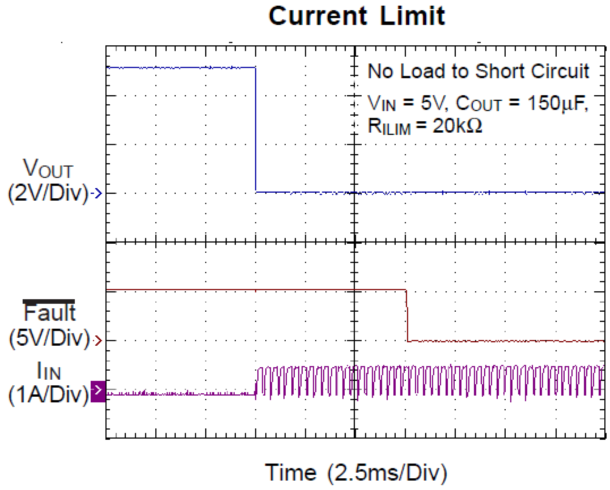


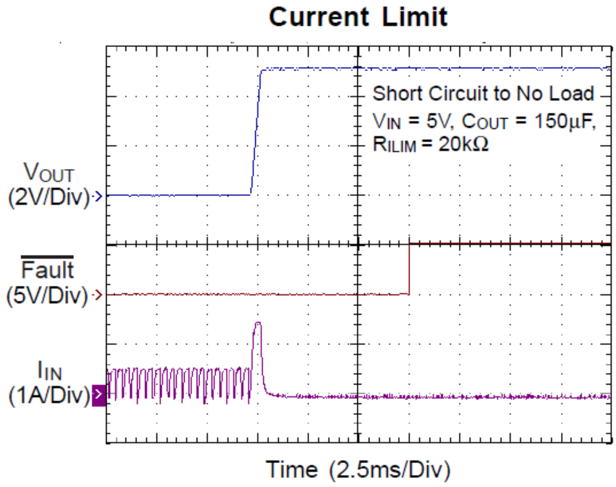
Current Limit

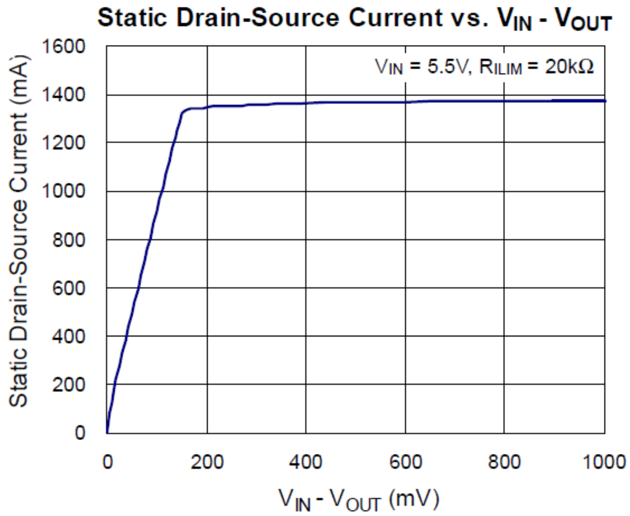


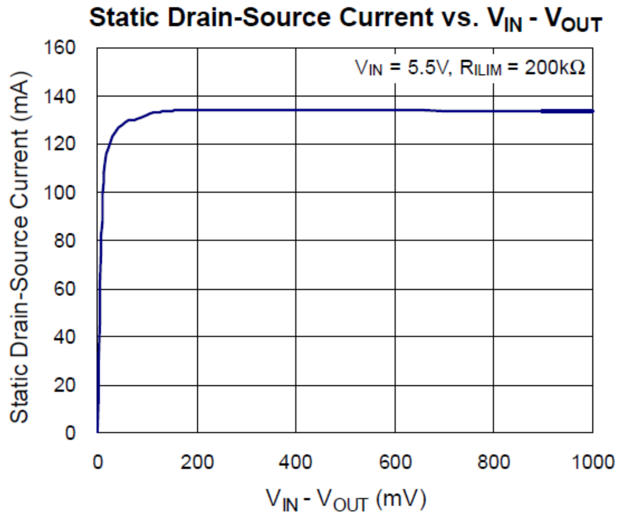
Current Limit




Current Limit
No Load to Short Circuit
VIN = 5V, COUT = 150μF, RILIM = 20kΩ
VOUT (2V/Div)
Fault (5V/Div)
IIN (1A/Div)
Time (2.5ms/Div)


Current Limit
Short Circuit to No Load
VIN = 5V, COUT = 150μF, RILIM = 20kΩ
VOUT (2V/Div)
Fault (5V/Div)
IIN (1A/Div)
Time (2.5ms/Div)


Static Drain-Source Current vs. VIN - VOUT
VIN = 5.5V, RILIM = 20kΩ
Static Drain-Source Current (mA)
1600
1400
1200
1000
800
600
400
200
0
0
200
400
600
800
1000
VIN - VOUT (mV)


Static Drain-Source Current vs. VIN - VOUT
VIN = 5.5V, RILIM = 200kΩ
Static Drain-Source Current (mA)
160
140
120
100
80
60
40
20
0
0
200
400
600
800
1000
VIN - VOUT (mV)

16 Operation

The RT9728A is a current-limited power switch that employs a P-MOSFET for applications prone to short circuits or heavy capacitive loads. Users can adjust the current-limit threshold from 75mA to 1.3A (typical) using an external resistor. Additional shutdown features of the device include over-temperature protection and reverse-voltage protection.

The RT9728A provides a built-in soft-start function to control the gate voltage of the power switch gradually. This driver possesses advanced circuitry designed to regulate the rise and fall times of the output voltage, thereby limiting large inrush currents and voltage spikes. The RT9728A enters a constant-current mode whenever the load exceeds the preset current-limit threshold.

17 Application Information

(Note 7)

The RT9728A is a single P-MOSFET high-side power switch featuring an active-high/low enable input, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. The switch's low $R_{DS(ON)}$ meets USB voltage drop requirements, and a flag output is provided to signal fault conditions to the local USB controller.

17.1 Current Limiting and Short-Circuit Protection

When a heavy load or short-circuit situation occurs while the switch is enabled, a large transient current may flow through the device. The RT9728A includes current-limit circuitry to prevent these large currents from damaging the MOSFET switch and the hub downstream ports. The RT9728A provides an adjustable current-limit threshold between 120mA and 1.3A (typical) via an external resistor, R_{ILIM}, ranging from 19.1kΩ to 232kΩ. However, if the ILIM pin is connected to VIN, the current-limit threshold will be 75mA (typical). The maximum −100mA fault flag assertion offset needs caution, especially for very low ILIM applications. For example, with ILIM = 250mA, the minimum fault flag assertion level might be 150mA (40% error versus its target). For the condition where I_{LIM} is shorted to V_{IN} (75mA), the fault flag may go low. Once the current-limit threshold is exceeded, the device enters constant-current mode until either over-temperature protection occurs or the fault is removed. Table 1 shows a recommended current limit value vs. R_{ILIM} resistor.

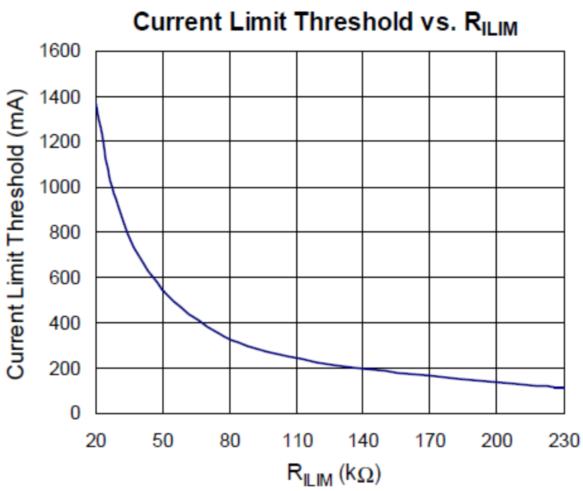


Figure 1. Current-Limit Threshold vs R_{ILIM}

Table 1. Recommended R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)	Ideal Resistor (kΩ)	Closet 1% Resistor (kΩ)	Actual Limits (Include R Tolerance)		
			IOS Min (mA)	IOS Nom (mA)	IOS Max (mA)
75	ILIM is shorted to VIN		50.0	75.0	100.0
120	226.1	226.0	101.3	120.0	142.1
200	134.0	133.0	173.7	201.5	233.9
300	88.5	88.7	262.1	299.4	342.3
400	65.9	66.5	351.1	396.7	448.7
500	52.5	52.3	443.9	501.6	562.4
600	43.5	43.2	535.1	604.6	674.1
700	37.2	37.4	616.0	696.0	776.0
800	32.4	32.4	708.7	800.8	892.9
900	28.7	28.7	797.8	901.5	1005.2
1000	25.8	26.1	875.4	989.1	1102.8
1100	23.4	23.2	982.1	1109.7	1237.3
1200	21.4	21.5	1057.9	1195.4	1332.9
1300	19.7	19.6	1178.0	1308.5	1439.0

17.2 Fault Flag

The RT9728A provides a $\overline{\text{FAULT}}$ signal pin, which is an N-channel open-drain MOSFET output. This open-drain output goes low when the current exceeds the current-limit threshold, VOUT − VIN exceeds the reverse voltage trip level, or the die temperature exceeds approximately 160°C. The $\overline{\text{FAULT}}$ output is capable of sinking a 1mA load to typically 180mV above ground. The $\overline{\text{FAULT}}$ pin requires a pull-up resistor; this resistor should be large in value to reduce energy drain. A 100kΩ pull-up resistor works well for most applications. In the case of an overcurrent condition, $\overline{\text{FAULT}}$ will be asserted only after the flag response delay time, t_D, has elapsed. This ensures that FAULT is asserted upon valid overcurrent conditions and that erroneous error reporting is eliminated. For example, false overcurrent conditions may occur during hot-plug events when extremely large capacitive loads are connected, which induces a high transient inrush current that exceeds the current-limit threshold. The $\overline{\text{FAULT}}$ response delay time, t_D, is typically 7.5ms.

17.3 Supply Filter/Bypass Capacitor:

A 10μF low ESR ceramic capacitor connected from VIN to GND and located close to the device is strongly recommended to prevent input voltage drooping during hot plug events. However, higher capacitor values may be used to further reduce the voltage droop on the input. Without this bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. Note that the input transient voltage must never exceed 6V as stated in the Absolute Maximum Ratings.

17.4 Output Filter Capacitor

Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused by hot-insertion transients in downstream cables. Ferrite beads in series with VBUS, the ground line, and the bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies. For commercial applications where the ambient temperature is 0°C to 70°C (such as a PC or USB hub), the RT9728A supports an output capacitor range of up to 120μF. For industrial applications with an ambient temperature of −40°C to 125°C, limit the output capacitance to less than 50μF to ensure normal startup.

17.5 Chip Enable Input

The RT9728A will be disabled when the $EN/\overline{EN}$ pin is in a logic-low or logic-high condition. During this condition, the internal circuitry and MOSFET are turned off, reducing the supply current to 1μA (typical). Floating the input may cause unpredictable operation, and the $EN/\overline{EN}$ should not be allowed to go negative with respect to GND. The $EN/\overline{EN}$ signal must be asserted after the input voltage is ready or higher than the UVLO threshold to satisfy the power sequence.

17.6 Undervoltage-Lockout

The undervoltage-lockout (UVLO) feature prevents the MOSFET switch from turning on until the input voltage exceeds approximately 2.3V (typical). If the input voltage drops below approximately 2.1V (typical), the UVLO circuit will turn off the MOSFET switch.

17.7 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For SOT-23-6 packages, the thermal resistance, θ_{JA}, is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board. For WDFN-6L 2x2 packages, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C − 25°C) / (250°C/W) = 0.400W for a SOT-23-6 package.

$P_{D(MAX)}$ = (125°C − 25°C) / (165°C/W) = 0.606W for a WDFN-6L 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

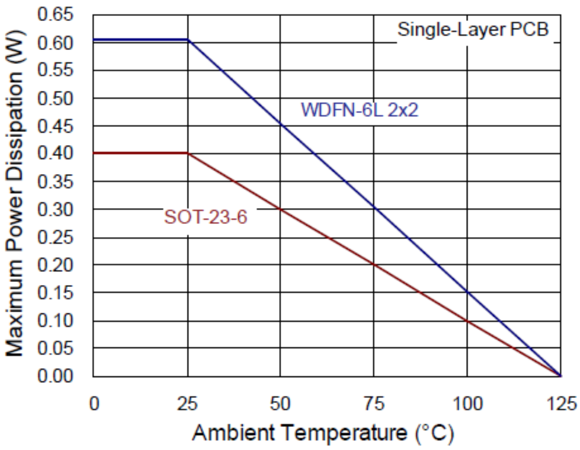
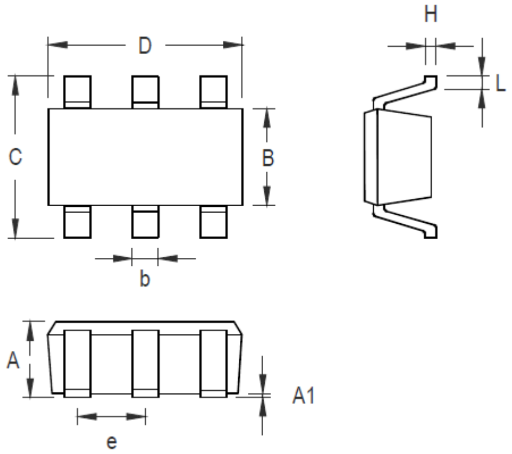


Figure 2. Derating Curves of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

18 Outline Dimension

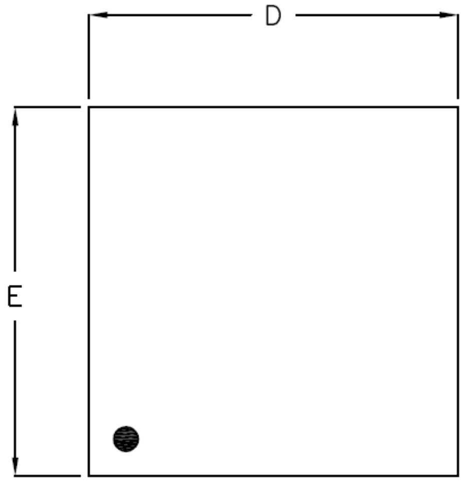
18.1 SOT-23-6 Package

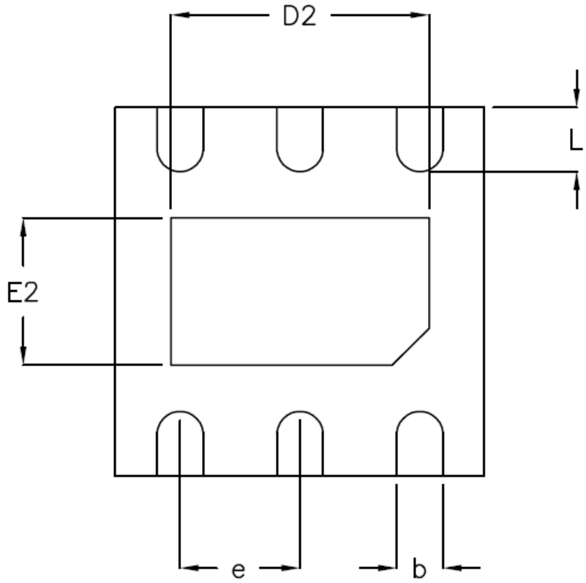


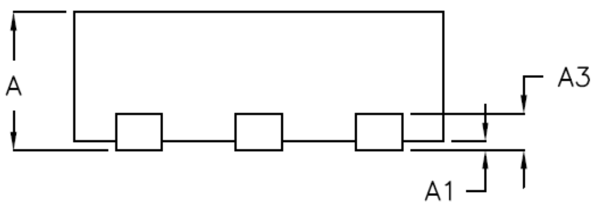
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

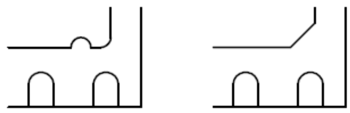
SOT-23-6 Surface Mount Package

18.2 WDFN-6L 2x2 Package









DETAILA
Pin #1 ID and Tie Bar Mark Options

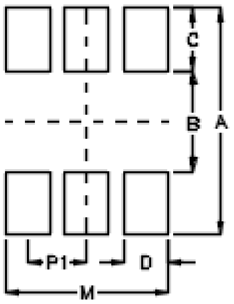
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

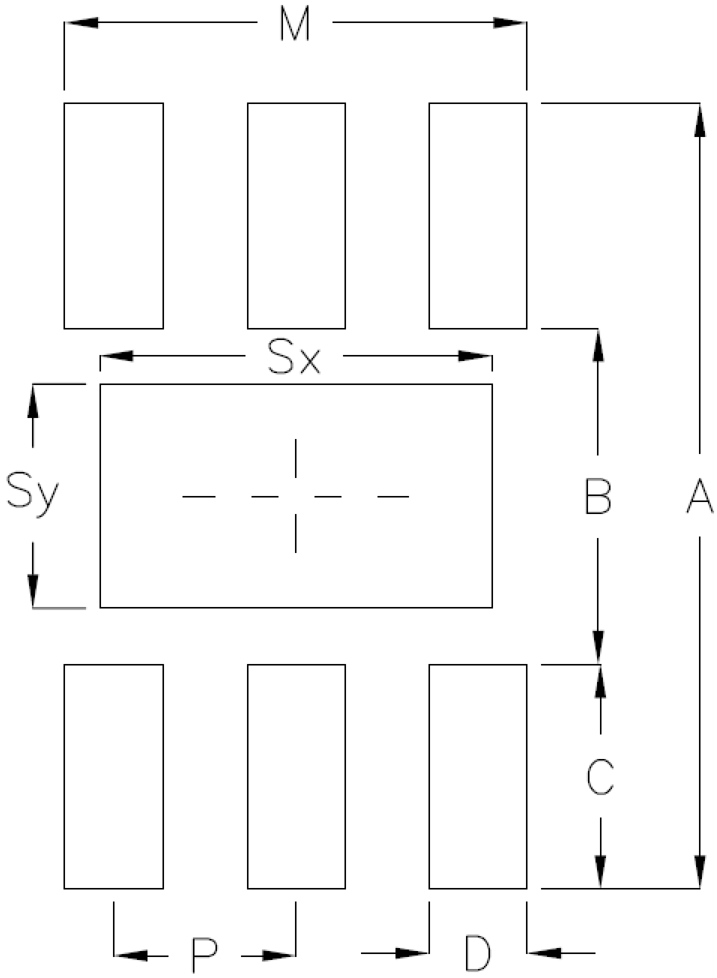
19 Footprint Information

19.1 SOT-23-6 Package



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

19.2 WDFN-6L 2x2 Package



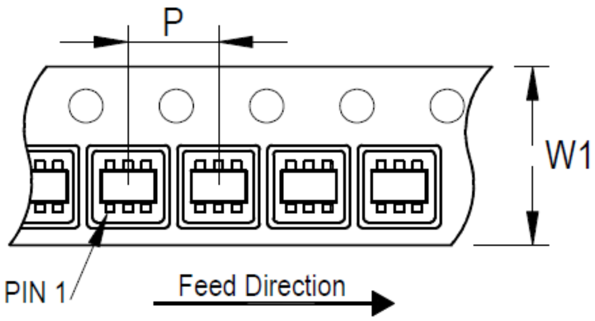
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-6	6	0.65	2.80	1.20	0.80	0.35	1.40	0.80	1.65	±0.05

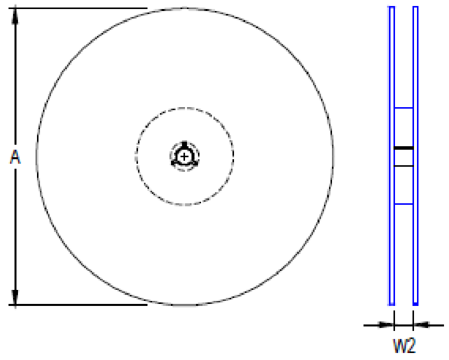
20 Packing Information

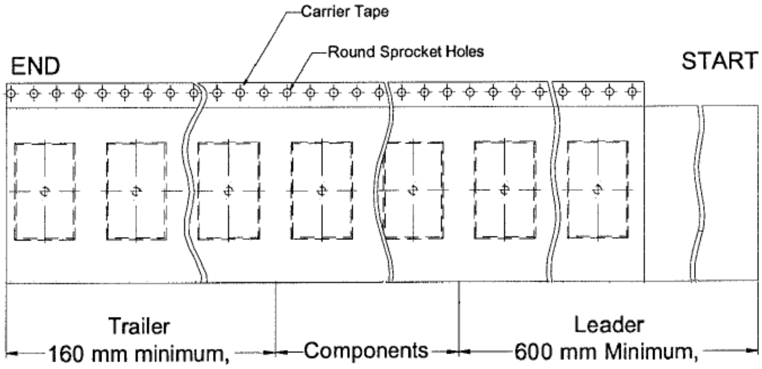
20.1 Tape and Reel Data

20.1.1 SOT-23-6

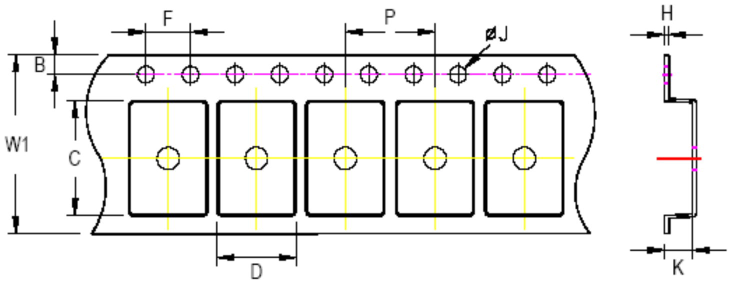
SOT/TSOT-23-6/8:







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-23-6	8	4	180	7	3,000	160	600	8.4/9.9

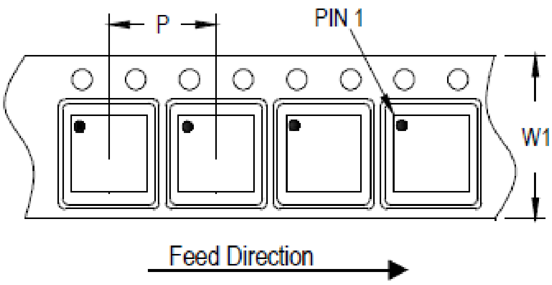


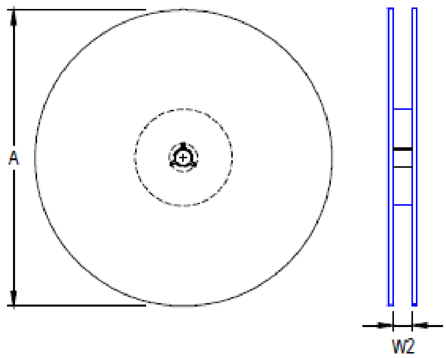
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

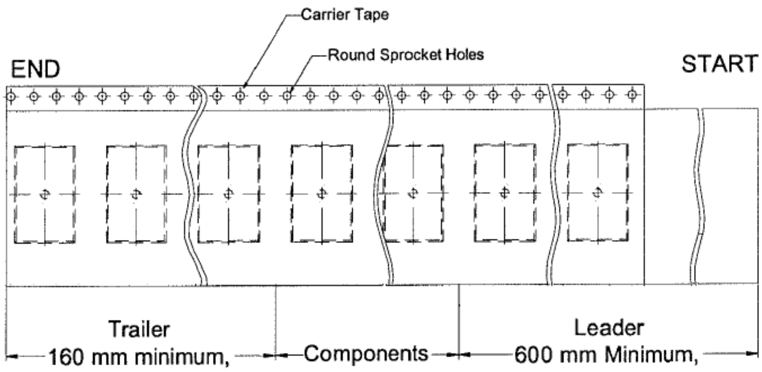
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.3mm	1.7mm	0.6mm

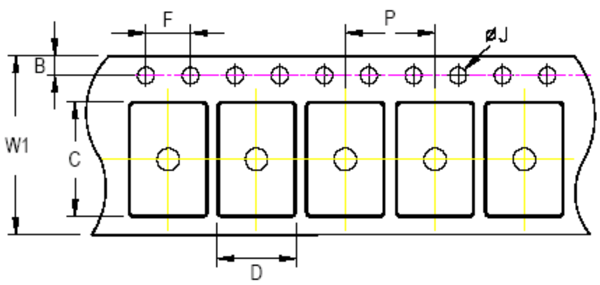
20.1.2 WDFN-6L 2x2

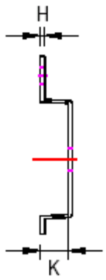






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leade r(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

20.2.1 SOT-23-6

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-23-6	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

20.2.2 WDFN-6L 2x2

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

21 Datasheet Revision History

Version	Date	Description	Item
12	2024/10/6	Modify	*General Description on page 1* *Features on page 1* *Simplified Application Circuit on page 1* *Functional Pin Description on page 4* *Functional Block Diagram on page 5* *Electrical Characteristics on page 7* *Operation on page 12* - Added Operation *Application Information on page 13, 14* *Footprint Information on page 19, 20* - Added Footprint Information *Packing Information on page 21 to 25* - Added packing information