Synchronous Buck Dr.MOS Power Stage

General Description

The RT9680A is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high-side MOSFET has low capacitance and gate charge for fast switching with low duty cycle operation. The low-side MOSFET has ultra low $R_{DS(ON)}$ to minimize conduction losses. A number of features are provided making the RT9680A a highly versatile power module. The boot strap diode is integrated in the driver. The low-side MOSFET can be driven into diode emulation mode to provide asynchronous operation to improve light load efficiency. The pin-out is optimized for low inductance routing of the RT9680A keeping the parasitics and their effects to the minimum.

The RT9680A is available in a UQFN-11HL 3x3 (FC) package.

Ordering Information

RT9680A □□

- Package Type
  QUF : UQFN-11HL 3x3 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

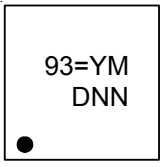
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT9680AGQUF



93= : Product Code

YMDNN : Date Code

Features

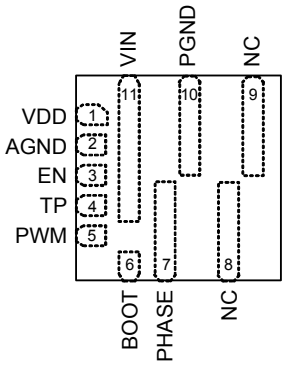
- **Up to 1MHz Operating Frequency**
- **For PWM 5V Logic**
- **Input Voltage Up to 23V**
- **Over-Temperature Protection**
- **Max Continue Current up to 8A**
- **Low Quiescent Current**
- **Tri-State PWM Input**
- **Integrated Bootstrap Diode**
- **High Density Package with UQFN-11HL 3x3 (FC)**

Applications

- Notebook
- Wireless Charger Solutions
- VCORE and DDR Solutions

Pin Configuration

(TOP VIEW)

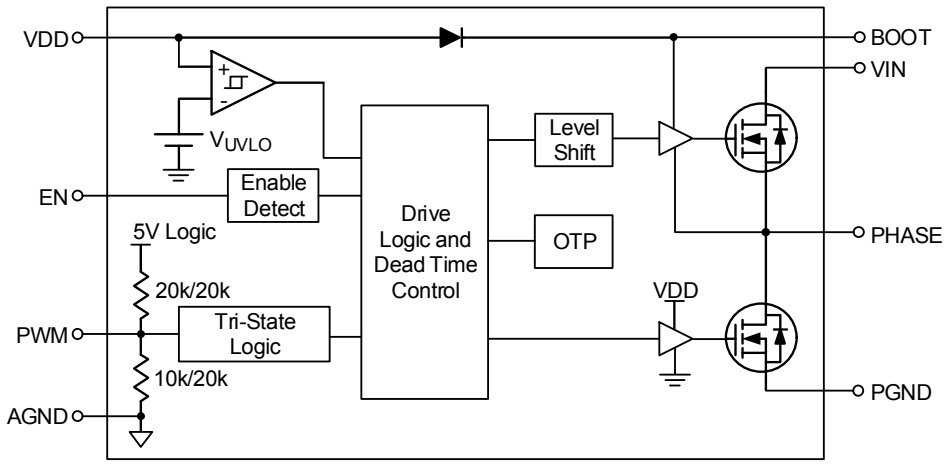


UQFN-11HL 3x3 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDD	Supply voltage to gate drivers and internal circuitry.
2	AGND	Analog ground.
3	EN	Enable control input. Pull this pin high to turn on the driver. Do not leave this pin floating.
4	TP	Connect this pin to AGND.
5	PWM	PWM signal input. Connect this pin to the PWM output of the controller.
6	BOOT	Bootstrap supply for high-side gate driver. A 0.1μF ceramic capacitor and a 10Ω R_{BOOT} are connected between this pin and PHASE pin.
7	PHASE	Voltage switching node – pin connection to the output inductor.
8, 9	NC	No internal connection.
10	PGND	Power ground.
11	VIN	Power input. Decouple this pin to AGND pin with an at least 10μF ceramic capacitor.

Functional Block Diagram



Operation

The RT9680A is a fully integrated driver and power MOSFET designed to work for gate drive and internal control circuits.

Under-Voltage Lockout

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage of V_{IN} is lower than the UVLO falling threshold voltage, the device will be lockout.

Enable Detect

The enable input (EN) has a logic-low level. When V_{EN} is below this level the IC enters shutdown mode. When V_{EN} exceeds its logic-high level the IC is fully operational.

Over-Temperature Protection (OTP)

The RT9680A includes an Over-Temperature Protection (OTP) circuitry to prevent overheating due to excessive power dissipation.

Tri-State Logic

The PWM signal is acted as "High" if the signal is above the rising threshold and acted as "Low" if the signal is below the falling threshold. When PWM signal level enters and remains within the shutdown window, the internal drivers are disabled and both internal MOSFET gates are pulled and held low.

Bootstrap Diode

The internal bootstrap diode and an external bootstrap capacitor and resister form a charge pump that supplies voltage to the BOOT pin.

Drive Logic and Dead Time control

The RT9680A has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned ON at the same time.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 27V
- Switch Voltage, PHASE to GND
  - DC ---------- –0.3V to (V_{IN} + 0.3V)
  - <30ns ---------- –5V to 28V
- Boot Voltage, BOOT ---------- (V_{SW} – 0.3V) to (V_{PHASE} + 6V)
- EN, PWM, TP to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  - UQFN-11HL 3x3 (FC) ---------- 1.29W
- Package Thermal Resistance (Note 2)
  - UQFN-11HL 3x3 (FC), θ_{JA} ---------- 77.3°C/W
  - UQFN-11HL 3x3 (FC), θ_{JC} ---------- 8.8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 23V
- Supply VDD Voltage ---------- 4.5V to 5.5V
- Switching Frequency Rang ---------- 300kHz to 1MHz
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, V_{DD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Supply Current						
Supply Current		5V Logic, EN = high, PWM = floating	--	80	120	μA
VDD Shutdown Current		EN = low, PWM = floating	--	--	5	μA
VIN Quiescent Current	I_Q	PWM = floating, V_{IN} = 23V	--	--	1	μA
Power-On Reset						
VDD POR Rising			--	4.2	4.4	V
VDD POR Falling			3.8	4	--	V
VDD POR Hysteresis			--	200	--	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Input							
Input Current			V_{PWM} = 5V	--	250	--	μA
			V_{PWM} = 0V	--	–250	--	
Logic Level High			5V Logic	4.1	--	--	V
Logic Level Low			5V Logic	--	--	0.7	V
Tri-state Open Voltage			5V Logic	1.35	--	3.5	V
Tri-State Hold-off Time		t_{Tr-Off}		--	40	--	ns
Tri-State Recovery Time		t_{Tr}		--	40	--	ns
Disable Exit Recovery Time		t_{DER}		--	--	100	μs
Switching Time							
PWM to PHS Propagation Delay		t_{PD}	$V_{BOOT} - V_{SW}$ = 5V, PHS 0% to 90% VIN	--	40	--	ns
$R_{DS(ON)}$							
Switch On-Resistance	High-Side		$V_{BOOT} - V_{SW}$ = 5V	--	30	--	mΩ
	Low-Side			--	10	--	
Thermal Shutdown Protection							
Thermal Shutdown				--	160	--	°C
Thermal Shutdown Hysteresis				--	25	--	°C
EN Input							
EN Input Voltage		V_{EN_H}		2.6	--	--	V
		V_{EN_L}		--	--	1.8	

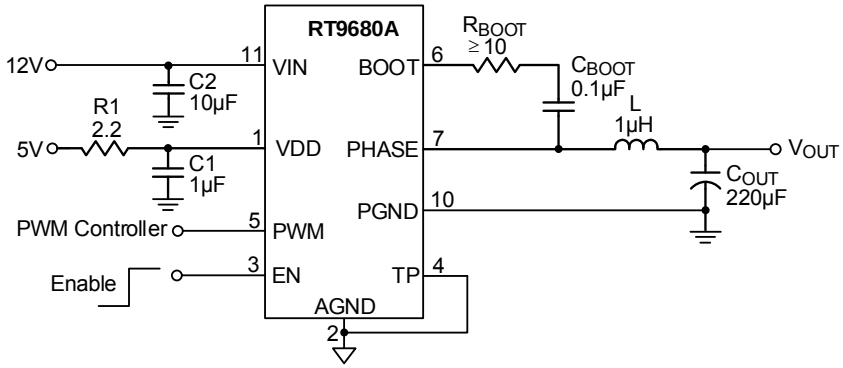
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Richtek Evaluation Board.

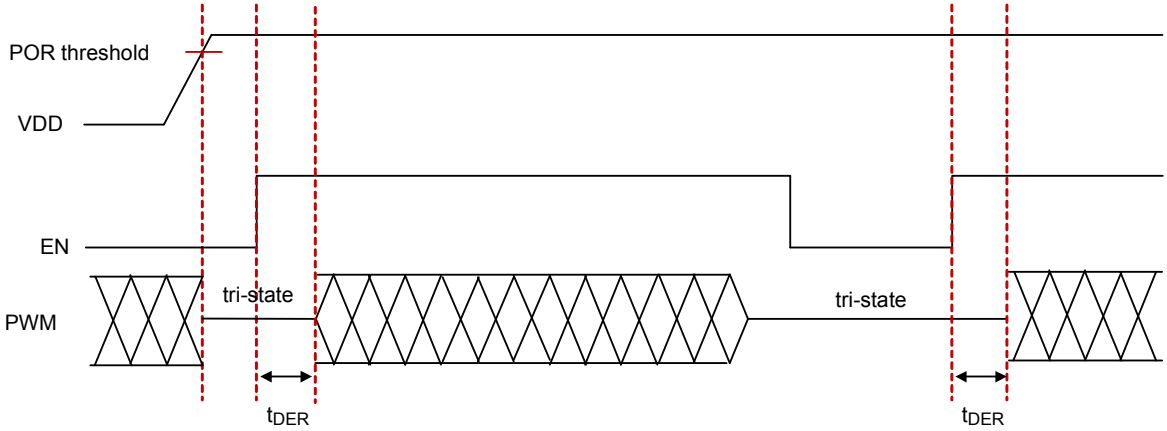
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

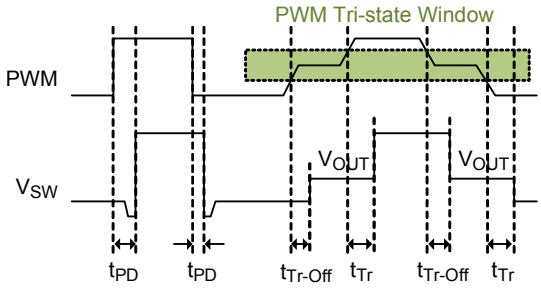
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit



Timing Diagram

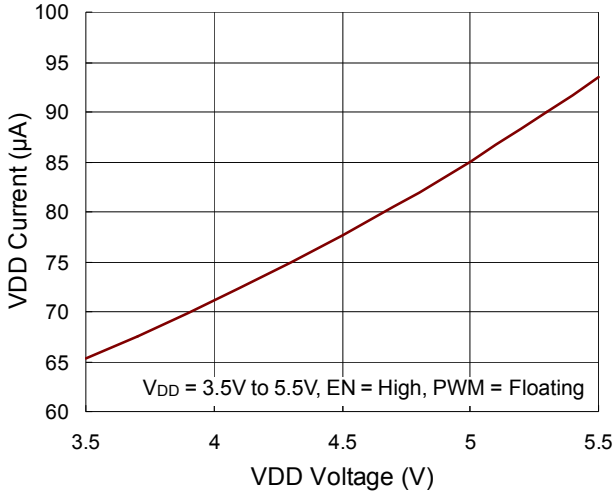




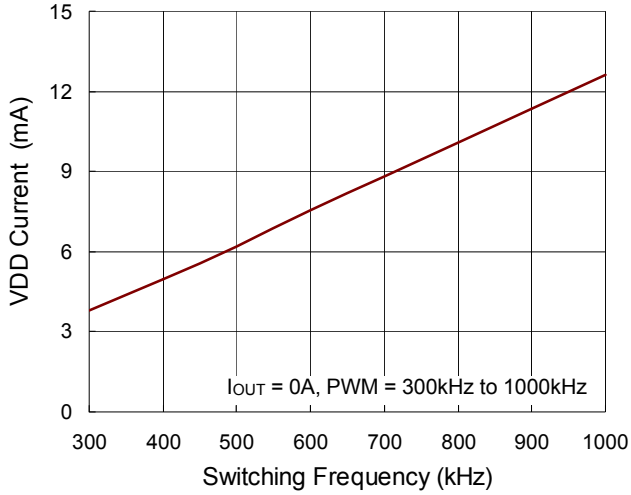
Typical Operating Characteristics

Unless otherwise specified, V_{DD} = 5V, V_{IN} = 12V, MHCI06030-R56M-R8 Inductor, L_{OUT} = 560nH, DCR = 5.5mΩ, V_{OUT} = 1V, T_A = 25°C

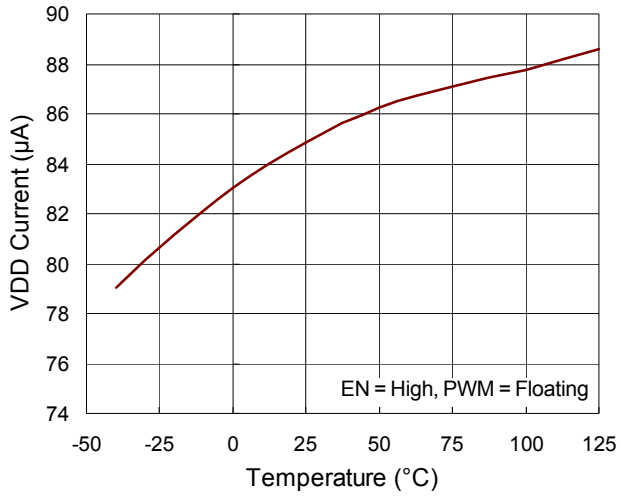
VDD Current vs. VDD Voltage



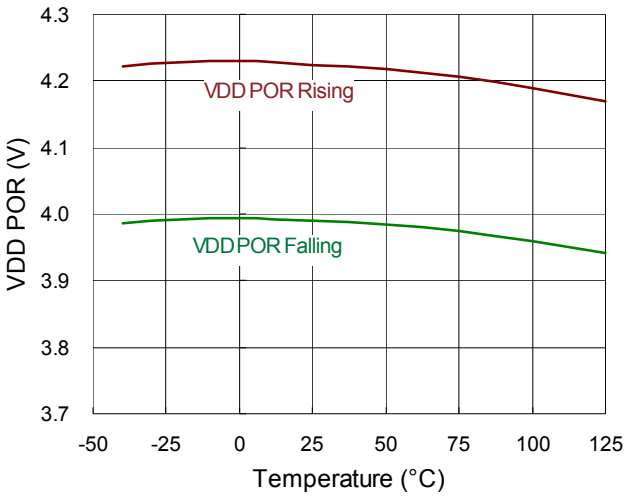
VDD Current vs. Switching Frequency



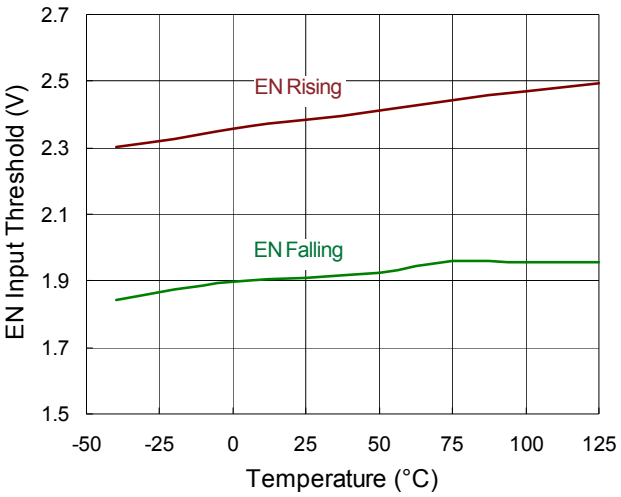
VDD Current vs. Temperature



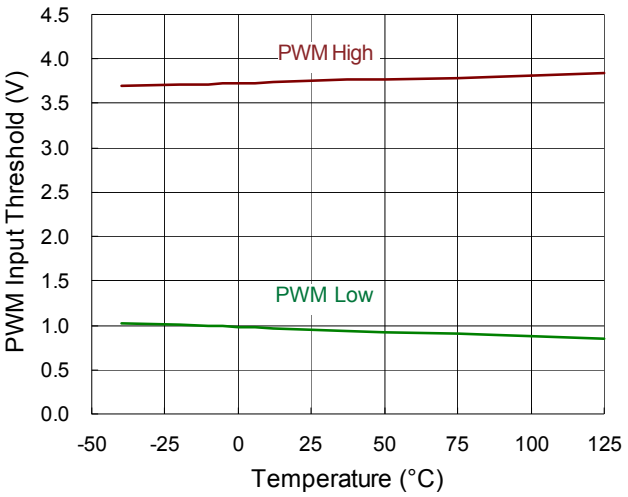
VDD POR vs. Temperature

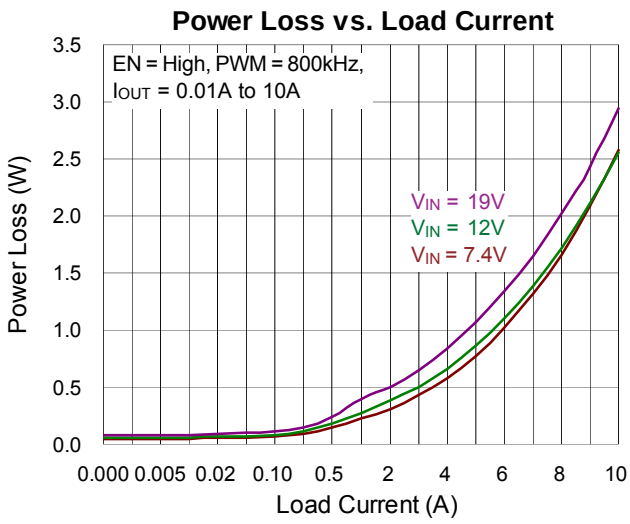


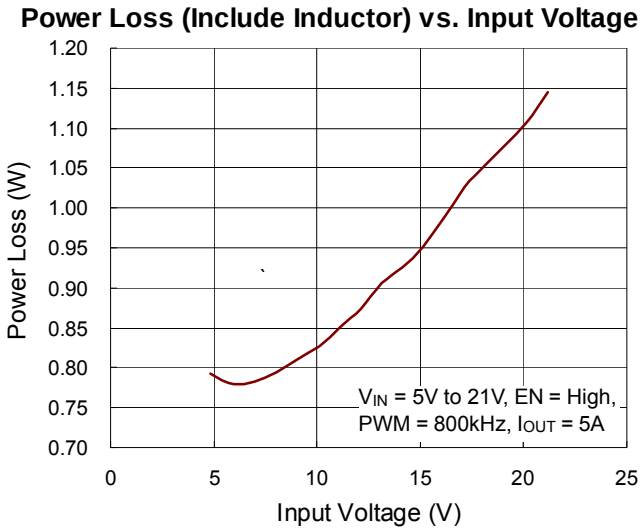
EN Input Threshold vs. Temperature



PWM Input Threshold vs. Temperature







Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The RT9680A is a fully integrated driver and power MOSFET designed to work over an input voltage range of 4.5 V to 23V with 5V supplies for gate drive and internal control circuits.

A number of features are provided making the RT9680A a highly versatile module. Internal high-side and internal low-side power MOSFETs are combined in one package with the pin outs optimized for power routing with minimum parasitic inductances. The internal MOSFETs are individually tailored for efficient operation as either high-side or low-side switches in a low duty cycle synchronous buck converter. A high current driver is also included in the package which minimizes the gate drive loop and results in extremely fast switching.

Supply Voltage and POR (Power-On Reset)

The RT9680A can be utilized under V_{DD} = 5V and it is designed to drive both internal high-side and internal low-side N-MOSFET through external input PWM control signal. It has power on protection function which held Internal UGATE and internal LGATE low before the V_{DD} voltage rises to higher than POR rising threshold voltage.

Power on reset (POR) occurs when VDD rises above 3.3V (typ.). The RT9680A will reset the fault latch and preparing the PWM for operation .When VDD below 200mV POR hysteresis , the VDD Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping driver low.

Enable and Disable

The RT9680A includes an EN pin for sequence control. When the EN pin rises above the V_{EN_H} trip point, the RT9680A begins a new initialization and follows the PWM command to control the internal UGATE and internal LGATE. When the EN pin falls below the V_{EN_L} trip point, the RT9680A shutdown and keeps internal UGATE and internal LGATE low.

There is a special case when EN go low to shutdown the RT9680A, that is when CCM operation and EN go low, this moment the RT9680A can not immediately turn off internal low-side MOSFET. The low-side MOSFET must turn on until inductor current decrease below 3A (typ). This behavior is in order to protects internal low-side MOSFET avoid damage from high inductor current.

Tri-State PWM Input

After the initialization, the PWM signal takes the control. The rising PWM signal first forces the internal LGATE signal to turn low then internal UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot through current. The falling of PWM signal first forces internal UGATE to go low. When internal UGATE and PHASE signal reach a predetermined low level, internal LGATE signal is allowed to turn high. The PWM signal is acted as " High" if the signal is above the rising threshold and acted as "Low" if the signal is below the falling threshold. When PWM signal level enters and remains within the shutdown window, the internal drivers are disabled and both internal MOSFET gates are pulled and held low. If the RT9680A PWM signal is left floating, the pin will be kept around 2.5V by the internal divider and provide the PWM controller with a recognizable level.

Internal Bootstrap Diode

The RT9680A builds in an internal bootstrap schottky diode to replace external bootstrap diode, and this can facilitate PCB design and reduce total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor and a 10 ohm resistor between BOOT pin and PHASE pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET switch.

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power

loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{PHASE} rises rapidly. In some cases, it is desirable to reduce EMI further, by the expense of some additional power dissipation.

Over-Temperature Protection

The RT9680A has internal temperature sense circuit to provide Over-Temperature Protection (OTP).When the junction temperature rising to 160°C, the IC will shutdown and with 25°C hysteresis.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-11HL 3x3 (FC) package, the thermal resistance, θ_{JA}, is 77.3°C/W on a four-layer Richtek Evaluation Board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (77.3°C/W) = 1.29W for a UQFN-11HL 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

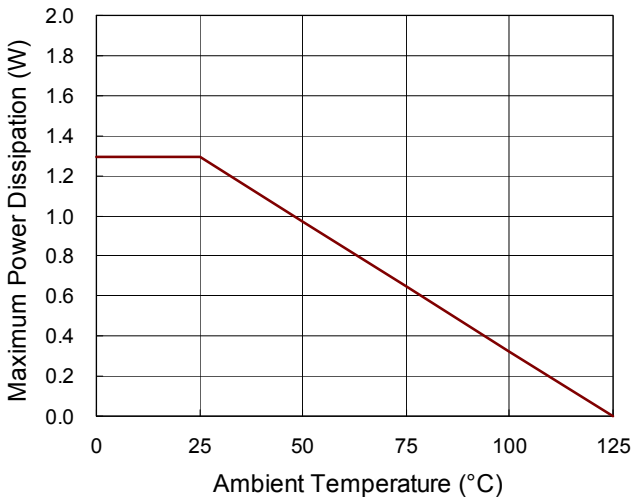
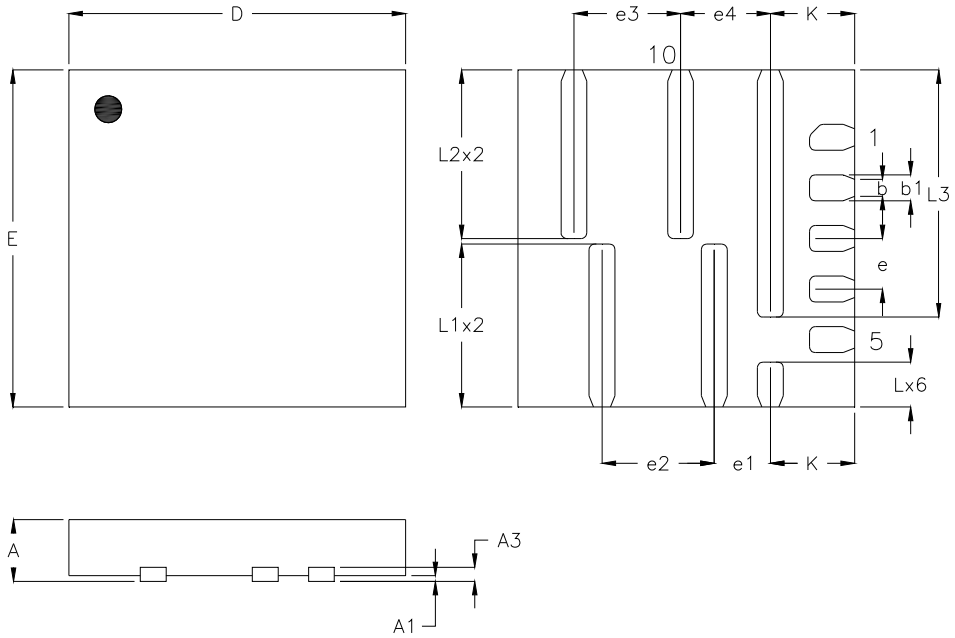


Figure 1. Derating Curve of Maximum Power Dissipation

PCB Layout Guidelines

The RT9680A is a high current rated for operation to up 1MHz.This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitic of the package or PCB. While excellent switching speeds are achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. The PCB design is somewhat simplified because integrated of the driver and power MOSFET in one package. The bulk of VIN and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The PHASE switching loop, formed by PHASE, output inductor and output capacitor C_{OUT} is the next critical parameter, this requires second layer. Should always be an uninterrupted PGND plane with sufficient GND vias placed as close as possible to by-pass Capacitors PGND pads. VIN and PGND to simplify thermal management. Using vias, Both VIN and PGND pads should be attached to VIN and PGND plane directly as shown below. Thermal reliefs should be avoided to ensure proper heat dissipation to the board. VDD By-pass capacitor C_{VDD} should connect directly to PGND plane as shown below, use a via to connect C_{VDD} directly to GND plane, connect C_{BOOT} and R_{BOOT} directly to pins 6 and pin7.

Outline Dimension

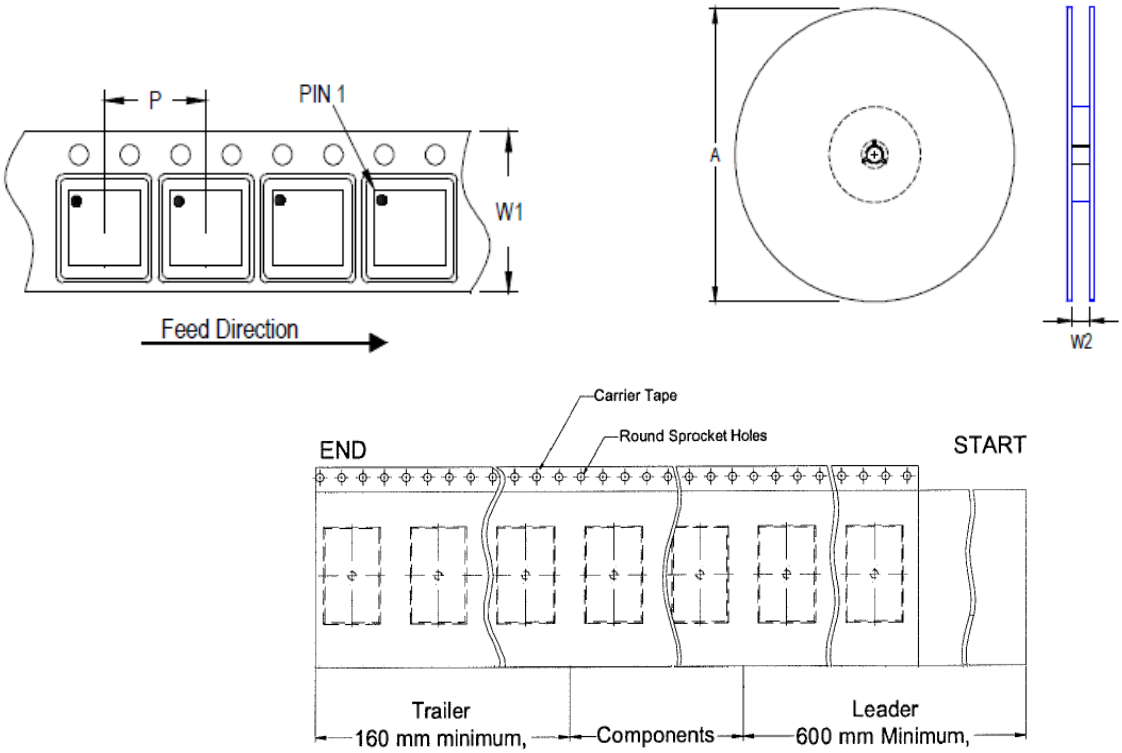


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
b	0.100	0.200	0.004	0.008
b1	0.180	0.280	0.007	0.011
L	0.300	0.500	0.012	0.020
L1	1.350	1.550	0.053	0.061
L2	1.400	1.600	0.055	0.063
L3	2.100	2.300	0.083	0.091
e	0.450		0.018	
e1	0.500		0.020	
e2	1.000		0.039	
e3	0.950		0.037	
e4	0.800		0.031	
K	0.750		0.030	

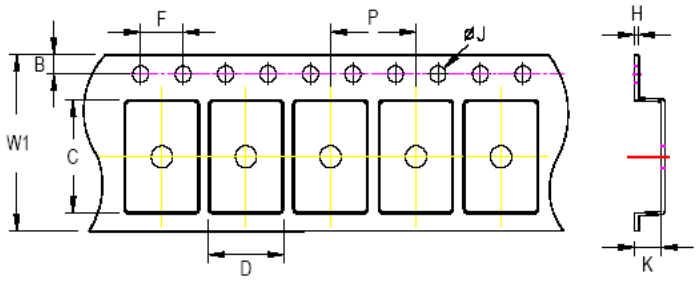
U-Type 11HL QFN 3x3 (FC) Package

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



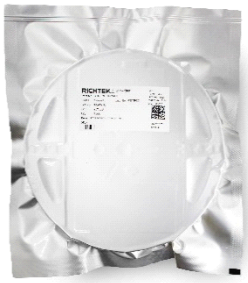
C, D and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Un -full Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$

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Datasheet Revision History

Version	Date	Description	Item
01	2022/12/7	Modify	Part No. on P1, 3, 4, 5, 8 Application Information on P9 Outline Dimension on P11 Packing Information on 12, 13, 14