RICHTEK® **RT9470/D**

3A Single Cell Switching Battery Charger

1 General Description

The RT9470/D is a highly-integrated 3A switch mode battery charge management and system power path management device for single cell Li-Ion and Li-Polymer batteries. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The recommended junction temperature range is –40°C to 150°C, and the ambient temperature range is –40°C to 85°C.

2 Applications

- Smart Phone/Tablet PC
- Personal Information Appliances
- Portable Device and Accessory

3 Ordering Information

RT9470/D □

- **Package Type**(1)
  WSC: WL-CSP-30B 2.1x2.5 (BSC)
- **BC1.2 Detection**
  Default: Not Support
  D: Support

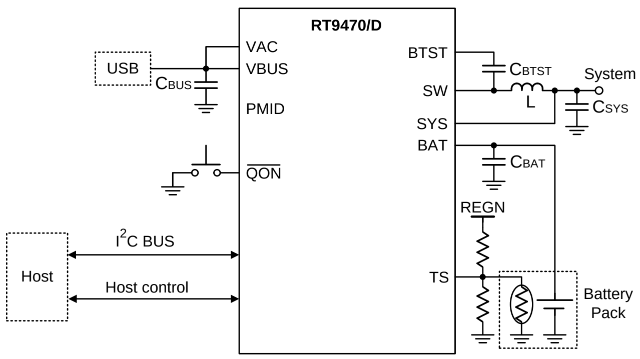
Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

4 Features

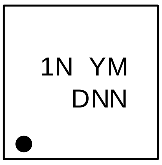
- **High Efficiency, 1.5MHz, Synchronous Switch-Mode Buck Charger**
  - **92% Charge Efficiency at 2A from 5V Input and 3.8V Battery**
  - **Support 3.9V to 13.5V Input Voltage Range**
  - **Average Input Current Regulation (AICR)**
  - **Minimum Input Voltage Regulation (MIVR)**
  - **Minimum Input Voltage Regulation Track (MIVR Track)**
  - **Charge Current Regulation (CCR)**
  - **Charge Voltage Regulation (CVR)**
  - **Charge Voltage Regulation Track (CVR Track)**
  - **Junction Thermal Regulation (JTR)**
- **Support USB On-The-Go (OTG)**
  - **92% Boost Efficiency at 1A with 3.8V Battery and 5.15V Output**
  - **OTG Current Limit Regulation (OCLR)**
  - **OTG Voltage Limit Regulation (OVLR)**
- **Protection**
  - **Over-Temperature Protection (OTP)**
  - **VBUS Overvoltage Protection (VBUS OVP)**
  - **Battery Overvoltage Protection (VBAT OVP)**
  - **System Overvoltage Protection (VSYS OVP)**
  - **System Undervoltage Protection (VSYS UVP)**
  - **System Over-Load Protection (VSYS OLP)**
  - **Cycle-by-Cycle Overcurrent Protection (OCP)**
  - **OTG Low Battery Protection (OTG LBP)**

5 Simplified Application Circuit



6 Marking Information

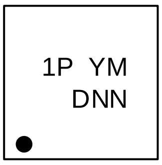
RT9470WSC



1N: Product Code

YMDNN: Date Code

RT9470DWSC



1P: Product Code

YMDNN: Date Code

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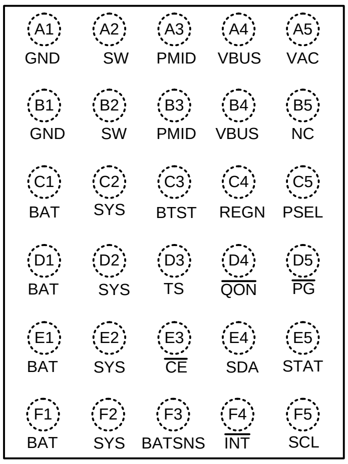
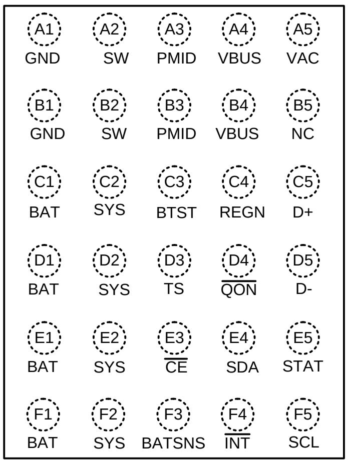
7 Pin Configuration

(TOP VIEW)



WL-CSP-30B 2.1x2.5 (BSC) (RT9470)



WL-CSP-30B 2.1x2.5 (BSC) (RT9470D)

8 Functional Pin Description

Pin No.		Pin Name	I/O	Pin Function
RT9470	RT9470D			
A1, B1	A1, B1	GND	P	Power ground.
A2, B2	A2, B2	SW	P	Switching node connecting to the output inductor. Internally, SW is connected to the source of the high-side switching MOSFET (Q2) and the drain of the low-side switching MOSFET (Q3). Connect a 47nF bootstrap capacitor from SW to BTST.
A3, B3	A3, B3	PMID	P	Connected to the drain of the reverse blocking MOSFET (Q1) and the drain of the high-side switching MOSFET (Q2). Connect a 10μF capacitor from PMID to GND.
A4, B4	A4, B4	VBUS	P	Charger input voltage. The internal reverse block MOSFET (Q1) is connected between VBUS and PMID, with VBUS on the source. Connect a 1μF capacitor from VBUS to GND and place it as close as possible to the IC.
A5	A5	VAC	AI	Input voltage sensing. This pin must be tied to VBUS.
B5	B5	NC	--	No internal connection.
C1, D1, E1, F1	C1, D1, E1, F1	BAT	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10μF capacitor closely to the BAT pin.
C2, D2, E2, F2	C2, D2, E2, F2	SYS	P	Converter output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect two 10μF capacitors closely to the SYS pin.
C3	C3	BTST	P	PWM high-side driver positive supply. Internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 47nF bootstrap capacitor from SW to BTST.

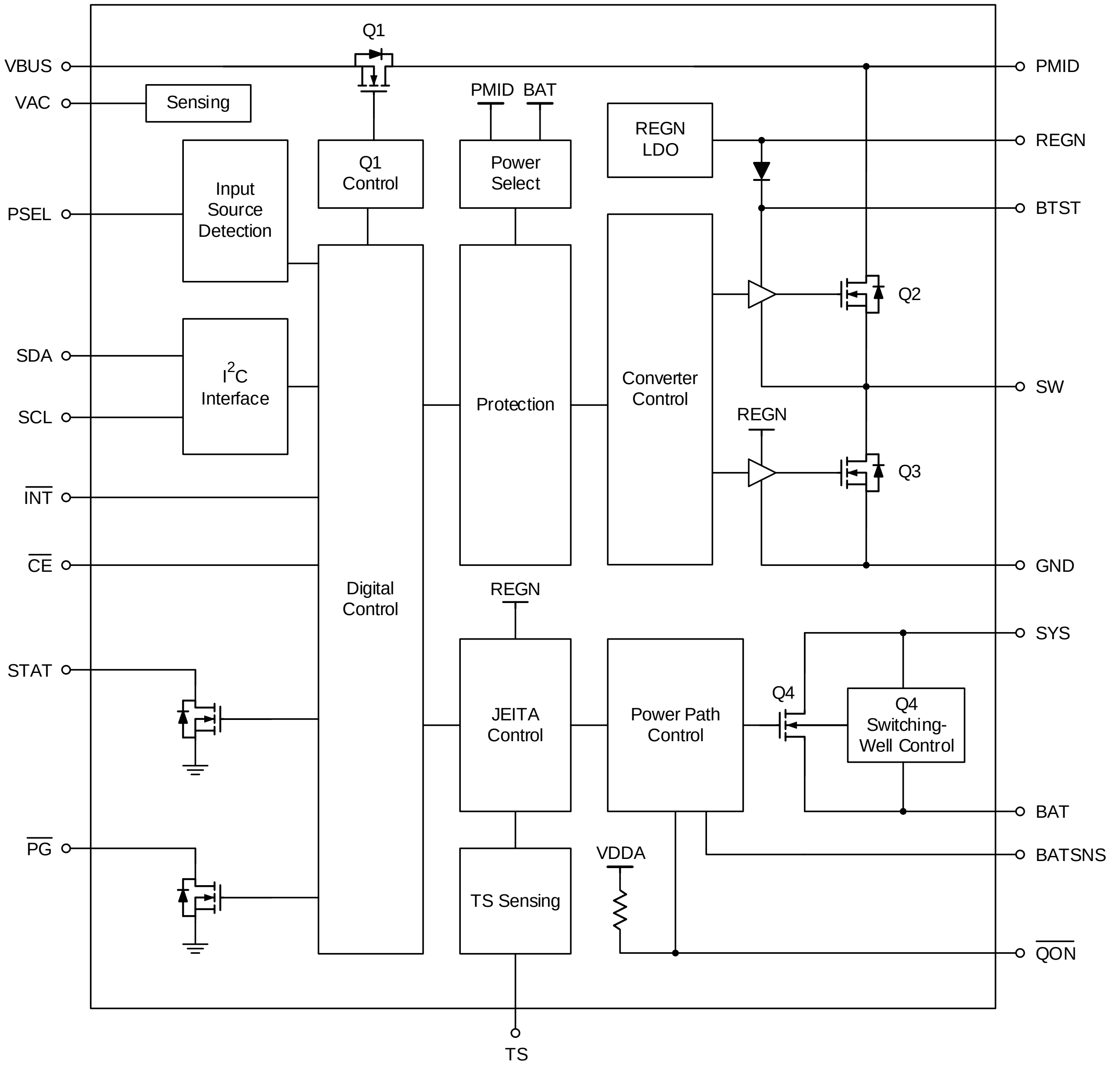
Pin No.		Pin Name	I/O	Pin Function
RT9470	RT9470D			
C4	C4	REGN	P	PWM low-side driver and internal supply output. Internally, REGN is connected to the anode of the bootstrap diode. Connect a 4.7μF capacitor from REGN to GND. The capacitor should be placed close to the IC.
C5	--	PSEL	DI	Power source selection input. A high level indicates a 0.5A input current limit, while a low level indicates a 2.4A input current limit. Once the device enters host mode, the host can program a different input current limit to the AICR register.
--	C5	D+	AIO	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary detection, and secondary detections in BC1.2.
D3	D3	TS	AI	Temperature qualification voltage input to support the JEITA profile. Connect a negative temperature coefficient thermistor. Program the temperature window with a resistor divider from REGN to TS to GND. Charging suspends when the TS pin voltage is out of range. When the TS pin is not used, connect a 10kΩ resistor from REGN to TS and a 10kΩ resistor from TS to GND.
D4	D4	$\overline{QON}$	DI	BATFET (Q4) enable control input. When BATFET is in ship mode, a logic low duration turns on BATFET (Q4) to exit shipping mode. When there is no VBUS, a logic low for t_{QON_RST} turns off the BATFET for t_{BATFET_RST}, and then re-enables BATFET to provide a system reset. Pull-High to the internal bias circuit via a 250kΩ resistor.
D5	--	$\overline{PG}$	DO	Open-drain active low power good indicator. Connect the $\overline{PG}$ pin to a logic rail via a 2.2kΩ to 10kΩ resistor.
--	D5	D-	AIO	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary detection, and secondary detections in BC1.2.
E3	E3	$\overline{CE}$	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
E4	E4	SDA	DIO	I^2C interface clock. Connect SDA to the logic rail through a 10kΩ resistor.
E5	E5	STAT	DO	Open-drain charger status output. Connect the STAT pin to a logic rail via a 2.2kΩ to 10kΩ resistor. The STAT pin indicates the charger status.
F3	F3	BATSNS	AI	Battery voltage sensing pin for charge current regulation. The BATNS pin must be connected to the battery pack as close as possible.
F4	F4	$\overline{INT}$	DO	Open-drain active-low interrupt output. Connect the INT pin to a logic rail through a 10kΩ resistor. The INT pin sends an active-low pulse to the host to report charger device status and faults.
F5	F5	SCL	DI	I^2C interface clock. Connect SCL to the logic rail through a 10kΩ resistor.

8.1 I/O Type Definition

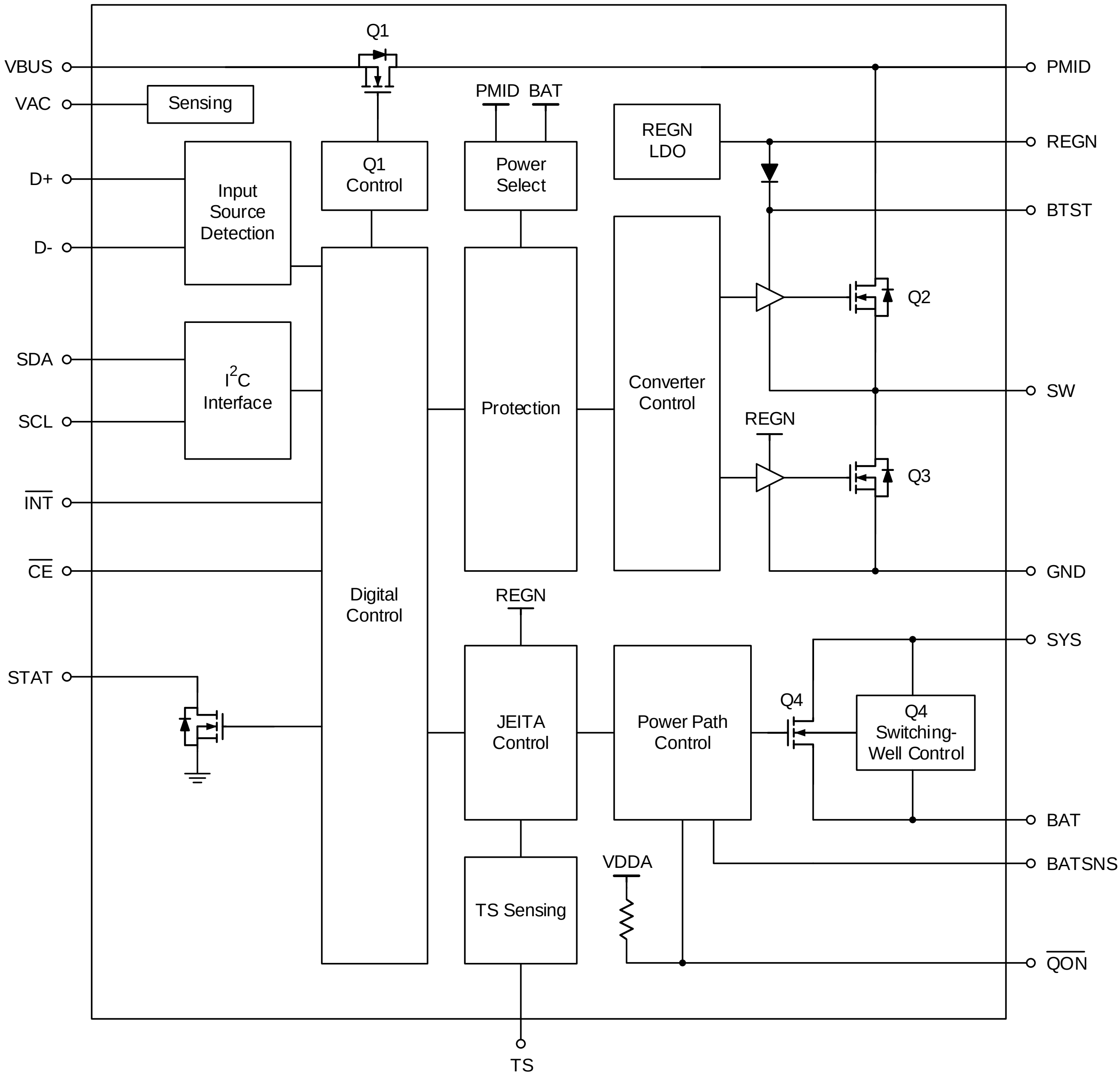
- DIO: Digital Input/Output Pin
- DI: Digital input Pin
- DO: Digital Output Pin
- AIO: Analog Input/Output Pin
- AI: Analog Input Pin
- P: Power Pin

9 Functional Block Diagram

9.1 For the RT9470



9.2 For the RT9470D



10 Absolute Maximum Ratings

(Note 2)

- Voltage Sense Pin Voltage, VAC ---------- –1.4V to 26V
- Supply Pin Voltage, VBUS ---------- –1.4V to 26V
- Terminal Pin Voltage, PMID ---------- –0.3V to 26V
- Terminal Pin Voltage, SW ---------- –0.3V to 16V
- Terminal Pin Voltage, BTST-SW ---------- –0.3V to 6V
- Terminal Pin Voltage, SYS ---------- –0.3V to 6V
- Supply Pin Voltage, BAT ---------- –0.3V to 6V
- Voltage Sense Pin Voltage, BATSNS ---------- –0.3V to 6V
- Other Pins Voltage, STAT, SCL, SDA, $\overline{INT}$, $\overline{CE}$, TS, $\overline{QON}$, REGN ---------- –0.3V to 6V
- Other Pins Voltage for RT9470, PSEL, $\overline{PG}$ ---------- –0.3V to 6V
- Other Pins Voltage for RT9470D, D+, D- ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WL-CSP-30B 2.1x2.5 (BSC) ---------- 4.22W
- Package Thermal Resistance (Note 3)

  WL-CSP-30B 2.1x2.5 (BSC), θ_{JA} ---------- 29.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Voltage Sense Pin Voltage, VAC ---------- 3.9V to 13.5V
- Supply Input Voltage Range, VBUS ---------- 3.9V to 13.5V
- Maximum Input Current, IBUS ---------- 3.2A
- Maximum Input Current, IBUS (VBUS ≥ 12V) ---------- 2A
- Maximum Output Current (SW), ISYS ---------- 3.2A
- Maximum Battery Voltage, VBAT ---------- 4.7V
- Voltage Sense Pin Voltage, BATSNS ---------- 4.7V

- Maximum Charge Current, IBAT --- 3.15A
- Maximum Discharge Current, IBAT -- 6A
- Ambient Temperature Range -- –40°C to 85°C
- Junction Temperature Range --- –40°C to 150°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

($V_{BUS\_MIN\_RISE}$ < V_{AC} < $V_{AC\_OVP\_RISE}$ and V_{AC} > V_{BAT} + V_{SLEEP_RISE}, T_A = 25°C, unless otherwise specified) (Note 6)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
Battery Discharge Current (BAT) in Q4 Disabled	$I_{BAT\_Q4\_DIS}$	V_{BAT} = 4.5V, High-Z mode and I^2C disabled, Q4 disabled	--	15	32	μA
Battery Discharge Current (BAT) in Q4 Enable	$I_{BAT\_Q4\_EN}$	V_{BAT} = 4.5V, High-Z mode and I^2C disabled, Q4 enabled	--	55	85	μA
Input Supply Current (VBUS) in Buck Mode	I_{BUS_HIZ}	V_{BUS} = 5V, High-Z mode and no battery	--	50	86	μA
		V_{BUS} = 12V, High-Z mode and no battery	--	52	88	
Input Supply Current (VBUS) in Buck Mode	I_{BUS_BUCK}	V_{BUS} > $V_{BUS\_MIN\_RISE}$, V_{BUS} > V_{BAT}, converter switching, V_{BAT} = 3.8V, I_{SYS} = 0A	--	5	7	mA
Battery Discharge Current (BAT) in Boost Mode	I_{BAT_BOOST}	V_{BAT} = 4.2V, boost mode, I_{BUS} = 0A, converter switching	--	4	5	mA
VAC, VBUS and BAT Power						
VBUS Operating Range	V_{BUS_OP}	V_{BUS} rising	3.9	--	13.5	V
REGN Turn Off Level with Only VBUS	V_{BUS_UVLO}	V_{BUS} falling	3.0	3.3	3.6	V
Sleep Mode Falling Threshold	V_{SLEEP_FALL}	V_{AC} falling, V_{AC} – V_{BAT}	10	60	120	mV
Sleep Mode Rising Threshold	V_{SLEEP_RISE}	V_{AC} rising, V_{AC} – V_{BAT}	160	250	340	mV
VAC 5.8V Overvoltage rising threshold	$V_{AC\_OVP\_RISE}$	V_{AC} rising	5.5	5.8	6.1	V
VAC 6.5V Overvoltage rising threshold		V_{AC} rising	6.2	6.5	6.8	
VAC 10.9V Overvoltage Rising Threshold		V_{AC} rising	10.3	10.9	11.5	
VAC 14V Overvoltage Rising Threshold		V_{AC} rising	13.3	14	14.7	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VAC 5.8V Overvoltage Hysteresis	$V_{AC\_OVP\_HYS}$	V_{AC} falling	--	300	--	mV
VAC 6.5V Overvoltage Hysteresis		V_{AC} falling	--	300	--	
VAC 10.9V Overvoltage Hysteresis		V_{AC} falling	--	300	--	
VAC 14V Overvoltage Hysteresis		V_{AC} falling	--	300	--	
BAT for Active I^2C, No Adapter	V_{BAT_UVLO}	V_{BAT} rising	2	2.2	2.4	V
Battery Depletion Falling Threshold	$V_{BAT\_DPL\_FALL}$	V_{BAT} falling	2.15	2.38	2.65	V
Battery Depletion Rising Threshold	$V_{BAT\_DPL\_RISE}$	V_{BAT} rising	2.4	2.6	2.8	V
Battery Depletion Rising Hysteresis	$V_{BAT\_DPL\_HYS}$	V_{BAT} rising	--	220	--	mV
Bad Adapter Detection Rising Threshold	$V_{BUS\_MIN\_RISE}$	V_{BUS} rising	3.6	3.8	4	V
Bad Adapter Detection Hysteresis	$V_{BUS\_MIN\_HYS}$	V_{BUS} falling	--	200	--	mV
Bad Adapter Detection Current Source	I_{BADSRC}	Sink current from V_{BUS} to GND	--	40	--	mA
Power Path						
System Regulation Voltage	V_{SYS_MIN}	V_{BAT} < V_{SYS_MIN} = 3.5V, Q4 disabled/enable	3.5	3.5 +0.2	--	V
	V_{SYS}	I_{SYS} = 0A, V_{BAT} > V_{SYS_MIN} = 3.5V, Q4 disabled	--	V_{BAT} +0.05	--	
Top Reverse Blocking MOSFET On-Resistance Between VBUS and PMID	$R_{ON(Q1)}$	–40°C ≤ T_A ≤ 125°C	--	29	--	mΩ
Top Switching MOSFET On- Resistance Between PMID and SW	$R_{ON(Q2)}$	V_{REGN} = 5V, –40°C ≤ T_A ≤ 125°C	--	46	--	mΩ
Bottom Switching MOSFET On-Resistance Between SW and GND	$R_{ON(Q3)}$	V_{REGN} = 5V, –40°C ≤ T_A ≤ 125°C	--	51	--	mΩ
SYS-BAT MOSFET On-Resistance	$R_{ON(BAT-SYS)}$	Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = 25°C	--	14	--	mΩ
Battery Charger						
Charge Voltage Range	$V_{BAT\_REG\_RANGE}$	Default = 4.2V	3.9	--	4.7	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$		--	10	--	mV
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$		–0.5	--	0.5	%
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$	Default = 2000mA	0	--	3150	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$		--	50	--	mA
Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	V_{BAT} = 3.8V, I_{CHG_REG} < 150mA	–20	--	20	%
		V_{BAT} = 3.8V, 150mA ≤ I_{CHG_REG} < 750mA	–10	--	10	
		V_{BAT} = 3.8V, I_{CHG_REG} ≥ 750mA	–5	--	5	
Pre-Charge Falling Threshold	$V_{PRE\_CHG\_FALL}$	I_{CHG} = 200mA, V_{PRE_CHG} = 3.1V	2.75	2.9	3.05	V
Pre-Charge Rising Threshold	$V_{PRE\_CHG\_RISE}$	Pre-charge to fast charge, V_{PRE_CHG} = 3.1V	2.95	3.1	3.25	V
Pre-Charge Current Range	$I_{PRE\_CHG\_RANGE}$	Default = 150mA	50	--	800	mA
Pre-Charge Current Step	$I_{PRE\_CHG\_STEP}$		--	50	--	mA
Pre-Charge Accuracy	$I_{PRE\_CHG\_ACC}$	V_{BUS} = 5V, I_{PRE_CHG} = 150mA	–15	--	25	%
End-Of-Charge Current Range	$I_{EOC\_CHG\_RANGE}$	Default = 200mA	50	--	800	mA
End-Of-Charge Current Step	$I_{EOC\_CHG\_STEP}$		--	50	--	mA
End-Of-Charge Accuracy	$I_{EOC\_CHG\_ACC}$	I_{CHG_REG} > 700mA, I_{EOC_CHG} = 200mA, VBAT = 4.2V	–20	--	20	%
		I_{CHG_REG} ≤ 700mA, I_{EOC_CHG} = 200mA, VBAT = 4.2V	–10	--	10	
		I_{CHG_REG} = 600mA, I_{EOC_CHG} = 50mA, VBAT = 4.2V	–25	--	25	
Trickle-Charge Falling Threshold	$V_{TRICKLE\_CHG\_FALL}$	V_{BAT} falling	1.8	2	2.2	V
Trickle-Charge Rising Threshold	$V_{TRICKLE\_CHG\_RISE}$	V_{BAT} rising	2.05	2.25	2.45	V
Trickle-Charge Current	$I_{TRICKLE\_CHG}$	V_{BAT} < $V_{TRICKLE\_CHG\_RISE}$	80	100	120	mA
Re-Charge Threshold Below VBAT_REG	V_{RE_CHG}	V_{BAT} falling, V_{RECHG} = 100mV	70	100	130	mV
		V_{BAT} falling, V_{RECHG} = 200mV	170	200	230	
System Discharge Load Current	I_{SYS_LOAD}	V_{SYS} = 4.2V	--	30	--	mA
Input Voltage and Current Regulation						
Minimum Input Voltage Regulation Range	V_{MIVR_RANGE}	Default = 4.5V	3.9	--	5.4	V
Minimum Input Voltage Regulation Step	V_{MIVR_STEP}		--	100	--	mV
Minimum Input Voltage Regulation Accuracy	V_{MIVR_ACC}	V_{MIVR} = 3.9V and 4.4V	–1.5	--	1.5	%
MIVR Tracking VBAT	$V_{MIVR\_BAT\_TRACK}$	V_{MIVR} = 3.9V, $V_{MIVR\_BAT\_TRACK}$ = 300mV, V_{BAT} = 4V	--	4.3	--	V
MIVR Tracking VBAT Accuracy	$V_{MIVR\_BAT\_TRACK\_ACC}$		–3	--	3	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Average Input Current Regulation Range	I_{AICR_RANGE}	Default = 0.5A	0.05	--	3.2	A
Average Input Current Regulation Step	I_{AICR_STEP}		--	50	--	mA
Average Input Current Regulation Accuracy	I_{AICR_ACC}	V_{BUS} = 5V, I_{AICR} = 500mA	450	470	500	mA
		V_{BUS} = 5V, I_{AICR} = 900mA	780	840	900	mA
		V_{BUS} = 5V, I_{AICR} = 1500mA	1300	1400	1500	mA
		V_{BUS} = 5V, I_{AICR} > 1500mA	–15	--	0	%
BAT Overvoltage Protection						
Battery Overvoltage Rising	$V_{BAT\_OVP\_RISE}$	V_{BAT} rising, as percentage of V_{BAT_REG}	103	104	105	%
Battery Overvoltage Falling	$V_{BAT\_OVP\_FALL}$	V_{BAT} falling, as percentage of V_{BAT_REG}	101	102	103	%
Input Reverse Blocking NFET and Regulation						
Junction Thermal Regulation Range	$T_{J\_THREG\_RANGE}$	Default = 120°C	100	--	120	°C
Junction Thermal Regulation Step	$T_{J\_THREG\_STEP}$		--	20	--	°C
Thermal Shutdown Rising	T_{OTP}	Temperature rising	--	160	--	°C
Thermal Shutdown Hysteresis	T_{OTP_HYS}	Temperature falling	--	30	--	°C
NTC Monitor (Charger Mode)						
Battery Temperature COLD Threshold (0°C)	V_{VTS_COLD}	V_{TS} rising, the ratio of V_{REGN}	72.5	73.5	74.5	%
Battery Temperature COOL Threshold (10°C)	V_{VTS_COOL}	V_{TS} rising, the ratio of V_{REGN}	67.5	68.5	69.5	%
Battery Temperature WARM Threshold (45°C)	V_{VTS_WARM}	V_{TS} falling, the ratio of V_{REGN}	44	45	46	%
Battery Temperature HOT Threshold (60°C)	V_{VTS_HOT}	V_{TS} falling, the ratio of V_{REGN}	33.5	34.5	35.5	%
Battery Temperature Hysteresis	V_{VTS_HYS}		--	1.5	--	%
NTC Monitor (OTG Mode)						
Battery Temperature COLD Threshold OTG mode (–20°C)	$V_{VTS\_COLD\_OTG}$	V_{TS} rising, the ratio of V_{REGN}	79	80	81	%
Battery Temperature HOT Threshold OTG mode (60°C)	$V_{VTS\_HOT\_OTG}$	V_{TS} falling, the ratio of V_{REGN}	33.5	34.5	35.5	%
Battery Temperature Hysteresis OTG mode	$V_{VTS\_HYS\_OTG}$		--	1.5	--	%

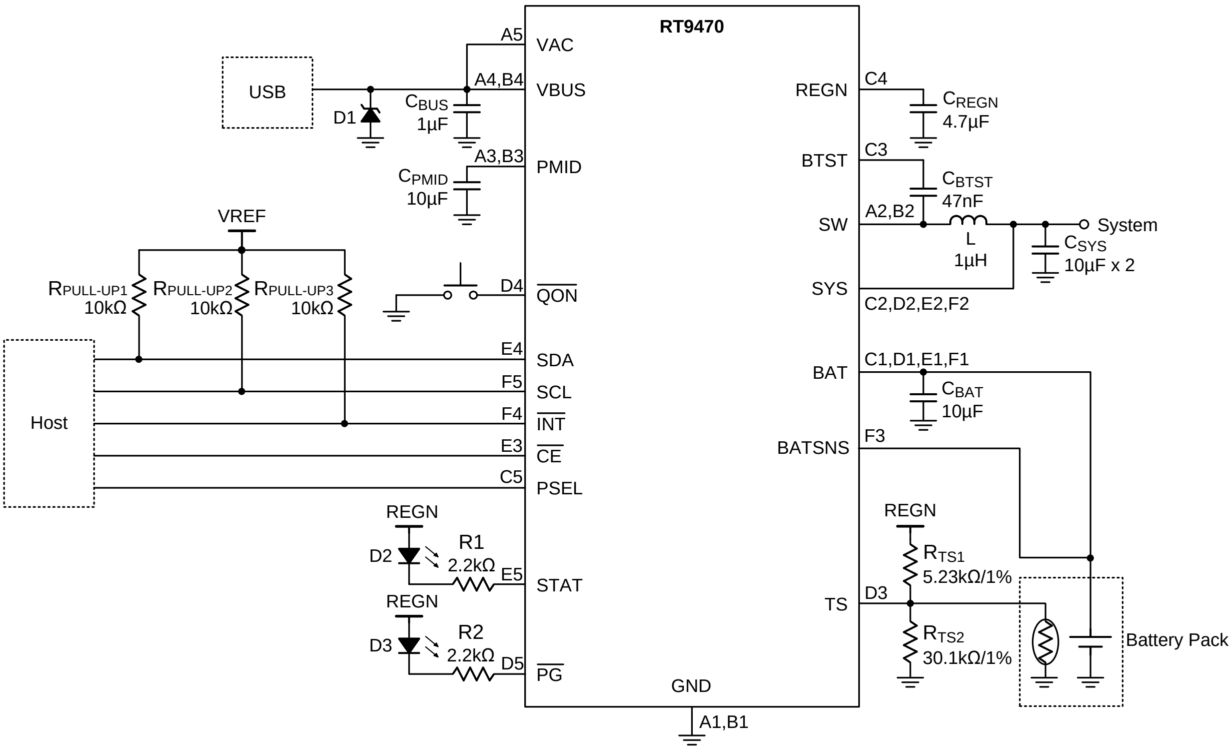
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Charger Overcurrent Threshold						
UGFET Cycle-by-Cycle Overcurrent Threshold	I_{OCP_UG}		5.5	6.5	7.5	A
System Over-Load Threshold	I_{OCP_BATFET}		6	--	--	A
USB On-The-Go (OTG)						
OTG Low Battery Protection	V_{OTG_LBP}	V_{BAT} falling, V_{OTG_LBP} = 2.8V	2.65	2.8	2.95	V
		V_{BAT} rising, V_{OTG_LBP} = 2.8V	2.75	2.9	3.05	
		V_{BAT} falling, V_{OTG_LBP} = 2.5V	2.35	2.5	2.65	
		V_{BAT} rising, V_{OTG_LBP} = 2.5V	2.45	2.6	2.75	
OTG Voltage Limit Regulation Range	$V_{OTG\_CV\_RANGE}$	Default = 5.15V	4.85	--	5.3	V
OTG Voltage Limit Regulation Step	$V_{OTG\_CV\_STEP}$		--	150	--	mV
OTG Voltage Limit Regulation Accuracy	$V_{OTG\_CV\_ACC}$	V_{BAT} = 3.8V, I_{PMID} = 0A, V_{OTG_REG} = 5.15V	–3	--	3	%
OTG Current Limit Regulation Accuracy	I_{OTG_CC}	$I_{OTG\_LIMIT\_REG\_SEL}$ = 1.2A	1.2	1.4	1.6	A
		$I_{OTG\_LIMIT\_REG\_SEL}$ = 0.5A	0.5	0.6	0.7	
OTG Overvoltage Threshold	V_{OTG_OVP}	V_{AC} rising, V_{AC_OVP} = 6.5V	6.2	6.5	6.8	V
OTG Capacitive Load	C_{OTG_LOAD}	V_{BAT} = 3.8V, V_{OTG_REG} = 5.15V, capacitive load plug in	--	--	300	μF
PWM						
PWM Switching Frequency	f_{SW_BUCK}	Oscillator frequency, buck mode	1350	1500	1650	kHz
	f_{SW_BOOST}	Oscillator frequency, boost mode	1350	1500	1650	
Maximum PWM Duty Cycle	D_{MAX}		--	97	--	%
REGN						
REGN LDO Output Voltage	VREGN	V_{BUS} = 9V, I_{REGN} = 40mA	4.5	4.9	5.3	V
		V_{BUS} = 5V, I_{REGN} = 20mA	4.5	4.9	5	
Control I/O Pin ($\overline{CE}$, PSEL, SCL and SDA)						
Input High Threshold Voltage	V_{IH_CTRL}		1.3	--	--	V
Input Low Threshold Voltage	V_{IL_CTRL}		--	--	0.4	V
High Level Leakage Current	I_{BIAS}	Pull high to 1.8V	--	--	1	μA
Control I/O Pin ($\overline{PG}$, STAT, and $\overline{INT}$)						
Output Low Threshold Voltage	V_{OL_CTRL}		--	--	0.4	V
$\overline{INT}$ Pull Low Time	$t_{INT\_PULL\_LOW}$	$\overline{INT}$ pull low time	--	256	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
D+/D- Detection						
Data Detect Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
D- Current Sink	I_{D-_ISNK}		50	100	150	μA
D+D- Leakage Current	I_{D+D-_LKG}		−1	--	1	μA
D- Pull Down for Connection Check	R_{D-_19K}		14.25	19.53	24.8	kΩ
D+D- Threshold for Non-Standard Adapter (1.2V)	V_{D+D-_1P2}		--	1.2	--	V
D+D- Threshold for Non-Standard Adapter (2V)	V_{D+D-_2P0}		--	2	--	V
D+D- Threshold for Non-Standard Adapter (2.8V)	V_{D+D-_2P8}		--	2.8	--	V
Timing Requirements						
VAC OVP Reaction Time	t_{VAC_OVP}		--	200	--	ns
Bad Adapter Detection Duration	$t_{BAD\_AD\_DETECTION}$		--	30	--	ms
Deglitch Time for Charger EOC	t_{EOC_DGL}		--	256	--	ms
Deglitch Time for Re-Charge	$t_{RE\_CHG\_DGL}$		--	256	--	ms
Charge Safe Timer	$t_{CHG\_SAFE\_TMR}$	Timer = 10hr	9	10	11	hr
Back-Ground Charge Timer	$t_{BG\_CHG\_TMR}$	Timer = 30min	29	30	31	min
$\overline{\text{QON}}$ Timing						
$\overline{\text{QON}}$ Low Time to Exit Shipping Mode	$t_{SHIPMODE\_EXIT}$		0.9	1.1	1.3	s
$\overline{\text{QON}}$ Low Time to Reset System	t_{QON_RST}		9	10	11	s
BATFET Reset Time	t_{BATFET_RST}		430	453	480	ms
Enter Shipping Mode Delay Time	$t_{SHIP\_MODE\_ENTER}$		11	12	13	s
I^2C Clock and Watchdog Timer						
SCL Clock	f_{SCL}	CB ≤ 100pF	--	--	3.4	MHz
		100pF < CB ≤ 400pF	--	--	1.7	
Watchdog Timer	t_{WDT}	Default = 40s	--	40	--	s
Watchdog Reset Wait Time	t_{WDT_WAIT}		--	500	--	ms

Note 6. Specification is guaranteed by design and/or correlation with statistical process control.

13 Typical Application Circuit

13.1 For the RT9470



13.2 For the RT9470D

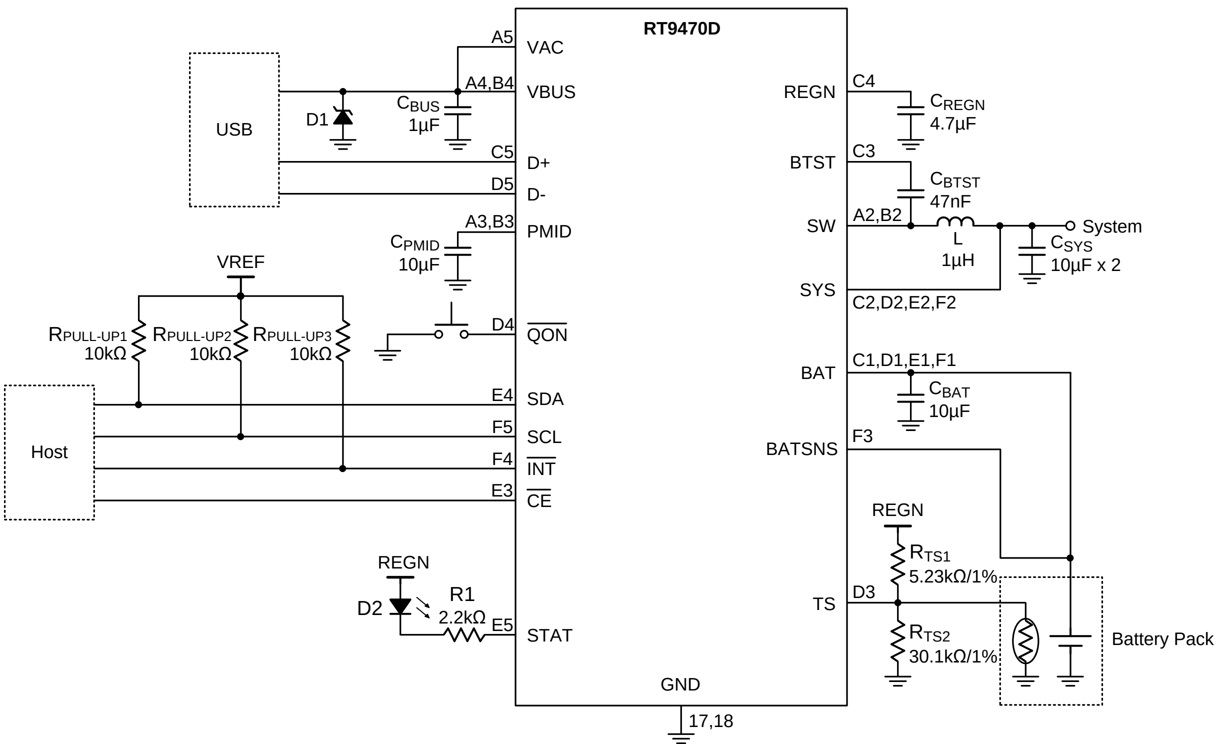
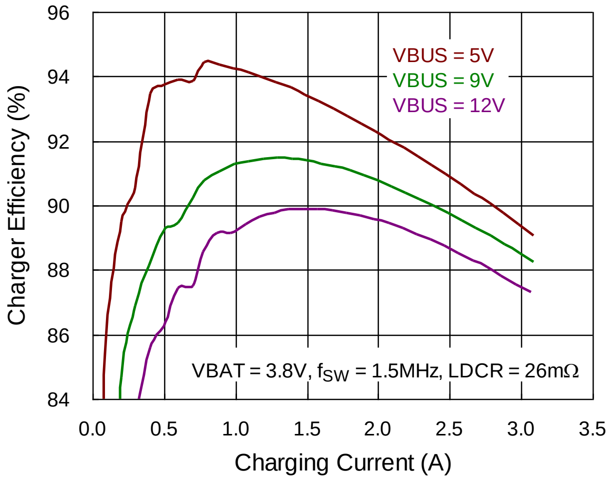


Table 1. Below are recommended components information

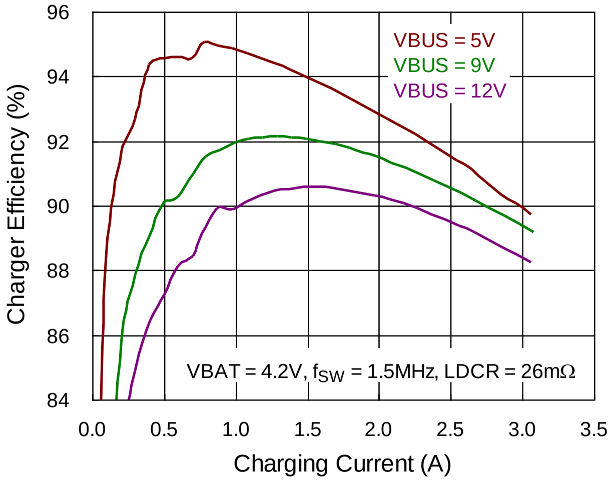
Name	Description	Part Number	Package	Manufacturer
C_{BUS}	1μF/25V/X5R	GRM155R61E105KA12	0402	muRata
C_{PMID}	10μF/25V/X5R	GRM188R61E106MA73	0603	muRata
C_{BTST}	47nF/16V/X5R	GRM033R61C473KE84	0201	muRata
C_{SYS}	10μF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
C_{BAT}	10μF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
C_{REGN}	4.7μF/6.3V/X5R	GRM155R60J475ME47	0402	muRata
L	1μH/20%	CIGT252010EH1R0MNE	2.5 x 2.0 x 1.0mm	Samsung
D1	PTVSHC3N12VU	TVS Diode	DFN2x2-3L	Prisemi

14 Typical Operating Characteristics

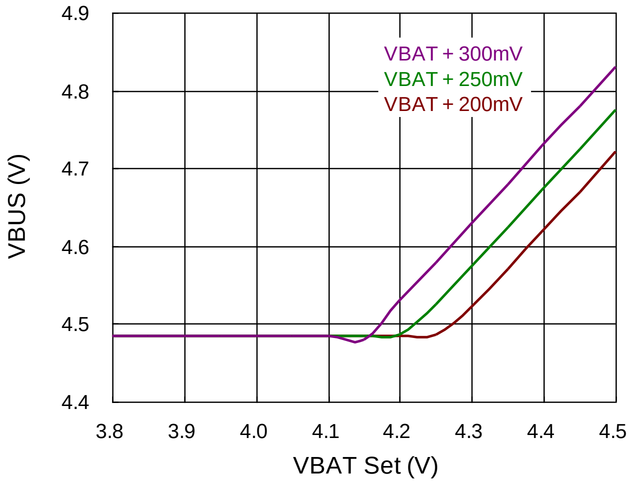
Charger Efficiency vs. Charging Current



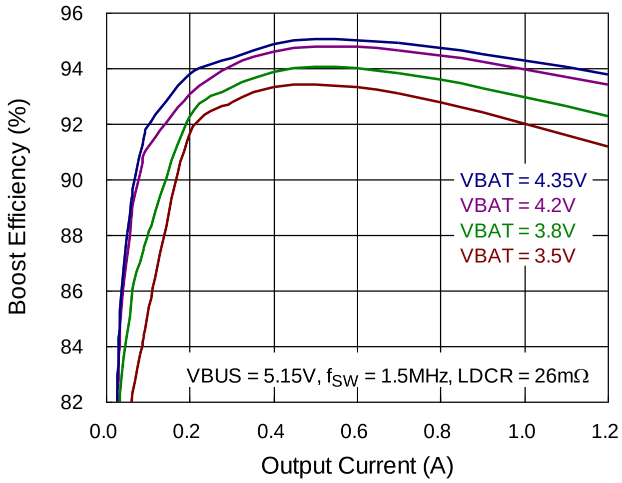
Charger Efficiency vs. Charging Current



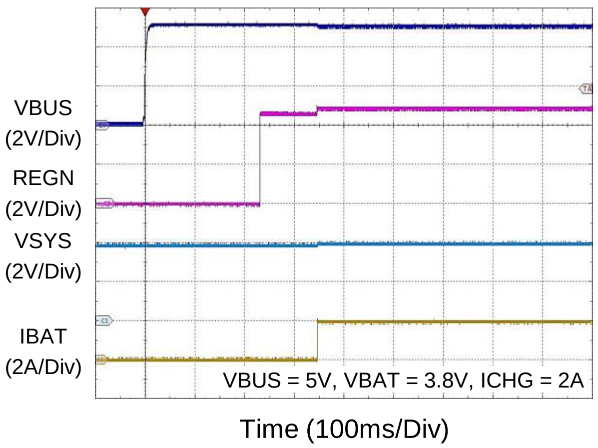
MIVR Tracking VBAT



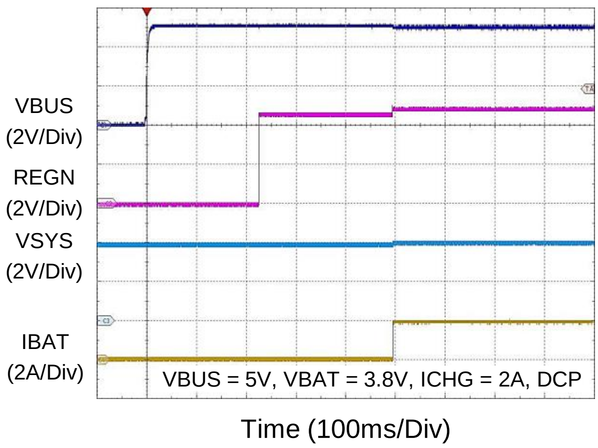
Boost Efficiency vs. Output Current



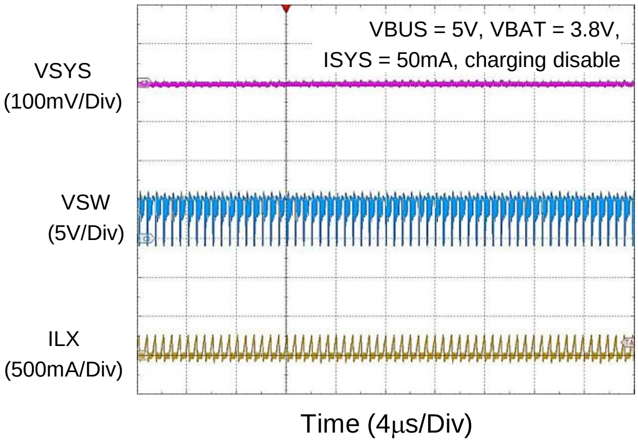
RT9470 Power-UP with VBUS Plug In



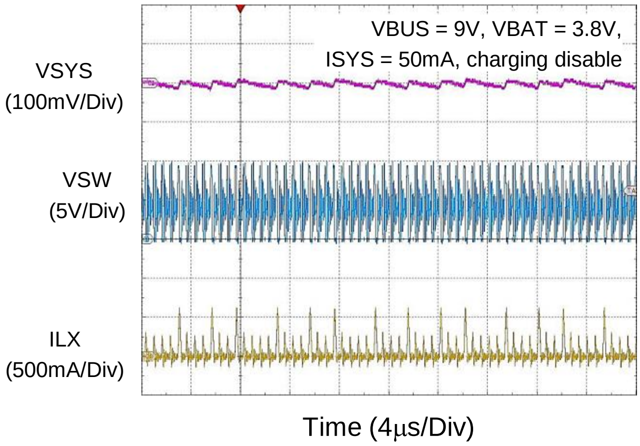
RT9470D Power-UP with VBUS Plug In



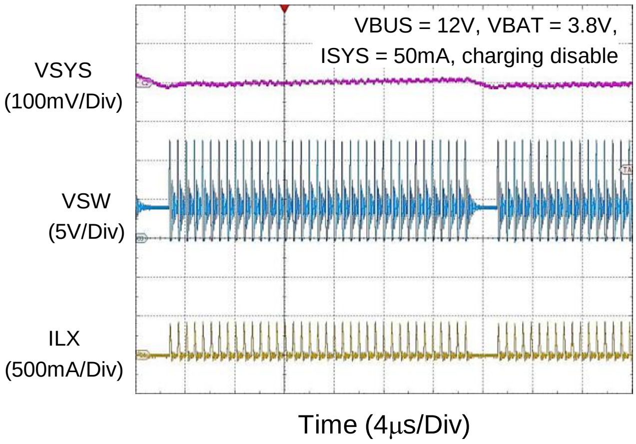
Buck Switching



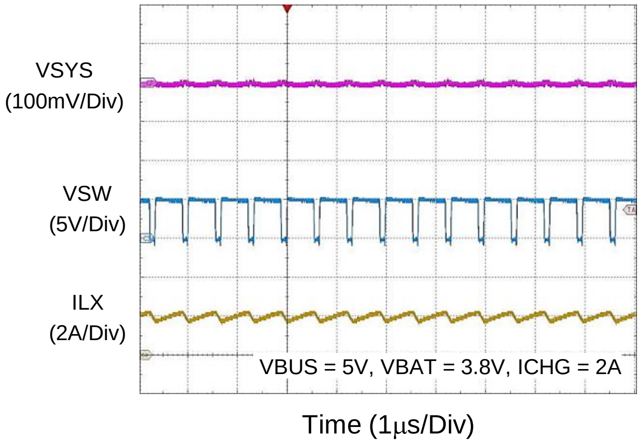
Buck Switching



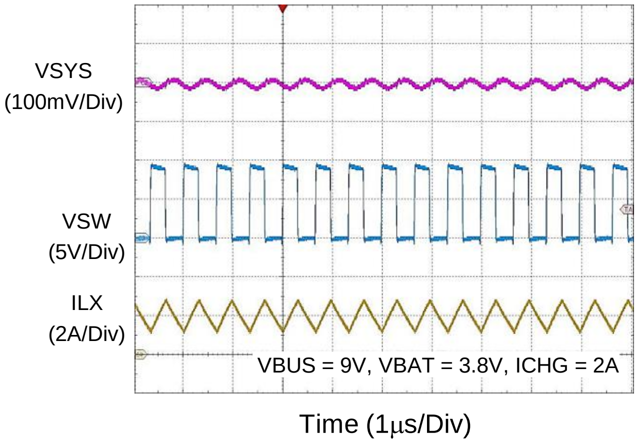
Buck Switching



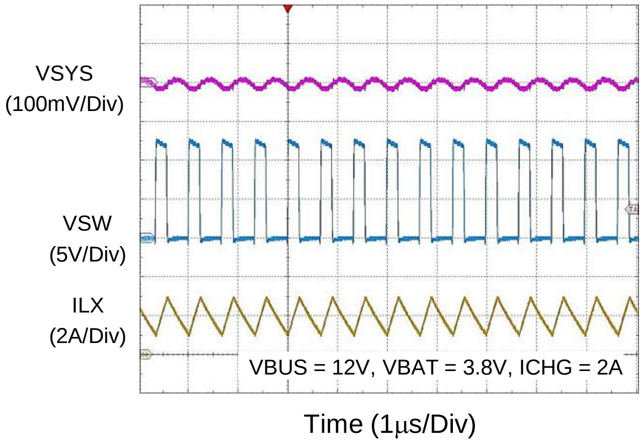
Buck Switching



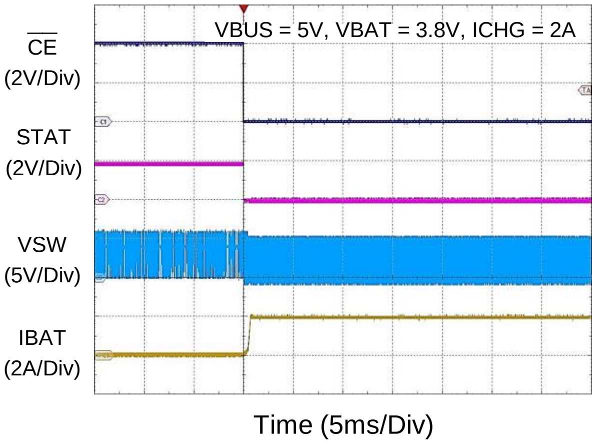
Buck Switching



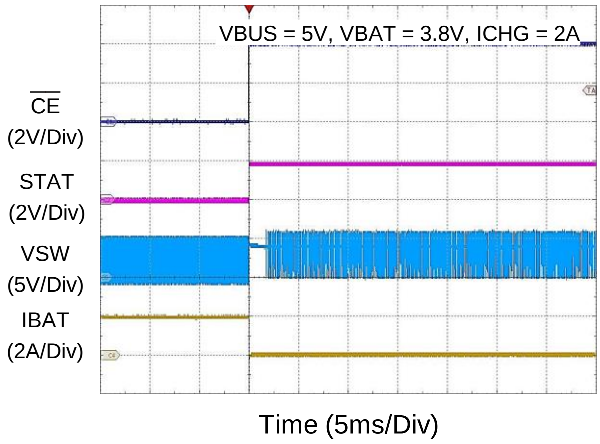
Buck Switching



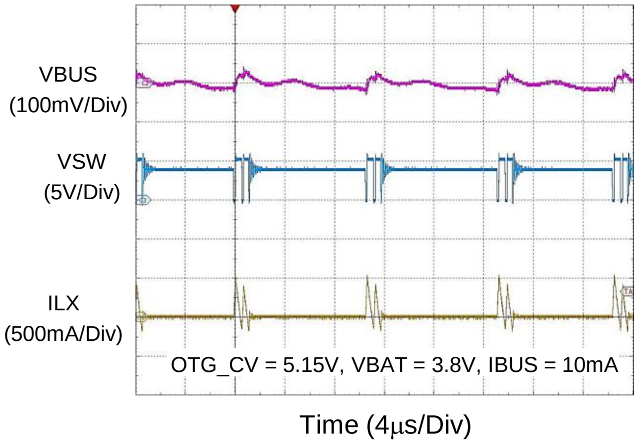
Charge Enable



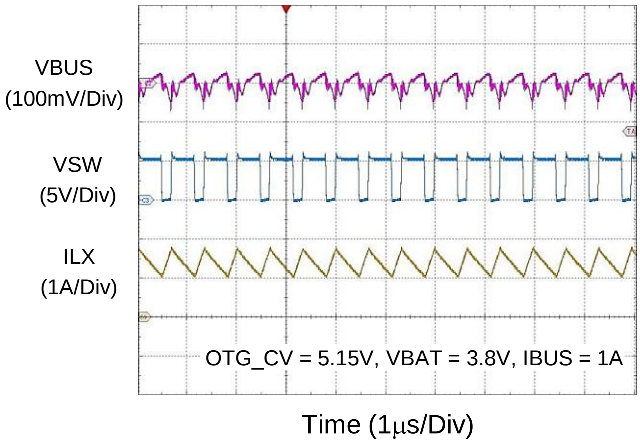
Charge Disable



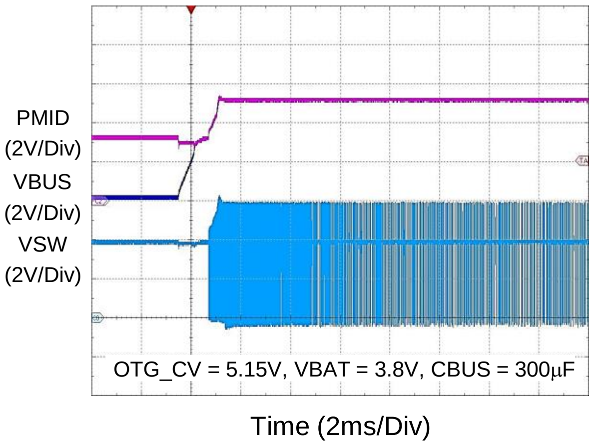
Boost Switching



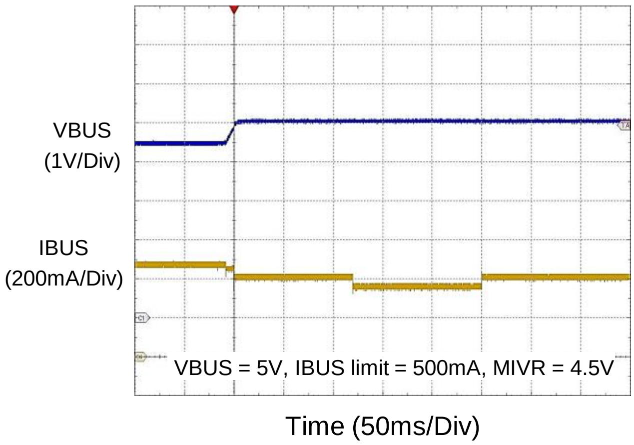
Boost Switching



Boost Start-Up



AICC Enable



15 Functional Register Description

I^2C Slave Address: 1010011 (53H)

R: Read only

R/W: Read and write

RWSC: Read and write, also automatically set/clear by a particular condition

Register Address: 0x00, Register Name: OTG_CONFIG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	OTG_CV	10	N	Y	R/W	OTG voltage limit regulation 00: 4.85V 01: 5.0V 10: 5.15V (default) 11: 5.3V
5:2	Reserved	0000	NA	NA	R	Reserved
1	OTG_LBP	0	N	Y	R/W	OTG low battery protection 0: 2.8V (default) 1: 2.5V
0	OTG_CC	1	Y	Y	R/W	OTG current limit regulation 0: 0.5A 1: 1.2A (default)

Register Address: 0x01, Register Name: TOP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	$\overline{QON}$_RST_EN	1	Y	Y	R/W	0: $\overline{QON}$ = 0 for 10s will NOT have any effect 1: $\overline{QON}$ = 0 for 10s will turn off BATFET (default)
6	STAT_EN	1	N	Y	R/W	0: The STAT pin function disabled 1: The STAT pin function enabled (default)
5:4	Reserved	00	NA	NA	R	Reserved
3	DIS_I2C_TO	0	Y	Y	R/W	0: Enable I^2C time-out function (default) 1: Disable I^2C time-out function
2	WDT_CNT_RST	0	Y	Y	RWSC	0: No action 1: Reset watchdog counter (Notice: Back to 0 after watchdog reset)
1:0	WDT	01	Y	Y	R/W	00: Disable watchdog timer reset function 01: 40s (default) 10: 80s 11: 160s

Register Address: 0x02, Register Name: FUNCTION

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	BATFET_DIS	0	N	Y	RWSC	0: Allow BATFET turn on (default) 1: Force BATFET turn off (Clear by VBUS plug in or QON = 0 for 1s, auto set BATFET_DIS = 1 by system overload from BAT to SYS)
6	BATFET_DIS_ DLY	1	N	Y	R/W	0: BATFET turn off immediately while BATFET_DIS = 0 1: BATFET turn off with 12s delay while BATFET_DIS = 1 (default)
5	HZ	0	Y	Y	RWSC	0: Normal mode (default) 1: HZ mode (Clear by VBUS plug in)
4	Reserved	0	NA	NA	R	Reserved
3	BUCK_PFM_ DIS	0	N	Y	R/W	0: Enable PFM (default) 1: Disable PFM
2	UUG_FULLON	0	N	Y	R/W	0: Q1 turns on by condition (default) 1: Force Q1 full on
1	OTG_EN	0	Y	Y	RWSC	0: Disable OTG (default) 1: Enable OTG (Clear by HZ = 1 or OTP or OTG_LBP or VBUS_OV or QON reset or BATFET_DIS = 1 or auto 7 times hiccup for soft-start failure or overload)
0	CHG_EN	1	Y	Y	R/W	0: Disable charge 1: Enable charge (default)

Register Address: 0x03, Register Name: IBUS

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	AICC_EN	0	Y	Y	RWSC	0: Disable AICC function (default) 1: Enable AICC function (Auto clear after AICC function is completed)
6	AUTO_AICR	1	Y	Y	R/W	0: No action 1: Auto set IAICR by BC1.2 done or PSEL change (default)
5:0	IAICR	001010	N	Y	RWSC	Average input current regulation 000000: 50mA 000001: 50mA 000010: 100mA … 001010: 500mA (default) … 111101: 3050mA 111110: 3100mA 111111: 3200mA (Auto set by BC1.2 done or PSEL change if AUTO_AICR = 1)

Register Address: 0x04, Register Name: VBUS

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	VAC_OVP	01	N	Y	R/W	VAC OVP threshold 00: 5.8V 01: 6.5V (default) 10: 10.9V (6.5V while OTG) 11: 14V (6.5V while OTG)
5:4	VMIVR_BAT_TRACK	00	N	Y	R/W	00: VMIVR by 0x04[3:0] (default) 01: VMIVR = VBAT + 200mV 10: VMIVR = VBAT + 250mV 11: VMIVR = VBAT + 300mV
3:0	VMIVR	0110	N	Y	R/W	Minimum input voltage regulation 0000: 3900mV 0001: 4000mV … 0110: 4500mV (default) ... 1110: 5300mV 1111: 5400mV

Register Address: 0x05, Register Name: PRECHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	R	Reserved
6:4	VPRE_CHG	100	Y	Y	R/W	Pre-charge voltage threshold 000: 2700mV 001: 2800mV 010: 2900mV 011: 3000mV 100: 3100mV (default) 101: 3200mV 110: 3300mV 111: 3400mV
3:0	IPRE_CHG	0010	Y	Y	R/W	Pre-charge current 0000: 50mA 0001: 100mA 0010: 150mA (default) ... 1110: 750mA 1111: 800mA

Register Address: 0x06, Register Name: REGU

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	Reserved	0	NA	NA	R	Reserved
6	THREG	1	Y	Y	R/W	Junction thermal regulation threshold 0: 100°C 1: 120°C (default)
5:4	Reserved	00	NA	NA	R	Reserved
3:0	VSYS_MIN	1001	N	Y	R/W	System minimum voltage 0000: 2600mV 0001: 2700mV … 1001: 3500mV (default) ... 1110: 4000mV 1111: 4100mV

Register Address: 0x07, Register Name: VCHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	VRE_CHG	0	Y	Y	R/W	Re-charge voltage threshold 0: 100mV (default) 1: 200mV
6:0	VBAT_REG	0011110	Y	Y	R/W	Charge voltage 0000000: 3900mV 0000001: 3910mV … 0011110: 4200mV (default) … 1010000: 4700mV 1010000 to 1111111: 4700mV

Register Address: 0x08, Register Name: ICHG

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:6	Reserved	00	NA	NA	R	Reserved
5:0	ICHG_REG	101000	Y	Y	R/W	Charge current 000000: 0mA (disable charge) 000001: 50mA 000010: 100mA 000011: 150mA … 101000: 2000mA (default) … 111101: 3100mA 111111: 3150mA

Register Address: 0x09, Register Name: CHG_TIMER

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	CHG_SAFE_TMR_EN	1	Y	Y	R/W	0: Disable charge safe timer 1: Enable charge safe timer (default)
6	CHG_SAFE_TMR_2XT	1	Y	Y	R/W	Double the charge safe timer during MIVR, AICR, thermal regulation, and JEITA to reduce ICHG 0: Disable 2x extended charge safe timer 1: Enable 2x extended charge safe timer (default)
5:4	CHG_SAFE_TMR	01	Y	Y	R/W	Charge safe timer 00: 5hr 01: 10hr (default) 10: 15hr 11: 20hr
3:0	Reserved	0000	NA	NA	R	Reserved

Register Address: 0x0A, Register Name: EOC

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	IEOC_CHG	0011	Y	Y	R/W	End-of-charge current threshold 0000: 50mA 0001: 100mA 0010: 150mA 0011: 200mA (default) ... 1110: 750mA 1111: 800mA
3:2	BG_CHG_TMR	00	Y	Y	R/W	EOC back-ground charge timer 00: 0min (default) 01: 15min 10: 30min 11: 45min
1	TE	1	Y	Y	R/W	0: Disable charge current termination 1: Enable charge current termination (default)
0	EOC_RST	0	Y	Y	RWSC	0: No action 1: Reset EOC (Notice: Back to 0 after reset EOC done)

Register Address: 0x0B, Register Name: INFO

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	REG_RST	0	NA	NA	RWSC	0: No action 1: Reset register (Notice: Back to 0 after register reset)
6:3	DEVICE_ID	1001	NA	NA	R	1001: RT9470 (PSEL, PGB) 1010: RT9470D (D+, D-)
2:0	DEVICE_RE	NA	NA	NA	R	Revision

Register Address: 0x0C, Register Name: JEITA

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	JEITA_EN	1	Y	Y	R/W	0: JEITA disabled 1: JEITA enabled (default)
6	JEITA_COLD	0	Y	Y	R/W	0: COLD do NOT charging/OTG (default) 1: COLD still charging/OTG
5	JEITA_COOL_ISET	1	Y	Y	R/W	0: 50% of I_{CHG} 1: 25% of I_{CHG} (default)
4	JEITA_COOL_VSET	1	Y	Y	R/W	0: V_{BAT_REG} = 4.1V 1: V_{BAT_REG} = Register setting (default)
3	JEITA_WARM_ISET	1	Y	Y	R/W	0: 50% of I_{CHG} 1: I_{CHG} = Register setting (default)
2	JEITA_WARM_VSET	0	Y	Y	R/W	0: V_{BAT_REG} = 4.1V (default) 1: V_{BAT_REG} = Register setting
1	JEITA_HOT	0	Y	Y	R/W	0: HOT do NOT charging/OTG (default) 1: HOT still charging/OTG
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x0D, Register Name: PUMP_EXP

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	PE_EN	0	Y	Y	RWSC	0: Idle (default) 1: Trigger MTK Pump Express process (Auto clear while PE is done or no VBUS)
6	PE_SEL	0	Y	Y	R/W	0: PE 1.0 process select (default) 1: PE 2.0 process select
5	PE10_INC	0	Y	Y	R/W	0: PE 1.0 voltage down (default) 1: PE 1.0 voltage up
4:0	PE20_CODE	00000	Y	Y	R/W	MTK PE 2.0 voltage request setting 00000: 5.5V (default) 00001: 6V … 11101: 20V 11110: Adapter healthy self-testing 11111: Disable cable drop compensation

Register Address: 0x0E, Register Name: DPDM_DET

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	BC12_EN	1	Y	Y	R/W	0: Disable BC1.2 detection 1: Enable BC1.2 detection while VBUS > 3.8V (default) (For the RT9470D only)
6:5	DCDT_SEL	01	Y	Y	R/W	00: Disable DCD timeout function 01: Enable 300ms DCD timeout function (default) 10: Enable 600ms DCD timeout function 11: Wait data contact
4	SPEC_TA_EN	1	Y	Y	R/W	0: Disable Samsung/Apple TA detection 1: Enable Samsung/Apple TA detection (default)
3:1	Reserved	000	NA	NA	R	Reserved
0	DCP_DP_OPT	0	Y	Y	R/W	DCP DP behavior option 0: DP = 0V after BC 1.2 done (default) 1: DP keep 0.6V while DCP port detected

Register Address: 0x0F, Register Name: IC_STATUS

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7:4	PORT_STAT	0000	NA	NA	R	0000: No information 0001 to 0111: Reserved 1000: VBUS = device 1 (2100mA-APPLE-10w) 1001: VBUS = device 2 (2000mA-SAMSUNG-10w) 1010: VBUS = device 3 (1000mA-APPLE-5w) 1011: VBUS = device 4 (2400mA-APPLE-12w) 1100: VBUS = unknown/NSDP (500mA) 1101: VBUS = SDP (500mA)/PSEL = High 1110: VBUS = CDP (1500mA) 1111: VBUS = DCP (2400mA)/PSEL = Low
3:0	IC_STAT	0000	NA	NA	R	0000: HZ/SLEEP 0001: VBUS ready for charge 0010: Trickle-charge 0011: Pre-charge 0100: Fast-charge 0101: IEOC-charge (EOC and TE = 0) 0110: Back-Ground charge (EOC and TE = 1 and before turning off power path) 0111: Charge done (EOC and TE = 1 and power path off) 1000: Charge fault (VAC_OV/CHG_BUSUV/CHG_TOUT/CHG_SYSOV/CHG_BATOV/JEITA_HOT/JEITA_COLD/OTP) 1001 to 1110: Reserved 1111: OTG

Register Address: 0x10, Register Name: STAT0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_VBUS_GD	0	NA	NA	R	0: VBUS is not good 1: VBUS is good (Notice: After current capability of the input source detection, and HZ = 0, VAC_OV = 0, and VBUS > 3.8V)
6	ST_CHG_RDY	0	NA	NA	R	0: VBUS is not ready for charging 1: VBUS is ready for charging (Notice: After port detection, and HZ = 0, VAC_OV = 0, and VBUS > 3.8V)
5	ST_IEOC	0	NA	NA	R	0: Not in EOC state 1: While in EOC state (Charge current < IEOC level)
4	ST_BG_CHG	0	NA	NA	R	0: Not in EOC state or TE = 0 or BG_CHG_TMR = 00 1: While in EOC state and TE = 1 and BG_CHG_TMR ≠ 00
3	ST_CHG_DONE	0	NA	NA	R	0: Not in EOC state or BATFET on 1: While in EOC state and BATFET off
2:1	Reserved	00	NA	NA	R	Reserved
0	ST_BC12_DONE	0	NA	NA	R	0: BC1.2 process is not ready 1: While BC1.2 process is done

Register Address: 0x11, Register Name: STAT1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_CHG_MIVR	0	NA	NA	R	0: Not in MIVR loop 1: While in MIVR loop
6	ST_CHG_AICR	0	NA	NA	R	0: Not in AICR loop 1: While in AICR loop
5	ST_CHG_THREG	0	NA	NA	R	0: Not in THERMAL loop 1: While in THERMAL loop
4	ST_CHG_BUSUV	0	NA	NA	R	0: Not VBAT < VBUS < 3.8V 1: While VBAT < VBUS < 3.8V
3	ST_CHG_TOUT	0	NA	NA	R	0: Not in charge safety time-out 1: While in charge safety time-out
2	ST_CHG_SYSOV	0	NA	NA	R	0: Not in SYS OV 1: While in SYS OV
1	ST_CHG_BATOV	0	NA	NA	R	0: Not in BAT OV 1: While in BAT OV
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x12, Register Name: STAT2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_JEITA_ HOT	0	NA	NA	R	0: Not in BAT is hot 1: While in BAT is hot
6	ST_JEITA_ WARM	0	NA	NA	R	0: Not in BAT is warm 1: While in BAT is warm
5	ST_JEITA_ COOL	0	NA	NA	R	0: Not in BAT is cool 1: While in BAT is cool
4	ST_JEITA_ COLD	0	NA	NA	R	0: Not in BAT is cold 1: While in BAT is cold
3:2	Reserved	00	NA	NA	R	Reserved
1	ST_SYS_MIN	0	NA	NA	R	0: Not in VBAT < VSYS_MIN 1: While in VBAT < VSYS_MIN
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x13, Register Name: STAT3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	ST_OTP	0	NA	NA	R	0: Not OTP 1: OTP
6	ST_VAC_OV	0	NA	NA	R	0: Not VAC_OV 1: VAC_OV (charge or OTG mode)
5	ST_WDT	0	NA	NA	R	0: WDT is counting 1: WDT reset will occur after 500ms
4:3	Reserved	00	NA	NA	R	Reserved
2	ST_OTG_CC	0	NA	NA	R	0: Not in OTG_CC 1: While in OTG_CC
1:0	Reserved	00	NA	NA	R	Reserved

Register Address: 0x20, Register Name: IRQ0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_VBUS_GD	0	NA	NA	R	0: ST_VBUS_GD not rising 1: While ST_VBUS_GD is rising, read clear
6	FL_CHG_RDY	0	NA	NA	R	0: ST_CHG_RDY not rising 1: While ST_CHG_RDY is rising, read clear
5	FL_IEOC	0	NA	NA	R	0: ST_IEOC not rising 1: While ST_IEOC is rising, read clear
4	FL_BG_CHG	0	NA	NA	R	0: ST_BG_CHG not rising 1: While ST_BG_CHG is rising, read clear
3	FL_CHG_DONE	0	NA	NA	R	0: ST_CHG_DONE not rising 1: While ST_CHG_DONE is rising, read clear
2	FL_RECHG	0	NA	NA	R	0: While VBAT > VRECHG after EOC 1: While VBAT < VRECHG after EOC, read clear
1	FL_DETACH	0	NA	NA	R	0: ST_VBUS_GD not rising or in ST_VBUS_GD 1: While ST_VBUS_GD is falling then VBUS < VBAT or VBUS < 3.3V, read clear
0	FL_BC12_DONE	0	NA	NA	R	0: BC1.2 process is not ready 1: While BC1.2 process is done

Register Address: 0x21, Register Name: IRQ1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_CHG_MIVR	0	NA	NA	R	0: ST_CHG_MIVR not rising 1: While ST_CHG_MIVR is rising, read clear
6	FL_CHG_AICR	0	NA	NA	R	0: ST_CHG_AICR not rising 1: While ST_CHG_AICR is rising, read clear
5	FL_CHG_THREG	0	NA	NA	R	0: ST_CHG_THREG not rising 1: While ST_CHG_THREG is rising, read clear
4	FL_CHG_BUSUV	0	NA	NA	R	0: ST_CHG_BUSUV not rising 1: While ST_CHG_BUSUV is rising, read clear
3	FL_CHG_TOUT	0	NA	NA	R	0: ST_CHG_TOUT not rising 1: While ST_CHG_TOUT is rising, read clear
2	FL_CHG_SYSOV	0	NA	NA	R	0: ST_CHG_SYSOV not rising 1: While ST_CHG_SYSOV is rising, read clear
1	FL_CHG_BATOV	0	NA	NA	R	0: ST_CHG_BATOV not rising 1: While ST_CHG_BATOV is rising, read clear
0	Reserved	0	NA	NA	R	Reserved

Register Address: 0x22, Register Name: IRQ2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_JEITA_HOT	0	NA	NA	R	0: ST_JEITA_HOT not rising 1: While ST_JEITA_HOT is rising, read clear
6	FL_JEITA_WARM	0	NA	NA	R	0: ST_JEITA_WARM not rising 1: While ST_JEITA_WARM is rising, read clear
5	FL_JEITA_COOL	0	NA	NA	R	0: ST_JEITA_COOL not rising 1: While ST_JEITA_COOL is rising, read clear
4	FL_JEITA_COLD	0	NA	NA	R	0: ST_JEITA_COLD not rising 1: While ST_JEITA_COLD is rising, read clear
3	FL_PE_DONE	0	NA	NA	R	0: FL_PE_DONE not rising 1: While PE processing is done, read clear
2	FL_AICC_DONE	0	NA	NA	R	0: FL_AICC_DONE not rising 1: While AICC processing is done, read clear
1	FL_SYS_MIN	0	NA	NA	R	0: ST_SYS_MIN not rising 1: While ST_SYS_MIN is rising, read clear
0	FL_SYS_SHORT	0	NA	NA	R	0: ST_SYS_SHORT not rising 1: While ST_SYS_SHORT is rising, read clear

Register Address: 0x23, Register Name: IRQ3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	FL_OTP	0	NA	NA	R	0: ST_OTP not rising 1: While ST_OTP is rising, read clear
6	FL_VAC_OV	0	NA	NA	R	0: ST_VAC_OV not rising 1: While ST_VAC_OV is rising, read clear
5	FL_WDT	0	NA	NA	R	0: ST_WDT not rising 1: While ST_WDT is rising, read clear
4:3	Reserved	00	NA	NA	R	Reserved
2	FL_OTG_CC	0	NA	NA	R	0: ST_OTG_CC not rising 1: While ST_OTG_CC is rising, read clear
1	FL_OTG_LBP	0	NA	NA	R	0: ST_OTG_LBP not rising 1: While ST_OTG_LBP is rising, read clear
0	FL_OTG_FAULT	0	NA	NA	R	0: ST_OTG_FAULT not rising 1: While ST_OTG_FAULT is rising, read clear

Register Address: 0x30, Register Name: MASK0

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_VBUS_GD	1	N	Y	R/W	0: Not mask IRQ of FL_VBUS_GD 1: Mask IRQ of FL_VBUS_GD (default)
6	MK_CHG_RDY	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_RDY 1: Mask IRQ of FL_CHG_RDY (default)
5	MK_IEOC	1	N	Y	R/W	0: Not mask IRQ of FL_IEOC 1: Mask IRQ of FL_IEOC (default)
4	MK_BG_CHG	1	N	Y	R/W	0: Not mask IRQ of MK_BG_CHG 1: Mask IRQ of MK_BG_CHG (default)
3	MK_CHG_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_DONE 1: Mask IRQ of FL_CHG_DONE (default)
2	MK_RECHG	1	N	Y	R/W	0: Not mask IRQ of FL_RECHG 1: Mask IRQ of FL_RECHG (default)
1	MK_DETACH	1	N	Y	R/W	0: Not mask IRQ of FL_DETACH 1: Mask IRQ of FL_DETACH (default)
0	MK_BC12_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_BC12_DONE 1: Mask IRQ of FL_BC12_DONE (default)

Register Address: 0x31, Register Name: MASK1

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_CHG_MIVR	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_MIVR 1: Mask IRQ of FL_CHG_MIVR (default)
6	MK_CHG_AICR	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_AICR 1: Mask IRQ of FL_CHG_AICR (default)
5	MK_CHG_THREG	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_THREG 1: Mask IRQ of FL_CHG_THREG (default)
4	MK_CHG_BUSUV	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_BUSUV 1: Mask IRQ of FL_CHG_BUSUV (default)
3	MK_CHG_TOUT	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_TOUT 1: Mask IRQ of FL_CHG_TOUT (default)
2	MK_CHG_SYSOV	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_SYSOV 1: Mask IRQ of FL_CHG_SYSOV (default)
1	MK_CHG_BATOV	1	N	Y	R/W	0: Not mask IRQ of FL_CHG_BATOV 1: Mask IRQ of FL_CHG_BATOV (default)
0	Reserved	1	NA	NA	R	Reserved

Register Address: 0x32, Register Name: MASK2

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_JEITA_HOT	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_HOT 1: Mask IRQ of FL_JEITA_HOT (default)
6	MK_JEITA_WARM	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_WARM 1: Mask IRQ of FL_JEITA_WARM (default)
5	MK_JEITA_COOL	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_COOL 1: Mask IRQ of FL_JEITA_COOL (default)
4	MK_JEITA_COLD	1	N	Y	R/W	0: Not mask IRQ of FL_JEITA_COLD 1: Mask IRQ of FL_JEITA_COLD (default)
3	MK_PE_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_PE_DONE 1: Mask IRQ of FL_PE_DONE (default)
2	MK_AICC_DONE	1	N	Y	R/W	0: Not mask IRQ of FL_AICC_DONE 1: Mask IRQ of FL_AICC_DONE (default)
1	MK_SYS_MIN	1	N	Y	R/W	0: Not mask IRQ of FL_SYS_MIN 1: Mask IRQ of FL_SYS_MIN (default)
0	MK_SYS_SHORT	1	N	Y	R/W	0: Not mask IRQ of FL_SYS_SHORT 1: Mask IRQ of FL_SYS_SHORT (default)

Register Address: 0x33, Register Name: IRQ3

Bit	Bit Name	Default	WDT RST	REG RST	Type	Description
7	MK_OTP	1	N	Y	R/W	0: Not mask IRQ of FL_OTP 1: Mask IRQ of FL_OTP (default)
6	MK_VAC_OV	1	N	Y	R/W	0: Not mask IRQ of FL_VAC_OV 1: Mask IRQ of FL_VAC_OV (default)
5	MK_WDT	1	N	Y	R/W	0: Not mask IRQ of FL_WDT 1: Mask IRQ of FL_WDT (default)
4:3	Reserved	11	NA	NA	R	Reserved
2	MK_OTG_CC	1	N	Y	R/W	0: Not mask IRQ of FL_OTG_CC 1: Mask IRQ of FL_OTG_CC (default)
1	MK_OTG_LBP	1	N	Y	R/W	0: Not mask IRQ of FL_OTG_LBP 1: Mask IRQ of FL_OTG_LBP (default)
0	MK_OTG_FAULT	1	N	Y	R/W	0: Not mask IRQ of FL_OTG_FAULT 1: Mask IRQ of FL_OTG_FAULT (default)

16 Application Information

(Note 7)

16.1 Power Up

16.1.1 Power-On-Reset (POR)

Upon power-up, the device initiates its internal bias circuits using the higher of two voltage sources: VBUS or VBAT. The Power-On-Reset sequence begins when VBUS exceeds 1.8V, or when VBAT rises above V_{BAT_UVLO}. Following this, the I^2C interface becomes operational, enabling communication. Simultaneously, all registers are reset to the default values.

16.1.2 Device Power Up from Battery Only

When a battery is connected and the voltage at VBAT exceeds the threshold $V_{BAT\_DPL\_RISE}$, the BATFET is activated, connecting VBAT to VSYS. The REGN stays off to minimize the quiescent current. The low quiescent current on VBAT and the low $R_{DS(ON)}$ of the BATFET reduce the device power consumption and conduction losses, thereby extending the battery life.

The device continuously monitors the discharge current passing through the BATFET in Battery Supply Mode. If the system experiences an overload or a short circuit condition (I_{BAT} > I_{BATFET_OCP}), the device immediately deactivates the BATFET and sets BATFET_DIS = 1. This action initiates Shipping Mode, which persists until VBUS is reconnected or specific procedures are followed to exit Shipping Mode to reactivate the BATFET.

16.1.3 Device Power Up from VBUS

When VBUS is connected, the device initiates the power-up sequence as follows:

1. Activate the REGN LDO.
2. Initiate Poor Source Detection.
3. Determine PORT_STAT based on PSEL or the type of input source, and configure the default setting of the Average Input Current Regulation (AICR) register.
4. Set the Minimum Input Voltage Regulation (MIVR) setting.
5. Engage the Buck Converter.

16.1.4 Power-Up REGN LDO

The REGN LDO provides power to the gate drives of both high-side and low-side MOSFETs. Additionally, it supplies bias to the external TS resistor and the pull-up rail for the STAT pin. The REGN is activated under the following conditions:

1. VAC exceeds VBAT + V_{SLEEP_RISE} in buck mode, or the OTG bit is set in boost mode.
2. After a delay of 220ms, V_{AC} remains above VBAT + V_{SLEEP_RISE}.
3. The REGN LDO is deactivated when the device enters HZ mode, sleep mode, experiences VBUS overvoltage, or when OTG is disabled.

16.1.5 Poor Source Detection

After REGN is powered up, the device evaluates the current capability of the input source. The input source must meet the following requirements to enable the buck converter.

1. VBUS must be below the VAC_OVP_RISE threshold.
2. VBUS must be above the VBUS_BAD_ADP threshold, which then triggers the device to pull I_{BADSRC} (typical = 40mA).

When the input source satisfies these conditions, the ST_VBUS_GD and the FL_VBUS_GD signals go high, and the device generates a pulse on the $\overline{INT}$ pin to trigger an interrupt on the host. If ST_VBUS_GD does not go high, the device will retry the poor source detection process every 2 seconds.

16.1.6 VBUS Source Type Detection

After ST_VBUS_GD goes high, the device initiates VBUS source type detection (for the RT9470D) or checks the status of the PSEL pin (for the RT9470). After the detection process is completed, both ST_CHG_RDY and FL_CHG_RDY signals turn to high, and the $\overline{INT}$ pin pulsed to interrupt the host system.

Then the following registers are changed:

1. The Average Input Current Regulation (AICR) register is automatically changed to the result of the VBUS source type detection or the PSEL pin status, provided that AUTO_AICR = 1.
2. The PORT_STAT bit is revised to indicate the detected VBUS source type.

16.1.7 Average Input Current Regulation (AICR)

The charger input current is limited by the AICR register with a range from 50mA to 3.2A and a resolution 50mA.

1. If the AUTO_AICR bit is set to 0, the device cannot adjust the AICR value automatically after detecting the VBUS source type.
2. The host can overwrite the AICR register to set a new input current limit.
3. For the RT9470, the PSEL value updates the AICR settings. In the RT9470D, the AICR is updated according to Table 2 or based on D+/D- line detection (including standard USB BC 1.2). Refer to Table 3.
4. In the RT9470, the AICR is updated in real-time with changes to the PSEL value.
5. In the RT9470D, the AICR is updated by the D+/D- detection value after BC12_EN is disabled and then re-enabled, or when VBUS is reconnected.

Table 2. AICR Setting from PSEL

PSEL pin	AICR setting	PORT_STAT
High	0.5 A	1101
Low	2.4 A	1111

Table 3. AICR Setting from D+/D- Detection

Detection	AICR setting	PORT_STAT
Device 1	2.1A	1000
Device 2	2A	1001
Device 3	1A	1010
Device 4	2.4A	1011
Unknown/NSDP	0.5A	1100
SDP	0.5A	1101
CDP	1.5A	1110
DCP	2.4A	1111

16.1.8 Minimum Input Voltage Regulation (MIVR)

The MIVR function is designed to prevent input voltage drops that occur when the input power source cannot provide sufficient current. The VBUS voltage decreases to the level set by the VMIVR setting level when an overcurrent condition arises from the input power source. The default value of the VMIVR register is 4.5V. The value can be adjusted via the I^2C interface, with a range from 3.9V to 5.4V in increments of 0.1V. Additionally, the device provides a MIVR tracking function that can be enabled through the VMIVR_BAT_TRACK register bits. When this tracking function is enabled, the MIVR will be set to the higher between the VMIVR register setting and the VBAT+VMIVR_BAT_TRACK offset.

16.1.9 Buck Converter Power-Up

After the AICR is set, the converter is enabled, initiating the switching process. BATFET remains active unless the charger is disabled (CHG_EN = 0) or the device enters shipping mode (BATFET_DIS = 1).

The device integrates a synchronous PWM controller with a 1.5MHz switching frequency for high-accuracy current and voltage regulation. Additionally, the device supports PFM control to enhance efficiency under light-load conditions. The BUCK_PFM_DIS register bit allows users to disable PFM operation in the buck converter configuration.

16.1.10 Boost Mode Operation (OTG)

The device supports OTG (On-The-Go) mode by utilizing a boost converter to facilitate power delivery from the battery to other portable devices. The maximum output current in boost mode is 1.2A, which satisfies the USB OTG requirement of 500mA.

The boost operation can be enabled by the following conditions:

1. VBAT must be above the VOTG_LBP threshold.
2. VBUS must be less than VBAT + V_{SLEEP_FALL} value.
3. OTG_EN must be set to high.
4. The voltage at the TS pin must be within the acceptable range, specifically V_{VTS_HOT} < VTS < V_{VTS_COLD}.
5. A 30ms delay must pass after setting OTG_EN to high before the boost converter powers up.

In boost mode, the IC_STAT register bits are updated to 1111, the VBUS output voltage is 5.15V, and the output limit current is 1.2A by default. Both the output voltage (OTG_CV) and the output current limit (OTG_CC) can be configured via I^2C. The boost output remains active as long as VBAT stays above the V_{OTG_LBP} threshold.

16.2 Watchdog Timer (WDT)

When the device is controlled by the host, most of the registers can be programmed by the host. The host must write WDT_CNT_RST = 1 to reset the counter before the watchdog timeout, and it can also disable the WDT function by setting the WDT bits to 00.

When the watchdog timer expires, ST_WDT and FL_WDT go high, and the $\overline{\text{INT}}$ pin is pulsed to interrupt the host. After a delay of 512ms, the related registers are reset to their default values. (refer to Register Descriptions for details). If the device is in a watchdog timeout status, the host can write to any registers or set WDT_CNT_RST = 1 to reset the counter.

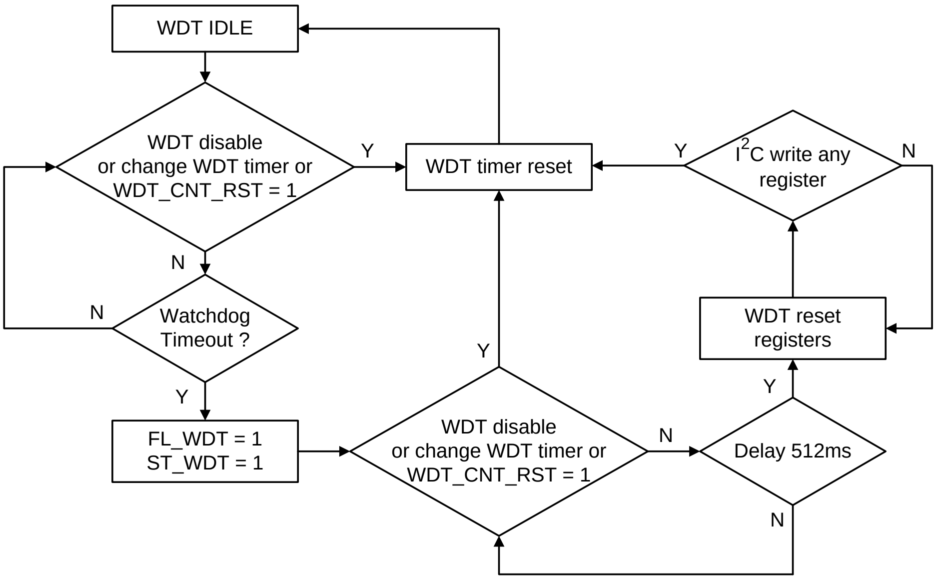


Figure 1. WDT Flow Chart

16.3 Power Path Management

The device provides an automatic power path selection mechanism that enables the system power supply (VSYS) to be sourced from either VBUS, VBAT (battery), or both.

16.3.1 Entering Shipping Mode (BATFET Disable)

To extend the battery life during shipping or storage, the device can disable BATFET to minimize the battery leakage current. The host can configure the BATFET_DIS bit to disable BATFET immediately, or set the BATFET_DIS_DLY bit to introduce a delay $t_{SHIP\_MODE\_ENTER}$ before disabling the BATFET.

16.3.2 Exiting Shipping Mode (BATFET Enable)

When the device is in shipping mode, one of the following methods can be used to exit shipping mode and restore power to the system:

1. Connect VBUS.
2. Set the BATFET_DIS bit to 0.
3. Set the REG_RST bit to reset all registers to their default values.
4. Activate the $\overline{\text{QON}}$ pin by transitioning it from high to low for a duration exceeding $t_{SHIPMODE\_EXIT}$.

16.3.3 $\overline{\text{QON}}$ Pin Operations

The $\overline{\text{QON}}$ pin serves two functions to control BATFET.

1. BATFET Enable: Transitioning the $\overline{\text{QON}}$ pin from high to low for a duration exceeding the $t_{SHIPMODE\_EXIT}$ deglitch time threshold will turn on BATFET, allowing the device to exit shipping mode.
2. SYSTEM Reset: If the $\overline{\text{QON}}$ pin transitions from high to low for a duration exceeding the t_{QON_RST} deglitch time threshold, and if VBUS is not connected, BATFET is turned off for t_{BATFET_RST}. Subsequently, BATFET is re-enabled. This functionality allows the system connected to VSYS to perform a power-on reset. This feature can be deactivated by setting the QON_RST_EN bit to 0.

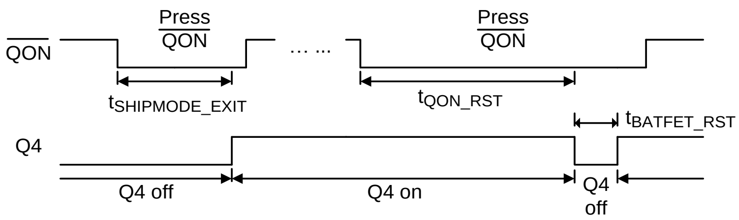


Figure 2. $\overline{\text{QON}}$ Timing

16.4 Battery Charging Management

The device supports a maximum charge current of 3.15A and incorporates an 18mΩ BATFET to enhance charging efficiency and reduce voltage drop during battery discharge.

16.4.1 Charging Cycle

When battery charging is enabled (the $\overline{\text{CE}}$ pin is set to low and CHG_EN = 1), the device autonomously completes a charging cycle without host controls. The default parameters for the device are detailed in Table 4. Additionally, the host can modify the charging parameters via I^2C.

Table 4. Default Charging Parameters

Default Mode	RT9470/D
Charging Voltage	4.2V
Charging Current	2A
Pre-Charge Current	150mA
End of Charge (EOC) Current	200mA
Temperature Profile	JEITA
Fast Charge Safety Timer	10 Hours

A charging cycle starts with the following conditions:

1. The buck converter initiates operation.
2. Battery charging is enabled ($\overline{\text{CE}}$ pin is low, CHG_EN = 1, and ICHG_REG is not 0mA).
3. There are no thermal faults detected on TS.
4. There is no safety timer fault.
5. BATFET is active (BATFET_DIS = 0).

The charger reaches the end-of-charge status when the charging current falls below the EOC current threshold, the battery voltage exceeds the recharge voltage threshold, and the device is not in AICR, MIVR, or thermal regulation.

If the battery voltage drops below the recharge threshold (threshold setting through the VRE_CHG register bits), the device automatically initiates a new charging cycle. Once charging is complete, a new charging cycle can be started by toggling either the $\overline{CE}$ pin or the CHG_EN bit.

16.4.2 Battery Charging Profile

The device charges the battery in five statuses: trickle charge, pre-charge, constant current, constant voltage and back-ground charge (optional).

Table 5. Charging Current Setting

Current Parameter	Default Current Setting	IC_STAT
$I_{TRICKLE\_CHG}$	100mA	0010
I_{PRE_CHG}	150mA	0011
I_{CHG_REG}	2A	0100
I_{EOC_CHG}	200mA	0111

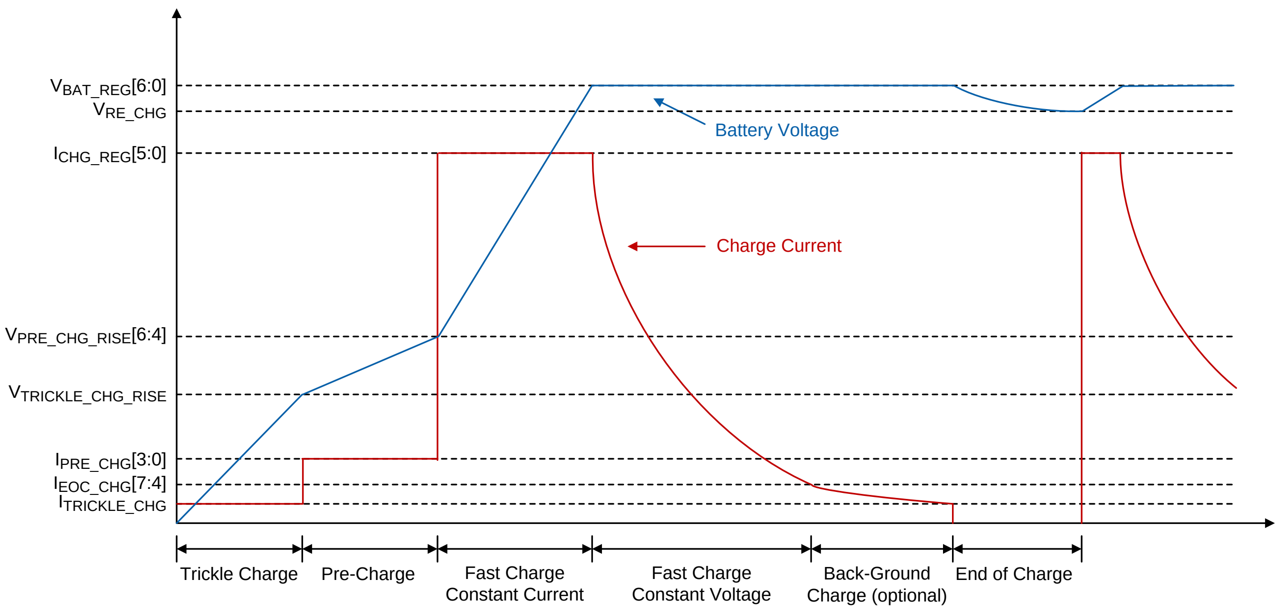


Figure 3. Charging Profile

16.4.3 End of Charge (EOC)

The charger enters the end of charge status when the battery voltage exceeds the recharge threshold and the charge current falls below I_{EOC_CHG}. The I_{EOC_CHG} can be set within a range from 50mA to 800mA in increments of 50mA. Upon reaching EOC, the BATFET is turned off with TE = 1 and BG_CHG_TMR = 00. Meanwhile, the buck converter continues to switch, providing power to the system. The BATFET will be re-enabled when the battery voltage drops below the recharge voltage threshold or when the device enters Battery Supply Mode during EOC.

When EOC is triggered, there are four conditions:

Table 6. EOC Status Scenario

	TE = 1 BG_CHG_TMR (disable)	TE = 1 BG_CHG_TMR (counting)	TE = 1 BG_CHG_TMR (timeout)	TE = 0 BG_CHG_TMR (disable)
ST_EOC	1	1	1	1
ST_CHG_DONE	1	0	1	0
ST_BG_CHG	0	1	0	0
STAT Pin	High	High	High	Low
IC_STAT	0111	0110	0111	0101
BATFET	OFF	ON	OFF	ON

1. If the device triggers AICR, MIVR, JEITA, or thermal regulation status during charging, the actual charging current will be less than the programmed value. In this condition, the EOC function will be disabled, and the safety timer's counting rate will be halved.
2. Background charging can be initiated after EOC detection. To enable background charging, set both BG_CHG_TMR and TE = 1. When background charging is active, IC_STAT is set to 0110, and the BATFET will turn off once the background charge timer expires.
3. The BG_CHG_TMR is reset under any of the following conditions:
   - CHG_EN is disabled and then re-enabled.
   - EOC status is triggered again.
   - EOC_RST bit is set.
   - REG_RST bit is set.
   - The value of BG_CHG_TMR changes.

An $\overline{INT}$ pulse is sent to the host upon entering background charge mode and when the background charge timer expires.

16.4.4 Optimized VDS on BATFET

The device incorporates a power path function featuring a BATFET that separates system from the battery. The minimum system voltage is determined by the VSYS_MIN bits (default 3.5V).

When the battery voltage exceeds VSYS_MIN, the BATFET is fully activated to minimize $R_{DS(ON)}$, thereby optimizing VDS (voltage difference between VSYS and VBAT) on the BATFET.

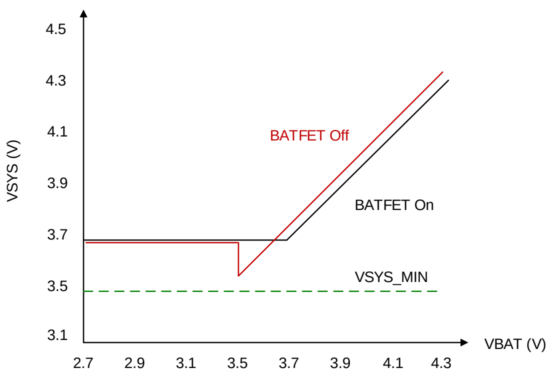


Figure 4. VSYS vs. VBAT

When the BATFET is off and the battery voltage is above VSYS_MIN, the system voltage is regulated to be typically 50mV higher than the battery voltage. The status register ST_SYS_MIN = 1 to indicate that the system is operating under minimum system voltage regulation.

16.4.5 Power Management System

To apply the maximum current and avoid overloading the power source on VBUS, the device's Power Management System continuously monitors the voltage and current of the power source. If the power source becomes overloaded, indicated by the current exceeding the AICR limit or the voltage dropping below MIVR, the device will reduce the charging current to prioritize power for the system's operations.

If the charging current is reduced to zero and the power source still triggers the AICR or MIVR conditions, VSYS begins to drop. Once VSYS falls below VBAT, the device automatically switches to battery supply mode. In this mode, the BATFET turns fully on, and the battery starts to discharge so that the system is supported from both the battery and the power source.

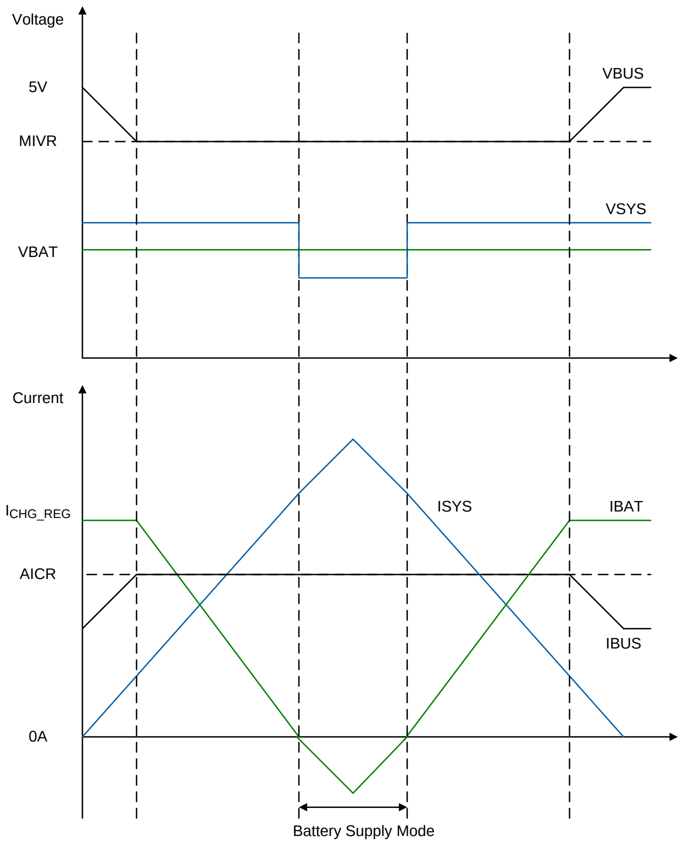


Figure 5. Power Management System

16.4.6 Battery Supply Mode

When the voltage difference between VBAT and VSYS is above 50mV, the BATFET turns on, and the BATFET gate is regulated to keep VBAT-VSYS at 40mV to prevent frequent entry and exit from the battery supply mode. When the voltage of VBAT-VSYS drops below 0mV, the charger exits the battery supply mode and starts to charge the battery.

16.4.7 JEITA Protection During Charge Mode

The device incorporates a dedicated thermistor input for precise temperature monitoring.

To ensure battery thermal protection, the device adheres to the JEITA guidelines established in 2007.

To initiate a charging cycle, the voltage on the TS pin must fall within the T1 to T4 range. The device will stop charging if the battery temperature drops below T1 (Cold) or rises above T4 (Hot) when JEITA_COLD = 0 and JEITA_HOT = 0.

In this case, the IC_STAT = 1000 to signal a charging fault, and an $\overline{INT}$ will be sent to the host.

In the cool temperature range (T1 to T2), the charge current is reduced to either 50% or 25% of I_{CHG_REG}, as determined by JEITA_COOL_ISET.

In the warm temperature range (T3 to T4), the voltage setting of V_{BAT_REG} is lowered to 4.1V or maintained at the V_{BAT_REG} value, as determined by JEITA_WARM_VSET.

The device offers configuration options that exceed the standard JEITA requirements for added flexibility.

Within the cool temperature range (T1 to T2), the charger can set the voltage of V_{BAT_REG} down to 4.1V, as set by JEITA_COOL_VSET.

Within the warm temperature range (T3 to T4), the charge current can be reduced to 50% of I_{CHG_REG}, as set by JEITA_WARM_ISET.

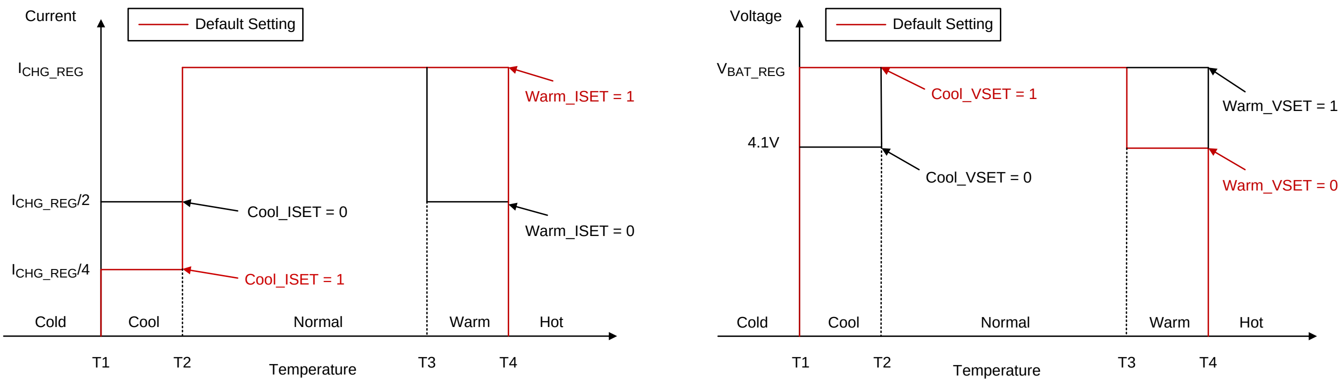


Figure 6. JEITA Protect for Charging Current and Voltage

The JEITA protection feature is comprised of four sections. Herein, R_{HOT} represents the NTC resistance at the battery over-temperature threshold, and R_{COLD} represents the NTC resistance at the battery under-temperature threshold. Based on R_{HOT} and R_{COLD}, R_{TS1} and R_{TS2} can be calculated using equations (1) and (2).

$R_{TS1} = V_{REGN} \times [(1/V_{T1} - 1/V_{T4})/(1/R_{COLD} - 1/R_{HOT})]$.............(1)

$R_{TS2} = R_{TS1} \times [1/(V_{REGN}/V_{T1} - R_{T1}/R_{COLD} - 1)]$.............(2)

16.4.8 Thermal Protect During Boost Mode

To initiate boost mode to discharge from the battery, the voltage on the TS pin must fall within the T0 to T4 range. The device will stop the converter if the battery temperature falls below T0 (COLD_OTG) or rises above T4 (HOT_OTG). In this case, the IC_STAT = 1000 for a charge fault, and an $\overline{INT}$ is asserted to the host.

Once the temperature re-enters the normal range, the boost mode will resume.

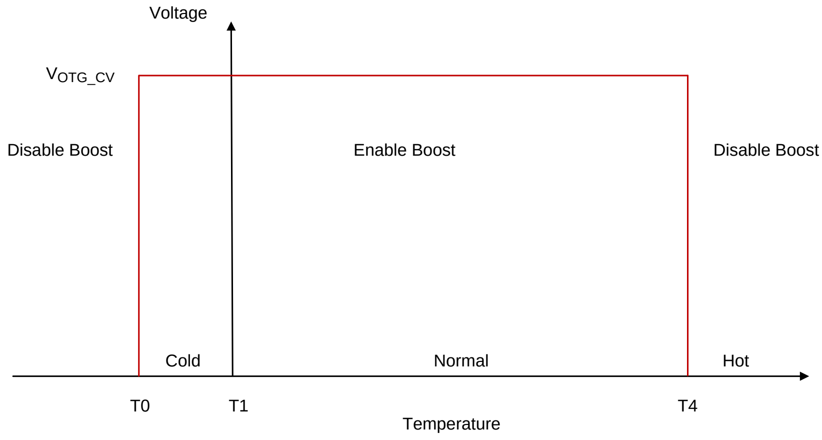


Figure 7. Thermal Protect During Boost Mode

16.4.9 Charging Safety Timer

The device incorporates a safety timer to prevent abnormal charging times due to a poor battery condition. The device can be set with the CHG_SAFE_TMR bits to change the timer for the fast charge cycle. When the safety timer expires, the device stops charging, the IC_STAT becomes 1000 to indicate a charge fault, ST_CHG_TOUT is set to 1, and an $\overline{\text{INT}}$ is asserted to the host. The safety timer can be disabled by setting CHG_SAFE_TMR_EN to 0.

Table 6. Charging Safety Timer

VBAT	Safety Timer
< V_{PRE_CHG}	2 Hours
> V_{PRE_CHG}	5 Hours, 10 Hours (Default), 15 Hours, 20 Hours

When the charger is in AICR, MIVR, JEITA cool, JEITA warm, or thermal regulation mode, the safety timer's counter clock rate will be halved. For example, if the charger is in AICR status and the timer setting is 10 hours, the actual safety timer will expire in 20 hours. The extended charge timer setting can be disabled by setting CHG_SAFE_TMR_2XT to 0. The safety timer can be reset by any of the following actions:

1. Toggling the $\overline{\text{CE}}$ pin.
2. Disabling and then enabling CHG_EN.
3. Disabling and then enabling CHG_SAFE_TMR
4. Setting REG_RST.

16.4.10 MediaTek Pump Express+ (MTK, PE+)

The device can provide an input current pulse to communicate with an MTK-PE+ high voltage adapter. When the PE_EN bit is enabled, the device can increase or decrease the adapter output voltage by setting PE10_INC to the desired value. After enabling the PE function, the device will generate a VBUS current pattern for the MTK-PE+ adapter to automatically identify whether to increase or decrease the output voltage. After the PE pattern is completed, the PE_EN bit will be cleared to 0, and an $\overline{\text{INT}}$ will be asserted to the host to indicate that the PE_DONE event has occurred.

16.4.11 Adaptive Input Current Control (AICC)

The AICC function provides an adaptive AICR setting to prevent input voltage drops. When the input power source experiences overcurrent and the VBUS drops to the MIVR level, setting the AICC_EN bit to 1 will cause the device to automatically decrease the AICR level step by step until the MIVR event is exited. After the AICC process is completed, the AICC_EN bit will be cleared to 0, and an $\overline{\text{INT}}$ will be asserted to the host to indicate the AICC_DONE has occurred.

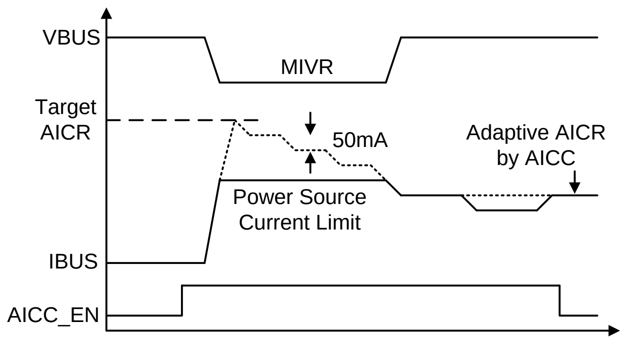


Figure 8. AICC Enable

16.5 Status Outputs

16.5.1 Power Good Indicator ($\overline{\text{PG}}$ Pin and ST_CHG_RDY Bit)

The $\overline{\text{PG}}$ pin goes low to indicate a good power source under the following conditions:

1. VBUS is above the $V_{BUS\_MIN\_RISE}$ threshold, and I_{BADSRC} is applied.
2. VBUS is above VBAT (not in sleep mode).
3. VBUS is below the V_{AC_OVP} threshold setting.
4. HZ = 0 (not in HZ mode).
5. The charger's temperature is under the THREG threshold setting.
6. VBUS Source Type Detection is completed.

16.5.2 Charging Status Indicator (STAT Pin)

The device indicates charging status IC_STAT on the STAT pin. The STAT pin is an open-drain output that can be used to drive an LED. The STAT pin function can be disable by setting STAT_EN = 0.

Table 7. STAT Pin State

IC_STAT	STAT Indicator
Trickle, Pre, Fast charge, IEOC-charge (EOC and TE = 0)	Low
Charge done, Back-Ground charge	High
HZ/SLEEP, VBUS ready for charge, OTG	High
Charge fault	Blinking at 1Hz

16.5.3 Interrupt to Host ($\overline{\text{INT}}$ Pin)

The device reports IRQ to the host via the $\overline{\text{INT}}$ pin, which is configured as an open-drain output.

The $\overline{\text{INT}}$ pin generates a low pulse with 256μs when an IRQ event occurs. All IRQ events are masked by default.

When a fault occurs, the device triggers an $\overline{INT}$ pulse to the host and retains the IRQ event details in registers 0x20 to 0x23. These details remain in the registers until the host reads the IRQ registers. The device will not send another $\overline{INT}$ pulse until the IRQ events are cleared by the host reading the registers, unless a new event occurs.

Table 8. STATUS, FLAG, and MASK Register Map

Name	STAT	IRQ	MASK
VBUS_GD	Y	Y	Y
CHG_RDY	Y	Y	Y
IEOC	Y	Y	Y
BK_CHG	Y	Y	Y
CHG_DONE	Y	Y	Y
RECHG	N	Y	Y
DETACH	N	Y	Y
BC12_DONE	Y	Y	Y
MIVR	Y	Y	Y
AICR	Y	Y	Y
CHG_THREG	Y	Y	Y
CHG_BUSUV	Y	Y	Y
CHG_TOUT	Y	Y	Y
CHG_SYSOV	Y	Y	Y
CHG_BATOV	Y	Y	Y
JEITA_HOT	Y	Y	Y
JEITA_WARM	Y	Y	Y
JEITA_COOL	Y	Y	Y
JEITA_COLD	Y	Y	Y
SYS_MIN	Y	Y	Y
SYS_SHORT	N	Y	Y
OTP	Y	Y	Y
VAC_OV	Y	Y	Y
WDT	Y	Y	Y
OTG_CC	Y	Y	Y
OTG_LBP	N	Y	Y
OTG_FAULT	N	Y	Y

16.6 Protections

16.6.1 VBUS Overvoltage Protection in Buck Mode

If the VBUS voltage is over the VAC_OVP setting (programmable by the VAC_OVP bits), the device stops switching immediately and asserts an $\overline{INT}$ pulse to the host. When VBUS overvoltage occurs, the status ST_VAC_OV is set to 1 and the IC_STAT is set to 1000 to indicate a charge fault. The device resumes normal operation when the VBUS voltage drops below the VAC_OVP threshold.

16.6.2 VBUS Overvoltage Protection in Boost Mode

When in boost mode, the VAC_OVP setting is locked at 6.35V, even if the VAC_OVP threshold is set at 10.8V or 14V. When the output voltage (VBUS) exceeds the VAC_OVP threshold, the device stops switching immediately, clears the OTG_EN bit to 0, and exits boost mode. The fault (OTG_FAULT) is set to high, and an $\overline{INT}$ pulse is asserted to the host. When the output voltage falls below VAC_OVP_HYS, the OTG_EN bit can be set to 1 by the host.

16.6.3 IBUS Overload Protection in Boost Mode

The device monitors the boost output voltage and current to provide VBUS short circuit protection. The device also includes built-in constant current regulation to allow OTG to adapt to various types of loads. If a short circuit is detected on VBUS, the boost will hiccup 7 times. If the boost retries are not successful, the OTG_EN bit will be set to 0 to disable boost mode, and an $\overline{INT}$ pulse will be asserted to the host to indicate OTG_FAULT.

16.6.4 VBUS Soft-Start

When the boost function is enabled, the device soft-starts on VBUS to avoid inrush current.

16.6.5 VSYS Overvoltage Protection

The SYSOVP threshold is set at 5.2V. Once VSYS is above the SYSOVP level, the buck stops switching immediately, and an $\overline{INT}$ pulse is asserted to the host to indicate a CHG_SYSOV fault. The device provides a 30mA current sink on VSYS to bring down the VSYS voltage.

16.6.6 VSYS Overcurrent Protection

The SYSOVP threshold is set at 5.2V. Once VSYS is above the SYSOVP level, the buck stops switching immediately, and an $\overline{INT}$ pulse is asserted to the host to indicate a CHG_SYSOV fault. The device provides a 30mA current sink on VSYS to bring down the VSYS voltage.

16.6.7 Battery Overvoltage Protection

The BAT_OVP threshold is set at 4% above the V_{BAT_REG} setting. If the battery voltage exceeds this overvoltage threshold, the device immediately disables charging, and asserts an $\overline{INT}$ to the host to indicate a CHG_BATOV event.

16.6.8 Battery Over-Discharge Protection

If the battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET turns off to prevent over-discharge. Upon connection of VBUS, the BAFET is activated to allow battery charging.

16.6.9 Thermal Protection in Buck Mode

The device continuously monitors the internal junction temperature to prevent overheating. In buck mode, the thermal regulation threshold is set at 120°C (programmable by the register THREG bits). If the junction temperature rise above the thermal regulation threshold, the device reduces the charging current. During thermal regulation, the EOC function is disabled, the safety timer's counting rate is reduced by half, and an $\overline{INT}$ signal is asserted to the host to indicate CHG_THREG.

Additionally, the device features a thermal shutdown mechanism that turns off the converter if the IC surface temperature exceeds T_{OTP} (160°C). An $\overline{INT}$ signal is also asserted to the host to indicate an OTP fault. The converter resumes normal operation once the surface temperature falls below the recovery threshold, which is T_{OTP} (160°C) - T_{OTP_HYS} (30°C).

16.6.10 Thermal Protection in Boost Mode

The device has thermal shutdown during boost mode. In boost mode, when the IC surface temperature exceeds T_{OTP} (160°C), the OTG_EN bit is set to 0 to disable boost mode, and an $\overline{INT}$ is asserted to the host to indicate an OTP fault.

16.7 Communication Interface

The RT9470/D uses an I²C-compatible interface with a 2-wire line (SCL and SDA) to communicate with the host. The SCL and SDA pins are open drain and need to be connected to the supply voltage by pull-up resistors. The RT9470/D operates as an I²C slave device with a 7-bit address of 53H and supports up to 3.4Mbits conditionally. To start an I²C communication, the process begins with a START (S) condition, and then the host sends the slave address. This address is 7 bits long, followed by an eighth bit which is a data direction bit (R/W). The second byte is the register address. The third byte contains data for the selected register, and the communication ends with a STOP (P) condition.

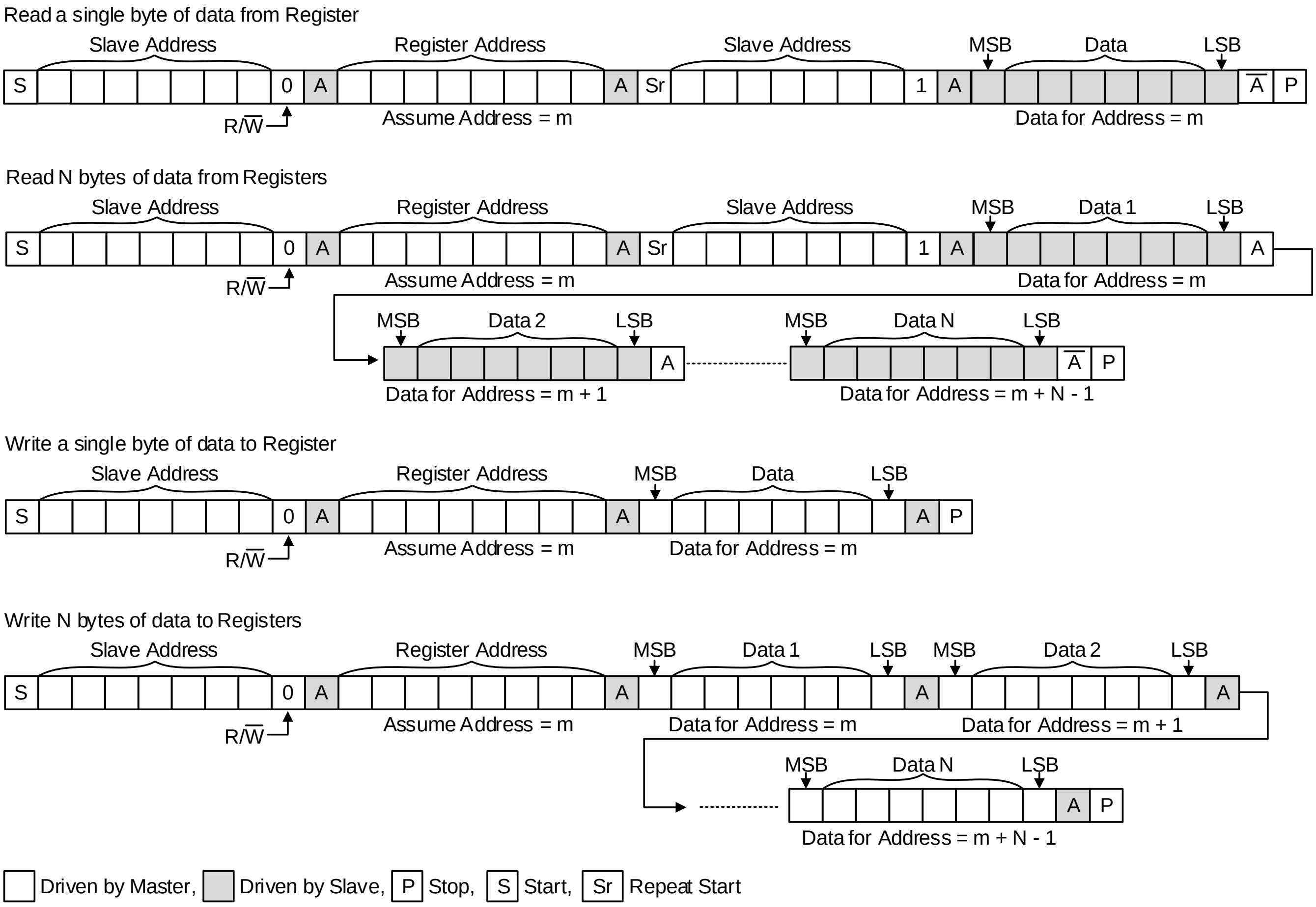


Figure 9. Read and Write Function

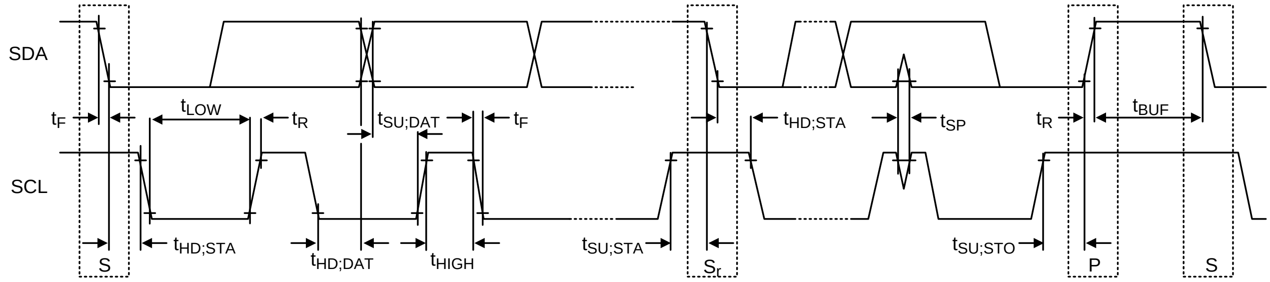


Figure 10. I^{2}C Waveform Information

16.7.1 I^{2}C Time-Out Reset

To avoid I^{2}C hang-ups, a timer runs during I^{2}C activity. If the SDA remains low for longer than 1 second, the RT9470/D will reset the I^{2}C to release SDA and return it to a high state. The I^{2}C hang-ups reset function can be disabled by setting bit 3 of register 0x01.

16.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-30B 2.1x2.5 (BSC) package, the thermal resistance, θ_{JA}, is 29.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (150°C - 25°C) / (29.6°C/W) = 4.22W for a WL-CSP-30B 2.1x2.5 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

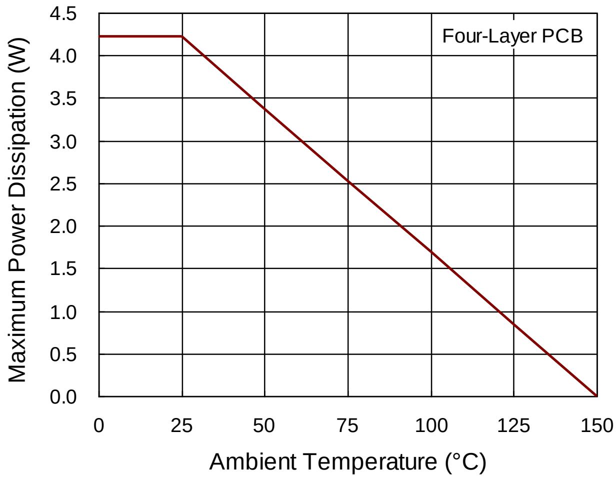


Figure 11. Derating Curve of Maximum Power Dissipation

16.9 Layout Considerations

The layout guidelines for the RT9470/D are provided below, along with several recommendations:

- Place the capacitor connected to the PMID pin as close as possible to the RT9470/D to minimize impedance and enhance performance.
- Position the inductor connected to the SW pin as close as possible to the RT9470/D. The trace should be routed as short as possible to reduce EMI, and the copper area of the trace must be adequate for the operating current.
- Connect the GND pins to the Thermal Pad pin on the TOP layer to minimize parasitic inductance and reduce EMI.
- The Thermal Pad pin should be connected to the ground plane through multiple vias to enhance thermal performance.
- Capacitors connected to IC pins should be placed as close as possible to the RT9470/D to ensure stability and reduce noise.

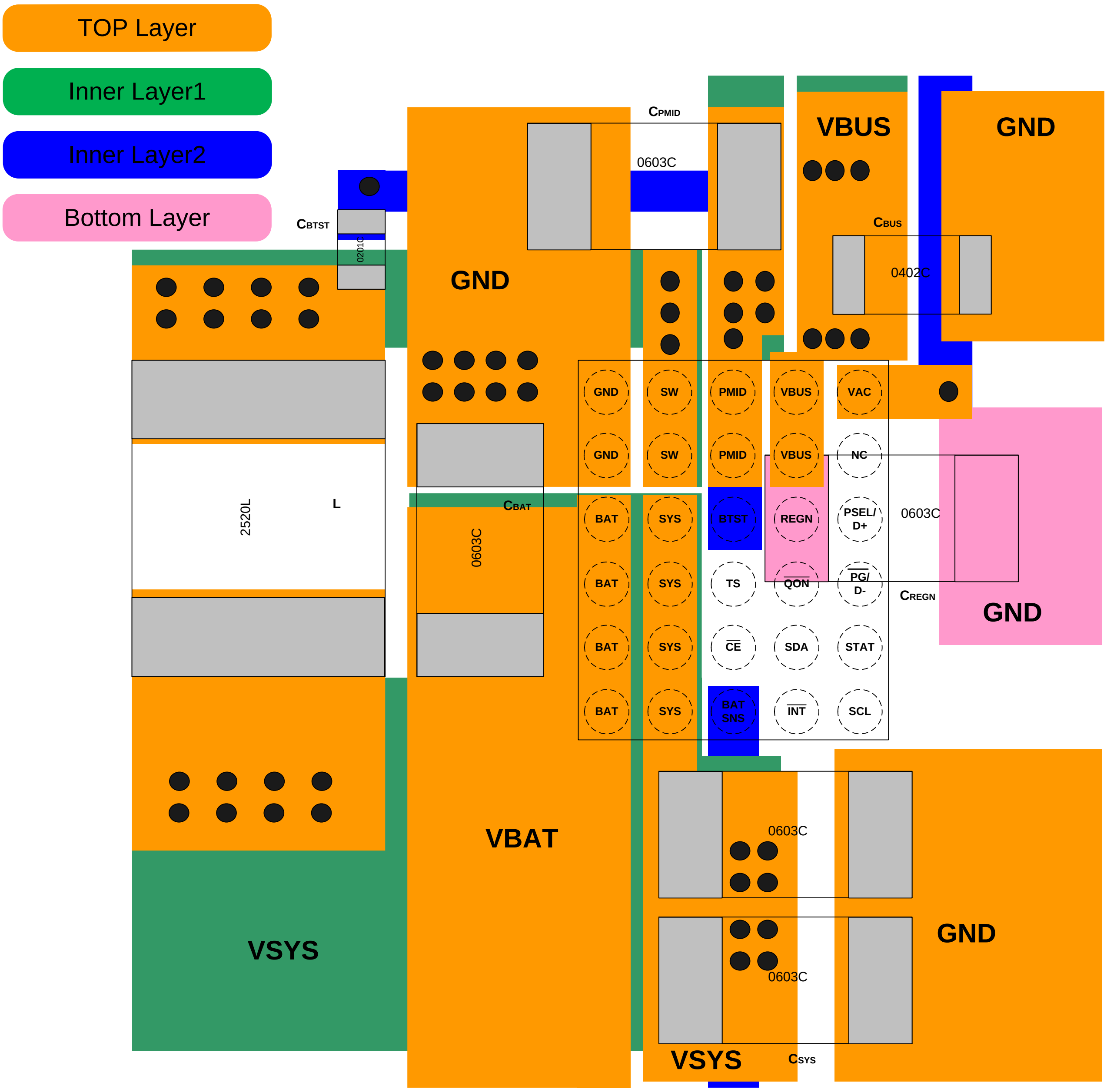
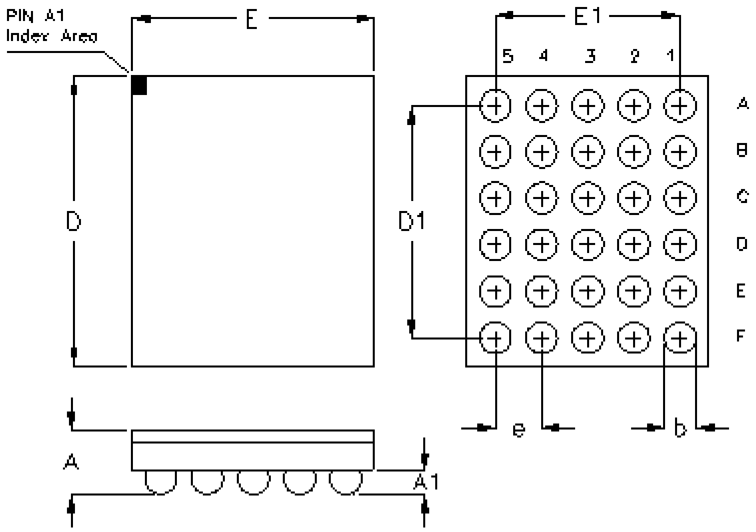


Figure 12. PCB Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

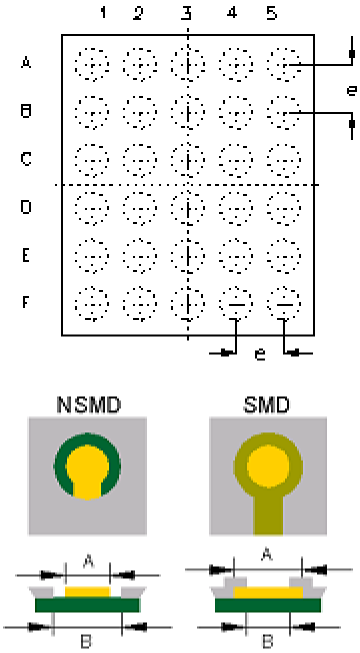
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	2.460	2.540	0.097	0.100
D1	2.000		0.079	0.000
E	2.060	2.140	0.081	0.084
E1	1.600		0.063	0.000
e	0.400		0.016	

30B WL-CSP 2.1x2.5 Package (BSC)

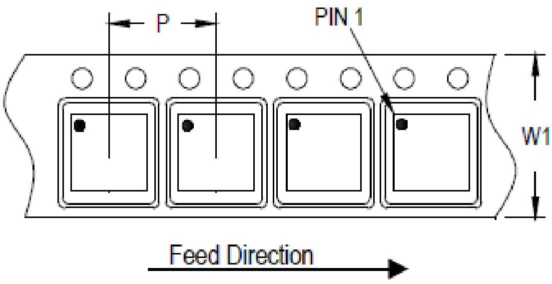
18 Footprint Information

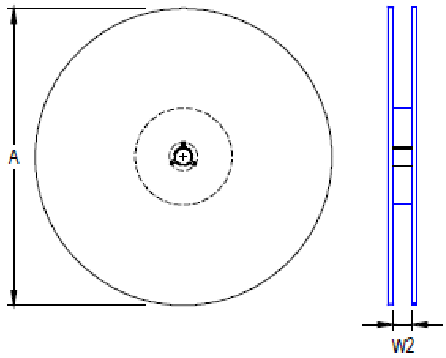


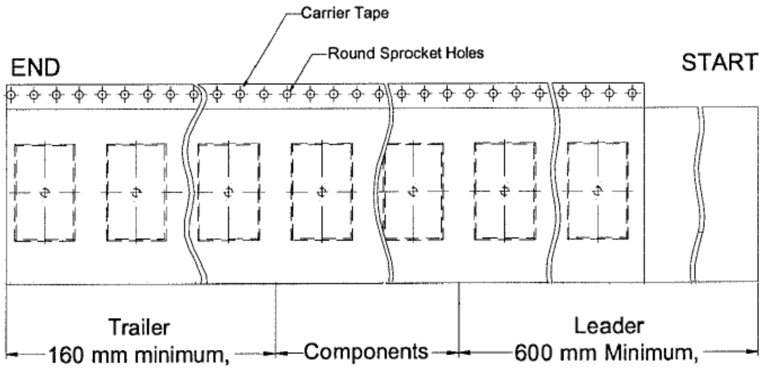
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.1x2.5-30(BSC)	30	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

19 Packing Information

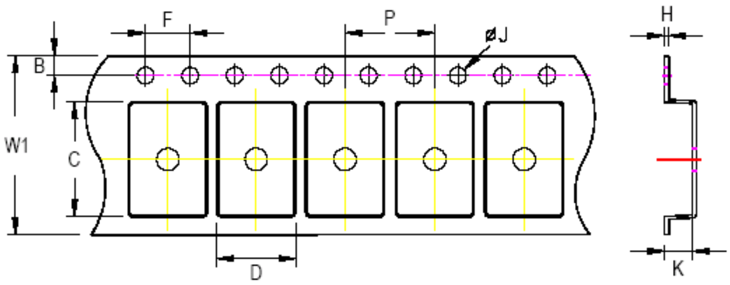
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 2.1x2.5	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.72mm	0.82mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 2.1x2.5	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
02	2023/10/19	Modify	General Description on P1 Ordering Information on P1 Absolute Maximum Ratings on P6 Application Information on P32 Packing Information on P47, 48, 49
03	2024/10/22	Modify	Ordering Information on P1 Application Information on P41. 50 Packing Information on P53, 54