RICHTEK®

RT9467

5A Single-Cell Li-Ion Switching Battery Charger with Power Path Management and USB-OTG Boost Mode

1 General Description

The RT9467 is a switch-mode single-cell Li-Ion/Li-Polymer battery charger for portable applications. It integrates a synchronous PWM controller, power MOSFETs, input current sensing and regulation, high-accuracy voltage regulation, and charge termination. The charge current is regulated through integrated sensing resistors. The RT9467 also features USB OTG (On-The-Go) support and integrates the D+/D- pins for USB host/charging port detection.

The RT9467 optimizes the charging task by using a control algorithm to vary the charge rate for different modes, including pre-charge mode and fast charge mode (constant voltage and constant current). The key charge parameters are programmable through an I2C interface. The RT9467 will resume the charge cycle whenever the battery voltage falls below an internal recharge threshold and can automatically enter sleep mode if the input power supply is removed.

Other features include undervoltage protection, overvoltage protection, thermal regulation and reverse leakage protection.

The RT9467 is available in a WQFN-24L 4x4 package.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PCs
- Power Banks
- Portable Instruments

3 Features

- **High Efficiency 5A, 1.5MHz Switching Charger with Output Inductor DFE252012F, TOKO**
  - **Charging Efficiency 90.25% at ICHG = 2A**
  - **Charging Efficiency 88.86% at ICHG = 3A**
  - **Charging Efficiency 84.2% at ICHG = 5A**
- **Synchronous 1.5MHz/0.75MHz Fixed-Frequency PWM Controller with Up to 95% Duty Cycle**
- **Power Path Management by BATFET Control**
- **Support High Voltage Input (9V/12V)**
- **Support High Voltage Input Adapter (Pump Express 1.0/2.0)**
- **Support IR Compensation Function from Charger Output to Cell Terminal**
- **Optimize Input Sourcing Capability to Prevent Overload**
  - **AICR Current Limit Setting via I2C**
  - **ILIM Pin for Current Limit Setting**
  - **Average Input Current Limit Measurement**
- **Shipping Mode for Battery Leakage Reduction**
  - **Wake Up System, Exit Shipping Mode, and Reset System by the $\overline{QON}$ Pin**
- **Automatic Charging**
- **Average Input Current Regulation (AICR): 0.1A to 3.25A in 50mA Steps**
- **Charge Current Regulation Accuracy: ±7%**
- **Charge Voltage Regulation Accuracy: ±1% (0 to 85˚C)**
- **Protection for Overall System Considerations**
  - **Thermal Regulation for Current Reduction and Over-Temperature Protection**
  - **Input Overvoltage Protection**
  - **Input Bad Adapter Protection**
  - **Battery Overvoltage Protection**
- **Support ADC Conversion for VBUS, VBAT, VSYS, REGN, TS_BAT, IBUS, IBAT, TEMP_JC**
- **INT Output for Communication with Host through I^2C (Watch Dog/Polling Function)**

4 Ordering Information

RT9467 □□

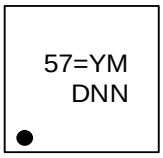
Package Type(1)
QW: WQFN-24L 4x4 (W-Type)
(Exposed Pad: Option 2)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

5 Marking Information



57=: Product Code
YMDNN: Date Code

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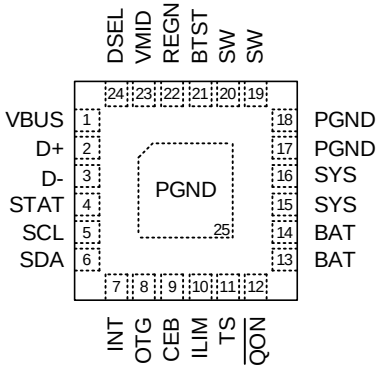
6 Pin Configuration

(TOP VIEW)



WQFN-24L 4x4

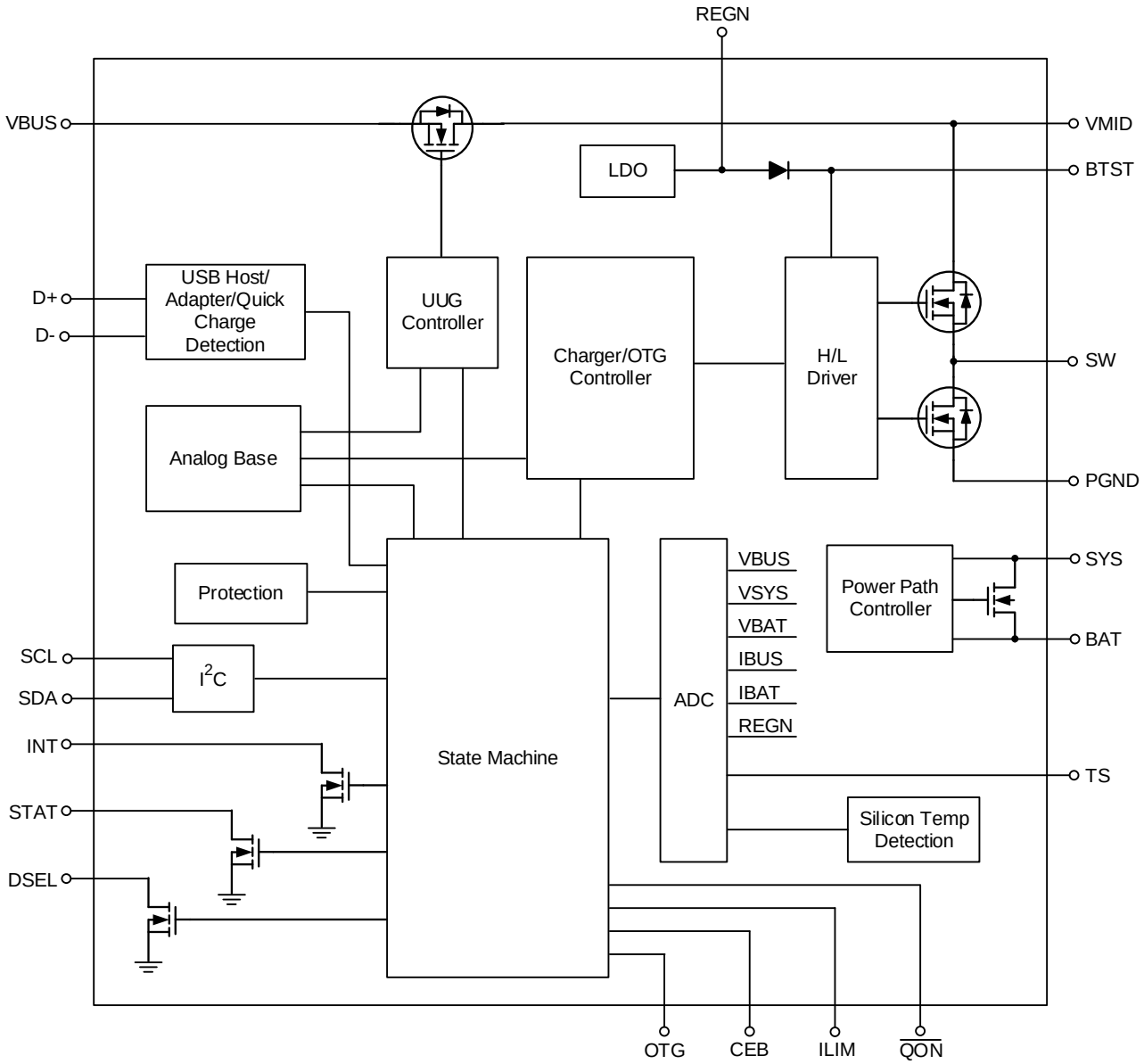
7 Functional Pin Description

Pin No.	Pin Name	Pin Description
1	VBUS	Power input.
2	D+	USB D+ port.
3	D-	USB D- port.
4	STAT	Charge status indicator. The open-drain output that indicates the charge is in progress when held low and the charge is finished when held high. If any fault occurs, CHG_STAT will blink at a frequency of 1Hz. Connect a 2.2k-10kΩ pull-up resistor.
5	SCL	I^2C interface serial clock input, open-drain. An external pull-up resistor is required.
6	SDA	I^2C interface serial data input/output, open-drain. An external pull-up resistor is required.
7	INT	Active-low Interrupt output, open-drain. It serves as an indicator of the charger/boost event for the system processor.
8	OTG	OTG boost mode enable control, active-high. It acts with OTG_PIN_EN (Addr0x01[1]). This pin has an internal pull-down resistor of 102kΩ.
9	CEB	Charger enable input, active-low. This pin has an internal pull-down resistor of 102kΩ.
10	ILIM	Input current limit setting pin. A resistor is connected from the ILIM pin to ground to set the maximum input current limit. The actual input current limit is the lower value set through the ILIM pin and the IAICR register bits.
11	TS	Battery temperature-sense input. Connect to a resistor divider for temperature programming. If the battery temperature-sense function is not needed, connect a 50kΩ resistor to REGN and another 50kΩ resistor to ground.
12	$\overline{QON}$	Internal BATFET enable control input. In shipping mode, this pin is pulled low for the duration of $t_{SHIPMODE}$ (typical 0.9s) to exit shipping mode.
13, 14	BAT	Charge current output node for battery connection. The internal BATFET is connected between VSYS and BAT. Connect a 10μF ceramic capacitor between BAT and ground.

Pin No.	Pin Name	Pin Description
15, 16	SYS	System connection node. The internal BATFET is connected between SYS and BAT. Connect a 20μF ceramic capacitor between SYS and ground.
17, 18	PGND	Power ground.
19, 20	SW	Switch node for output inductor connection.
21	BTST	Bootstrap capacitor connection for high-side gate driver. Connect a capacitor from BTST to SW to power the internal gate driver.
22	REGN	Regulated output voltage for PWM low-side gate driver and bootstrap capacitor. Connect a 4.7μF ceramic capacitor from REGN to GND. 1. If VBUS is plugged in, REGN will be powered by VBUS and regulated to 4.9V. 2. If VBUS is unplugged, the charger will operate in sleep mode and the REGN voltage will be 0V. (Note 2)
23	VMID	Connection point between the reverse blocking MOSFET and the high-side switching MOSFET.
24	DSEL	1. Open-drain type configuration 2. During input source type detection, the pin drives low. 3. When detection is completed: • The pin keeps low for DCP/HVDCP. • The pin keeps high for other types of source detection (SDP/CDP).
25 (Exposed Pad)	PGND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

Note 2. Since the REGN voltage is also used to power the TS resistor, when the charger is in sleep mode, the REGN will be woken up (reactivated) if VBAT is greater than forward voltage (V_F) of the internal high-side (HS) MOS diode by V_{SLP_EXIT}. In this state, all functions of the internal ADC are activated and I^2C R/W operations are enabled. The REGN wake-up time is 500ms.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 3)

- Supply Input Voltage, VBUS ---------- –0.3V to 22V
- Supply Input Voltage, VBUS (Peak <100ns Duration) ---------- –2V
- VMID, BTST ---------- –0.3V to 22V
- SW ---------- –0.3V to 16V
- SW (Peak <100ns duration) ---------- –2V
- VMID – VBUS, BTST – SW ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x4 ---------- 4.54W
- Package Thermal Resistance (Note 4)
  WQFN-24L 4x4, θ_{JA} ---------- 22°C/W
  WQFN-24L 4x4, θ_{JC} ---------- 5.4°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model) ---------- 2kV

Note 3. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 4. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage ---------- 4V to 14V
- Maximum Input Current (VBUS), I_{AICR} ---------- 3.25A
- Maximum SYS Output Current (SW), I_{SYS} ---------- 5A
- Maximum Battery Voltage, V_{BAT} ---------- 4.71V
- Maximum I_{BAT} Fast Charging Current ---------- 5A
- Maximum I_{BAT} Discharging Current ---------- 6A
- Maximum I_{BAT} Discharging Current (Peak,1sec Duration) ---------- 9A
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 6. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

(V_{BUS} = 5V, V_{BAT} = 4.2V, L = 1μH, C_{IN} = 2.2μF, C_{BAT} = 10μF, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
V_{BUS} Supply Current	I_{VBUS_SW}	V_{SW} is switching, V_{BUS} = 5V, V_{SYS} = 3.8V	--	8	--	mA
	I_{VBUS_NSW}	V_{SW} Is non-switching, V_{BUS} = 5V, V_{SYS} = 4.4V	--	--	5	mA
	I_{VBUS_HZ}	V_{SW} is in high-impendence mode, V_{BUS} = 5V, V_{SYS} = 3.8V	--	--	170	μA
Battery Leakage Current	$I_{BAT\_LK\_OFF}$	V_{BAT} = 4.2V, power path is off	--	--	25	μA
	$I_{BAT\_LK\_ON}$	V_{BAT} = 4.2V, SCL and SDA pull low, no VBUS	--	--	60	
Boost-Mode Battery Discharge Current	$I_{BAT\_BOOST\_SW}$	V_{BAT} = 4.2V, boost mode, I_{VBUS} = 0A, V_{SW} is switching	--	5	--	mA
V_{BUS}/V_{BAT} Power-Up						
Sleep-Mode Entry Threshold, V_{BUS} – V_{BAT}	V_{ENTER_SLP}	2.5V < V_{BAT} < V_{BAT_REG}, V_{BUS} falling	0	40	100	mV
Sleep-Mode Exit Threshold, V_{BUS} – V_{BAT}	V_{EXIT_SLP}	2.5V < V_{BAT} < V_{BAT_REG}, V_{BUS} rising	40	100	200	mV
Sleep-Mode Exit Deglitch Time	$t_{DEGLITCH\_EXIT\_SLP}$	Exit sleep-mode	--	120	--	ms
V_{BUS} Bad Adapter Threshold	V_{BAD_ADP}		--	3.8	--	V
V_{BUS} Bad Adapter Hysteresis	$V_{BAD\_ADP\_HYS}$		--	150	--	mV
V_{BUS} Bad Adapter Sink Current	$I_{SNK\_BAD\_ADP}$		--	50	--	mA
V_{BUS} Bad Adapter Detection Time	$t_{DET\_BAD\_ADP}$		--	30	--	ms
Input Current Limit Factor	K_{ILIM}	The input current is regulated to 508mA by the ILIM pin with a resistance of 698Ω	320	355	390	AΩ
Input Current Limit Regulation	I_{ILIM_MIN}	Minimum input current for regulation on the ILIM pin	0.5	--	--	A
Input Power Regulation						
Minimum Input Voltage Regulation (MIVR) Threshold Range	V_{MIVR}	I^2C programmable in 0.1V steps	3.9	--	13.4	V
Default Minimum Input Voltage Regulation Threshold	V_{MIVR_DEF}	Default	--	4.4	--	V
Minimum Input Voltage Regulation Accuracy	V_{MIVR_ACC}	VMIVR = 4.4V, 9V	–3	--	3	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Average Input Current Regulation Accuracy	I_{AICR_ACC}	USB charge mode, I_{AICR} = 100mA	86	93	100	mA
		USB charge mode, I_{AICR} = 500mA	440	470	500	
		USB charge mode, I_{AICR} = 1000mA	880	940	1000	
		Adapter 1.5A charge mode, I_{AICR} = 1500mA	1300	1400	1500	
Protection						
V_{BUS}						
V_{BUS} Undervoltage Protection Threshold	V_{UVP}	V_{BUS} rising	3.05	3.3	3.55	V
V_{BUS} Undervoltage Protection Hysteresis	V_{UVP_HYS}	V_{BUS} falling from UVLO	--	150	--	mV
V_{BUS} Overvoltage Protection Threshold	V_{BUS_OVP}	V_{BUS} rising	14	14.5	15	V
V_{BUS} Overvoltage Protection Hysteresis	$V_{BUS\_OVP\_HYS}$	V_{BUS} falling	--	250	--	mV
V_{BAT}						
Battery Overvoltage Protection Threshold	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{BAT_REG}, as (V_{BAT_OVP} – V_{BAT_REG}) / V_{BAT_REG}	106	108	110	%
Battery Overvoltage Protection Hysteresis	$V_{BAT\_OVP\_HYS}$	V_{BAT} falling, as ($V_{BAT\_OVP\_HYS}$) / V_{BAT_REG}	--	4	--	%
Thermal Protection						
Over-Temperature Protection Threshold	T_{OTP}	Thermal shutdown threshold temperature	--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Thermal shutdown hysteresis temperature	--	30	--	°C
Thermal Regulation Threshold	T_{TR}	Charge current starts decreasing	--	120	--	°C
V_{SYS}						
V_{SYS} Overvoltage Protection Threshold	V_{SYS_OVP}	V_{SYS} rising	--	5.25	--	V
V_{SYS} Undervoltage Protection Threshold	V_{SYS_UVP}	V_{SYS} falling	--	2.4	--	V
Battery Charging Stages						
End-of-Charge						
Battery Regulation Voltage Range	V_{BAT_REG}	I^2C programmable in 10mV steps	3.9	--	4.71	V
Battery Regulation Voltage	$V_{BAT\_REG\_DEF}$	Default	--	4.2	--	V
Battery Regulation Voltage Accuracy	$V_{BAT\_REG\_ACC}$	Temperature = 0 to 85°C	–1	--	1	%
Re-Charge Mode Threshold	V_{RECHG}	V_{BAT} falling, the difference below V_{BAT_REG}, (Addr 0x0B[2:0] = 00)	50	100	150	mV

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Re-Charge Deglitch Time	$t_{DEGLITCH\_RECHG}$			--	120	--	ms
End-of-Charge Current	I_{EOC}	I^2C programmable in 50mA steps		100	--	850	mA
Default End-of-Charge Current	I_{EOC_DEF}	Default		--	250	--	mA
End-of-Charge Current Accuracy	I_{EOC_ACC}			–20	--	20	%
Default End-of-Charge Deglitch Time	$t_{DEGLITCH\_EOC\_DEF}$	Default		--	2	--	ms
Fast Charge							
Charge Current Range	I_{CHG}	I^2C programmable in 0.1A steps		0.1	--	5	A
Charge Current Accuracy	I_{CHG_ACC}	V_{BAT} = 3.8V	I_{CHG} < 500mA	–20	--	20	%
			500mA < I_{CHG} < 1000mA	–10	--	10	
			I_{CHG} > 1000mA	–7	--	7	
Pre-Charge							
Pre-Charge Mode Threshold	V_{PRECHG}	I^2C programmable in 0.1V steps		2	--	3.5	V
Pre-Charge Mode Hysteresis	V_{PRECHG_HYS}	Pre-charge hysteresis, falling		--	0.2	--	V
Pre-Charge Mode Threshold Accuracy	V_{PRECHG_ACC}			–5	--	5	%
Pre-Charge Current Range	I_{PRECHG}	I^2C programmable in 50mA steps		100	--	850	mA
Default Pre-Charge Current	I_{PRECHG_DEF}	Default		--	150	--	mA
Pre-Charge Current Accuracy	I_{PRECHG_ACC}			–20	--	20	%
Trickle Charge							
Trickle Charge Threshold	V_{TRICHG}	V_{BAT} falling		--	2	--	V
Trickle Charge Threshold Hysteresis	V_{TRICHG_HYS}	V_{BAT} rising		--	200	--	mV
Trickle Charge Threshold Accuracy	V_{TRICHG_ACC}			–5	--	5	%
Trickle Current	I_{TRICHG}	V_{BAT} < 2V, charge with I_{CHG} = 100mA V_{BAT} < 1.6V, charge with AICR = 100mA		--	100	--	mA
Trickle Current Accuracy	I_{TRICHG_ACC}			–20	--	20	%
V_{SYS}							
System Regulation Voltage	V_{SYS_REG}	Minimum system regulation voltage, I^2C programmable in 0.1V steps		3.3	--	4	V
Default System Regulation Voltage	$V_{SYS\_REG\_DEF}$	Default minimum system regulation voltage		--	3.6	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System Regulation Accuracy	$V_{SYS\_REG\_ACC}$		–5	--	5	%
Battery Charger						
On-Resistance of UUG	R_{DSON_UUG}	From VBUS to VMID	--	17	32	mΩ
On-Resistance of High-Side MOSFET	R_{DSON_H}	From VBUS to SW	--	42	79	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	From SW to PGND	--	28	40	mΩ
On-Resistance of Power-Path-Side MOSFET	R_{DSON_PP}	From SYS to BAT	--	13	30	mΩ
Switching Frequency (1.5MHz)	f_{SW1}	I^2C programmable to 1.5 MHz (Addr 0x01[7] =0)	--	1.5	--	MHz
Switching Frequency (750kHz)	f_{SW2}	I^2C programmable to 0.75MHz (Addr 0x01[7] =1)	--	0.75	--	MHz
Frequency Accuracy	f_{SW_ACC}		–10	--	10	%
Maximum Duty Cycle	D_{MAX}	At minimum input voltage	--	97	--	%
Minimum Duty Cycle	D_{MIN}		0	--	--	%
REGN Regulation	V_{REGN_REG}	V_{BUS} = 5V/9V/12V	--	4.9	--	V
REGN Current Limit	I_{LIM_REGN}	V_{BUS} = 5V/9V/12V	50	--	--	mA
Sink Current for Battery Detection	I_{SNK_BAT}		--	300	--	μA
Internal $\overline{QON}$ Pull-Up Resistance	$R_{PU\_\overline{QON}}$		--	200	--	kΩ
Internal $\overline{QON}$ Pull-Up Voltage	$V_{PU\_\overline{QON}}$	Battery only	--	V_{BAT}	--	V
		V_{BUS} = 5V/9V	--	4.8	--	
$\overline{QON}$ Exit Shipping Mode Time	$t_{SHIPMODE}$	$\overline{QON}$ low for BATFET on-time to exit shipping mode	--	0.9	--	sec
System Reset by $\overline{QON}$ Pin	$t_{\overline{QON}\_RST}$	$\overline{QON}$ low time to enable full system reset	--	10	--	sec
BATFET Reset Time	t_{BATFET_RST}	BATFET off-time during full system reset	--	0.41	--	sec
Shipping Mode Entry Deglitch Time	$t_{DEGLITCH\_ENTRY\_SM}$	Enter shipping mode	--	9	--	sec
AICL	V_{AICL}	V_{BUS} rising, I^2C programmable	--	4.6	--	V
AICL Hysteresis	V_{AICL_HYS}		--	50	--	mV
Inductor Overcurrent Protection Buck Threshold	I_{OCP_BUCK}	Inductor OCP level for buck mode	--	6	--	A
OTG Boost Mode Operation						
OTG Boost-Mode Output Regulation Voltage Range	V_{OTGBST}	To VBUS	4.425	--	5.825	V
OTG Boost-Mode Output Regulation Voltage Accuracy	V_{OTGBST_ACC}		–3	--	3	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OTG Boost-Mode Overload Protection Threshold	I_{OTG_OLP}	I^2C programmable	0.5	--	2.4	A
OTG Boost-Mode Default Overload Protection Threshold	$I_{OTG\_OLP\_DEF}$	Address 0x0A [2:0] = 000	0.5	--	--	A
OTG Low Battery Protection Threshold	V_{OTG_LBP}	I^2C programmable, hysteresis = 0.4 V	2.3	--	3.8	V
OTG Default Low Battery Protection Threshold	$V_{OTG\_LBP\_DEF}$	OTG_LBP = 2.8V (Addr0x0A[7:4] = 0101)	--	2.8	--	V
OTG Low Battery Protection Threshold Accuracy	$V_{OTG\_LBP\_ACC}$		–5	--	5	%
OTG VMID Overvoltage Protection	$V_{OTG\_VMID\_OVP}$	V_{VMID} rising	--	6	--	V
OTG VMID Overvoltage Protection Hysteresis	$V_{OTG\_VMID\_OVP\_HYS}$		--	200	--	mV
Inductor Overcurrent Protection Boost Threshold	I_{OCP_BOOST}	Inductor OCP level for boost mode	--	5.5	--	A
Current Pulse Control, PE1.0						
Current Pulse Control Stop Pulse	t_{PUMPX_STOP}		430	--	570	ms
Current Pulse Control Long On Pulse	t_{PUMPX_ON1}		240	--	360	ms
Current Pulse Control Short On Pulse	t_{PUMPX_ON2}		70	--	130	ms
Current Pulse Control Off Pulse	t_{PUMPX_OFF}		70	--	130	ms
Current Pulse Control Stop Start Delay	t_{DLY_PUMPX}		80	--	225	ms
I^2C Characteristics						
Output Low Level	V_{OL_I2C}	I_{DS} = 10mA	--	--	0.4	V
SCL, SDA High-Level Input Threshold Voltage	V_{IH_I2C}		1.3	--	--	V
SCL, SDA Low-Level Input Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock Frequency	f_{SCL}		--	--	400	kHz
High Level Leakage Current	I_{LK_I2C}	V_{PULL_UP} = 1.8V, SDA and SCL	--	--	1	μA
Capacitive Load for I^2C Bus	C_b	V_{PULL_UP} = 1.8V	--	--	1	pF
Default Wait Time for Watch Dog Reset	t_{WDT_DEF}	Watch Dog timer selection, Default: 0x0D[6] = 1	--	500	--	ms
NTC Monitor						
Battery Temperature HOT Threshold	V_{VTS_HOT}	V_{TS} falling, the ratio of V_{REGN}	33.5	34.5	35.5	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Temperature WARM Threshold	V_{VTS_WARM}	V_{TS} falling, the ratio of V_{REGN}	44	45	46	%
Battery Temperature COOL Threshold	V_{VTS_COOL}	V_{TS} rising, the ratio of V_{REGN}	67.5	68.5	69.5	%
Battery Temperature COLD Threshold	V_{VTS_COLD}	V_{TS} rising, the ratio of V_{REGN}	72.5	73.5	74.5	%
Battery Temperature Hysteresis	V_{VTS_HYS}		--	2	--	%
Control I/O Pin (STAT, INT)						
Output Voltage Logic-Low	V_{OL_CTRL}	I_{DS} = 10mA	--	--	0.4	V
Control I/O Pin (OTG, CEB, $\overline{QON}$)						
Input Voltage Logic High	V_{IH_CTRL}	Logic high threshold	1.3	--	--	V
Input Voltage Logic Low	V_{IL_CTRL}	Logic low threshold	--	--	0.4	V
Battery Charge Detection Spec (D+/D-)						
VDP_SRC Voltage	V_{DP_SRC}	With I_{DAT_SRC} = 0 to 250μA	0.5	0.65	0.7	V
VDAT_REF Voltage	V_{DAT_REF}		0.25	0.325	0.4	V
VLGC Voltage	V_{LGC}		0.8	1.2	2	V
IDM SINK Current	I_{SNK_DM}	May be a resistance if desired	50	100	150	μA
Data Contact Timeout	t_{DCDT}	Setting by register 0x12[5:4]	--	600	--	ms
ADC						
ADC Conversion Time for Each Channel	t_{CONV}		35	200	--	ms
Number of Bits for ADC Resolution	RES	Logic high threshold	--	10	--	bit
ADC Accuracy and Measurement Range						
VBUS_DIV5 Measurement Range	$V_{VBUS\_DIV5ADC\_MR}$		1	--	22	V
VBUS_DIV5 Resolution	$V_{VBUS\_DIV5ADC\_RES}$		--	25	--	mV
VBUS_DIV5 Accuracy	$V_{VBUS\_DIV5ADC\_ACC}$		–2	--	2	LSB
VBUS_DIV2 Measurement Range	$V_{VBUS\_DIV2ADC\_MR}$		1	--	9.8	V
VBUS_DIV2 Resolution	$V_{VBUS\_DIV2ADC\_RES}$		--	10	--	mV
VBUS_DIV2 Accuracy	$V_{VBUS\_DIV2ADC\_ACC}$		–2	--	2	LSB
VBAT Measurement Range	$V_{VBAT\_ADC\_MR}$		0	--	4.9	V
VBAT Resolution	$V_{VBAT\_ADC\_RES}$		--	5	--	mV
VBAT Accuracy	$V_{VBAT\_ADC\_ACC}$		–2	--	2	LSB
VSYS Measurement Range	$V_{VSYS\_ADC\_MR}$		0	--	4.9	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSYS Resolution	$V_{VSYS\_ADC\_RES}$		--	5	--	mV
VSYS Accuracy	$V_{VSYS\_ADC\_ACC}$		–2	--	2	LSB
REGN Measurement Range	$V_{REGN\_ADC\_MR}$		0	--	4.9	V
REGN Resolution	$V_{REGN\_ADC\_RES}$		--	5	--	mV
REGN Accuracy	$V_{REGN\_ADC\_ACC}$		–2	--	2	LSB
TS_BAT Measurement Range	TS_{BAT_MR}		0	--	100	%
TS_BAT Resolution	TS_{BAT_RES}		--	0.25	--	%
TS_BAT Accuracy	TS_{BAT_ACC}		–2	--	2	LSB
IBUS Measurement Range	$I_{IBAT\_ADC\_MR}$		0	--	3.25	A
IBUS Resolution	$I_{IBAT\_ADC\_RES}$		--	50	--	mA
IBUS Accuracy	$I_{IBAT\_ADC\_ACC}$		–2	--	2	LSB
IBAT Measurement Range	$I_{IBAT\_ADC\_MR}$		0	--	5	A
IBAT Resolution	$I_{IBAT\_ADC\_RES}$		--	50	--	mA
IBAT Accuracy	$I_{IBAT\_ADC\_ACC}$		–2	--	2	LSB
TEMP_JC Measurement Range	$T_{TEMP\_JC\_ADC\_MR}$		–40	--	120	°C
TEMP_JC Resolution	$T_{TEMP\_JC\_ADC\_RES}$		--	2	--	°C
TEMP_JC Accuracy	$T_{TEMP\_JC\_ADC\_ACC}$	Temperature < 85°C	–2	--	2	LSB

12 Typical Application Circuit

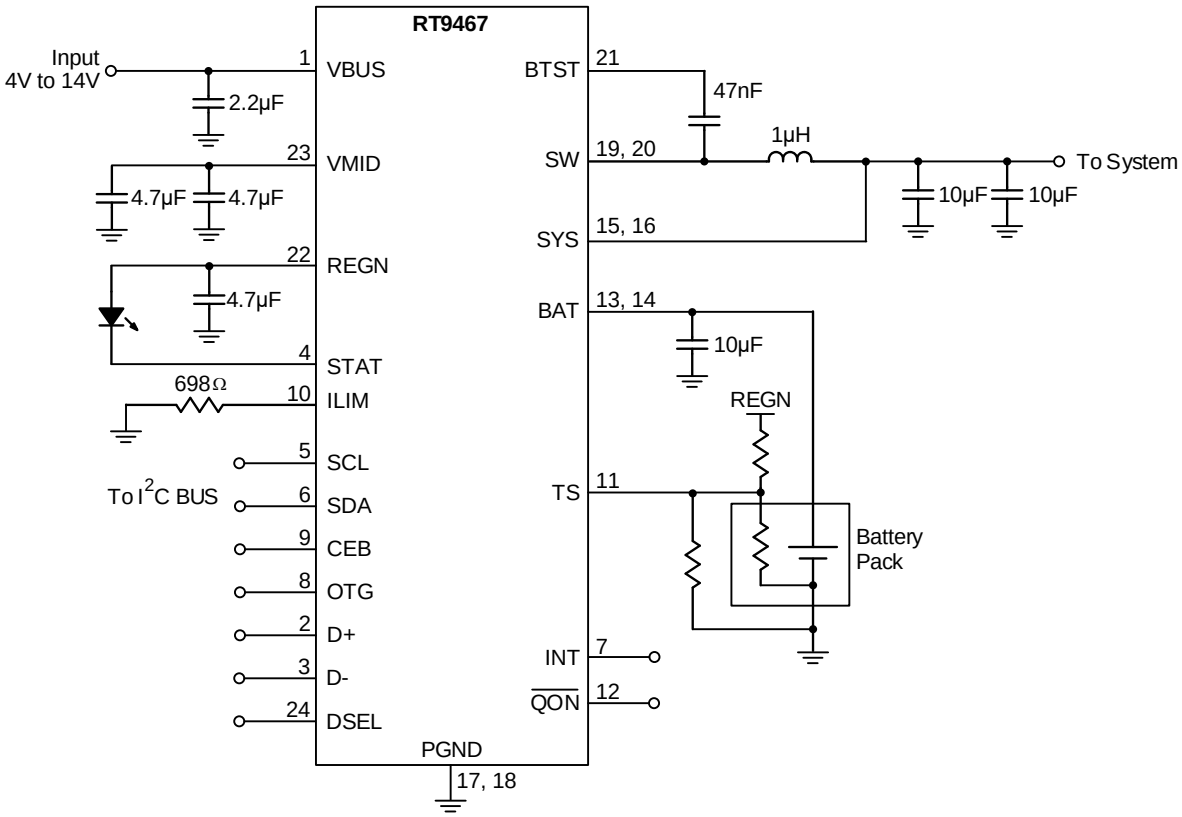
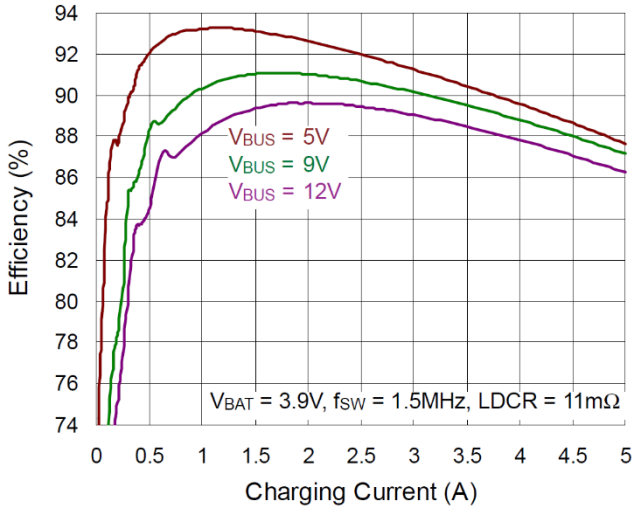


Table 1. Recommended Components Information

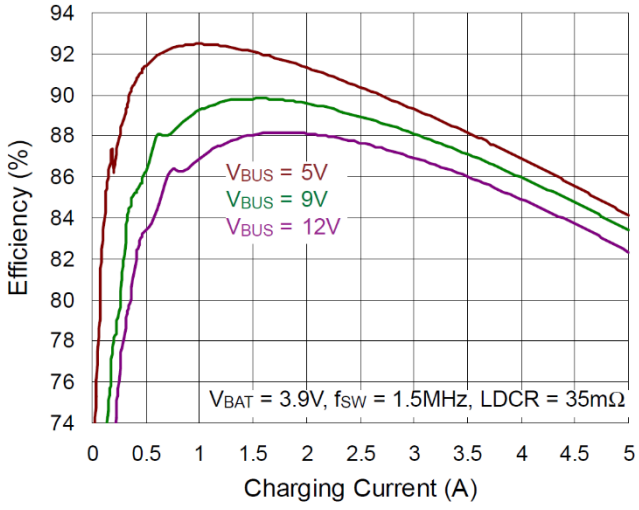
Pin	Description	Part Number	Package	Manufacturer
VBUS	2.2µF/25V/X5R	GRM155R61E225KE11	0402	muRata
VMID	4.7µF/25V/X5R	GRM188R61E475KE11	0603	muRata
BTST	47nF/16V/X5R	GRM033R61C473KE84	0201	muRata
SYS	10µF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
BAT	10µF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
REGN	4.7µF/6.3V/X5R	GRM155R60J475ME47	0402	muRata
SW	1µH/20%	DFE252012F-1R0	2.5 x 2mm	TOKO
ILIM	698Ω/1%	RR0306S-6980-FNH	0201	CYNTEC

13 Typical Operating Characteristics

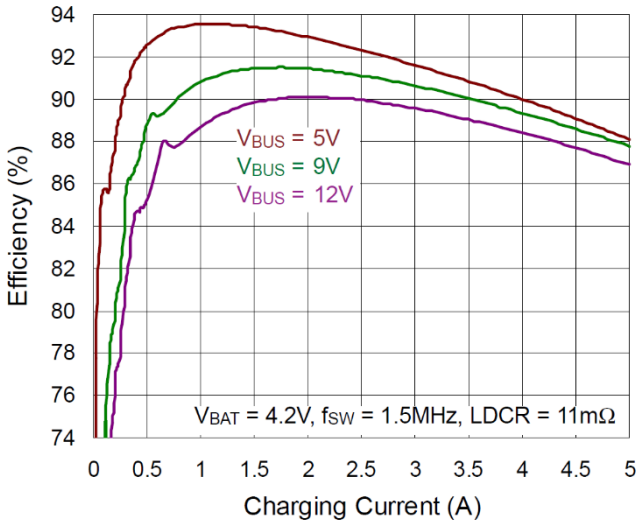
Charger Efficiency vs. Charging Current



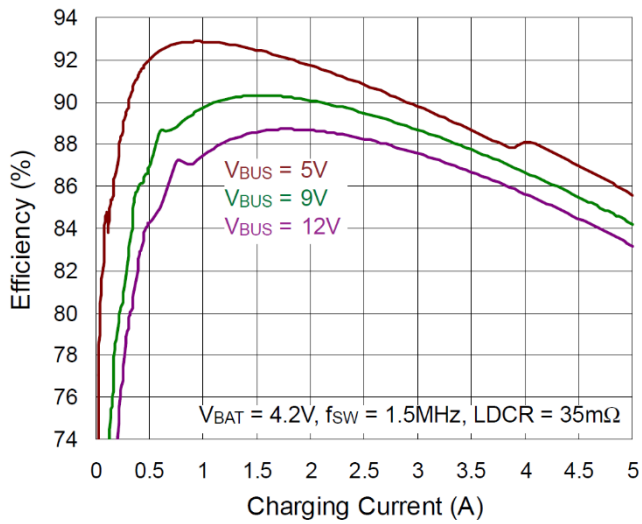
Charger Efficiency vs. Charging Current



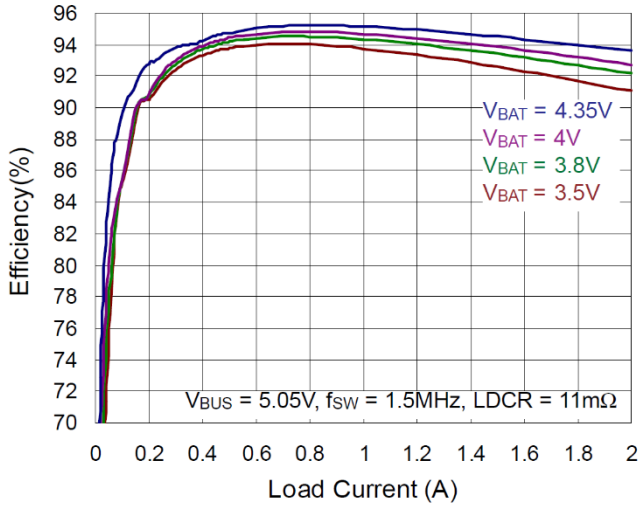
Charger Efficiency vs. Charging Current



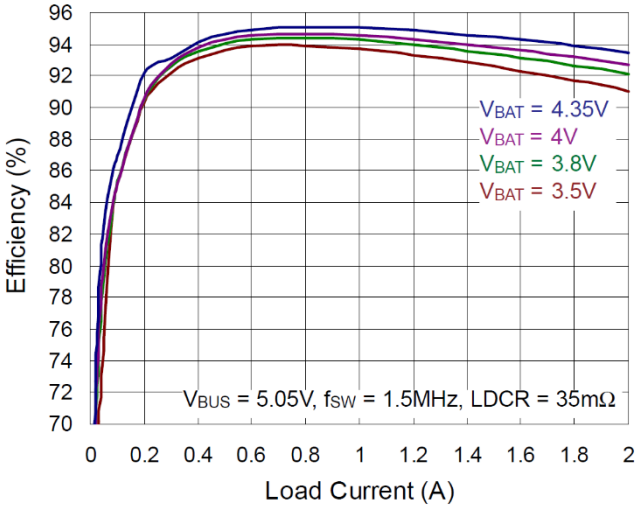
Charger Efficiency vs. Charging Current

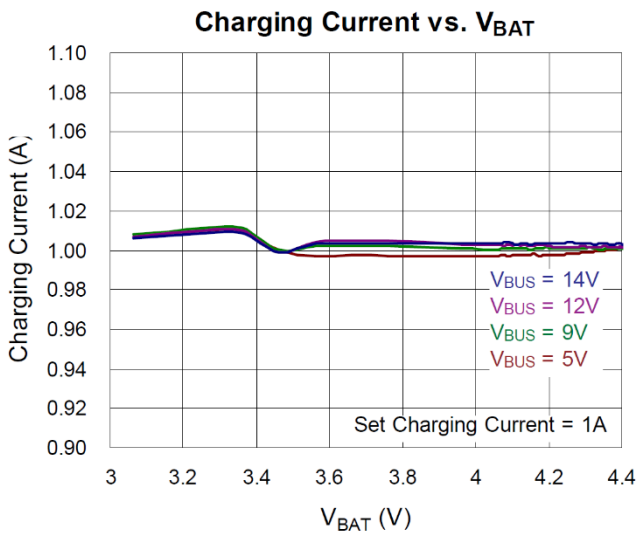


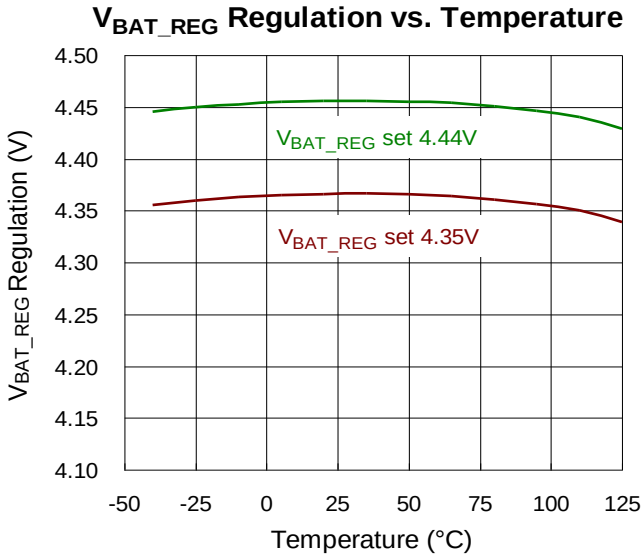
Boost Efficiency vs. Load Current

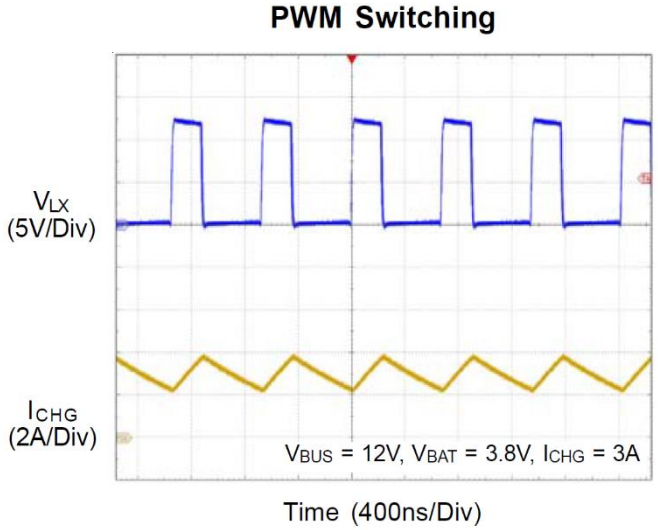


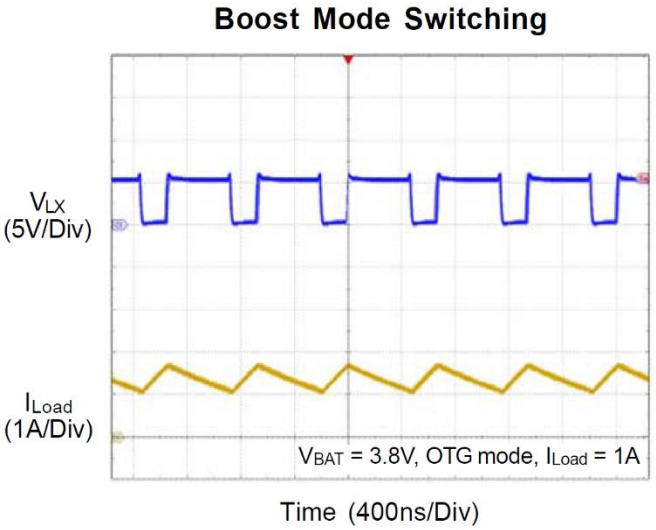
Boost Efficiency vs. Load Current











14 Operation

The RT9467 is an integrated single-cell Li-ion battery switching charger with a power path controller.

14.1 Base Circuits

The base circuits provide the internal power, VREGN, reference voltage, and bias current.

14.2 Protection Circuits

The protection circuits include the VINOVP, VINUVLO, BATOVP, and OTP circuits. The protection circuits turn off the charging when the input power or die temperature is at an abnormal level.

14.3 Buck Regulator for Charging and Boost Regulator as OTG

The multi-loop controller controls the operation of the charging process and current supply to the system. It also controls the circuits as a boost converter for OTG applications.

14.4 Battery Detection

The RT9467 is capable of performing battery absence detection. The detection protects the charger when the battery is removed accidentally.

14.5 Adapter Detection

If a poor input power source is connected to the RT9467, the operation will be shut down by the adapter detection.

14.6 Power Path Management and Control

Once the battery voltage increases to a defined system minimum regulation voltage, the internal path between SYS and BAT will be fully turned on, achieving better charging efficiency. When the end of charge occurs, the charging will stop, and the internal path will be turned off.

14.7 USB Charger Detection

The RT9467 can detect and distinguish Standard Downstream Port, Charging Downstream Port, and Dedicated Charging Port via the DP and DM pins.

14.8 TS Detection

The RT9467 detects the temperature of the battery pack via the REGN and TS pins. The REGN pin provides a constant voltage source to drive the voltage divider composed of a pull-up resister and an NTC resister. The RT9467 reports the sensing results via IRQ and status bits for COLD, COOL, WARM, and HOT.

14.9 I^2C Controller

The key parameters of charging and OTG are programmable through I^2C commands.

15 Application Information

(Note 7)

15.1 Switching Charger

The switching charger integrates a synchronous PWM controller with power MOSFETs to provide Minimum Input Voltage Regulation (MIVR), Average Input Current Regulation (AICR), high-accuracy current and voltage regulation, and charge termination. The charger also features OTG (On-The-Go) Boost Mode.

The switching charger has three operation modes: charge mode, boost mode (OTG-Boost), and high-impedance mode. In charge mode, the charger supports a precision charging system for single-cell batteries. In boost mode, the charger works as a boost converter to boost the battery voltage back to the VBUS pin for sourcing OTG devices. In high-impedance mode, the charger stops charging or boosting and operates at a low current sunk from the VBUS pin or the battery to reduce power consumption when the device is in standby mode.

15.2 Charge Mode Operation

15.2.1 Battery Charge Profile

The device charges the battery in four states: trickle charge, pre-charge, constant current, and constant voltage. Users can set the voltage threshold and charge current rating in pre-charge, constant current, and constant voltage via the I^{2}C interface. In portable device applications, changing the adapter's output to higher than 5V is a general solution to achieve fast charging. For this kind of application, users must set the VBUS back to 5V when the charger enters constant voltage and the charge current is lower than 1A. Refer to application note document AN065 for detailed information.

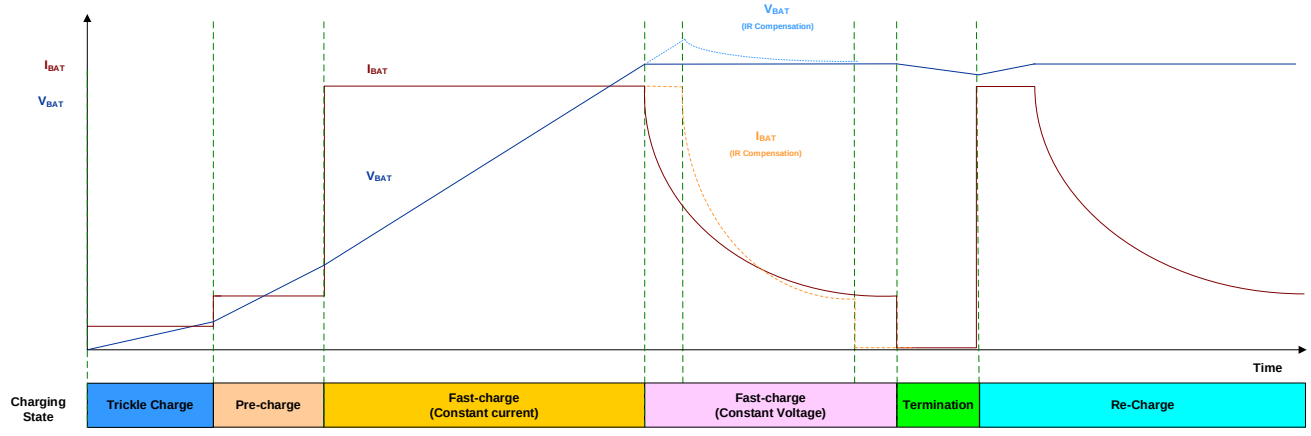


Figure 1. Charging Profile

15.2.2 Minimum Input Voltage Regulation

The switching charger features Minimum Input Voltage Regulation (MIVR) function to prevent input voltage drop due to insufficient current provided from the adapter or USB input. If MIVR function is enabled, the input voltage decreases if the overcurrent condition of the input power source occurs. The VBUS voltage is regulated at a predetermined voltage level which can be set from 3.9V to 13.4V in 0.1V increments via the I^{2}C interface. At this time, the current drawn by the switching charger equals the maximum current value that the input power can provide at the predetermined voltage level, instead of the set value.

15.2.3 Pre-Charge Mode

For life-cycle consideration, the battery cannot be charged with large current under low-battery conditions. When the BAT voltage is below pre-charge threshold voltage, the charger is in pre-charge mode with a weak charge current, which is equal to the pre-charge current.

There are two control loops in the pre-charge mode: ICHG and SYSREG. If the battery voltage is lower than the SYS voltage, the MOSFET will not be fully turned on so the V_{SYS} is not equal to V_{BAT}. This means that the V_{SYS} can be powered from the buck converter rather than the low battery, which is in pre-charge mode. As a result, the system power can be guaranteed in this low-battery condition.

15.2.4 Fast-Charge Mode and Settings

As the BAT voltage rises above V_{PRECHG}, the charger enters fast-charge mode and starts charging. Notice that the MUIC integrates input power source (AC adapter or USB input) detection. Thus, the switching charger can set the charge current via options automatically. Unlike the linear charger (LDO), the switching charger (buck converter) is like a current amplifier, where the current drawn by the switching charger differs from the current supplied to the battery.

Average Input Current Regulation (AICR) level and the output charge current (I_{CHG}) can be set independently.

15.2.5 Cycle-by-Cycle Current Limit

The switching charger includes a cycle-by-cycle current limit for the output inductor. Once the inductor current reaches the current limit, the charger stops charging immediately to prevent overcurrent conditions and damage to the device. Note that this protection can never be disabled.

15.2.6 Average Input Current Regulation

The Average Input Current Regulation (AICR) levels can be set via the I^2C interface. For example, the AICR100 mode limits the input current to 100mA, and AICR500 mode to 500mA. This function can be disabled if not needed. The AICR current levels are in the range of 100mA to 3250mA with a resolution of 50mA.

15.2.7 Average Input Current Level

The Average Input Current Level (AICL) levels can be set via the I^2C interface (0x0E[7:0]). When the IAICR is set to a large current and the VBUS voltage drops to the VMIVR level, the AICL measurement mechanism will automatically decrease the IAICR level step by step until the VBUS voltage exceeds the AICL threshold voltage.

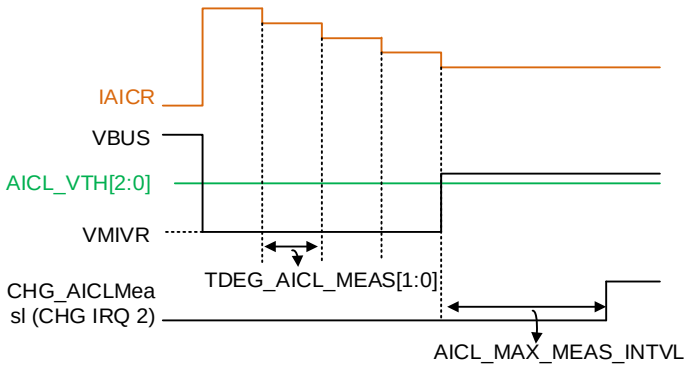


Figure 2. AICL Enable

15.2.8 Charge Current

The charge current (I_{CHG}) into the battery is determined by the power path sensing R_{ON} and the I_{CHG} setting via I^2C. The voltage between the SYS and BAT pins is regulated by the I_{CHG} setting, and the fast-charge currents range from 100mA to 5000mA in increments of 100mA, programmable via I^2C.

15.2.9 Constant Voltage Mode

The switching charger enters constant voltage mode when the BAT voltage is closed to the output-charge voltage (V_{BAT_REG}). In this mode, the charge current begins to decrease. For the default settings (charge current termination is disabled), the switching charger does not turn off and always regulates the battery voltage at V_{BAT_REG}. However, once the charge current termination is enabled, the charger terminates if the charge current is below the termination current (I_{EOC}) in constant-voltage mode. The output-charge voltage is set by the I^2C interface. Its range is from 3.9V to 4.71V in increments of 10mV.

15.3 End-of-Charge Current

If the charger current termination is enabled, the end-of-charge current (I_{EOC}) is determined by the termination current sense voltage (V_{EOC}). IEOC is set by the I^2C interface from 100mA to 850mA in steps of 50mA.

15.4 Charge Trip

When the input power source is plugged in, the RT9467 checks the current sourcing capability of the input power source when V_{BUS} exceeds 3.3V. The following conditions should be met to start battery charging:

1. VBUS is below 14V (for example, V_{BUS_OVP}).
2. VBUS is above 3.8V (for example, V_{BAD_ADP}) when sinking 50mA (for example, $I_{BAD\_ADP\_SNK}$) during 30ms of detection period, t_{BADADP_DET}. This detection function can be disabled by the ADP_DIS (0x0B, bit 7) register bit.

The charge modes are as follows, and the charge mode in which the charger operates will be determined according to the V_{BAT} level:

	Battery Voltage Level V_{BAT}	Battery Charge Current I_{BAT}
Trickle Mode	V_{BAT} < 2V	100mA
Pre-Charge Mode	V_{BAT} < V_{BAT_REG} (0x08, bit[7:4])	IPREC (0x08, bit[3:0])
Fast-Charge Mode	V_{BAT} < V_{BAT_REG} (0x04, bit[7:1])	Charge current is determined by several control loops
End-of-Charge Mode	V_{BAT} = V_{BAT_REG} (0x04, bit[7:1])	Charge current decreases naturally

In fast-charge mode, the input current limit can be selected by IINLMTSEL (0x02, bit[3:2]). This flexible setting is suitable for a wide range of adapter applications. In addition, the RT9467 also provides charger warning statuses, such as MIVR, AICR and TREG (0x50, bit[6:4]), to host.

There are 2 register bits related to the SW switching of the RT9467:

1. SEL_SWFREQ (0x01, bit 7):
   - If SEL_SWFREQ is disabled (set to 0), the switching frequency is 1.5MHz (default).
   - If SEL_SWFREQ is enabled (set to 1), the switching frequency is 0.75MHz.
2. FIXFREQ (0x01, bit 6):
   - If FIXFREQ is disabled (set to 0), the charge switching frequency will vary when VBUS is close to VBAT.
   - If FIXFREQ is enabled (set to 1), the charger switching frequency is fixed.

There are 3 enable bits related to the charger:

1. CFO_EN (0x02, bit 1): This bit is used to enable or disable the charger and boost.
2. CHG_EN (0x02, bit 0): When CHG_EN bit is disabled, the power path MOSFET will be turned off, resulting in zero charging current. At this time, the input power source continuously delivers power to the system without charging the battery. However, if the system load is larger than the input source current limit, the power path MOSFET will be turned back on immediately to supply power to the system. The CHG_EN bit function is the same as the CEB pin.
3. HZ (0x01, bit 2): When the HZ bit is enabled, most of the charger's internal circuits will be turned off to reduce quiescent current.

In end-of-charge mode, if EOC_EN (0x09, bit 3) is enabled, once the charge current is lower than the IEOC (0x09, bit[7:4]) level and within CHG_TEDG_EOC (0x09, bit[2:0]), the RT9467 will send out an INT and set CHG_IEOCI = 1 (0x54, bit 7). Then, the RT9467 will start to check statuses of the following three bits:

1. TE (0x02, bit 4): If this bit is enabled, the power path will be turned off, and the buck converter of the charger will keep providing power to the system.
2. EOC_TIMER (0x07, bit[1:0]): With CHG_IEOC1 = 1, the power path will not be turned off. The RT9467 can keep charging the battery for 30 to 60 minutes to extend battery charging capacity.
3. BATD_EN (0x0B, bit 6): After charge is done, the RT9467 will start to sink a sink current of I_{BAT_SNK} 375mA for about 256ms from the battery. If VBAT drops to trigger the recharge function, it indicates that the battery is not connected to the charger. The RT9467 will continue battery detection every two seconds.

15.5 OTG Mode

The RT9467 also supports OTG mode. It not only provides several output current-limit protection levels, but also has low battery protection for overall system considerations. The RT9467 can select the switching frequency via SEL_SWFREQ (0x01, bit 7), whether the RT9467 is already operating in OTG mode.

Two methods are available to enable OTG mode:

1. Via software: Through I^2C to set OPA_MODE (0x01, bit 0).
2. Via hardware: Through I^2C to set OTG_PIN_EN (0x01, bit 1) and OPA_MODE (0x01, bit 0). Users can then use GPIO to change the OTG pin level to enter/exit OTG mode.

The RT9467 also provides UUG_ON (0x0D, bit 1) bit, which can be applied to different applications:

1. If OTG mode and UUG_ON are enabled, the boost-mode output is on the VBUS pin, which can be used for OTG (On-the-Go) mode in mobile phones.
2. If OTG mode is enabled and the UUG_ON bit is disabled, the boost-mode output is on the VMID pin, which can be used in power banks, meaning that adapter power can be delivered directly to the PD (Powered Device).

15.6 Shipping Mode

From manufacture to an end user, it may take a long time for products to travel. In view of this, the RT9467 provides a shipping mode to further minimize battery leakage. After enabling SHIP_MODE (0x02, bit 7), the RT9467 will shut down internal circuits to reduce quiescent current. The delay time for BATFET to be turned off can be selected by BATDET_DIS_DLY (0x02, bit 6). Below are several ways to exit shipping mode:

1. Input power source is plugged in.
2. Disable the SHIP_MODE bit.
3. The $\overline{QON}$ pin is pulled from Logic High to Logic Low within 1 second.
4. Enable RST_REG (0x00, bit 7) to reset all registers to default values.

15.7 MeidaTek Pump Express+ (MTK, PE+)

The RT9467 can provide an input current pulse to communicate with an MTK-PE+ high voltage adapter. When EN_PUMPX (0x19, bit 7) is enabled, the host can increase or decrease the adapter output voltage by setting PUMPX_UP_DN to the desired value. After enabling either one of them, the RT9467 will generate a VBUS current pattern for the MTK-PE+ adapter to automatically identify whether to increase or decrease the output voltage (VBUS pin). Once the current pattern is finished, an INT will be triggered accordingly to request the processor to read the registers.

15.8 JEITA Protection

JEITA protection is implemented in the RT9467 to achieve battery thermal protection. JEITA guidelines were released in 2007. It includes warm and cool protection (Cool section is between T1 and T2; warm section is between T3 and T4, see the figure below). When the battery temperature is in the warm section, the RT9467 will lower the charge voltage (V_{BAT_REG}) by 200mV. If the battery is in the cool section, the charger will reduce the charge current (by half of the CC mode current). The RT9467 will stop charging the battery if the battery temperature is lower than T1 or higher than T4.

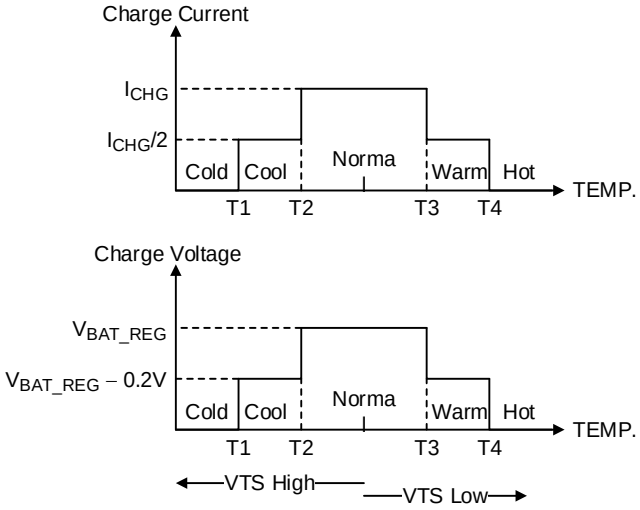


Figure 3. JEITA Protect for Charging Current and Voltage

The thermal condition of a battery can be monitored by the TS pin. There are four sections implemented for JEITA protection. Based on R_{HOT} and R_{COLD}, R_{T1} and R_{T2} can be calculated using equation (1) and equation (2). Here, R_{HOT} represents the NTC resistance of the battery over-temperature threshold, and R_{COLD} represents the NTC resistance of the battery under-temperature threshold.

$$R_{T1} = V_{REGN} \times [(1/V_{T1} - 1/V_{T4})/(1/R_{COLD} - 1/R_{HOT})] \quad (1)$$

$$R_{T2} = R_{T1} \times [1/(V_{REGN}/V_{T1} - R_{T1}/R_{COLD} - 1)] \quad (2)$$

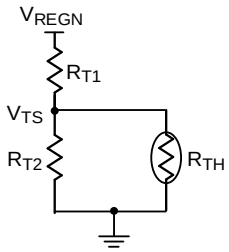


Figure 4. Schematic of TS Pin

The respective percentages of the voltages at T1 to T4 are shown in the following table.

No.	Parameter	Symbol	Condition	$\frac{V_{TS}}{V_{REGN}}$	Units
1	T1 (0°C) Threshold	V_{T1}	V_{TS} rising, as percentage to V_{REGN}	73.5	%
2	T1 Hysteresis	V_{T1_HYS}	Hysteresis, V_{TS} falling	2	%
3	T2 (10°C) Threshold	V_{T2}	V_{TS} rising, as percentage to V_{REGN}	68.5	%
4	T2 Hysteresis	V_{T2_HYS}	Hysteresis, V_{TS} falling	2	%
5	T3 (45°C) Threshold	V_{T3}	V_{TS} falling, as percentage to V_{REGN}	45	%
6	T3 Hysteresis	V_{T3_HYS}	Hysteresis, V_{TS} rising	2	%
7	T4 (60°C) Threshold	V_{T4}	V_{TS} falling, as percentage to V_{REGN}	34.5	%
8	T4 Hysteresis	V_{T4_HYS}	Hysteresis, V_{TS} rising	2	%

15.9 Analog IR Drop Compensation

Since the resistance between the charger output and the battery cell terminal can force a premature shift from constant current mode to constant voltage mode, thereby increasing charging time. To expedite the charging cycle, the RT9467 provides an analog IR drop compensation function to deliver maximum power to the battery and extend the constant current mode charging time. The host (AP) can set the IR compensation function using BAT_COM (0x1A bit[5:3]) and VCLAMP (0x1A bit[2:0]).

$V_{ACTUAL} = V + \min (I_{CHG\_ACTUAL} \times BAT\_COM, V_{CLAMP})$

15.10 DSEL Pin

The DSEL pin is an open-drain output. When the device starts to detect the input supply source, DSEL drives Low to indicate the detection is in progress and the device needs to take control of the D+ and D- signals. When detection is completed, DSEL holds low if DCP (Dedicated Charging Port) /HVDCP adapter is detected. DSEL returns to high if an SDP (Standard Downstream Port)/CDP (Charging Downstream Port) is detected.

15.11 STAT Pin

There are two ways to check the status of the RT9467:

1. Hardware checking: The STAT pin of the RT9467 is an open-drain output used to indicate charge statuses, which are summarized in Table 2. This applies to charge mode only.
2. Software checking: The status of the RT9467 is indicated in the register at address 0x42 as follows:
   - CHG_STAT: Charger status

- BOOST_STAT: Boost mode status
- ADC_STAT: ADC status. Check whether the ADC is active or idle

Table 2. Charge Status Indication

Charge Status	STAT Pin Output
Charge is in progress.	LOW
Charge is done.	HIGH
Charge is disabled.	HIGH
Any fault occurs.	Blink at 1Hz

15.12 Interrupt

The RT9467 reports status to the host (CPU, MCU, EC, etc.) by the INT (interrupt to host) pin, which is an open-drain output. The INT pin goes low when any fault occurs. It will be automatically reset when all the fault flags are cleared. The IRQ_Pulse (0x01, bit 3) provides a reminder function. If the system is interrupted by the interrupt signal but does not take any action to check the registers, the INT pin will be released every 2 seconds and be triggered again.

The RT9467 INT pin is used to indicate whether the any charging events occur. When the AP (Access Point) detects a falling edge on the INT pin, the AP starts to read the INT register 0x51 to 0x56 sequentially. However, if any of the events is triggered again during this checking period, it will be miss. If any of the INT registers are not checked, the INT_REZ bit can help release the INT pin for 2ms and then reset it again in order to remind the host of the missing events again.

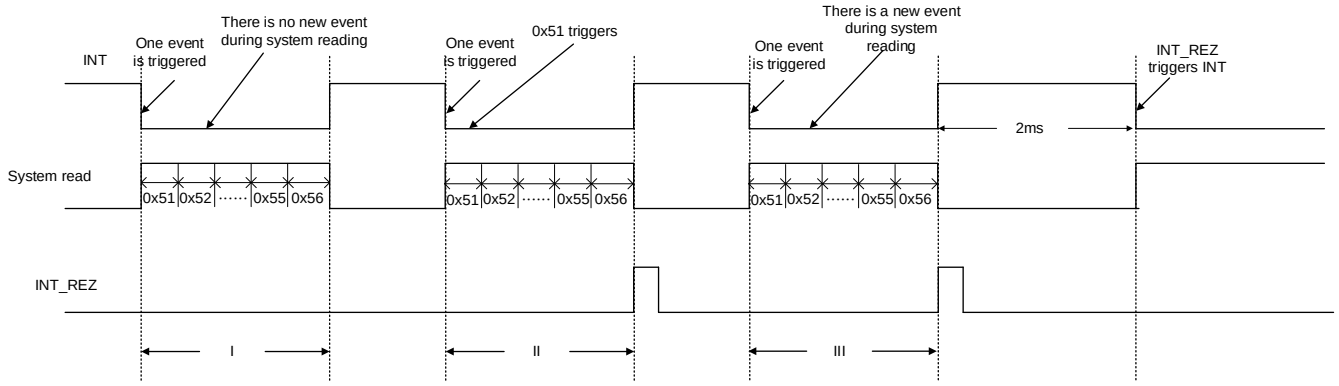


Figure 5. Interrupt Behavior

15.13 ILIM Pin

For hardware protection, the RT9467 supports input current limit setting on the ILIM pin by way of a resistor from the ILIM pin to ground.

$I_{INMAX} = K_{ILIM}/R_{ILIM}$

For example, if the input current limit is to be set as 2A with a typical input current limit factor K_{ILIM} as 355AΩ, a resistor of 180Ω will then be chosen as the resistor from the ILIM pin to ground. The actual input current limit is the minimum between the result of IINLMTSEL (0x02, bit[3:2]) and ILIM.

15.14 ADC Conversion Operation Flow

The figure below shows the flow chart of ADC conversion operation. ADC conversion starts from selecting an ADC channel by setting ADC_IN_SEL (0x11, bit[7:4]) and enabling ADC_START (0x11, bit 0). After about 200ms of ADC conversion time for a conversion to be completed, ADC_DONEI (0x55, bit 0) will be enabled and ADC_STAT (0x42, bit 0) will be disabled. The host can be informed that ADC conversion is completed by reading the register bits.

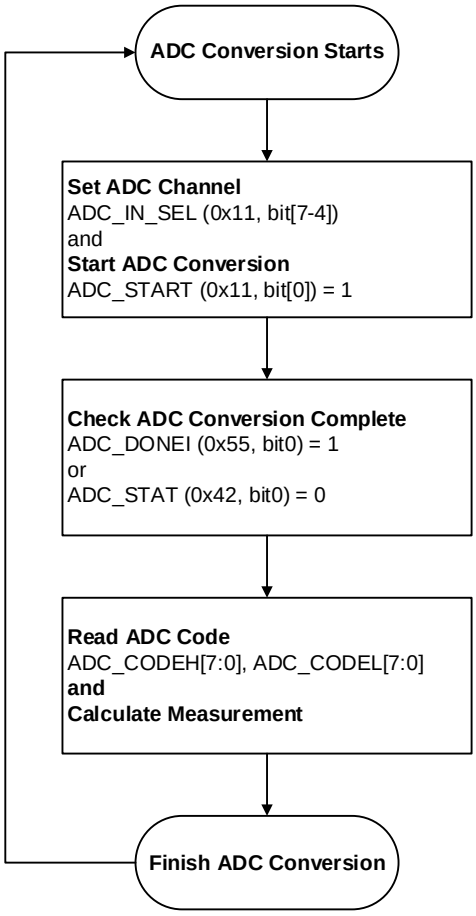


Figure 6. ADC Flow Chart

The host can read ADC high-byte codes from ADC_CODEH (0x44, bit 7-0) and low-byte codes from ADC_CODEL (0x45, bit 7-0) to calculate the measured voltage/current/temperature data with respect to each ADC channel. The table below shows measurement equations for various ADC channels. When measuring IBUS, the AICR setting needs to be at least 350mA. When measuring I_{BAT}, the ICHG setting needs to be at least 1A.

ADC Channel	Measurement Equation	Measurement Range
VBUS_DIV5	[(ADC_CODEH x 256) + ADC_CODEL] x 25mV	1V to 22V
VBUS_DIV2	[(ADC_CODEH x 256) + ADC_CODEL] x 10mV	1V to 9.8V
VBAT	[(ADC_CODEH x 256) + ADC_CODEL] x 5mV	0V to 4.9V
VSYS	[(ADC_CODEH x 256) + ADC_CODEL] x 5mV	0V to 4.9V
REGN	[(ADC_CODEH x 256) + ADC_CODEL] x 5mV	0V to 4.9V

ADC Channel	Measurement Equation	Measurement Range
TS_BAT	[(ADC_CODEH x 256) + ADC_CODEL] x 0.25%	0% to 100%
IBUS IAICR[5:0] Setting < 400mA	[(ADC_CODEH x 256) + ADC_CODEL] x 50mA x 0.67	0A to 0.4A
IBUS IAICR[5:0] Setting ≥ 400mA	[(ADC_CODEH x 256) + ADC_CODEL] x 50mA	0A to 3.25A
IBAT ICHG[5:0] Setting 100mA to 450mA	[(ADC_CODEH x 256) + ADC_CODEL] x 50mA x 0.57	0A to 0.45A
IBAT ICHG[5:0] Setting 500mA to 850mA	[(ADC_CODEH x 256) + ADC_CODEL] x 50mA x 0.63	0A to 0.85A
IBAT ICHG[5:0] Setting ≥ 900mA	[(ADC_CODEH x 256) + ADC_CODEL] x 50mA	0A to 5A
TEMP_JC	[(ADC_CODEH x 256) + ADC_CODEL] x 2°C – 40°C	–40°C to 120°C

15.15 I²C Interface Timing Diagram

The RT9467 acts as an I²C – bus slave. The I²C – bus master configures the settings for charge mode and boost mode by sending command bytes to the RT9467 via the 2-wire I²C – bus. After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The second byte selects the register to which the data will be written. The third byte contains data to be written to the selected register.

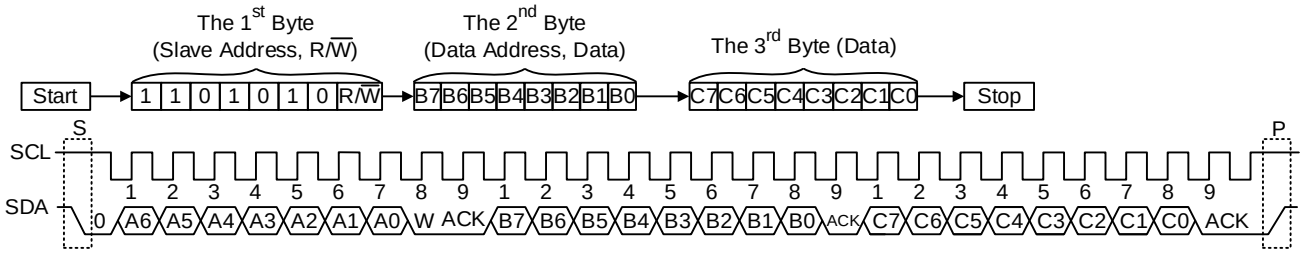


Figure 7. I²C Read and Write Function

15.16 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-

24L 4x4 package, the thermal resistance, θ_{JA}, is 22°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C)/(22°C/W) = 4.54W for a WQFN-24L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

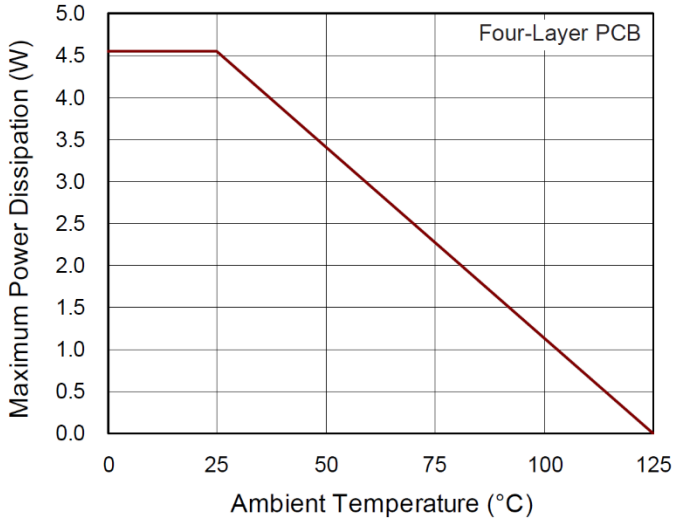


Figure 8. Derating Curve of Maximum Power Dissipation

15.17 Layout Considerations

The RT9467 layout guidelines are shown below, and several suggestions are provided:

- The bypass capacitor, connected from the REGN pin to AGND, should be placed as close to the IC as possible.
- AGND should be connected to PGND via the GND plane.
- The capacitor connected to the VMID pin should be placed as close as possible to the IC to reduce EMI. The recommended trace length from the IC VMID pads to the VMID capacitor should not be longer than 100 mil.
- The boot capacitor, connected from the BTST pin to the SW pin, should be placed as close to the IC as possible. The recommended trace length from the IC BTST pads to the BTST capacitor should not be longer than 40 mil.
- The inductor should be placed as close to the IC as possible. The recommended trace length from the IC SW pads to the inductor should not be longer than 180 mil.
- The GND paths of both capacitors, connected to the VMID pin and the VBUS pin, need to be connected together at the TOP layer.
- PGND is connected to the thermal heat sink to improve thermal performance.

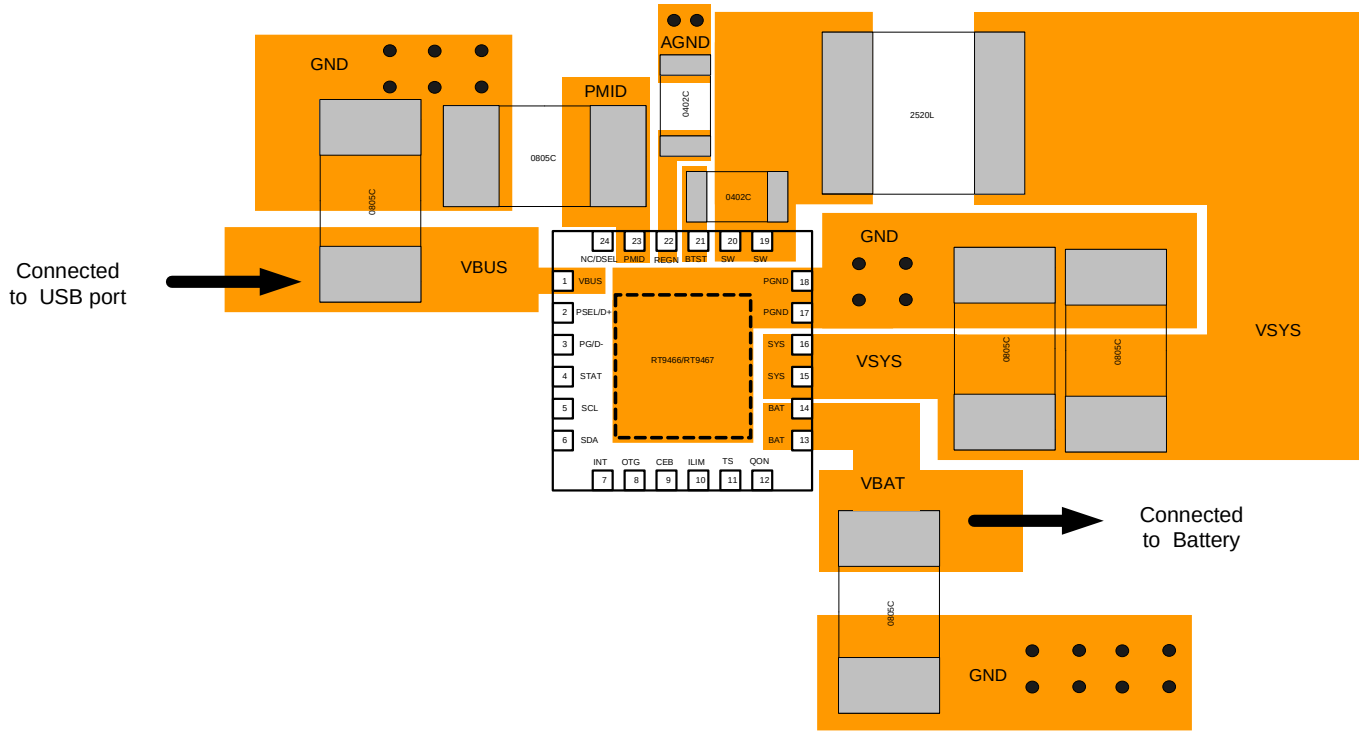


Figure 9. PCB Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

16 Functional Register Description

I²C Slave Address: 1011011 (5BH)

Name		Function	Addr	Reset
CORE_CTRL0		Control 0	0x00	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	RST_REG	0	All registers reset bit. 0: Do not reset all registers. 1: Reset all registers. Notice: 1. This bit will be reset to "0" after the reset procedure finishes. 2. In high-impedance mode, this bit resets all registers after leaving high-impedance mode.
6:0	R/W	Reversed	0000000	Reversed

Name		Function	Addr	Reset
CHG_CTRL1		Control 1	0x01	0x10
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	SEL_SWFREQ	0	The switching frequency selection bit (Charger/OTG) 0: The switching frequency is 1.5MHz. (default) 1: The switching frequency is 0.75MHz.
6	R/W	FIXFREQ	0	Charger switching frequency 0: Charger switching frequency will be varied if VBUS is close to VBAT (default) 1: Charger switching frequency is fixed
5	R/W	Reversed	0	Reversed
4	R/W	STAT_EN	1	Charger STAT pin function 0: Disable 1: Enable (default)
3	R/W	IRQ_PULSE	0	IRQ reminder function 0: IRQ reminder is disabled (default) 1: IRQ reminder is enabled. If IRQ is triggered but no check action, the INT pin will be released as well as being triggered again with every 2s intervals
2	R/W	HZ	0	High-impedance selection 0: No high-impedance mode (default) 1: High-impedance mode
1	R/W	OTG_PIN_EN	0	Boost mode enable with the OTG pin 0: Enable boost mode by OPA_MODE (default) 1: Enable boost by both OPA_MODE bit and the OTG pin
0	R/W	OPA_MODE	0	Boost mode enable 0: Charge mode (default) 1: Boost mode for OTG

Name		Function	Addr	Reset
CHG CTRL 2		Charger Control 2	0x02	0x03
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	SHIP_MODE	0	Shipping mode enable, force BATFET OFF 0: Allow BATFET turn on (default) 1: Force BATFET turn off
6	R/W	BATDET_DIS_DLY	0	BATFET turn off delay 0: BATFET turns off immediately (default) 1: BATFET turns off with a 10s delay after the SHIP_MODE bit is set
5	R/W	Reserved	0	Reserved
4	R/W	TE	0	Termination enable 0: Disable charge current termination (default) 1: Enable charge current termination
3:2	R/W	IINLMTSEL	00	Input current limit selection bit 00: Input limit is set as 3.25A (default) 01: CHG_TYP results are applied from D+/D- detection 10: IAICR[5:0] results is applied 11: Input limit is set by the lower level of these three
1	R/W	CFO_EN	1	Charger and OTG enable 0: Charger and OTG disable 1: Charger and OTG enable (default)
0	R/W	CHG_EN	1	Charger enable 0: Charger is disabled 1: Charger is enabled (default)

Name		Function	Addr	Reset
CHG_CTRL4		Control 4	0x04	0x3C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:1	R/W	VBAT_REG[6:0]	0011110	Battery regulation voltage. The delta-V of the battery regulation voltage is 10mV. 0000000: 3.9V 0000001: 3.91V 0000010: 3.92V 0000011: 3.93V … 0011101: 4.19V 0011110: 4.2V (default) 0011111: 4.21V … 0101100: 4.34V 0101101: 4.35V 0101110: 4.36V ... 1010001: 4.71V 1010001 to 1111111: 4.71V
0	R/W	Reserved	0	Reserved

Name		Function	Addr	Reset
CHG_CTRL5		Control 5	0x05	0x67
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:2	R/W	VOTGBST[5:0]	011001	OTG boost-mode output regulation voltage. The delta-V of the OTG regulation voltage is 25mV. 000000: 4.425V 000001: 4.45V 000010: 4.475V … 010111: 5V 011000: 5.025V 011001: 5.05V (default) 011010: 5.075V 011011: 5.1V ... 111000: 5.825V 111001 to 111111: 5.825V
1:0	R/W	THREG[1:0]	11	Charger thermal regulation threshold 00: 60°C 01: 80°C 10: 100°C 11: 120°C (default)

Name		Function	Addr	Reset
CHG_CTRL6		Control 6	0x06	0x0B
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:1	R/W	VMIVR[6:0]	0000101	Input MIVR threshold 0000000: 3.9V 0000001: 4V 0000010: 4.1V 0000011: 4.2V 0000100: 4.3V 0000101: 4.4V (default) 0000110: 4.5V … 0011110: 6.9V 0011111: 7V … 0110010: 8.9V 0110011: 9V … 1010000: 11.9V 1010001: 12V … 1011111: 13.4V 1100000 to 1111111: 13.4V
0	R/W	MIVR_EN	1	MIVR loop enable 0: MIVR loop disable 1: MIVR loop enable (default)

Name		Function	Addr	Reset
CHG_CTRL7		Control 7	0x07	0x4C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:2	R/W	ICHG[5:0]	010011	Charging regulation current 000000: 0.1A 000001: 0.2A 000010: 0.3A ... 001000: 0.9A 001001: 1A 001010: 1.1A ... 010010: 1.9A 010011: 2A (default) ... 011100: 2.9A 011101: 3A … 100110: 3.9A 100111: 4A … 110000: 4.9A 110001: 5A 110010 to 111111: 5A Note: When ICHG is set above 2.5A, it is recommended to set the OCP to a higher level. (Addr 0x0D[2] = 1)
1:0	R/W	EOC_TIMER[1:0]	00	EOC back-charging time 00: 0mins (default) 01: 30mins 10: 45mins 11: 60mins

Name		Function	Addr	Reset
CHG_CTRL8		Control 8	0x08	0xA1
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:4	R/W	VPREC[3:0]	1010	Pre-Charge voltage threshold 0000: 2V 0001: 2.1V 0010: 2.2V 0011: 2.3V 0100: 2.4V 0101: 2.5V 0110: 2.6V 0111: 2.7V 1000: 2.8V 1001: 2.9V 1010: 3.0V (default) 1011: 3.1V 1100: 3.2V 1101: 3.3V 1110: 3.4V 1111: 3.5V
3:0	R/W	IPREC[3:0]	0001	Pre-Charge current threshold 0000: 100mA 0001: 150mA (default) 0010: 200mA 0011: 250mA 0100: 300mA 0101: 350mA 0110: 400mA 0111: 450mA 1000: 500mA 1001: 550mA 1010: 600mA 1011: 650mA 1100: 700mA 1101: 750mA 1110: 800mA 1111: 850mA

Name		Function	Addr	Reset
CHG_CTRL9		Control 9	0x09	0x3C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:4	R/W	IEOC[3:0]	0011	EOC current 0000: 100mA 0001: 150mA 0010: 200mA 0011: 250mA (default) 0100: 300mA 0101: 350mA 0110: 400mA 0111: 450mA 1000: 500mA 1001: 550mA 1010: 600mA 1011: 650mA 1100: 700mA 1101: 750mA 1110: 800mA 1111: 850mA
3	R/W	EOC_EN	1	IEOC enable/disable 0: Disable 1: Enable (default)
2:0	R/W	CHG_TDEG_EOC [2:0]	100	EOC deglitch time 000: 32μs 001: 64μs 010: 128μs 011: 256μs 100: 2ms (default) 101: 4ms 110: 8ms 111: 16ms

Name		Function	Addr	Reset
CHG_CTRL10		Control 10	0x0A	0x58
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:4	R/W	OTG_LBP[3:0]	0101	OTG low battery protection voltage selection (falling edge threshold, hysteresis voltage = 0.4V) 0000: 2.3V 0001: 2.4V 0010: 2.5V 0011: 2.6V 0100: 2.7V 0101: 2.8V (default) 0110: 2.9V 0111: 3.0V 1000: 3.1V 1001: 3.2V 1010: 3.3V 1011: 3.4V 1100: 3.5V 1101: 3.6V 1110: 3.7V 1111: 3.8V
3	R/W	OTG_LBP_EN	1	OTG low battery protection enable/disable 0: Disable 1: Enable (default)
2:0	R/W	OTG_OLP[2:0]	000	OTG over-load threshold (Minimum) 000: 0.5A (default) 001: 0.7A 010: 1.1A 011: 1.3A 100: 1.8A 101: 2.1A 110: 2.4A 111: Reserved Note: When OTG_OLP is set 2.1A or 2.4A, it is recommended to set the OCP to a higher level. (Addr 0x0D[2] = 1)

Name		Function	Addr	Reset
CHG_CTRL11		Control 11	0x0B	0x2C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	ADP_DIS	0	Charger adapter detection disable 0: Adapter detection is enabled (default) 1: Adapter detection is disabled
6	R/W	BATD_EN	0	Charger battery detection when charge is done 0: Battery detection is disabled (default) 1: Battery detection is enabled
5	R/W	SYSUV_HW_SEL	1	System UV protection selection bit 0: Buck switching is not turned off when system UVP is triggered 1: Buck switching is turned off when system UVP is triggered (default)
4:2	R/W	SYSREG[2:0]	011	Minimum system regulation voltage 000: 3.3V 001: 3.4V 010: 3.5V 011: 3.6V (default) 100: 3.7V 101: 3.8V 110: 3.9V 111: 4.0V
1:0	R/W	VRECHG	00	Charging recharge voltage threshold with V_{BAT_REG} 00: 100mV (default) 01: 200mV 10: 300mV 11: 400mV

Name		Function	Addr	Reset
CHG_CTRL12		Control 12	0x0C	0x02
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:5	R/W	WT_FC[2:0]	000	Fast charge timer 000: 4hrs (default) 001: 6hrs 010: 8hrs 011: 10hrs 100: 12hrs 101: 14hrs 110: 16hrs 111: 20hrs
4:3	R/W	WT_PRC[1:0]	00	Pre-charge timer 00: 30mins (default) 01: 45mins 10: 60mins 11: 60mins
2	R/W	TMR2X_EN	0	Double charger timer during MIVR, AICR, and thermal regulation 0: Disable 2x extended charger timer (default) 1: Enable 2x extended charger timer
1	R/W	TMR_EN	1	Charger timer enable/disable 0: Disable 1: Enable (default)
0	R/W	TMR_PAUSE	0	Timer control bit 0: Timer is active (default) 1: Timer is pause

Name		Function	Addr	Reset
CHG_CTRL13		Control 13	0x0D	0x52
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	WDT_EN	0	Charger and boost watch dog timer enable/disable 0: Disable (default) 1: Enable
6	R/W	WDT_TRST	1	Waiting timer to reset I^2C setup after watchdog is asserted 0: 200ms 1: 500ms (default)
5:4	R/W	WDT[1:0]	01	Watch dog timer, from WDTEN is enabled to watchdog IRQ 00: 8s 01: 40s (default) 10: 80s 11: 160s
3	R/W	AJITA	0	Charger current setting of JEITA 0: ICHG value is kept (default) 1: ICHG value becomes half
2	R/W	OCP	0	Inductor OCP current level 0: OCP (buck mode/boost mode) = 6A/5.5A (default) 1: OCP (buck mode/boost mode) = 7.5A/7A
1	R/W	UUG_ON	1	UUG enable/disable control 0: Force UUG turn off 1: Allow UUG turn on (default)
0	R/W	INT_REZ	0	The INT pin re-trigger control0: No action (default) 1: Release the INT pin, then it will re-trigger after 2ms if any event exists (this bit will auto reset to 0 when the re-trigger is done)

Name		Function	Addr	Reset
CHG CTRL 14		Charger Control 14	0x0E	0x05
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	AICL_MEAS	0	AICL measurement mechanism 0: No operation (default) 1: Execute AICL measurement
6:5	R/W	TDEG_AICL_MEAS[1:0]	00	Comparator output deglitch time 00: 2ms (default) 01: 4ms 10: 8ms 11: 16ms
4:3	R/W	AICL_MAX_MEAS_INTVL	00	Detection internal time 00: 50ms (default) 01: 100ms 10: 200ms 11: 400ms
2:0	R/W	AICL_VTH[2:0]	101	Detection comparator threshold 000: 4.1V 001: 4.2V 010: 4.3V 011: 4.4V 100: 4.5V 101: 4.6V (default) 110: 4.7V 111: 4.8V

Name		Function	Addr	Reset
CHG CTRL 15		Charger Control 15	0x0F	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	ICHG_MEAS	0	ICHG measurement mechanism 0: No operation (default) 1: Execute ICHG measurement
6:3	R	ICHG_RPT[3:0]	0000	Report the ICHG measurement result 0000: 100mA 0001: 150mA 0010: 200mA 0011: 250mA 0100: 300mA 0101: 350mA 0110: 400mA 0111: 450mA 1000: 500mA 1001: 550mA 1010: 600mA 1011: 650mA 1100: 700mA 1101: 750mA 1110: 800mA 1111: 850mA
2:0	R/W	Reversed	000	Reversed

Name		Function	Addr	Reset
CHG CTRL 16		Charger Control 16	0x10	0x10
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:5	R/W	Reserved	000	Reserved
4	R/W	JEITA_EN	1	JEITA function enable/disable 0: Disable 1: Enable (default)
3	R/W	JEITA_COOL_ISET	0	JEITA current setting in COOL region 0: Set charge current to ICHG/2 (default) 1: Set charge current to ICHG
2	R/W	JEITA_WARM_ISET	0	JEITA current setting in WARM region 0: Set charge current to ICHG/2 (default) 1: Set charge current to ICHG
1	R/W	JEITA_COOL_VSET	0	JEITA voltage setting in COOL region 0: Set charge voltage to V_{BAT_REG} – 0.2V (default) 1: Set charge voltage to V_{BAT_REG}
0	R/W	JEITA_WARM_VSET	0	JEITA voltage setting in WARM region 0: Set charge voltage to V_{BAT_REG} – 0.2V (default) 1: Set charge voltage to V_{BAT_REG}

Name		Function	Addr	Reset
CHG ADC		ADC	0x11	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:4	R/W	ADC_IN_SEL[3:0]	0000	ADC channel selection 0000: Reserved (default) 0001: VBUS/5 0010: VBUS/2 0011: VSYS 0100: VBAT 0101: Reserved 0110: TS_BAT 0111: Reserved 1000: IBUS 1001: IBAT 1010: Reserved 1011: REGN 1100: TEMP_JC 1101 to 1111: Reserved
3:1	R/W	Reversed	000	Reversed
0	R/W	ADC_START	0	ADC start control 0: ADC conversion is not active (default) 1: Start ADC conversion (auto clear when conversion is done)

Name		Function	Addr	Reset
CHG DPDM1		DPDM1	0x12	0xD0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	USBCHGEN	1	USB charger detection flow enable/disable 0: Disable USB charger detection flow 1: Enable USB charger detection flow (default)
6	R/W	Reserved	1	Reserved
5:4	R/W	DCD_TIMEOUT	01	Data contact detection timeout 00: 300ms 01: 600ms (default) 10: 900ms 11: 1200ms
3	R	Reserved	0	Reserved
2	R	DCP STD	0	Report of the standard DCP detection 0: Standard DCP is not detected (default) 1: Standard DCP is detected
1	R	CDP	0	Report of the charging downstream port detection 0: Charging downstream port is not detected (default) 1: Charging downstream port is detected
0	R	SDP	0	Report of the standard USB port detection 0: Standard USB port is not detected (default) 1: Standard USB port is detected

Name		Function	Addr	Reset
CHG DPDM2		DPDM2	0x13	0x80
Bit	**Mode**	**Name**	**Reset Value**	**Bit**
7:5	R/W	Reserved	100	Reserved
4:3	R	Reserved	00	Reserved
2:0	R	USB Status	000	USB status 000: No VBUS (default) 001: VBUS flow is under going 010: SDP (sSDPORT_CHD=1 & DCDT=0) 011: SDP NSTD (sSDPORT_CHD=1 & DCDT=1) 100: DCP (sDCPORT_CHD=1) 101: CDP (sCDPORT_CHD=1)

Name		Function	Addr	Reset
CHG DPDM3		DPDM3	0x14	0x20
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:2	R/W	Reserved	0	Reserved
1	R	DCDT_STATUS	0	Data contact timeout status 0: Data contact timeout is not expired 1: Date contact timeout is expired
0	R	CHGDET_STATUS	0	BC detection output 0: Charger port (DCP and CDP) is not detected 1: Charger port (DCP and CDP) is detected

Name		Function	Addr	Reset
CHG_CTRL19		Charger Control 19	0x18	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	PPOFF_RST_DIS	0	System reset function disable bit 0: System reset is enabled (default) 1: System reset is disabled
6:0	R/W	Reserved	0000000	Reserved

Name		Function	Addr	Reset
CHG_CTRL17		Charger Control 17	0x19	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	EN_PUMPX	0	Enable MTK pump express pulse 0: Disable (default) 1: Allow MTK pump express pulse
6	R/W	PUMPX_2.0_1.0	0	MTK pump express 2.0/1.0 enable 0: PE1.0 Enable (default) 1: PE 2.0 Enable
5	R/W	PUMPX_UP_DN	0	MTK pump express 1.0 voltage up/down enable 0: PE 1.0 voltage down enable (default) 1: PE 1.0 voltage up enable
4:0	R/W	PUMPX_DEC	00000	MTK pump express 2.0 voltage request setting 00000: 5.5V (default) 00001: 6V 00010: 6.5V … 00111: 9V … 01101: 12V 01110: 12.5V 01111: 13V 10000: 13.5V 10001: 14V 10010: 14.5V 10011: Reserved … 11101: Reserved 11110: Adapter healthy self-testing 11111: Disable cable drop compensation

Name		Function	Addr	Reset
CHG_CTRL18		Charger Control 18	0x1A	0x40
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:6	R/W	Reserved	01	Reserved
5:3	R/W	BAT_COMP	000	Battery IR compensation resistor setting 000: 0mΩ (default) 001: 25mΩ 010: 50mΩ 011: 75mΩ 100: 100mΩ 101: 125mΩ 110: 150mΩ 111: 175mΩ
2:0	R/W	VCLAMP	000	Battery IR compensation maximum voltage clamp 000: 0mV (default) 001: 32mV 010: 64mV 011: 96mV 100: 128mV 101: 160mV 110: 192mV 111: 224mV

Name		Function	Addr	Reset
DEVICE_ID		DEVICE_ID	0x40	0x95
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:4	R	VENDOR[3:0]	1001	Vendor IC
3:0	R	CHIP_REV[3:0]	0101	Chip version: 0001 = A, 0010 = B, 0011 = C, etc.

Name		Function	Addr	Reset
CHG_STAT		CHG STAT	0x42	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:6	R	CHG_STAT	00	Charger status bit 00: Ready 01: Charge in progress 10: Charge is done 11: Fault
5	R	VBAT_LVL	0	Battery voltage level for operation mode 0: Charger operates in pre-charge 1: Charger operates in fast- charge level
4	R	VBAT_TRICKLE	0	Battery voltage level for operation mode 0: Charger does not operate in trickle level 1: Charger operates in trickle level
3	R	BOOST_STAT	0	Boost mode status 0: Not in boost mode 1: In boost mode
2	R	BST_VBUSOV_STAT	0	Boost mode VBUS overvoltage protection (VBUS OVP) status 0: Boost VBUS OVP is not triggered 1: Boost VBUS OVP is triggered
1	R	Reserved	0	Reserved
0	R	ADC_STAT	0	ADC status 0: ADC is idle 1: ADC is under conversion

Name		Function	Addr	Reset
CHG_NTC		CHG NTC	0x43	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	Reserved	0	Reserved
6:4	R	BAT_NTC_FAULT[2:0]	000	BAT NTC fault status 000: Normal 010: Warm 011: Cool 101: Cold 110: Hot
3:0	R	Reserved	0000	Reserved

Name		Function	Addr	Reset
ADC_DATA_H		ADC DATA H	0x44	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:0	R	ADC_CODEH[7:0]	00000000	ADC code high byte

Name		Function	Addr	Reset
ADC_DATA_L		ADC DATA L	0x45	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7:0	R	ADC_CODEL[7:0]	00000000	ADC code low byte

Name		Function	Addr	Reset
CHG_STATC		CHG STATC	0x50	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	PWR_RDY	0	Power ready status bit 0: Input power is bad, VBUS > VOVP or VBUS < VUVLO or VBUS < BAT + VSLP 1: Input power is good, UVLO < VBUS < VOVP & VBUS > BAT + VSLP
6	R	CHG_MIVR	0	Charger warning. Input voltage MIVR loop status. 0: MIVR loop is not active 1: MIVR loop is active
5	R	CHG_AICR	0	Charger warning. Input current AICR loop status. 0: AICR loop is not active 1: AICR loop is active
4	R	CHG_TREG	0	Charger warning. Thermal regulation loop status. 0: Thermal regulation loop is not active 1: Thermal regulation loop is active
3:0	R	Reserved	0000	Reserved

Name		Function	Addr	Reset
CHG_FAULT		CHG FAULT	0x51	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	CHG_VBUSOV	0	VBUS overvoltage protection. Set when VBUS > VBUS_OVP is detected. 0: VBUS is not in OVP 1: VBUS is in OVP
6	R	CHG_VBATOV	0	Charger fault. Battery OVP. 0: Battery is not in OVP 1: Battery is in OVP
5	R	CHG_VSYSOV	0	Charger fault. System OVP. 0: System is not in OVP 1: System is in OVP
4	R	CHG_VSYSUV	0	Charger fault. System UVP. 0: System is not in UVP 1: System is in UVP
3:0	R	Reserved	0000	Reserved

Name		Function	Addr	Reset
TS_STATC		TS STATC	0x52	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	TS_BAT_HOT	0	BAT temperature status read bit 0: Normal temperature 1: Temperature is hot
6	R	TS_BAT_WARM	0	BAT temperature status read bit 0: Normal temperature 1: Temperature is warm
5	R	TS_BAT_COOL	0	BAT temperature status read bit 0: Normal temperature 1: Temperature is cool
4	R	TS_BAT_COLD	0	BAT temperature status read bit 0: Normal temperature 1: Temperature is cold
3:0	R	Reserved	0000	Reserved

Name		Function	Addr	Reset
CHG_IRQ1		CHG IRQ 1	0x53	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/C	OTPI	0	Thermal shutdown fault 0: No event occurs 1: Event occurs
6	R/C	CHG_RVPI	0	Charger reverse protection fault 0: No event occurs 1: Event occurs
5	R/C	CHG_ADPBADI	0	Charger bad adapter fault 0: No event occurs 1: Event occurs
4	R/C	CHG_BATABSI	0	Battery absence fault 0: No event occurs 1: Event occurs
3	R/C	CHG_TMRI	0	Charger timer time-out fault 0: No event occurs 1: Event occurs
2	R/C	CHG_STATCI	0	Status of each CHG_STATC register (Reg0x50) is changed 0: No event occurs 1: Event occurs
1	R/C	CHG_FAULTI	0	Status of each CHG_FAULT register (Reg0x51) is changed 0: No event occurs 1: Event occurs
0	R/C	TS_STATCI	0	Status of each TS_STATC register (Reg0x52) is changed 0: No event occurs 1: Event occurs

Name		Function	Addr	Reset
CHG_IRQ2		CHG IRQ 2	0x54	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/C	CHG_IEOCI	0	Charging current is lower than EOC current ever occurs 0: No event occurs 1: Event occurs
6	R/C	CHG_TERMI	0	Charge terminated event 0: No event occurs 1: Event occurs
5	R/C	CHG_RECHGI	0	Re-Charge behavior ever occurs. 0: No event occurs 1: Event occurs
4	R/C	SSFINISHI	0	Charger or boost–mode soft-start finishes event 0: No event occurs 1: Event occurs
3	R/C	WDTMRI	0	Watch dog timer timeout fault 0: No event occurs 1: Event occurs
2	R/C	Reserved	0	Reserved
1	R/C	CHG_ICHGMeasI	0	ICHG measurement function is done event 0: No event occurs 1: Event occurs
0	R/C	CHG_AICLMeasI	0	AICL measurement function is done event 0: No event occurs 1: Event occurs

Name		Function	Addr	Reset
CHG_IRQ3		CHG IRQ 3	0x55	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/C	BST_OLPI	0	Boost over-load protection event 0: No event occurs 1: Event occurs
6	R/C	BST_MIDOVI	0	Boost VMID OVP fault event 0: No event occurs 1: Event occurs
5	R/C	BST_BATUVI	0	Boost low voltage input fault event 0: No event occurs 1: Event occurs
4:2	R/W	Reserved	000	Reserved
1	R/C	PUMPX_DONEI	0	MTK pump express function done event 0: No event occurs 1: Event occurs
0	R/C	ADC_DONEI	0	ADC measurement done event 0: No event occurs 1: Event occurs

Name		Function	Addr	Reset
DPDM_IRQ		DPDM IRQ	0x56	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/C	DCDTI	0	Data contact detection event 0: Data contact detection timeout is not detected 1: Data contact detection timeout is detected when DCDT goes from 0 to 1
6	R/C	CHGDETI	0	Output of USB charger detection. The bit will be set to 1 if COMN > VDAT_REF & COMN < VLGC 0: COMN < VDAT_REF or COMN > VLGC (charger port is not detected) 1: COMN > VDAT_REF & COMN < VLGC (charger port is detected) when CHGDET goes from 0 to 1
5:2	R/C	Reserved	000	Reserved
1	R/C	Detach_I	0	VBUS detached, when VBUSPG_D goes from 1 to 0 0: No event occurs 1: Event occurs
0	R/C	Attach_I	0	VBUS attached, when DCP STD (Reg0x12[2]) goes from 0 to 1 or when CDP (Reg0x12[1]) goes from 0 to 1 or when SDP (Reg0x12[0]) goes from 0 to 1 0: No event occurs 1: Event occurs

Name		Function	Addr	Reset
CHG_STATC_CTRL		CHG STATC CTRL	0x60	0xF0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	PWR_RDYM	1	Power ready interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	CHG_MIVRM	1	Input voltage MIVR loop active interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	CHG_AICRM	1	Input current AICR loop active interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4	R/W	CHG_TREGM	1	Thermal regulation loop active interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
3:0	R/W	Reserved	0000	Reserved

Name		Function	Addr	Reset
CHG_FAULT_CTRL		CHG FAULT CTRL	0x61	0xF0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	CHG_VBUSOVM	1	VBUS overvoltage protection interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	CHG_VBATOVM	1	Battery OVP interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	CHG_VSYSOVM	1	System OVP interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4	R/W	CHG_VSYSUVM	1	System UVP interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
3:0	R/W	Reserved	0000	Reserved

Name		Function	Addr	Reset
TS_STATC_CTRL		TS STATC CTRL	0x62	0xFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	TS_BAT_HOTM	1	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	TS_BAT_WARMM	1	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	TS_BAT_COOLM	1	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4	R/W	TS_BAT_COLDM	1	BAT temperature status interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
3:0	R/W	Reserved	1111	Reserved

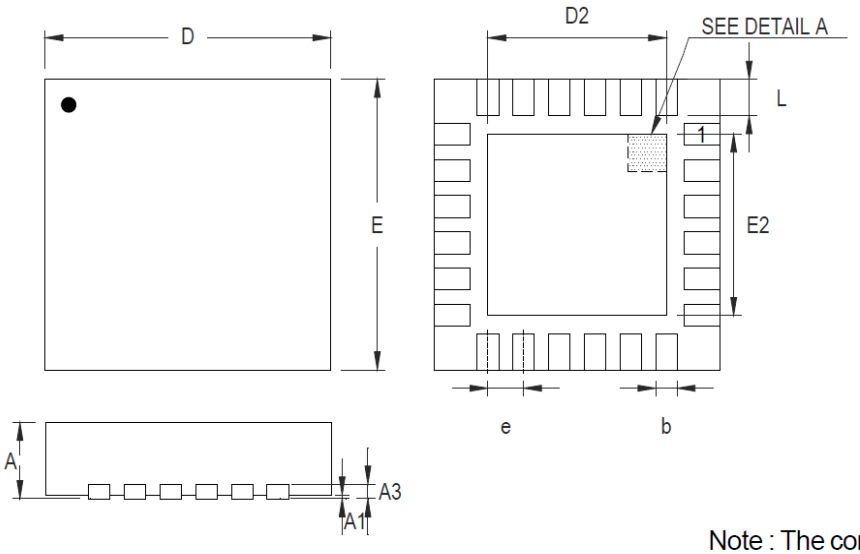
Name		Function	Addr	Reset
CHG_IRQ1_CTRL		CHG IRQ 1 CTRL	0x63	xFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	OTPM	1	Thermal shutdown fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	CHG_RVPM	1	Charger reverse protection fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	CHG_ADPBADM	1	Charger bad adapter fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4	R/W	CHG_BATABSM	1	Battery absence fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
3	R/W	CHG_TMRM	1	Charger timer time-out fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
2	R/W	CHG_STATCM	1	Status of each CHG_STATC register (Reg0x50) changed interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
1	R/W	CHG_FAULTM	1	Status of each CHG_FAULT register (Reg0x51) changed interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0	R/W	TS_STATCM	1	Status of each TS_STATC register (Reg0x52) changed interrupt mask 0: Interrupt is not masked 1: Interrupt is masked

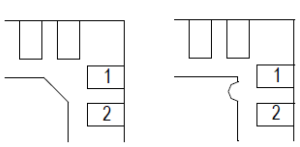
Name		Function	Addr	Reset
CHG_IRQ2_CTRL		CHG IRQ 2 CTRL	0x64	0xFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	CHG_IEOCM	1	Charging current is lower than EOC current interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	CHG_TERMM	1	Charge terminated event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	CHG_RECHGM	1	Re-Charge behavior interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4	R/W	SSFINISHM	1	Charger or boost-mode soft-start finishes event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
3	R/W	WDTMRM	1	Watch dog timer timeout fault interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
2	R/C	Reserved	0	Reserved
1	R/W	CHG_ICHGMeasM	1	ICHG measurement function done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0	R/W	CHG_AICLMeasM	1	AICL measurement function done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked

Name		Function	Addr	Reset
CHG_IRQ3_CTRL		CHG IRQ 3 CTRL	0x65	0xFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	BST_OLPM	1	Boost overload protection event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	BST_MIDOVM	1	Boost VMID OVP fault event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	BST_BATUVM	1	Boost low voltage input fault event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4:2	R/W	Reserved	111	Reserved
1	R/W	PUMPX_DONEM	1	MTK pump express function done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0	R/W	ADC_DONEM	1	ADC measurement done event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked

Name		Function	Addr	Reset
DPDM_IRQ_CTRL		DPDM IRQ CTRL	0x66	0xFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	DCDTM	1	Data contact detection event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
6	R/W	CHGDETM	1	Output of USB charger detection interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
5	R/W	HVDCP DETM	1	HVDCP detection event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
4:2	R/W	Reserved	111	Reserved
1	R/W	Detach_M	1	VBUS detach event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked
0	R/W	Attach_M	1	VBUS attach event interrupt mask 0: Interrupt is not masked 1: Interrupt is masked

17 Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

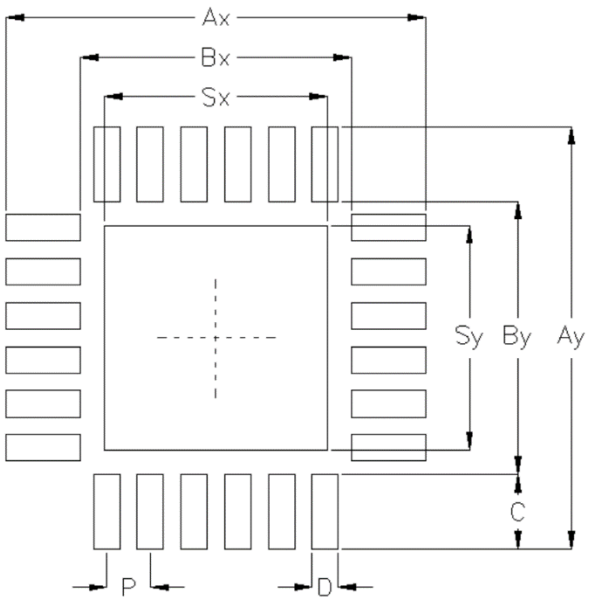
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

Note 8. The package of the RT0467 uses Option 2.

18 Footprint Information

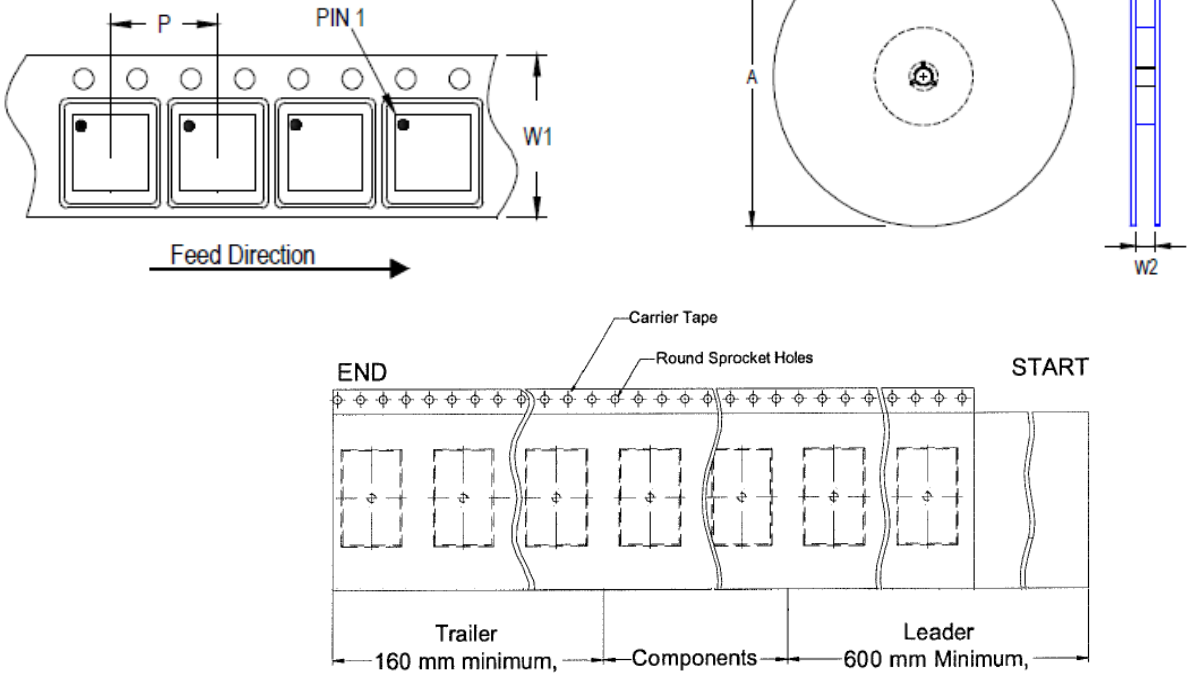


Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24	Option1	24	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.55	2.55	±0.05
	Option2									2.60	2.60	

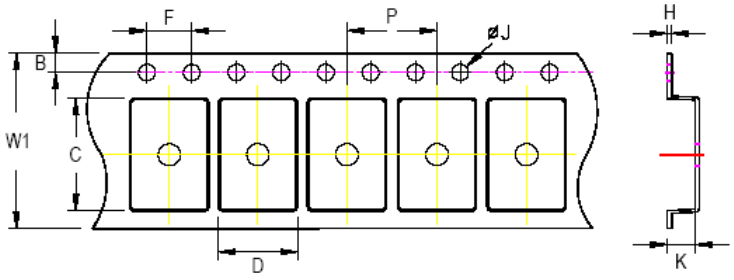
Note 9. The package of the RT0467 uses Option 2.

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

20 Datasheet Revision History

Version	Date	Description	Item
02	2025/1/2	Modify	*Changed the names of pin 19 and pin 20 to SW.* *General Description on page 1* - Added Temperature range *Ordering Information on page 2* - Added note Absolute Maximum Ratings on page 6 - Updated description *Electrical Characteristics on page 8 to 14* - Updated description and symbol *Application Information on page 29* - Added declaration *Footprint Information on page 57* - Added information *Packing Information on page 58, 59, 60* - Added information