RICHTEK®

RT9427

5μA System-Side Single Cell Fuel Gauge

1 General Description

The RT9427 Li-Ion/Li-Polymer battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell battery packs. The RT9427 resides within the system's main board and manages a non-removable battery or removable battery pack.

The RT9427 reports *StateOfCharge*, *StateOfHealth*, *FullChargeCapacity*, *TimeToEmpty* and *CycleCount* based on the Voltaic Gauge with Current Sensing (VGCS) algorithm by using the voltage difference between battery voltage and OCV to calculate the increasing or decreasing SOC, with current sensing compensation to report battery SOC.

The Voltaic Gauge with Current Sensing algorithm can support smoothly SOC tracking and does not accumulate error over time and with current changes. That is an advantage compared to coulomb counter which suffer from SOC drift caused by current sense error and battery self-discharge.

The RT9427 provides a complete battery status monitor with an interrupt alarm function. It can actively alert the host processor when conditions of battery overvoltage, undervoltage, or over-temperature conditions during charging or discharging. This is especially useful for high C-rate battery charging applications, as it can measure battery voltage using a Kelvin sense connection to eliminate the IR drop effect for an optimal charging profile and safety. Additional useful alarm functions include under SOC alert, SOC Change and battery presence status change.

The RT9427 is available in WDFN-10L 2x2.5 (FC) and WL-CSP-9B 1.68x1.81 (BSC) packages. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Features

- **Support System-Side Fuel Gauging**
- **Battery Fuel Gauge for 1-Series (1sXp) Li-Ion/Li-Polymer Applications**
- **State of Charge (SOC) Calculated by VoltaicGauge with Current Sensing (VGCS)**
- **No Accumulation Error on Capacity Calculation**
- **Battery SOC, SOH, FCC, TTE, and Cycle Count Report**
- **Ultra-Low Power Consumption: 5μA**
- **Voltage Measurement: ±5mV**
- **Current Measurement: ±0.5%**
- **Battery Temperature Measurement: ±1°C (T_A = 0°C to 45°C)**
- **Battery Monitoring with Alert Indicators for Voltage, Current, Temperature, SOC and Presence**
- **High C-Rate Battery Charging Compliance**
- **Voltage Kelvin-Sense Connection for WDFN Package**
- **Low-Value Sense Resistor (0.5mΩ to 40mΩ, Typical 10mΩ)**
- **9-Bump WL-CSP Package with 0.5mm Pitch**
- **10 Pin WDFN Package with 0.4mm Pitch**
- **I^2C Controlled Interface with 1.2V and 1.8V IO Compatible**

3 Applications

- Smartphones
- Tablet PCs
- Wearable Devices
- Digital Still Cameras
- Digital Video Cameras
- Handheld and Portable Applications

4 Ordering Information

RT9427 □□

Package Type(1)
WSC: WL-CSP-9B 1.68x1.81 (BSC)
QWF: WDFN-10L 2x2.5 (FC) (W-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)
(For WDFN-10L 2x2.5 (FC) Only)

Note 1.

- Marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicates that Richtek products are Richtek Green Policy compliant.

5 Marking Information

RT9427WSC

2HXXYY
CCC-RRR
YMDAN

2H: Product Code
XXYY: Wafer ID with Check Sum
CCC-RRR: IC Coordinate (X, Y)
YMDAN: Date Code

RT9427GQWF

00W

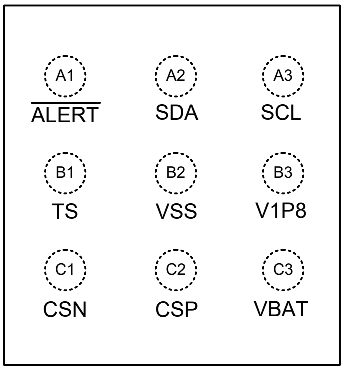
00: Product Code
W: Date Code

Table of Contents

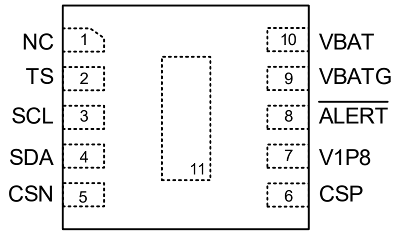
1 **General Description** 1
2 **Features** 1
3 **Applications** 1
4 **Ordering Information** 2
5 **Marking Information** 2
6 **Pin Configuration** 4
7 **Functional Pin Description** 4
8 **Functional Block Diagram** 5
9 **Absolute Maximum Ratings** 6
10 **Recommended Operating Conditions** 6
11 **Electrical Characteristics** 7
11.1 Electrical Characteristics: I^2C Interface 8
12 **Typical Application Circuit** 10
12.1 For WL-CSP-9B 1.68x1.81 (BSC) 10
12.2 For WDFN-10L 2x2.5 (FC) 10
13 **Typical Operating Characteristics** 12
14 **Application Information** 14
14.1 ADC for Voltage, Current and Temperature 14
14.2 VoltaicGauge with Current Sensing (VGCS) Algorithm 14
14.3 Design Capacity 15
14.4 SOC Report 15
14.5 Power Mode 15
14.6 Active Mode 15
14.7 Sleep Mode 15
14.8 Shutdown Mode 15
14.9 Power Mode Switching 16
14.10 Controller 16
14.11 Power Up Sequence 16
14.12 Quick Sensing 16
14.13 Alert Function 16
14.14 I^2C Interface 19
14.15 I^2C Waveform Information 19
14.16 Shutdown and Wake-Up Timing 20
14.17 Register Summary Table 20
14.18 Thermal Considerations 21
14.19 Layout Considerations 22
15 **Outline Dimension** 26
15.1 WL-CSP-9B 1.68x1.81 (BSC) Package 26
15.2 WDFN-10L 2x2.5 (FC) Package 27
16 **Footprint Information** 28
16.1 WL-CSP-9B 1.68x1.81 (BSC) Package 28
16.2 WDFN-10L 2x2.5 (FC) Package 29
17 **Packing Information** 30
17.1 Tape and Reel Data 30
17.2 Tape and Reel Packing 32
17.3 Packing Material Anti-ESD Property 34
18 **Datasheet Revision History** 35

6 Pin Configuration

(TOP VIEW)



WL-CSP-9B 1.68x1.81 (BSC)

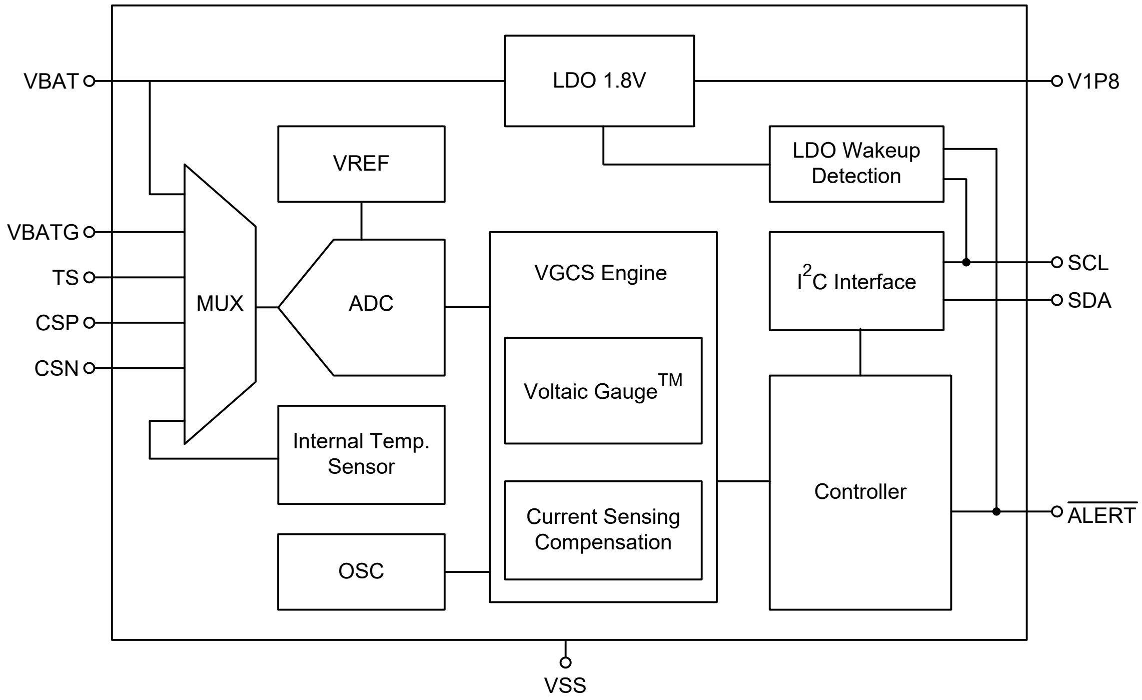


WDFN-10L 2x2.5 (FC)

7 Functional Pin Description

Pin No.		Pin Name	Pin Function
WL-CSP-9B 1.68x1.81 (BSC)	WDFN-10L 2x2.5 (FC)		
A1	8	$\overline{\text{ALERT}}$	Alert open-drain indicator output.
A2	4	SDA	Serial data input. Slave I^2C serial communications data line for communication with system. Open-drain I/O.
A3	3	SCL	Serial cock input. Slave I^2C serial communications clock line for communication with system. Open-drain I/O.
B1	2	TS	Temperature measurement input.
B2	--	VSS	Device ground.
B3	7	V1P8	1.8V LDO output. Connect a 2.2μF ceramic capacitor to VSS. It cannot provide power for other device in the system.
C1	5	CSN	Battery current sensing negative input. Connect a 10mΩ sense resistor with Kelvin sense connection.
C2	6	CSP	Battery current sensing positive input. Connect a 10mΩ sense resistor with Kelvin sense connection.
C3	10	VBAT	Power supply input and battery voltage sensing input.
--	1	NC	No internal connection. Keep it floating.
--	9	VBATG	Battery voltage sensing negative input. Connect to battery connector with Kelvin sense connection.
--	11	EP	Exposed Pad. Connect to CSP.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- Voltage on CSN Pin to CSP ---------- –0.3V to 2V
- Voltage on V1P8 pin Relative to VSS ---------- –0.3V to 2V
- Voltage on VBAT Pin Relative to VSS---------- –0.3V to 6V
- Voltage on All Other Pins Relative to VSS ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 2x2.5 (FC) ---------- 0.88W
  WL-CSP-9B 1.68x1.81 (BSC) ---------- 1.81W
- Package Thermal Resistance (Note 3)
  WDFN-10L 2x2.5 (FC), θ_{JA} ---------- 112.6°C/W
  WDFN-10L 2x2.5 (FC), θ_{JC} ---------- 0.8°C/W
  WL-CSP-9B 1.68x1.81 (BSC), θ_{JA} ---------- 55°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model)---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 5)

- Supply Voltage, VBAT ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

(2.5V ≤ V_{BAT} ≤ 5.5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage		VBAT - VSS	2.5	--	5.5	V
Active Current	I_{ACTIVE}	VBAT = 3.8V, battery present & ExTemp disabled	--	12	20	μA
Sleep Current	I_{SLEEP}	VBAT = 3.8V, battery present & ExTemp disabled, period is 4 times of active mode	--	5	12	μA
Shutdown Current	I_{SHDN}	VBAT = 3.8V, LDO off	--	1	1.5	μA
1.8V LDO	V_{1P8}		--	1.85	--	V
Voltage Measurement Range			2.5	--	VBAT	V
Voltage Measurement Error	V_{ERR}	VBAT = 4V	–5	--	5	mV
Current Measurement Range		V_{CSP} - V_{CSN}	–100	--	100	mV
Current Measurement Gain Error	I_{GERR}	|V_{CSP} - V_{CSN}| = 80mV	–0.5	--	0.5	%
Current Measurement Offset Error	I_{OERR}	|V_{CSP} - V_{CSN}| = 0V (Note 6)	–5	±2.5	5	μV
Temperature Measurement Error	ExT_{GERR}	T_A = 0°C to 45°C (Note 7)	–1	--	1	°C
		T_A = –40°C to 85°C (Note 7)	–3	--	3	°C
Internal Temperature Measurement Range		(Note 8)	–40	--	85	°C
Internal Temperature Measurement Error	$IntT_{GERR}$	T_A = 25°C	--	±3	--	°C
Battery Presence Detection Threshold			0.93 x VBAT	0.95 x VBAT	0.97 x VBAT	V
Battery Presence Detection Pull High Resistor			--	150	--	kΩ
Battery Insertion Detection Time		Battery detection delay time Programmable	20	--	145	ms
Battery Removal Detection Time			--	--	1.1	sec
Input Logic-High: SCL, SDA, $\overline{ALERT}$	V_{IH}	Reference to VSS	0.78	--	--	V
Input Logic-Low: SCL, SDA, $\overline{ALERT}$	V_{IL}	Reference to VSS	--	--	0.5	V
Output Logic-Low: SDA, $\overline{ALERT}$	V_{OL}	I_{OL} = 3mA, reference to VSS	--	--	0.3	V
Pull Down Current: SCL, SDA, $\overline{ALERT}$	I_{PDN}		0.05	0.2	0.4	μA
SHUTDOWN Low Detection Time: SCL, $\overline{ALERT}$	t_{SLDT}		20	--	--	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SHUTDOWN Entry Time	t_{SHDN}	Delay time from SHUTDOWN command to V1P8 turned off, programmable	1	--	256	sec
I²C ACK Delay Time	t_{ACK}	I²C ACK, register information not ready.	--	--	10	ms
Initialization Ready Time	t_{RDY}	Delay time from rising edge of VBAT to the active state.	--	--	250	ms
I²C Time Out		Programmable	0.5	--	2.25	sec

Note 6. Typical result is a long-term average.

Note 7. The thermistor utilizes a 10k NTC with a beta value of 3435k. The default model is SEMITEC 103KT1608T.

Note 8. Specifications are 100% tested at T_A = 25°C. Limits over the operating range are guaranteed by design and characterization.

11.1 Electrical Characteristics: I²C Interface

(2.5V ≤ VBAT ≤ 5.5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Operating Frequency	f_{SCL}	(Note 9)	10	--	400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	μs
Hold Time After START Condition	$t_{HD;STA}$	(Note 9)	0.6	--	--	μs
Low Period of the SCL Clock	t_{LOW}		1.3	--	--	μs
High Period of the SCL Clock	t_{HIGH}		0.6	--	--	μs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time	$t_{HD;DAT}$	(Note 10 and Note 11)	0	--	0.9	μs
Data Setup Time	$t_{SU;DAT}$	(Note 10)	100	--	--	ns
Data Valid Time	$t_{VD;DAT}$	(Note 12 and Note 13)	--	--	0.9	μs
Data Valid Acknowledge Time	$t_{VD;ACK}$	(Note 12 and Note 14)	--	--	0.9	μs
Clock Data Rise Time	t_R		20	--	300	ns
Clock Data Fall Time	t_F		20	--	300	ns
Set-up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	μs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 15)	0	--	50	ns
Capacitive Load for Each Bus Line	C_B	(Note 16)	--	--	400	pF
SCL, SDA Input Capacitance	C_{BIN}		--	--	5	pF

Note 9. f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 10. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 11. This device internally provides a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN}) of the SCL signal to bridge the undefined region of the falling edge of SCL.

Note 12. The maximum $t_{VD;DAT}$ can be 0.9ms for Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

Note 13. $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

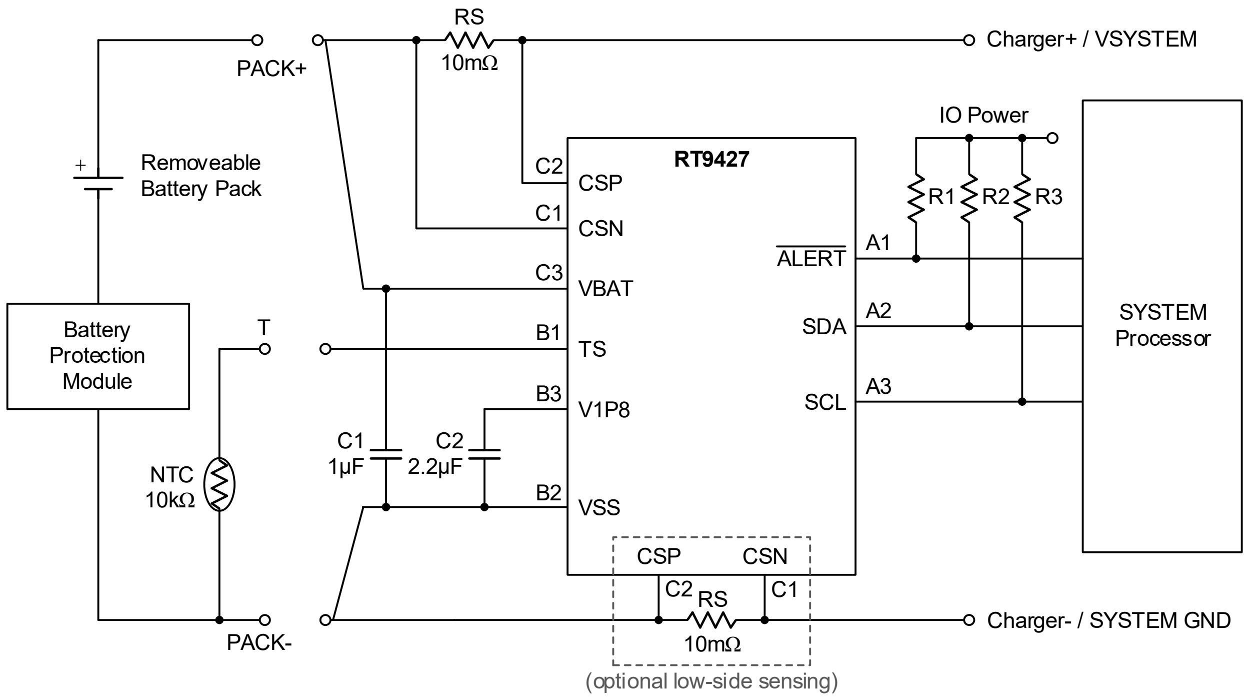
Note 14. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

Note 15. Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 16. C_B – total capacitance of one bus line in pF.

12 Typical Application Circuit

12.1 For WL-CSP-9B 1.68x1.81 (BSC)



12.2 For WDFN-10L 2x2.5 (FC)

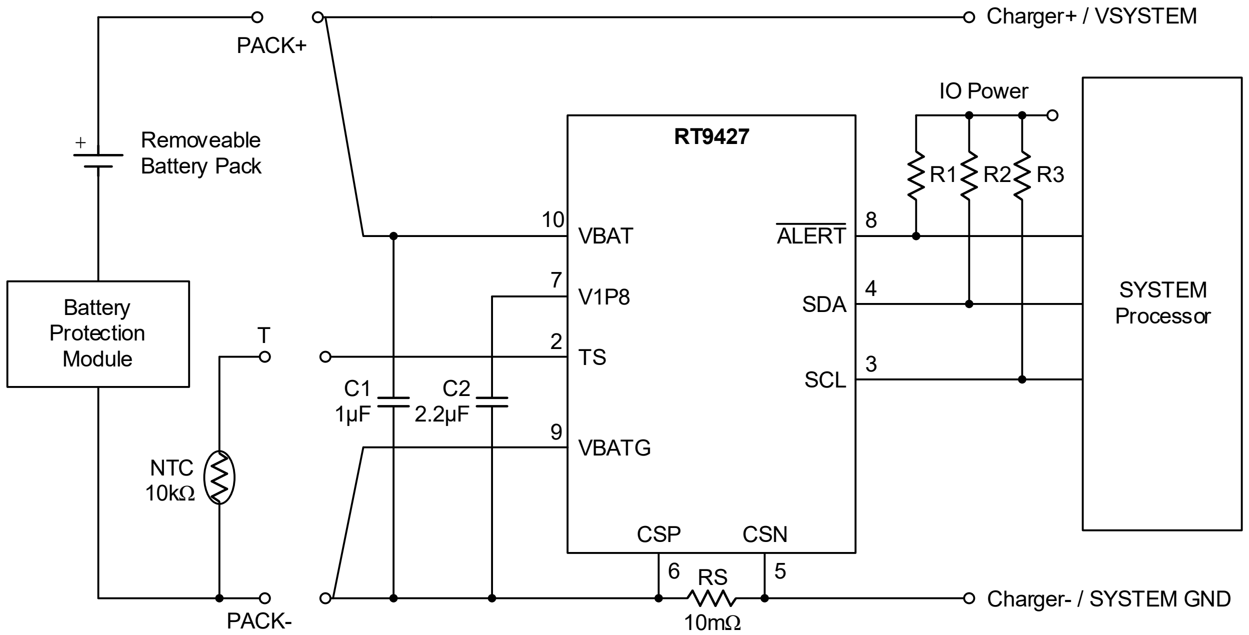


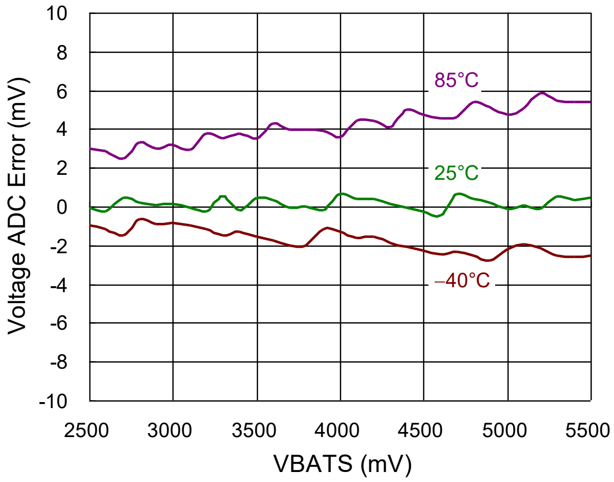
Table 1. BOM List

Name	Part Number	Description	Package	Manufacturer
C1	GRM155R61A105KE01	CAP, CERM, 1μF, 10V, ±10%, X5R	0402	Murata
C2	GRM155R60J225KE01	CAP, CERM, 2.2μF, 6.3V, ±10%, X5R	0402	Murata
R1, R2, R3	WR06X3301FTL	3.3k, 1%, 0.1W	0603	WALSIN
RS	RLM-1220-6F-R010-FNH	10mΩ, 1%, 1W	0805	CYNTEC
NTC	103KT1608-1P	10kΩ, 1%, B = 3435K	0603	SEMITEC

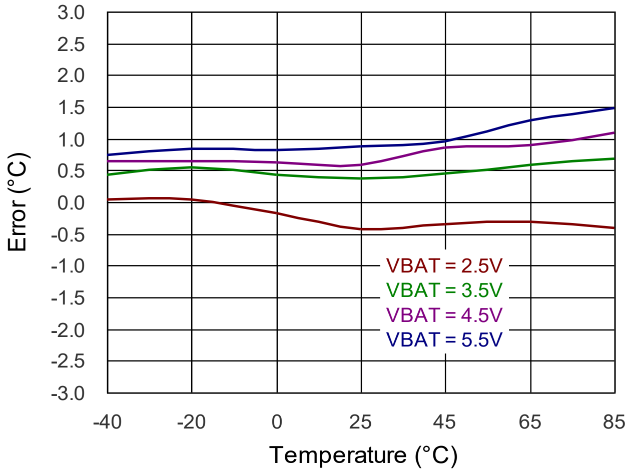
13 Typical Operating Characteristics

*: SOC accuracy tested by IC with custom parameter.

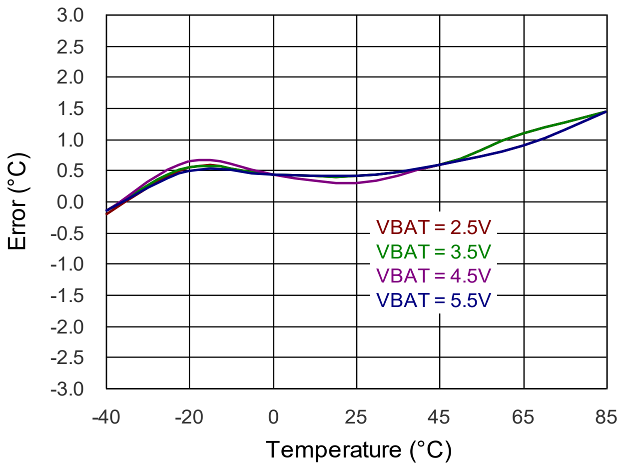
Voltage ADC Error vs. Temperature



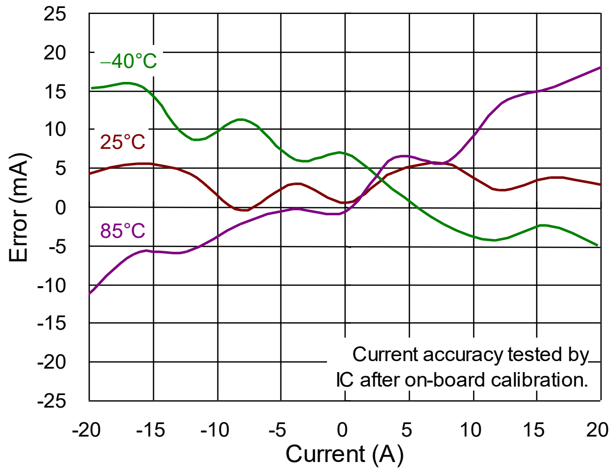
Internal Temperature Measurement Error



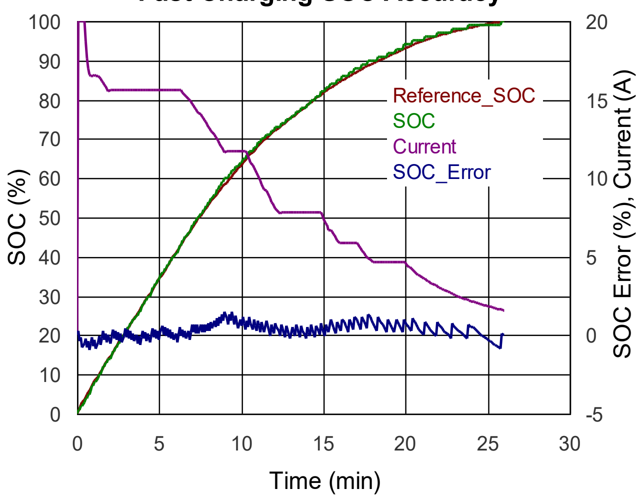
External Temperature Measurement Error



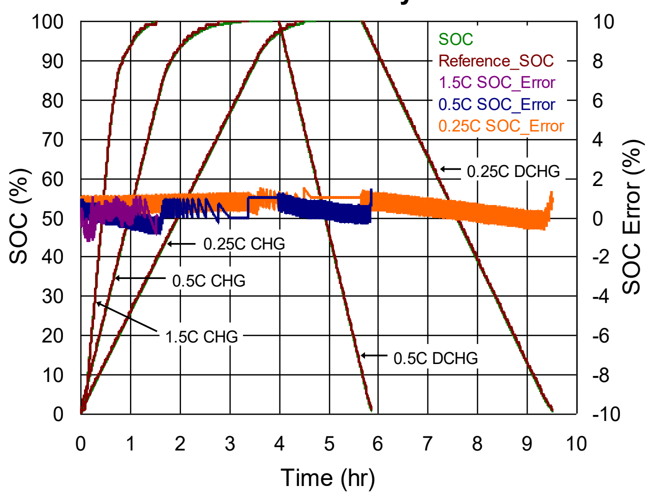
Current ADC Error with 0.5mΩ Rsense vs. Temperature

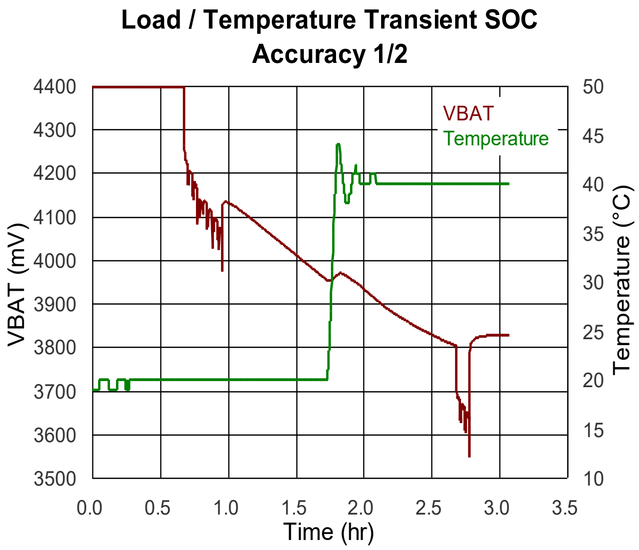


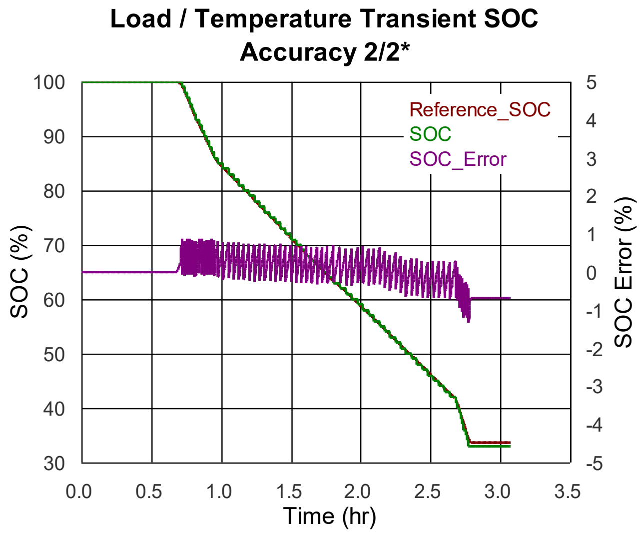
Fast Charging SOC Accuracy*

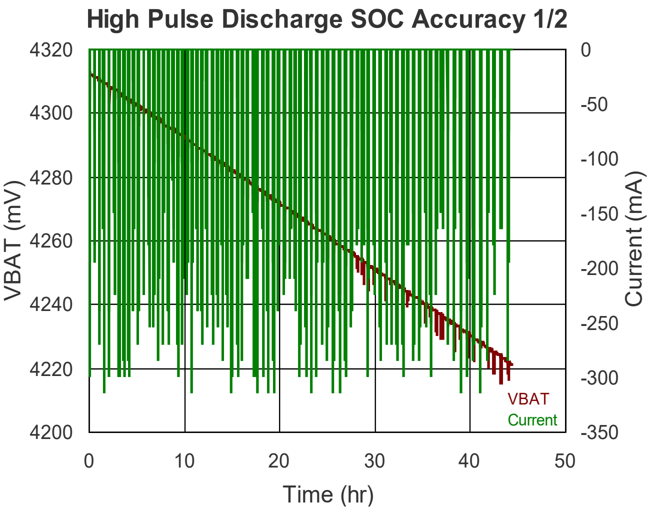


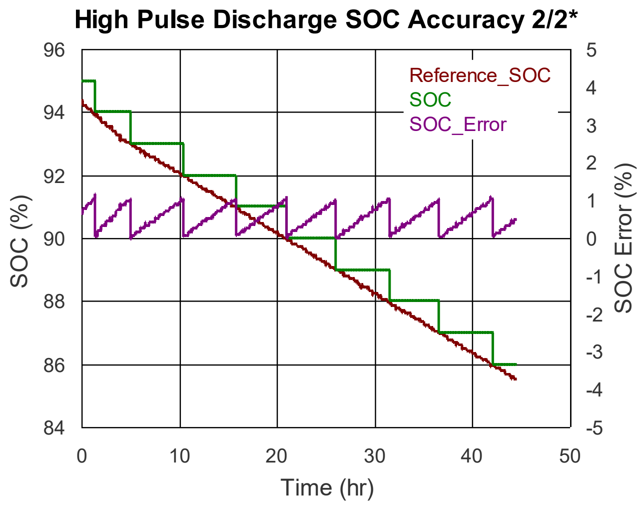
SOC Accuracy*




Load / Temperature Transient SOC Accuracy 1/2
VBAT
Temperature
VBAT (mV)
Temperature (°C)
Time (hr)


Load / Temperature Transient SOC Accuracy 2/2*
Reference_SOC
SOC
SOC_Error
SOC (%)
SOC Error (%)
Time (hr)


High Pulse Discharge SOC Accuracy 1/2
VBAT
Current
VBAT (mV)
Current (mA)
Time (hr)


High Pulse Discharge SOC Accuracy 2/2*
Reference_SOC
SOC
SOC_Error
SOC (%)
SOC Error (%)
Time (hr)

14 Application Information

(Note 17)

14.1 ADC for Voltage, Current, and Temperature

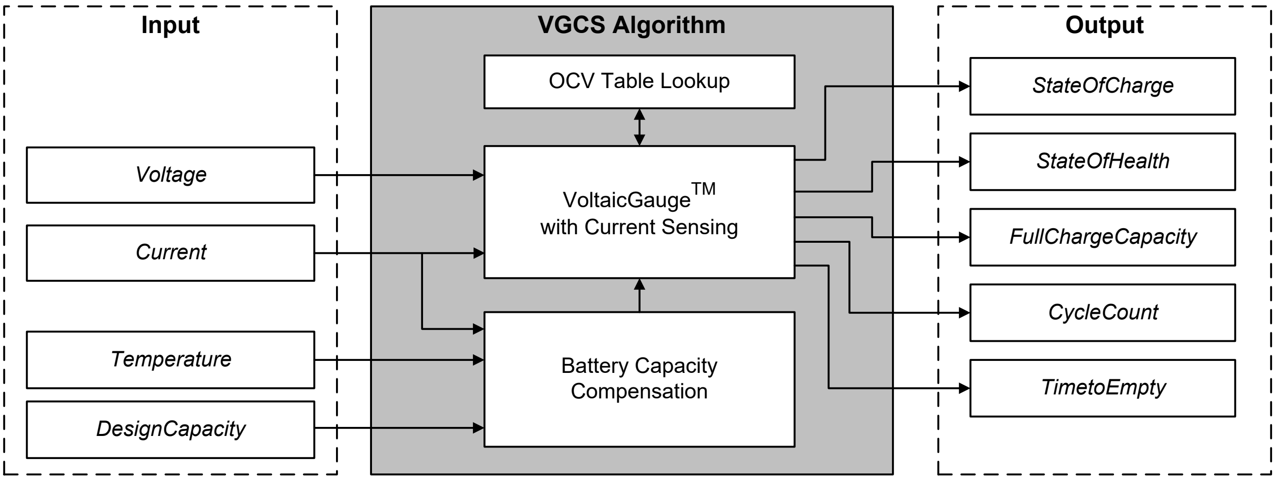
Battery voltage is measured at the VBAT pin input with respect to VBATG over a 2.5 to 5.5V range with a resolution of 1mV. The ADC calculates the first cell voltage for a period of 250ms after IC power on and then for a period of 1s for every cycle afterwards. The Voltage register requires 1s to update after exiting Sleep mode. The result is placed in the *Voltage* register at the end of each conversion period.

The RT9427 Fuel Gauge measures the battery current during charging and discharging and reports the values to the *Current* register. The measurement range is 10A (when RS = 10mΩ), and the resolution is 1mA.

The RT9427 reports the temperature to the *Temperature* register by measuring either the battery temperature or the chip temperature. When measuring the battery temperature, an external NTC resistor is used.

14.2 VoltaicGauge with Current Sensing (VGCS) Algorithm

The VGCS algorithm is based on the battery voltage and the dynamic difference between the battery voltage and battery current measurements. It iterates battery voltage information and compensates with current information to increase or decrease the delta SOC, which is then integrated into the SOC. The following figure illustrates the VGCS functional block.



The RT9427 obtains battery voltage information, and then uses an OCV table along with iterate calculations that include current correction to calculate delta SOC. It references the design capacity and actual battery capacity as references to optimize the result and outputs the final SOC.

The coulomb counter-based fuel gauges are subject to SOC drift, which can be attributed to errors in current sensing and the natural self-discharge of cells. Over time, even minimal errors in current sensing can result in significant drift due to cumulative errors. The VGCS system employs a voltage-based iterative algorithm that ensures consistent SOC readings.

It incorporates current data primarily to enhance the accuracy of transient responses. As a result, VGCS avoids the issue of error accumulation and the resultant SOC drift commonly associated with traditional coulomb counters.

Additionally, VGCS also supports high C-rate charging technology, battery capacity aging compensation through full charge, full discharge, and relaxation conditions, and Battery Aging Profile Adjust (BAPA) command.

14.3 Design Capacity

The *DesignCapacity* register should be set to the correct value after the IC's Power-On Reset (POR). The Design Capacity represents the cell's expected capacity at the time of manufacture and should remain unchanged while the VGCS is active. It serves as a reference input for the VGCS algorithm. The resolution of the design capacity is 1mAh, with a default value of 0x07D0 (2000mAh), which corresponds to 2000mAh.

14.4 SOC Report

The *StateOfCharge* register is a read-only register that displays the cell's state of charge as calculated by the VGCS algorithm. The result is expressed as a percentage of the cell's full capacity. This register automatically adjusts to changes in battery size, as the fuel gauge naturally accounts for relative SOC. The SOC is measured in percent (%). The reported SOC also includes residual capacity, which may not be accessible to the actual application due to the requirements for early termination voltage. When the SOC reads 0%, it typically indicates that there is no remaining capacity for standard applications. The register is first updated 250ms after the IC's Power-On Reset (POR).

14.5 Power Mode

The RT9427 features three power modes, each tailored for various applications with differing power consumption requirements. These modes include active mode, sleep mode, and shutdown mode.

14.6 Active Mode

The active mode is recommended and is the default power mode after a Power-On Reset (POR). In active mode, the *Voltage*, *Current*, *Temperature*, *AverageVoltage*, *AverageCurrent* and *AverageTemperature* registers are updated every second.

14.7 Sleep Mode

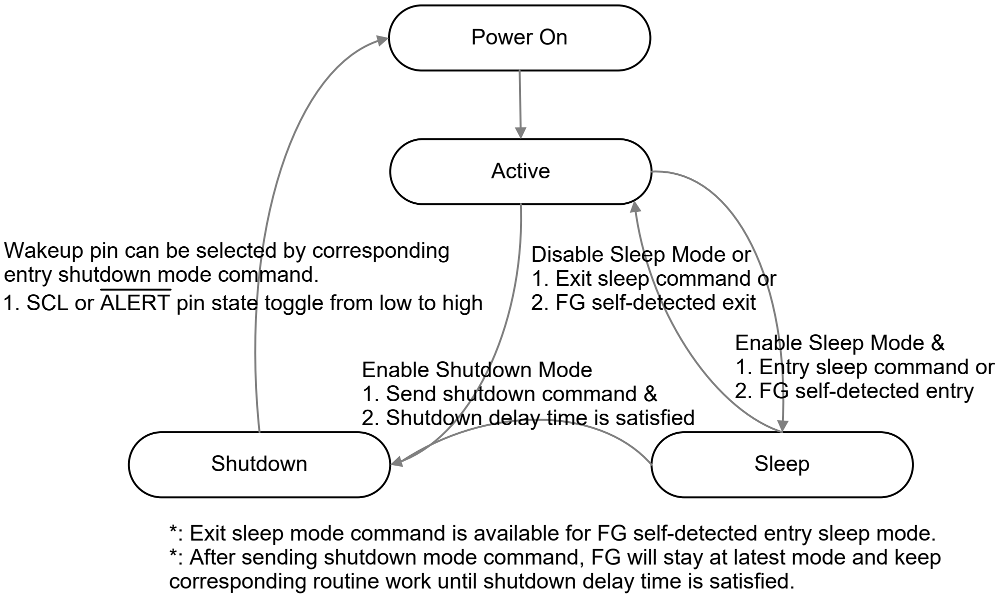
The sleep mode behavior is the same as the active mode but with a longer measurement period. The period programmable in the sleep mode, with the minimum being twice that of active mode and the maximum being 16 times longer. The default period is 4 times that of active mode. Sleep mode can be entered or exited by sending specific commands or through the fuel gauge's self-detection feature.

14.8 Shutdown Mode

In shutdown mode, the RT9427 stops all measurement activities and does not update registers, thereby maintaining minimum power consumption. To enter shutdown mode, the function must first be enabled, and shutdown delay time is satisfied after sending entry shutdown mode command.

To exit shutdown mode, it can be woken up by SCL or $\overline{\text{ALERT}}$ pin transition from low to high and the low period should satisfy t_{WAKE}. The wakeup pin can be selected by corresponding entry shutdown mode command.

14.9 Power Mode Switching



14.10 Controller

The controller manages the control flow of system routines, ADC measurement processes, algorithm calculations, and alert determinations.

14.11 Power-Up Sequence

When the RT9427 is powered on, the fuel gauge measures the battery voltage and estimates the initial SOC according to the voltage over a period of 250ms. The initial SOC will be accurate if the battery has been well relaxed for over 30 minutes. If not, there may be an initial SOC discrepancy. However, this discrepancy will diminish overtime as the SOC adjusts gradually and eventually aligns with the open circuit voltage (OCV) when the battery is at rest.

14.12 Quick Sensing

A Quick Sensing operation allows the RT9427 to restart battery voltage sensing and *StateOfCharge* calculation. The operation is used to reduce the initial *StateOfCharge* error caused by improper power-on sequence. A Quick Sensing operation can be performed by I^2C Quick Sensing command (0x4000) to the *Control* register.

14.13 Alert Function

The RT9427 supports various alerts to inform the system of abnormal conditions , such as over-temperature or undervoltage. These alerts include over-temperature in charge (OTC), over-temperature in discharge (OTD), overvoltage (OV), undervoltage (UV), under-SOC (US), SOC change (SC), overcurrent in charge (OCC), overcurrent in discharge (ODC), and temperature change (TC) alerts.

The host can periodically poll the ALERT flag to monitor the system status or configure it to receive an interrupt notification from the RT9427 $\overline{\text{ALERT}}$ pin. The alert must be enabled to function properly. There are 2 ways to enable the alert function. One is to enable a specific bit operation, and the other requires setting a proper value for the detection threshold. For detailed information, refer to the diagram and descriptions below.

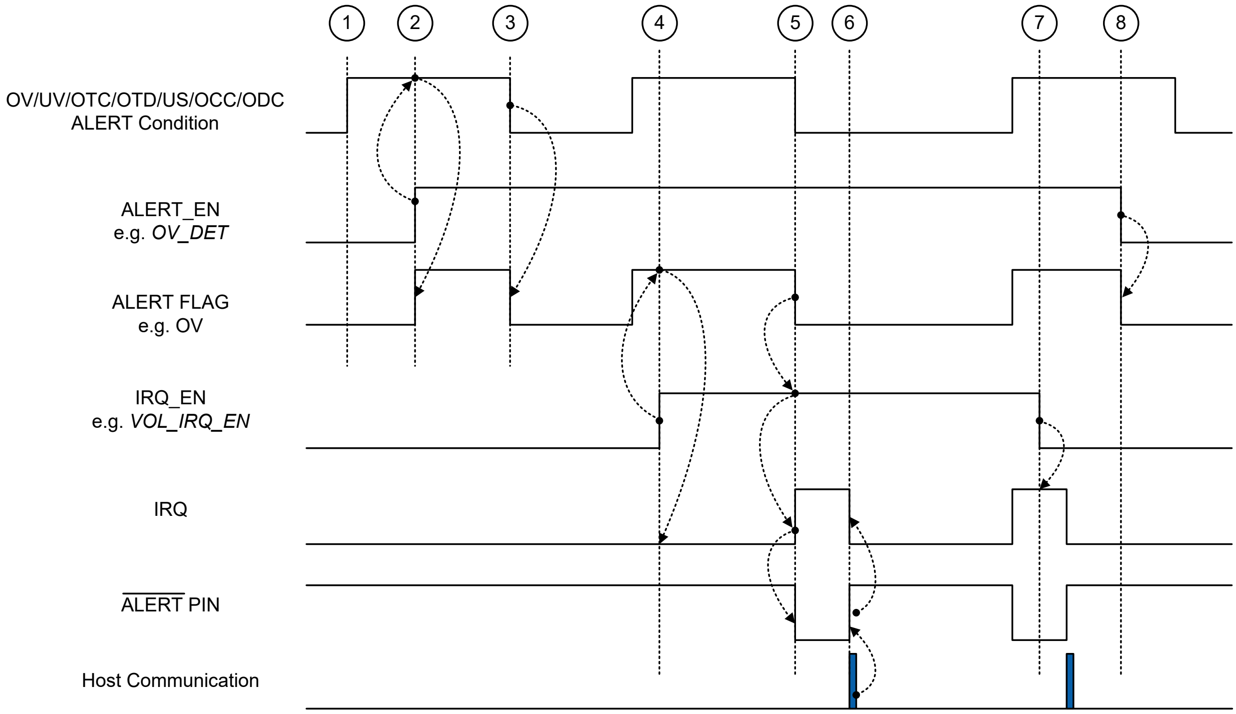


Figure 1. ALERT Function Timing Diagram

1. When an ALERT occurs but ALERT_EN is disabled, the ALERT FLAG will not generate a response.
2. When an ALERT_EN is enabled, the ALERT FLAG is set when an ALERT condition occurs
3. The ALERT FLAG is cleared when the ALERT condition is recovered.
4. When the ALERT FLAG is already set and IRQ_EN is also set, the IRQ and $\overline{\text{ALERT}}$ PIN outputs will not generate a response.
5. The IRQ is set, and the $\overline{\text{ALERT}}$ PIN outputs low only when the IRQ_EN is set, and the ALERT FLAG state changes.
6. IRQ and $\overline{\text{ALERT}}$ PIN are read clear only.
7. Clearing the IRQ_EN has no effect on the IRQ and $\overline{\text{ALERT}}$ PIN outputs.
8. Disable the ALERT_EN will also clear the ALERT FLAG.

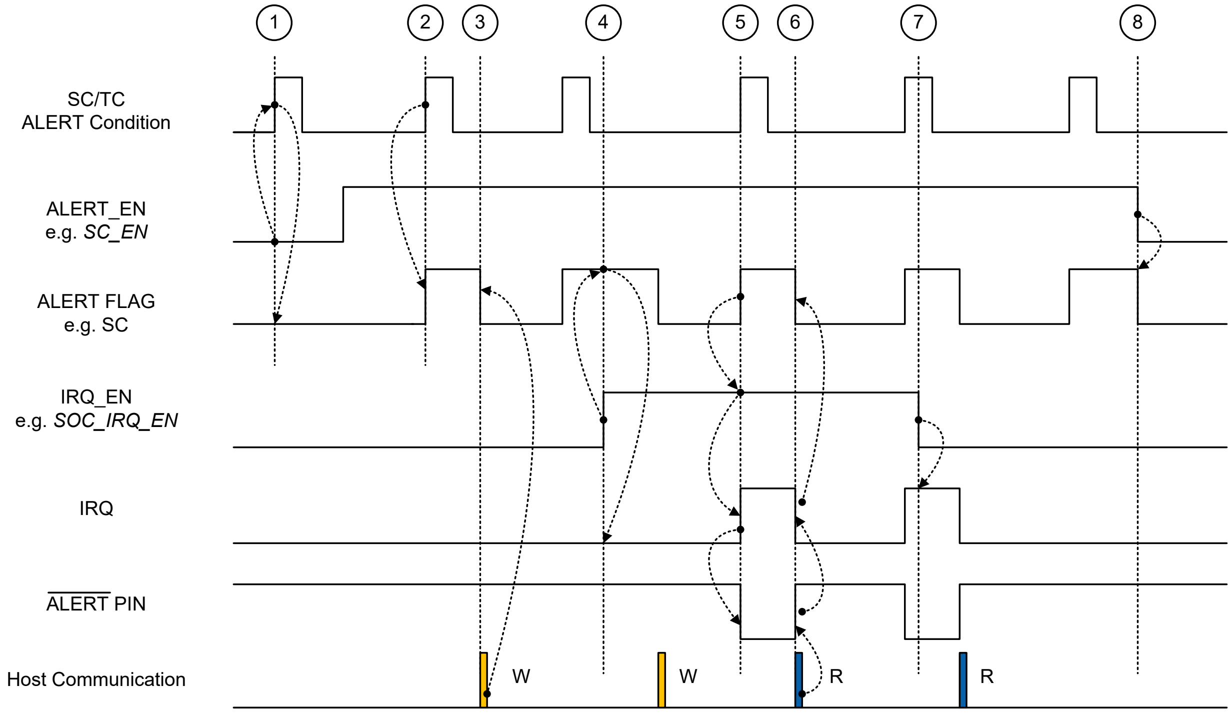
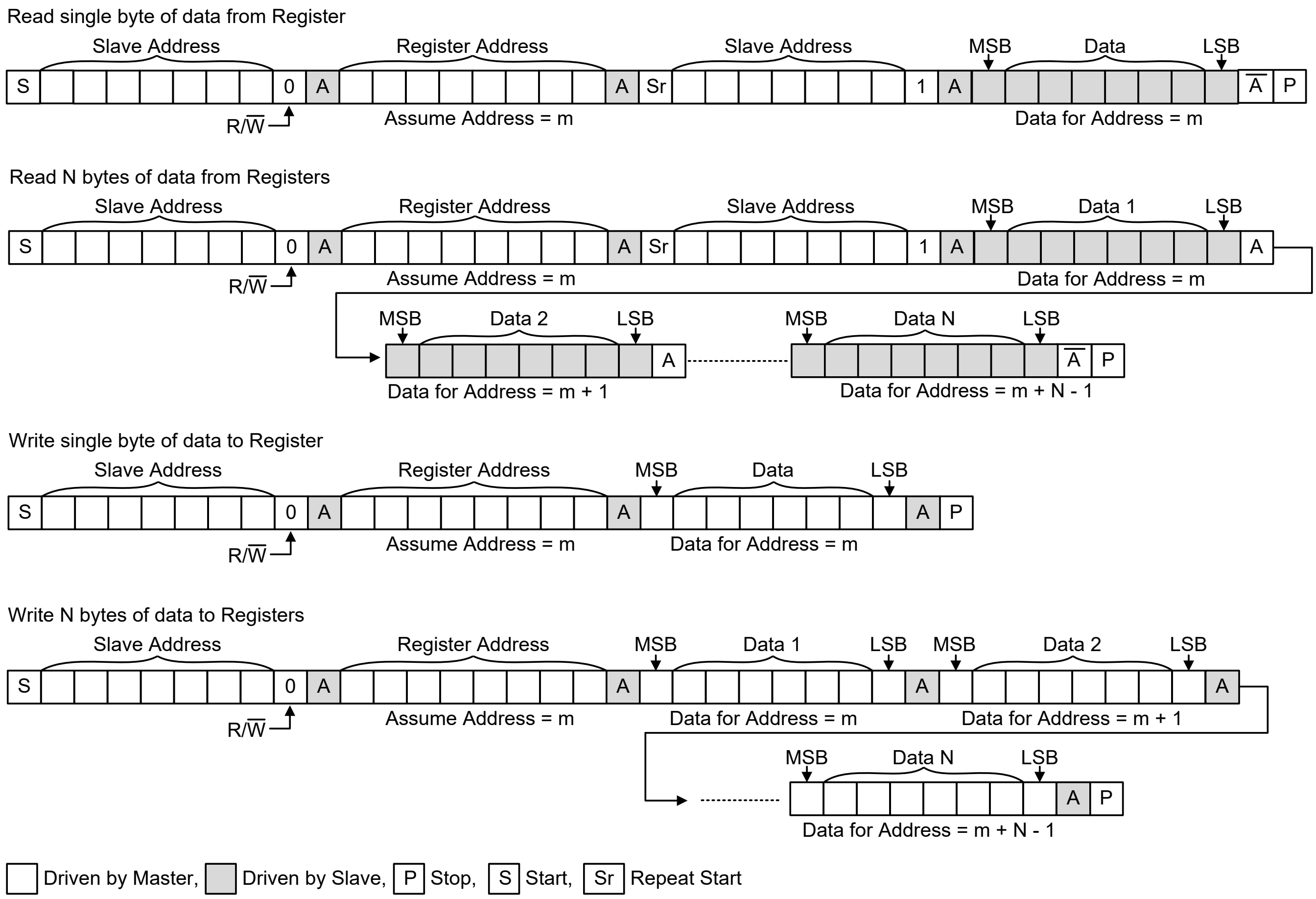


Figure 2. SC/TC ALERT Function Timing Diagram

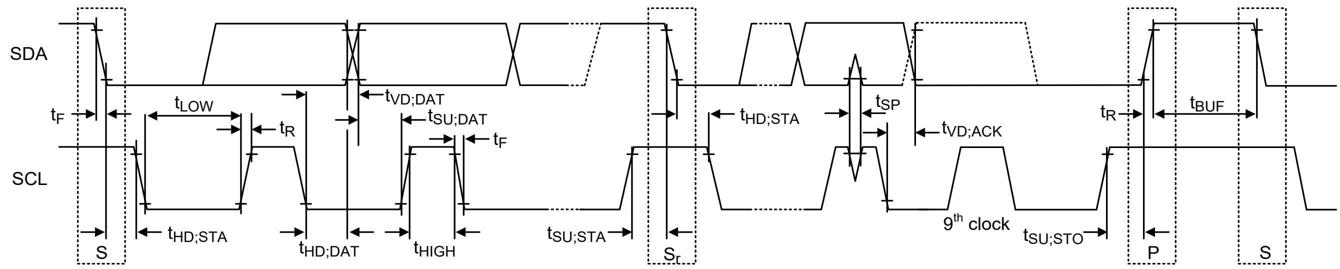
1. When an ALERT condition occurs but the ALERT_EN is disabled, the ALERT FLAG will not generate a response.
2. When the ALERT_EN is enabled, the ALERT FLAG is set when an ALERT condition occurs.
3. The ALERT FLAG is cleared when the driver writes ALERT_FLAG to 0.
4. When the ALERT_FLAG is already set and IRQ_EN is also set, the IRQ and the $\overline{\text{ALERT}}$ PIN outputs will not generate a response.
5. The IRQ is set and the $\overline{\text{ALERT}}$ PIN outputs low only when the IRQ_EN is set, and the ALERT FLAG state changes.
6. The IRQ and the $\overline{\text{ALERT}}$ PIN are read-only and will be cleared when the driver executes a read action.
7. Clearing the IRQ_EN has no effect on the IRQ and the $\overline{\text{ALERT}}$ PIN outputs.
8. Disabling the ALERT_EN will also clear the ALERT_FLAG.

14.14 I²C Interface

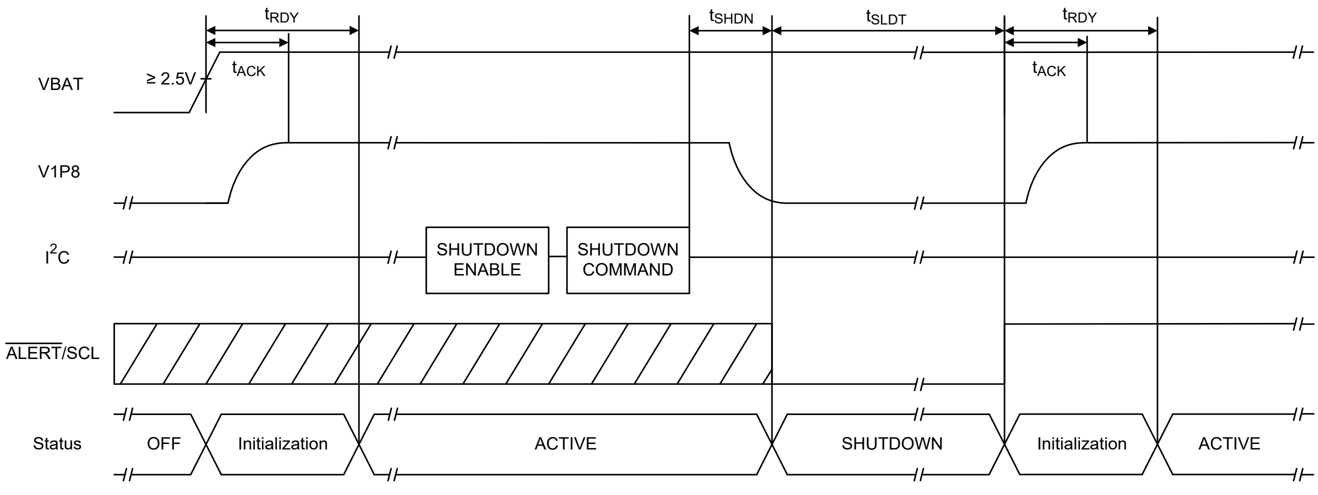
The RT9427 I²C slave address = 7'b1010101. The I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream is shown below:



14.15 I²C Waveform Information



14.16 Shutdown and Wake-Up Timing



*: Wake-up pin can be selected by corresponding entry shutdown mode command.

14.17 Register Summary Table

Name	Symbol	Address	Unit	Mode	Reset
Control	CNTL	0x00 to 0x01	--	R/W	0x0000
Current	CURR	0x04 to 0x05	mA	R	0x0000
Temperature	TEMP	0x06 to 0x07	0.1°K	R/W	0x0BA6
Voltage	VBAT	0x08 to 0x09	mV	R	0x0ED8
Flag1	FLAG1	0x0A to 0x0B	--	R	0x0000
Flag2	FLAG2	0x0C to 0x0D	--	R	0x0000
DeviceID	DVCID	0x0E to 0x0F	--	R	0x2720
RemainingCapacity	RM	0x10 to 0x11	mAh	R	0x03E8
FullChargeCapacity	FCC	0x12 to 0x13	mAh	R	0x07D0
AverageCurrent	AI	0x14 to 0x15	mA	R	0x0000
TimeToEmpty	TTE	0x16 to 0x17	minute	R	0xFFFF
Version	VER	0x20 to 0x21	--	R	0x0001
VGCOMP12	VGCOMP12	0x24 to 0x25	--	R/W	0x3232
VGCOMP34	VGCOMP34	0x26 to 0x27	--	R/W	0x3232
InternalTemerature	INTT	0x28 to 0x29	0.1°K	R	0x0BA6
CycleCount	CYC	0x2A to 0x2B	Counts	R/W	0x0000
StateOfCharge	SOC	0x2C to 0x2D	%	R	0x0032
StateOfHealth	SOH	0x2E to 0x2F	%	R	0x0064
Flag3	FLAG3	0x30 to 0x31	--	R	0x0000
IRQ	IRQ	0x36 to 0x37	--	R	0x0000
DesignCapacity	DC	0x3C to 0x3D	mAh	R	0x07D0
ExtendedControl	EXTDCNTL	0x3E to 0x3F	--	W	0x0000
ExtendReg0 to 15	EXTREG0 to 15	0x40 to 0x4F	--	R/W	0xFFFF

Name	Symbol	Address	Unit	Mode	Reset
ExtPageChecksum	PAGE_CKS	0x50 to 0x51	--	R	0xFFFF
AverageVoltage	AV	0x64 to 0x65	mV	R	0x0ED8
AverageTemperature	AT	0x66 to 0x67	0.1°K	R	0x0BA6
ExtTotalChecksum	TOTAL_CKS	0x68 to 0x69	--	R	0x0000

14.18 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to- ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 2x2.5 (FC) package, the thermal resistance, θ_{JA}, is 112.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WL-CSP-9B 1.68x1.81 (BSC) package, the thermal resistance, θ_{JA}, is 55°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (112.6°C/W) = 0.88W for a WDFN-10L 2x2.5 (FC) package.

$P_{D(MAX)}$ = (125°C – 25°C) / (55°C/W) = 1.81W for a WL-CSP-9B 1.68x1.81 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allow the user to see the effect of rising ambient temperature on the maximum power dissipation.

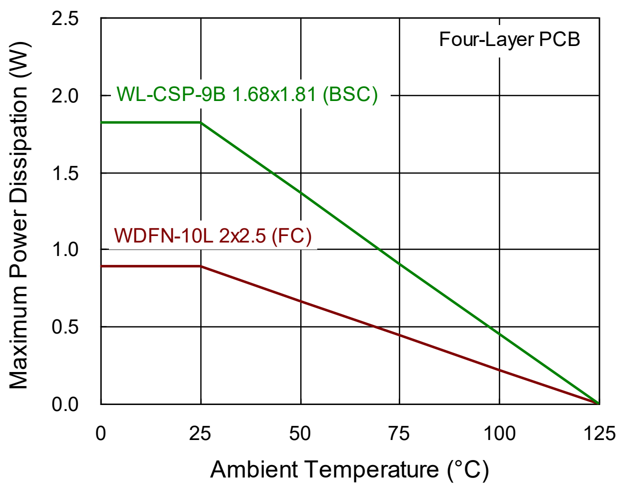


Figure 3. Derating Curve of Maximum Power Dissipation

14.19 Layout Considerations

To ensure the measurement accuracy of the RT9427, follow these recommended layout guidelines:

- The capacitor on the VBAT pin must be placed as close as possible to each other to minimize noise interference.
- The VBAT and VBATG paths must form Kelvin sense connection with the P+ and P- to minimize the IR drop effect on voltage measurement accuracy.
- The CSN and CSP paths must form Kelvin Sense connection with the RS to minimize the IR drop effect on current measurement accuracy.
- The NTC should be placed as close as possible to the battery and far away from the heat-generating area.
- The capacitor of the V1P8 pin must be placed as close as possible to the IC.
- There are no special layout requirements for other pins.

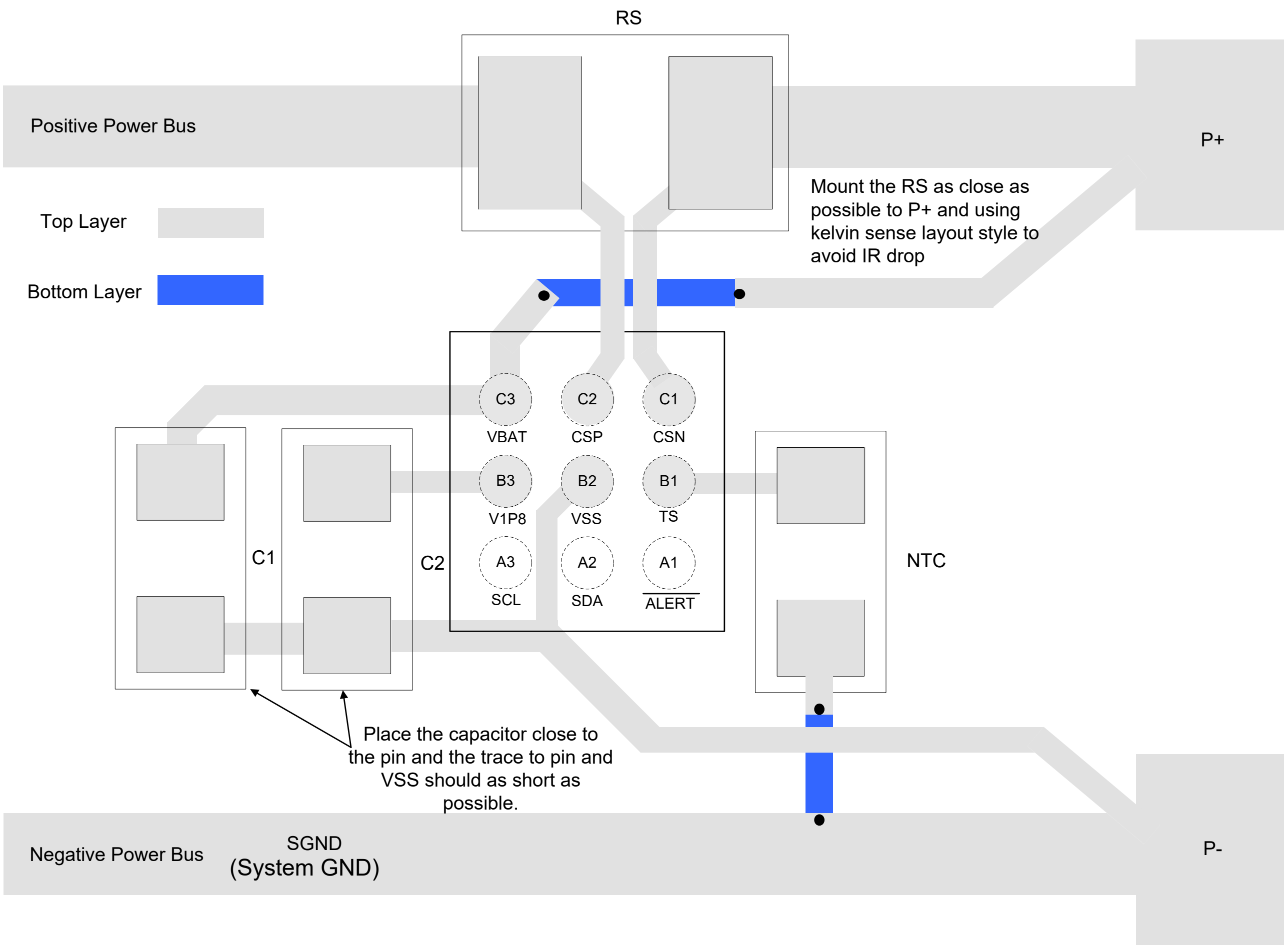


Figure 4. High-Side Sensing PCB Layout Guide for WL-CSP-9B 1.68x1.81 (BSC) Package

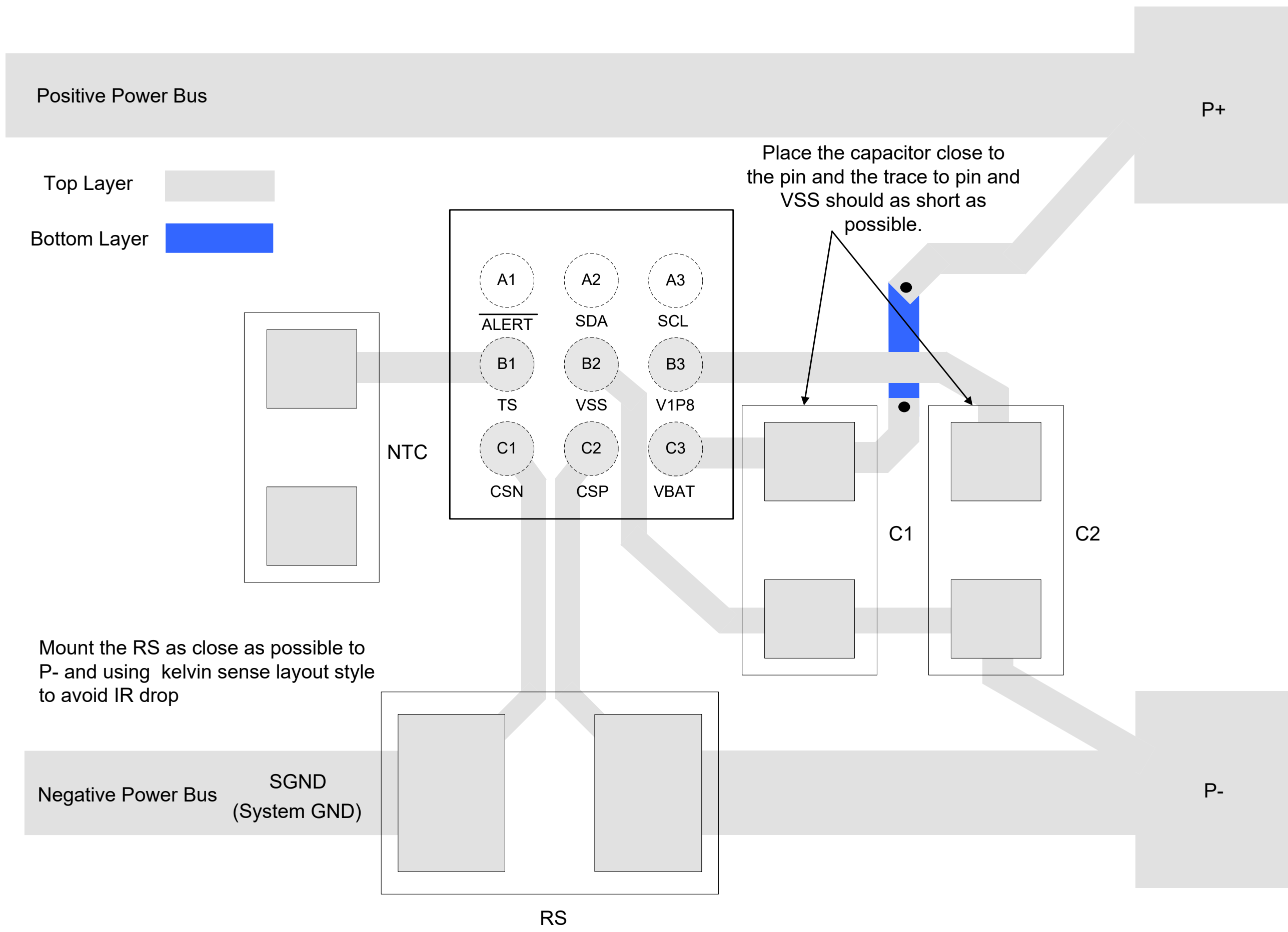


Figure 5. Low-Side Sensing PCB Layout Guide for WL-CSP-9B 1.68x1.81 (BSC) Package

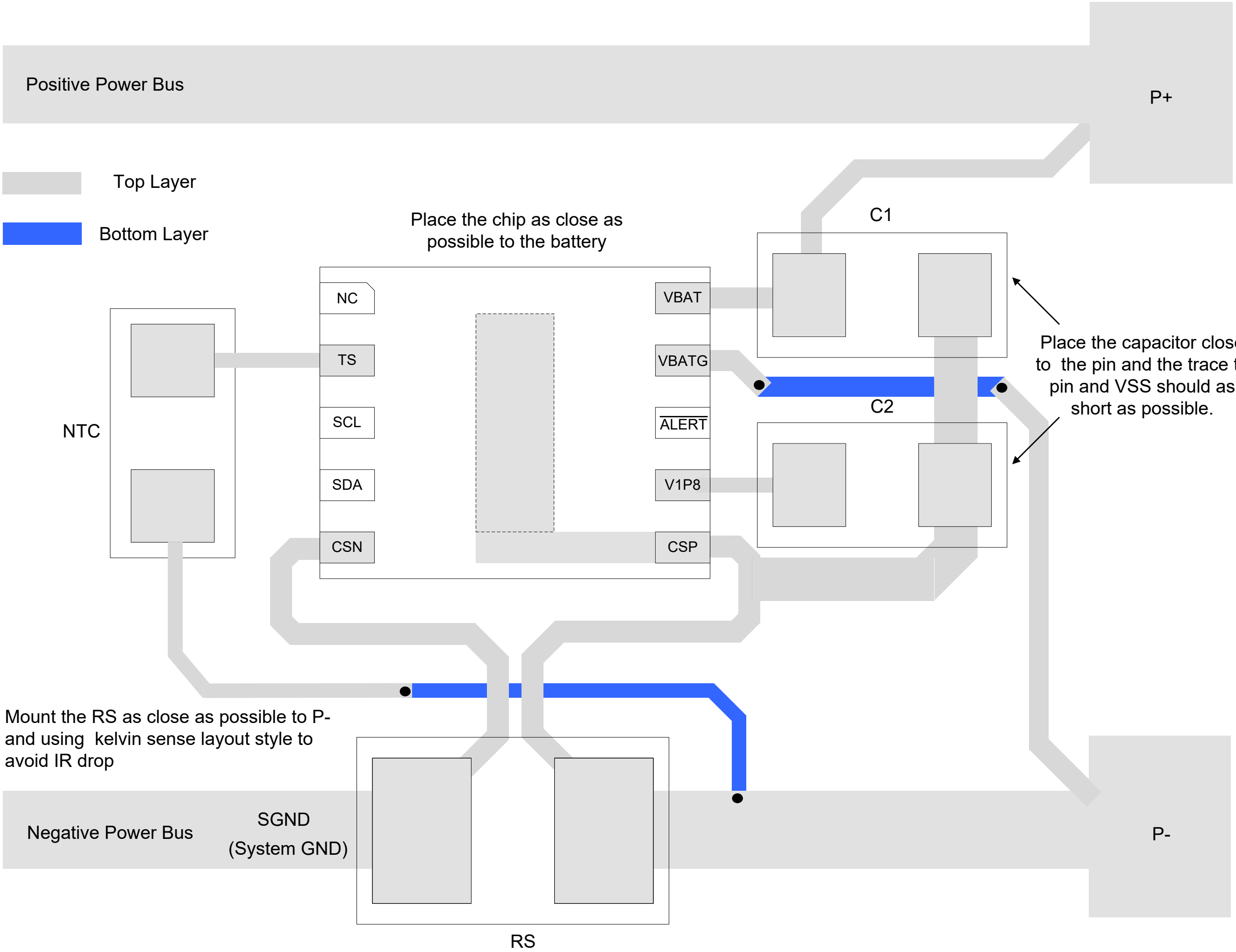
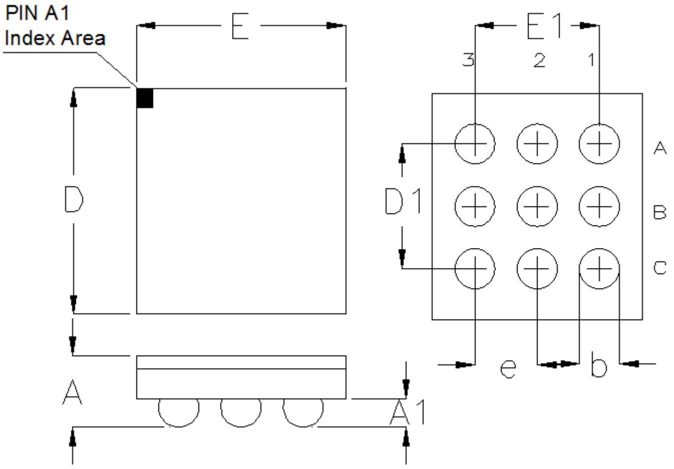


Figure 6. Low-Side Sensing PCB Layout Guide for WDFN-10L 2x2.5 (FC) Package

Note 17. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

15 Outline Dimension

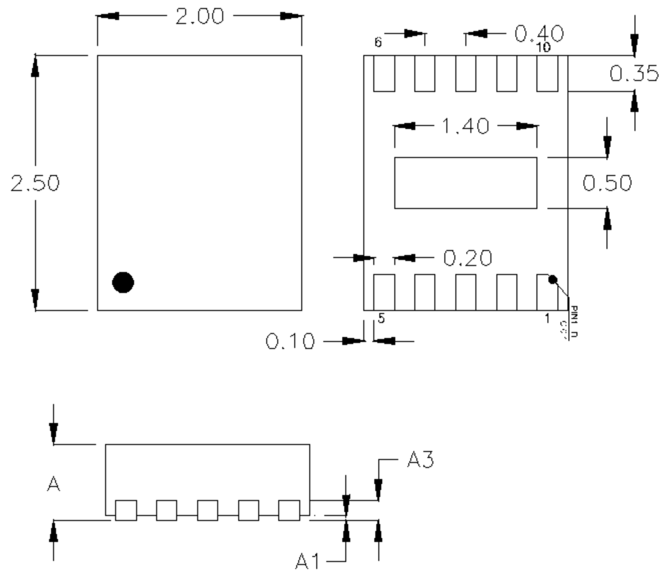
15.1 WL-CSP-9B 1.68x1.81 (BSC) Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.525	0.625	0.021	0.025
A1	0.200	0.260	0.008	0.010
b	0.290	0.350	0.011	0.014
D	1.770	1.850	0.070	0.073
D1	1.000		0.039	
E	1.640	1.720	0.065	0.068
E1	1.000		0.039	
e	0.500		0.020	

9B WL-CSP 1.68x1.81 Package (BSC)

15.2 WDFN-10L 2x2.5 (FC) Package



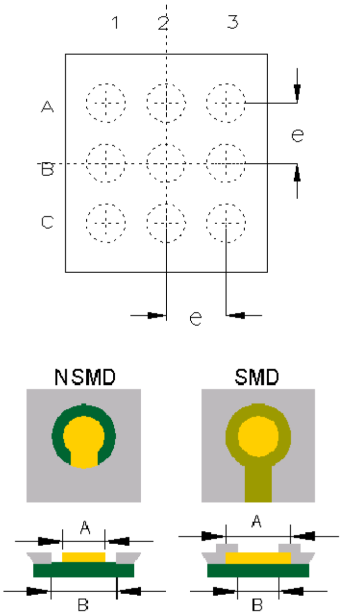
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010

Tolerance
±0.050

W-Type 10L DFN 2x2.5 Package (FC)

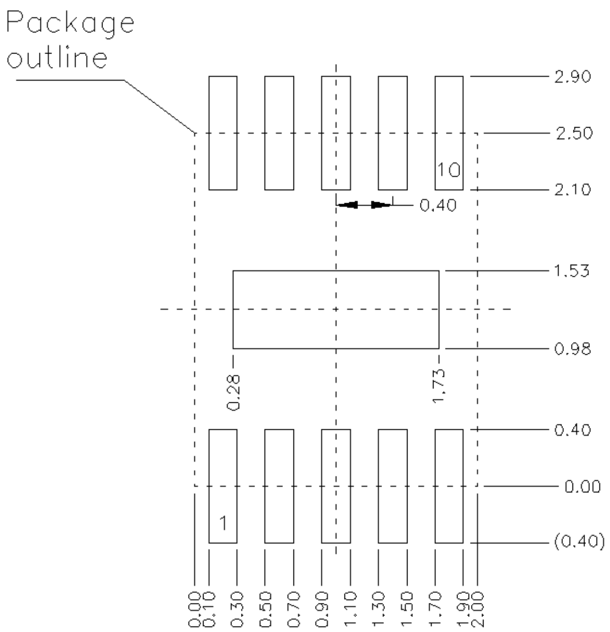
16 Footprint Information

16.1 WL-CSP-9B 1.68x1.81 (BSC) Package



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.68x1.81-9(BSC)	9	NSMD	0.500	0.275	0.375	±0.025
		SMD		0.305	0.275	

16.2 WDFN-10L 2x2.5 (FC) Package

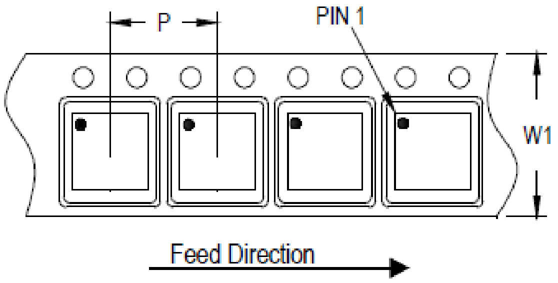


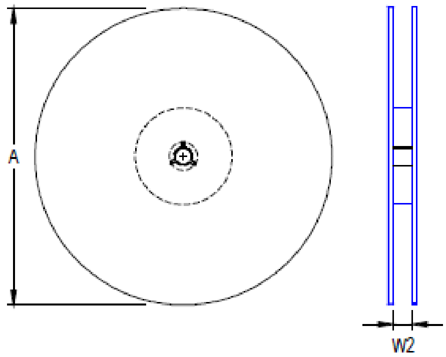
Package	Number of Pin	Tolerance
V/W/U/XDFN2x2.5-10(FC)	10	±0.05

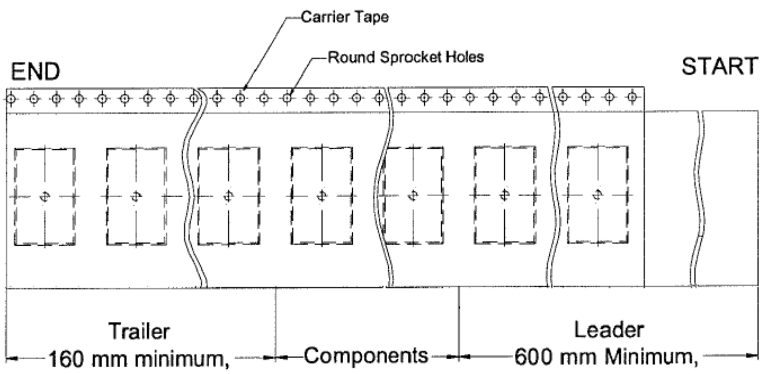
17 Packing Information

17.1 Tape and Reel Data

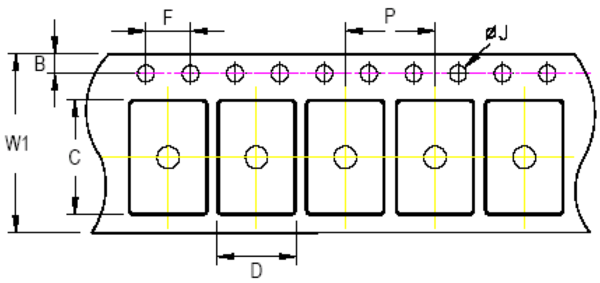
17.1.1 WL-CSP-9B 1.68x1.81 (BSC)

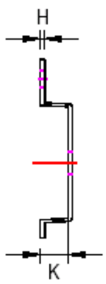






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 1.68x1.81	8	4	180	7	3,000	160	600	8.4/9.9



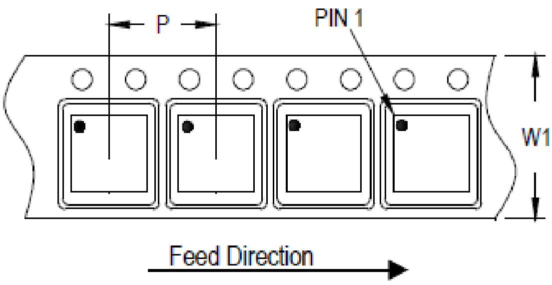


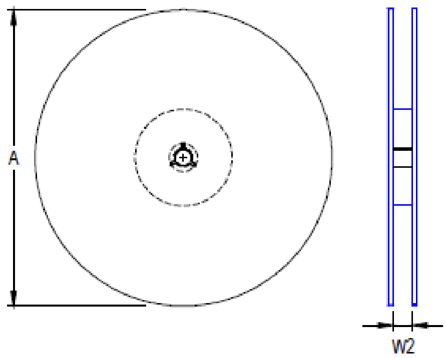
C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

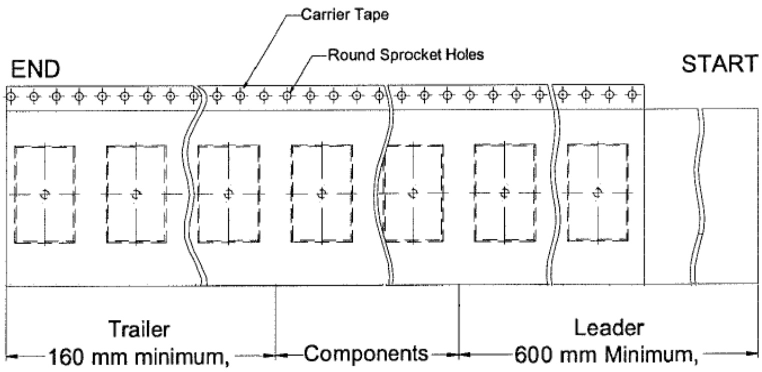
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.68mm	0.78mm	0.6mm

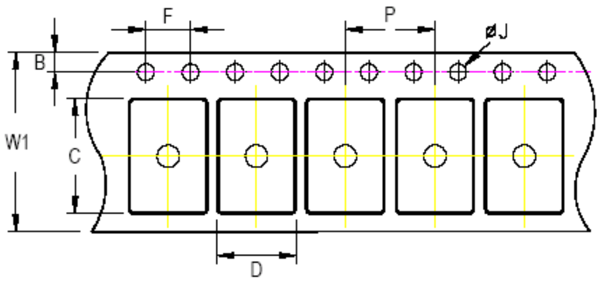
17.1.2 WDFN-10L 2x2.5 (FC)

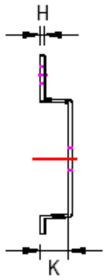






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 2x2.5	12	8	180	7	1,500	160	600	12.4/14.4





C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

17.2 Tape and Reel Packing

17.2.1 WL-CSP-9B 1.68x1.81 (BSC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 1.68x1.81	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

17.2.2 WDFN-10L 2x2.5 (FC)

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 2x2.5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

17.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

18 Datasheet Revision History

Version	Date	Description
00	2023/1/17	First Edition
01	2026/3/5	Ordering Information - Updated notes Marking Information - Updated Packing Information WL-CSP-9B 1.68x1.81 (BSC) WDFN-10L 2x2.5 (FC) - Added tape size K