RICHTEK®

RT9297

3A High-Performance Boost Converter

1 General Description

The RT9297 is a high-performance boost converter that provides a regulated supply voltage for active-matrix thin-film transistor (TFT) liquid-crystal displays (LCDs).

The boost converter incorporates current-mode, fixed-frequency, pulse-width modulation (PWM) circuitry with a built-in N-Channel power MOSFET to achieve high efficiency and fast transient response.

The RT9297 is available in a WDFN-10L 3x3 package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT9297 □□□

Pin 1 Orientation
Empty: Quadrant 1
(2): Quadrant 2, Follow EIA-481

Package Type(1)
QW: WDFN-10L 3x3 (W-Type)

Lead Plating System
G: Green (Halogen Free and Pb Free)(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **High Efficiency up to 90%**
- **Adjustable Output Voltage: V_{DD} to 24V**
- **Wide Input Supply Voltage: 2.6V to 5.5V**
- **Input Undervoltage-Lockout**
- **Pin-Programmable Switching Frequency 640kHz/1.2MHz**
- **Programmable Soft-Start**
- **Small 10-Lead WDFN Package**

4 Applications

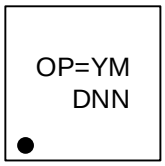
- Notebook Computer Displays
- LCD Monitor Panels
- LCD TV Panels

5 Marking Information

RT9297GQW

EZ=: Product Code
YMDNN: Date Code

RT9297GQW(2)



OP=: Product Code
YMDNN: Date Code

6 Simplified Application Circuit

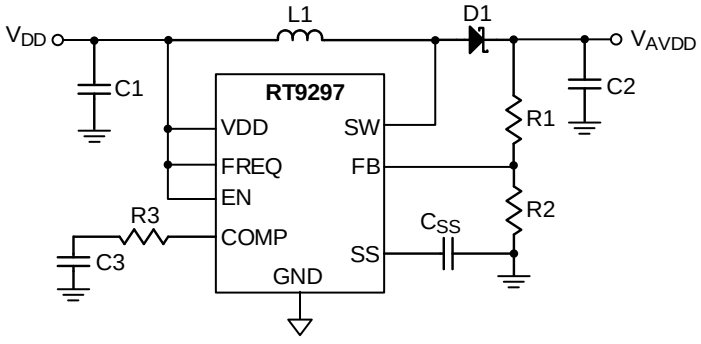
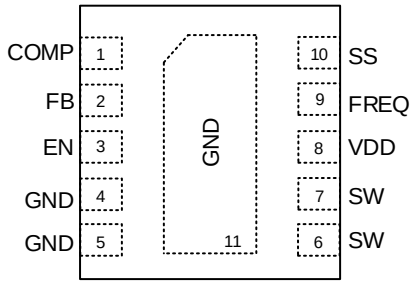


Table of Contents

7 Pin Configuration

(TOP VIEW)

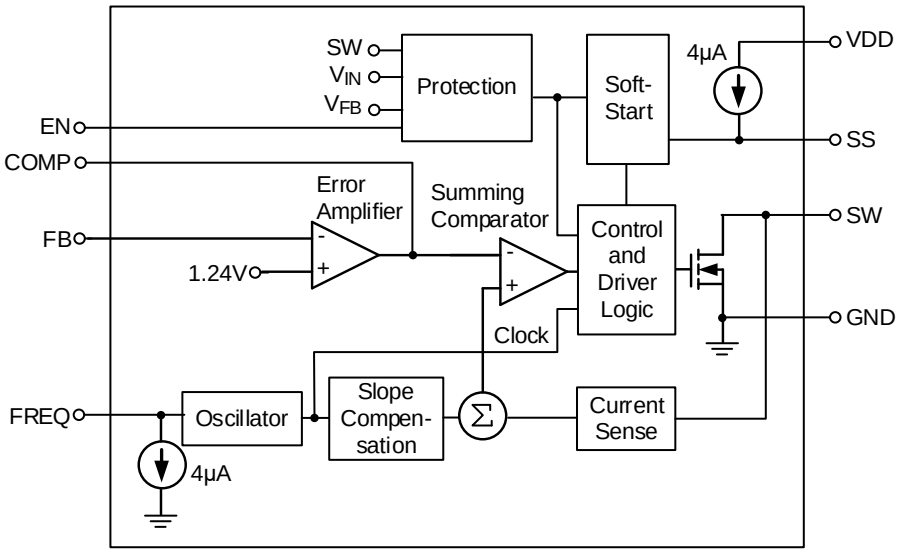


WDFN-10L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	COMP	Compensation pin. Connect a series RC circuit from the COMP pin to ground for error amplifier compensation.
2	FB	Feedback pin. The nominal feedback regulation voltage is 1.24V. Connect an external resistor voltage divider between the boost converter's output (VAVDD) and ground (GND), with the center tap connected to the FB pin. To reduce noise coupling, place the voltage-divider close to the IC and minimize the trace area.
3	EN	Enable control input. Drive EN low to turn off the boost converter.
4, 5, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6, 7	SW	Switch node. SW serves as the drain of the internal MOSFET. To minimize electromagnetic interference (EMI), connect the junction of the inductor and rectifier diode to SW and ensure the trace area is as small as possible.
8	VDD	Supply pin. Bypass VDD by connecting a ceramic capacitor with a minimum value of 1μF directly to GND.
9	FREQ	Frequency-select input. The oscillator frequency is set to 640kHz when the FREQ input is low, and is set to 1.2MHz when FREQ is high. Additionally, this input features a pull-down current of 6μA.
10	SS	Soft-start control pin. Connect a soft-start capacitor (CSS) to this pin. A 4μA constant current charges the soft-start capacitor. When EN is connected to GND, the soft-start capacitor is discharged. When EN is connected to VDD high, the soft-start capacitor is charged to VDD. Leave floating if not using soft-start.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- SW to GND ---------- –0.3V to 26V
- Other Pins to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-10L 3x3 ---------- 1.667W
- Package Thermal Resistance (Note 3)

  WDFN-10L 3x3, θ_{JA} ---------- 60°C/W

  WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD ---------- 2.6V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

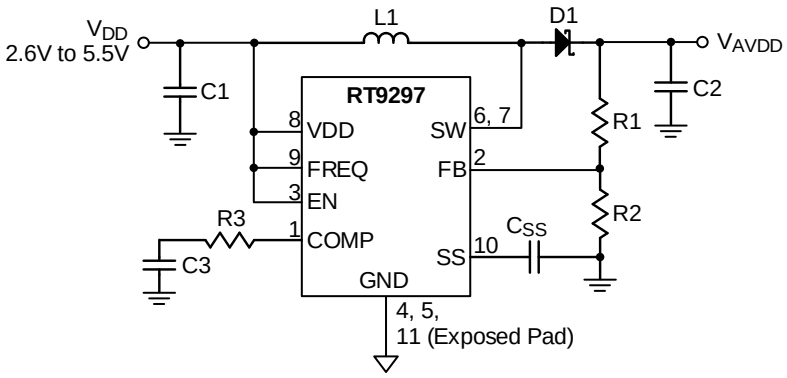
12 Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Input Voltage Range	V_{DD}	V_{AVDD} < 18V	2.6	--	5.5	V
		18V < V_{AVDD} < 24V	4	--	5.5	
Output Voltage Range	V_{AVDD}		V_{DD}	--	24	V
Undervoltage-Lockout Threshold	V_{UVLO}	V_{DD} rising	--	2.4	--	V
	V_{UVLO_HYS}	Hysteresis	--	50	--	mV
Quiescent Current	I_Q	V_{FB} = 1.3V, SW not switching	--	0.5	--	mA
		V_{FB} = 1V, SW switching	--	4	--	
Shutdown Current	I_{SHDN}	EN = GND	--	0.1	10	μA

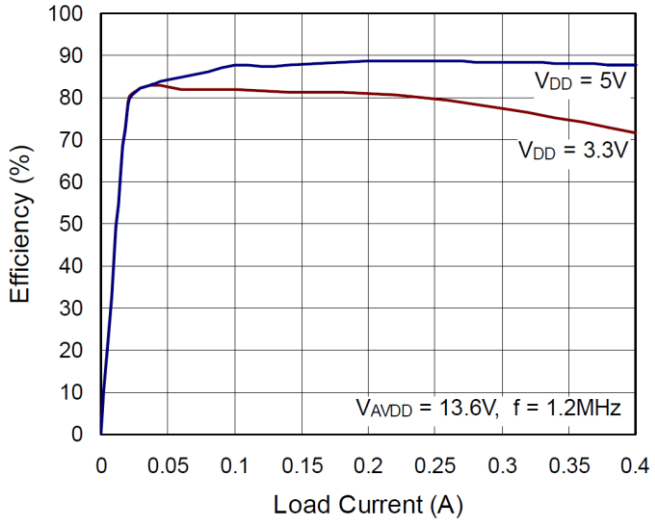
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator						
Oscillator Frequency	f_{SW}	FREQ = GND	500	640	750	kHz
		FREQ = VIN	1000	1240	1500	
Maximum Duty Cycle	D_{MAX}		--	90	--	%
Error Amplifier						
Feedback Regulation Voltage	V_{FB}		1.22	1.24	1.26	V
Feedback Input Bias Current	I_{FB}		--	125	250	nA
Feedback Line Regulation	$V_{LINE\_REG\_FB}$		--	0.05	0.2	%/V
Transconductance	gm	$\Delta I = \pm 2.5\mu A$ at COMP = 1V	--	135	--	μA/V
Voltage Gain	A_V	FB to COMP	--	700	--	V/V
N-MOSFET						
Current Limit	I_{LIM}		3	3.8	5	A
On-Resistance	R_{DSON}		--	125	250	mΩ
Leakage Current	I_{LK}	V_{SW} = 24V	--	30	45	μA
Current-Sense Transresistance	R_{CS}		--	0.25	--	V/A
Soft-Start						
Charge Current	I_{SS}		--	4	--	μA
Control Inputs						
EN, FREQ Input Voltage Logic-Low	V_{IL}		--	--	0.3 x V_{DD}	V
EN, FREQ Input Voltage Logic-High	V_{IH}		0.7 x V_{DD}	--	--	V
EN, FREQ Input Voltage Hysteresis	V_{IN_HYS}		--	0.1 x V_{DD}	--	V
FREQ Pull-Down Current	I_{PD}		--	6	--	μA
EN Input Current	I_{EN}	EN = GND	--	0.001	1	μA

13 Typical Application Circuit

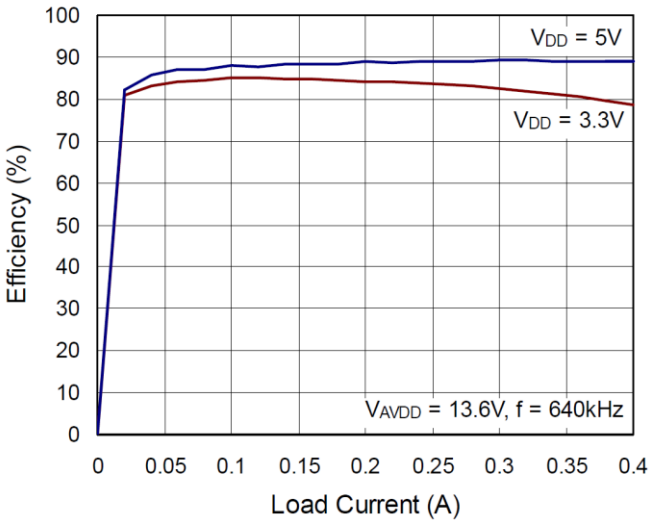


14 Typical Operating Characteristics

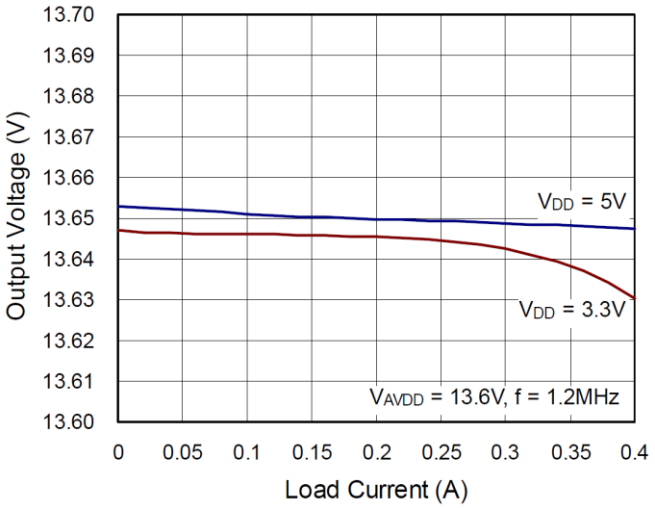
Efficiency vs. Load Current



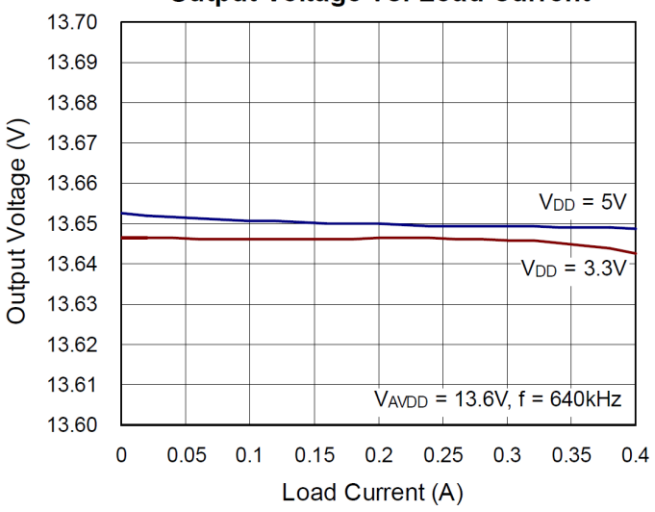
Efficiency vs. Load Current



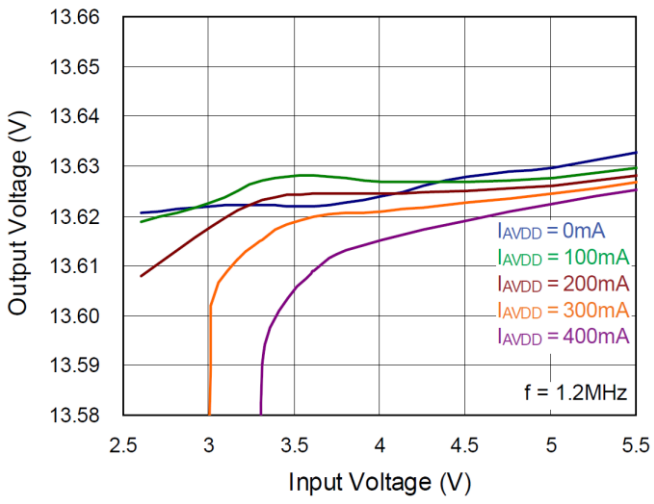
Output Voltage vs. Load Current



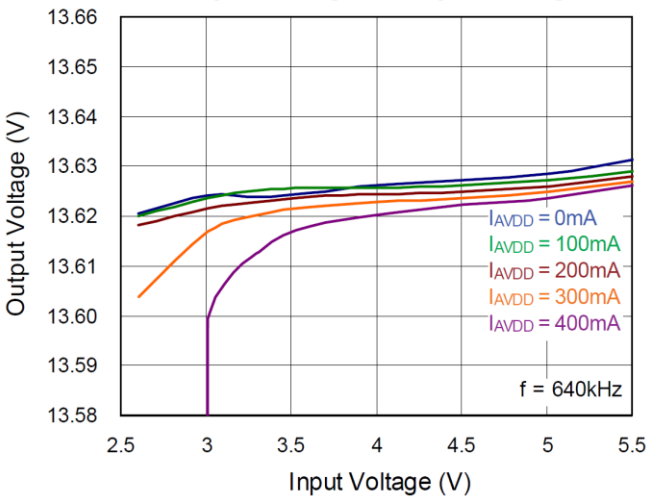
Output Voltage vs. Load Current



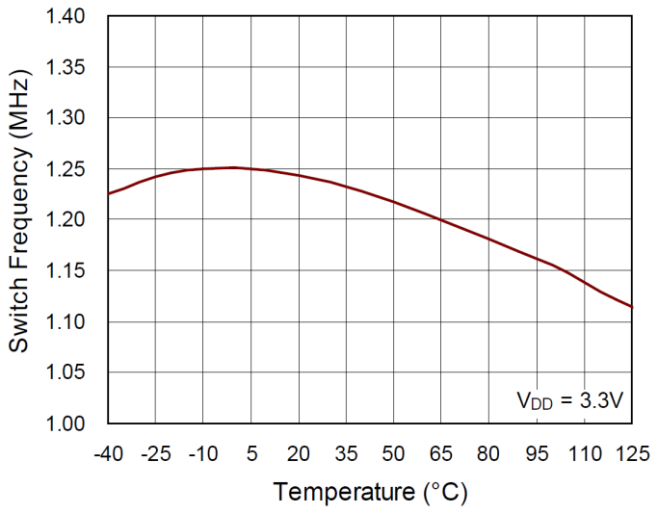
Output Voltage vs. Input Voltage



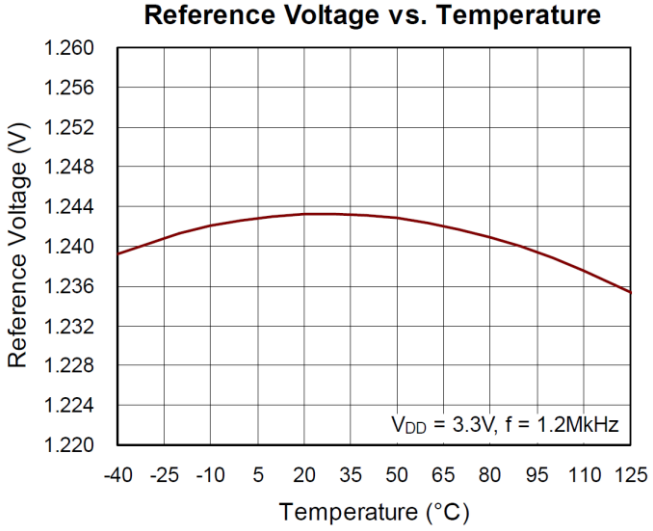
Output Voltage vs. Input Voltage



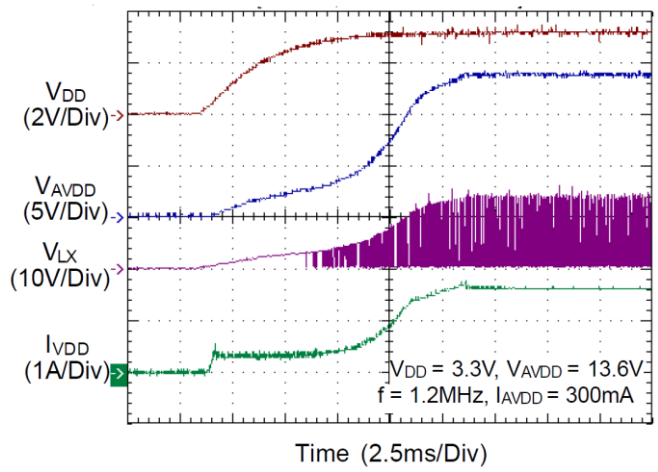
Switching Frequency vs. Temperature



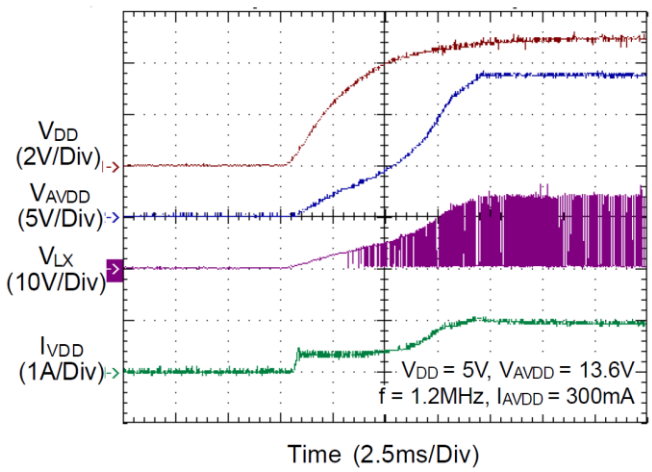
Reference Voltage vs. Temperature



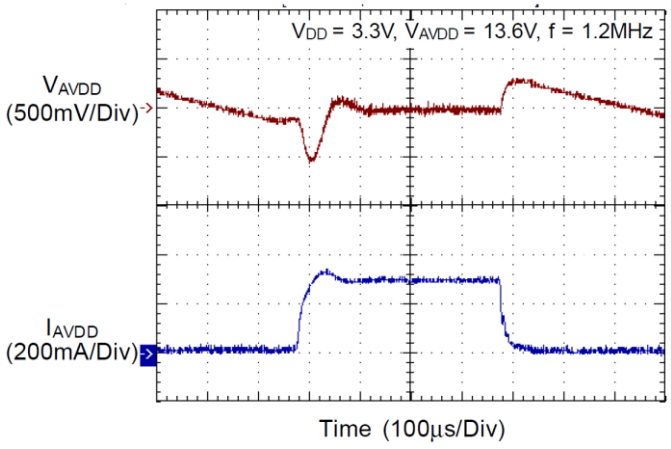
Start Up



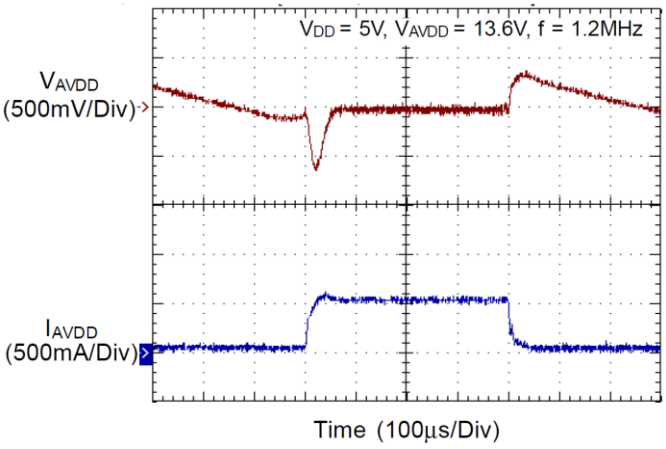
Start Up



Load Transient Response



Load Transient Response



15 Application Information

(Note 6)

The RT9297 is a high-performance boost converter designed to generate the voltage required by the panel source driver ICs. Detailed descriptions and component selection information follow.

15.1 Boost Converter

The boost converter features a high-efficiency, current-mode PWM architecture that operates at frequencies of either 640kHz or 1.2MHz. It is designed for fast transient responses, enabling it to generate the necessary power supplies for the source drivers of TFT LCD displays. The high operating frequency permits the use of smaller components, which helps to reduce the overall thickness of the LCD panel. The output voltage can be set by configuring a resistive voltage-divider connected to the FB (feedback) pin. The error amplifier adjusts the COMP (compensation) voltage in response to the voltage sensed at the FB pin, thereby regulating the output voltage. To enhance stability, a slope compensation signal is added to the current-sense signal. This combined signal is then compared with the COMP voltage to determine the current trip point and duty cycle.

15.2 Soft-Start Function

The RT9297 features a soft-start function designed to minimize inrush current during power-up. Upon powering on, an internal constant current source charges an external capacitor. This process limits the rate of voltage rise on the COMP pin during the charging period, which concurrently restricts the peak current in the inductor. When the power is turned off, the external capacitor is discharged, preparing it for the next soft-start cycle.

The soft-start function is facilitated by an external capacitor that is charged with a 4μA (microampere) constant current. To ensure proper output voltage regulation, the capacitor must have a sufficient capacitance. A typical value for the soft-start capacitor is 33nF, with an acceptable range from 10nF to 100nF.

15.3 Output Voltage Setting

The regulated output voltage is shown in the following equation:

$$V_{AVDD} = 1.24V \times \left(1+\frac{R_1}{R_2}\right)$$

The recommended value for R2 should be up to 10kΩ without any sacrifice in performance. Placing the resistor divider as close as possible to the chip can help reduce noise sensitivity.

15.4 Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of R_{COMP} and C_{COMP}. Choose R_{COMP} to set the high-frequency integrator gain for a fast transient response, and select C_{COMP} to set the integrator zero to maintain loop stability. For a typical application with V_{DD} = 3.3V, V_{AVDD} = 13.6V, C4 = 4.7μF x 3, and L = 3.6μH, the recommended values for compensation are as follows: R_{COMP} = 56kΩ and C_{COMP} = 330pF.

15.5 Overcurrent Protection

The RT9297 boost converter features overcurrent protection to limit the peak current in the inductor, preventing potential damage to the inductor and diode. During the ON-time, if the inductor current exceeds the preset current limit, the internal SW switch turns off immediately, effectively shortening the duty cycle. As a result, the output voltage may drop if an overcurrent condition occurs. It is important to note that the current limit is also influenced by the input voltage, duty cycle, and the value of the inductor.

15.6 Over-Temperature Protection

The RT9297 boost converter is equipped with over-temperature protection function to prevent the chip from overheating. When the junction temperature exceeds 155°C, the device will shut down to protect itself. Once the temperature has decreased by approximately 30°C, the device will resume normal operation. To ensure continuous operation, it is recommended not to exceed the maximum junction temperature rating of 125°C.

15.7 Inductor Selection

The inductance value is determined based on the maximum input current. A general rule of thumb is that the inductor current ripple should be between 20% and 40% of the maximum input current. Assuming we choose 40% as the criterion, then the calculation for the inductance will proceed accordingly.

$$I_{VDD(MAX)} = \frac{V_{AVDD} \times I_{AVDD(MAX)}}{\eta \times V_{DD}}$$

$I_{RIPPLE} = 0.4 \times I_{VDD(MAX)}$

where η is the efficiency, $I_{VDD(MAX)}$ is the maximum input current, I_{RIPPLE} is the inductor current ripple.

Additionally, the peak input current is the sum of the maximum input current and half of the inductor current ripple.

$I_{PEAK} = 1.2 \times I_{VDD(MAX)}$

Note that the saturation current of the inductor must exceed the peak current (I_{PEAK}). The inductance value can ultimately be determined using the following equation:

$$L = \frac{\eta \times (V_{DD})^2 \times (V_{AVDD} - V_{DD})}{0.4 \times (V_{AVDD})^2 \times I_{AVDD(MAX)} \times f_{SW}}$$

where f_{SW} represents the switching frequency of the system. To optimize system performance and minimize electromagnetic interference (EMI) issues, the use of a shielded inductor is recommended.

15.8 Diode Selection

A Schottky diode is an excellent choice for an asynchronous boost converter due to its low forward voltage drop. However, when selecting a Schottky diode, it is crucial to consider power dissipation, reverse voltage rating, and pulsating peak current as important parameters. It is advisable to select a diode with a reverse voltage rating that exceeds the maximum output voltage to ensure reliable operation.

15.9 Capacitor Selection

Output ripple voltage is an important metric for assessing performance. It comprises two components: one is the product of the input current and the Equivalent Series Resistance (ESR) of the output capacitor; the other is created by the charging and discharging cycles of the output capacitor. As shown in Figure 1, ΔV_{OUT1} can be evaluated using the principle of ideal energy equalization. Based on the definition of charge (Q), the Q value can be calculated using the following equation:

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{SW}} = C_{OUT} \times \Delta V_{OUT1}$$

where f_{SW} is the switching frequency, and ΔI_L represents the inductor ripple current. To estimate the value of ΔV_{OUT1}, move C_{OUT} to the left side of the equation as shown below:

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{SW}}$$

Finally, by incorporating the Equivalent Series Resistance (ESR) into the calculation, the total output ripple voltage can be determined using the following equation:

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{SW}}$$

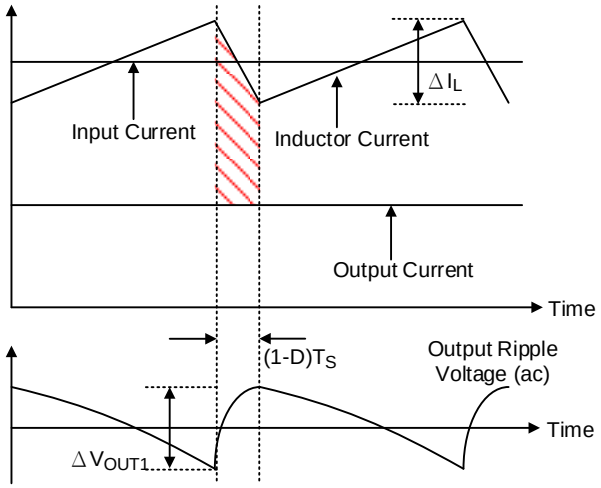


Figure 1. The Output Ripple Voltage without the Contribution of ESR

15.10 Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. A low ESR effectively reduces the input voltage ripple caused by the switching operation. A capacitance of 10μF is sufficient for most applications. However, this value can be reduced for applications with lower output current requirements. Another important consideration is that the voltage rating of the input capacitor must exceed the maximum input voltage.

15.11 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (60°C/W) = 1.667W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

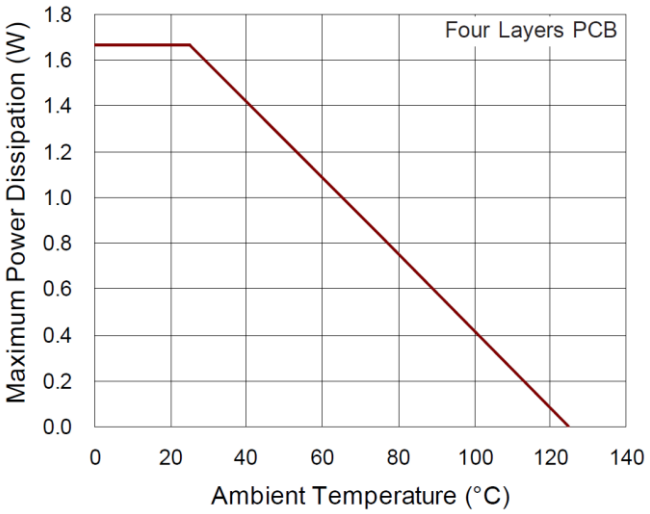


Figure 2. Derating Curve of Maximum Power Dissipation

15.12 Layout Considerations

For high-frequency switching power supplies, PCB layout plays a crucial role in achieving good regulation, high efficiency, and stability. The guidelines provided below are intended to assist in optimizing the PCB layout.

- For optimal regulation, position the power components as close together as possible. Ensure that the traces are both wide and short, particularly for the high-current output loop.
- Place the feedback voltage divider resistors close to the feedback pin. Keep the trace connecting to the center of the divider short and ensure it is isolated from any switching nodes to prevent noise interference.
- The compensation circuit should be placed at a distance from the power loops and shielded with a ground trace to avoid noise coupling.
- Minimize the area of the SW node and ensure that it is wide and short. Additionally, maintain a distance between the SW node and the FB pin to prevent interference.
- Connect the exposed pad of the chip to a robust ground plane to ensure optimal thermal management.

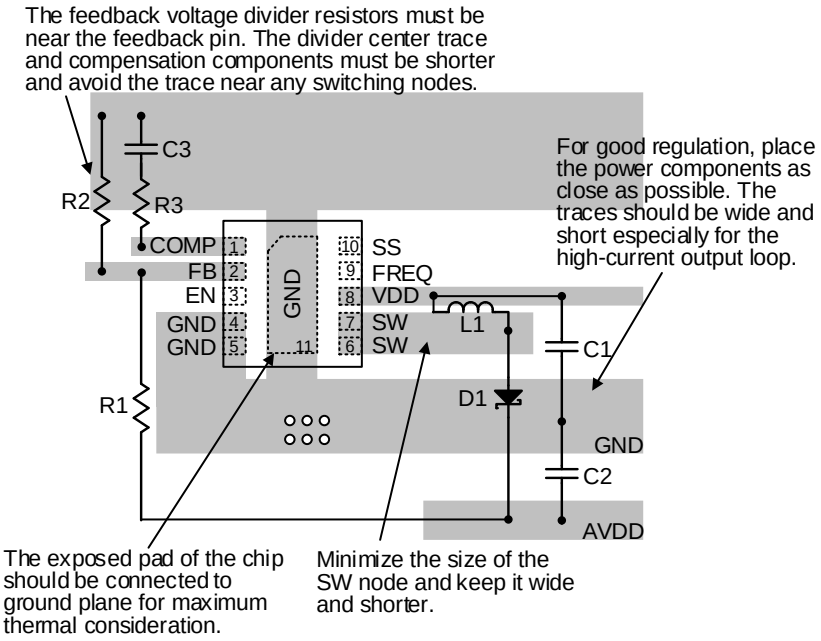
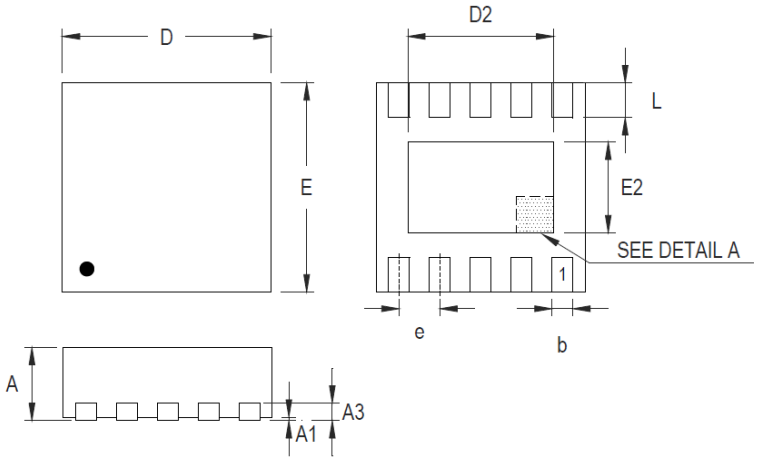
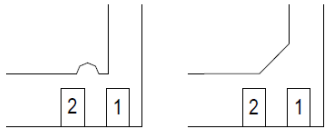


Figure 3. PCB Layout Guide

Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

16 Outline Dimension





DETAIL A

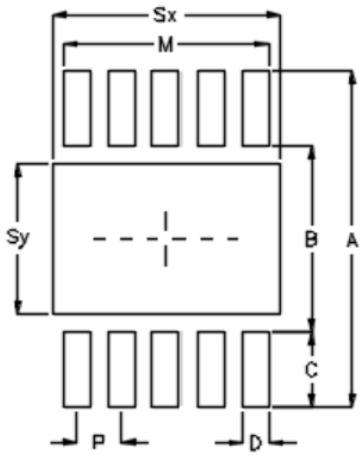
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

17 Footprint Information

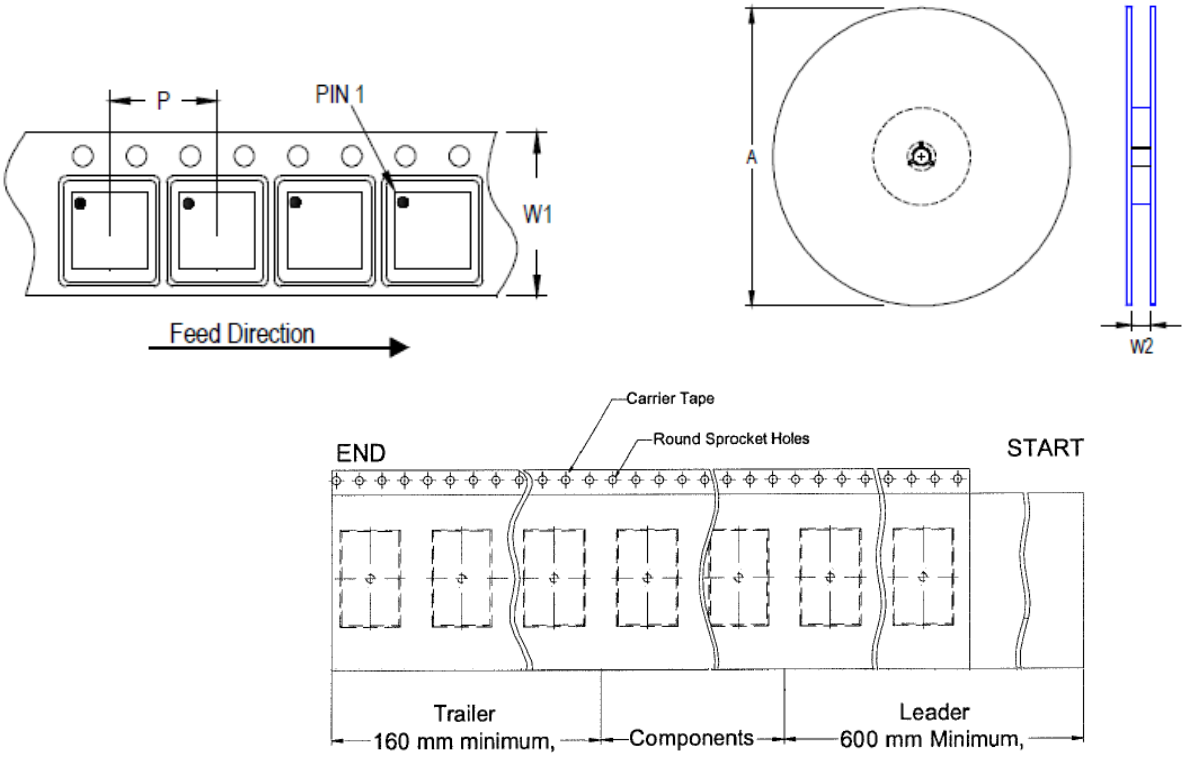


Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

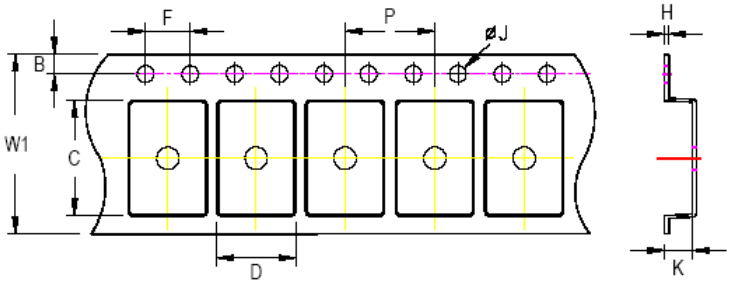
18 Packing Information

18.1 Tape and Reel Data

18.1.1 Pin 1 at Quadrant 1 for 7”



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4

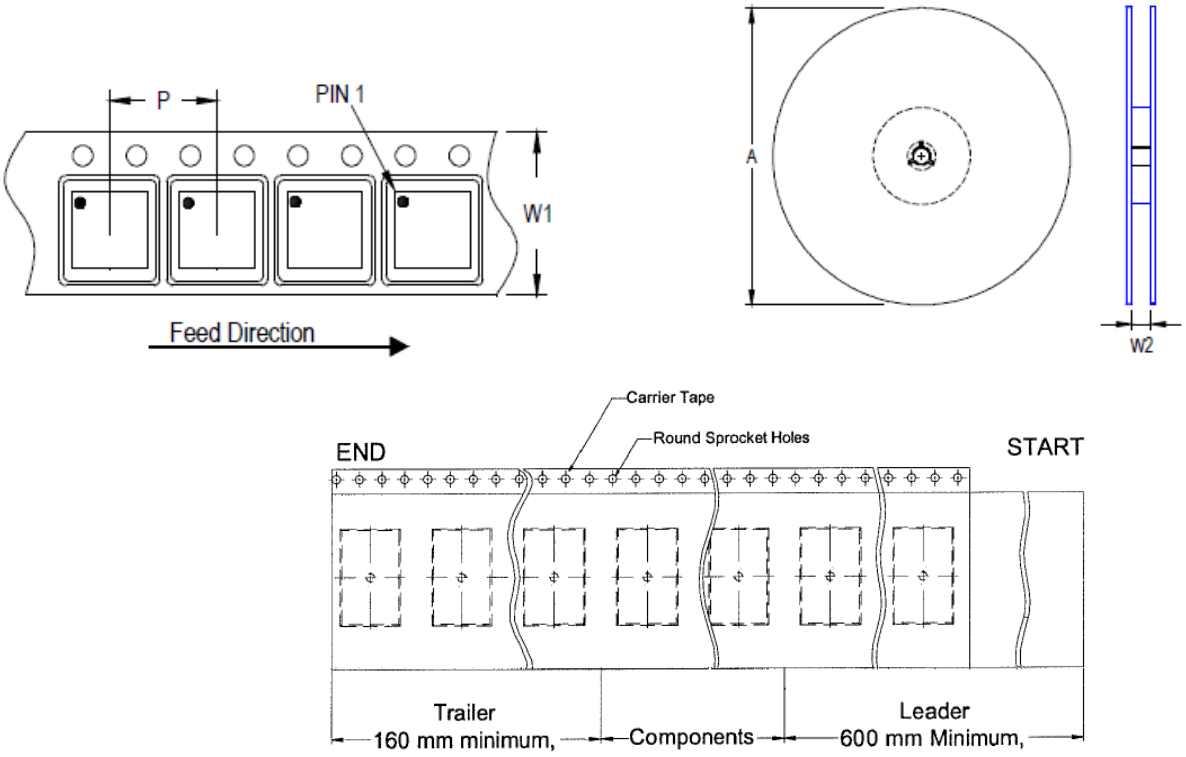


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

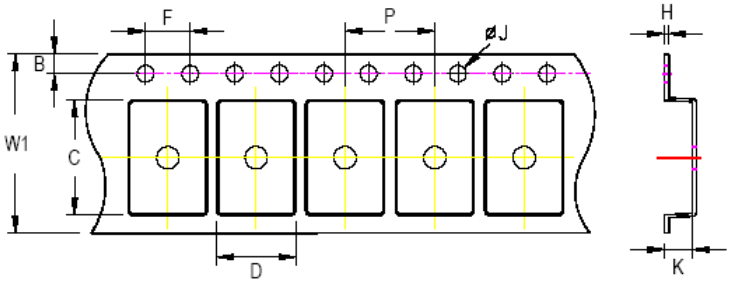
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

18.1.2 Pin 1 at Quadrant 1 for 13”



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	330	13	2,500	160	600	12.4/14.4

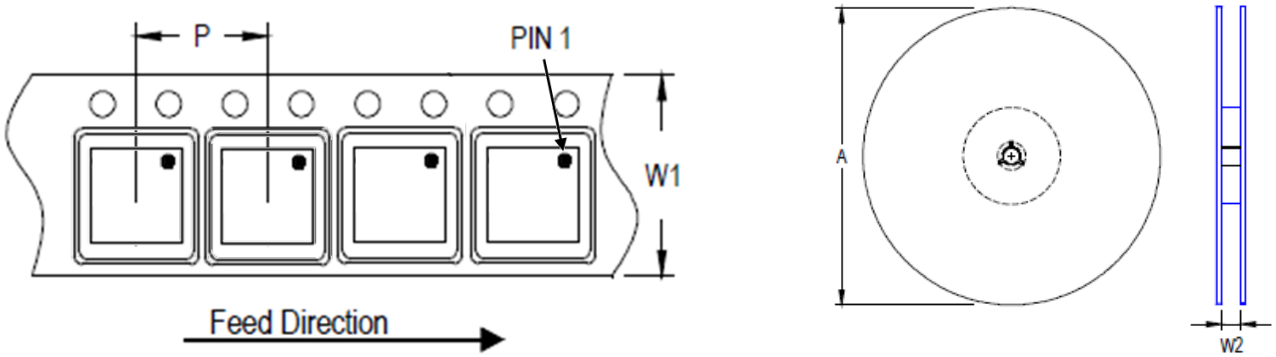


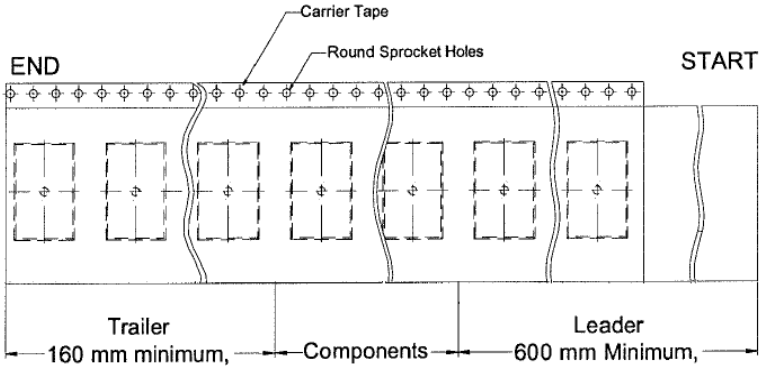
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

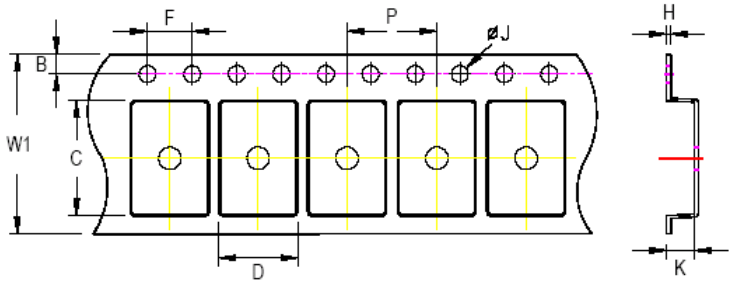
Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

18.1.3 Pin 1 at Quadrant 2 for 7”





Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

18.2 Tape and Reel Packing

18.2.1 Pin 1 at Quadrant 1 for 7”

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

18.2.2 Pin 1 at Quadrant 1 for 13”

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
(V, W) QFN and DFN 3x3	13”	2,500	Box G	1	2,500	Carton A	6	15,000

18.2.3 Pin 1 at Quadrant 2 for 7”

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
04	2024/11/28	Modify	*Changed the names of pin 6 and pin 7 to SW.* *General Description on page 1* -Added Temperature range *Ordering Information on page 1* -Added note *Footprint Information on page 16* -Added footprint information *Packing Information on page 17 to 23* -Added packing information