30W Stereo, Inductor-Less Digital Audio, Closed-Loop System with 192kHz Extended Audio Processing

General Description

The RT9121 is a high efficiency, I^2S-input, stereo channel audio power amplifier delivering 2x30W into 8Ω BTL speaker loads. It can deliver over 94% power efficiency and eliminate the need for heat-sink.

Built-in protection circuits can provide over-temperature, overcurrent, overvoltage, DC and undervoltage protections and report error status.

The RT9121 is an I^2S device receiving all clocks from external sources. It can support both master and slave mode with wide input sampling rate from 8kHz to 192kHz. A fully programmable data path routes these channels to the internal speaker drivers.

The RT9121 features three band DRC and flexible multi-band biquads for anti-clipping, power limiting, and speaker equalization.

Ordering Information

RT9121 □□

- Package Type
  QV: VQFN-48L 6x6 (V-Type)
- Lead Plating System
  G: Green (Halogen Free and Pb Free)

Note:

Richtek products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

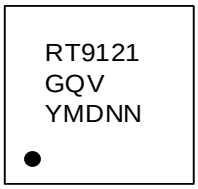
Features

- **Flexible Power Supply Range**
  - **PVDD from 4.5V to 26.4V**
  - **DVDD and I/O, 1.8V or 3.3V**
- **Support Wide Range Audio Format**
  - **Bit Resolution Up to 32 Bits**
  - **Support TDM Up to 32 Bit**
  - **Sampling Frequency from 8kHz to 192kHz**
- **Excellent Audio Performance**
  - **2x30W at into 8Ω BTL at 24V**
  - **SNR ≥ 110dB**
  - **Efficiency ≥ 94%**
- **Built-in Programmable DSP Function**
  - **40 Programmable Biquads for Speaker Equalization**
  - **Programmable Coefficients for DRC Filters and Supporting Multi-Compression Ratios**
  - **Programmable 256-taps FIR**
- **Excellent Self-Protection**
  - **UVLO, OVP, OCP, thermal foldback, OTP and DCP**
  - **Built-In DC Blocking Filters**
- **Filter-Less Application**
- **Hifi-3 DSP Process, 160kB SRAM**
- **Adjustable PWM frequency up to 1.5MHz**
- **VQFN-48L Thermally-Enhanced Package**
- **RoHS Compliant and Halogen Free**

Applications

- LCD-TV
- Monitors
- Home Audio
- Amusement Equipment
- Electronic Music Equipment

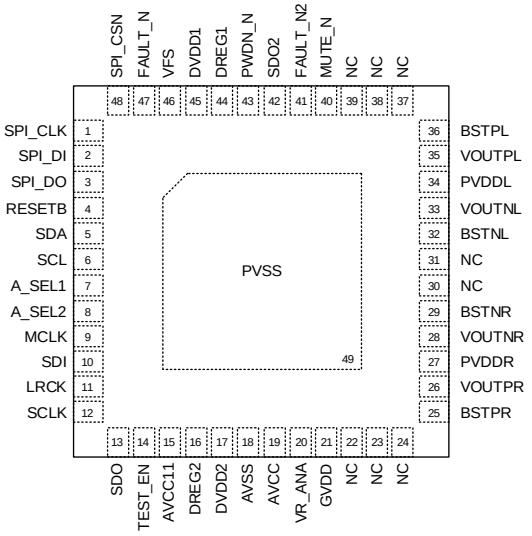
Marking Information



RT9121GQV: Product Code
YMDNN: Date Code

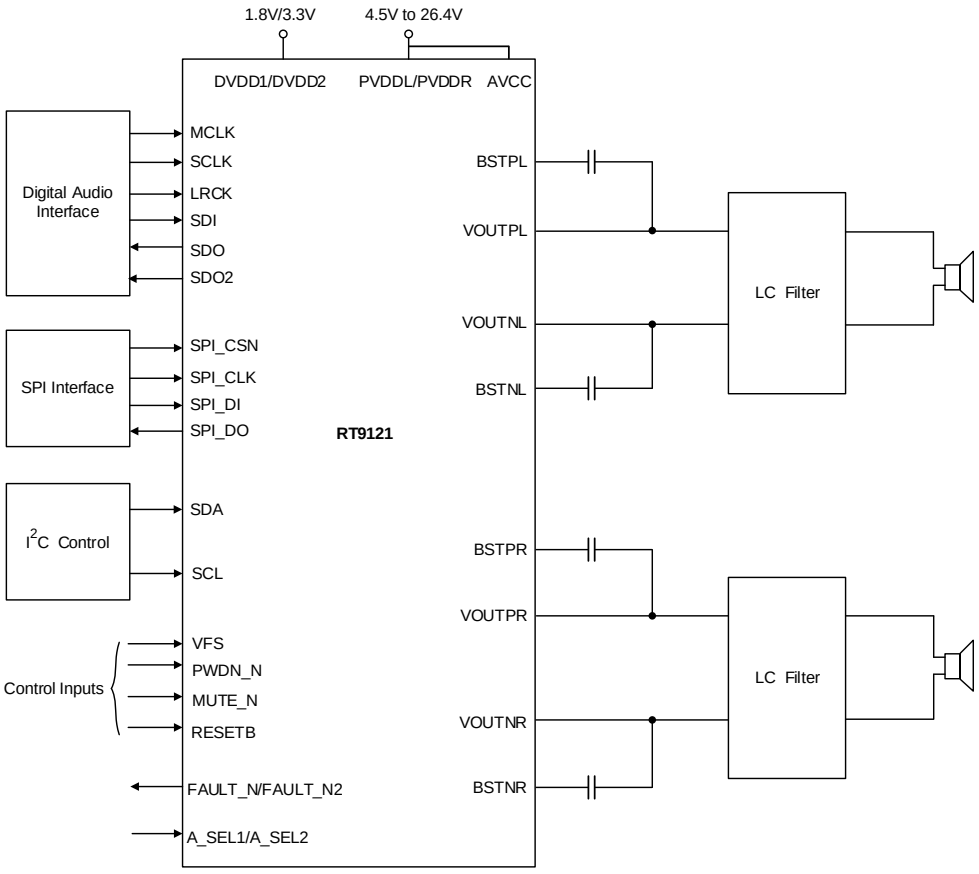
Pin Configuration

(TOP VIEW)



VQFN-48L 6x6

Simplified Application Circuit

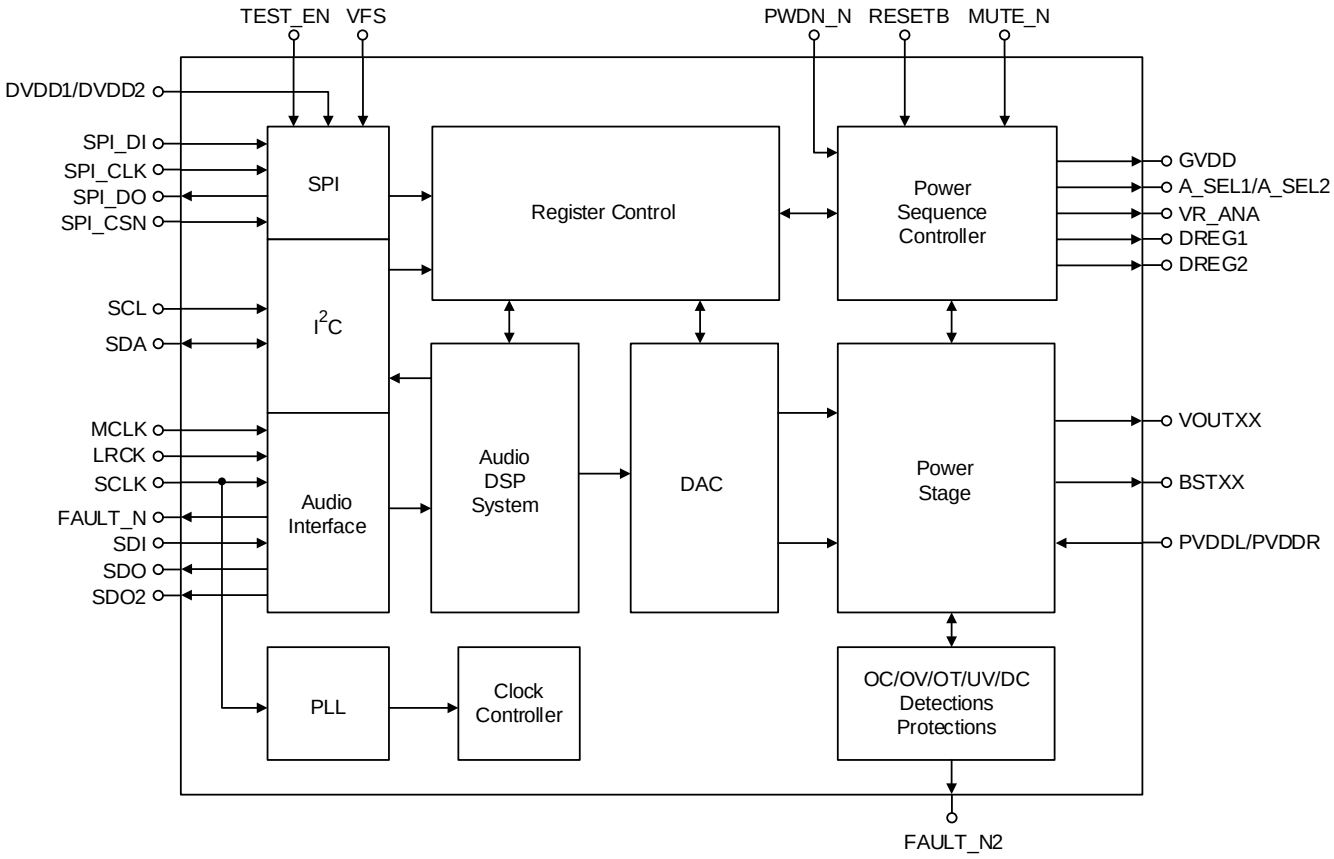


Functional Pin Description

Pin No.	Pin Name	IO	Pin Function
1	SPI_CLK	DI	SPI interface clock. Max is 12MHz. Tied to GND if no use.
2	SPI_DI	DI	SPI interface data input. Tied to GND if no use.
3	SPI_DO	DO	SPI interface data output. Floating if no use.
4	RESETB	DI	RESET for DSP, low active.
5	SDA	DIO	I^2C data input/output.
6	SCL	DI	I^2C clock input.
7	A_SEL1	DI	Slave address selection 1.
8	A_SEL2	DI	Slave address selection 2.
9	MCLK	DI	Master clock input.
10	SDI	DI	I^2S data input.
11	LRCK	DI	I^2S L/R clock input.
12	SCLK	DI	I^2S bit clock input.
13	SDO	DO	I^2S data output for DSP.
14	TEST_EN	DI	Test mode enable, tie to GND for normal operation.
15	AVCC11	P	Analog 1.1V power, connect to DREG1, typical current is about 2mA, maximum is about 5mA.
16	DREG2	P	1.8V LDO output, typical current is about 13mA, maximum current is about 20mA. Please connect external power supply to DVDD1, DVDD2 and VREG2 if I/O voltage is 1.8V.
17	DVDD2	P	1.8V or 3.3V power supply for I/O. Connect to DVDD1.
18	AVSS	P	Ground for analog circuits.
19	AVCC	P	26.4V power supply for analog circuits.
20	VR_ANA	P	Analog reference voltage. Typical current is about 11.6mA, maximum current is about 12mA.
21	GVDD	P	Internal power supply generated by LDO. Typical current is about 4.2mA, maximum current is about 5mA.
22, 23, 24, 30, 31, 37, 38, 39	NC	P	No internal connection. Tied to GND.
25	BSTPR	P	Bootstrap supply for VOUTPR.
26	VOUTPR	AO	Positive output of RCH.
27	PVDDR	P	26.4V power supply for RCH.
28	VOUTNR	AO	Negative output of RCH.
29	BSTNR	P	Bootstrap supply of VOUTNR.
32	BSTNL	P	Bootstrap supply of VOUTNL.
33	VOUTNL	AO	Negative output of LCH.
34	PVDDL	P	26.4V power supply for LCH.
35	VOUTPL	AO	Positive output of LCH.
36	BSTPL	P	Bootstrap supply for VOUTPL.
40	MUTE_N	DI	Mute pin, low active.

Pin No.	Pin Name	IO	Pin Function
41	FAULT_N2	DO	Fault indication for AMP portion. It is open drain design.
42	SDO2	DO	I^2S data output for AMP portion.
43	PWDN_N	DI	RESET for the AMP portion, low active.
44	DREG1	P	1.1V LDO output. Typical current is about 100mA, maximum is about 100mA.
45	DVDD1	P	1.8V or 3.3V power supply for DSP portion and I/O. Connect to DVDD2
46	VFS	P	E-fuse program pin. 0V for read only, 3.3V for program. Minimum current consumption for the VFS is 20mA.
47	FAULT_N	DO	Fault indication for DSP portion. It is open drain design.
48	SPI_CSN	DI	SPI interface Chip select. Tied to DVDD1 or DVDD2 if no use.
49 (Exposed Pad)	PVSS	P	Ground.

Functional Block Diagram



Operation

Error Reporting

The FAULT_N, and FAULT_N2 pin is for report error status. The FAULT_N, and FAULT_N2 go to low when protection happen. This pin is open-drain configuration, need pull-up resistor.

Clock Detection

The RT9121 can accept SCLK to be as 32fs, 48fs and 64fs and support only a 1xfs LRCK. The internal oscillator will check SCLK input constantly. If clock is lost, the RT9121 will shut down the power stage automatically.

Overvoltage Protection

The RT9121 monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin rise behind the overvoltage threshold, 30V, the OVP circuit turns off the output immediately and operates in auto-recovery mode, or the latch mode can configured to use.

Volume Control

The RT9121 have master volume MS_VOL and each channel volume CH1_VOL, CH2_VOL control. The step of each volume is 0.0625dB per step, from 24dB to mute. CH1 and CH2 also have each mute control, CH1_MUTE and CH2_MUTE.

Built-In Anti-POP Function

An internal soft-start function controls the duty ramp-up rate of the output PWM voltage to minimize the POP noise during start-up. Similarly, when power shut-down, the duty also ramp-down to eliminate the POP noise. This function also acts when the PWDN_N pin turns-ON/OFF.

Overcurrent Protection

The RT9121 provides OCP function to prevent the device from damages during overload or short-circuit conditions.

The current function is detected by an internal sensing circuit. Once when the inductor short to the each other and to GND the OCP function is design to operate the latch mode.

Undervoltage Protection

The RT9121 monitors the voltage on PVDD voltage threshold. When the voltage on PVDDL/R pin falls below the undervoltage threshold, 4V (Which can be programmable.), the UVP circuit turns off the output immediately, or the latch mode can configure to use.

Over-Temperature Protection

The over-temperature protection function will turn off the power MOSFET when the junction temperature exceeds 150°C (minimum). Once the junction temperature cools down by approximately 30°C, the regulator will automatically resume operation, or the latch mode can configure to use.

Dynamic Range Enhancement

The dynamic range enhancement which enhance the dynamic range for the application. It will optimize the noise when the operating.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, AVCC, PVDDL, PVDDR ---------- –0.3V to 32V
- Supply Voltage, DVDD2 ---------- –0.3V to 9V
- Supply Voltage, DVDD1 ---------- –0.3V to 4.6V
- GND (NC Pin) to PVSS and AVSS ---------- –0.3V to 0.3V
- Speaker Amplifier Output Voltage, VOUTXX (Note 2) ---------- –0.3V to 32V
- BSTXX ---------- –0.3V to 36V
- SCL, SDA, SPI_XX, FAULT_N ---------- –0.5 to 5.8V
- A_SEL1, A_SEL2, TEST_EN, MCLK, LRCK, SCLK, SDI, SDO2, RESETB ---------- –0.5 to 4.6V
- MUTE_N, PWDN_N ---------- –0.3V to DVDD + 0.5V
- VOUTPR, VOUTNR, VOUTPL, VOUTNL (AC Peak Limit) (Note 3) ---------- –10V to 37V
- SDO ---------- –0.3V to 9V
- DREG2 ---------- –0.5V to 4V
- VFS ---------- –0.3V to 4.6V
- AVCC11, DREG1 ---------- –0.5V to 1.5V
- VR_ANA, GVDD, FAULT_N2 ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C

  VQFN-48L 6x6 ---------- 5.6W
- Package Thermal Resistance (Note 4)

  VQFN-48L 6x6, θ_{JA} ---------- 22.3°C/W

  VQFN-48L 6x6, $\theta_{JC(TOP)}$ ---------- 1.1°C/W

  VQFN-48L 6x6, $\theta_{JC(BOTTOM)}$ ---------- 2.2°C/W
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 6)

- Supply Input Voltage, DVDD1 DVDD2 ---------- 3V to 3.6V
- Supply Input Voltage (For 1.8V I/O), DVDD1, DVDD2, DREG2 (Note 7) ---------- 1.62V to 1.98V
- Supply Input Voltage, PVDDL, PVDDR, AVCC ---------- 4.5V to 26.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 150°C

Electrical Characteristics

(PVDDL = PVDDR = AVCC = 12V, DVDD = 3.3V, R_L = 8Ω, T_A = 25°C, fsw = 384kHz, L = 10μH, C = 0.47μF, unless otherwise specified.) (Note 8)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
PWDN_N, RESETB	VIH: High-Level-Input Voltage	V_{IH}			DVDD x 0.7	--	--	V
	VIL: Low-Level-Input Voltage	V_{IL}			--	--	DVDD x 0.3	
FAULT_N, FAULT_N2	VOL: Low-Level-Output Voltage	V_{OL}	I_{PULLUP} = 3mA		--	--	0.4	V
DVDD2 Quiescent Current (Normal Mode)		I_{Q_D}	PWDN_N = 3.3V, for DVDD		--	7.5	15	mA
DVDD1 Quiescent Current		I_{Q_D1}	PWDN_N = 3.3V for DSP DVDD, no load, no LC filter		--	30	--	mA
DVDD2 Shutdown Current		I_{SD_D2}	PWDN_N = 0.8V, no load, no LC filter		--	5	--	μA
DVDD1 Shutdown Current		I_{SD_DSP}	PWDN_N = 0.8V, no load, no LC filter		--	10	--	μA
PVDDL/R+AVCC Quiescent Current (Normal Mode)		I_{Q_P}	PWDN_N = 3.3V, switch 50% duty, no load, no LC filter		--	20	25	mA
PVDDL/R+AVCC Shutdown Current		I_{SD_P}	PWDN_N = 0.8V, no load, no LC filter		--	--	20	μA
Sleep Mode		Idvdd2+ dvdd1	When entering sleep mode		--	1	--	mA
Drain-Source On-State Resistance		$R_{DS(ON)}$	PVDD = 12V, I_O = 500mA, T_J = 25°C	High-Side	--	95	--	mΩ
				Low-Side	--	85	--	
AMP Gain variation		$\Delta A_{V(SPK\_AMP)}$	AMP to AMP gain difference		–0.5	--	0.5	dB
Speaker Gain variation		$\Delta A_{V(L/R\ Ch)}$	L/R Channel gain difference		--	--	0.4	dB
Startup Time from Shutdown		t_{ON}			--	250	--	ms
Shutdown Time from Enable (Note 9)		t_{OFF}			--	60	--	ms
PWM Switching Frequency			384kHz mode		--	384	--	kHz
			768kHz mode		--	768	--	
			1536kHz mode		--	1536	--	
RMS Output Power BD Modulation		P_O	THD + N = 10%, (BTL), PVDD = 12V, R_L = 8Ω		9	10	--	W
			THD + N = 1%, (BTL), PVDD = 24V, R_L = 8Ω		28	30	--	
Total Harmonic Distortion + Noise		THD+N	P_O =1W (BTL)		--	0.03	--	%
Output Integrated Noise		Vn	20Hz to 20kHz, A-weighted		--	35	--	μV
Output Offset Voltage		V_{OS}	PVDD = 12V		–5	--	5	mV
			PVDD = 24V		–5	--	5	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cross-Talk	X_{TALK}	Output power = 1W, 1kHz with none shielding choke	--	-75	--	dB
		Output power = 1W, 1kHz with shielding choke	--	-100	--	
Signal-to-Noise Ratio	SNR	PVDD = 24V, 1% THD + N	--	110	--	dB
Power Supply Rejection Ratio	PSRR	Frequency @1kHz with 200mVpp ripple	--	–80	--	dB
Dynamic Range	DR	Input level –60dBFS	--	105	--	dB
Efficiency	η	PVDD = 12V, output power = 10W + 10W, Load = 8Ω	--	94	--	%
Over-Temperature Protection	OTP	Guaranteed by design	150	160	175	°C
Thermal Hysteresis			--	30	--	°C
Overcurrent Protection	OCP		6	7	8.8	A
PVDDL/PVDDR Overvoltage	OVP		--	30	--	V
PVDDL/PVDDR Undervoltage	UVP	Amp address 0x06C bit [2:0] = 0'b000	--	4	--	V
I^2C Interface Electrical Characteristics						
High-Level Input Voltage (Belongs to the internal 1.8V domain)	V_{IH}		DVDD x 0.7	--	--	V
Low-Level Input Voltage (Belongs to the internal 1.8V domain)	V_{IL}		--	--	DVDD x 0.3	V
Digital Output Low (SDA)	V_{OL}	I_{PULLUP} = 3mA	--	--	0.4	V
Clock Operating Frequency	f_{SCL}		--	--	400	kHz
Bus Free Time Between Stop and Start Condition	t_{BUF}		1.3	--	--	µs
Hold Time After (Repeated) Start Condition	$t_{HD,STA}$		0.6	--	--	µs
Repeated Start Condition Setup Time	$t_{SU,STA}$		0.6	--	--	µs
Stop Condition Time	t_{SU_STO}		0.6	--	--	µs
Input Data Hold Time	$t_{HD,DAT}$ (IN)		0	--	900	ns
Data Setup Time	$t_{SU,DAT}$		100	--	--	ns
Clock Low Period	t_{LOW}		1.3	--	--	µs
Clock High Period	t_{HIGH}		0.6	--	--	µs
Clock Data Fall Time	tf		20	--	300	ns
Clock Data Rise Time	tr		20	--	300	ns
Spike Suppression Time	t_{SP}		--	--	20	ns
Slave Mode I^2S Interface Electrical Characteristics						
High-Level Input Voltage	V_{IH}		DVDD x 0.7	--	--	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Low-Level Input Voltage		V_{IL}		--	--	DVDD x 0.3	V
SDO	VOH: High-Level Output Voltage	V_{OH}	--	--	3.3	--	V
	VOL: Low-Level Output Voltage	V_{OL}		--	--	0.4	
High-Level Input Voltage		V_{IH}	DVDD = 1.8V	1.4	--	--	V
Low-Level Input Voltage		V_{IL}	DVDD = 1.8V	--	--	0.5	V
SDO	VOH: High-Level Output Voltage	V_{OH}	DVDD = 1.8V	--	1.8	--	V
	VOL: Low-Level Output Voltage	V_{OL}	DVDD = 1.8V	--	--	0.2	V
Frequency		f_{SCLKIN}		1.024	--	12.288	MHz
Setup Time, LRCK to SCLK Rising Edge		t_{su1}		10	--	--	ns
Hold Time, LRCK from SCLK Rising Edge		t_{h1}		10	--	--	ns
Setup Time, SDI to SCLK Rising Edge		t_{su2}		10	--	--	ns
Hold Time, SDI from SCLK Rising Edge		t_{h2}		10	--	--	ns
Rise/Fall Time for SCLK/LRCK		trs/tfs		--	--	--	ns
I^2S Duty Cycle		%		40	--	60	%

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. The result is defined when the cross voltage between BST and VOUT is 5V.

Note 3. The switching terminal should be used within AC peak limits. Overshoot and undershoot must be less than 100ns.

Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four-layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is measured at the case top of the package. The result is including the bonding, GND, and real Die.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

Note 6. The device is not guaranteed to function outside its operating conditions.

Note 7. In 1.8 V I/O application, 1.8 V is needed to be supplied from an external voltage source to DVDD1, DVDD2 and VREG2.

Note 8. Measurements were made using the RT9121_EVM board and Audio Precision System 2722 with AUX-0025 low-pass filter.

Note 9. Enable is the state that AMP IC outputs PWM.

Timing Diagram

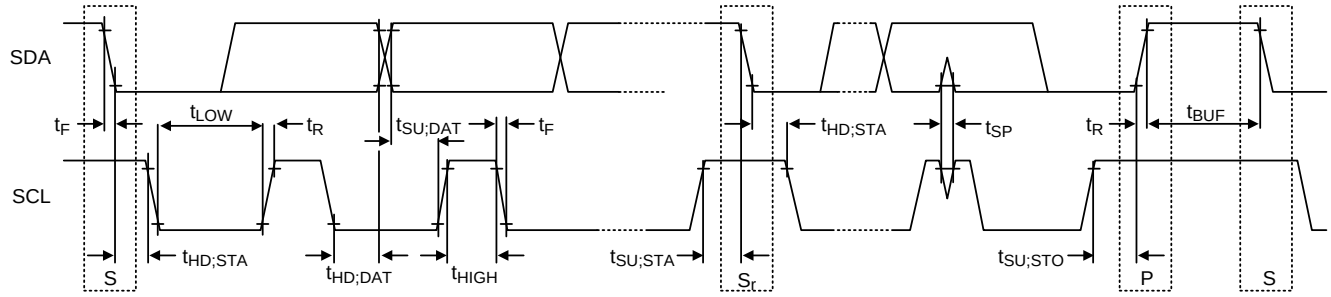


Figure 1. I2C Interface Timing Diagram

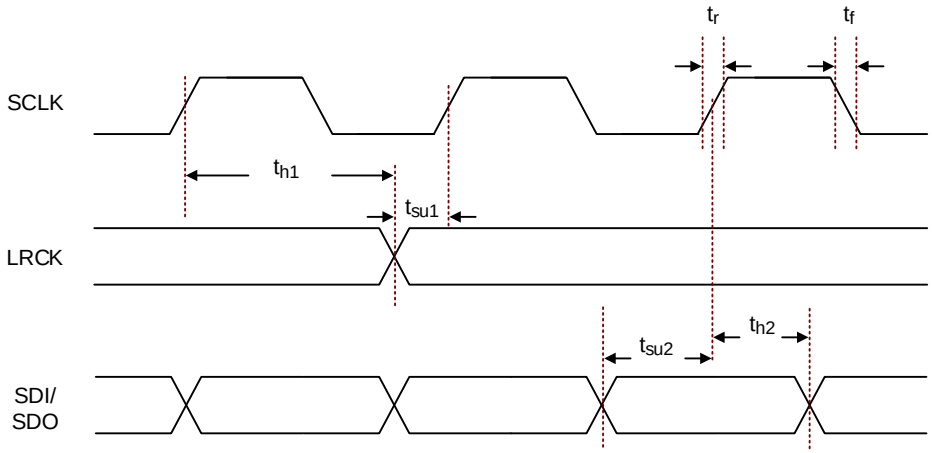
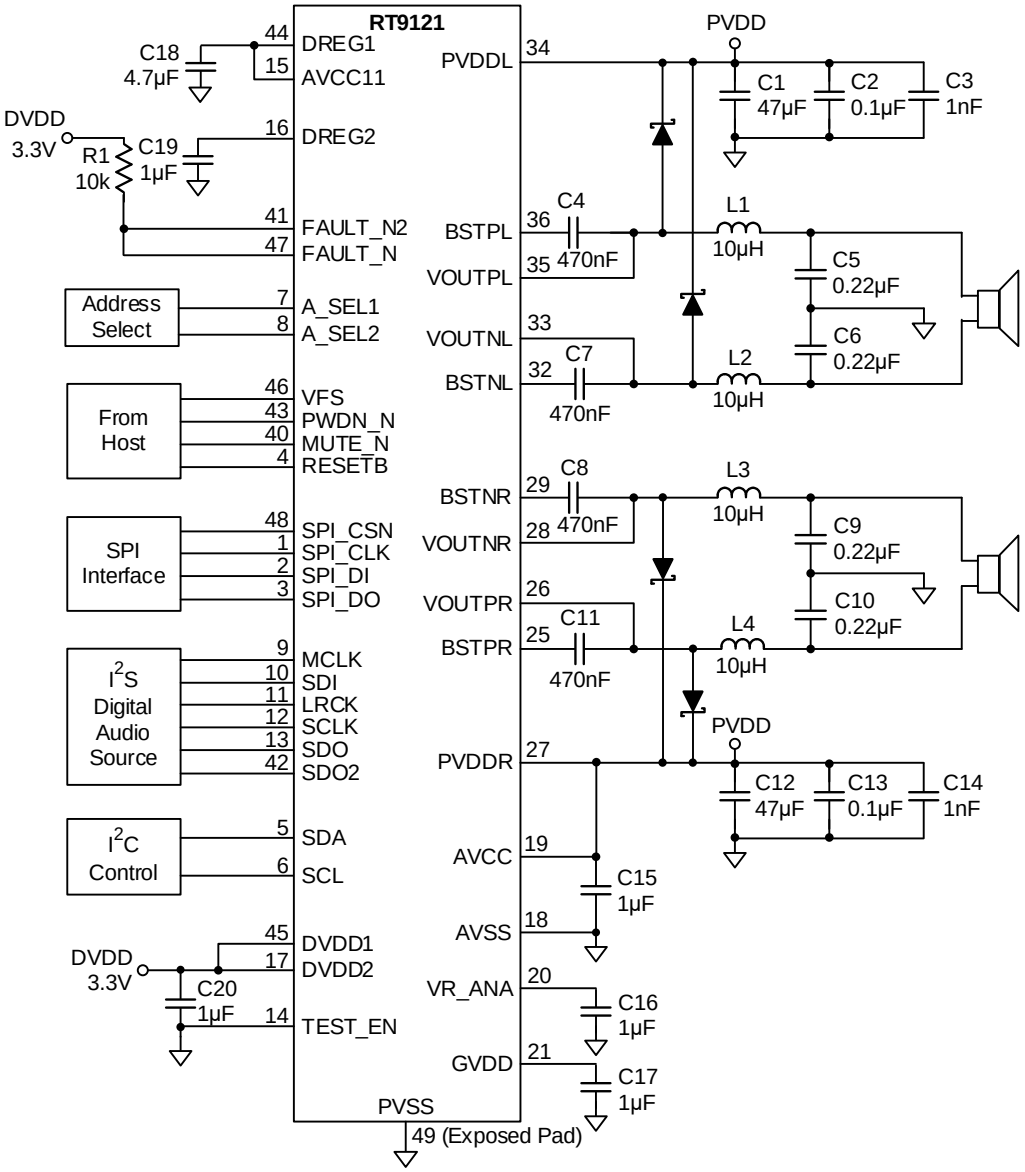


Figure 2. Timing Diagram of Slave Mode I2S Interface

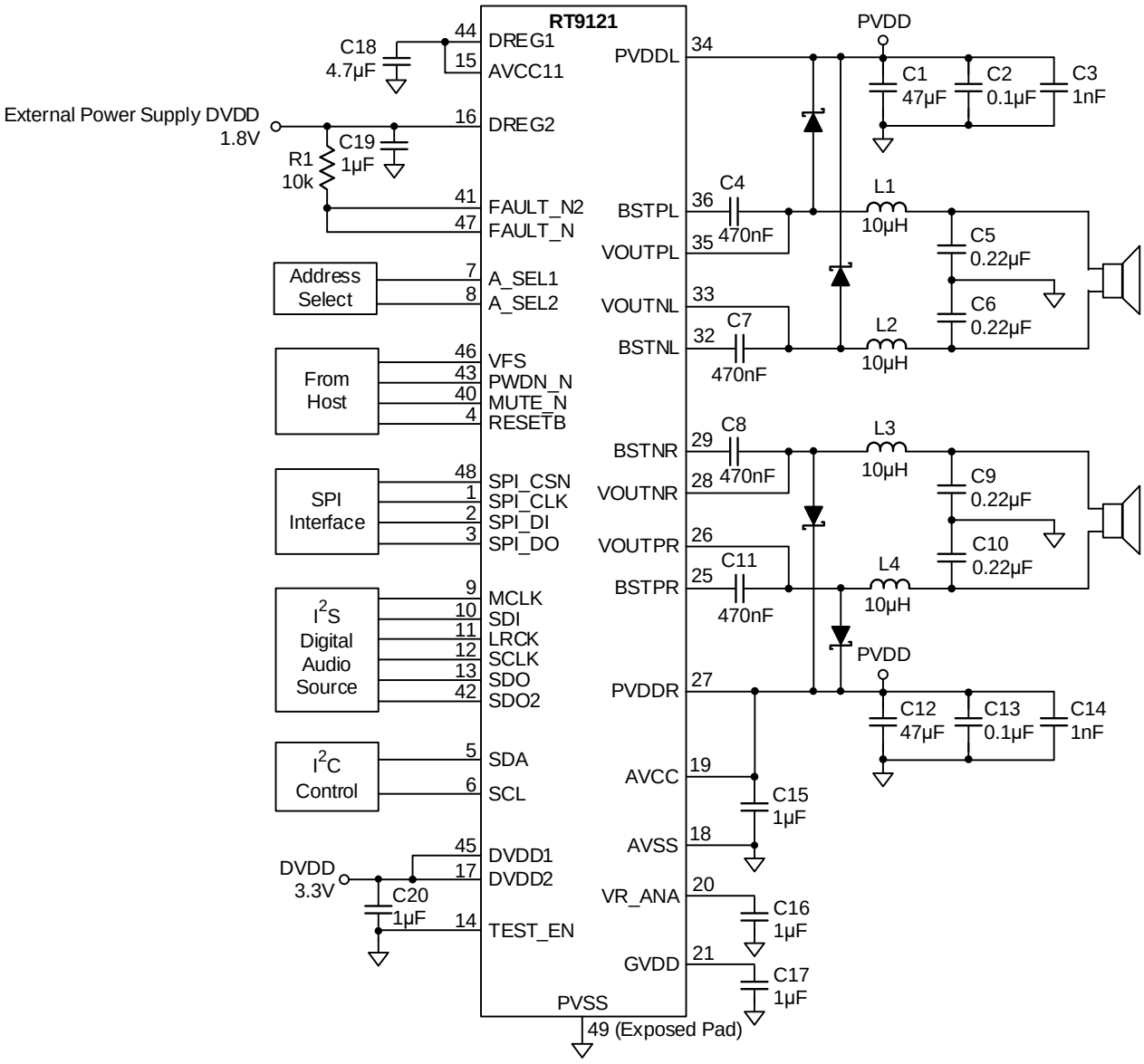
Typical Application Circuit

3.3V I/O Application (BTL)



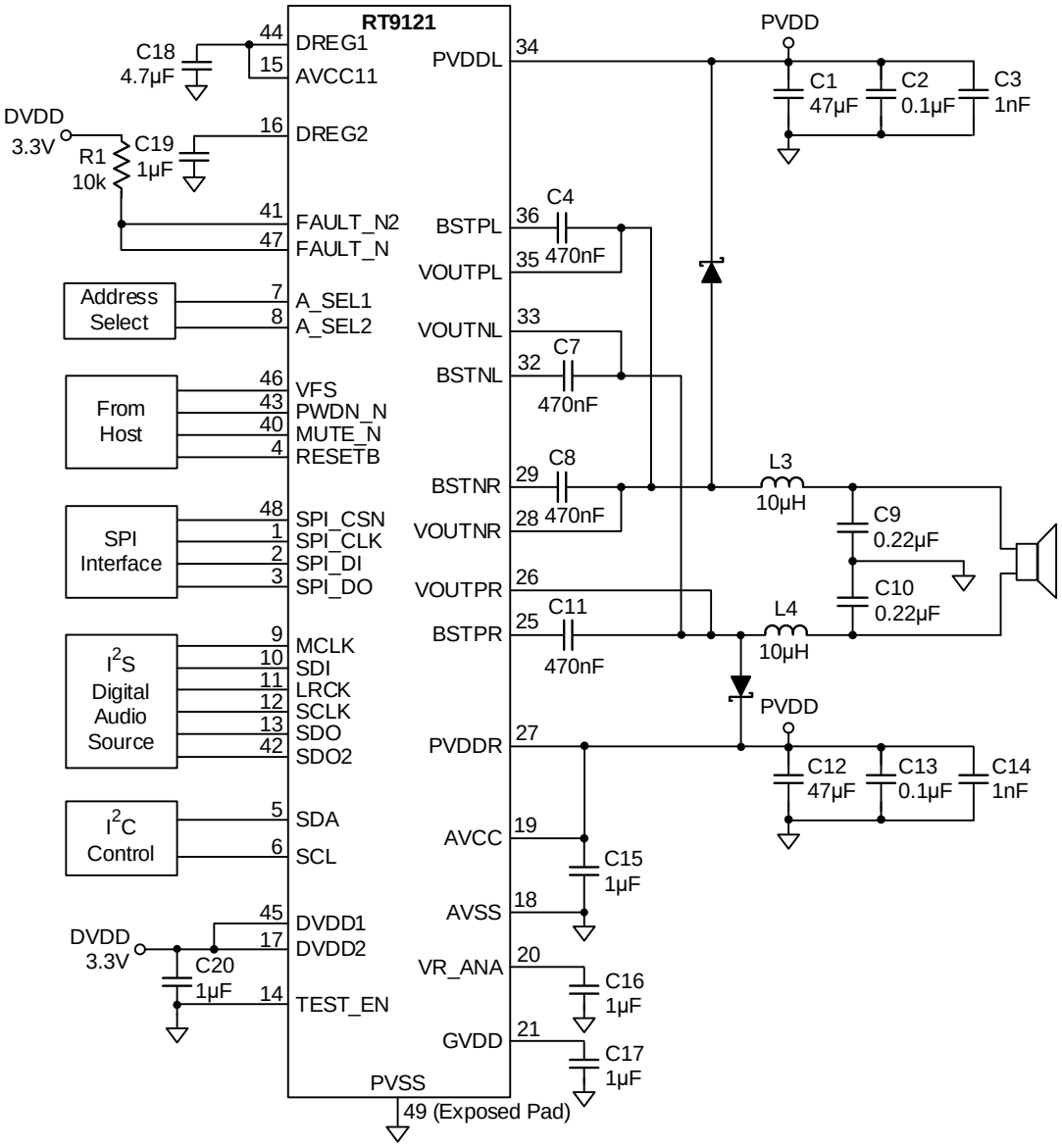
Note: Diode is optional, please refer to Page 71.

1.8V I/O Application (BTL)



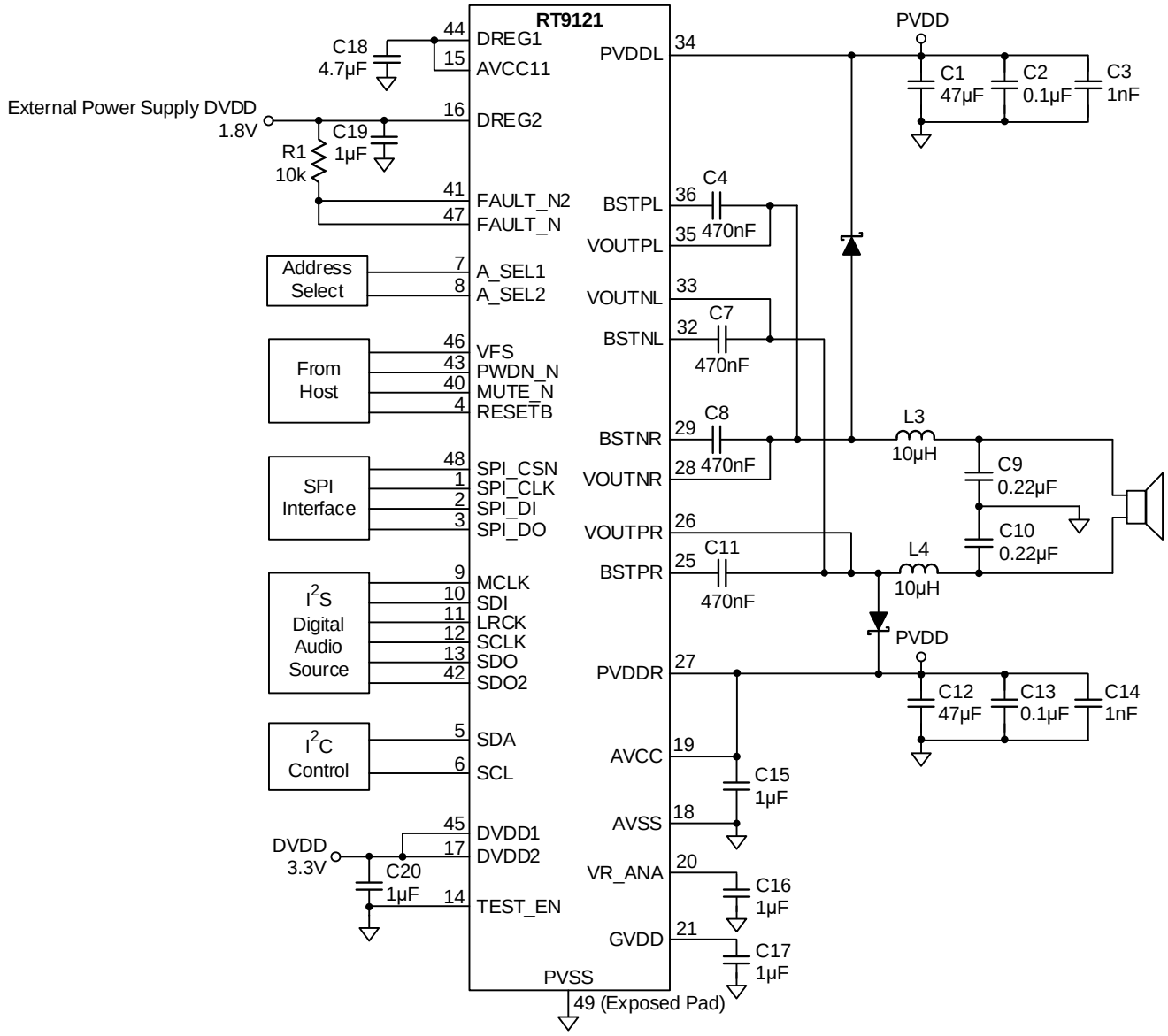
Note: Diode is optional, please refer to Page 71.

3.3V I/O Application (PBTL)



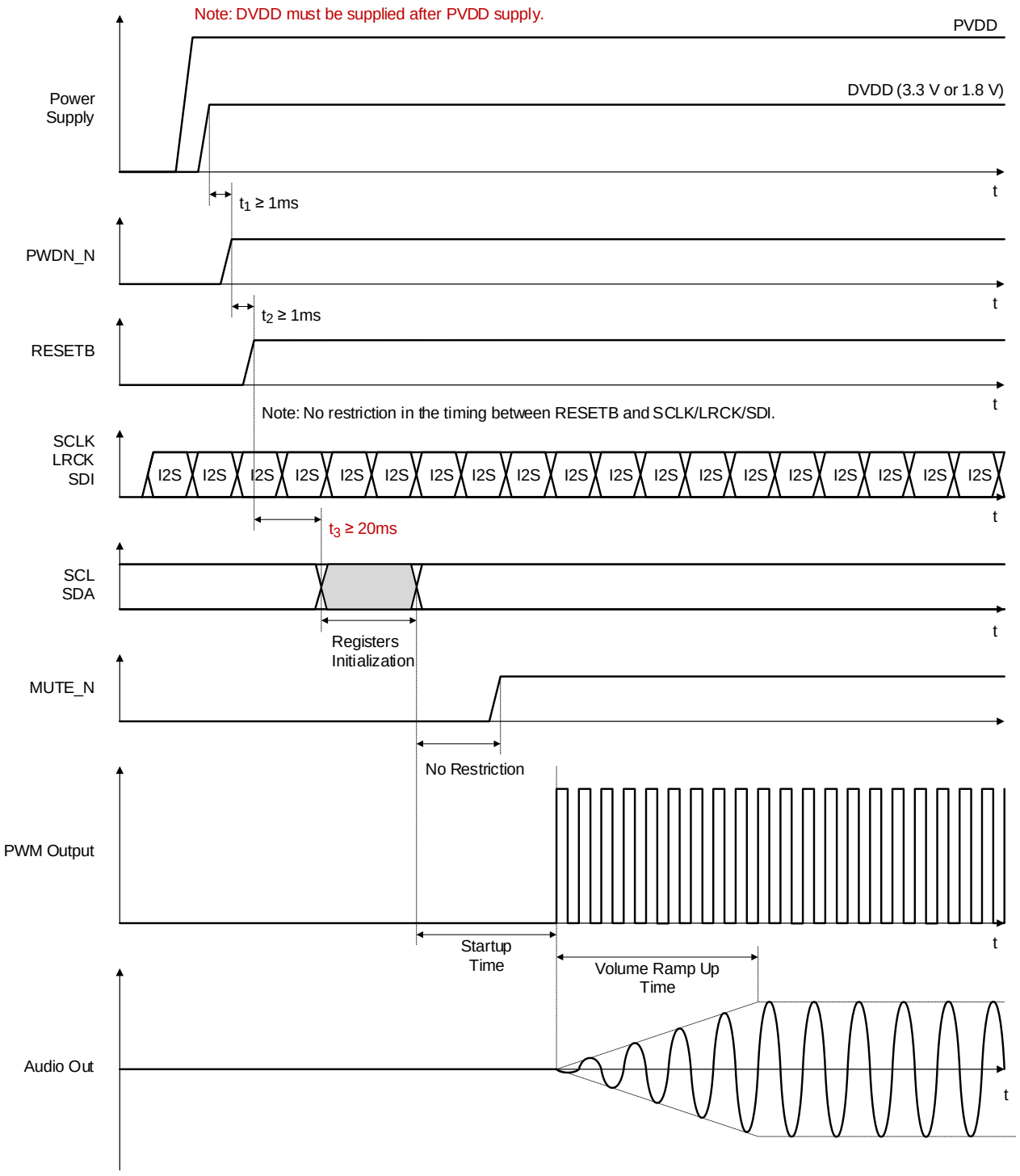
Note: Diode is optional, please refer to Page 71.

1.8V I/O Application (PBTL)

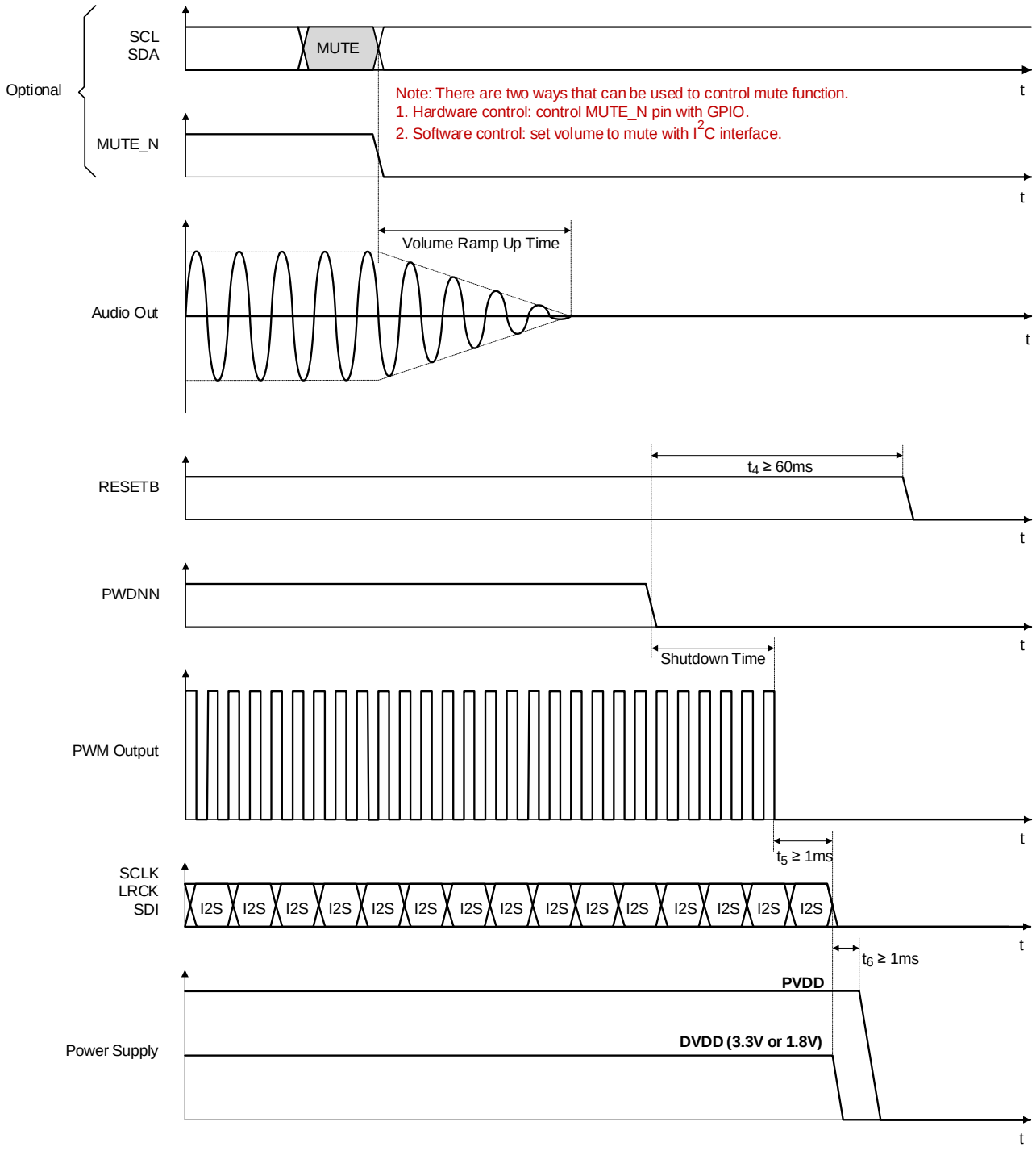


Note: Diode is optional, please refer to Page 71.

Turn-On Timing Diagram



Turn-Off Timing Diagram



Initial Sequence (BTL Mode)

Step1	**Sequence**	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF01	1	0x01	To run ROM
Step2	**Set AMP SW RESET**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x40	DSP set AMP SW RESET address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x80	DSP set AMP SW RESET setting
	5	0xFF43	1	0x02	DSP set AMP to write
	Delay 20ms				
Step3	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x63	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0xDE	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step4	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x65	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x66	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step5	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x15	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x20	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write

Step6	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x6E	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x19	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step7	**Set AMP Skip Volume Ramp**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x0A	DSP set AMP skip volume ramp address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x09	DSP set AMP skip volume ramp setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step8	**Set AMP Volume to 0dB**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x20	DSP set AMP volume address
	3	0xFF41	1	0x02	DSP set AMP data length
	4	0xFF42	1	0x01, 0x80	DSP set AMP volume setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step9	**Set AMP SPK Gain**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x07	DSP set AMP SPK Gain address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x37	DSP set AMP SPK Gain setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step10	**Entering DSP Active Mode**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0x00	4	0x02037800	Entering DSP active mode
Step11	**Set DSP On**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0x00	4	0x06037800	DSP Turn On

Step12	**Set AMP On (For 384kHz)**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x05	DSP set AMP ON address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x80	DSP set AMP on setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step12	**Set AMP On (For 768kHz)**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x05	DSP set AMP ON address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x84	DSP set AMP on setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step12	**Set AMP On (For 1.5MHz)**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x05	DSP set AMP ON address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x8C	DSP set AMP on setting
	5	0xFF43	1	0x02	DSP set AMP to write

Initial Sequence (PBTL Mode)

Step1	**Sequence**	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF01	1	0x01	To run ROM
Step2	**Set AMP SW RESET**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x40	DSP set AMP SW RESET address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x80	DSP set AMP SW RESET setting
	5	0xFF43	1	0x02	DSP set AMP to write
	Delay 20ms				

Step3	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x64	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x39	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step4	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x65	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x11	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step5	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x15	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x60	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step6	**Set AMP Internal Setting**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x6E	DSP set AMP internal setting address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x19	DSP set AMP internal setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step7	**Set AMP Skip Volume Ramp**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x0A	DSP set AMP skip volume ramp address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x09	DSP set AMP skip volume ramp setting
	5	0xFF43	1	0x02	DSP set AMP to write

Step8	**Set AMP Volume to 0dB**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x20	DSP set AMP volume address
	3	0xFF41	1	0x02	DSP set AMP data length
	4	0xFF42	1	0x01, 0x80	DSP set AMP volume setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step9	**Set AMP SPK Gain**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x07	DSP set AMP SPK Gain address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x37	DSP set AMP SPK Gain setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step10	**Set AMP L+R Input Mixer**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x30	DSP set AMP input mixer
	3	0xFF41	1	0x03	DSP set AMP data length
	4	0xFF42	1	0x01, 0xC0, 0x07	DSP set AMP input mixer setting
	5	0xFF43	1	0x02	DSP set AMP to write
	6	0xFF45	1	0x18	DSP set AMP slave address
	7	0xFF40	1	0x31	DSP set AMP input mixer
	8	0xFF41	1	0x03	DSP set AMP data length
	9	0xFF42	1	0x01, 0xC0, 0x07	DSP set AMP Input mixer setting
	10	0xFF43	1	0x02	DSP set AMP to write
Step11	**Entering DSP Active Mode**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0x00	4	0x02037800	Entering DSP active mode
Step12	**Set DSP On**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0x00	4	0x06037800	DSP turn on
Step13	**Set AMP On (For 384kHz)**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x05	DSP set AMP ON address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x90	DSP set AMP on setting
	5	0xFF43	1	0x02	DSP set AMP to write

Step13	**Set AMP On (For 768KHz)**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x05	DSP set AMP ON address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x94	DSP set AMP on setting
	5	0xFF43	1	0x02	DSP set AMP to write
Step13	**Set AMP On (For 1.5MHz)**				
	Sequence	**reg_addr**	**reg_size**	**reg_value**	**Description**
	1	0xFF45	1	0x18	DSP set AMP slave address
	2	0xFF40	1	0x05	DSP set AMP ON address
	3	0xFF41	1	0x01	DSP set AMP data length
	4	0xFF42	1	0x9C	DSP set AMP on setting
	5	0xFF43	1	0x02	DSP set AMP to write

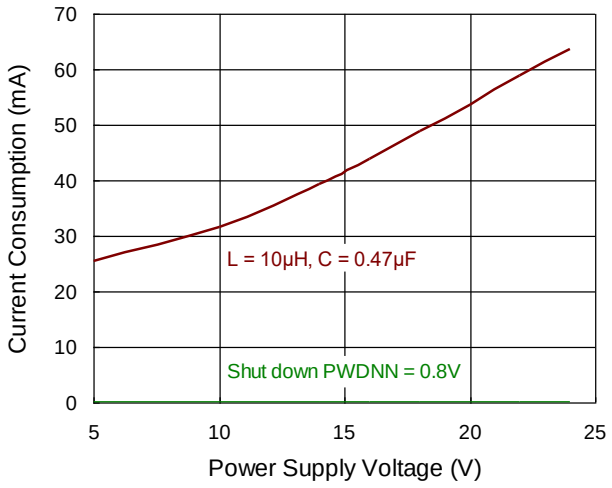
Command to access AMP Prtion

Description
→ Step 1: 0xFF45 set to 0x18 to select AMP address. → Step 2: 0xFF40 set to AMP portion address. Where the address is wanted to set. → Step 3: 0xFF41 set to AMP portion address data length. If set 0x01, is 1 byte, 0x02 is 2 byte. → Step 4: 0xFF42 set to AMP portion setting. → Step 5: 0xFF43 set 0x02 to **write** the setting which above list. → Step 6: 0xFF42 set 0x01 to **read** the setting which above list, if writing 1 byte. → Step 6: 0xFF42 set 0x02 to **read** the setting which above list, if writing 2 byte. For Example: → To Write when need to set 0x20 value to 0x10, 0x80 → Step 1: Write 0xFF45 value to 0x18 **→ Step 2: Write 0xFF40 value to 0x20** → Step 3: Write 0xFF41 value to 0x02 **→ Step 4: Write 0xFF42 value to 0x01, 0x80** → Step 5: Write 0xFF43 value to 0x02. → Step 6: Write 0xFF42 value to 0x02 to read the 0x20 setting. Note: Those 5 command is a set, if need to access AMP portion.

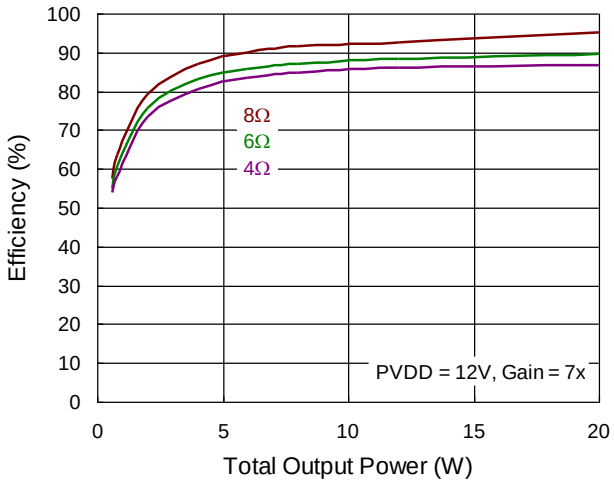
Typical Operating Characteristics

PWM = 384kHz

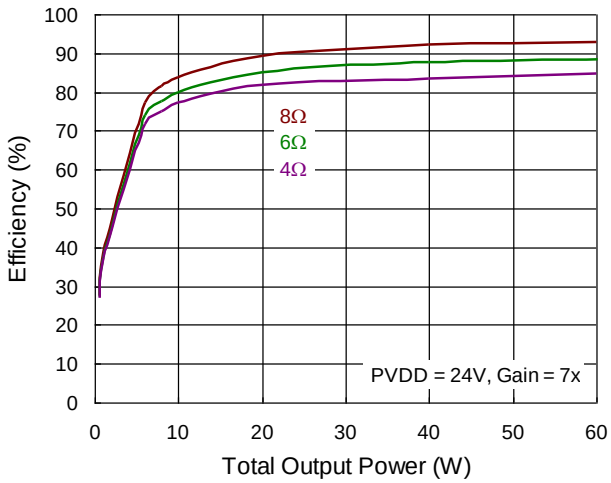
Current Consumption vs. Power Supply Voltage



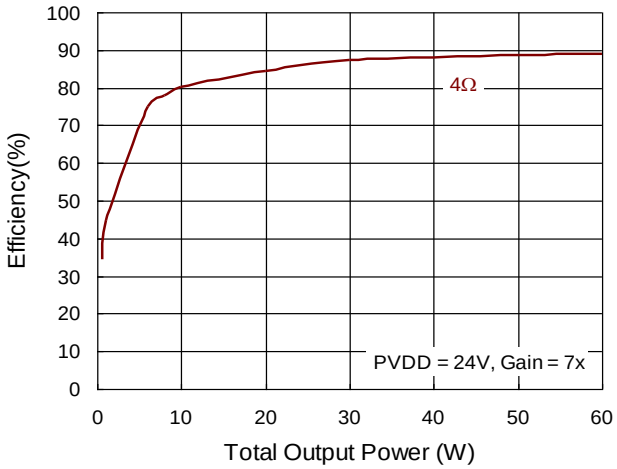
Efficiency vs. Total Output Power (BTL)



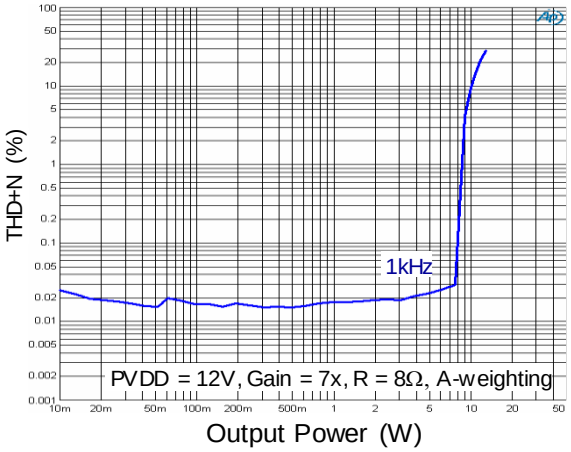
Efficiency vs. Total Output Power (BTL)



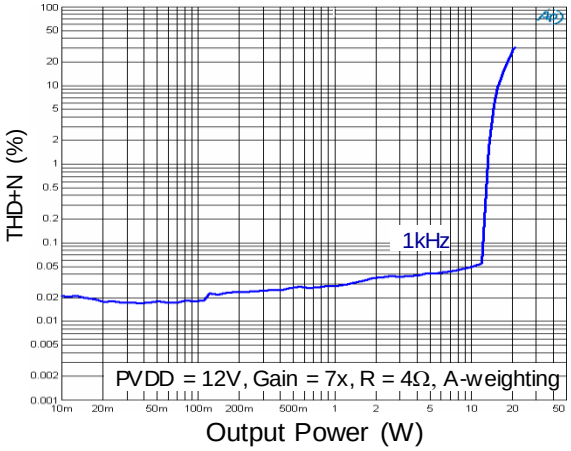
Efficiency vs. Total Output Power (PBTL)



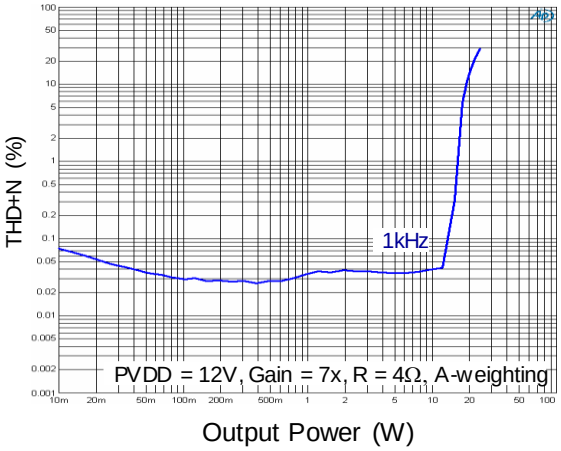
THD + N vs. Output Power (BTL)



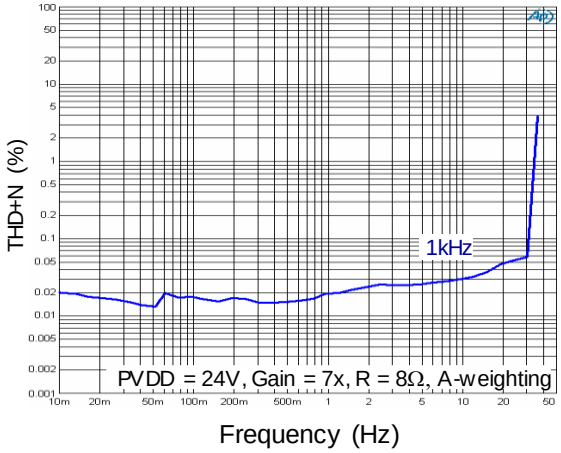
THD + N vs. Output Power (BTL)



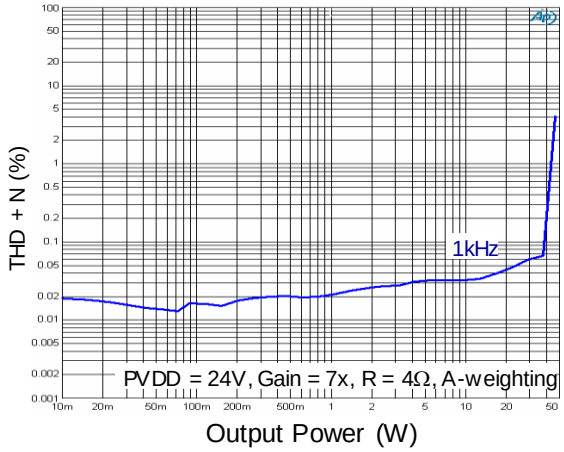
THD + N vs. Output Power (PBTL)



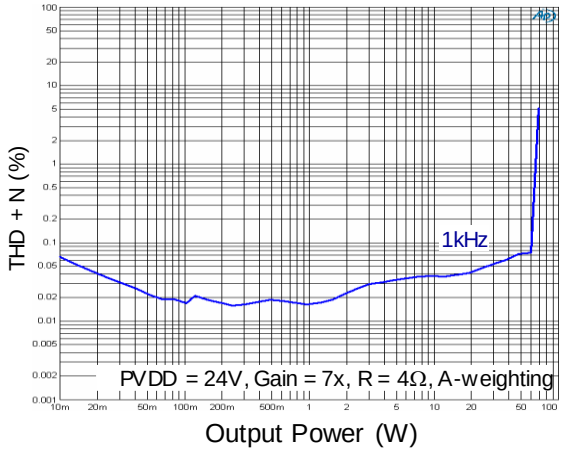
THD + N vs. Output Power (BTL)



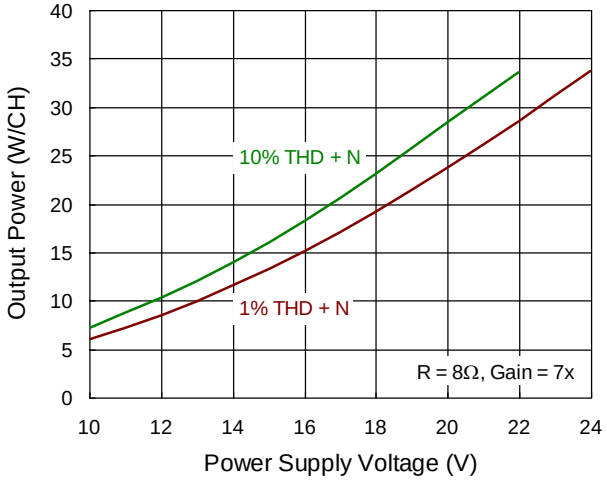
THD + N vs. Output Power (BTL)



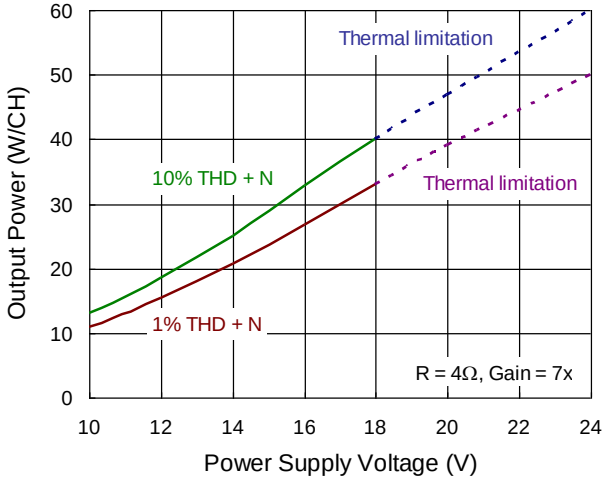
THD + N vs. Output Power (PBTL)



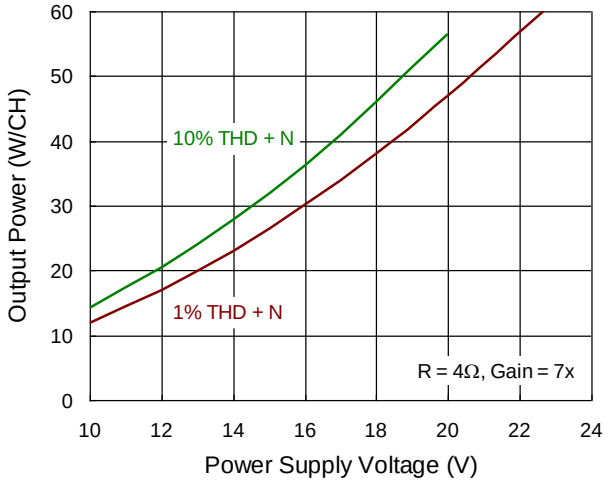
Output Power vs. Power Supply Voltage (BTL)



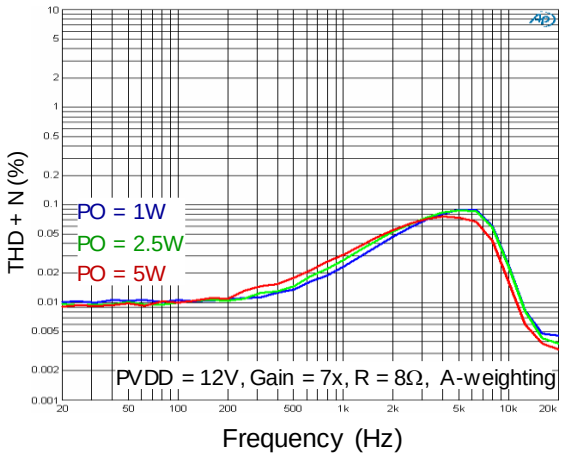
Output Power vs. Power Supply Voltage (BTL)



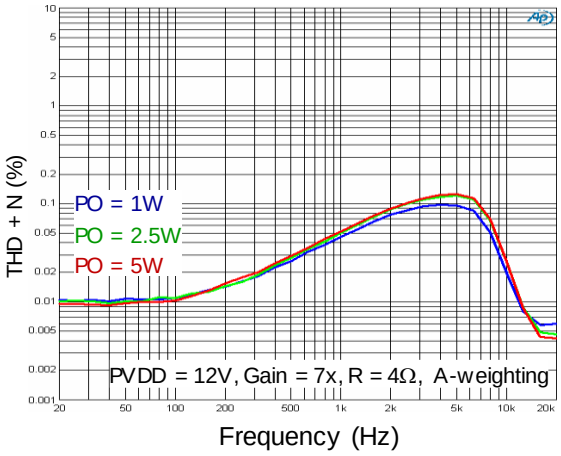
Output Power vs. Power Supply Voltage (PBTL)



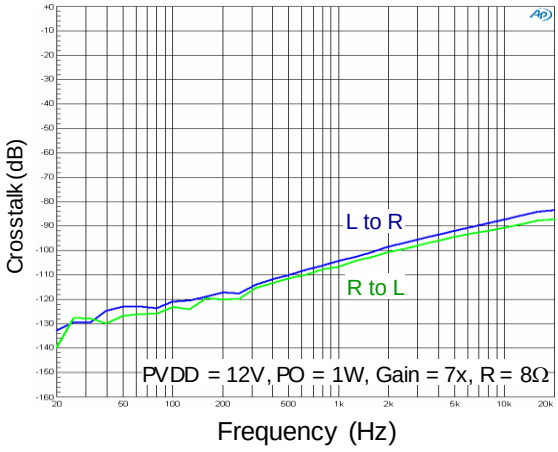
THD + N vs. Frequency (BTL)



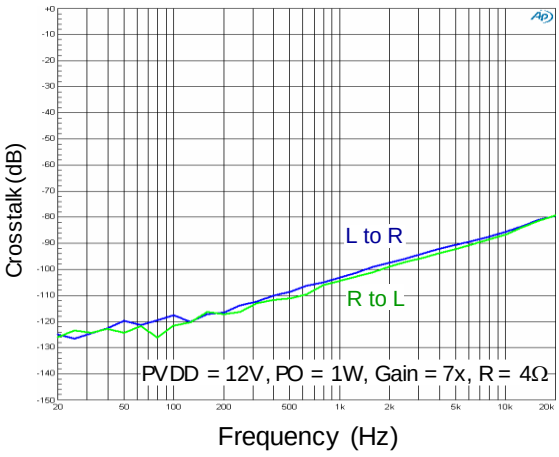
THD + N vs. Frequency (BTL)



Crosstalk vs. Frequency

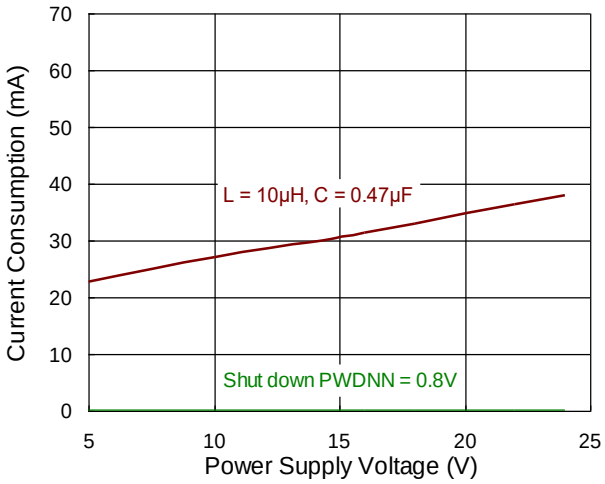


Crosstalk vs. Frequency

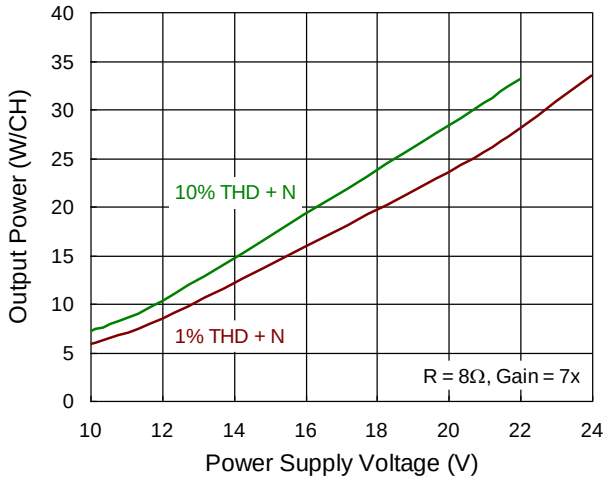


PWM = 768kHz

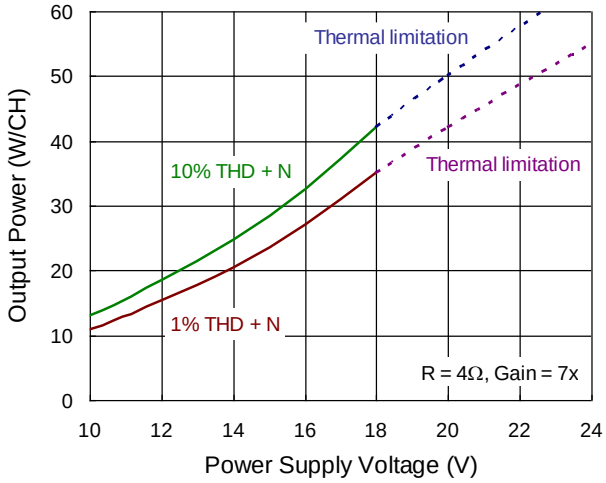
Current Consumption vs. Power Supply Voltage



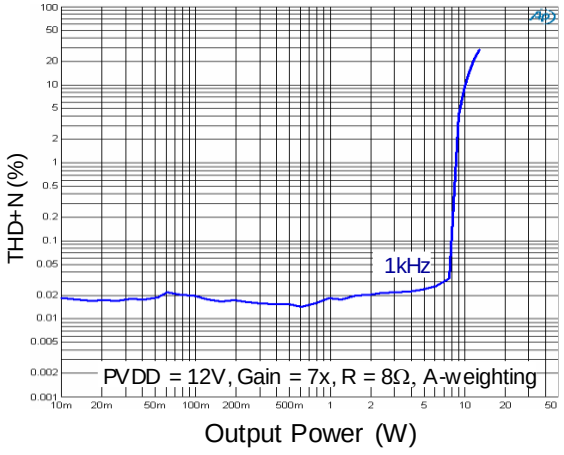
Output Power vs. Power Supply Voltage (BTL)



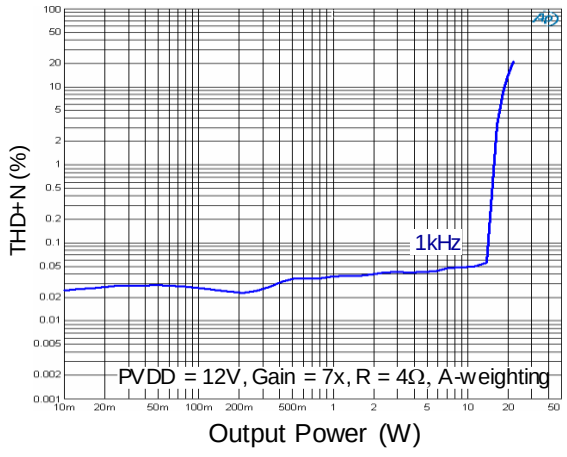
Output Power vs. Power Supply Voltage (BTL)



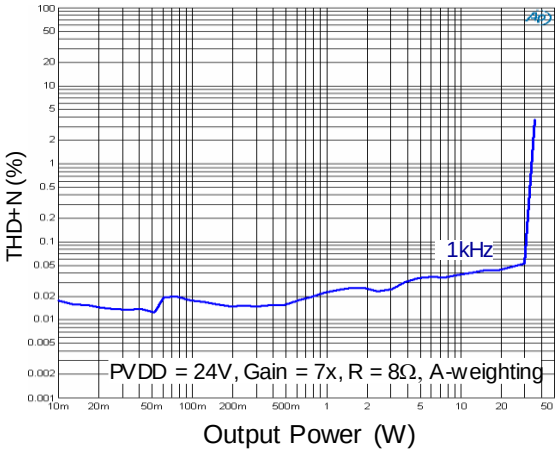
THD + N vs. Output Power (BTL)



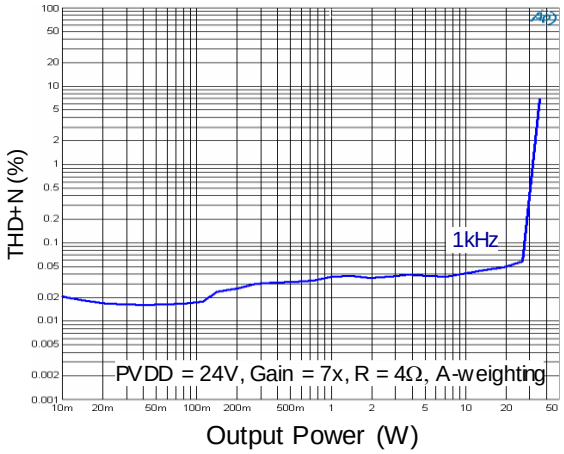
THD + N vs. Output Power (BTL)



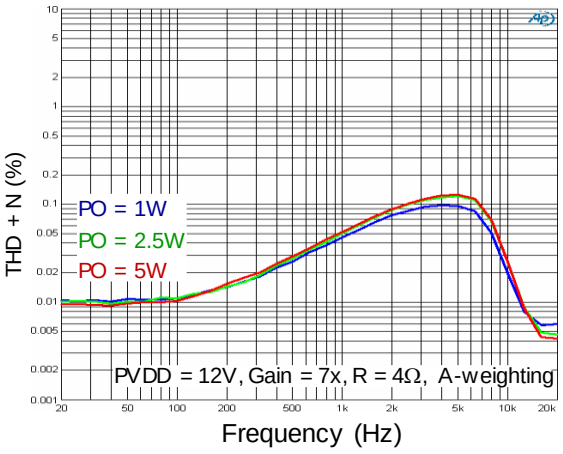
THD + N vs. Output Power (BTL)



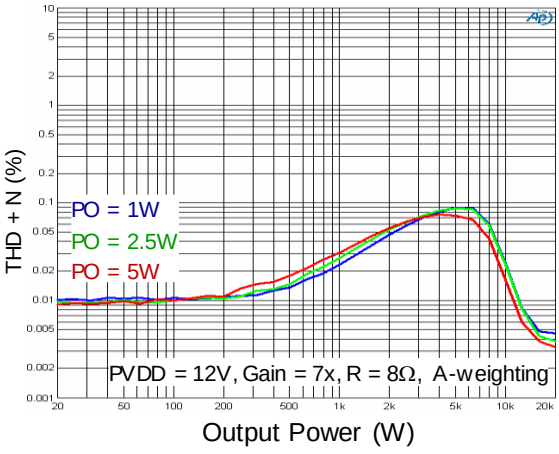
THD + N vs. Output Power (BTL)



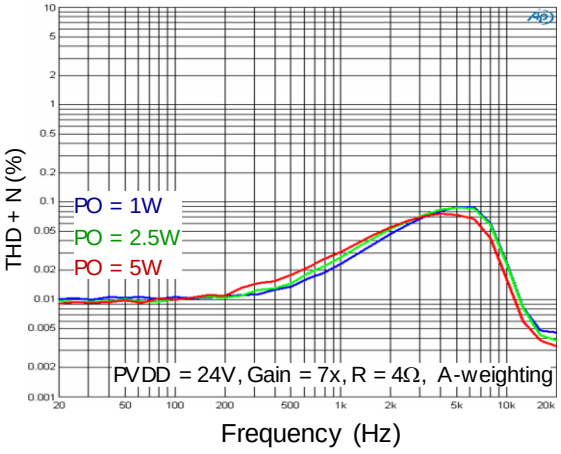
THD + N vs. Frequency (BTL)



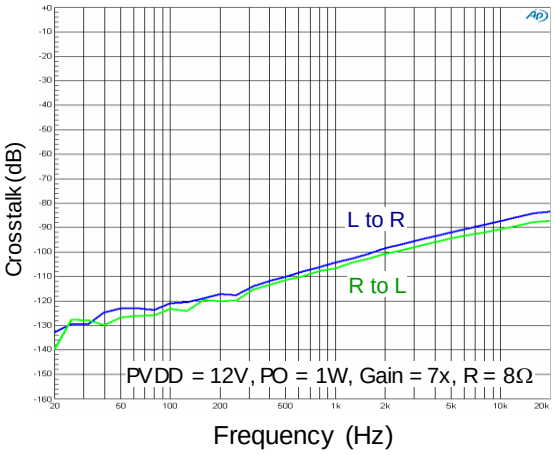
THD + N vs. Frequency (BTL)



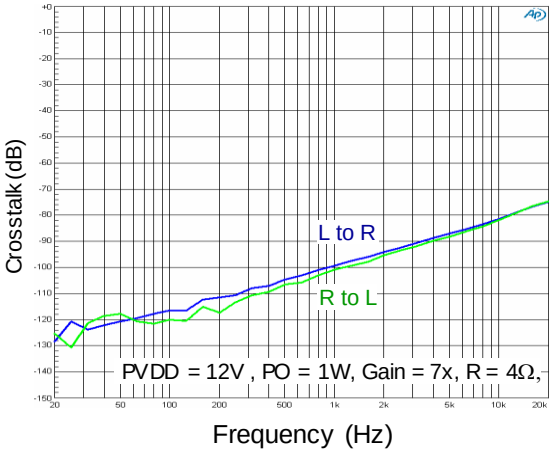
THD + N vs. Frequency (BTL)

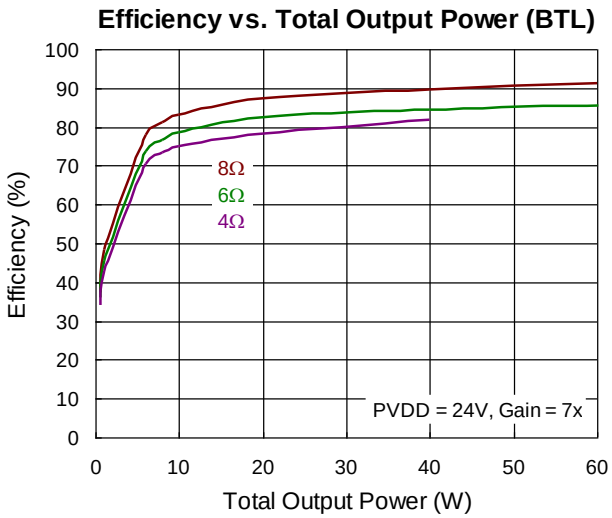


Crosstalk vs. Frequency



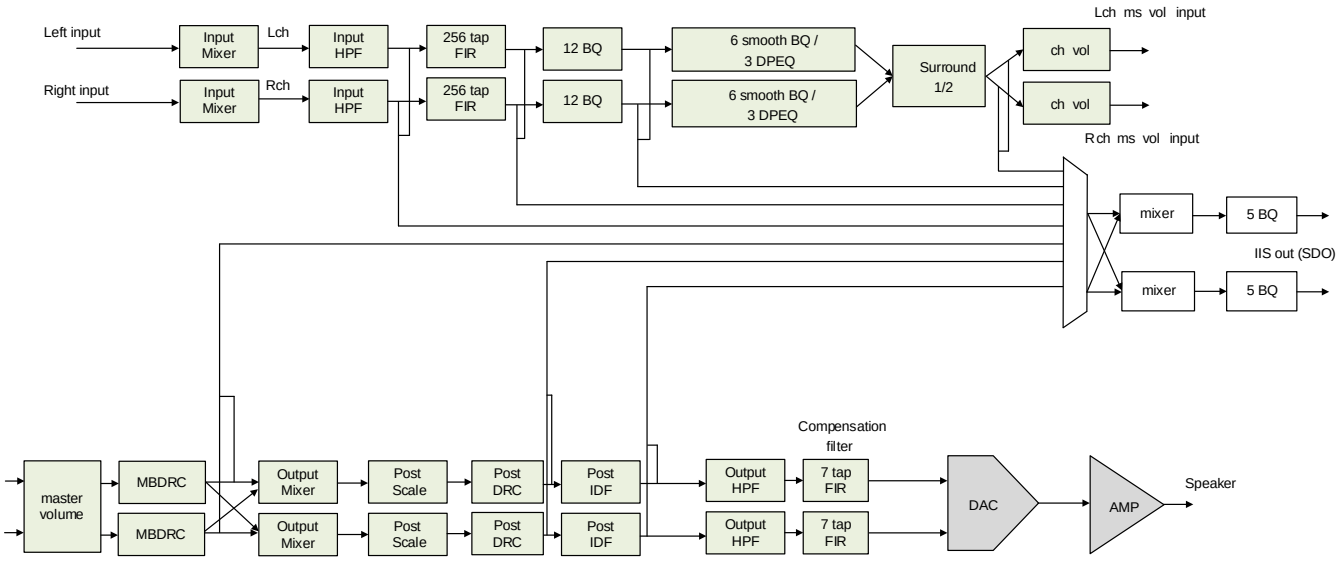
Crosstalk vs. Frequency



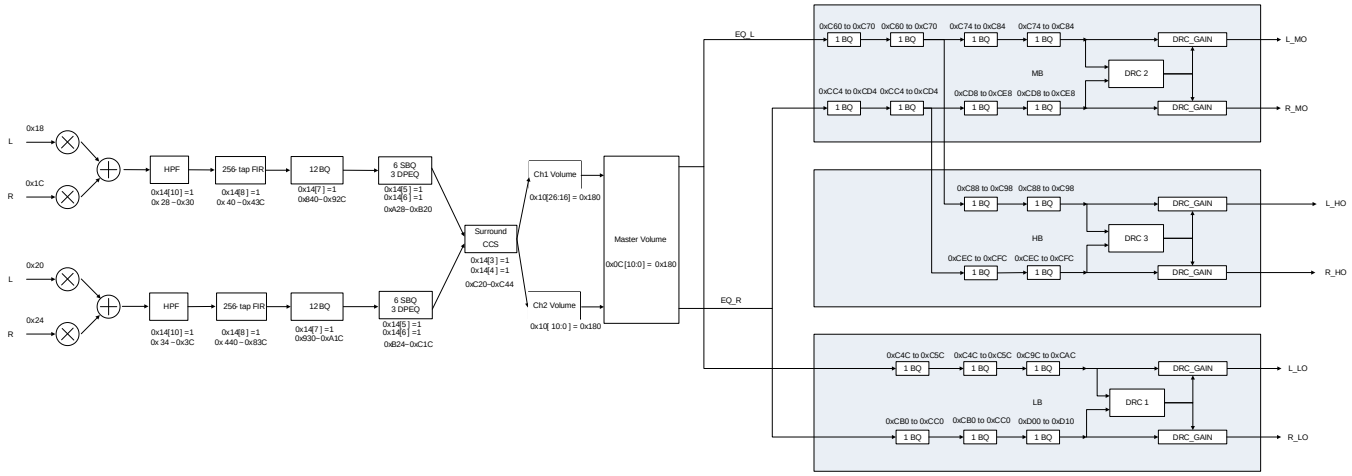


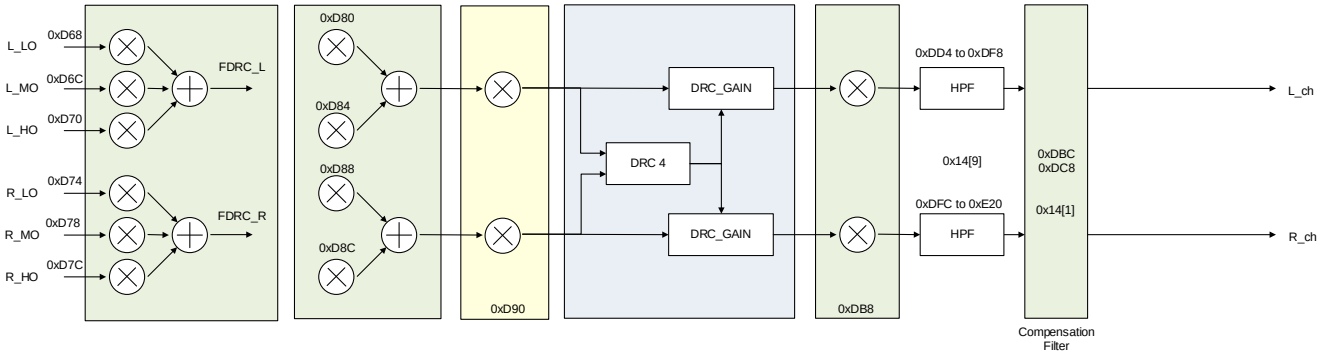
Noted: Measurements were made using the RT9121_EVM board and Audio Precision System 2722 with AUX0025 low-pass filter. All measurements taken with 1kHz.

Overall Signal Path



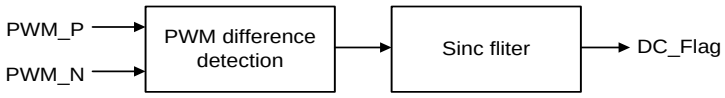
Detailed Signal Path





DC Protection Function

It is to use to protect the loudspeaker, when there are some DC exists at the output. The method is to detect DC at final stage (PWM), calculate the difference of the PWM and a Sinc filter to decide the DC level. The IC will shut down when detect the DC.



Address	BITS	Name	Description
0x14	7:4	Reserved	
	3:2	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%
	1	DC_TIME_SEL	Detection time 0: 342ms (default) 1: 684ms
	0	DC_EN	0: DC Protection disable 1: DC protection enable

Protection Behavior (FAULT_N)

If the protection behavior happened, the IC will automated detect, the error condition can be checked by the register or FAULT_N pin.

Protection Flag

Address	BITS	Name	Description
0xFF03	7	SM Update_ERR	SM update flag report 0: SM Update error (default) 1: SM Update error, write 0 to clear flag
	6	I2C Master Event _ERR	I^2C master event flag report 0: No I^2C master event error (default) 1: I^2C master event error, write 0 to clear flag
	5	129K Over loading_ERR	0: 129K over loading error (default) 1: 129K over loading, write 0 to clear flag
	4	WDT Reset Event _ERR	0: WDT reset event error (default) 1: WDT reset event, write0 to clear flag
	3	Software Reset Event _ERR	0: Software reset event error (default) 1: Software reset event, write 0 to clear flag
	2	SPI_ERR	0: SPI error (default) 1: SPI, write 0 to clear flag
	1	I2C_ERR	0: I^2C error (default) 1: I^2C, write 0 to clear flag
	0	POR Init_ERR	0: POR Init error (default) 1: POR Init, write 0 to clear flag

Protection Behavior (FAULT_N2)

If the protection behavior happened, the IC will automated detect, the error condition can be checked by the register or FAULT_N2 pin.

Protection Flag

Address	BITS	Name	Description
0x10	7	Reserved	
	6	DC_ERR	DC flag report 0: No DC error (default) 1: DC error
	5	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag
	4	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag
	3	OC_ERR	0: No OC error (default) 1: OC, write 0 to clear flag
	2	OV_ERR	0: No OV error (default) 1: OV, write 0 to clear flag
	1	OT_ERR	0: No OT error (default) 1: OT, write 0 to clear flag
	0	UV_ERR	0: No UV error (default) 1: UV, write 0 to clear flag

Protection Type

Protection	Auto-Recovery	Shutdown Amp (Latch Type)	Fault Pin Pull Low
DC Protection	No	Yes	Yes
SCLK ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[5]	Yes, but the MASK can be configured by the 0x11 bit[5]
LRCK ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[4]	Yes, but the MASK can be configured by the 0x11 bit[4]
OC ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[3]	Yes, but the MASK can be configured by the 0x11 bit[3]
OV ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[2]	Yes, but the MASK can be configured by the 0x11 bit[2]
OT ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[1]	Yes, but the MASK can be configured by the 0x11 bit[1]
UV ERROR	Yes. The default setting is Auto-recovery.	Yes, it can be configured by the 0x12 bit[0]	Yes, but the MASK can be configured by the 0x1 bit[0]

When protection happened, there are 2 types of the protection behavior can be use.

1. Latch type: Will shut down the AMP directly.
2. Auto recovery type: The AMP will enter the auto recovery mode, until the protection behavior stop, the AMP will continued to work.
3. The DC protection only has the latch type.

Fault Behavior Type Select (FAULT_N2)

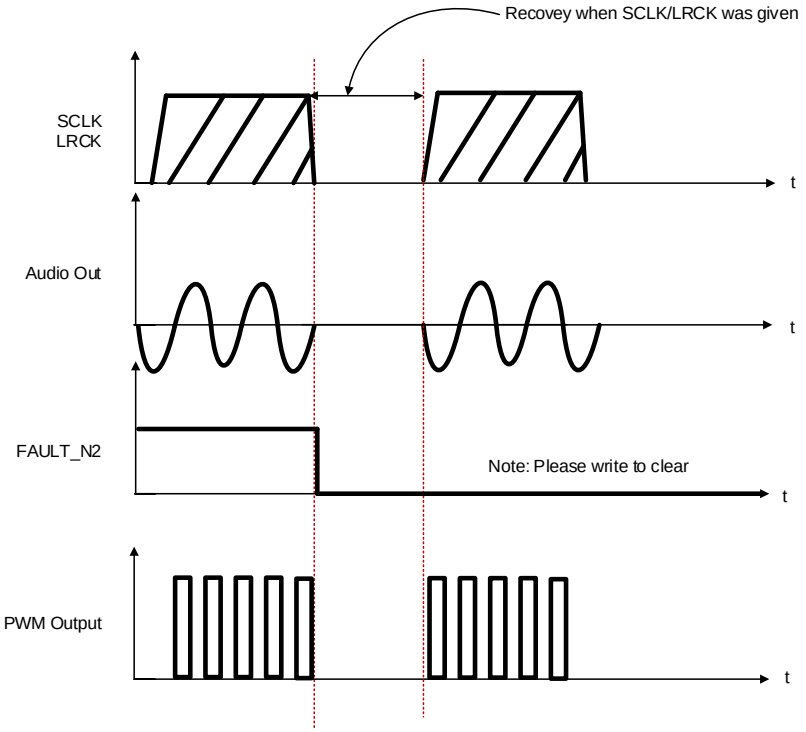
If the protection behavior happened, the IC will automate detect, there are some error type can been configured by below list.

Address	BITS	Name	Description
0x12	5	SCLK_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	4	LRCK_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	3	OC_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch (default)
	2	OV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	1	OT_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch
	0	UV_ERROR_FAULT_TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch

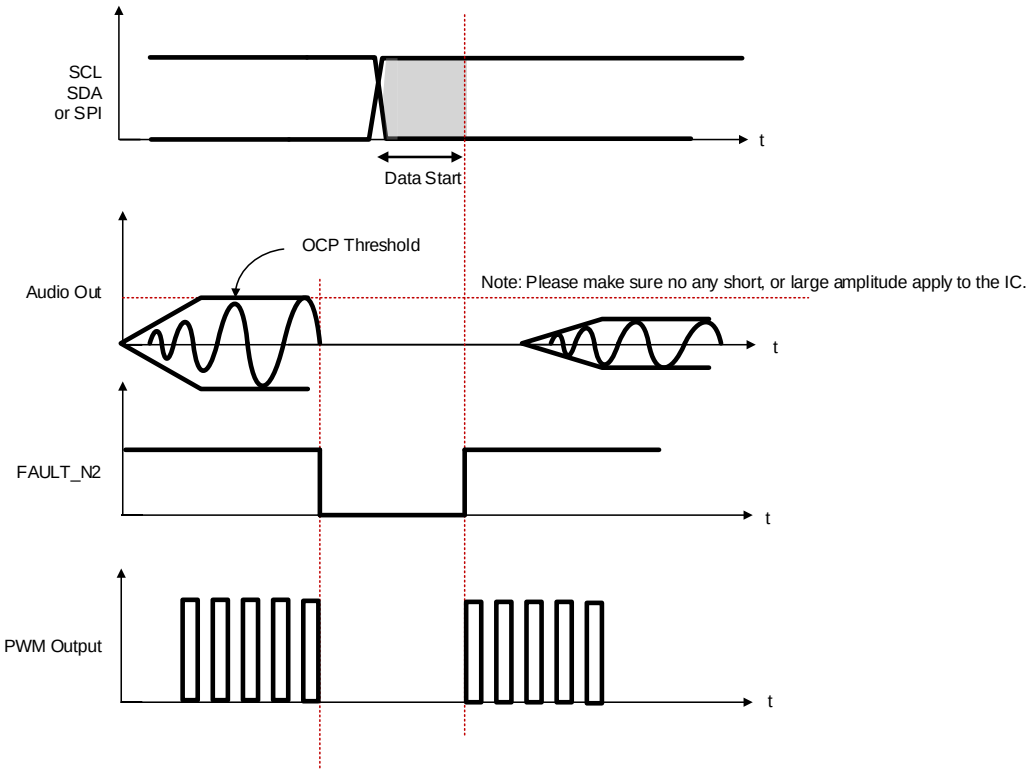
Fault Mask

Address	BITS	Name	Description
0x11	5	SCLK_ERROR_mask	Fault mask for 0x10 SCLK error
	4	LRCK_ERROR_mask	Fault mask for 0x10 LRCK error
	3	OC_ERROR_mask	Fault mask for 0x10 OC error
	2	OV_ERROR_mask	Fault mask for 0x10 OV error
	1	OT_ERROR_mask	Fault mask for 0x10 OT error
	0	UV_ERROR_mask	Fault mask for 0x10 UV error

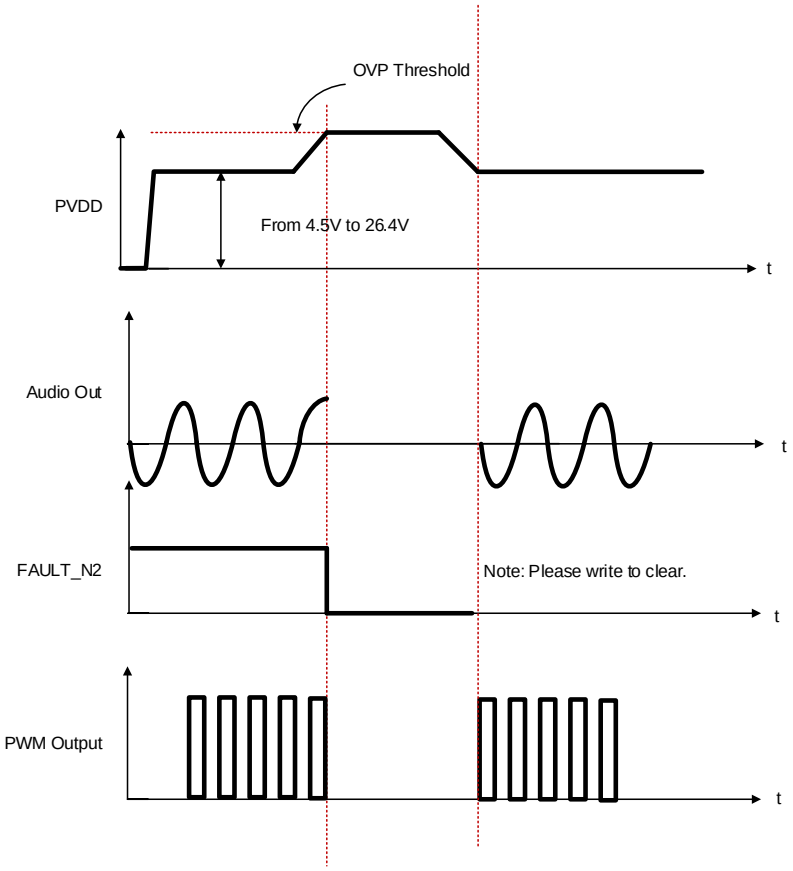
SCLK/LRCK Error



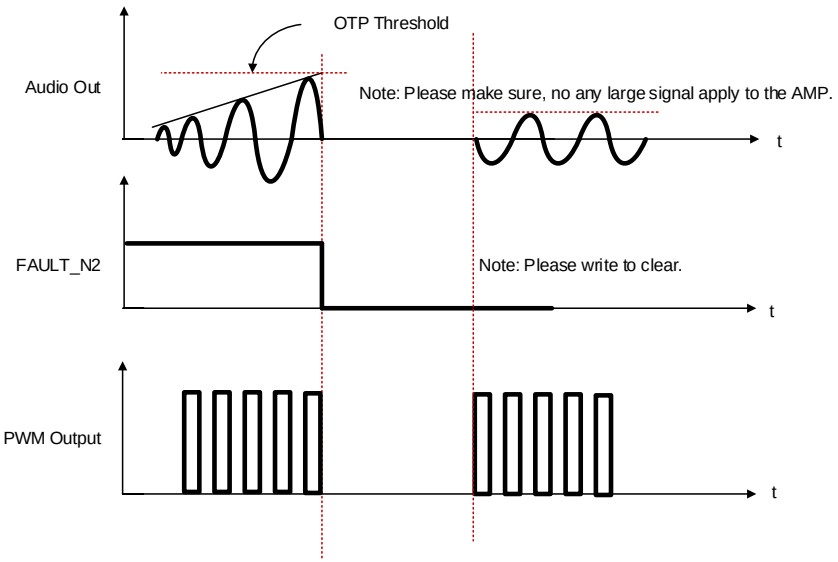
OCP Error



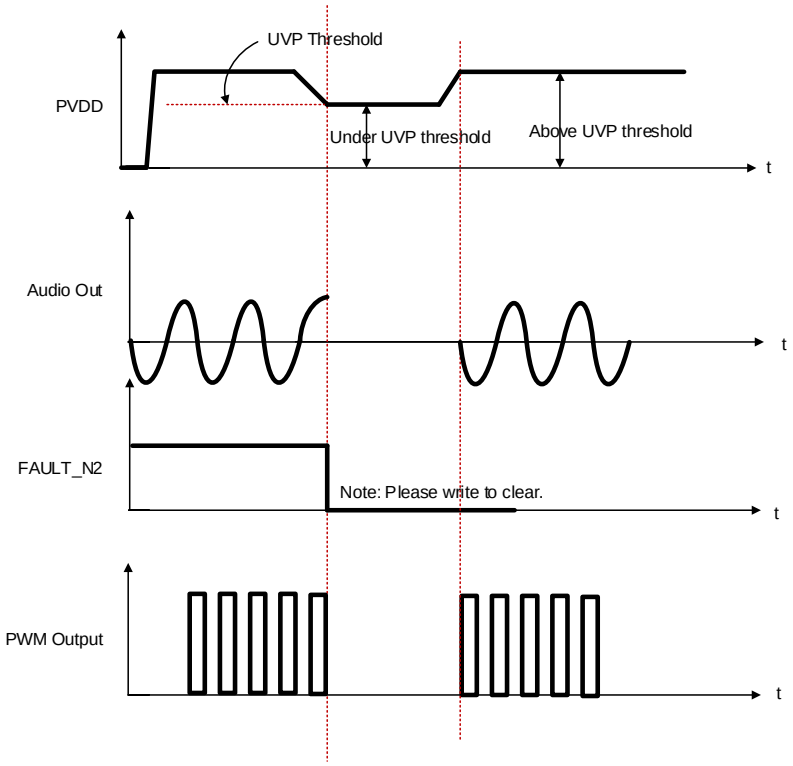
OVP Error



OTP Error



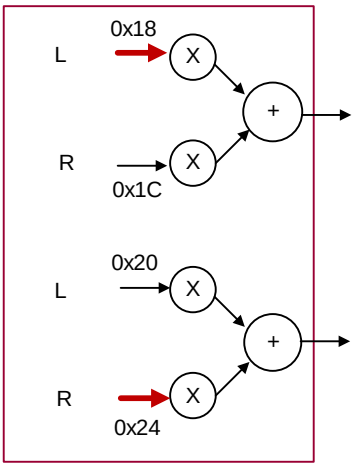
UVP Error



Input Mixer

Block Diagram and Description

→Input mixer range is from mute to 12dB, 1 step is 0.0625dB.



→Default signal flow for L is 0x18
→Default signal flow for R is 0x24

Address	BITS	Name	Description
0x18	31:0	CH1_IN_MIX_0	Input mixer for L ch
0x1C	31:0	CH1_IN_MIX_1	Input mixer for R ch
0x20	31:0	CH2_IN_MIX_0	Input mixer for L ch
0x24	31:0	CH2_IN_MIX_1	Input mixer for R ch

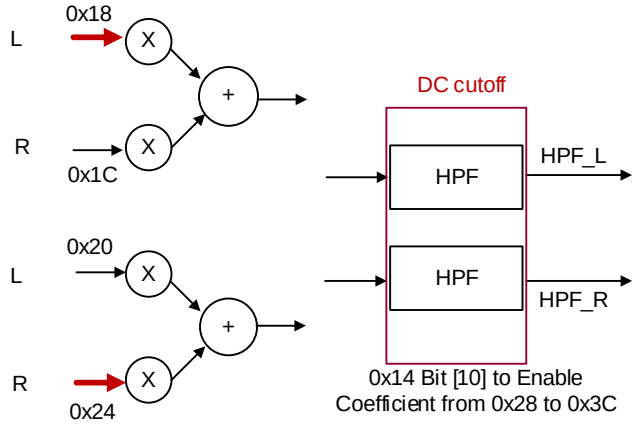
Mixer Gain Setting

Address	BITS	Name	Equation
0x18, 0x1C, 0x20, 0x24	31:0	mix_1[31:0] mix_0[31:0]	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: −6dB = 0.5011872336, then convert 0.5011872336 into fix point will be 0x3F004DCE. Example 2: 0dB = 1, then convert 1 into fix point will be 0x3F800000.

Input High Pass Filter

Block Diagram and Description

→There are DC-Cut filter for each channel. Which belongs to the 1st order filter.



Address	BITS	Name	Description
0x14	10	HPF_EN	0: Input high-pass filter disable (default) 1: Input high-pass filter enable

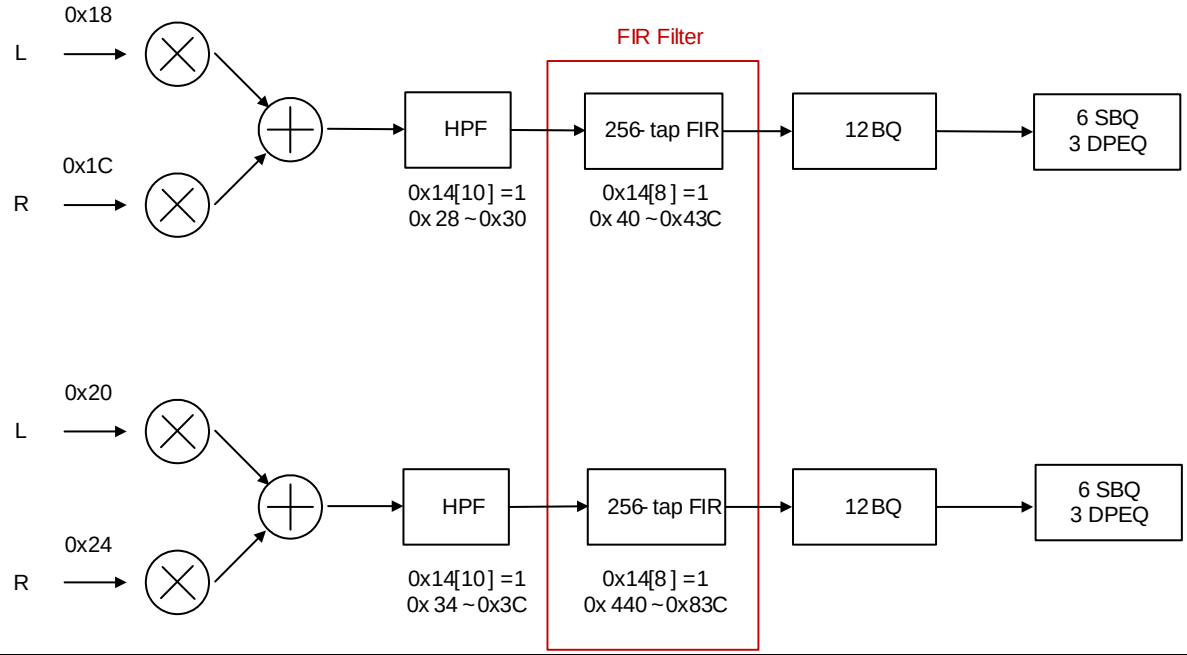
Address	BITS	Name	Description
0x28	31:0	CH1_IN_HPF_B0	Coefficient B0 for Ch1 HPF
0x2C	31:0	CH1_IN_HPF_B1	Coefficient B1 for Ch1 HPF
0x30	31:0	CH1_IN_HPF_A1	Coefficient A1 for Ch1 HPF

Address	BITS	Name	Description
0x34	31:0	CH2_IN_HPF_B0	Coefficient B0 for Ch2 HPF
0x38	31:0	CH2_IN_HPF_B1	Coefficient B1 for Ch2 HPF
0x3C	31:0	CH2_IN_HPF_A1	Coefficient A1 for Ch2 HPF

FIR Filter

Block Diagram and Description

→There is a 128 tap FIR filter, the data is 3.23 format.



Address	BITS	Name	Description
0x14	8	FIR_EN	FIR filter enable 0: Disable (default) 1: Enable
0x14	14	FIR_Link	0: CH1, CH2 independent 1: CH2 coefficient = CH1 (default)

FIR Coefficient

Address	BITS	Name	Description
0x40 to 0x43C	31:0	CH1_FIR_TAP1 to CH1 FIR_TAP255	Register 0x40 to 0x43C are 256 coefficients, L/R are the same. Each coefficient is 4-byte, 3.23 format

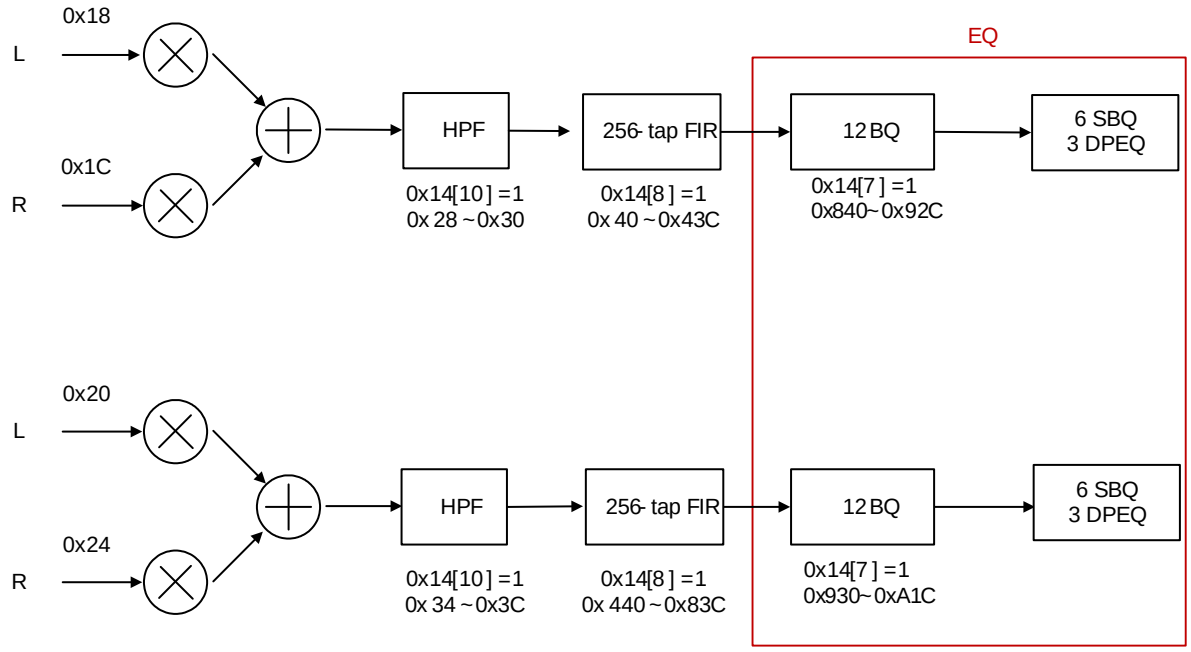
Address	BITS	Name	Description
0x440 to 0x83C	31:0	CH2_FIR_TAP1 to CH2 FIR_TAP255	Register 0x440 to 0x83C are 256 coefficients, L/R are the same. Each coefficient is 4-byte, 3.23 format

EQ Link & Bypass

Block Diagram and Description

→Link L/R channel EQ parameter automatically and using the same parameter.

→EQ_BYPASS can bypass the EQ path in signal path. Each EQ band has disable bit.



EQ Function Control

Address	BITS	Name	Description
0x14	7	EQ_EN	EQ filter enable 0: Bypass (default) 1: Enable
0x14	12	EQ_PART_LINK	EQ7 to EQ12 coefficient link. When EQ_LINK_ALL = 1 0: Link all (default) 1: Link EQ7 to EQ12
0x14	13	EQ_Link_All	EQ1 to EQ12 and SEQ1 to 8 coefficient link 0: CH1, CH2 independent (default) 1: Take CH1 coefficients to CH2
0xA20	19:16	EQ_NUM	Number of Bi-Quad control: Set 0x01: Enable 1 Bi-Quad Set 0x0C: Enable 12 Bi-Quad

EQ Coefficient

Address	BITS	Name	Description
0x840 to 0x92C	4	CH1_EQ1_B0 to CH1_EQ12_A2	Coefficient for Ch1 EQ1 to Ch1 EQ 12
0x930 to 0xA1C	4	CH2_EQ1_B0 to CH2_EQ12_A2	Coefficient for Ch2 EQ1 to Ch2 EQ 12

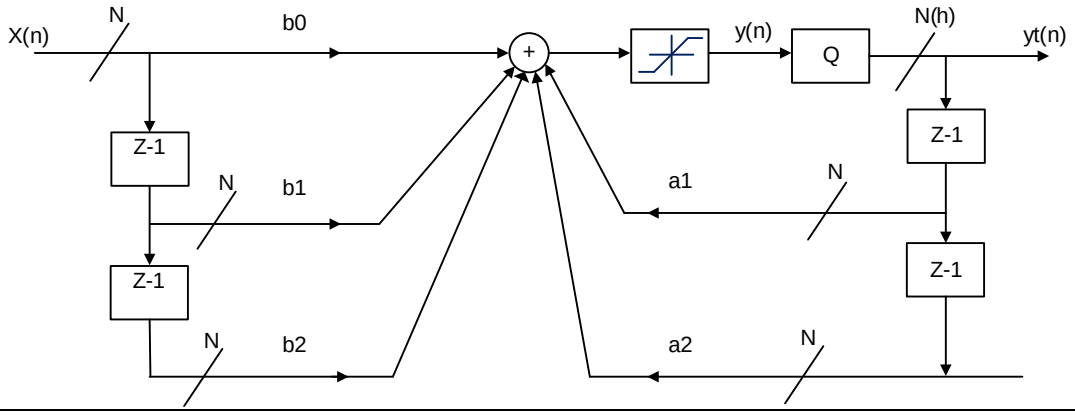
EQ

Block Diagram and Description

→There are 12 Bands of Bi-Quad filter for each Channel. So There are 18 bands of the Bi-Quad can be used including the smooth Bi-Quad.

EQ parameter: b0/b1/b2/a1/a2

Update coefficient after writing 5 coefficients

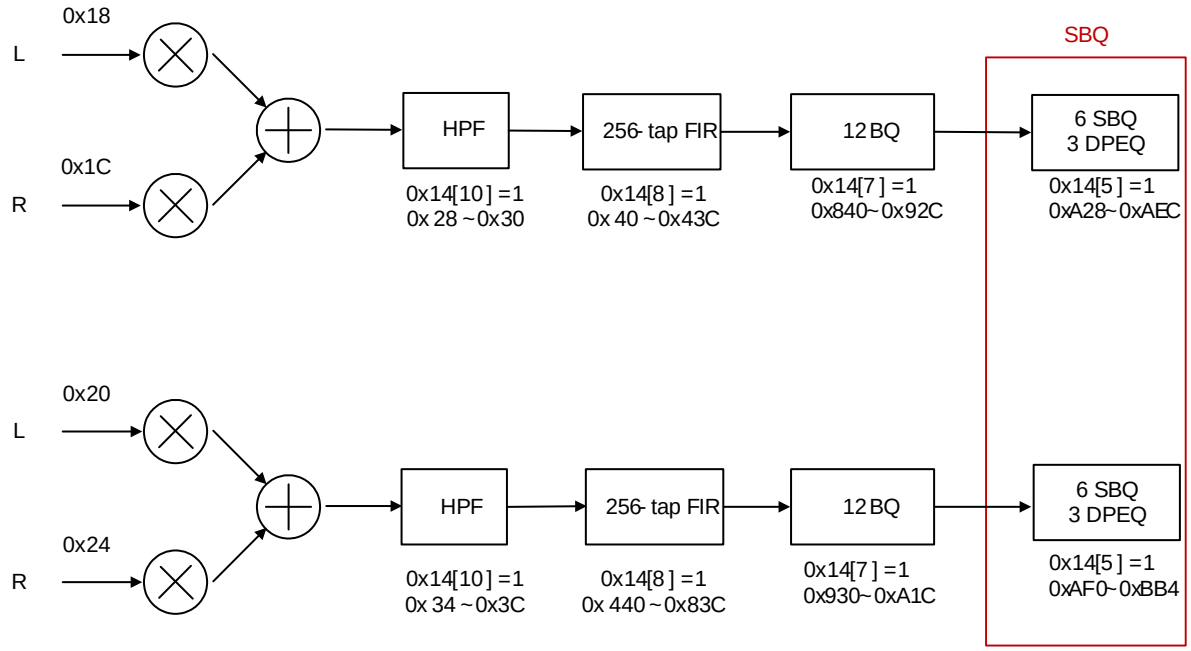


Smooth Bi-Quad

Block Diagram and Description

→Smooth biquad is identical biquad filter with coefficient updated smoothly.

→New coefficient update linearly/exponentially to avoid undesirable sound during setting new coefficient for biquad.



→One smooth-BQ consists of 2 BQs to process the same audio signal in parallel. One of the BQs uses current coefficients and the other one uses updating coefficients to generate the outputs, BQ_1_output and BQ_2_output, respectively.

→For a-filter smooth, the output of smooth-BQ is the summation of BQ_1_output and BQ_2_output using the below equations.

SBQ_output[n] = a_1[n] * BQ_1_output[n]+a_2[n] * BQ_2_output[n]

a_1[n] = (1-AS) + AS * a_1[n-1], if BQ_1 is the current active BQ and a_1[0] = 1

a_2[n] = (1-AS) + AS * a_2[n-1], if BQ_2 is the updating BQ and a_2[0] = 0

If SBQ_UPDATE is triggered, a_1[n] = 0 and a_2[n] = 1 after TS samples

→For linear smooth, the equations for smooth-BQ are listed below.

a_1[n] = a_1[n-1] - 1/TS, if BQ_1 is the active BQ and a_1[0] = 1

a_2[n] = a_2[n-1] + 1/TS, if BQ_2 is the updating BQ and a_2[0] = 0

If SBQ_UPDATE is triggered, a_1[n] = 0 and a_2[n] = 1 after TS samples. When linear smooth is used, the TS shall be the power of 2 for design simplicity.

Note: When using SMBQ, DPEQ cannot be used.

Smooth EQ Function Control

Address	BITS	Name	Description
0x14	5	SEQ_DPEQ_EN	Smooth EQ filter enable 0: Bypass (default) 1: Enable
0x14	6	SEQ_DPEQ_SEL	Select Smooth EQ or DPEQ 0: Smooth EQ (default) 1: Dynamic EQ
0x14	13	EQ_Link_All	EQ1 to EQ12 and SEQ1 to 8 coefficient link 0: CH1, CH2 independent (default) 1: Take CH1 coefficients to CH2
0xA20	2:0	SEQ_UPDATE	000: No update (default) 001: Update BK1/BK2 to SEQ1/SEQ2 010: Update BK1/BK2 to SEQ3/SEQ4 011: Update BK1/BK2 to SEQ5/SEQ6 100: Update BK1/BK2 to SEQ7/SEQ8 Others: Reserved
0xA20	3	SMOOTH_DONE	Read 0xFF03 bit7 for smooth done (read clear) 1 = Done
0xA20	4	SMOOTH_METHOD	0: Alpha filter (default) 1: Linear
0xA20	15:8	SMOOTH_EQ_TS	Smooth EQ Linear setting, From 4 Sample to 1024 Sample
0xA24	31:0	SMOOTH_EQ_ALPHA	Alpha filter coefficient for smoothing From 4 Sample to 1024 Sample

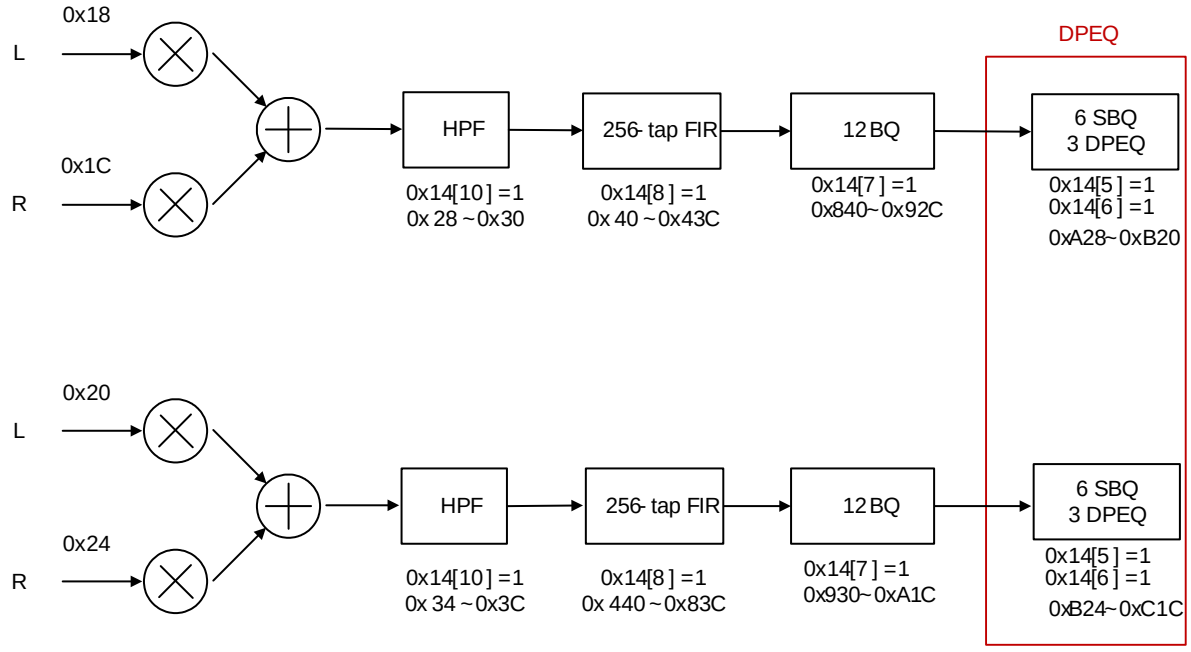
Smooth EQ Coefficient

Address	BITS	Name	Description
0xA28 to 0xAEC	4	CH1_SEQ1 to CH1_SEQBK2	Coefficient for Ch1 SEQ1 to Ch1 SEQ update coefficient
0xAF0 to 0xBB4	4	CH2_SEQ1 to CH2_SEQBK2	Coefficient for Ch2 SEQ1 to Ch2 SEQ update coefficient

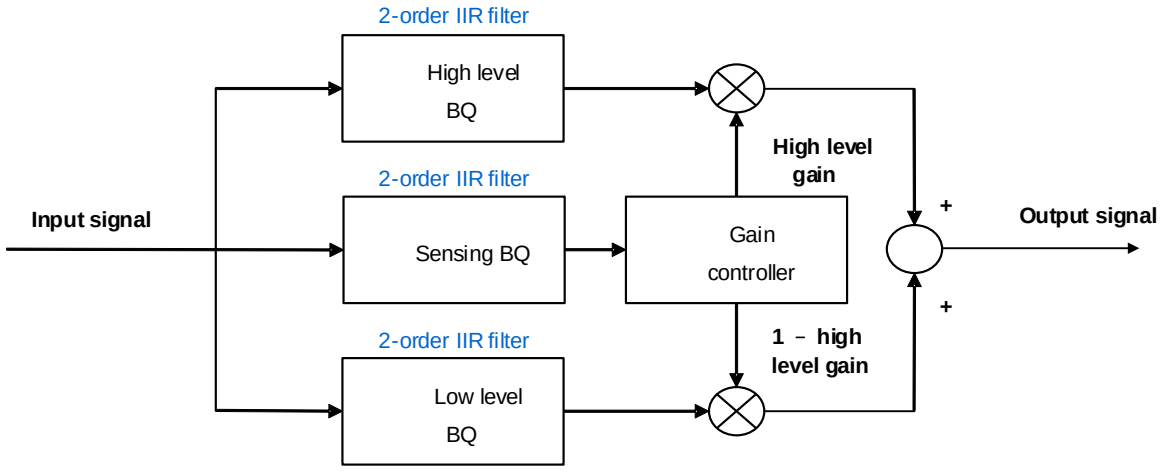
DPEQ

Block Diagram and Description

→The dynamic equalizer provides the ballistic control of a dynamic range compressor to the conventional equalizer allowing time-varying adjustment of equalization curve.



→Flow Chart



Note: When using DPBQ, SMBQ cannot be used.

DPEQ Function Control

Address	BITS	Name	Description
0x14	5	SEQ_DPEQ_EN	Smooth EQ filter enable 0: Bypass (default) 1: Enable
0x14	6	SEQ_DPEQ_SEL	Select Smooth EQ or DPEQ 0: Smooth EQ (default) 1: Dynamic EQ
0x14	11	SEQ_LINK	SEQ1 to SEQ8 or DPEQ1 to DPEQ3 coefficient link When EQ_LINK_ALL = 1 0: CH1/CH2 independent (default) 1: Link All (CH2 as CH1)
0xA20	6:5	DPEQ_NUM	Set number of DPEQ 0x00: No DPEQ (default) 0x01: 1 set of DPEQ enable 0x10: 2 set of DPEQ enable 0x11: 3 set of DPEQ enable
0xA24	31:0	DPEQ_MODE_PEAK	0: RMS mode Note: Recommended to use RMS mode

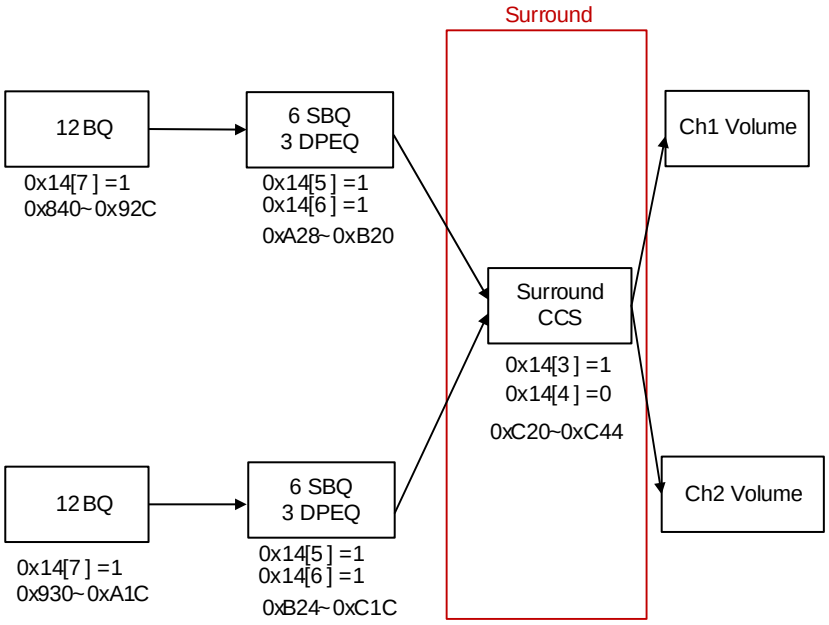
DPEQ Coefficient

Address	BITS	Name	Description
0xA28 to 0xB20	4	CH1_DPEQ1 to CH1_DPEQ3	Coefficient for Ch1 DPEQ1 to Ch1 DPEQ3
0xB24 to 0xC1C	4	CH2_DPEQ1 to CH2_DPEQ3	Coefficient for Ch2 DPEQ1 to Ch2 DPEQ3

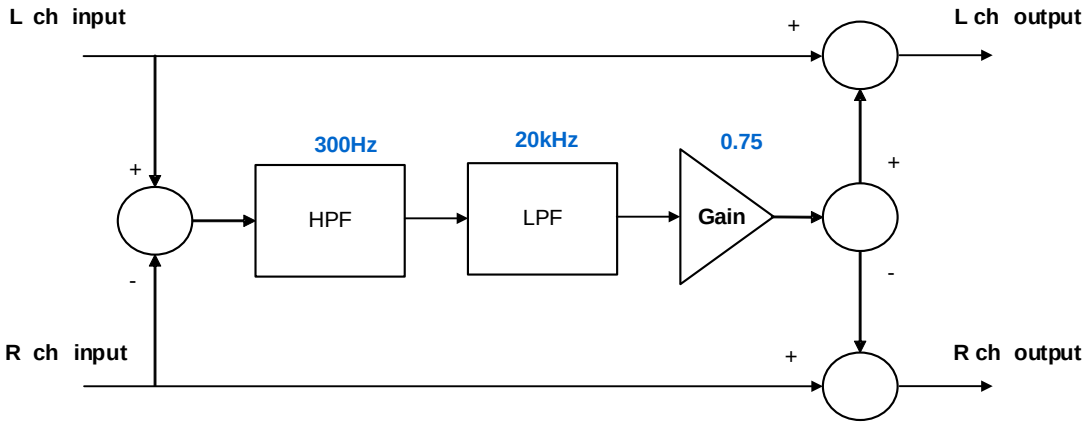
Surround (Spatializer)

Block Diagram and Description

→Spatializer is a method to increase the field of sound for a broader and more encompassing audio experience.



→Flow Chart



Note: When using Surround, CCS cannot be used.

Surround Function Control

Address	BITS	Name	Description
0x14	3	SURROUND_EN	Surround enable 0: Bypass (default) 1: Enable
0x14	4	SURROUND_SEL	Select Surround (Spatializer) or CCS 0: Spatializer (default) 1: CCS

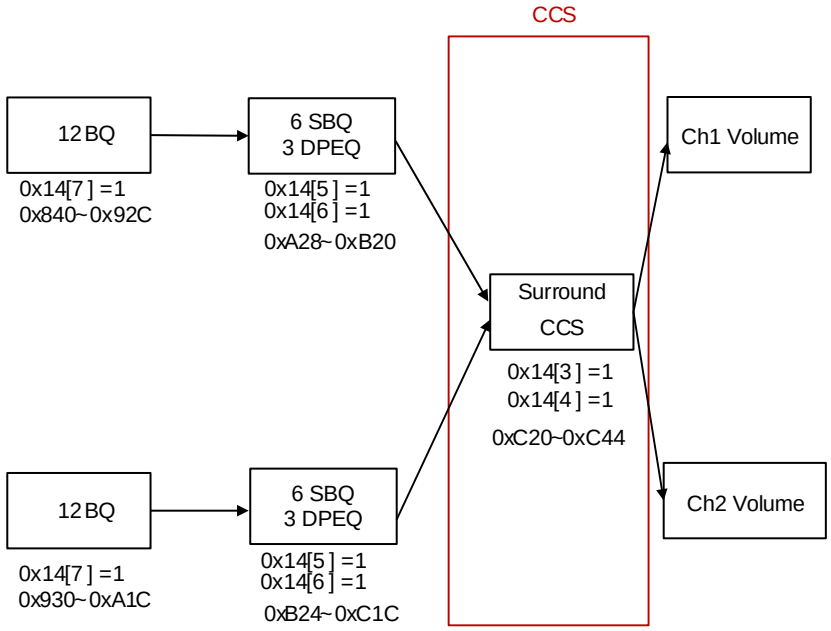
Surround Coefficient

Address	BITS	Name	Description
0xC20 to 0xC44	4	SURROUND_H1_B0 to SURROUND_H2_A2	Surround Bi-Quad Coefficient setting

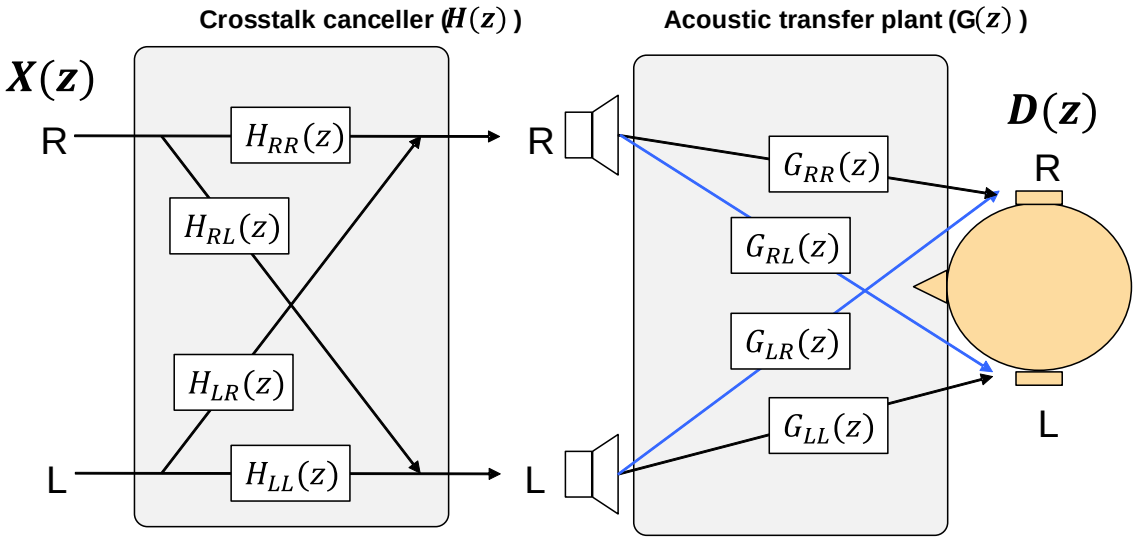
CCS (Cross Talk Cancellation System)

Block Diagram and Description

→In general terms, any unwanted leakage between parallel information channels is considered crosstalk.



→Flow Chart



Note: When using CCS, Surround cannot be used.

CCS Function Control

Address	BITS	Name	Description
0x14	3	SURROUND_EN	Surround enable 0: Bypass (default) 1: Enable
0x14	4	SURROUND_SEL	Select Surround (Spatializer) or CCS 0: Spatializer (default) 1: CCS

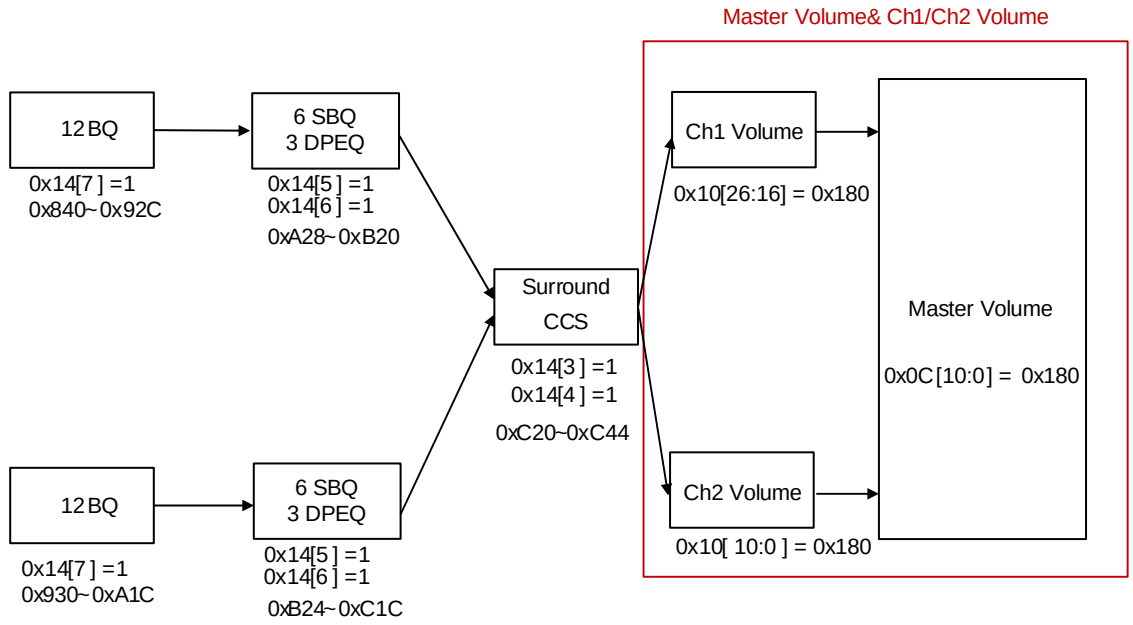
CCS Coefficient

Address	BITS	Name	Description
0xC20 to 0xC44	4	CCS_H1_B0 to CCS_H2_A2	CCS Bi-Quad Coefficient setting

Master Volume & Ch1/Ch2 Volume

Block Diagram and Description

→The RT9121 has separate L/R channel volume control, also has the mater volume to control both L/R channel volume.



Volume Function Control

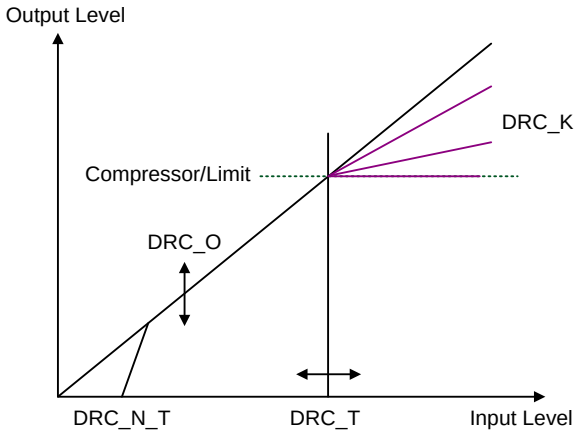
Address	BITS	Name	Description
0x0C	10:0	MS_VOL	24dB to −103.9375dB, 0.0625dB per step
0x10	31	CH1_MUTE	0: un-mute (default) 1: mute
0x10	26:16	CH1_VOL	24dB to −103.9375dB, 0.0625dB per step
0x10	15	CH2_MUTE	0: un-mute (default) 1: mute
0x10	10:0	CH2_VOL	24dB to −103.9375dB, 0.0625dB per step

Master Volume and Ch1/Ch2 Gain Equation

Equation
Equation: 24dB - (Dec * 0.0625) Range: 24dB (0X000) to mute (0x7ff) Example : 10dB, Hex = 0xE0 Dec = 224 Gain = 24dB - (224 * 0.0625) = 10dB

Gain	Dec	Hex
24dB	0	0x00
10dB	224	0XE0
. . .	. . .	. . .
0dB	384	0x180
. . .	. . .	. . .

Multi-Band DRC

DRC Description	Address	Description
DRC_T: Threshold	0xD24, 0x40, 0xD5C, 0xDAC	
DRC_K: Compress ratio	0xD28, 0xD44, 0xD60, 0xDB0	
DRC_O: Make up gain	0xD2C, 0xD48, 0xD64, 0xDB4	
DRC_N_T: Noise gate threshold	0xD94	
Noise Gate Enable	0xC48	

Address	BITS	Name	Description
0xC48	20	DRC4_N_EN	1: DRC4 Noise gate enable 0: DRC4 Noise gate disable (default)
	19	DRC3_N_EN	1: DRC3 Noise gate enable 0: DRC3 Noise gate disable (default)
	18	DRC2_N_EN	1: DRC2 Noise gate enable 0: DRC2 Noise gate disable (default)
	17	DRC1_N_EN	1: DRC1 Noise Gate enable 0: DRC1 Noise gate disable (default)

Address	BITS	Name	Description
0xD14	31:0	DRC1 RMS ALPHA	DRC 1 AE
0xD18	31:0	DRC1 RMS OMEGA	DRC 1 1-AE
0xD1C	31:0	DRC1 GAIN AT	DRC 1 Attack time AA
0xD20	31:0	DRC1 GAIN RT	DRC 1 Release time AD
0xD24	31:0	DRC1 TH0 [31:0]	DRC1 threshold
0xD28	31:0	DRC1 RATIO[31:0]	DRC1 compression ratio
0xD2C	31:0	DRC1 MAKEUP [31:0]	DRC1 make up gain
0xD30	31:0	DRC2 RMS ALPHA	DRC 2 AE
0xD34	31:0	DRC2 RMS OMEGA	DRC 2 1-AE
0xD38	31:0	DRC2 GAIN AT	DRC 2 Attack time AA
0xD3C	31:0	DRC2 GAIN RT	DRC 2 Release time AD
0xD40	31:0	DRC2 TH0 [31:0]	DRC2 threshold
0xD44	31:0	DRC2 RATIO[31:0]	DRC2 compression ratio
0xD48	31:0	DRC2 MAKEUP [31:0]	DRC2 make up gain
0xD4C	31:0	DRC3 RMS ALPHA	DRC 3 AE
0xD50	31:0	DRC3 RMS OMEGA	DRC 3 1-AE
0xD54	31:0	DRC3 GAIN AT	DRC 3 Attack time AA
0xD58	31:0	DRC3 GAIN RT	DRC 3 Release time AD
0xD5C	31:0	DRC3 TH0 [31:0]	DRC3 threshold
0xD60	31:0	DRC3 RATIO [31:0]	DRC3 compression ratio
0xD64	31:0	DRC3 MAKEUP [31:0]	DRC3 make up gain
0xD9C	31:0	DRC4_ALPHA	DRC 4 AE
0xDA0	31:0	DRC4_OMEGA	DRC 4 1-AE
0xDA4	31:0	DRC4_AT	DRC 4 Attack time AA
0xDA8	31:0	DRC4 RT	DRC 4 Release time AD
0xDAC	31:0	DRC4 TH0 [31:0]	DRC4 threshold
0xDB0	31:0	DRC4 RATIO [31:0]	DRC4 compression ratio
0xDB4	31:0	DRC4 MAKEUP [31:0]	DRC4 make up gain
0xD94	31:0	DRC_TH2 [31:0]	DRC1, 2, 3, 4 noise gate of the DRC

DRC Timing Equation

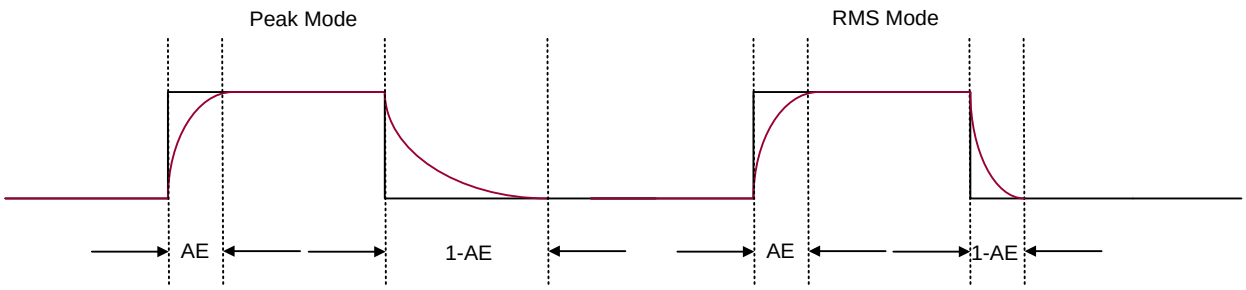
DRC Description	Equation
AA/AE/AD/1-AE Timing	Equation 1: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Equation 2: AA = (1-e-1/(ta * fs)) ta = AA/AD/AE timing, fs = sampling rate Example: ta = 0.1ms, fs = 48k AA = (1-e-1/(0.0001 * 48000)) =0.188063654 Put 0.188063654 into floating point convert to the fix point will be 0x3E4093C2 Note: For peak mode, 1-AE, must be defined by users and there is no limitation. For RMS mode, there is no need define the omega value.

DRC Formula

DRC Description	Equation
DRC_TH0: Threshold	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: –10dB, then convert –10 into fix point will be 0xC1200000. Example 2: –30dB, then convert –30 into fix point will be 0xC1F00000.
DRC RATIO: Compress ratio	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: 0.5, then convert 0.5 into fix point will be 0x3F000000. Example 2: 0, then convert 0 into fix point will be 0x00000000.
DRC MAKEUP: Make up gain	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: 5dB, then convert 5 into fix point will be 0x40A00000. Example 2: 6dB, then convert 6 into fix point will be 0x40C00000.

Peak Mode RMS Mode

Block Diagram and Description
→The detecting threshold using different calculated methods. Peak mode: AE and 1-AE is independent RMS mode: AE + (1-AE) = 1



Address	BITS	Name	Description
0xC48	28	DRC4_PEAK	1: Peak mode 0 : RMS mode (default)
	27	DRC3_PEAK	1: Peak mode 0 : RMS mode (default)
	26	DRC2_PEAK	1: Peak mode 0 : RMS mode (default)
	25	DRC1_PEAK	1: Peak mode 0 : RMS mode (default)

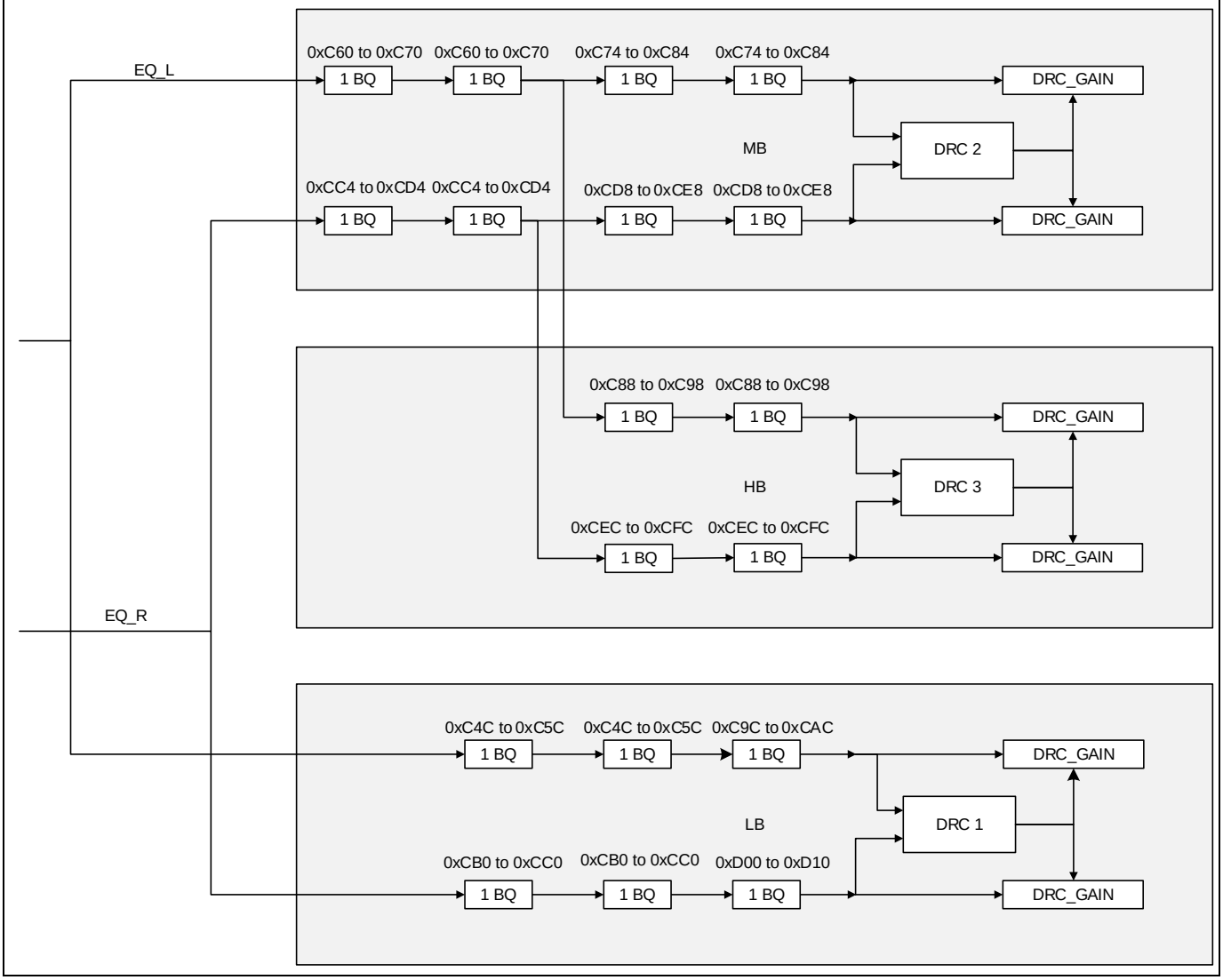
DRC Enable

Address	BITS	Name	Description
0xC48	24	DRC4_ON	DRC4 Enable (Final DRC) 1: Enable 0: Disable (default) →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC4)
	23	DRC3_ON	DRC3 Enable (H band) 1: Enable 0: Disable (default) →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC3)
	22	DRC2_ON	DRC2 Enable (M band) 1: Enable 0: Disable (default) →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC2)
	21	DRC1_ON	DRC1 Enable (L_band) 1: Enable 0: Disable (default) →When disable, input signal is the same as output signal. →Final Stage DRC enable (DRC1)

Multi Band DRC EQ

Block Diagram and Description

→To adjust the cut off frequency of the DRC1, 2, 3



DRC_EQ Link

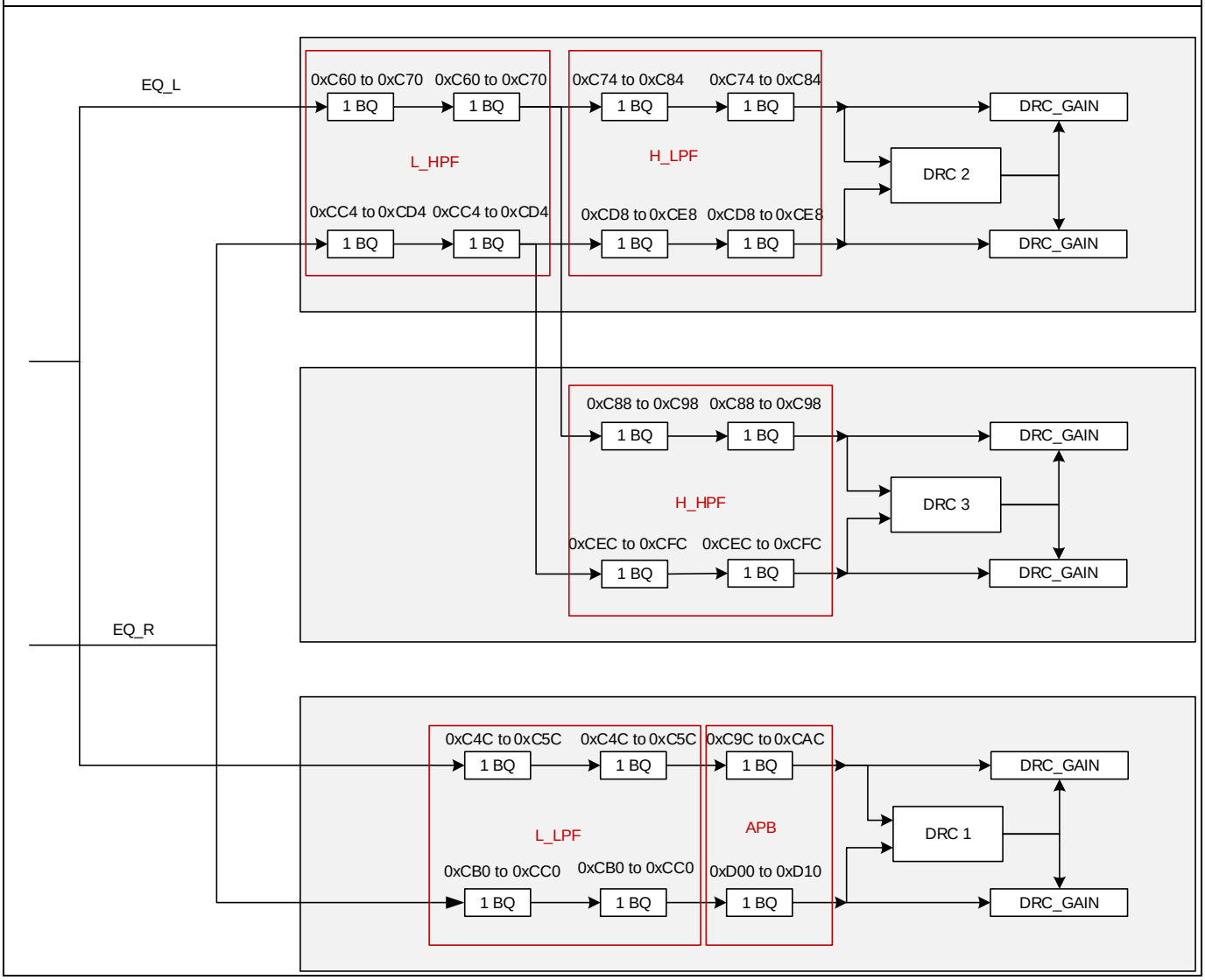
Address	BITS	Name	Description
0x14	15	DRC_EQ_LINK	0: DRC slpit frequency EQ coef independent (default) 1: DRC slpit frequency EQ CH2 coef = CH1

DRC_EQ Coefficient

Address	BITS	Name	Description
0xC4C to D10	31:0	LB_CH1_BQ1_B0	Low Band Ch1 BQ1 B0
	. . .		
	31:0	LB_CH2_BQ2_A2	Low Band Ch2 BQ2 A2

MBDRC First Order Setting

Block Diagram and Description



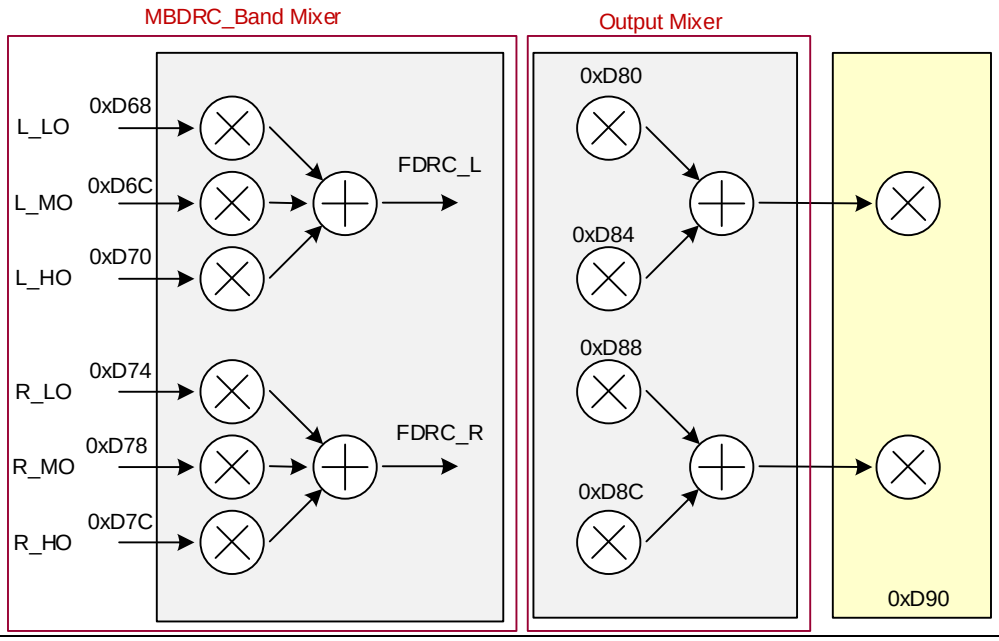
Address	BITS	Name	Description
0xC48	13	SKIP_BQ1_L_MBAND	(register 0xC60) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	12	SKIP_BQ2_L_MBAND	(register 0xC74) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	11	SKIP_BQ1_R_MBAND	(register 0xCC4) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	10	SKIP_BQ2_R_MBAND	(register 0xCD8) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	9	SKIP_BQ1_L_HBAND	(register 0xC88) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	8	SKIP_BQ1_R_HBAND	(register 0xCEC) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	7	SKIP_BQ1_L_LBAND	(register 0xC4C) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped
	6	SKIP_BQ1_R_LBAND	(register 0xCB0) 0: Coefficients applied to 2 identical BQ stages (default) 1: Coefficients applied to 1 stage only, 1 is skipped

DRC Filter Bypass

Address	BITS	Name	Description
0xC48	5	SKIP_DRC_L_HPF	L_HPF for MB and HB DRC 0: Normal mode (default) 1: SKIP
	4	SKIP_DRC_H_LPF	H_LPF for MB DRC 0: Normal mode (default) 1: SKIP
	3	SKIP_DRC_H_HPF	H_HPF for HB DRC 0: Normal mode (default) 1: SKIP
	2	SKIP_DRC_L_LPF	L_LPF for LB DRC 0: Normal mode (default) 1: SKIP
	1	SKIP_DRC_APB	APB for LB DRC 0: Normal mode (default) 1: SKIP

MBDRC/Output Mixer

Block Diagram and Description



Address	BITS	Name	Description
D68	31:0	CH1_OUT_MIX_L	Ch1 L band output mixer
D6C	31:0	CH1_OUT_MIX_M	Ch1 M band output mixer
D70	31:0	CH1_OUT_MIX_H	Ch1 H band output mixer
D74	31:0	CH2_OUT_MIX_L	Ch2 L band output mixer
D78	31:0	CH2_OUT_MIX_M	Ch2 M band output mixer
D7C	31:0	CH2_OUT_MIX_H	Ch2 H band output mixer
D80	31:0	CH1_OUT_MIX_0	Ch1 1 Output Mixer 0 Note: Default signal flow is from CH1_OUT_MIX_0
D84	31:0	CH1_OUT_MIX_1	Ch1 1 Output Mixer 1
D88	31:0	CH2_OUT_MIX_0	Ch2 1 Output Mixer 0
D8C	31:0	CH2_OUT_MIX_1	Ch2 1 Output Mixer 1 Note: Default signal is flow from CH2_OUT_MIX_1

Output/MBDRC Mixer Gain Setting

Address	BITS	Name	Equation
0xD68 to 0xD8C	31:0	mix_1[31:0] mix_0[31:0]	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: −6dB = 0.5011872336, then convert 0.5011872336 into fix point will be 0x3F004DCE. Example 2: 0dB = 1, then convert 1 into fix point will be 0x3F800000.

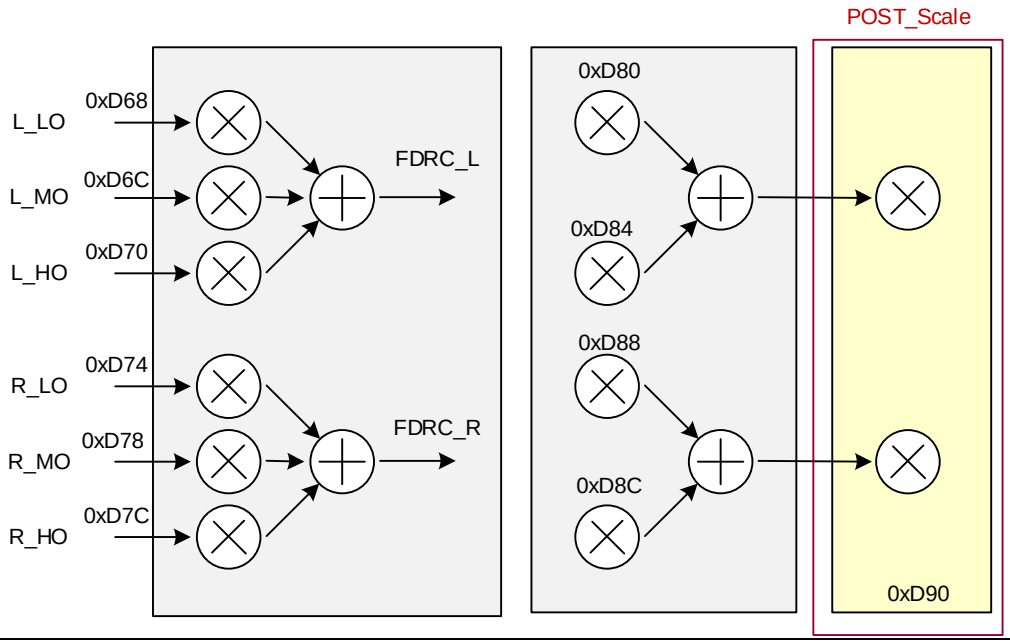
Mixer Inverse Phase Setting

Address	BITS	Name	Equation
0xD68 to 0xD8C	31:0	mix_1[31:0] mix_0[31:0]	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: 6dB = −0.5011872336, then convert -0.5011872336 into fix point will be 0xBF004DCE. Example 2: 0dB = −1, then convert -1 into fix point will be 0xBF800000.

Post-Scale

Block Diagram & Description

→The gain stage after output mixer

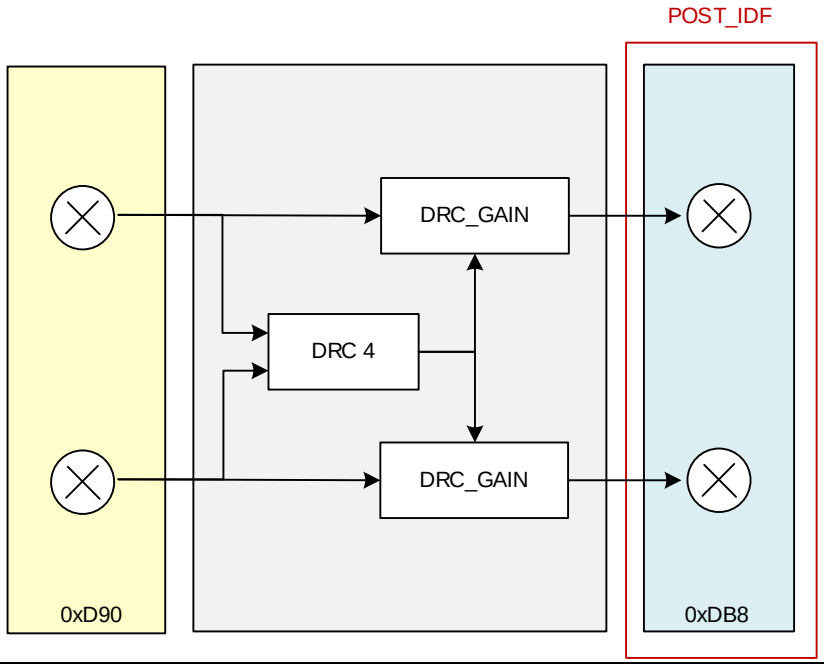


Address	BITS	Name	Equation
0xD90	31:0	POST_SCALE	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: –6dB = 0.5011872336, then convert 0.5011872336 into fix point will be 0x3F004DCE. Example 2: 6dB = 1.995262314, then convert 1.995262314 into fix point will be 0x3FFF64C1.

POST_IDF

Block Diagram and Description

→The gain stage after DRC 4



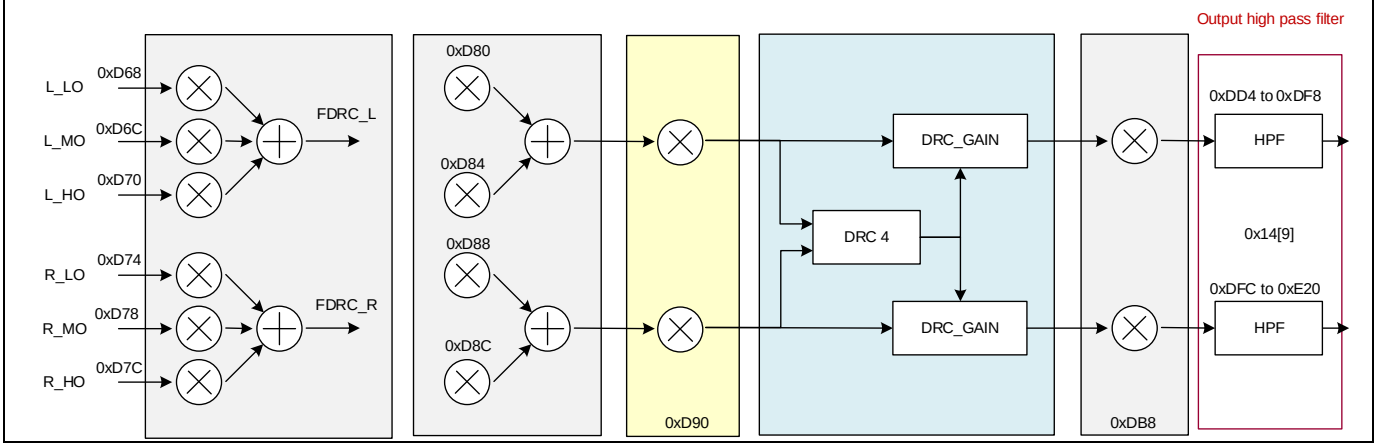
POST_IDF Gain

Address	BITS	Name	Equation
0xDB8	31:0	POST_IDF	Equation: Please use **IEEE-754 Floating Point Converter** to convert the floating point to fix point. Example 1: –6dB = 0.5011872336, then convert 0.5011872336 into fix point will be 0x3F004DCE. Example 2: 6dB = 1.995262314, then convert 1.995262314 into fix point will be 0x3FFF64C1.

Output High Pass Filter

Block Diagram & Description

→There are DC-Cut filter for each channel. The cut off frequency is 1.5Hz



Output HPF Control Function

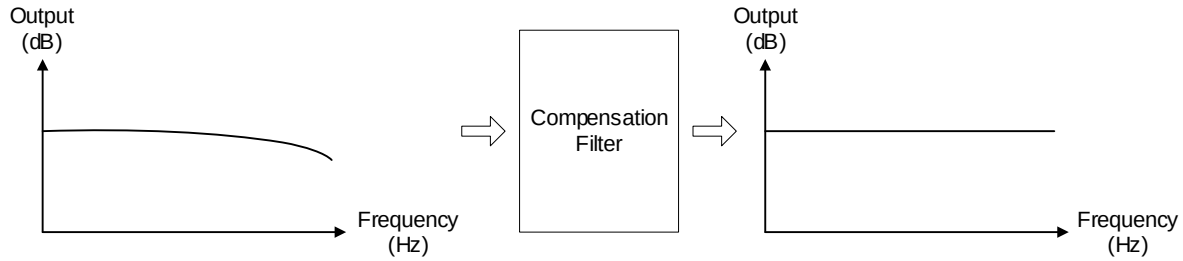
Address	BITS	Name	Description
0x14	9	HPF_POS_EN	1: Post high-pass filter enable 0: Post high-pass filter disable (default)

Output HPF EQ Coefficient

Address	BITS	Name	Description
0xDD4 to 0xDF8	31:0	Ch1 HPF1 B0 to Ch1 HPF2 A2	Ch1 Output HPF coefficient
0xDFC to 0xE20	31:0	Ch2 HPF1 B0 to Ch2 HPF2 A2	Ch2 Output HPF coefficient

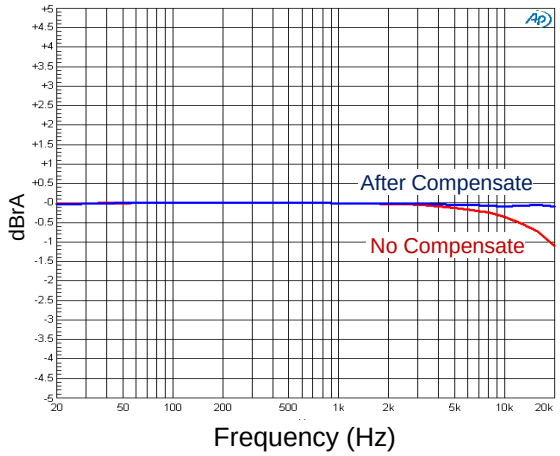
Compensate Filter

Compensation filter is purpose to compensate internal gain from DAC, this filter can also compensate the frequency response affected by LC filter, recommended setting will based on different application circuit to fit the curve



Compensate Description	Equation
Compensate	y[n] = B3* x [n-6] + B2* x [n-5] + B1* x [n-4] + B0* x [n-3] + B1* x [n-2] + B2* x [n-1] + B3* x [n] B0, B1, B2, B3: Compensate coefficient N: Input signal when applied

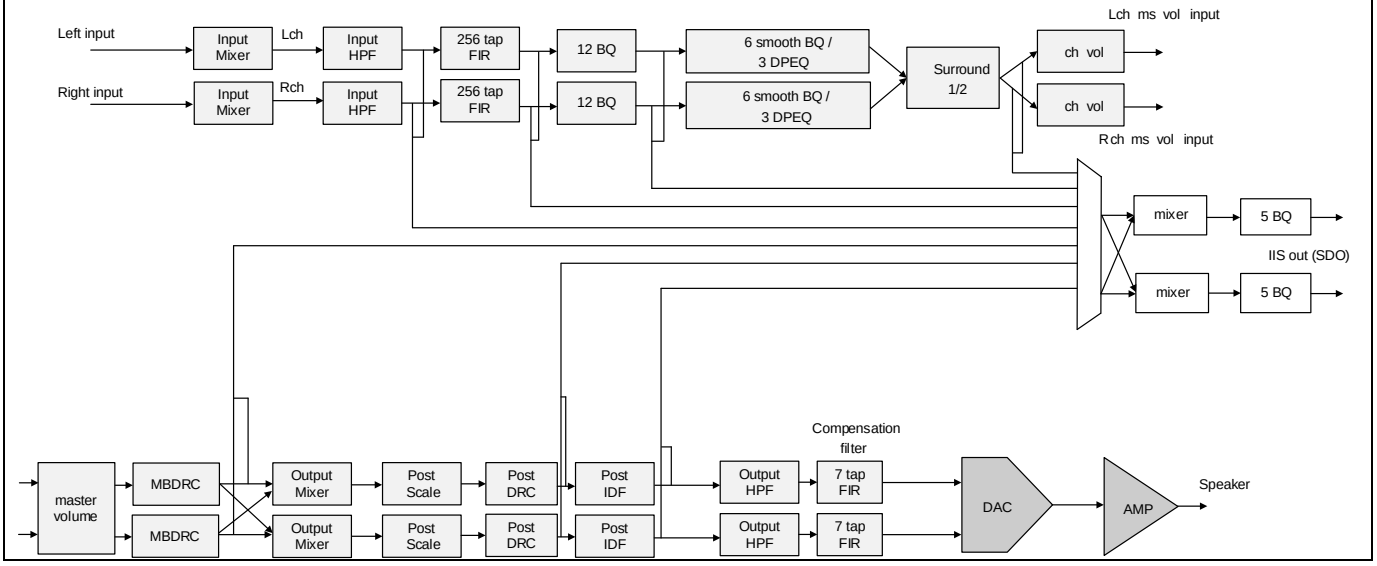
Address	BITS	Name	Description
0x14	1	COMP_EN	1: Compensation filter enable 0: Compensation filter disable (default)
DBC	31:0	COMP_B0	Compensate B0, B1, B2, and B3 coefficient
DC0	31:0	COMP_B1	
DC4	31:0	COMP_B2	
DC8	31:0	COMP_B3	



Data Output

Block Diagram and Description

→The RT9121 has SDO output which can configure signal output after processor
→The SDO output consist output mixer, and 5 Bi-Quad, which can be used for sub woofer application.



SDO Control Function

Address	BITS	Name	Description
0x14	30:28	SDO_SEL	0000:IN HPF (default) 0001: FIR 0010: EQ 0011: Smooth/Dynamic EQ 0100: Surround 0101 MBDRC 0110: PostDRC 0111: Post IDF 1111 and others: Reserved

SDO Output Mixer Control

Address	BITS	Name	Description
E24	31:0	SDO1_OUT_MIX_1	Ch1 SDO output mixer 1 Note: Default signal is from Ch1 SDO output mixer 1
E28	31:0	SDO1_OUT_MIX_0	Ch1 SDO output mixer 0
E2C	31:0	SDO2_OUT_MIX_1	Ch2 SDO output mixer 1
E30	31:0	SDO2_OUT_MIX_0	Ch2 SDO output mixer 0 Note: Default signal is from Ch2 SDO output mixer 0

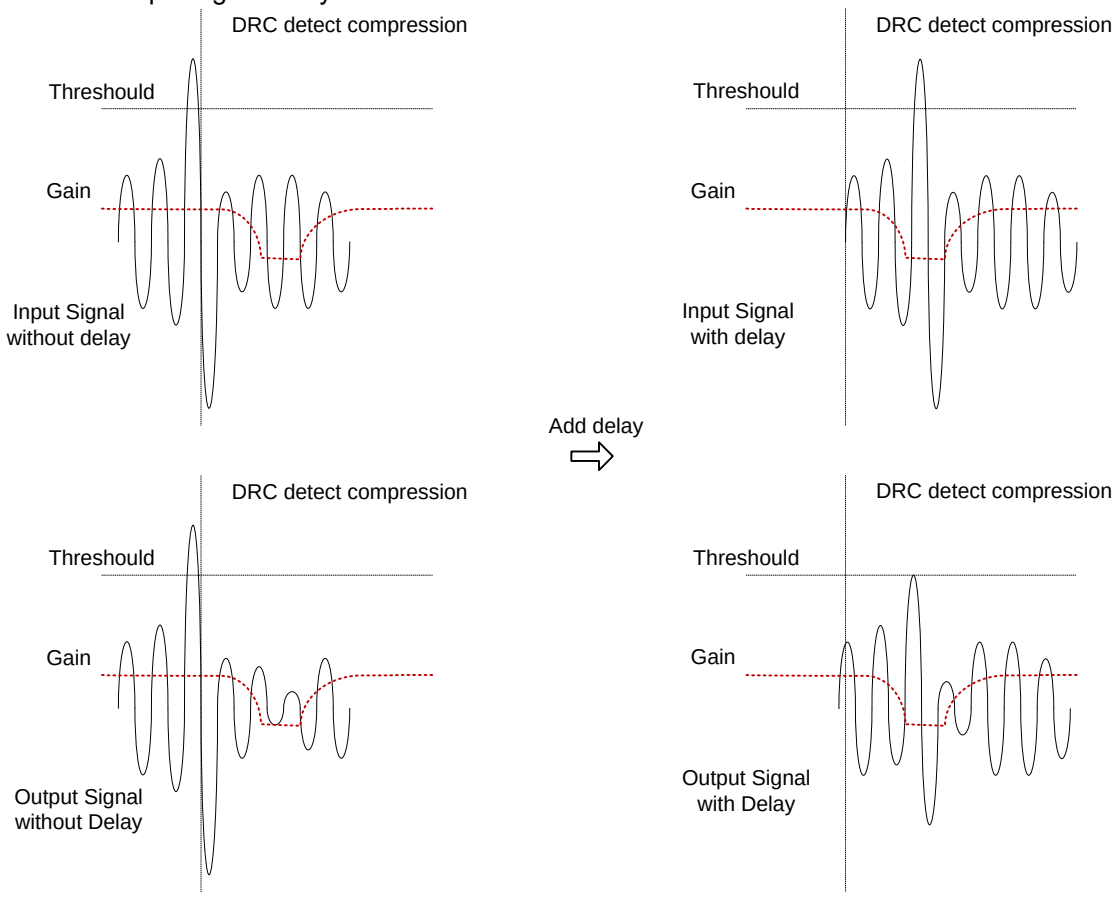
SDO EQ Coefficient

Address	BITS	Name	Description
E34	31:0	SDO1_BQ1_B0	Ch1 SDO BQ 1 coefficient BO
		. . .	
EF8	31:0	SDO2_BQ5_A2	Ch2 SDO BQ 5 coefficient A2

DRC4 is final stage of DRC. It can be configured as the final DRC to limit the output power.

Block Diagram and Description

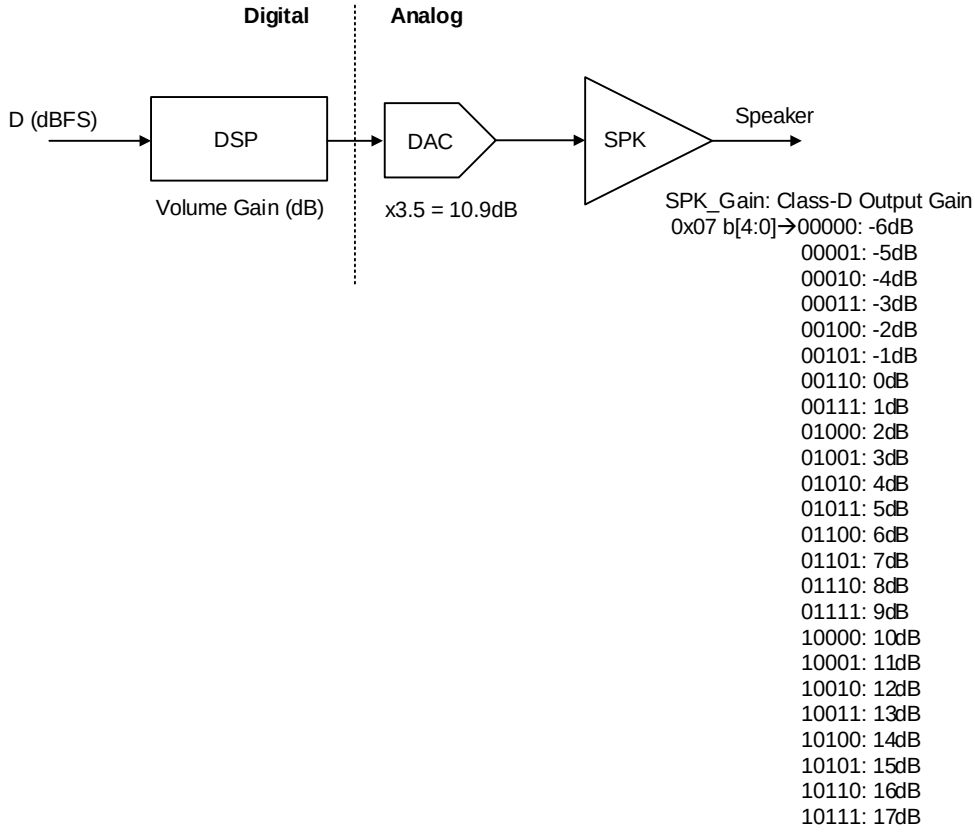
→ Make the audio output signal lately.



Delay = (DRC4_Delay)*1 / Sample rate

Address	BITS	Name	Description
0xD98	31:0	DRC4_DELAY	DRC4_DELAY →The delay make the audio signal output delay

Amplification Gain



Address	BITS	Name	Description
0x07	4:0	D_SPK_GAIN[4:0]	Class-D output gain 00000: –6dB 00001: –5dB 00010: –4dB 00011: –3dB 00100: –2dB 00101: –1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010:12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 6dB 10111: 17dB

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

I²C Bus Specification

The RT9121 supports the I²C protocol via the input ports SCL and SDA. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The RT9121 is always a slave device in all of its communications. It can operate at up to 400kb/s.

Communication Protocol

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition. START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer. STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the RT9121 and the bus master. During the data input, the RT9121 samples the SDA signal on the rising edge of clock SCL. For correct device operation, the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

Boost Capacitor Selection

For the large power output, and low frequency, the boost capacitor can be chosen from 0.47μF to 1μF. Reference value can refer to Table 1.

Table 1. Boost Capacitor Select Table

Test Condition	Capacitor Value
PVDD = 24V, R = 8Ω, Output Power > 2x25W, 20Hz, BTL Mode	1μF
PVDD = 24V, R = 4Ω, Output Power > 2x20W, 20Hz, BTL Mode	0.47μF
PVDD = 24V, R = 4Ω, Output Power > 60W, 20Hz, PBTL Mode	1μF
PVDD = 24V, R = 8Ω, Output Power > 35W, 20Hz, PBTL Mode	1μF

Device Addressing

The RT9121 Support I²C Control interface. When A_SEL1 = low and A_SEL2 = low. A_SEL will latch from the power-on or software reset, then define the address depends on the low, or high. The address configuration can refer to Table 2.

Table 2. Address Select Table

A_SEL2	A_SEL1	Device Address
High	High	0x37
High	Low	0x36
Low	High	0x35
Low	Low	0x34

I²C Write Control

Following the START condition, the master sends a device select code with the RW bit set to 0. The RT9121 acknowledges this and the writes for the byte of internal address. After receiving the internal byte address, the RT9121 again responds with an acknowledgement.

I²C Read Control

Following the START condition the master sends a device select code with the RW bit set to 1. The RT9121 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

Speaker Inductance and Schottky Diode Adding

If need to operate the RT9121 to reach the OCP value (minimum OCP SPEC is 6A) and using 4Ω or under 4Ω impedance speaker, the speaker inductance will be needed to consider like Table 3 list, if speaker inductance is over Table 3 list, please added Schottky diode to the AMP.

Table 3. Speaker Inductance Range

PVDD	Speaker Impedance	Max Application Current	Voice Coil Inductance Without Schottky Diode
≤26.4V	≥4Ω	<6A$_{peak}$	No need
≤26.4V	≥4Ω	≥6A$_{peak}$	<80μH

Note 1: The reverse current will through to the AMP due to the speaker inductance, lager inductance through much more. So the Schottky diode will be added to prevent large reverse current to cause any serious problem while operating to reach OCP value.

Note 2: Example 1, if speaker impedance is 4Ω, and speaker inductance is 140μH, need to operate above 72W$_{peak}$, the diode will be needed to add.

Example 2, if speaker impedance is 4Ω, and speaker inductance is 50μH, need to operate above72W$_{peak}$, the diode will no needed to add.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-48L 6x6 package, the thermal resistance, θ_{JA}, is 22.3°C/W on a standard JEDEC 51-7 high effective- thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (150°C - 25°C) / (22.3°C/W) = 5.6W for a VQFN-48L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

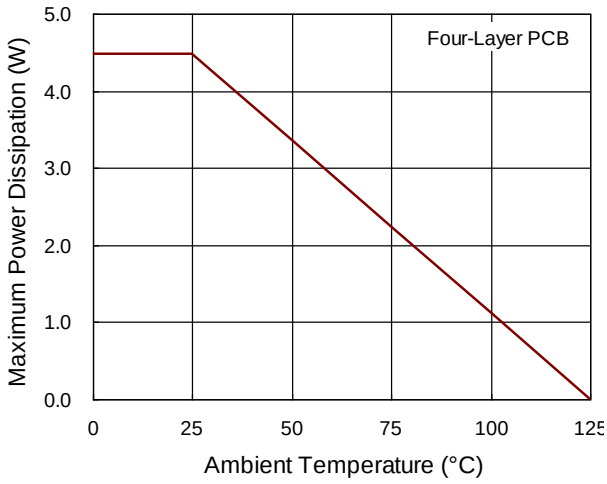
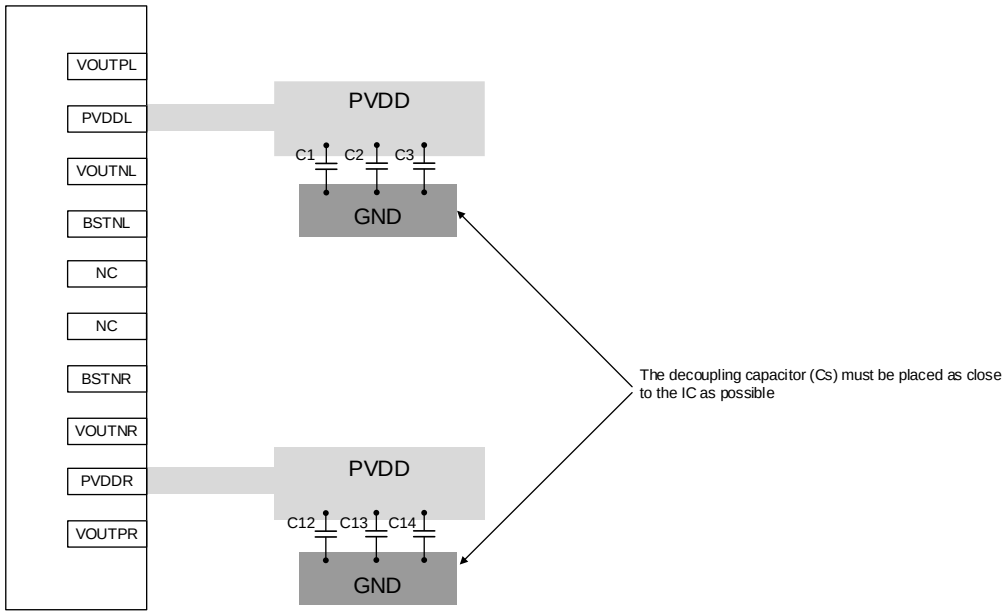


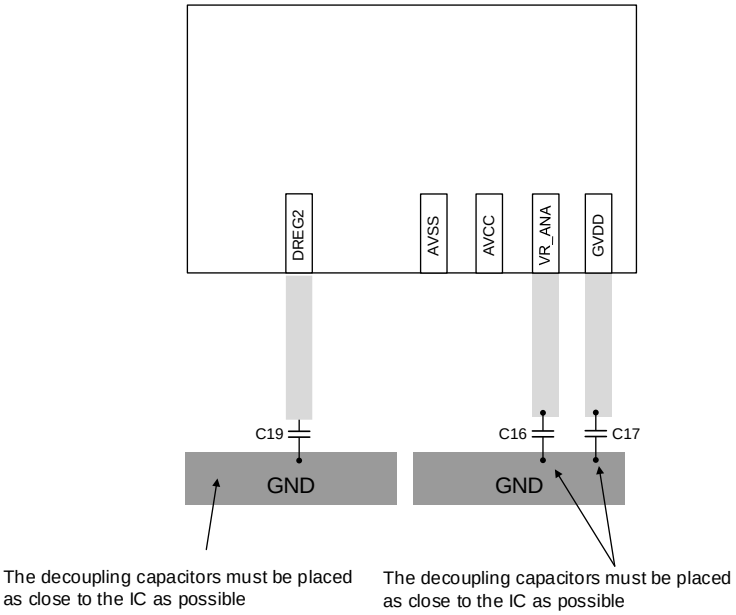
Figure 4. Derating Curve of Maximum Power Dissipation

Layout Guide

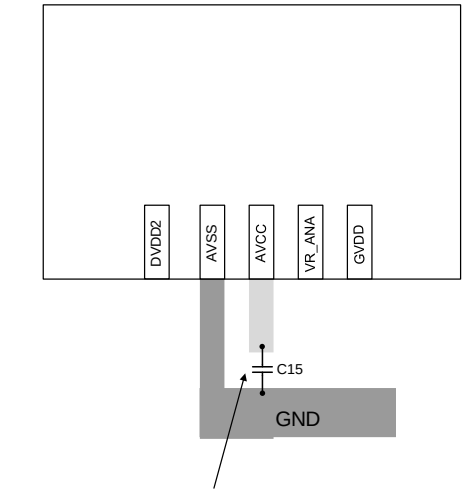
Place the decoupling capacitors as close as possible to the PVCC and GND, then use shortest trace to link these capacitors, and use more vias for GND link to GND layer to reduce parasitic inductance and resistance. The trace width is 30mil at least.



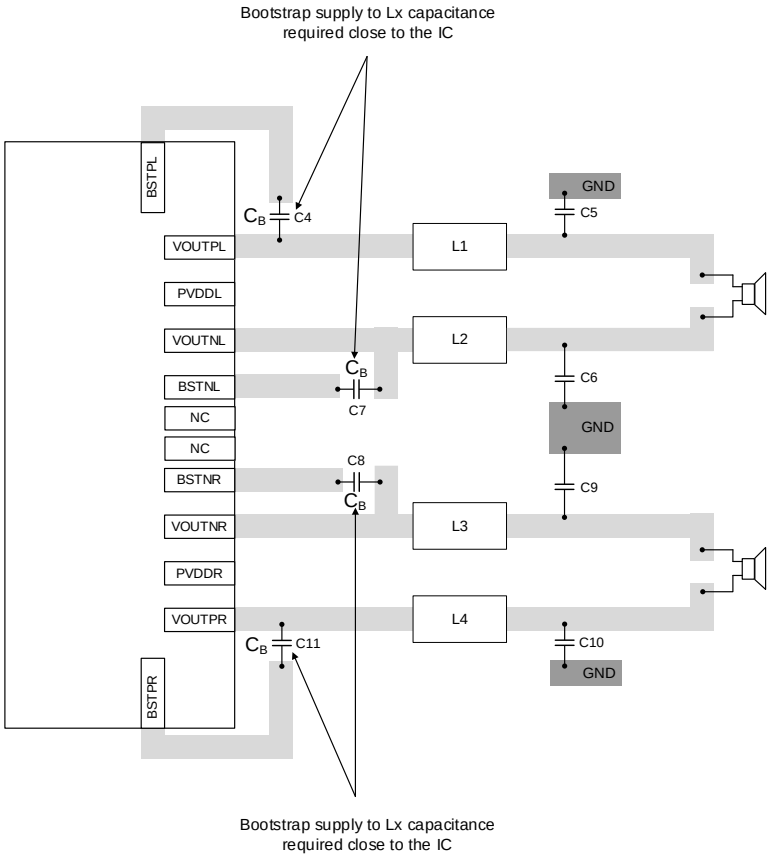
The DREG2 VR_ANA and GVDD decoupling capacitors must be placed as close to the IC as possible.



Place the decoupling capacitors as close as possible to the AVCC and AVSS Pin for achieving good audio quality, the trace width of AVCC is 30mil at least.



The traces of VOUTPL VOUTNL VOUTPR and VOUTNR should be kept equal width and length respectively and Bootstrap supply to Lx capacitance required close to the IC.



If possible, coplanar ground fill on both sides for differential pair of speaker out shielding.

Register Map

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x00	4	DSP_MODE	31:16	RW	Prohibit	Prohibit	16'b0000000100100000
			31:16	RW	Prohibit	Prohibit	16'b0000000100100000
			15:12	RW	Reserved	Reserved	14'b0011
			11:8	RW	I2C Master Freq	Set I^2C master SCL frequency (period = (sel + 2)*3*166ns) 0000: 1M (SCL period = 2*3*166ns = 996ns) ... 0011: 400k (SCL period = 5*3*166ns = 2490ns) (default) … 1111: 11.81k (SCL period = 17*3*166ns = 8466ns)	14'b0011
			7	RW	Reserved		0
			6	RW	Reserved		0
			5	RW	OUTPUT_FLOAT	Output format as floating point 0: Fixed point (default) 1: Floating Point	0
			4	RW	Prohibit		0
			3	RW	INPUT_FLOAT	Input Format as floating point 0: Fixed point (default) 1: Floating point	0
			2	RW	I2S EN	Enable I^2S data output	1'b1
			1:0	RW	DSP_MODE	Note: Filter and DRC coefficients are only updated when DSP is from inactive to active. 00: I^2S input CH0/CH1 bypass to DSP output 01: DSP output is all zero 10: DSP active (default) Others: Reserved	2'b10

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x04	4	I2S_FMT	31:28	RW	Reserved	Reserved	0x0000
			27:24	RW	i2s_dsp_ch_n	Audio channel enable per channel 0000: 1 L-ch and 1 R-ch (default) 0001: 2 L-ch and 2 R-ch … 1111: 16 L-ch and 16 R-ch	0x0000
			23:22	RW	Reserved	Reserved	0x00
			21:20	RW	i2s_dsp_aud_bit	Audio word length 00: 16 bits 01: 24bits 10: 32bits (default) Others: Reserved	0x10
			19	RW	i2s_dsp_tdm_en	0: Disable 1: Enable (default)	0x1
			18:16	RW	i2s_dsp_fmt	000: I^2S (default) 001: Left Justified 010: Right Justified 011: DSPM_A Others: DSPM_B	0x0
			15:12	RW	Reserved	Reserved	0x0000
			11:8	RW	i2s_dsp_ch_n	Audio channel enable per channel 0000: 1 L-ch and 1 R-ch(default) 0001: 2 L-ch and 2 R-ch … 1111: 16 L-ch and 16 R-ch	0x0
			7:6	RW	Reserved	Reserved	0x00
			5:4	RW	i2s_dsp_aud_bit	Audio word length 00: 16 bits 01: 24bits 10: 32bits (default)	0x10
			3	RW	i2s_dsp_tdm_en	0: Disable 1: Enable (default)	0x1
			2:0	RW	i2s_dsp_fmt	000: I^2S (default) 001: Left Justified 010: Right Justified 011: DSPM_A Others: DSPM_B	0x0
0x08	4	I2S_CH_EN	31:16	RW	i2s_dsp_ch_in_en_r	Channel enable for R channel serial data input bit 0: Enable channel 0 bit 1: Enable channel 1 (default) … bit 15: Enable channel 15	0x01
			15:0	RW	i2s_dsp_ch_in_en_l	Channel enable for L channel serial data input bit 0: Enable channel 0 bit 1: Enable channel 1 (default) … bit 15: Enable channel 15	0x01

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x0C	4	MS_VOL	31	RW	SKIP_RAMP	0: Ramp enable (default) 1: Skip ramp	0
			30:28	RW	VOL_RAMP_MODE	Volume slew step control 000: 1 step in every sample (default) 001: mute -> -40dB, every sample with 1 step. -40dB -> 24dB, 2 sample with 1 step. 010: mute -> -40dB, 2 sample with 1 step. -40dB -> 24dB, 4 sample with 1 step. Others: mute -> -40dB, 4 sample with 1 step. - 40dB -> 24dB, 8 sample with 1 step.	0x00
			10:0	RW	MS_VOL	24dB to −103.9375dB, 0.0625dB per step	0x180
0x10	4	CH_VOL	31	RW	CH1_MUTE	0: Un-mute (default) 1: Mute	0
			30:27	RW	Reserved	Reserved	
			26:16	RW	CH1_VOL	24dB to −103.9375dB, 0.0625dB per step	0x180
			15	RW	CH2_MUTE	0: Un-mute (default) 1: Mute	0
			14:11	RW	Reserved	Reserved	
			10:0	RW	CH2_VOL	24dB to −103.9375dB, 0.0625dB per step	0x180

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x14	4	DSP_FLTR_CTRL	31	RW	SDO_EN	0: Disable (default) 1: Enable	0
			30:28	RW	SDO_SEL	0000:IN HPF (default) 0001: FIR 0010: EQ 0011: Smooth/Dynamic EQ 0100: Surround 0101 MBDRC 0110: PostDRC 0111: Post IDF 1111 and others: Reserved	0
			27:16	RW	Reserved	Reserved	
			15	RW	DRC_EQ_LINK	0: DRC slpit frequency EQ coef independent (default) 1: DRC slpit frequency EQ CH2 coef = CH1	0
			14	RW	FIR_LINK	0: CH1/CH2 independent (default) 1: CH2 coefficient = CH1	0
			13	RW	EQ_LINK_ALL	EQ1 to EQ12 and SEQ1 to 8 coefficient link 0: CH1/CH2 independent (default) 1: Take CH1 coefficients for CH2	0
			12	RW	EQ_PART_LINK	EQ7 to EQ12 coefficient link When EQ_LINK_ALL = 1 0: Link all (default) 1: Link EQ7 to EQ12	0
			11	RW	SEQ_LINK	SEQ1 to SEQ8 or DPEQ1 to DPEQ3 coefficient link When EQ_LINK_ALL = 1 0: CH1/CH2 independent (default) 1: Link All (CH2 as CH1)	0
			10	RW	HPF_IN_EN	0: Bypass (default) 1: Enable	0
			9	RW	HPF_OUT_EN	0: Bypass (default) 1: Enable	0
			8	RW	FIR_EN	0: Bypass (default) 1: Enable	0
			7	RW	EQ_EN	0: Bypass(default) 1: Enable	0
			6	RW	SEQ_DPEQ_SEL	0: Smooth EQ (default) 1: Dynamic EQ	0
			5	RW	SEQ_DPEQ_EN	0: Bypass (default) 1: Enable	0
			4	RW	SURROUND_SEL	0: Spatialize (default) 1: CCS	0
			3	RW	SURROUND_EN	0: Bypass (default) 1: Enable	0
			2	RW	MBDRC_EN	0: Bypass(default) 1: Enable	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
			1	RW	COMP_EN	0: Bypass (default) 1: Enable	0
0x18	4	CH1_IN_MIX_0	31:0	RW	CH1_IN_MIX_0	Ch1 input mixer	0x3f800000
0x1C	4	CH1_IN_MIX_1	31:0	RW	CH1_IN_MIX_1	Ch1 input mixer	0
0x20	4	CH2_IN_MIX_0	31:0	RW	CH2_IN_MIX_0	Ch2 input mixer	0
0x24	4	CH2_IN_MIX_1	31:0	RW	CH2_IN_MIX_1	Ch2 input mixer	0x3f800000
0x28	4	CH1_IN_HPF_B0	31:0	RW	CH1_IN_HPF_B0	Filter Coefficient	0x3f800000
0x2C	4	CH1_IN_HPF_B1	31:0	RW	CH1_IN_HPF_B1	Filter Coefficient	0
0x30	4	CH1_IN_HPF_A1	31:0	RW	CH1_IN_HPF_A1	Filter Coefficient	0
0x34	4	CH2_IN_HPF_B0	31:0	RW	CH2_IN_HPF_B0	Filter Coefficient	0x3f800000
0x38	4	CH2_IN_HPF_B1	31:0	RW	CH2_IN_HPF_B1	Filter Coefficient	0
0x3C	4	CH2_IN_HPF_A1	31:0	RW	CH2_IN_HPF_A1	Filter Coefficient	0
0x40	4	CH1_FIR_TAP0	31:0	RW	CH1_FIR_TAP0	Filter Coefficient	0x3f800000
0x44	4	CH1_FIR_TAP1	31:0	RW	CH1_FIR_TAP1	Filter Coefficient	0
0x48	4	CH1_FIR_TAP2	31:0	RW	CH1_FIR_TAP2	Filter Coefficient	0
0x4C	4	CH1_FIR_TAP3	31:0	RW	CH1_FIR_TAP3	Filter Coefficient	0
0x50	4	CH1_FIR_TAP4	31:0	RW	CH1_FIR_TAP4	Filter Coefficient	0
0x54	4	CH1_FIR_TAP5	31:0	RW	CH1_FIR_TAP5	Filter Coefficient	0
0x58	4	CH1_FIR_TAP6	31:0	RW	CH1_FIR_TAP6	Filter Coefficient	0
0x5C	4	CH1_FIR_TAP7	31:0	RW	CH1_FIR_TAP7	Filter Coefficient	0
0x60	4	CH1_FIR_TAP8	31:0	RW	CH1_FIR_TAP8	Filter Coefficient	0
0x64	4	CH1_FIR_TAP9	31:0	RW	CH1_FIR_TAP9	Filter Coefficient	0
0x68	4	CH1_FIR_TAP10	31:0	RW	CH1_FIR_TAP10	Filter Coefficient	0
0x6C	4	CH1_FIR_TAP11	31:0	RW	CH1_FIR_TAP11	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x70	4	CH1_FIR_TAP12	31:0	RW	CH1_FIR_TAP12	Filter Coefficient	0
0x74	4	CH1_FIR_TAP13	31:0	RW	CH1_FIR_TAP13	Filter Coefficient	0
0x78	4	CH1_FIR_TAP14	31:0	RW	CH1_FIR_TAP14	Filter Coefficient	0
0x7C	4	CH1_FIR_TAP15	31:0	RW	CH1_FIR_TAP15	Filter Coefficient	0
0x80	4	CH1_FIR_TAP16	31:0	RW	CH1_FIR_TAP16	Filter Coefficient	0
0x84	4	CH1_FIR_TAP17	31:0	RW	CH1_FIR_TAP17	Filter Coefficient	0
0x88	4	CH1_FIR_TAP18	31:0	RW	CH1_FIR_TAP18	Filter Coefficient	0
0x8C	4	CH1_FIR_TAP19	31:0	RW	CH1_FIR_TAP19	Filter Coefficient	0
0x90	4	CH1_FIR_TAP20	31:0	RW	CH1_FIR_TAP20	Filter Coefficient	0
0x94	4	CH1_FIR_TAP21	31:0	RW	CH1_FIR_TAP21	Filter Coefficient	0
0x98	4	CH1_FIR_TAP22	31:0	RW	CH1_FIR_TAP22	Filter Coefficient	0
0x9C	4	CH1_FIR_TAP23	31:0	RW	CH1_FIR_TAP23	Filter Coefficient	0
0xA0	4	CH1_FIR_TAP24	31:0	RW	CH1_FIR_TAP24	Filter Coefficient	0
0xA4	4	CH1_FIR_TAP25	31:0	RW	CH1_FIR_TAP25	Filter Coefficient	0
0xA8	4	CH1_FIR_TAP26	31:0	RW	CH1_FIR_TAP26	Filter Coefficient	0
0xAC	4	CH1_FIR_TAP27	31:0	RW	CH1_FIR_TAP27	Filter Coefficient	0
0xB0	4	CH1_FIR_TAP28	31:0	RW	CH1_FIR_TAP28	Filter Coefficient	0
0xB4	4	CH1_FIR_TAP29	31:0	RW	CH1_FIR_TAP29	Filter Coefficient	0
0xB8	4	CH1_FIR_TAP30	31:0	RW	CH1_FIR_TAP30	Filter Coefficient	0
0xBC	4	CH1_FIR_TAP31	31:0	RW	CH1_FIR_TAP31	Filter Coefficient	0
0xC0	4	CH1_FIR_TAP32	31:0	RW	CH1_FIR_TAP32	Filter Coefficient	0
0xC4	4	CH1_FIR_TAP33	31:0	RW	CH1_FIR_TAP33	Filter Coefficient	0
0xC8	4	CH1_FIR_TAP34	31:0	RW	CH1_FIR_TAP34	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xCC	4	CH1_FIR_TAP35	31:0	RW	CH1_FIR_TAP35	Filter Coefficient	0
0xD0	4	CH1_FIR_TAP36	31:0	RW	CH1_FIR_TAP36	Filter Coefficient	0
0xD4	4	CH1_FIR_TAP37	31:0	RW	CH1_FIR_TAP37	Filter Coefficient	0
0xD8	4	CH1_FIR_TAP38	31:0	RW	CH1_FIR_TAP38	Filter Coefficient	0
0xDC	4	CH1_FIR_TAP39	31:0	RW	CH1_FIR_TAP39	Filter Coefficient	0
0xE0	4	CH1_FIR_TAP40	31:0	RW	CH1_FIR_TAP40	Filter Coefficient	0
0xE4	4	CH1_FIR_TAP41	31:0	RW	CH1_FIR_TAP41	Filter Coefficient	0
0xE8	4	CH1_FIR_TAP42	31:0	RW	CH1_FIR_TAP42	Filter Coefficient	0
0xEC	4	CH1_FIR_TAP43	31:0	RW	CH1_FIR_TAP43	Filter Coefficient	0
0xF0	4	CH1_FIR_TAP44	31:0	RW	CH1_FIR_TAP44	Filter Coefficient	0
0xF4	4	CH1_FIR_TAP45	31:0	RW	CH1_FIR_TAP45	Filter Coefficient	0
0xF8	4	CH1_FIR_TAP46	31:0	RW	CH1_FIR_TAP46	Filter Coefficient	0
0xFC	4	CH1_FIR_TAP47	31:0	RW	CH1_FIR_TAP47	Filter Coefficient	0
0x100	4	CH1_FIR_TAP48	31:0	RW	CH1_FIR_TAP48	Filter Coefficient	0
0x104	4	CH1_FIR_TAP49	31:0	RW	CH1_FIR_TAP49	Filter Coefficient	0
0x108	4	CH1_FIR_TAP50	31:0	RW	CH1_FIR_TAP50	Filter Coefficient	0
0x10C	4	CH1_FIR_TAP51	31:0	RW	CH1_FIR_TAP51	Filter Coefficient	0
0x110	4	CH1_FIR_TAP52	31:0	RW	CH1_FIR_TAP52	Filter Coefficient	0
0x114	4	CH1_FIR_TAP53	31:0	RW	CH1_FIR_TAP53	Filter Coefficient	0
0x118	4	CH1_FIR_TAP54	31:0	RW	CH1_FIR_TAP54	Filter Coefficient	0
0x11C	4	CH1_FIR_TAP55	31:0	RW	CH1_FIR_TAP55	Filter Coefficient	0
0x120	4	CH1_FIR_TAP56	31:0	RW	CH1_FIR_TAP56	Filter Coefficient	0
0x124	4	CH1_FIR_TAP57	31:0	RW	CH1_FIR_TAP57	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x128	4	CH1_FIR_TAP58	31:0	RW	CH1_FIR_TAP58	Filter Coefficient	0
0x12C	4	CH1_FIR_TAP59	31:0	RW	CH1_FIR_TAP59	Filter Coefficient	0
0x130	4	CH1_FIR_TAP60	31:0	RW	CH1_FIR_TAP60	Filter Coefficient	0
0x134	4	CH1_FIR_TAP61	31:0	RW	CH1_FIR_TAP61	Filter Coefficient	0
0x138	4	CH1_FIR_TAP62	31:0	RW	CH1_FIR_TAP62	Filter Coefficient	0
0x13C	4	CH1_FIR_TAP63	31:0	RW	CH1_FIR_TAP63	Filter Coefficient	0
0x140	4	CH1_FIR_TAP64	31:0	RW	CH1_FIR_TAP64	Filter Coefficient	0
0x144	4	CH1_FIR_TAP65	31:0	RW	CH1_FIR_TAP65	Filter Coefficient	0
0x148	4	CH1_FIR_TAP66	31:0	RW	CH1_FIR_TAP66	Filter Coefficient	0
0x14C	4	CH1_FIR_TAP67	31:0	RW	CH1_FIR_TAP67	Filter Coefficient	0
0x150	4	CH1_FIR_TAP68	31:0	RW	CH1_FIR_TAP68	Filter Coefficient	0
0x154	4	CH1_FIR_TAP69	31:0	RW	CH1_FIR_TAP69	Filter Coefficient	0
0x158	4	CH1_FIR_TAP70	31:0	RW	CH1_FIR_TAP70	Filter Coefficient	0
0x15C	4	CH1_FIR_TAP71	31:0	RW	CH1_FIR_TAP71	Filter Coefficient	0
0x160	4	CH1_FIR_TAP72	31:0	RW	CH1_FIR_TAP72	Filter Coefficient	0
0x164	4	CH1_FIR_TAP73	31:0	RW	CH1_FIR_TAP73	Filter Coefficient	0
0x168	4	CH1_FIR_TAP74	31:0	RW	CH1_FIR_TAP74	Filter Coefficient	0
0x16C	4	CH1_FIR_TAP75	31:0	RW	CH1_FIR_TAP75	Filter Coefficient	0
0x170	4	CH1_FIR_TAP76	31:0	RW	CH1_FIR_TAP76	Filter Coefficient	0
0x174	4	CH1_FIR_TAP77	31:0	RW	CH1_FIR_TAP77	Filter Coefficient	0
0x178	4	CH1_FIR_TAP78	31:0	RW	CH1_FIR_TAP78	Filter Coefficient	0
0x17C	4	CH1_FIR_TAP79	31:0	RW	CH1_FIR_TAP79	Filter Coefficient	0
0x180	4	CH1_FIR_TAP80	31:0	RW	CH1_FIR_TAP80	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x184	4	CH1_FIR_TAP81	31:0	RW	CH1_FIR_TAP81	Filter Coefficient	0
0x188	4	CH1_FIR_TAP82	31:0	RW	CH1_FIR_TAP82	Filter Coefficient	0
0x18C	4	CH1_FIR_TAP83	31:0	RW	CH1_FIR_TAP83	Filter Coefficient	0
0x190	4	CH1_FIR_TAP84	31:0	RW	CH1_FIR_TAP84	Filter Coefficient	0
0x194	4	CH1_FIR_TAP85	31:0	RW	CH1_FIR_TAP85	Filter Coefficient	0
0x198	4	CH1_FIR_TAP86	31:0	RW	CH1_FIR_TAP86	Filter Coefficient	0
0x19C	4	CH1_FIR_TAP87	31:0	RW	CH1_FIR_TAP87	Filter Coefficient	0
0x1A0	4	CH1_FIR_TAP88	31:0	RW	CH1_FIR_TAP88	Filter Coefficient	0
0x1A4	4	CH1_FIR_TAP89	31:0	RW	CH1_FIR_TAP89	Filter Coefficient	0
0x1A8	4	CH1_FIR_TAP90	31:0	RW	CH1_FIR_TAP90	Filter Coefficient	0
0x1AC	4	CH1_FIR_TAP91	31:0	RW	CH1_FIR_TAP91	Filter Coefficient	0
0x1B0	4	CH1_FIR_TAP92	31:0	RW	CH1_FIR_TAP92	Filter Coefficient	0
0x1B4	4	CH1_FIR_TAP93	31:0	RW	CH1_FIR_TAP93	Filter Coefficient	0
0x1B8	4	CH1_FIR_TAP94	31:0	RW	CH1_FIR_TAP94	Filter Coefficient	0
0x1BC	4	CH1_FIR_TAP95	31:0	RW	CH1_FIR_TAP95	Filter Coefficient	0
0x1C0	4	CH1_FIR_TAP96	31:0	RW	CH1_FIR_TAP96	Filter Coefficient	0
0x1C4	4	CH1_FIR_TAP97	31:0	RW	CH1_FIR_TAP97	Filter Coefficient	0
0x1C8	4	CH1_FIR_TAP98	31:0	RW	CH1_FIR_TAP98	Filter Coefficient	0
0x1CC	4	CH1_FIR_TAP99	31:0	RW	CH1_FIR_TAP99	Filter Coefficient	0
0x1D0	4	CH1_FIR_TAP100	31:0	RW	CH1_FIR_TAP100	Filter Coefficient	0
0x1D4	4	CH1_FIR_TAP101	31:0	RW	CH1_FIR_TAP101	Filter Coefficient	0
0x1D8	4	CH1_FIR_TAP102	31:0	RW	CH1_FIR_TAP102	Filter Coefficient	0
0x1DC	4	CH1_FIR_TAP103	31:0	RW	CH1_FIR_TAP103	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x1E0	4	CH1_FIR_TAP104	31:0	RW	CH1_FIR_TAP104	Filter Coefficient	0
0x1E4	4	CH1_FIR_TAP105	31:0	RW	CH1_FIR_TAP105	Filter Coefficient	0
0x1E8	4	CH1_FIR_TAP106	31:0	RW	CH1_FIR_TAP106	Filter Coefficient	0
0x1EC	4	CH1_FIR_TAP107	31:0	RW	CH1_FIR_TAP107	Filter Coefficient	0
0x1F0	4	CH1_FIR_TAP108	31:0	RW	CH1_FIR_TAP108	Filter Coefficient	0
0x1F4	4	CH1_FIR_TAP109	31:0	RW	CH1_FIR_TAP109	Filter Coefficient	0
0x1F8	4	CH1_FIR_TAP110	31:0	RW	CH1_FIR_TAP110	Filter Coefficient	0
0x1FC	4	CH1_FIR_TAP111	31:0	RW	CH1_FIR_TAP111	Filter Coefficient	0
0x200	4	CH1_FIR_TAP112	31:0	RW	CH1_FIR_TAP112	Filter Coefficient	0
0x204	4	CH1_FIR_TAP113	31:0	RW	CH1_FIR_TAP113	Filter Coefficient	0
0x208	4	CH1_FIR_TAP114	31:0	RW	CH1_FIR_TAP114	Filter Coefficient	0
0x20C	4	CH1_FIR_TAP115	31:0	RW	CH1_FIR_TAP115	Filter Coefficient	0
0x210	4	CH1_FIR_TAP116	31:0	RW	CH1_FIR_TAP116	Filter Coefficient	0
0x214	4	CH1_FIR_TAP117	31:0	RW	CH1_FIR_TAP117	Filter Coefficient	0
0x218	4	CH1_FIR_TAP118	31:0	RW	CH1_FIR_TAP118	Filter Coefficient	0
0x21C	4	CH1_FIR_TAP119	31:0	RW	CH1_FIR_TAP119	Filter Coefficient	0
0x220	4	CH1_FIR_TAP120	31:0	RW	CH1_FIR_TAP120	Filter Coefficient	0
0x224	4	CH1_FIR_TAP121	31:0	RW	CH1_FIR_TAP121	Filter Coefficient	0
0x228	4	CH1_FIR_TAP122	31:0	RW	CH1_FIR_TAP122	Filter Coefficient	0
0x22C	4	CH1_FIR_TAP123	31:0	RW	CH1_FIR_TAP123	Filter Coefficient	0
0x230	4	CH1_FIR_TAP124	31:0	RW	CH1_FIR_TAP124	Filter Coefficient	0
0x234	4	CH1_FIR_TAP125	31:0	RW	CH1_FIR_TAP125	Filter Coefficient	0
0x238	4	CH1_FIR_TAP126	31:0	RW	CH1_FIR_TAP126	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x23C	4	CH1_FIR_TAP127	31:0	RW	CH1_FIR_TAP127	Filter Coefficient	0
0x240	4	CH1_FIR_TAP128	31:0	RW	CH1_FIR_TAP128	Filter Coefficient	0
0x244	4	CH1_FIR_TAP129	31:0	RW	CH1_FIR_TAP129	Filter Coefficient	0
0x248	4	CH1_FIR_TAP130	31:0	RW	CH1_FIR_TAP130	Filter Coefficient	0
0x24C	4	CH1_FIR_TAP131	31:0	RW	CH1_FIR_TAP131	Filter Coefficient	0
0x250	4	CH1_FIR_TAP132	31:0	RW	CH1_FIR_TAP132	Filter Coefficient	0
0x254	4	CH1_FIR_TAP133	31:0	RW	CH1_FIR_TAP133	Filter Coefficient	0
0x258	4	CH1_FIR_TAP134	31:0	RW	CH1_FIR_TAP134	Filter Coefficient	0
0x25C	4	CH1_FIR_TAP135	31:0	RW	CH1_FIR_TAP135	Filter Coefficient	0
0x260	4	CH1_FIR_TAP136	31:0	RW	CH1_FIR_TAP136	Filter Coefficient	0
0x264	4	CH1_FIR_TAP137	31:0	RW	CH1_FIR_TAP137	Filter Coefficient	0
0x268	4	CH1_FIR_TAP138	31:0	RW	CH1_FIR_TAP138	Filter Coefficient	0
0x26C	4	CH1_FIR_TAP139	31:0	RW	CH1_FIR_TAP139	Filter Coefficient	0
0x270	4	CH1_FIR_TAP140	31:0	RW	CH1_FIR_TAP140	Filter Coefficient	0
0x274	4	CH1_FIR_TAP141	31:0	RW	CH1_FIR_TAP141	Filter Coefficient	0
0x278	4	CH1_FIR_TAP142	31:0	RW	CH1_FIR_TAP142	Filter Coefficient	0
0x27C	4	CH1_FIR_TAP143	31:0	RW	CH1_FIR_TAP143	Filter Coefficient	0
0x280	4	CH1_FIR_TAP144	31:0	RW	CH1_FIR_TAP144	Filter Coefficient	0
0x284	4	CH1_FIR_TAP145	31:0	RW	CH1_FIR_TAP145	Filter Coefficient	0
0x288	4	CH1_FIR_TAP146	31:0	RW	CH1_FIR_TAP146	Filter Coefficient	0
0x28C	4	CH1_FIR_TAP147	31:0	RW	CH1_FIR_TAP147	Filter Coefficient	0
0x290	4	CH1_FIR_TAP148	31:0	RW	CH1_FIR_TAP148	Filter Coefficient	0
0x294	4	CH1_FIR_TAP149	31:0	RW	CH1_FIR_TAP149	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x298	4	CH1_FIR_TAP150	31:0	RW	CH1_FIR_TAP150	Filter Coefficient	0
0x29C	4	CH1_FIR_TAP151	31:0	RW	CH1_FIR_TAP151	Filter Coefficient	0
0x2A0	4	CH1_FIR_TAP152	31:0	RW	CH1_FIR_TAP152	Filter Coefficient	0
0x2A4	4	CH1_FIR_TAP153	31:0	RW	CH1_FIR_TAP153	Filter Coefficient	0
0x2A8	4	CH1_FIR_TAP154	31:0	RW	CH1_FIR_TAP154	Filter Coefficient	0
0x2AC	4	CH1_FIR_TAP155	31:0	RW	CH1_FIR_TAP155	Filter Coefficient	0
0x2B0	4	CH1_FIR_TAP156	31:0	RW	CH1_FIR_TAP156	Filter Coefficient	0
0x2B4	4	CH1_FIR_TAP157	31:0	RW	CH1_FIR_TAP157	Filter Coefficient	0
0x2B8	4	CH1_FIR_TAP158	31:0	RW	CH1_FIR_TAP158	Filter Coefficient	0
0x2BC	4	CH1_FIR_TAP159	31:0	RW	CH1_FIR_TAP159	Filter Coefficient	0
0x2C0	4	CH1_FIR_TAP160	31:0	RW	CH1_FIR_TAP160	Filter Coefficient	0
0x2C4	4	CH1_FIR_TAP161	31:0	RW	CH1_FIR_TAP161	Filter Coefficient	0
0x2C8	4	CH1_FIR_TAP162	31:0	RW	CH1_FIR_TAP162	Filter Coefficient	0
0x2CC	4	CH1_FIR_TAP163	31:0	RW	CH1_FIR_TAP163	Filter Coefficient	0
0x2D0	4	CH1_FIR_TAP164	31:0	RW	CH1_FIR_TAP164	Filter Coefficient	0
0x2D4	4	CH1_FIR_TAP165	31:0	RW	CH1_FIR_TAP165	Filter Coefficient	0
0x2D8	4	CH1_FIR_TAP166	31:0	RW	CH1_FIR_TAP166	Filter Coefficient	0
0x2DC	4	CH1_FIR_TAP167	31:0	RW	CH1_FIR_TAP167	Filter Coefficient	0
0x2E0	4	CH1_FIR_TAP168	31:0	RW	CH1_FIR_TAP168	Filter Coefficient	0
0x2E4	4	CH1_FIR_TAP169	31:0	RW	CH1_FIR_TAP169	Filter Coefficient	0
0x2E8	4	CH1_FIR_TAP170	31:0	RW	CH1_FIR_TAP170	Filter Coefficient	0
0x2EC	4	CH1_FIR_TAP171	31:0	RW	CH1_FIR_TAP171	Filter Coefficient	0
0x2F0	4	CH1_FIR_TAP172	31:0	RW	CH1_FIR_TAP172	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x2F4	4	CH1_FIR_TAP173	31:0	RW	CH1_FIR_TAP173	Filter Coefficient	0
0x2F8	4	CH1_FIR_TAP174	31:0	RW	CH1_FIR_TAP174	Filter Coefficient	0
0x2FC	4	CH1_FIR_TAP175	31:0	RW	CH1_FIR_TAP175	Filter Coefficient	0
0x300	4	CH1_FIR_TAP176	31:0	RW	CH1_FIR_TAP176	Filter Coefficient	0
0x304	4	CH1_FIR_TAP177	31:0	RW	CH1_FIR_TAP177	Filter Coefficient	0
0x308	4	CH1_FIR_TAP178	31:0	RW	CH1_FIR_TAP178	Filter Coefficient	0
0x30C	4	CH1_FIR_TAP179	31:0	RW	CH1_FIR_TAP179	Filter Coefficient	0
0x310	4	CH1_FIR_TAP180	31:0	RW	CH1_FIR_TAP180	Filter Coefficient	0
0x314	4	CH1_FIR_TAP181	31:0	RW	CH1_FIR_TAP181	Filter Coefficient	0
0x318	4	CH1_FIR_TAP182	31:0	RW	CH1_FIR_TAP182	Filter Coefficient	0
0x31C	4	CH1_FIR_TAP183	31:0	RW	CH1_FIR_TAP183	Filter Coefficient	0
0x320	4	CH1_FIR_TAP184	31:0	RW	CH1_FIR_TAP184	Filter Coefficient	0
0x324	4	CH1_FIR_TAP185	31:0	RW	CH1_FIR_TAP185	Filter Coefficient	0
0x328	4	CH1_FIR_TAP186	31:0	RW	CH1_FIR_TAP186	Filter Coefficient	0
0x32C	4	CH1_FIR_TAP187	31:0	RW	CH1_FIR_TAP187	Filter Coefficient	0
0x330	4	CH1_FIR_TAP188	31:0	RW	CH1_FIR_TAP188	Filter Coefficient	0
0x334	4	CH1_FIR_TAP189	31:0	RW	CH1_FIR_TAP189	Filter Coefficient	0
0x338	4	CH1_FIR_TAP190	31:0	RW	CH1_FIR_TAP190	Filter Coefficient	0
0x33C	4	CH1_FIR_TAP191	31:0	RW	CH1_FIR_TAP191	Filter Coefficient	0
0x340	4	CH1_FIR_TAP192	31:0	RW	CH1_FIR_TAP192	Filter Coefficient	0
0x344	4	CH1_FIR_TAP193	31:0	RW	CH1_FIR_TAP193	Filter Coefficient	0
0x348	4	CH1_FIR_TAP194	31:0	RW	CH1_FIR_TAP194	Filter Coefficient	0
0x34C	4	CH1_FIR_TAP195	31:0	RW	CH1_FIR_TAP195	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x350	4	CH1_FIR_TAP196	31:0	RW	CH1_FIR_TAP196	Filter Coefficient	0
0x354	4	CH1_FIR_TAP197	31:0	RW	CH1_FIR_TAP197	Filter Coefficient	0
0x358	4	CH1_FIR_TAP198	31:0	RW	CH1_FIR_TAP198	Filter Coefficient	0
0x35C	4	CH1_FIR_TAP199	31:0	RW	CH1_FIR_TAP199	Filter Coefficient	0
0x360	4	CH1_FIR_TAP200	31:0	RW	CH1_FIR_TAP200	Filter Coefficient	0
0x364	4	CH1_FIR_TAP201	31:0	RW	CH1_FIR_TAP201	Filter Coefficient	0
0x368	4	CH1_FIR_TAP202	31:0	RW	CH1_FIR_TAP202	Filter Coefficient	0
0x36C	4	CH1_FIR_TAP203	31:0	RW	CH1_FIR_TAP203	Filter Coefficient	0
0x370	4	CH1_FIR_TAP204	31:0	RW	CH1_FIR_TAP204	Filter Coefficient	0
0x374	4	CH1_FIR_TAP205	31:0	RW	CH1_FIR_TAP205	Filter Coefficient	0
0x378	4	CH1_FIR_TAP206	31:0	RW	CH1_FIR_TAP206	Filter Coefficient	0
0x37C	4	CH1_FIR_TAP207	31:0	RW	CH1_FIR_TAP207	Filter Coefficient	0
0x380	4	CH1_FIR_TAP208	31:0	RW	CH1_FIR_TAP208	Filter Coefficient	0
0x384	4	CH1_FIR_TAP209	31:0	RW	CH1_FIR_TAP209	Filter Coefficient	0
0x388	4	CH1_FIR_TAP210	31:0	RW	CH1_FIR_TAP210	Filter Coefficient	0
0x38C	4	CH1_FIR_TAP211	31:0	RW	CH1_FIR_TAP211	Filter Coefficient	0
0x390	4	CH1_FIR_TAP212	31:0	RW	CH1_FIR_TAP212	Filter Coefficient	0
0x394	4	CH1_FIR_TAP213	31:0	RW	CH1_FIR_TAP213	Filter Coefficient	0
0x398	4	CH1_FIR_TAP214	31:0	RW	CH1_FIR_TAP214	Filter Coefficient	0
0x39C	4	CH1_FIR_TAP215	31:0	RW	CH1_FIR_TAP215	Filter Coefficient	0
0x3A0	4	CH1_FIR_TAP216	31:0	RW	CH1_FIR_TAP216	Filter Coefficient	0
0x3A4	4	CH1_FIR_TAP217	31:0	RW	CH1_FIR_TAP217	Filter Coefficient	0
0x3A8	4	CH1_FIR_TAP218	31:0	RW	CH1_FIR_TAP218	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x3AC	4	CH1_FIR_TAP219	31:0	RW	CH1_FIR_TAP219	Filter Coefficient	0
0x3B0	4	CH1_FIR_TAP220	31:0	RW	CH1_FIR_TAP220	Filter Coefficient	0
0x3B4	4	CH1_FIR_TAP221	31:0	RW	CH1_FIR_TAP221	Filter Coefficient	0
0x3B8	4	CH1_FIR_TAP222	31:0	RW	CH1_FIR_TAP222	Filter Coefficient	0
0x3BC	4	CH1_FIR_TAP223	31:0	RW	CH1_FIR_TAP223	Filter Coefficient	0
0x3C0	4	CH1_FIR_TAP224	31:0	RW	CH1_FIR_TAP224	Filter Coefficient	0
0x3C4	4	CH1_FIR_TAP225	31:0	RW	CH1_FIR_TAP225	Filter Coefficient	0
0x3C8	4	CH1_FIR_TAP226	31:0	RW	CH1_FIR_TAP226	Filter Coefficient	0
0x3CC	4	CH1_FIR_TAP227	31:0	RW	CH1_FIR_TAP227	Filter Coefficient	0
0x3D0	4	CH1_FIR_TAP228	31:0	RW	CH1_FIR_TAP228	Filter Coefficient	0
0x3D4	4	CH1_FIR_TAP229	31:0	RW	CH1_FIR_TAP229	Filter Coefficient	0
0x3D8	4	CH1_FIR_TAP230	31:0	RW	CH1_FIR_TAP230	Filter Coefficient	0
0x3DC	4	CH1_FIR_TAP231	31:0	RW	CH1_FIR_TAP231	Filter Coefficient	0
0x3E0	4	CH1_FIR_TAP232	31:0	RW	CH1_FIR_TAP232	Filter Coefficient	0
0x3E4	4	CH1_FIR_TAP233	31:0	RW	CH1_FIR_TAP233	Filter Coefficient	0
0x3E8	4	CH1_FIR_TAP234	31:0	RW	CH1_FIR_TAP234	Filter Coefficient	0
0x3EC	4	CH1_FIR_TAP235	31:0	RW	CH1_FIR_TAP235	Filter Coefficient	0
0x3F0	4	CH1_FIR_TAP236	31:0	RW	CH1_FIR_TAP236	Filter Coefficient	0
0x3F4	4	CH1_FIR_TAP237	31:0	RW	CH1_FIR_TAP237	Filter Coefficient	0
0x3F8	4	CH1_FIR_TAP238	31:0	RW	CH1_FIR_TAP238	Filter Coefficient	0
0x3FC	4	CH1_FIR_TAP239	31:0	RW	CH1_FIR_TAP239	Filter Coefficient	0
0x400	4	CH1_FIR_TAP240	31:0	RW	CH1_FIR_TAP240	Filter Coefficient	0
0x404	4	CH1_FIR_TAP241	31:0	RW	CH1_FIR_TAP241	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x408	4	CH1_FIR_TAP242	31:0	RW	CH1_FIR_TAP242	Filter Coefficient	0
0x40C	4	CH1_FIR_TAP243	31:0	RW	CH1_FIR_TAP243	Filter Coefficient	0
0x410	4	CH1_FIR_TAP244	31:0	RW	CH1_FIR_TAP244	Filter Coefficient	0
0x414	4	CH1_FIR_TAP245	31:0	RW	CH1_FIR_TAP245	Filter Coefficient	0
0x418	4	CH1_FIR_TAP246	31:0	RW	CH1_FIR_TAP246	Filter Coefficient	0
0x41C	4	CH1_FIR_TAP247	31:0	RW	CH1_FIR_TAP247	Filter Coefficient	0
0x420	4	CH1_FIR_TAP248	31:0	RW	CH1_FIR_TAP248	Filter Coefficient	0
0x424	4	CH1_FIR_TAP249	31:0	RW	CH1_FIR_TAP249	Filter Coefficient	0
0x428	4	CH1_FIR_TAP250	31:0	RW	CH1_FIR_TAP250	Filter Coefficient	0
0x42C	4	CH1_FIR_TAP251	31:0	RW	CH1_FIR_TAP251	Filter Coefficient	0
0x430	4	CH1_FIR_TAP252	31:0	RW	CH1_FIR_TAP252	Filter Coefficient	0
0x434	4	CH1_FIR_TAP253	31:0	RW	CH1_FIR_TAP253	Filter Coefficient	0
0x438	4	CH1_FIR_TAP254	31:0	RW	CH1_FIR_TAP254	Filter Coefficient	0
0x43C	4	CH1_FIR_TAP255	31:0	RW	CH1_FIR_TAP255	Filter Coefficient	0
0x440	4	CH2_FIR_TAP0	31:0	RW	CH2_FIR_TAP0	Filter Coefficient	0x3f800000
0x444	4	CH2_FIR_TAP1	31:0	RW	CH2_FIR_TAP1	Filter Coefficient	0
0x448	4	CH2_FIR_TAP2	31:0	RW	CH2_FIR_TAP2	Filter Coefficient	0
0x44C	4	CH2_FIR_TAP3	31:0	RW	CH2_FIR_TAP3	Filter Coefficient	0
0x450	4	CH2_FIR_TAP4	31:0	RW	CH2_FIR_TAP4	Filter Coefficient	0
0x454	4	CH2_FIR_TAP5	31:0	RW	CH2_FIR_TAP5	Filter Coefficient	0
0x458	4	CH2_FIR_TAP6	31:0	RW	CH2_FIR_TAP6	Filter Coefficient	0
0x45C	4	CH2_FIR_TAP7	31:0	RW	CH2_FIR_TAP7	Filter Coefficient	0
0x460	4	CH2_FIR_TAP8	31:0	RW	CH2_FIR_TAP8	Filter Coefficient	0
0x464	4	CH2_FIR_TAP9	31:0	RW	CH2_FIR_TAP9	Filter Coefficient	0
0x468	4	CH2_FIR_TAP10	31:0	RW	CH2_FIR_TAP10	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x46C	4	CH2_FIR_TAP11	31:0	RW	CH2_FIR_TAP11	Filter Coefficient	0
0x470	4	CH2_FIR_TAP12	31:0	RW	CH2_FIR_TAP12	Filter Coefficient	0
0x474	4	CH2_FIR_TAP13	31:0	RW	CH2_FIR_TAP13	Filter Coefficient	0
0x478	4	CH2_FIR_TAP14	31:0	RW	CH2_FIR_TAP14	Filter Coefficient	0
0x47C	4	CH2_FIR_TAP15	31:0	RW	CH2_FIR_TAP15	Filter Coefficient	0
0x480	4	CH2_FIR_TAP16	31:0	RW	CH2_FIR_TAP16	Filter Coefficient	0
0x484	4	CH2_FIR_TAP17	31:0	RW	CH2_FIR_TAP17	Filter Coefficient	0
0x488	4	CH2_FIR_TAP18	31:0	RW	CH2_FIR_TAP18	Filter Coefficient	0
0x48C	4	CH2_FIR_TAP19	31:0	RW	CH2_FIR_TAP19	Filter Coefficient	0
0x490	4	CH2_FIR_TAP20	31:0	RW	CH2_FIR_TAP20	Filter Coefficient	0
0x494	4	CH2_FIR_TAP21	31:0	RW	CH2_FIR_TAP21	Filter Coefficient	0
0x498	4	CH2_FIR_TAP22	31:0	RW	CH2_FIR_TAP22	Filter Coefficient	0
0x49C	4	CH2_FIR_TAP23	31:0	RW	CH2_FIR_TAP23	Filter Coefficient	0
0x4A0	4	CH2_FIR_TAP24	31:0	RW	CH2_FIR_TAP24	Filter Coefficient	0
0x4A4	4	CH2_FIR_TAP25	31:0	RW	CH2_FIR_TAP25	Filter Coefficient	0
0x4A8	4	CH2_FIR_TAP26	31:0	RW	CH2_FIR_TAP26	Filter Coefficient	0
0x4AC	4	CH2_FIR_TAP27	31:0	RW	CH2_FIR_TAP27	Filter Coefficient	0
0x4B0	4	CH2_FIR_TAP28	31:0	RW	CH2_FIR_TAP28	Filter Coefficient	0
0x4B4	4	CH2_FIR_TAP29	31:0	RW	CH2_FIR_TAP29	Filter Coefficient	0
0x4B8	4	CH2_FIR_TAP30	31:0	RW	CH2_FIR_TAP30	Filter Coefficient	0
0x4BC	4	CH2_FIR_TAP31	31:0	RW	CH2_FIR_TAP31	Filter Coefficient	0
0x4C0	4	CH2_FIR_TAP32	31:0	RW	CH2_FIR_TAP32	Filter Coefficient	0
0x4C4	4	CH2_FIR_TAP33	31:0	RW	CH2_FIR_TAP33	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x4C8	4	CH2_FIR_TAP34	31:0	RW	CH2_FIR_TAP34	Filter Coefficient	0
0x4CC	4	CH2_FIR_TAP35	31:0	RW	CH2_FIR_TAP35	Filter Coefficient	0
0x4D0	4	CH2_FIR_TAP36	31:0	RW	CH2_FIR_TAP36	Filter Coefficient	0
0x4D4	4	CH2_FIR_TAP37	31:0	RW	CH2_FIR_TAP37	Filter Coefficient	0
0x4D8	4	CH2_FIR_TAP38	31:0	RW	CH2_FIR_TAP38	Filter Coefficient	0
0x4DC	4	CH2_FIR_TAP39	31:0	RW	CH2_FIR_TAP39	Filter Coefficient	0
0x4E0	4	CH2_FIR_TAP40	31:0	RW	CH2_FIR_TAP40	Filter Coefficient	0
0x4E4	4	CH2_FIR_TAP41	31:0	RW	CH2_FIR_TAP41	Filter Coefficient	0
0x4E8	4	CH2_FIR_TAP42	31:0	RW	CH2_FIR_TAP42	Filter Coefficient	0
0x4EC	4	CH2_FIR_TAP43	31:0	RW	CH2_FIR_TAP43	Filter Coefficient	0
0x4F0	4	CH2_FIR_TAP44	31:0	RW	CH2_FIR_TAP44	Filter Coefficient	0
0x4F4	4	CH2_FIR_TAP45	31:0	RW	CH2_FIR_TAP45	Filter Coefficient	0
0x4F8	4	CH2_FIR_TAP46	31:0	RW	CH2_FIR_TAP46	Filter Coefficient	0
0x4FC	4	CH2_FIR_TAP47	31:0	RW	CH2_FIR_TAP47	Filter Coefficient	0
0x500	4	CH2_FIR_TAP48	31:0	RW	CH2_FIR_TAP48	Filter Coefficient	0
0x504	4	CH2_FIR_TAP49	31:0	RW	CH2_FIR_TAP49	Filter Coefficient	0
0x508	4	CH2_FIR_TAP50	31:0	RW	CH2_FIR_TAP50	Filter Coefficient	0
0x50C	4	CH2_FIR_TAP51	31:0	RW	CH2_FIR_TAP51	Filter Coefficient	0
0x510	4	CH2_FIR_TAP52	31:0	RW	CH2_FIR_TAP52	Filter Coefficient	0
0x514	4	CH2_FIR_TAP53	31:0	RW	CH2_FIR_TAP53	Filter Coefficient	0
0x518	4	CH2_FIR_TAP54	31:0	RW	CH2_FIR_TAP54	Filter Coefficient	0
0x51C	4	CH2_FIR_TAP55	31:0	RW	CH2_FIR_TAP55	Filter Coefficient	0
0x520	4	CH2_FIR_TAP56	31:0	RW	CH2_FIR_TAP56	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x524	4	CH2_FIR_TAP57	31:0	RW	CH2_FIR_TAP57	Filter Coefficient	0
0x528	4	CH2_FIR_TAP58	31:0	RW	CH2_FIR_TAP58	Filter Coefficient	0
0x52C	4	CH2_FIR_TAP59	31:0	RW	CH2_FIR_TAP59	Filter Coefficient	0
0x530	4	CH2_FIR_TAP60	31:0	RW	CH2_FIR_TAP60	Filter Coefficient	0
0x534	4	CH2_FIR_TAP61	31:0	RW	CH2_FIR_TAP61	Filter Coefficient	0
0x538	4	CH2_FIR_TAP62	31:0	RW	CH2_FIR_TAP62	Filter Coefficient	0
0x53C	4	CH2_FIR_TAP63	31:0	RW	CH2_FIR_TAP63	Filter Coefficient	0
0x540	4	CH2_FIR_TAP64	31:0	RW	CH2_FIR_TAP64	Filter Coefficient	0
0x544	4	CH2_FIR_TAP65	31:0	RW	CH2_FIR_TAP65	Filter Coefficient	0
0x548	4	CH2_FIR_TAP66	31:0	RW	CH2_FIR_TAP66	Filter Coefficient	0
0x54C	4	CH2_FIR_TAP67	31:0	RW	CH2_FIR_TAP67	Filter Coefficient	0
0x550	4	CH2_FIR_TAP68	31:0	RW	CH2_FIR_TAP68	Filter Coefficient	0
0x554	4	CH2_FIR_TAP69	31:0	RW	CH2_FIR_TAP69	Filter Coefficient	0
0x558	4	CH2_FIR_TAP70	31:0	RW	CH2_FIR_TAP70	Filter Coefficient	0
0x55C	4	CH2_FIR_TAP71	31:0	RW	CH2_FIR_TAP71	Filter Coefficient	0
0x560	4	CH2_FIR_TAP72	31:0	RW	CH2_FIR_TAP72	Filter Coefficient	0
0x564	4	CH2_FIR_TAP73	31:0	RW	CH2_FIR_TAP73	Filter Coefficient	0
0x568	4	CH2_FIR_TAP74	31:0	RW	CH2_FIR_TAP74	Filter Coefficient	0
0x56C	4	CH2_FIR_TAP75	31:0	RW	CH2_FIR_TAP75	Filter Coefficient	0
0x570	4	CH2_FIR_TAP76	31:0	RW	CH2_FIR_TAP76	Filter Coefficient	0
0x574	4	CH2_FIR_TAP77	31:0	RW	CH2_FIR_TAP77	Filter Coefficient	0
0x578	4	CH2_FIR_TAP78	31:0	RW	CH2_FIR_TAP78	Filter Coefficient	0
0x57C	4	CH2_FIR_TAP79	31:0	RW	CH2_FIR_TAP79	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x580	4	CH2_FIR_TAP80	31:0	RW	CH2_FIR_TAP80	Filter Coefficient	0
0x584	4	CH2_FIR_TAP81	31:0	RW	CH2_FIR_TAP81	Filter Coefficient	0
0x588	4	CH2_FIR_TAP82	31:0	RW	CH2_FIR_TAP82	Filter Coefficient	0
0x58C	4	CH2_FIR_TAP83	31:0	RW	CH2_FIR_TAP83	Filter Coefficient	0
0x590	4	CH2_FIR_TAP84	31:0	RW	CH2_FIR_TAP84	Filter Coefficient	0
0x594	4	CH2_FIR_TAP85	31:0	RW	CH2_FIR_TAP85	Filter Coefficient	0
0x598	4	CH2_FIR_TAP86	31:0	RW	CH2_FIR_TAP86	Filter Coefficient	0
0x59C	4	CH2_FIR_TAP87	31:0	RW	CH2_FIR_TAP87	Filter Coefficient	0
0x5A0	4	CH2_FIR_TAP88	31:0	RW	CH2_FIR_TAP88	Filter Coefficient	0
0x5A4	4	CH2_FIR_TAP89	31:0	RW	CH2_FIR_TAP89	Filter Coefficient	0
0x5A8	4	CH2_FIR_TAP90	31:0	RW	CH2_FIR_TAP90	Filter Coefficient	0
0x5AC	4	CH2_FIR_TAP91	31:0	RW	CH2_FIR_TAP91	Filter Coefficient	0
0x5B0	4	CH2_FIR_TAP92	31:0	RW	CH2_FIR_TAP92	Filter Coefficient	0
0x5B4	4	CH2_FIR_TAP93	31:0	RW	CH2_FIR_TAP93	Filter Coefficient	0
0x5B8	4	CH2_FIR_TAP94	31:0	RW	CH2_FIR_TAP94	Filter Coefficient	0
0x5BC	4	CH2_FIR_TAP95	31:0	RW	CH2_FIR_TAP95	Filter Coefficient	0
0x5C0	4	CH2_FIR_TAP96	31:0	RW	CH2_FIR_TAP96	Filter Coefficient	0
0x5C4	4	CH2_FIR_TAP97	31:0	RW	CH2_FIR_TAP97	Filter Coefficient	0
0x5C8	4	CH2_FIR_TAP98	31:0	RW	CH2_FIR_TAP98	Filter Coefficient	0
0x5CC	4	CH2_FIR_TAP99	31:0	RW	CH2_FIR_TAP99	Filter Coefficient	0
0x5D0	4	CH2_FIR_TAP100	31:0	RW	CH2_FIR_TAP100	Filter Coefficient	0
0x5D4	4	CH2_FIR_TAP101	31:0	RW	CH2_FIR_TAP101	Filter Coefficient	0
0x5D8	4	CH2_FIR_TAP102	31:0	RW	CH2_FIR_TAP102	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x5DC	4	CH2_FIR_TAP103	31:0	RW	CH2_FIR_TAP103	Filter Coefficient	0
0x5E0	4	CH2_FIR_TAP104	31:0	RW	CH2_FIR_TAP104	Filter Coefficient	0
0x5E4	4	CH2_FIR_TAP105	31:0	RW	CH2_FIR_TAP105	Filter Coefficient	0
0x5E8	4	CH2_FIR_TAP106	31:0	RW	CH2_FIR_TAP106	Filter Coefficient	0
0x5EC	4	CH2_FIR_TAP107	31:0	RW	CH2_FIR_TAP107	Filter Coefficient	0
0x5F0	4	CH2_FIR_TAP108	31:0	RW	CH2_FIR_TAP108	Filter Coefficient	0
0x5F4	4	CH2_FIR_TAP109	31:0	RW	CH2_FIR_TAP109	Filter Coefficient	0
0x5F8	4	CH2_FIR_TAP110	31:0	RW	CH2_FIR_TAP110	Filter Coefficient	0
0x5FC	4	CH2_FIR_TAP111	31:0	RW	CH2_FIR_TAP111	Filter Coefficient	0
0x600	4	CH2_FIR_TAP112	31:0	RW	CH2_FIR_TAP112	Filter Coefficient	0
0x604	4	CH2_FIR_TAP113	31:0	RW	CH2_FIR_TAP113	Filter Coefficient	0
0x608	4	CH2_FIR_TAP114	31:0	RW	CH2_FIR_TAP114	Filter Coefficient	0
0x60C	4	CH2_FIR_TAP115	31:0	RW	CH2_FIR_TAP115	Filter Coefficient	0
0x610	4	CH2_FIR_TAP116	31:0	RW	CH2_FIR_TAP116	Filter Coefficient	0
0x614	4	CH2_FIR_TAP117	31:0	RW	CH2_FIR_TAP117	Filter Coefficient	0
0x618	4	CH2_FIR_TAP118	31:0	RW	CH2_FIR_TAP118	Filter Coefficient	0
0x61C	4	CH2_FIR_TAP119	31:0	RW	CH2_FIR_TAP119	Filter Coefficient	0
0x620	4	CH2_FIR_TAP120	31:0	RW	CH2_FIR_TAP120	Filter Coefficient	0
0x624	4	CH2_FIR_TAP121	31:0	RW	CH2_FIR_TAP121	Filter Coefficient	0
0x628	4	CH2_FIR_TAP122	31:0	RW	CH2_FIR_TAP122	Filter Coefficient	0
0x62C	4	CH2_FIR_TAP123	31:0	RW	CH2_FIR_TAP123	Filter Coefficient	0
0x630	4	CH2_FIR_TAP124	31:0	RW	CH2_FIR_TAP124	Filter Coefficient	0
0x634	4	CH2_FIR_TAP125	31:0	RW	CH2_FIR_TAP125	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x638	4	CH2_FIR_TAP126	31:0	RW	CH2_FIR_TAP126	Filter Coefficient	0
0x63C	4	CH2_FIR_TAP127	31:0	RW	CH2_FIR_TAP127	Filter Coefficient	0
0x640	4	CH2_FIR_TAP128	31:0	RW	CH2_FIR_TAP128	Filter Coefficient	0
0x644	4	CH2_FIR_TAP129	31:0	RW	CH2_FIR_TAP129	Filter Coefficient	0
0x648	4	CH2_FIR_TAP130	31:0	RW	CH2_FIR_TAP130	Filter Coefficient	0
0x64C	4	CH2_FIR_TAP131	31:0	RW	CH2_FIR_TAP131	Filter Coefficient	0
0x650	4	CH2_FIR_TAP132	31:0	RW	CH2_FIR_TAP132	Filter Coefficient	0
0x654	4	CH2_FIR_TAP133	31:0	RW	CH2_FIR_TAP133	Filter Coefficient	0
0x658	4	CH2_FIR_TAP134	31:0	RW	CH2_FIR_TAP134	Filter Coefficient	0
0x65C	4	CH2_FIR_TAP135	31:0	RW	CH2_FIR_TAP135	Filter Coefficient	0
0x660	4	CH2_FIR_TAP136	31:0	RW	CH2_FIR_TAP136	Filter Coefficient	0
0x664	4	CH2_FIR_TAP137	31:0	RW	CH2_FIR_TAP137	Filter Coefficient	0
0x668	4	CH2_FIR_TAP138	31:0	RW	CH2_FIR_TAP138	Filter Coefficient	0
0x66C	4	CH2_FIR_TAP139	31:0	RW	CH2_FIR_TAP139	Filter Coefficient	0
0x670	4	CH2_FIR_TAP140	31:0	RW	CH2_FIR_TAP140	Filter Coefficient	0
0x674	4	CH2_FIR_TAP141	31:0	RW	CH2_FIR_TAP141	Filter Coefficient	0
0x678	4	CH2_FIR_TAP142	31:0	RW	CH2_FIR_TAP142	Filter Coefficient	0
0x67C	4	CH2_FIR_TAP143	31:0	RW	CH2_FIR_TAP143	Filter Coefficient	0
0x680	4	CH2_FIR_TAP144	31:0	RW	CH2_FIR_TAP144	Filter Coefficient	0
0x684	4	CH2_FIR_TAP145	31:0	RW	CH2_FIR_TAP145	Filter Coefficient	0
0x688	4	CH2_FIR_TAP146	31:0	RW	CH2_FIR_TAP146	Filter Coefficient	0
0x68C	4	CH2_FIR_TAP147	31:0	RW	CH2_FIR_TAP147	Filter Coefficient	0
0x690	4	CH2_FIR_TAP148	31:0	RW	CH2_FIR_TAP148	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x694	4	CH2_FIR_TAP149	31:0	RW	CH2_FIR_TAP149	Filter Coefficient	0
0x698	4	CH2_FIR_TAP150	31:0	RW	CH2_FIR_TAP150	Filter Coefficient	0
0x69C	4	CH2_FIR_TAP151	31:0	RW	CH2_FIR_TAP151	Filter Coefficient	0
0x6A0	4	CH2_FIR_TAP152	31:0	RW	CH2_FIR_TAP152	Filter Coefficient	0
0x6A4	4	CH2_FIR_TAP153	31:0	RW	CH2_FIR_TAP153	Filter Coefficient	0
0x6A8	4	CH2_FIR_TAP154	31:0	RW	CH2_FIR_TAP154	Filter Coefficient	0
0x6AC	4	CH2_FIR_TAP155	31:0	RW	CH2_FIR_TAP155	Filter Coefficient	0
0x6B0	4	CH2_FIR_TAP156	31:0	RW	CH2_FIR_TAP156	Filter Coefficient	0
0x6B4	4	CH2_FIR_TAP157	31:0	RW	CH2_FIR_TAP157	Filter Coefficient	0
0x6B8	4	CH2_FIR_TAP158	31:0	RW	CH2_FIR_TAP158	Filter Coefficient	0
0x6BC	4	CH2_FIR_TAP159	31:0	RW	CH2_FIR_TAP159	Filter Coefficient	0
0x6C0	4	CH2_FIR_TAP160	31:0	RW	CH2_FIR_TAP160	Filter Coefficient	0
0x6C4	4	CH2_FIR_TAP161	31:0	RW	CH2_FIR_TAP161	Filter Coefficient	0
0x6C8	4	CH2_FIR_TAP162	31:0	RW	CH2_FIR_TAP162	Filter Coefficient	0
0x6CC	4	CH2_FIR_TAP163	31:0	RW	CH2_FIR_TAP163	Filter Coefficient	0
0x6D0	4	CH2_FIR_TAP164	31:0	RW	CH2_FIR_TAP164	Filter Coefficient	0
0x6D4	4	CH2_FIR_TAP165	31:0	RW	CH2_FIR_TAP165	Filter Coefficient	0
0x6D8	4	CH2_FIR_TAP166	31:0	RW	CH2_FIR_TAP166	Filter Coefficient	0
0x6DC	4	CH2_FIR_TAP167	31:0	RW	CH2_FIR_TAP167	Filter Coefficient	0
0x6E0	4	CH2_FIR_TAP168	31:0	RW	CH2_FIR_TAP168	Filter Coefficient	0
0x6E4	4	CH2_FIR_TAP169	31:0	RW	CH2_FIR_TAP169	Filter Coefficient	0
0x6E8	4	CH2_FIR_TAP170	31:0	RW	CH2_FIR_TAP170	Filter Coefficient	0
0x6EC	4	CH2_FIR_TAP171	31:0	RW	CH2_FIR_TAP171	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x6F0	4	CH2_FIR_TAP172	31:0	RW	CH2_FIR_TAP172	Filter Coefficient	0
0x6F4	4	CH2_FIR_TAP173	31:0	RW	CH2_FIR_TAP173	Filter Coefficient	0
0x6F8	4	CH2_FIR_TAP174	31:0	RW	CH2_FIR_TAP174	Filter Coefficient	0
0x6FC	4	CH2_FIR_TAP175	31:0	RW	CH2_FIR_TAP175	Filter Coefficient	0
0x700	4	CH2_FIR_TAP176	31:0	RW	CH2_FIR_TAP176	Filter Coefficient	0
0x704	4	CH2_FIR_TAP177	31:0	RW	CH2_FIR_TAP177	Filter Coefficient	0
0x708	4	CH2_FIR_TAP178	31:0	RW	CH2_FIR_TAP178	Filter Coefficient	0
0x70C	4	CH2_FIR_TAP179	31:0	RW	CH2_FIR_TAP179	Filter Coefficient	0
0x710	4	CH2_FIR_TAP180	31:0	RW	CH2_FIR_TAP180	Filter Coefficient	0
0x714	4	CH2_FIR_TAP181	31:0	RW	CH2_FIR_TAP181	Filter Coefficient	0
0x718	4	CH2_FIR_TAP182	31:0	RW	CH2_FIR_TAP182	Filter Coefficient	0
0x71C	4	CH2_FIR_TAP183	31:0	RW	CH2_FIR_TAP183	Filter Coefficient	0
0x720	4	CH2_FIR_TAP184	31:0	RW	CH2_FIR_TAP184	Filter Coefficient	0
0x724	4	CH2_FIR_TAP185	31:0	RW	CH2_FIR_TAP185	Filter Coefficient	0
0x728	4	CH2_FIR_TAP186	31:0	RW	CH2_FIR_TAP186	Filter Coefficient	0
0x72C	4	CH2_FIR_TAP187	31:0	RW	CH2_FIR_TAP187	Filter Coefficient	0
0x730	4	CH2_FIR_TAP188	31:0	RW	CH2_FIR_TAP188	Filter Coefficient	0
0x734	4	CH2_FIR_TAP189	31:0	RW	CH2_FIR_TAP189	Filter Coefficient	0
0x738	4	CH2_FIR_TAP190	31:0	RW	CH2_FIR_TAP190	Filter Coefficient	0
0x73C	4	CH2_FIR_TAP191	31:0	RW	CH2_FIR_TAP191	Filter Coefficient	0
0x740	4	CH2_FIR_TAP192	31:0	RW	CH2_FIR_TAP192	Filter Coefficient	0
0x744	4	CH2_FIR_TAP193	31:0	RW	CH2_FIR_TAP193	Filter Coefficient	0
0x748	4	CH2_FIR_TAP194	31:0	RW	CH2_FIR_TAP194	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x74C	4	CH2_FIR_TAP195	31:0	RW	CH2_FIR_TAP195	Filter Coefficient	0
0x750	4	CH2_FIR_TAP196	31:0	RW	CH2_FIR_TAP196	Filter Coefficient	0
0x754	4	CH2_FIR_TAP197	31:0	RW	CH2_FIR_TAP197	Filter Coefficient	0
0x758	4	CH2_FIR_TAP198	31:0	RW	CH2_FIR_TAP198	Filter Coefficient	0
0x75C	4	CH2_FIR_TAP199	31:0	RW	CH2_FIR_TAP199	Filter Coefficient	0
0x760	4	CH2_FIR_TAP200	31:0	RW	CH2_FIR_TAP200	Filter Coefficient	0
0x764	4	CH2_FIR_TAP201	31:0	RW	CH2_FIR_TAP201	Filter Coefficient	0
0x768	4	CH2_FIR_TAP202	31:0	RW	CH2_FIR_TAP202	Filter Coefficient	0
0x76C	4	CH2_FIR_TAP203	31:0	RW	CH2_FIR_TAP203	Filter Coefficient	0
0x770	4	CH2_FIR_TAP204	31:0	RW	CH2_FIR_TAP204	Filter Coefficient	0
0x774	4	CH2_FIR_TAP205	31:0	RW	CH2_FIR_TAP205	Filter Coefficient	0
0x778	4	CH2_FIR_TAP206	31:0	RW	CH2_FIR_TAP206	Filter Coefficient	0
0x77C	4	CH2_FIR_TAP207	31:0	RW	CH2_FIR_TAP207	Filter Coefficient	0
0x780	4	CH2_FIR_TAP208	31:0	RW	CH2_FIR_TAP208	Filter Coefficient	0
0x784	4	CH2_FIR_TAP209	31:0	RW	CH2_FIR_TAP209	Filter Coefficient	0
0x788	4	CH2_FIR_TAP210	31:0	RW	CH2_FIR_TAP210	Filter Coefficient	0
0x78C	4	CH2_FIR_TAP211	31:0	RW	CH2_FIR_TAP211	Filter Coefficient	0
0x790	4	CH2_FIR_TAP212	31:0	RW	CH2_FIR_TAP212	Filter Coefficient	0
0x794	4	CH2_FIR_TAP213	31:0	RW	CH2_FIR_TAP213	Filter Coefficient	0
0x798	4	CH2_FIR_TAP214	31:0	RW	CH2_FIR_TAP214	Filter Coefficient	0
0x79C	4	CH2_FIR_TAP215	31:0	RW	CH2_FIR_TAP215	Filter Coefficient	0
0x7A0	4	CH2_FIR_TAP216	31:0	RW	CH2_FIR_TAP216	Filter Coefficient	0
0x7A4	4	CH2_FIR_TAP217	31:0	RW	CH2_FIR_TAP217	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x7A8	4	CH2_FIR_TAP218	31:0	RW	CH2_FIR_TAP218	Filter Coefficient	0
0x7AC	4	CH2_FIR_TAP219	31:0	RW	CH2_FIR_TAP219	Filter Coefficient	0
0x7B0	4	CH2_FIR_TAP220	31:0	RW	CH2_FIR_TAP220	Filter Coefficient	0
0x7B4	4	CH2_FIR_TAP221	31:0	RW	CH2_FIR_TAP221	Filter Coefficient	0
0x7B8	4	CH2_FIR_TAP222	31:0	RW	CH2_FIR_TAP222	Filter Coefficient	0
0x7BC	4	CH2_FIR_TAP223	31:0	RW	CH2_FIR_TAP223	Filter Coefficient	0
0x7C0	4	CH2_FIR_TAP224	31:0	RW	CH2_FIR_TAP224	Filter Coefficient	0
0x7C4	4	CH2_FIR_TAP225	31:0	RW	CH2_FIR_TAP225	Filter Coefficient	0
0x7C8	4	CH2_FIR_TAP226	31:0	RW	CH2_FIR_TAP226	Filter Coefficient	0
0x7CC	4	CH2_FIR_TAP227	31:0	RW	CH2_FIR_TAP227	Filter Coefficient	0
0x7D0	4	CH2_FIR_TAP228	31:0	RW	CH2_FIR_TAP228	Filter Coefficient	0
0x7D4	4	CH2_FIR_TAP229	31:0	RW	CH2_FIR_TAP229	Filter Coefficient	0
0x7D8	4	CH2_FIR_TAP230	31:0	RW	CH2_FIR_TAP230	Filter Coefficient	0
0x7DC	4	CH2_FIR_TAP231	31:0	RW	CH2_FIR_TAP231	Filter Coefficient	0
0x7E0	4	CH2_FIR_TAP232	31:0	RW	CH2_FIR_TAP232	Filter Coefficient	0
0x7E4	4	CH2_FIR_TAP233	31:0	RW	CH2_FIR_TAP233	Filter Coefficient	0
0x7E8	4	CH2_FIR_TAP234	31:0	RW	CH2_FIR_TAP234	Filter Coefficient	0
0x7EC	4	CH2_FIR_TAP235	31:0	RW	CH2_FIR_TAP235	Filter Coefficient	0
0x7F0	4	CH2_FIR_TAP236	31:0	RW	CH2_FIR_TAP236	Filter Coefficient	0
0x7F4	4	CH2_FIR_TAP237	31:0	RW	CH2_FIR_TAP237	Filter Coefficient	0
0x7F8	4	CH2_FIR_TAP238	31:0	RW	CH2_FIR_TAP238	Filter Coefficient	0
0x7FC	4	CH2_FIR_TAP239	31:0	RW	CH2_FIR_TAP239	Filter Coefficient	0
0x800	4	CH2_FIR_TAP240	31:0	RW	CH2_FIR_TAP240	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x804	4	CH2_FIR_TAP241	31:0	RW	CH2_FIR_TAP241	Filter Coefficient	0
0x808	4	CH2_FIR_TAP242	31:0	RW	CH2_FIR_TAP242	Filter Coefficient	0
0x80C	4	CH2_FIR_TAP243	31:0	RW	CH2_FIR_TAP243	Filter Coefficient	0
0x810	4	CH2_FIR_TAP244	31:0	RW	CH2_FIR_TAP244	Filter Coefficient	0
0x814	4	CH2_FIR_TAP245	31:0	RW	CH2_FIR_TAP245	Filter Coefficient	0
0x818	4	CH2_FIR_TAP246	31:0	RW	CH2_FIR_TAP246	Filter Coefficient	0
0x81C	4	CH2_FIR_TAP247	31:0	RW	CH2_FIR_TAP247	Filter Coefficient	0
0x820	4	CH2_FIR_TAP248	31:0	RW	CH2_FIR_TAP248	Filter Coefficient	0
0x824	4	CH2_FIR_TAP249	31:0	RW	CH2_FIR_TAP249	Filter Coefficient	0
0x828	4	CH2_FIR_TAP250	31:0	RW	CH2_FIR_TAP250	Filter Coefficient	0
0x82C	4	CH2_FIR_TAP251	31:0	RW	CH2_FIR_TAP251	Filter Coefficient	0
0x830	4	CH2_FIR_TAP252	31:0	RW	CH2_FIR_TAP252	Filter Coefficient	0
0x834	4	CH2_FIR_TAP253	31:0	RW	CH2_FIR_TAP253	Filter Coefficient	0
0x838	4	CH2_FIR_TAP254	31:0	RW	CH2_FIR_TAP254	Filter Coefficient	0
0x83C	4	CH2_FIR_TAP255	31:0	RW	CH2_FIR_TAP255	Filter Coefficient	0
0x840	4	CH1_EQ1_B0	31:0	RW	CH1_EQ1_B0	Filter Coefficient	0x3f800000
0x844	4	CH1_EQ1_B1	31:0	RW	CH1_EQ1_B1	Filter Coefficient	0
0x848	4	CH1_EQ1_B2	31:0	RW	CH1_EQ1_B2	Filter Coefficient	0
0x84C	4	CH1_EQ1_A1	31:0	RW	CH1_EQ1_A1	Filter Coefficient	0
0x850	4	CH1_EQ1_A2	31:0	RW	CH1_EQ1_A2	Filter Coefficient	0
0x854	4	CH1_EQ2_B0	31:0	RW	CH1_EQ2_B0	Filter Coefficient	0x3f800000
0x858	4	CH1_EQ2_B1	31:0	RW	CH1_EQ2_B1	Filter Coefficient	0
0x85C	4	CH1_EQ2_B2	31:0	RW	CH1_EQ2_B2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x860	4	CH1_EQ2_A1	31:0	RW	CH1_EQ2_A1	Filter Coefficient	0
0x864	4	CH1_EQ2_A2	31:0	RW	CH1_EQ2_A2	Filter Coefficient	0
0x868	4	CH1_EQ3_B0	31:0	RW	CH1_EQ3_B0	Filter Coefficient	0x3f800000
0x86C	4	CH1_EQ3_B1	31:0	RW	CH1_EQ3_B1	Filter Coefficient	0
0x870	4	CH1_EQ3_B2	31:0	RW	CH1_EQ3_B2	Filter Coefficient	0
0x874	4	CH1_EQ3_A1	31:0	RW	CH1_EQ3_A1	Filter Coefficient	0
0x878	4	CH1_EQ3_A2	31:0	RW	CH1_EQ3_A2	Filter Coefficient	0
0x87C	4	CH1_EQ4_B0	31:0	RW	CH1_EQ4_B0	Filter Coefficient	0x3f800000
0x880	4	CH1_EQ4_B1	31:0	RW	CH1_EQ4_B1	Filter Coefficient	0
0x884	4	CH1_EQ4_B2	31:0	RW	CH1_EQ4_B2	Filter Coefficient	0
0x888	4	CH1_EQ4_A1	31:0	RW	CH1_EQ4_A1	Filter Coefficient	0
0x88C	4	CH1_EQ4_A2	31:0	RW	CH1_EQ4_A2	Filter Coefficient	0
0x890	4	CH1_EQ5_B0	31:0	RW	CH1_EQ5_B0	Filter Coefficient	0x3f800000
0x894	4	CH1_EQ5_B1	31:0	RW	CH1_EQ5_B1	Filter Coefficient	0
0x898	4	CH1_EQ5_B2	31:0	RW	CH1_EQ5_B2	Filter Coefficient	0
0x89C	4	CH1_EQ5_A1	31:0	RW	CH1_EQ5_A1	Filter Coefficient	0
0x8A0	4	CH1_EQ5_A2	31:0	RW	CH1_EQ5_A2	Filter Coefficient	0
0x8A4	4	CH1_EQ6_B0	31:0	RW	CH1_EQ6_B0	Filter Coefficient	0x3f800000
0x8A8	4	CH1_EQ6_B1	31:0	RW	CH1_EQ6_B1	Filter Coefficient	0
0x8AC	4	CH1_EQ6_B2	31:0	RW	CH1_EQ6_B2	Filter Coefficient	0
0x8B0	4	CH1_EQ6_A1	31:0	RW	CH1_EQ6_A1	Filter Coefficient	0
0x8B4	4	CH1_EQ6_A2	31:0	RW	CH1_EQ6_A2	Filter Coefficient	0
0x8B8	4	CH1_EQ7_B0	31:0	RW	CH1_EQ7_B0	Filter Coefficient	0x3f800000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x8BC	4	CH1_EQ7_B1	31:0	RW	CH1_EQ7_B1	Filter Coefficient	0
0x8C0	4	CH1_EQ7_B2	31:0	RW	CH1_EQ7_B2	Filter Coefficient	0
0x8C4	4	CH1_EQ7_A1	31:0	RW	CH1_EQ7_A1	Filter Coefficient	0
0x8C8	4	CH1_EQ7_A2	31:0	RW	CH1_EQ7_A2	Filter Coefficient	0
0x8CC	4	CH1_EQ8_B0	31:0	RW	CH1_EQ8_B0	Filter Coefficient	0x3f800000
0x8D0	4	CH1_EQ8_B1	31:0	RW	CH1_EQ8_B1	Filter Coefficient	0
0x8D4	4	CH1_EQ8_B2	31:0	RW	CH1_EQ8_B2	Filter Coefficient	0
0x8D8	4	CH1_EQ8_A1	31:0	RW	CH1_EQ8_A1	Filter Coefficient	0
0x8DC	4	CH1_EQ8_A2	31:0	RW	CH1_EQ8_A2	Filter Coefficient	0
0x8E0	4	CH1_EQ9_B0	31:0	RW	CH1_EQ9_B0	Filter Coefficient	0x3f800000
0x8E4	4	CH1_EQ9_B1	31:0	RW	CH1_EQ9_B1	Filter Coefficient	0
0x8E8	4	CH1_EQ9_B2	31:0	RW	CH1_EQ9_B2	Filter Coefficient	0
0x8EC	4	CH1_EQ9_A1	31:0	RW	CH1_EQ9_A1	Filter Coefficient	0
0x8F0	4	CH1_EQ9_A2	31:0	RW	CH1_EQ9_A2	Filter Coefficient	0
0x8F4	4	CH1_EQ10_B0	31:0	RW	CH1_EQ10_B0	Filter Coefficient	0x3f800000
0x8F8	4	CH1_EQ10_B1	31:0	RW	CH1_EQ10_B1	Filter Coefficient	0
0x8FC	4	CH1_EQ10_B2	31:0	RW	CH1_EQ10_B2	Filter Coefficient	0
0x900	4	CH1_EQ10_A1	31:0	RW	CH1_EQ10_A1	Filter Coefficient	0
0x904	4	CH1_EQ10_A2	31:0	RW	CH1_EQ10_A2	Filter Coefficient	0
0x908	4	CH1_EQ11_B0	31:0	RW	CH1_EQ11_B0	Filter Coefficient	0x3f800000
0x90C	4	CH1_EQ11_B1	31:0	RW	CH1_EQ11_B1	Filter Coefficient	0
0x910	4	CH1_EQ11_B2	31:0	RW	CH1_EQ11_B2	Filter Coefficient	0
0x914	4	CH1_EQ11_A1	31:0	RW	CH1_EQ11_A1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x918	4	CH1_EQ11_A2	31:0	RW	CH1_EQ11_A2	Filter Coefficient	0
0x91C	4	CH1_EQ12_B0	31:0	RW	CH1_EQ12_B0	Filter Coefficient	0x3f800000
0x920	4	CH1_EQ12_B1	31:0	RW	CH1_EQ12_B1	Filter Coefficient	0
0x924	4	CH1_EQ12_B2	31:0	RW	CH1_EQ12_B2	Filter Coefficient	0
0x928	4	CH1_EQ12_A1	31:0	RW	CH1_EQ12_A1	Filter Coefficient	0
0x92C	4	CH1_EQ12_A2	31:0	RW	CH1_EQ12_A2	Filter Coefficient	0
0x930	4	CH2_EQ1_B0	31:0	RW	CH2_EQ1_B0	Filter Coefficient	0x3f800000
0x934	4	CH2_EQ1_B1	31:0	RW	CH2_EQ1_B1	Filter Coefficient	0
0x938	4	CH2_EQ1_B2	31:0	RW	CH2_EQ1_B2	Filter Coefficient	0
0x93C	4	CH2_EQ1_A1	31:0	RW	CH2_EQ1_A1	Filter Coefficient	0
0x940	4	CH2_EQ1_A2	31:0	RW	CH2_EQ1_A2	Filter Coefficient	0
0x944	4	CH2_EQ2_B0	31:0	RW	CH2_EQ2_B0	Filter Coefficient	0x3f800000
0x948	4	CH2_EQ2_B1	31:0	RW	CH2_EQ2_B1	Filter Coefficient	0
0x94C	4	CH2_EQ2_B2	31:0	RW	CH2_EQ2_B2	Filter Coefficient	0
0x950	4	CH2_EQ2_A1	31:0	RW	CH2_EQ2_A1	Filter Coefficient	0
0x954	4	CH2_EQ2_A2	31:0	RW	CH2_EQ2_A2	Filter Coefficient	0
0x958	4	CH2_EQ3_B0	31:0	RW	CH2_EQ3_B0	Filter Coefficient	0x3f800000
0x95C	4	CH2_EQ3_B1	31:0	RW	CH2_EQ3_B1	Filter Coefficient	0
0x960	4	CH2_EQ3_B2	31:0	RW	CH2_EQ3_B2	Filter Coefficient	0
0x964	4	CH2_EQ3_A1	31:0	RW	CH2_EQ3_A1	Filter Coefficient	0
0x968	4	CH2_EQ3_A2	31:0	RW	CH2_EQ3_A2	Filter Coefficient	0
0x96C	4	CH2_EQ4_B0	31:0	RW	CH2_EQ4_B0	Filter Coefficient	0x3f800000
0x970	4	CH2_EQ4_B1	31:0	RW	CH2_EQ4_B1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x974	4	CH2_EQ4_B2	31:0	RW	CH2_EQ4_B2	Filter Coefficient	0
0x978	4	CH2_EQ4_A1	31:0	RW	CH2_EQ4_A1	Filter Coefficient	0
0x97C	4	CH2_EQ4_A2	31:0	RW	CH2_EQ4_A2	Filter Coefficient	0
0x980	4	CH2_EQ5_B0	31:0	RW	CH2_EQ5_B0	Filter Coefficient	0x3f800000
0x984	4	CH2_EQ5_B1	31:0	RW	CH2_EQ5_B1	Filter Coefficient	0
0x988	4	CH2_EQ5_B2	31:0	RW	CH2_EQ5_B2	Filter Coefficient	0
0x98C	4	CH2_EQ5_A1	31:0	RW	CH2_EQ5_A1	Filter Coefficient	0
0x990	4	CH2_EQ5_A2	31:0	RW	CH2_EQ5_A2	Filter Coefficient	0
0x994	4	CH2_EQ6_B0	31:0	RW	CH2_EQ6_B0	Filter Coefficient	0x3f800000
0x998	4	CH2_EQ6_B1	31:0	RW	CH2_EQ6_B1	Filter Coefficient	0
0x99C	4	CH2_EQ6_B2	31:0	RW	CH2_EQ6_B2	Filter Coefficient	0
0x9A0	4	CH2_EQ6_A1	31:0	RW	CH2_EQ6_A1	Filter Coefficient	0
0x9A4	4	CH2_EQ6_A2	31:0	RW	CH2_EQ6_A2	Filter Coefficient	0
0x9A8	4	CH2_EQ7_B0	31:0	RW	CH2_EQ7_B0	Filter Coefficient	0x3f800000
0x9AC	4	CH2_EQ7_B1	31:0	RW	CH2_EQ7_B1	Filter Coefficient	0
0x9B0	4	CH2_EQ7_B2	31:0	RW	CH2_EQ7_B2	Filter Coefficient	0
0x9B4	4	CH2_EQ7_A1	31:0	RW	CH2_EQ7_A1	Filter Coefficient	0
0x9B8	4	CH2_EQ7_A2	31:0	RW	CH2_EQ7_A2	Filter Coefficient	0
0x9BC	4	CH2_EQ8_B0	31:0	RW	CH2_EQ8_B0	Filter Coefficient	0x3f800000
0x9C0	4	CH2_EQ8_B1	31:0	RW	CH2_EQ8_B1	Filter Coefficient	0
0x9C4	4	CH2_EQ8_B2	31:0	RW	CH2_EQ8_B2	Filter Coefficient	0
0x9C8	4	CH2_EQ8_A1	31:0	RW	CH2_EQ8_A1	Filter Coefficient	0
0x9CC	4	CH2_EQ8_A2	31:0	RW	CH2_EQ8_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x9D0	4	CH2_EQ9_B0	31:0	RW	CH2_EQ9_B0	Filter Coefficient	0x3f800000
0x9D4	4	CH2_EQ9_B1	31:0	RW	CH2_EQ9_B1	Filter Coefficient	0
0x9D8	4	CH2_EQ9_B2	31:0	RW	CH2_EQ9_B2	Filter Coefficient	0
0x9DC	4	CH2_EQ9_A1	31:0	RW	CH2_EQ9_A1	Filter Coefficient	0
0x9E0	4	CH2_EQ9_A2	31:0	RW	CH2_EQ9_A2	Filter Coefficient	0
0x9E4	4	CH2_EQ10_B0	31:0	RW	CH2_EQ10_B0	Filter Coefficient	0x3f800000
0x9E8	4	CH2_EQ10_B1	31:0	RW	CH2_EQ10_B1	Filter Coefficient	0
0x9EC	4	CH2_EQ10_B2	31:0	RW	CH2_EQ10_B2	Filter Coefficient	0
0x9F0	4	CH2_EQ10_A1	31:0	RW	CH2_EQ10_A1	Filter Coefficient	0
0x9F4	4	CH2_EQ10_A2	31:0	RW	CH2_EQ10_A2	Filter Coefficient	0
0x9F8	4	CH2_EQ11_B0	31:0	RW	CH2_EQ11_B0	Filter Coefficient	0x3f800000
0x9FC	4	CH2_EQ11_B1	31:0	RW	CH2_EQ11_B1	Filter Coefficient	0
0xA00	4	CH2_EQ11_B2	31:0	RW	CH2_EQ11_B2	Filter Coefficient	0
0xA04	4	CH2_EQ11_A1	31:0	RW	CH2_EQ11_A1	Filter Coefficient	0
0xA08	4	CH2_EQ11_A2	31:0	RW	CH2_EQ11_A2	Filter Coefficient	0
0xA0C	4	CH2_EQ12_B0	31:0	RW	CH2_EQ12_B0	Filter Coefficient	0x3f800000
0xA10	4	CH2_EQ12_B1	31:0	RW	CH2_EQ12_B1	Filter Coefficient	0
0xA14	4	CH2_EQ12_B2	31:0	RW	CH2_EQ12_B2	Filter Coefficient	0
0xA18	4	CH2_EQ12_A1	31:0	RW	CH2_EQ12_A1	Filter Coefficient	0
0xA1C	4	CH2_EQ12_A2	31:0	RW	CH2_EQ12_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xA20	4	EQ_SEQ_CTRL	31:20	RW	Reserved	Reserved	0
			19:16	RW	EQ_NUM	0 to 12	0
			15:8	RW	SMOOTH_EQ_TS	4 to 1024 sample delay	0
			7	RW	Reserved	Reserved	0
			6:5	RW	DPEQ_NUM	0 to 3	0x10
			4	R	SMOOTH_METHOD	0: Alpha filter (default) 1: Linear	0
			3	RW	SMOOTH_DONE	Read 0xFF03 bit7 for smooth done (read clear), 1 = Done	0
			2:0	RW	SEQ_UPDATE	000: No update (default) 001: Update BK1/BK2 to SEQ1/SEQ2 010: Update BK1/BK2 to SEQ3/SEQ4 011: Update BK1/BK2 to SEQ5/SEQ6 100: Update BK1/BK2 to SEQ7/SEQ8	0
SMBQ **Note 1: When using SMBQ, DPEQ cannot be used.** **Note 2: Coefficient SMBQ from A24 to BB4**							
0xA24	4	SMOOTH_EQ_ALPHA	31:0	RW	SMOOTH_EQ_ALPHA	Smoot Biquad alpha setting	0
0xA28	4	CH1_SEQ1_B0	31:0	RW	CH1_SEQ1_B0	Filter Coefficient	0x3f800000
0xA2C	4	CH1_SEQ1_B1	31:0	RW	CH1_SEQ1_B1	Filter Coefficient	0
0xA30	4	CH1_SEQ1_B2	31:0	RW	CH1_SEQ1_B2	Filter Coefficient	0
0xA34	4	CH1_SEQ1_A1	31:0	RW	CH1_SEQ1_A1	Filter Coefficient	0
0xA38	4	CH1_SEQ1_A2	31:0	RW	CH1_SEQ1_A2	Filter Coefficient	0
0xA3C	4	CH1_SEQ2_B0	31:0	RW	CH1_SEQ2_B0	Filter Coefficient	0x3f800000
0xA40	4	CH1_SEQ2_B1	31:0	RW	CH1_SEQ2_B1	Filter Coefficient	0
0xA44	4	CH1_SEQ2_B2	31:0	RW	CH1_SEQ2_B2	Filter Coefficient	0
0xA48	4	CH1_SEQ2_A1	31:0	RW	CH1_SEQ2_A1	Filter Coefficient	0
0xA4C	4	CH1_SEQ2_A2	31:0	RW	CH1_SEQ2_A2	Filter Coefficient	0
0xA50	4	CH1_SEQ3_B0	31:0	RW	CH1_SEQ3_B0	Filter Coefficient	0x3f800000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xA54	4	CH1_SEQ3_B1	31:0	RW	CH1_SEQ3_B1	Filter Coefficient	0
0xA58	4	CH1_SEQ3_B2	31:0	RW	CH1_SEQ3_B2	Filter Coefficient	0
0xA5C	4	CH1_SEQ3_A1	31:0	RW	CH1_SEQ3_A1	Filter Coefficient	0
0xA60	4	CH1_SEQ3_A2	31:0	RW	CH1_SEQ3_A2	Filter Coefficient	0
0xA64	4	CH1_SEQ4_B0	31:0	RW	CH1_SEQ4_B0	Filter Coefficient	0x3f800000
0xA68	4	CH1_SEQ4_B1	31:0	RW	CH1_SEQ4_B1	Filter Coefficient	0
0xA6C	4	CH1_SEQ4_B2	31:0	RW	CH1_SEQ4_B2	Filter Coefficient	0
0xA70	4	CH1_SEQ4_A1	31:0	RW	CH1_SEQ4_A1	Filter Coefficient	0
0xA74	4	CH1_SEQ4_A2	31:0	RW	CH1_SEQ4_A2	Filter Coefficient	0
0xA78	4	CH1_SEQ5_B0	31:0	RW	CH1_SEQ5_B0	Filter Coefficient	0x3f800000
0xA7C	4	CH1_SEQ5_B1	31:0	RW	CH1_SEQ5_B1	Filter Coefficient	0
0xA80	4	CH1_SEQ5_B2	31:0	RW	CH1_SEQ5_B2	Filter Coefficient	0
0xA84	4	CH1_SEQ5_A1	31:0	RW	CH1_SEQ5_A1	Filter Coefficient	0
0xA88	4	CH1_SEQ5_A2	31:0	RW	CH1_SEQ5_A2	Filter Coefficient	0
0xA8C	4	CH1_SEQ6_B0	31:0	RW	CH1_SEQ6_B0	Filter Coefficient	0x3f800000
0xA90	4	CH1_SEQ6_B1	31:0	RW	CH1_SEQ6_B1	Filter Coefficient	0
0xA94	4	CH1_SEQ6_B2	31:0	RW	CH1_SEQ6_B2	Filter Coefficient	0
0xA98	4	CH1_SEQ6_A1	31:0	RW	CH1_SEQ6_A1	Filter Coefficient	0
0xA9C	4	CH1_SEQ6_A2	31:0	RW	CH1_SEQ6_A2	Filter Coefficient	0
0xAA0	4	CH1_SEQ7_B0	31:0	RW	CH1_SEQ7_B0	Filter Coefficient	0x3f800000
0xAA4	4	CH1_SEQ7_B1	31:0	RW	CH1_SEQ7_B1	Filter Coefficient	0
0xAA8	4	CH1_SEQ7_B2	31:0	RW	CH1_SEQ7_B2	Filter Coefficient	0
0xAAC	4	CH1_SEQ7_A1	31:0	RW	CH1_SEQ7_A1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xAB0	4	CH1_SEQ7_A2	31:0	RW	CH1_SEQ7_A2	Filter Coefficient	0
0xAB4	4	CH1_SEQ8_B0	31:0	RW	CH1_SEQ8_B0	Filter Coefficient	0x3f800000
0xAB8	4	CH1_SEQ8_B1	31:0	RW	CH1_SEQ8_B1	Filter Coefficient	0
0xABC	4	CH1_SEQ8_B2	31:0	RW	CH1_SEQ8_B2	Filter Coefficient	0
0xAC0	4	CH1_SEQ8_A1	31:0	RW	CH1_SEQ8_A1	Filter Coefficient	0
0xAC4	4	CH1_SEQ8_A2	31:0	RW	CH1_SEQ8_A2	Filter Coefficient	0
0xAC8	4	CH1_SEQBK1_B0	31:0	RW	CH1_SEQBK1_B0	Filter Coefficient	0x3f800000
0xACC	4	CH1_SEQBK1_B1	31:0	RW	CH1_SEQBK1_B1	Filter Coefficient	0
0xAD0	4	CH1_SEQBK1_B2	31:0	RW	CH1_SEQBK1_B2	Filter Coefficient	0
0xAD4	4	CH1_SEQBK1_A1	31:0	RW	CH1_SEQBK1_A1	Filter Coefficient	0
0xAD8	4	CH1_SEQBK1_A2	31:0	RW	CH1_SEQBK1_A2	Filter Coefficient	0
0xADC	4	CH1_SEQBK2_B0	31:0	RW	CH1_SEQBK2_B0	Filter Coefficient	0x3f800000
0xAE0	4	CH1_SEQBK2_B1	31:0	RW	CH1_SEQBK2_B1	Filter Coefficient	0
0xAE4	4	CH1_SEQBK2_B2	31:0	RW	CH1_SEQBK2_B2	Filter Coefficient	0
0xAE8	4	CH1_SEQBK2_A1	31:0	RW	CH1_SEQBK2_A1	Filter Coefficient	0
0xAEC	4	CH1_SEQBK2_A2	31:0	RW	CH1_SEQBK2_A2	Filter Coefficient	0
0xAF0	4	CH2_SEQ1_B0	31:0	RW	CH2_SEQ1_B0	Filter Coefficient	0x3f800000
0xAF4	4	CH2_SEQ1_B1	31:0	RW	CH2_SEQ1_B1	Filter Coefficient	0
0xAF8	4	CH2_SEQ1_B2	31:0	RW	CH2_SEQ1_B2	Filter Coefficient	0
0xAFC	4	CH2_SEQ1_A1	31:0	RW	CH2_SEQ1_A1	Filter Coefficient	0
0xB00	4	CH2_SEQ1_A2	31:0	RW	CH2_SEQ1_A2	Filter Coefficient	0
0xB04	4	CH2_SEQ2_B0	31:0	RW	CH2_SEQ2_B0	Filter Coefficient	0x3f800000
0xB08	4	CH2_SEQ2_B1	31:0	RW	CH2_SEQ2_B1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xB0C	4	CH2_SEQ2_B2	31:0	RW	CH2_SEQ2_B2	Filter Coefficient	0
0xB10	4	CH2_SEQ2_A1	31:0	RW	CH2_SEQ2_A1	Filter Coefficient	0
0xB14	4	CH2_SEQ2_A2	31:0	RW	CH2_SEQ2_A2	Filter Coefficient	0
0xB18	4	CH2_SEQ3_B0	31:0	RW	CH2_SEQ3_B0	Filter Coefficient	0x3f800000
0xB1C	4	CH2_SEQ3_B1	31:0	RW	CH2_SEQ3_B1	Filter Coefficient	0
0xB20	4	CH2_SEQ3_B2	31:0	RW	CH2_SEQ3_B2	Filter Coefficient	0
0xB24	4	CH2_SEQ3_A1	31:0	RW	CH2_SEQ3_A1	Filter Coefficient	0
0xB28	4	CH2_SEQ3_A2	31:0	RW	CH2_SEQ3_A2	Filter Coefficient	0
0xB2C	4	CH2_SEQ4_B0	31:0	RW	CH2_SEQ4_B0	Filter Coefficient	0x3f800000
0xB30	4	CH2_SEQ4_B1	31:0	RW	CH2_SEQ4_B1	Filter Coefficient	0
0xB34	4	CH2_SEQ4_B2	31:0	RW	CH2_SEQ4_B2	Filter Coefficient	0
0xB38	4	CH2_SEQ4_A1	31:0	RW	CH2_SEQ4_A1	Filter Coefficient	0
0xB3C	4	CH2_SEQ4_A2	31:0	RW	CH2_SEQ4_A2	Filter Coefficient	0
0xB40	4	CH2_SEQ5_B0	31:0	RW	CH2_SEQ5_B0	Filter Coefficient	0x3f800000
0xB44	4	CH2_SEQ5_B1	31:0	RW	CH2_SEQ5_B1	Filter Coefficient	0
0xB48	4	CH2_SEQ5_B2	31:0	RW	CH2_SEQ5_B2	Filter Coefficient	0
0xB4C	4	CH2_SEQ5_A1	31:0	RW	CH2_SEQ5_A1	Filter Coefficient	0
0xB50	4	CH2_SEQ5_A2	31:0	RW	CH2_SEQ5_A2	Filter Coefficient	0
0xB54	4	CH2_SEQ6_B0	31:0	RW	CH2_SEQ6_B0	Filter Coefficient	0x3f800000
0xB58	4	CH2_SEQ6_B1	31:0	RW	CH2_SEQ6_B1	Filter Coefficient	0
0xB5C	4	CH2_SEQ6_B2	31:0	RW	CH2_SEQ6_B2	Filter Coefficient	0
0xB60	4	CH2_SEQ6_A1	31:0	RW	CH2_SEQ6_A1	Filter Coefficient	0
0xB64	4	CH2_SEQ6_A2	31:0	RW	CH2_SEQ6_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xB68	4	CH2_SEQ7_B0	31:0	RW	CH2_SEQ7_B0	Filter Coefficient	0x3f800000
0xB6C	4	CH2_SEQ7_B1	31:0	RW	CH2_SEQ7_B1	Filter Coefficient	0
0xB70	4	CH2_SEQ7_B2	31:0	RW	CH2_SEQ7_B2	Filter Coefficient	0
0xB74	4	CH2_SEQ7_A1	31:0	RW	CH2_SEQ7_A1	Filter Coefficient	0
0xB78	4	CH2_SEQ7_A2	31:0	RW	CH2_SEQ7_A2	Filter Coefficient	0
0xB7C	4	CH2_SEQ8_B0	31:0	RW	CH2_SEQ8_B0	Filter Coefficient	0x3f800000
0xB80	4	CH2_SEQ8_B1	31:0	RW	CH2_SEQ8_B1	Filter Coefficient	0
0xB84	4	CH2_SEQ8_B2	31:0	RW	CH2_SEQ8_B2	Filter Coefficient	0
0xB88	4	CH2_SEQ8_A1	31:0	RW	CH2_SEQ8_A1	Filter Coefficient	0
0xB8C	4	CH2_SEQ8_A2	31:0	RW	CH2_SEQ8_A2	Filter Coefficient	0
0xB90	4	CH2_SEQBK1_B0	31:0	RW	CH2_SEQBK1_B0	Filter Coefficient	0x3f800000
0xB94	4	CH2_SEQBK1_B1	31:0	RW	CH2_SEQBK1_B1	Filter Coefficient	0
0xB98	4	CH2_SEQBK1_B2	31:0	RW	CH2_SEQBK1_B2	Filter Coefficient	0
0xB9C	4	CH2_SEQBK1_A1	31:0	RW	CH2_SEQBK1_A1	Filter Coefficient	0
0xBA0	4	CH2_SEQBK1_A2	31:0	RW	CH2_SEQBK1_A2	Filter Coefficient	0
0xBA4	4	CH2_SEQBK2_B0	31:0	RW	CH2_SEQBK2_B0	Filter Coefficient	0x3f800000
0xBA8	4	CH2_SEQBK2_B1	31:0	RW	CH2_SEQBK2_B1	Filter Coefficient	0
0xBAC	4	CH2_SEQBK2_B2	31:0	RW	CH2_SEQBK2_B2	Filter Coefficient	0
0xBB0	4	CH2_SEQBK2_A1	31:0	RW	CH2_SEQBK2_A1	Filter Coefficient	0
0xBB4	4	CH2_SEQBK2_A2	31:0	RW	CH2_SEQBK2_A2	Filter Coefficient	0
DPEQ **Note 1: When using DPEQ, SMBQ cannot be used.** **Note 2: Coefficient from A24 to C1C**							
0xA24	4	DPEQ_MODE_PEAK	31:0	RW	DPEQ_MODE_PEAK	DPEQ Mode select	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xA28	4	CH1_DPEQ1_HL_B0	31:0	RW	CH1_DPEQ1_HL_B0	Filter Coefficient	0x3f800000
0xA2C	4	CH1_DPEQ1_HL_B1	31:0	RW	CH1_DPEQ1_HL_B1	Filter Coefficient	0
0xA30	4	CH1_DPEQ1_HL_B2	31:0	RW	CH1_DPEQ1_HL_B2	Filter Coefficient	0
0xA34	4	CH1_DPEQ1_HL_A1	31:0	RW	CH1_DPEQ1_HL_A1	Filter Coefficient	0
0xA38	4	CH1_DPEQ1_HL_A2	31:0	RW	CH1_DPEQ1_HL_A2	Filter Coefficient	0
0xA3C	4	CH1_DPEQ1_SEN_B0	31:0	RW	CH1_DPEQ1_SEN_B0	Filter Coefficient	0x3f800000
0xA40	4	CH1_DPEQ1_SEN_B1	31:0	RW	CH1_DPEQ1_SEN_B1	Filter Coefficient	0
0xA44	4	CH1_DPEQ1_SEN_B2	31:0	RW	CH1_DPEQ1_SEN_B2	Filter Coefficient	0
0xA48	4	CH1_DPEQ1_SEN_A1	31:0	RW	CH1_DPEQ1_SEN_A1	Filter Coefficient	0
0xA4C	4	CH1_DPEQ1_SEN_A2	31:0	RW	CH1_DPEQ1_SEN_A2	Filter Coefficient	0
0xA50	4	CH1_DPEQ1_LL_B0	31:0	RW	CH1_DPEQ1_LL_B0	Filter Coefficient	0x3f800000
0xA54	4	CH1_DPEQ1_LL_B1	31:0	RW	CH1_DPEQ1_LL_B1	Filter Coefficient	0
0xA58	4	CH1_DPEQ1_LL_B2	31:0	RW	CH1_DPEQ1_LL_B2	Filter Coefficient	0
0xA5C	4	CH1_DPEQ1_LL_A1	31:0	RW	CH1_DPEQ1_LL_A1	Filter Coefficient	0
0xA60	4	CH1_DPEQ1_LL_A2	31:0	RW	CH1_DPEQ1_LL_A2	Filter Coefficient	0
0xA64	4	CH1_DPEQ1_ALPHA	31:0	RW	CH1_DPEQ1_ALPHA	DPEQ Time constant	0
0xA68	4	CH1_DPEQ1_OMEGA	31:0	RW	CH1_DPEQ1_OMEGA	DPEQ Time constant	0
0xA6C	4	CH1_DPEQ1_AT	31:0	RW	CH1_DPEQ1_AT	DPEQ Time constant	0
0xA70	4	CH1_DPEQ1_RT	31:0	RW	CH1_DPEQ1_RT	DPEQ Time constant	0
0xA74	4	CH1_DPEQ1_TH1	31:0	RW	CH1_DPEQ1_TH1	DPEQ Threshold	0
0xA78	4	CH1_DPEQ1_TH2	31:0	RW	CH1_DPEQ1_TH2	DPEQ Threshold	0
0xA7C	4	CH1_DPEQ2_HL_B0	31:0	RW	CH1_DPEQ2_HL_B0	Filter Coefficient	0x3f800000
0xA80	4	CH1_DPEQ2_HL_B1	31:0	RW	CH1_DPEQ2_HL_B1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xA84	4	CH1_DPEQ2_HL_B2	31:0	RW	CH1_DPEQ2_HL_B2	Filter Coefficient	0
0xA88	4	CH1_DPEQ2_HL_A1	31:0	RW	CH1_DPEQ2_HL_A1	Filter Coefficient	0
0xA8C	4	CH1_DPEQ2_HL_A2	31:0	RW	CH1_DPEQ2_HL_A2	Filter Coefficient	0
0xA90	4	CH1_DPEQ2_SEN_B0	31:0	RW	CH1_DPEQ2_SEN_B0	Filter Coefficient	0x3f800000
0xA94	4	CH1_DPEQ2_SEN_B1	31:0	RW	CH1_DPEQ2_SEN_B1	Filter Coefficient	0
0xA98	4	CH1_DPEQ2_SEN_B2	31:0	RW	CH1_DPEQ2_SEN_B2	Filter Coefficient	0
0xA9C	4	CH1_DPEQ2_SEN_A1	31:0	RW	CH1_DPEQ2_SEN_A1	Filter Coefficient	0
0xAA0	4	CH1_DPEQ2_SEN_A2	31:0	RW	CH1_DPEQ2_SEN_A2	Filter Coefficient	0
0xAA4	4	CH1_DPEQ2_LL_B0	31:0	RW	CH1_DPEQ2_LL_B0	Filter Coefficient	0x3f800000
0xAA8	4	CH1_DPEQ2_LL_B1	31:0	RW	CH1_DPEQ2_LL_B1	Filter Coefficient	0
0xAAC	4	CH1_DPEQ2_LL_B2	31:0	RW	CH1_DPEQ2_LL_B2	Filter Coefficient	0
0xAB0	4	CH1_DPEQ2_LL_A1	31:0	RW	CH1_DPEQ2_LL_A1	Filter Coefficient	0
0xAB4	4	CH1_DPEQ2_LL_A2	31:0	RW	CH1_DPEQ2_LL_A2	Filter Coefficient	0
0xAB8	4	Reserve	31:0	RW	Reserve	reserve	0
0xABC	4	Reserve	31:0	RW	Reserve	reserve	0
0xAC0	4	Reserve	31:0	RW	Reserve	reserve	0
0xAC4	4	Reserve	31:0	RW	Reserve	reserve	0
0xAC8	4	Reserve	31:0	RW	Reserve	reserve	0
0xACC	4	Reserve	31:0	RW	Reserve	reserve	0
0xAD0	4	CH1_DPEQ3_HL_B0	31:0	RW	CH1_DPEQ3_HL_B0	Filter Coefficient	0x3f800000
0xAD4	4	CH1_DPEQ3_HL_B1	31:0	RW	CH1_DPEQ3_HL_B1	Filter Coefficient	0
0xAD8	4	CH1_DPEQ3_HL_B2	31:0	RW	CH1_DPEQ3_HL_B2	Filter Coefficient	0
0xADC	4	CH1_DPEQ3_HL_A1	31:0	RW	CH1_DPEQ3_HL_A1	Filter Coefficient	0
0xAE0	4	CH1_DPEQ3_HL_A2	31:0	RW	CH1_DPEQ3_HL_A2	Filter Coefficient	0
0xAE4	4	CH1_DPEQ3_SEN_B0	31:0	RW	CH1_DPEQ3_SEN_B0	Filter Coefficient	0x3f800000

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xAE8	4	CH1_DPEQ3_SEN_B1	31:0	RW	CH1_DPEQ3_SEN_B1	Filter Coefficient	0
0xAEC	4	CH1_DPEQ3_SEN_B2	31:0	RW	CH1_DPEQ3_SEN_B2	Filter Coefficient	0
0xAF0	4	CH1_DPEQ3_SEN_A1	31:0	RW	CH1_DPEQ3_SEN_A1	Filter Coefficient	0
0xAF4	4	CH1_DPEQ3_SEN_A2	31:0	RW	CH1_DPEQ3_SEN_A2	Filter Coefficient	0
0xAF8	4	CH1_DPEQ3_LL_B0	31:0	RW	CH1_DPEQ3_LL_B0	Filter Coefficient	0x3f800000
0xAFC	4	CH1_DPEQ3_LL_B1	31:0	RW	CH1_DPEQ3_LL_B1	Filter Coefficient	0
0xB00	4	CH1_DPEQ3_LL_B2	31:0	RW	CH1_DPEQ3_LL_B2	Filter Coefficient	0
0xB04	4	CH1_DPEQ3_LL_A1	31:0	RW	CH1_DPEQ3_LL_A1	Filter Coefficient	0
0xB08	4	CH1_DPEQ3_LL_A2	31:0	RW	CH1_DPEQ3_LL_A2	Filter Coefficient	0
0xB0C	4	CH1_DPEQ3_ALPHA	31:0	RW	CH1_DPEQ3_ALPHA	DPEQ Time constant	0
0xB10	4	CH1_DPEQ3_OMEGA	31:0	RW	CH1_DPEQ3_OMEGA	DPEQ Time constant	0
0xB14	4	CH1_DPEQ3_AT	31:0	RW	CH1_DPEQ3_AT	DPEQ Time constant	0
0xB18	4	CH1_DPEQ3_RT	31:0	RW	CH1_DPEQ3_RT	DPEQ Time constant	0
0xB1C	4	CH1_DPEQ3_TH1	31:0	RW	CH1_DPEQ3_TH1	DPEQ Threshold	0
0xB20	4	CH1_DPEQ3_TH2	31:0	RW	CH1_DPEQ3_TH2	DPEQ Threshold	0
0xB24	4	CH2_DPEQ1_HL_B0	31:0	RW	CH2_DPEQ1_HL_B0	Filter Coefficient	0x3f800000
0xB28	4	CH2_DPEQ1_HL_B1	31:0	RW	CH2_DPEQ1_HL_B1	Filter Coefficient	0
0xB2C	4	CH2_DPEQ1_HL_B2	31:0	RW	CH2_DPEQ1_HL_B2	Filter Coefficient	0
0xB30	4	CH2_DPEQ1_HL_A1	31:0	RW	CH2_DPEQ1_HL_A1	Filter Coefficient	0
0xB34	4	CH2_DPEQ1_HL_A2	31:0	RW	CH2_DPEQ1_HL_A2	Filter Coefficient	0
0xB38	4	CH2_DPEQ1_SEN_B0	31:0	RW	CH2_DPEQ1_SEN_B0	Filter Coefficient	0x3f800000
0xB3C	4	CH2_DPEQ1_SEN_B1	31:0	RW	CH2_DPEQ1_SEN_B1	Filter Coefficient	0
0xB40	4	CH2_DPEQ1_SEN_B2	31:0	RW	CH2_DPEQ1_SEN_B2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xB44	4	CH2_DPEQ1_SEN_A1	31:0	RW	CH2_DPEQ1_SEN_A1	Filter Coefficient	0
0xB48	4	CH2_DPEQ1_SEN_A2	31:0	RW	CH2_DPEQ1_SEN_A2	Filter Coefficient	0
0xB4C	4	CH2_DPEQ1_LL_B0	31:0	RW	CH2_DPEQ1_LL_B0	Filter Coefficient	0x3f800000
0xB50	4	CH2_DPEQ1_LL_B1	31:0	RW	CH2_DPEQ1_LL_B1	Filter Coefficient	0
0xB54	4	CH2_DPEQ1_LL_B2	31:0	RW	CH2_DPEQ1_LL_B2	Filter Coefficient	0
0xB58	4	CH2_DPEQ1_LL_A1	31:0	RW	CH2_DPEQ1_LL_A1	Filter Coefficient	0
0xB5C	4	CH2_DPEQ1_LL_A2	31:0	RW	CH2_DPEQ1_LL_A2	Filter Coefficient	0
0xB60	4	CH2_DPEQ1_ALPHA	31:0	RW	CH2_DPEQ1_ALPHA	DPEQ Time constant	0
0xB64	4	CH2_DPEQ1_OMEGA	31:0	RW	CH2_DPEQ1_OMEGA	DPEQ Time constant	0
0xB68	4	CH2_DPEQ1_AT	31:0	RW	CH2_DPEQ1_AT	DPEQ Time constant	0
0xB6C	4	CH2_DPEQ1_RT	31:0	RW	CH2_DPEQ1_RT	DPEQ Time constant	0
0xB70	4	CH2_DPEQ1_TH1	31:0	RW	CH2_DPEQ1_TH1	DPEQ Threshold	0
0xB74	4	CH2_DPEQ1_TH2	31:0	RW	CH2_DPEQ1_TH2	DPEQ Threshold	0
0xB78	4	CH2_DPEQ2_HL_B0	31:0	RW	CH2_DPEQ2_HL_B0	Filter Coefficient	0x3f800000
0xB7C	4	CH2_DPEQ2_HL_B1	31:0	RW	CH2_DPEQ2_HL_B1	Filter Coefficient	0
0xB80	4	CH2_DPEQ2_HL_B2	31:0	RW	CH2_DPEQ2_HL_B2	Filter Coefficient	0
0xB84	4	CH2_DPEQ2_HL_A1	31:0	RW	CH2_DPEQ2_HL_A1	Filter Coefficient	0
0xB88	4	CH2_DPEQ2_HL_A2	31:0	RW	CH2_DPEQ2_HL_A2	Filter Coefficient	0
0xB8C	4	CH2_DPEQ2_SEN_B0	31:0	RW	CH2_DPEQ2_SEN_B0	Filter Coefficient	0x3f800000
0xB90	4	CH2_DPEQ2_SEN_B1	31:0	RW	CH2_DPEQ2_SEN_B1	Filter Coefficient	0
0xB94	4	CH2_DPEQ2_SEN_B2	31:0	RW	CH2_DPEQ2_SEN_B2	Filter Coefficient	0
0xB98	4	CH2_DPEQ2_SEN_A1	31:0	RW	CH2_DPEQ2_SEN_A1	Filter Coefficient	0
0xB9C	4	CH2_DPEQ2_SEN_A2	31:0	RW	CH2_DPEQ2_SEN_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xBA0	4	CH2_DPEQ2_LL_B0	31:0	RW	CH2_DPEQ2_LL_B0	Filter Coefficient	0x3f800000
0xBA4	4	CH2_DPEQ2_LL_B1	31:0	RW	CH2_DPEQ2_LL_B1	Filter Coefficient	0
0xBA8	4	CH2_DPEQ2_LL_B2	31:0	RW	CH2_DPEQ2_LL_B2	Filter Coefficient	0
0xBAC	4	CH2_DPEQ2_LL_A1	31:0	RW	CH2_DPEQ2_LL_A1	Filter Coefficient	0
0xBB0	4	CH2_DPEQ2_LL_A2	31:0	RW	CH2_DPEQ2_LL_A2	Filter Coefficient	0
0xBB4	4	Reserve	31:0	RW	Reserve	reserve	0
0xBB8	4	Reserve	31:0	RW	Reserve	reserve	0
0xBBC	4	Reserve	31:0	RW	Reserve	reserve	0
0xBC0	4	Reserve	31:0	RW	Reserve	reserve	0
0xBC4	4	Reserve	31:0	RW	Reserve	reserve	0
0xBC8	4	Reserve	31:0	RW	Reserve	reserve	0
0xBCC	4	CH2_DPEQ3_HL_B0	31:0	RW	CH2_DPEQ3_HL_B0	Filter Coefficient	0x3f800000
0xBD0	4	CH2_DPEQ3_HL_B1	31:0	RW	CH2_DPEQ3_HL_B1	Filter Coefficient	0
0xBD4	4	CH2_DPEQ3_HL_B2	31:0	RW	CH2_DPEQ3_HL_B2	Filter Coefficient	0
0xBD8	4	CH2_DPEQ3_HL_A1	31:0	RW	CH2_DPEQ3_HL_A1	Filter Coefficient	0
0xBDC	4	CH2_DPEQ3_HL_A2	31:0	RW	CH2_DPEQ3_HL_A2	Filter Coefficient	0
0xBE0	4	CH2_DPEQ3_SEN_B0	31:0	RW	CH2_DPEQ3_SEN_B0	Filter Coefficient	0x3f800000
0xBE4	4	CH2_DPEQ3_SEN_B1	31:0	RW	CH2_DPEQ3_SEN_B1	Filter Coefficient	0
0xBE8	4	CH2_DPEQ3_SEN_B2	31:0	RW	CH2_DPEQ3_SEN_B2	Filter Coefficient	0
0xBEC	4	CH2_DPEQ3_SEN_A1	31:0	RW	CH2_DPEQ3_SEN_A1	Filter Coefficient	0
0xBF0	4	CH2_DPEQ3_SEN_A2	31:0	RW	CH2_DPEQ3_SEN_A2	Filter Coefficient	0
0xBF4	4	CH2_DPEQ3_LL_B0	31:0	RW	CH2_DPEQ3_LL_B0	Filter Coefficient	0x3f800000
0xBF8	4	CH2_DPEQ3_LL_B1	31:0	RW	CH2_DPEQ3_LL_B1	Filter Coefficient	0
0xBFC	4	CH2_DPEQ3_LL_B2	31:0	RW	CH2_DPEQ3_LL_B2	Filter Coefficient	0
0xC00	4	CH2_DPEQ3_LL_A1	31:0	RW	CH2_DPEQ3_LL_A1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xC04	4	CH2_DPEQ3_LL_A2	31:0	RW	CH2_DPEQ3_LL_A2	Filter Coefficient	0
0xC08	4	CH2_DPEQ3_ALPHA	31:0	RW	CH2_DPEQ3_ALPHA	DPEQ Time constant	0
0xC0C	4	CH2_DPEQ3_OMEGA	31:0	RW	CH2_DPEQ3_OMEGA	DPEQ Time constant	0
0xC10	4	CH2_DPEQ3_AT	31:0	RW	CH2_DPEQ3_AT	DPEQ Time constant	0
0xC14	4	CH2_DPEQ3_RT	31:0	RW	CH2_DPEQ3_RT	DPEQ Time constant	0
0xC18	4	CH2_DPEQ3_TH1	31:0	RW	CH2_DPEQ3_TH1	DPEQ Threshold	0
0xC1C	4	CH2_DPEQ3_TH2	31:0	RW	CH2_DPEQ3_TH2	DPEQ Threshold	0
Surround **Note 1: When using Surround, DPEQ cannot be used.** **Note 2: Coefficient from C20 to C44**							
0xC20	4	SURROUND_H1_B0	31:0	RW	SURROUND_H1_B0	Filter Coefficient	0x3f800000
0xC24	4	SURROUND_H1_B1	31:0	RW	SURROUND_H1_B1	Filter Coefficient	0
0xC28	4	SURROUND_H1_B2	31:0	RW	SURROUND_H1_B2	Filter Coefficient	0
0xC2C	4	SURROUND_H1_A1	31:0	RW	SURROUND_H1_A1	Filter Coefficient	0
0xC30	4	SURROUND_H1_A2	31:0	RW	SURROUND_H1_A2	Filter Coefficient	0
0xC34	4	SURROUND_H2_B0	31:0	RW	SURROUND_H2_B0	Filter Coefficient	0x3f800000
0xC38	4	SURROUND_H2_B1	31:0	RW	SURROUND_H2_B1	Filter Coefficient	0
0xC3C	4	SURROUND_H2_B2	31:0	RW	SURROUND_H2_B2	Filter Coefficient	0
0xC40	4	SURROUND_H2_A1	31:0	RW	SURROUND_H2_A1	Filter Coefficient	0
0xC44	4	SURROUND_H2_A2	31:0	RW	SURROUND_H2_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
CCS **Note 1: When using CCS, Surround cannot be used.** **Note 2: Coefficient from C20 to C44**							
0xC20	4	CCS_HP_B0	31:0	RW	CCS_HP_B0	Filter Coefficient	0x3f800000
0xC24	4	CCS_HP_B1	31:0	RW	CCS_HP_B1	Filter Coefficient	0
0xC28	4	CCS_HP_B2	31:0	RW	CCS_HP_B2	Filter Coefficient	0
0xC2C	4	CCS_HP_A1	31:0	RW	CCS_HP_A1	Filter Coefficient	0
0xC30	4	CCS_HP_A2	31:0	RW	CCS_HP_A2	Filter Coefficient	0
0xC34	4	CCS_LP_B0	31:0	RW	CCS_LP_B0	Filter Coefficient	0x3f800000
0xC38	4	CCS_LP_B1	31:0	RW	CCS_LP_B1	Filter Coefficient	0
0xC3C	4	CCS_LP_B2	31:0	RW	CCS_LP_B2	Filter Coefficient	0
0xC40	4	CCS_LP_A1	31:0	RW	CCS_LP_A1	Filter Coefficient	0
0xC44	4	CCS_LP_A2	31:0	RW	CCS_LP_A2	Filter Coefficient	0
0xC48	4	Reserved	31:30	RW	Reserved	Reserved	0
		HYS_BYPASS	29	RW	HYS_ BYPASS	DRC hysteresis	0
		DRC4_PEAK	28	RW	DRC4_PEAK	DRC4 Peak mode	0
		DRC3_PEAK	27	RW	DRC3_PEAK	DRC3 Peak mode	0
		DRC2_PEAK	26	RW	DRC2_PEAK	DRC2 Peak mode	0
		DRC1_PEAK	25	RW	DRC1_PEAK	DRC1 Peak mode	0
		DRC4_ON	24	RW	DRC4_ON	DRC4 enable	0
		DRC3_ON	23	RW	DRC3_ON	DRC3 enable	0
		DRC2_ON	22	RW	DRC2_ON	DRC2 enable	0
		DRC1_ON	21	RW	DRC1_ON	DRC1 enable	0
		DRC4_N_EN	20	RW	DRC4_N_EN	DRC4 noise gate enable	0
		DRC3_N_EN	19	RW	DRC3_N_EN	DRC3 noise gate enable	0
		DRC2_N_EN	18	RW	DRC2_N_EN	DRC2 noise gate enable	0
		DRC1_N_EN	17	RW	DRC1_N_EN	DRC1 noise gate enable	0
		HB_MUTE	16	RW	HB_MUTE	DRC3 High band mute	0
		MB_MUTE	15	RW	MB_MUTE	DRC2 High band mute	0
		LB_MUTE	14	RW	LB_MUTE	DRC1 High band mute	0
		SKIP_BQ1_L_ MBAND	13	RW	SKIP_BQ1_L _MBAND	SKIP_BQ1_L_MBAND	0
		SKIP_BQ2_L_ MBAND	12	RW	SKIP_BQ2_L _MBAND	SKIP_BQ2_L_MBAND	0
		SKIP_BQ1_R_ MBAND	11	RW	SKIP_BQ1_ R_MBAND	SKIP_BQ1_R_MBAND	0
		SKIP_BQ2_R_ MBAND	10	RW	SKIP_BQ2_ R_MBAND	SKIP_BQ2_R_MBAND	0
		SKIP_BQ1_L_ HBAND	9	RW	SKIP_BQ1_L _HBAND	SKIP_BQ1_L_HBAND	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
		SKIP_BQ1_R_HBAND	8	RW	SKIP_BQ1_R_HBAND	SKIP_BQ1_R_HBAND	0
		SKIP_BQ1_L_LBAND	7	RW	SKIP_BQ1_L_LBAND	SKIP_BQ1_L_LBAND	0
		SKIP_BQ1_R_LBAND	6	RW	SKIP_BQ1_R_LBAND	SKIP_BQ1_R_LBAND	0
		SKIP_DRC_L_HPF	5	RW	SKIP_DRC_L_HPF	SKIP_DRC_L_HPF	0
		SKIP_DRC_H_LPF	4	RW	SKIP_DRC_H_LPF	SKIP_DRC_H_LPF	0
		SKIP_DRC_H_HPF	3	RW	SKIP_DRC_H_HPF	SKIP_DRC_H_HPF	0
		SKIP_DRC_L_LPF	2	RW	SKIP_DRC_L_LPF	SKIP_DRC_L_LPF	0
		SKIP_DRC_APB	1	RW	SKIP_DRC_APB	SKIP_DRC_APB	0
		PREDICT_O_ENABLE	0	RW	PREDICT_O_ENABLE	PREDICT_O_ENABLE	0
0xC4C	4	LB_CH1_BQ1_B0	31:0	RW	LB_CH1_BQ1_B0	Filter Coefficient	0x3f800000
0xC50	4	LB_CH1_BQ1_B1	31:0	RW	LB_CH1_BQ1_B1	Filter Coefficient	0
0xC54	4	LB_CH1_BQ1_B2	31:0	RW	LB_CH1_BQ1_B2	Filter Coefficient	0
0xC58	4	LB_CH1_BQ1_A1	31:0	RW	LB_CH1_BQ1_A1	Filter Coefficient	0
0xC5C	4	LB_CH1_BQ1_A2	31:0	RW	LB_CH1_BQ1_A2	Filter Coefficient	0
0xC60	4	MB_CH1_BQ1_B0	31:0	RW	MB_CH1_BQ1_B0	Filter Coefficient	0x3f800000
0xC64	4	MB_CH1_BQ1_B1	31:0	RW	MB_CH1_BQ1_B1	Filter Coefficient	0
0xC68	4	MB_CH1_BQ1_B2	31:0	RW	MB_CH1_BQ1_B2	Filter Coefficient	0
0xC6C	4	MB_CH1_BQ1_A1	31:0	RW	MB_CH1_BQ1_A1	Filter Coefficient	0
0xC70	4	MB_CH1_BQ1_A2	31:0	RW	MB_CH1_BQ1_A2	Filter Coefficient	0
0xC74	4	MB_CH1_BQ2_B0	31:0	RW	MB_CH1_BQ2_B0	Filter Coefficient	0x3f800000
0xC78	4	MB_CH1_BQ2_B1	31:0	RW	MB_CH1_BQ2_B1	Filter Coefficient	0
0xC7C	4	MB_CH1_BQ2_B2	31:0	RW	MB_CH1_BQ2_B2	Filter Coefficient	0
0xC80	4	MB_CH1_BQ2_A1	31:0	RW	MB_CH1_BQ2_A1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xC84	4	MB_CH1_BQ2_A2	31:0	RW	MB_CH1_BQ2_A2	Filter Coefficient	0
0xC88	4	HB_CH1_BQ1_B0	31:0	RW	HB_CH1_BQ1_B0	Filter Coefficient	0x3f800000
0xC8C	4	HB_CH1_BQ1_B1	31:0	RW	HB_CH1_BQ1_B1	Filter Coefficient	0
0xC90	4	HB_CH1_BQ1_B2	31:0	RW	HB_CH1_BQ1_B2	Filter Coefficient	0
0xC94	4	HB_CH1_BQ1_A1	31:0	RW	HB_CH1_BQ1_A1	Filter Coefficient	0
0xC98	4	HB_CH1_BQ1_A2	31:0	RW	HB_CH1_BQ1_A2	Filter Coefficient	0
0xC9C	4	LB_CH1_BQ2_B0	31:0	RW	LB_CH1_BQ2_B0	Filter Coefficient	0x3f800000
0xCA0	4	LB_CH1_BQ2_B1	31:0	RW	LB_CH1_BQ2_B1	Filter Coefficient	0
0xCA4	4	LB_CH1_BQ2_B2	31:0	RW	LB_CH1_BQ2_B2	Filter Coefficient	0
0xCA8	4	LB_CH1_BQ2_A1	31:0	RW	LB_CH1_BQ2_A1	Filter Coefficient	0
0xCAC	4	LB_CH1_BQ2_A2	31:0	RW	LB_CH1_BQ2_A2	Filter Coefficient	0
0xCB0	4	LB_CH2_BQ1_B0	31:0	RW	LB_CH2_BQ1_B0	Filter Coefficient	0x3f800000
0xCB4	4	LB_CH2_BQ1_B1	31:0	RW	LB_CH2_BQ1_B1	Filter Coefficient	0
0xCB8	4	LB_CH2_BQ1_B2	31:0	RW	LB_CH2_BQ1_B2	Filter Coefficient	0
0xCBC	4	LB_CH2_BQ1_A1	31:0	RW	LB_CH2_BQ1_A1	Filter Coefficient	0
0xCC0	4	LB_CH2_BQ1_A2	31:0	RW	LB_CH2_BQ1_A2	Filter Coefficient	0
0xCC4	4	MB_CH2_BQ1_B0	31:0	RW	MB_CH2_BQ1_B0	Filter Coefficient	0x3f800000
0xCC8	4	MB_CH2_BQ1_B1	31:0	RW	MB_CH2_BQ1_B1	Filter Coefficient	0
0xCCC	4	MB_CH2_BQ1_B2	31:0	RW	MB_CH2_BQ1_B2	Filter Coefficient	0
0xCD0	4	MB_CH2_BQ1_A1	31:0	RW	MB_CH2_BQ1_A1	Filter Coefficient	0
0xCD4	4	MB_CH2_BQ1_A2	31:0	RW	MB_CH2_BQ1_A2	Filter Coefficient	0
0xCD8	4	MB_CH2_BQ2_B0	31:0	RW	MB_CH2_BQ2_B0	Filter Coefficient	0x3f800000
0xCDC	4	MB_CH2_BQ2_B1	31:0	RW	MB_CH2_BQ2_B1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xCE0	4	MB_CH2_BQ2_B2	31:0	RW	MB_CH2_BQ2_B2	Filter Coefficient	0
0xCE4	4	MB_CH2_BQ2_A1	31:0	RW	MB_CH2_BQ2_A1	Filter Coefficient	0
0xCE8	4	MB_CH2_BQ2_A2	31:0	RW	MB_CH2_BQ2_A2	Filter Coefficient	0
0xCEC	4	HB_CH2_BQ1_B0	31:0	RW	HB_CH2_BQ1_B0	Filter Coefficient	0x3f800000
0xCF0	4	HB_CH2_BQ1_B1	31:0	RW	HB_CH2_BQ1_B1	Filter Coefficient	0
0xCF4	4	HB_CH2_BQ1_B2	31:0	RW	HB_CH2_BQ1_B2	Filter Coefficient	0
0xCF8	4	HB_CH2_BQ1_A1	31:0	RW	HB_CH2_BQ1_A1	Filter Coefficient	0
0xCFC	4	HB_CH2_BQ1_A2	31:0	RW	HB_CH2_BQ1_A2	Filter Coefficient	0
0xD00	4	LB_CH2_BQ2_B0	31:0	RW	LB_CH2_BQ2_B0	Filter Coefficient	0x3f800000
0xD04	4	LB_CH2_BQ2_B1	31:0	RW	LB_CH2_BQ2_B1	Filter Coefficient	0
0xD08	4	LB_CH2_BQ2_B2	31:0	RW	LB_CH2_BQ2_B2	Filter Coefficient	0
0xD0C	4	LB_CH2_BQ2_A1	31:0	RW	LB_CH2_BQ2_A1	Filter Coefficient	0
0xD10	4	LB_CH2_BQ2_A2	31:0	RW	LB_CH2_BQ2_A2	Filter Coefficient	0
0xD14	4	DRC1 RMS ALPHA	31:0	RW	DRC1 RMS ALPHA	DRC1 RMS ALPHA	0
0xD18	4	DRC1 RMS OMEGA	31:0	RW	DRC1 RMS OMEGA	DRC1 RMS OMEGA	0
0xD1C	4	DRC1 GAIN AT	31:0	RW	DRC1 GAIN AT	DRC1 GAIN AT	0
0xD20	4	DRC1 GAIN RT	31:0	RW	DRC1 GAIN RT	DRC1 GAIN RT	0
0xD24	4	DRC1 TH0	31:0	RW	DRC1 TH0	DRC1 TH0	0
0xD28	4	DRC1 RATIO	31:0	RW	DRC1 RATIO	DRC1 RATIO	0
0xD2C	4	DRC1 MAKEUP	31:0	RW	DRC1 MAKEUP	DRC1 MAKEUP	0
0xD30	4	DRC2 RMS ALPHA	31:0	RW	DRC2 RMS ALPHA	DRC2 RMS ALPHA	0
0xD34	4	DRC2 RMS OMEGA	31:0	RW	DRC2 RMS OMEGA	DRC2 RMS OMEGA	0
0xD38	4	DRC2 GAIN AT	31:0	RW	DRC2 GAIN AT	DRC2 GAIN AT	0
0xD3C	4	DRC2 GAIN RT	31:0	RW	DRC2 GAIN RT	DRC2 GAIN RT	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xD40	4	DRC2 TH0	31:0	RW	DRC2 TH0	DRC2 TH0	0
0xD44	4	DRC2 RATIO	31:0	RW	DRC2 RATIO	DRC2 RATIO	0
0xD48	4	DRC2 MAKEUP	31:0	RW	DRC2 MAKEUP	DRC2 MAKEUP	0
0xD4C	4	DRC3 RMS ALPHA	31:0	RW	DRC3 RMS ALPHA	DRC3 RMS ALPHA	0
0xD50	4	DRC3 RMS OMEGA	31:0	RW	DRC3 RMS OMEGA	DRC3 RMS OMEGA	0
0xD54	4	DRC3 GAIN AT	31:0	RW	DRC3 GAIN AT	DRC3 GAIN AT	0
0xD58	4	DRC3 GAIN RT	31:0	RW	DRC3 GAIN RT	DRC3 GAIN RT	0
0xD5C	4	DRC3 TH0	31:0	RW	DRC3 TH0	DRC3 TH0	0
0xD60	4	DRC3 RATIO	31:0	RW	DRC3 RATIO	DRC3 RATIO	0
0xD64	4	DRC3 MAKEUP	31:0	RW	DRC3 MAKEUP	DRC3 MAKEUP	0
0xD68	4	CH1_OUT_MIX_L	31:0	RW	CH1_OUT_MIX_L	Ch1 L band mixer	0x3f800000
0xD6C	4	CH1_OUT_MIX_M	31:0	RW	CH1_OUT_MIX_M	Ch1 M band mixer	0x3f800000
0xD70	4	CH1_OUT_MIX_H	31:0	RW	CH1_OUT_MIX_H	Ch H band mixer	0x3f800000
0xD74	4	CH2_OUT_MIX_L	31:0	RW	CH2_OUT_MIX_L	Ch2 L band mixer	0x3f800000
0xD78	4	CH2_OUT_MIX_M	31:0	RW	CH2_OUT_MIX_M	Ch2 M band mixer	0x3f800000
0xD7C	4	CH2_OUT_MIX_H	31:0	RW	CH2_OUT_MIX_H	Ch2 H band mixer	0x3f800000
0xD80	4	CH1_OUT_MIX_0	31:0	RW	CH1_OUT_MIX_0	Ch1 output mixer	0x3f800000
0xD84	4	CH1_OUT_MIX_1	31:0	RW	CH1_OUT_MIX_1	Ch1 output mixer	0
0xD88	4	CH2_OUT_MIX_0	31:0	RW	CH2_OUT_MIX_0	Ch2 output mixer	0
0xD8C	4	CH2_OUT_MIX_1	31:0	RW	CH2_OUT_MIX_1	Ch2 output mixer	0x3f800000
0xD90	4	POST_SCALE	31:0	RW	POST_SCALE	POST_SCALE	0x3f800000
0xD94	4	DRC_TH2	31:0	RW	DRC_TH2	DRC_TH2	0
0xD98	4	DRC4_DELAY	31:0	RW	DRC4_DELAY	DRC4_DELAY	0
0xD9C	4	DRC4_ALPHA	31:0	RW	DRC4_ALPHA	DRC4_ALPHA	0
0xDA0	4	DRC4_OMEGA	31:0	RW	DRC4_OMEGA	DRC4_OMEGA	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xDA4	4	DRC4_AT	31:0	RW	DRC4_AT	DRC4_AT	0
0xDA8	4	DRC4 RT	31:0	RW	DRC4 RT	DRC4 RT	0
0xDAC	4	DRC4 TH0	31:0	RW	DRC4 TH0	DRC4 TH0	0
0xDB0	4	DRC4 RATIO	31:0	RW	DRC4 RATIO	DRC4 RATIO	0
0xDB4	4	DRC4 MAKEUP	31:0	RW	DRC4 MAKEUP	DRC4 MAKEUP	0
0xDB8	4	POST_IDF	31:0	RW	POST_IDF	POST_IDF	0x3f800000
0xDBC	4	COMP_B0	31:0	RW	COMP_B0	COMP_B0	0
0xDC0	4	COMP_B1	31:0	RW	COMP_B1	COMP_B1	0
0xDC4	4	COMP_B2	31:0	RW	COMP_B2	COMP_B2	0
0xDC8	4	COMP_B3	31:0	RW	COMP_B3	COMP_B3	0
0xDCC	4	Reserve	31:0	RW	Reserve	Reserve	0
0xDD0	4	Reserve	31:0	RW	Reserve	Reserve	0
0xDD4	4	CH1_OUT_HPF1_B0	31:0	RW	CH1_OUT_HPF1_B0	Filter Coefficient	0x3f800000
0xDD8	4	CH1_OUT_HPF1_B1	31:0	RW	CH1_OUT_HPF1_B1	Filter Coefficient	0
0xDDC	4	CH1_OUT_HPF1_B2	31:0	RW	CH1_OUT_HPF1_B2	Filter Coefficient	0
0xDE0	4	CH1_OUT_HPF1_A1	31:0	RW	CH1_OUT_HPF1_A1	Filter Coefficient	0
0xDE4	4	CH1_OUT_HPF1_A2	31:0	RW	CH1_OUT_HPF1_A2	Filter Coefficient	0
0xDE8	4	CH1_OUT_HPF2_B0	31:0	RW	CH1_OUT_HPF2_B0	Filter Coefficient	0x3f800000
0xDEC	4	CH1_OUT_HPF2_B1	31:0	RW	CH1_OUT_HPF2_B1	Filter Coefficient	0
0xDF0	4	CH1_OUT_HPF2_B2	31:0	RW	CH1_OUT_HPF2_B2	Filter Coefficient	0
0xDF4	4	CH1_OUT_HPF2_A1	31:0	RW	CH1_OUT_HPF2_A1	Filter Coefficient	0
0xDF8	4	CH1_OUT_HPF2_A2	31:0	RW	CH1_OUT_HPF2_A2	Filter Coefficient	0
0xDFC	4	CH2_OUT_HPF1_B0	31:0	RW	CH2_OUT_HPF1_B0	Filter Coefficient	0x3f800000
0xE00	4	CH2_OUT_HPF1_B1	31:0	RW	CH2_OUT_HPF1_B1	Filter Coefficient	0
0xE04	4	CH2_OUT_HPF1_B2	31:0	RW	CH2_OUT_HPF1_B2	Filter Coefficient	0
0xE08	4	CH2_OUT_HPF1_A1	31:0	RW	CH2_OUT_HPF1_A1	Filter Coefficient	0
0xE0C	4	CH2_OUT_HPF1_A2	31:0	RW	CH2_OUT_HPF1_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xE10	4	CH2_OUT_HPF2_B0	31:0	RW	CH2_OUT_HPF2_B0	Filter Coefficient	0x3f800000
0xE14	4	CH2_OUT_HPF2_B1	31:0	RW	CH2_OUT_HPF2_B1	Filter Coefficient	0
0xE18	4	CH2_OUT_HPF2_B2	31:0	RW	CH2_OUT_HPF2_B2	Filter Coefficient	0
0xE1C	4	CH2_OUT_HPF2_A1	31:0	RW	CH2_OUT_HPF2_A1	Filter Coefficient	0
0xE20	4	CH2_OUT_HPF2_A2	31:0	RW	CH2_OUT_HPF2_A2	Filter Coefficient	0
0xE24	4	SDO1_OUT_MIX_1	31:0	RW	SDO1_OUT_MIX_1	SDO1_OUT_MIX_1	0x3f800000
0xE28	4	SDO1_OUT_MIX_0	31:0	RW	SDO1_OUT_MIX_0	SDO1_OUT_MIX_0	0
0xE2C	4	SDO2_OUT_MIX_1	31:0	RW	SDO2_OUT_MIX_1	SDO2_OUT_MIX_1	0
0xE30	4	SDO2_OUT_MIX_0	31:0	RW	SDO2_OUT_MIX_0	SDO2_OUT_MIX_0	0x3f800000
0xE34	4	SDO1_BQ1_B0	31:0	RW	SDO1_BQ1_B0	Filter Coefficient	0x3f800000
0xE38	4	SDO1_BQ1_B1	31:0	RW	SDO1_BQ1_B1	Filter Coefficient	0
0xE3C	4	SDO1_BQ1_B2	31:0	RW	SDO1_BQ1_B2	Filter Coefficient	0
0xE40	4	SDO1_BQ1_A1	31:0	RW	SDO1_BQ1_A1	Filter Coefficient	0
0xE44	4	SDO1_BQ1_A2	31:0	RW	SDO1_BQ1_A2	Filter Coefficient	0
0xE48	4	SDO1_BQ2_B0	31:0	RW	SDO1_BQ2_B0	Filter Coefficient	0x3f800000
0xE4C	4	SDO1_BQ2_B1	31:0	RW	SDO1_BQ2_B1	Filter Coefficient	0
0xE50	4	SDO1_BQ2_B2	31:0	RW	SDO1_BQ2_B2	Filter Coefficient	0
0xE54	4	SDO1_BQ2_A1	31:0	RW	SDO1_BQ2_A1	Filter Coefficient	0
0xE58	4	SDO1_BQ2_A2	31:0	RW	SDO1_BQ2_A2	Filter Coefficient	0
0xE5C	4	SDO1_BQ3_B0	31:0	RW	SDO1_BQ3_B0	Filter Coefficient	0x3f800000
0xE60	4	SDO1_BQ3_B1	31:0	RW	SDO1_BQ3_B1	Filter Coefficient	0
0xE64	4	SDO1_BQ3_B2	31:0	RW	SDO1_BQ3_B2	Filter Coefficient	0
0xE68	4	SDO1_BQ3_A1	31:0	RW	SDO1_BQ3_A1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xE6C	4	SDO1_BQ3_A2	31:0	RW	SDO1_BQ3_A2	Filter Coefficient	0
0xE70	4	SDO1_BQ4_B0	31:0	RW	SDO1_BQ4_B0	Filter Coefficient	0x3f800000
0xE74	4	SDO1_BQ4_B1	31:0	RW	SDO1_BQ4_B1	Filter Coefficient	0
0xE78	4	SDO1_BQ4_B2	31:0	RW	SDO1_BQ4_B2	Filter Coefficient	0
0xE7C	4	SDO1_BQ4_A2	31:0	RW	SDO1_BQ4_A2	Filter Coefficient	0
0xE80	4	SDO1_BQ4_A0	31:0	RW	SDO1_BQ4_A0	Filter Coefficient	0
0xE84	4	SDO1_BQ5_B0	31:0	RW	SDO1_BQ5_B0	Filter Coefficient	0x3f800000
0xE88	4	SDO1_BQ5_B1	31:0	RW	SDO1_BQ5_B1	Filter Coefficient	0
0xE8C	4	SDO1_BQ5_B2	31:0	RW	SDO1_BQ5_B2	Filter Coefficient	0
0xE90	4	SDO1_BQ5_A1	31:0	RW	SDO1_BQ5_A1	Filter Coefficient	0
0xE94	4	SDO1_BQ5_A2	31:0	RW	SDO1_BQ5_A2	Filter Coefficient	0
0xE98	4	SDO2_BQ1_B0	31:0	RW	SDO2_BQ1_B0	Filter Coefficient	0x3f800000
0xE9C	4	SDO2_BQ1_B1	31:0	RW	SDO2_BQ1_B1	Filter Coefficient	0
0xEA0	4	SDO2_BQ1_B2	31:0	RW	SDO2_BQ1_B2	Filter Coefficient	0
0xEA4	4	SDO2_BQ1_A1	31:0	RW	SDO2_BQ1_A1	Filter Coefficient	0
0xEA8	4	SDO2_BQ1_A2	31:0	RW	SDO2_BQ1_A2	Filter Coefficient	0
0xEAC	4	SDO2_BQ2_B0	31:0	RW	SDO2_BQ2_B0	Filter Coefficient	0x3f800000
0xEB0	4	SDO2_BQ2_B1	31:0	RW	SDO2_BQ2_B1	Filter Coefficient	0
0xEB4	4	SDO2_BQ2_B2	31:0	RW	SDO2_BQ2_B2	Filter Coefficient	0
0xEB8	4	SDO2_BQ2_A1	31:0	RW	SDO2_BQ2_A1	Filter Coefficient	0
0xEBC	4	SDO2_BQ2_A2	31:0	RW	SDO2_BQ2_A2	Filter Coefficient	0
0xEC0	4	SDO2_BQ3_B0	31:0	RW	SDO2_BQ3_B0	Filter Coefficient	0x3f800000
0xEC4	4	SDO2_BQ3_B1	31:0	RW	SDO2_BQ3_B1	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0xEC8	4	SDO2_BQ3_B2	31:0	RW	SDO2_BQ3_B2	Filter Coefficient	0
0xECC	4	SDO2_BQ3_A1	31:0	RW	SDO2_BQ3_A1	Filter Coefficient	0
0xED0	4	SDO2_BQ3_A2	31:0	RW	SDO2_BQ3_A2	Filter Coefficient	0
0xED4	4	SDO2_BQ4_B0	31:0	RW	SDO2_BQ4_B0	Filter Coefficient	0x3f800000
0xED8	4	SDO2_BQ4_B1	31:0	RW	SDO2_BQ4_B1	Filter Coefficient	0
0xEDC	4	SDO2_BQ4_B2	31:0	RW	SDO2_BQ4_B2	Filter Coefficient	0
0xEE0	4	SDO2_BQ4_A1	31:0	RW	SDO2_BQ4_A1	Filter Coefficient	0
0xEE4	4	SDO2_BQ4_A2	31:0	RW	SDO2_BQ4_A2	Filter Coefficient	0
0xEE8	4	SDO2_BQ5_B0	31:0	RW	SDO2_BQ5_B0	Filter Coefficient	0x3f800000
0xEEC	4	SDO2_BQ5_B1	31:0	RW	SDO2_BQ5_B1	Filter Coefficient	0
0xEF0	4	SDO2_BQ5_B2	31:0	RW	SDO2_BQ5_B2	Filter Coefficient	0
0xEF4	4	SDO2_BQ5_A1	31:0	RW	SDO2_BQ5_A1	Filter Coefficient	0
0xEF8	4	SDO2_BQ5_A2	31:0	RW	SDO2_BQ5_A2	Filter Coefficient	0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
AMP Portion Command							
0x01	1	I2S_CLK_FMT	7:4	R/W	SR_MODE [2:0]	Sampling rate report 0000: 8kHz 0001: 11.025/12kHz 0010: 16kHz 0011: 22.05/24kHz 0100: 32kHz 0101: 44.1/48kHz (default) 0110: 88.2/96kHz 0111: 192kHz Others: Reserved Others: Not supported/SCLK loss/LRCK loss	4'b0101
			3:0	R/W	SCLK_ MODE[2:0]	SCLK mode report 0000: SCLK = 32fs 0001: SCLK = 48fs 0010: SCLK = 64fs (default) 0011: SCLK = 96fs 0100: SCLK = 128fs 0101: SCLK = 192fs 0110: SCLK = 256fs 0111: SCLK = 384fs 1000: SCLK = 512fs Others: Reserved Note: for the 48fs, 96fs, 192fs, 384fs, 512fs, please set 0xF8 bit[6] to 0.	4'b0010
0x02	1	I2S_DATA_FMT	7:6	R/W	SCLK_DEG_ SEL[1:0]	SCLK deglitch time selection 00: No deglitch 01: 1T sync 10: 2T deglitch 11: 3T deglitch (default)	2'b11
			5	R/W	SCLK_EDGE _SEL	0: RX @SCLK rising edge and TX @ SCLK falling edge (default) 1: RX @ SCLK falling edge and TX @ SCLK rising edge	1'b0
			4	R/W	DSP_M_A_S	DSP mode A select, active with AUD_FMT == 2'b11 (DSP mode) 0: DSP mode A (default) 1: DSP mode B	1'b0
			3:2	R/W	AUD_FMT	00: I^2S (default) 01: Left Justify 10 : Right Justify 11 : DSP mode	2'b00
			1:0	R/W	AUD_BITS	00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits (default)	2'b11

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x04	1	SDIO_SEL	7	R	Reserved		1'b0
			6	R/W	Prohibit	Prohibited	1'b1
			5:4	R/W	SDO_SEL [1:0]	00: No output (default) 01: Interface output 10: Final output 11: Peak level detect result	2'b00
			3:2	R/W	CH1_SI[1:0]	00: SDIN-L to CH1 (default) 01: SDIN-R to CH1 1X: 0 to CH1	2'b00
			1:0	R/W	CH2_SI[1:0]	00: SDIN-L to CH2 01: SDIN-R to CH2 (default) 1X: 0 to CH2	2'b01
0x05	1	SYS_CTL	7	R/W	SR_AUTO_DET	Prohibited	1'b1
			6	R/W	SHUTDOWN	0: Turn on 1: Shutdown (default)	1'b1
			5	R	Reserved		1'b0
			4	R/W	D_PBTL	0: BTL (default) 1: PBTL	1'b0
			3:2	R/W	D_SPK_VT_FREQ	PWM frequency 00: 384kHz 01: Reserved 10: 768kHz (default) 11: 1536kHz Prohibited	2'b10
			1	R/W	DIS_A_SEL_PU	Prohibited	1'b0
			0	R/W	dSR_DIV_SEL	Prohibited	1'b0
0x06	1	DIG_BLK_EN	0	R/W	HARD_CLIP_EN	Hard clip enable 0: Disable (default) 1: Enable	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x07	1	SPK_GAIN	7:6	R	Reserved		2'b00
			5	R/W	SPK_GAIN_SW_TO_EN	SPK gain switch @ zero crossing point if the SPK gain change and no zero crossing point after 100ms the gain will switch to the target gain when time out function is enable 0: Disable 1: Enable (default)	1'b1
			4:0	R/W	D_SPK_GAIN[4:0]	Class-D output gain 00000: –6dB 00001: –5dB 00010: –4dB 00011: –3dB 00100: –2dB 00101: –1dB 00110: 0dB 00111: 1dB 01000: 2dB 01001: 3dB 01010: 4dB 01011: 5dB 01100: 6dB 01101: 7dB 01110: 8dB 01111: 9dB 10000: 10dB 10001: 11dB 10010: 12dB 10011: 13dB (default) 10100: 14dB 10101: 15dB 10110: 16dB 10111: 17dB	5'd13

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x08	1	INTER_PWR_CTRL	7	R/W	D_LPFR_EN	Enable DAC RCH LPF 0: Disable 1: Enable (default)	1'b1
			6	R/W	D_LPFL_EN	Enable DAC LCH LPF 0: Disable 1: Enable (default)	1'b1
			5	R/W	D_EN_RCH_PWR	RCH PWR stage enable 0: Disable 1: Enable (default)	1'b1
			4	R/W	D_EN_LCH_PWR	LCH PWR stage enable 0: Disable 1: Enable (default)	1'b1
			3	R/W	D_DAC_RCH_EN	Enable DAC_RCH 0: Disable 1: Enable (default)	1'b1
			2	R/W	D_DAC_LCH_EN	Enable DAC LCH 0: Disable 1: Enable (default)	1'b1
			1	R/W	D_SPK_RCH_EN	Enable Class-D RCH SPK 0: Disable 1: Enable (default)	1'b1
			0	R/W	D_SPK_LCH_EN	Enable Class-D LCH SPK 0: Disable 1: Enable (default)	1'b1
0x09	1	PWM_SS_OPT	7	R/W	D_FSS_EN	Spread spectrum enable 0: Disable (default) 1: Enable	1'b0
			6	R/W	PWM_MODE WHITE	Noise selection 0: Pink noise (default) 1: White noise	1'b0
			5	R/W	PWM_SELCOEF	Pink noise coefficient This will affect the noise amplitude for spread spectrum signal, not recommended to modify it. 0: 1/2 (default) 1: 1/4	1'b0
			4	R/W	PWM_NOISE_EN	Add noise to TRI_GEN 0: Disable (default) 1: Enable	1'b0
			3:2	R/W	D_NOISE_AMP[1:0]	Nosie amplitude for SSC	2'b00
			1:0	R/W	D_FSS_AMP[1:0]	Spread spectrum frequency variation amplitude 00: 20kHz 01: 40kHz (default) 10: 40kHz 11: 60kHz	2'b01

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x0A	1	VOL_RAMP	7:6	R	Reserved		2'b00
			5	R/W	CH2_MUTE	0: Unmute (default) 1: CH2 soft mute	1'b0
			4	R/W	CH1_MUTE	0: Unmute (default) 1: CH1 soft mute	1'b0
			3	R/W	SKIP_RAMP	Skip volume ramp	1'b0
			2	R	Reserved		1'b0
			1:0	R/W	VOL_RAMP_MODE [1:0]	Volume slew step control 00: 1 step in every sample 01: mute -> –40dB, every sample with1 step. –40dB -> 24dB, 2 sample with 1 step.(default) 10: mute -> –40dB, 2 sample with 1 step. –40dB -> 24dB, 4 sample with 1 step. (default) Others: Mute -> –40dB, 4 sample with 1 step. –40dB -> 24dB, 8 sample with 1 step.	2'b01
0x0B	1	TFC_CTRL	7:6	R	Reserved	Prohibited	2'b00
			5	R	D_TFC_UPBOUN_FLAG	Prohibited	1'b0
			4	R	D_TFC_LOWBOUN_FLAG	Prohibited	1'b0
			3:2	R/W	TFC_TH	Thermal fold back active threshold 00: Temp 110°C (default) 01: Temp 120°C 10: Temp 130°C 11: Temp 140°C	2'b00
			1:0	R/W	TFC_RATE	Thermal fold back attack/release rate 00: 0.0625dB/50ms (default) 01: 0.0625dB/100ms 10: 0.0625dB/200ms 11: 0.0625dB/400ms	2'b00
0x0C	1	Reserved	07:00	R/W	Reserved	Prohibited	8'h30

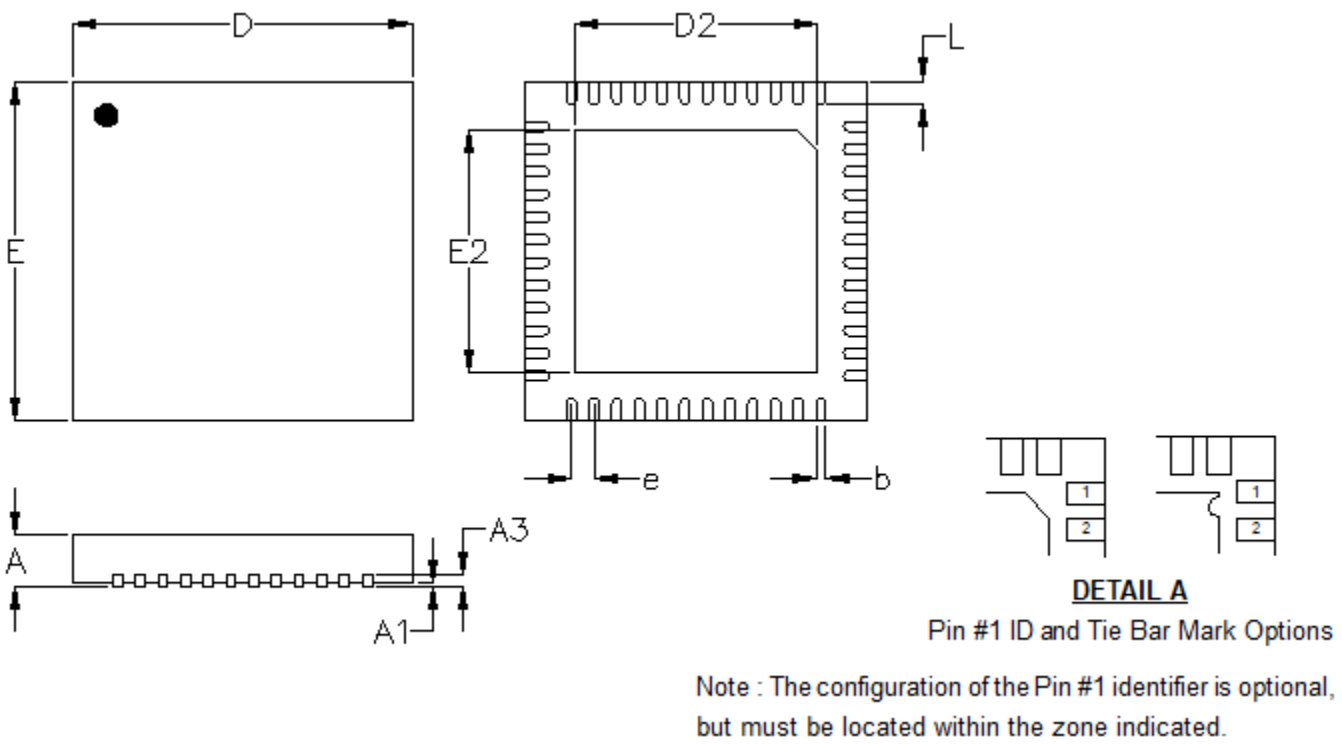
ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x10	1	ERR_RPT	7	R/W	ADS_ERR	Address R detection error 0: No ADS error (default) 1: R detect error, write 0 to clear flag	1'b0
			6	R	DC_ERR	DC flag report 0: No DC error (default) 1: DC error	1'b0
			5	R/W	SCLK_ERR	0: No SCLK error (default) 1: SCLK error, write 0 to clear flag	1'b0
			4	R/W	LRCK_ERR	0: No LRCK clock error (default) 1: LRCK clock error, write0 to clear flag	1'b0
			3	R/W	OC_ERROR	0: No OC error(default) 1: OC, write 0 to clear flag	1'b0
			2	R/W	OV_ERROR	0: No OV error(default) 1 : OV, write 0 to clear flag	1'b0
			1	R/W	OT_ERROR	0: No OT error(default) 1: OT, write 0 to clear flag	1'b0
			0	R/W	UV_ERROR	0: No UV error(default) 1: UV, write 0 to clear flag	1'b0
0x11	1	ERR_MASK	07:06	R	Reserved	Prohibited	2'b00
			5	R/W	SCLK_ ERROR_ MASK	Fault mask for 0x10 SCLK error 0: Not mask 1: Mask (default)	1'b1
			4	R/W	LRCK_ ERROR_ MASK	Fault mask for 0x10 LRCK error 0: Not mask 1: Mask (default)	1'b1
			3	R/W	OC_ERROR _MASK	Fault mask for 0x10 OC error 0: Not mask (default) 1: Mask	1'b0
			2	R/W	OV_ERROR _MASK	Fault mask for 0x10 OV error 0: Not mask (default) 1: Mask	1'b0
			1	R/W	OT_ERROR _MASK	Fault mask for 0x10 OT error 0: Not mask (default) 1: Mask	1'b0
			0	R/W	UV_ERROR _MASK	Fault mask for 0x10 UV error 0: Not mask (default) 1: Mask	1'b0

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x12	1	ERR_TYPE	7:6	R	Reserved		2'b00
			5	R/W	SCLK_ ERROR_ FAULT_ TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	1'b0
			4	R/W	LRCK_ ERROR_ FAULT_ TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	1'b0
			3	R/W	OC_ERROR _FAULT_ TYPE	Fault behavior type select. 0: Auto-recovery 1: Latch (default)	1'b1
			2	R/W	OV_ERROR _FAULT_ TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	1'b0
			1	R/W	OT_ERROR _FAULT_ TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	1'b0
			0	R/W	UV_ERROR _FAULT_ TYPE	Fault behavior type select. 0: Auto-recovery (default) 1: Latch	1'b0
0x13	1	AUTO_RCVRY	07:06	R	Reserved		2'b0
			5	R/W	FAULT_B_ TYPE	0: Recovery type (default) 1: Latch type	1'b1
			4	R/W	PROT_ PWR_PL_EN	Prohibited	1'b1
			03:00	R/W	RCVRY_ TIME[3:0]	Power stage auto-recovery time 0010: 299ms (default) 0011: 449ms 0100: 598ms 0101: 748ms 0110: 898ms 0111: 1047ms 1000: 1197ms 1001: 1346ms 101X: 1496ms 11XX: 1496ms	4'b0010
0x14	1	DC_PROT	7:4	R	Reserved	Prohibited	4'b0000
			3:2	R/W	DC_TH[1:0]	DC threshold for DC detection 00: No available 01: 12.5% 10: 18.75% (default) 11: 25%	2'b10
			1	R/W	DC_TIME_ SEL	Detection time 0: 342ms (default) 1: 684ms	1'b0
			0	R/W	DC_EN	DC protection enable 0: Disable 1: Enable (default)	1'b1

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x20	2	MS_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	MS_VOL [10:0]	Master volume control 11'h000: 24dB 11'h180: 0dB 11'h7FF: mute (default) 0.0625dB per step	11'h7FF
0x21	2	CH1_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	CH1_VOL [10:0]	CH1 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x22	2	CH2_VOL	15:11	R	Reserved	Prohibited	5'b00000
			10:0	R/W	CH2_VOL [10:0]	CH2 volume control 11'h000: 24dB 11'h180: 0dB (default) 11'h7FF: mute 0.0625dB per step	11'h180
0x30	3	CH1_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_ MIX_0	CH1_IN_MIX_0	17’h08000
0x31	3	CH1_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH1_IN_ MIX_1	CH1_IN_MIX_1	17’h00000
0x32	3	CH2_IN_MIX_0	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_ MIX_0	CH2_IN_MIX_0	17’h00000
0x33	3	CH2_IN_MIX_1	23:17	R	Reserved	Prohibited	7'h00
			16:0	R/W	CH2_IN_ MIX_1	CH2_IN_MIX_1	17’h08000
0x40	1	SW_RESET	7	W	SF_RESET	Write 1 to trigger Software reset Need to wait 20ms for reset completion	1'b0
			6:0	R	Reserved	Prohibited	7'h00

ADDR	Byte	RegName	BITS	R/W	Name	Description	Default
0x6C	1	UVP_OPT	7	R	D_VCORE_OK	Prohibited	1'b1
			6	R/W	D_EN_DVDD_UV	Prohibited	1'b1
			5:4	R/W	D_UVP_DVDD_VTH[1:0]	Prohibited	2'b10
			3	R/W	D_UV_RAMP_DOWN	SPK UV protection behavior 0: HZ_PROT directly (default) 1: Power-off sequence	1'b0
			2:0	R/W	D_UVP_PVDD_SEL[2:0]	Select UVP level for PVDD power domain 000: 4V (default) 001: 6.1V 010: 8.7V 011: 11V 100: 12.8V 101: 15.2V 110: 20.3V 111: 21.2V	3'b000

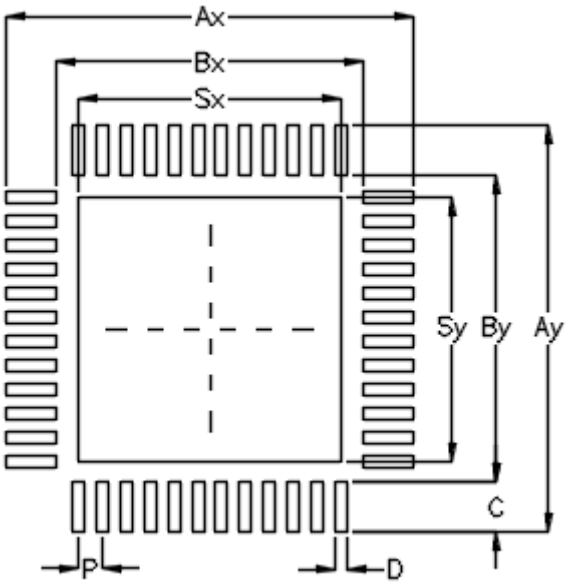
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.800	1.000	0.031	0.039
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		5.950	6.050	0.234	0.238
D2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
	Option 3	4.650	4.750	0.183	0.187
E		5.950	6.050	0.234	0.238
E2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
	Option 3	4.650	4.750	0.183	0.187
e		0.400		0.016	
L		0.350	0.450	0.014	0.018

V-Type 48L QFN 6x6 Package

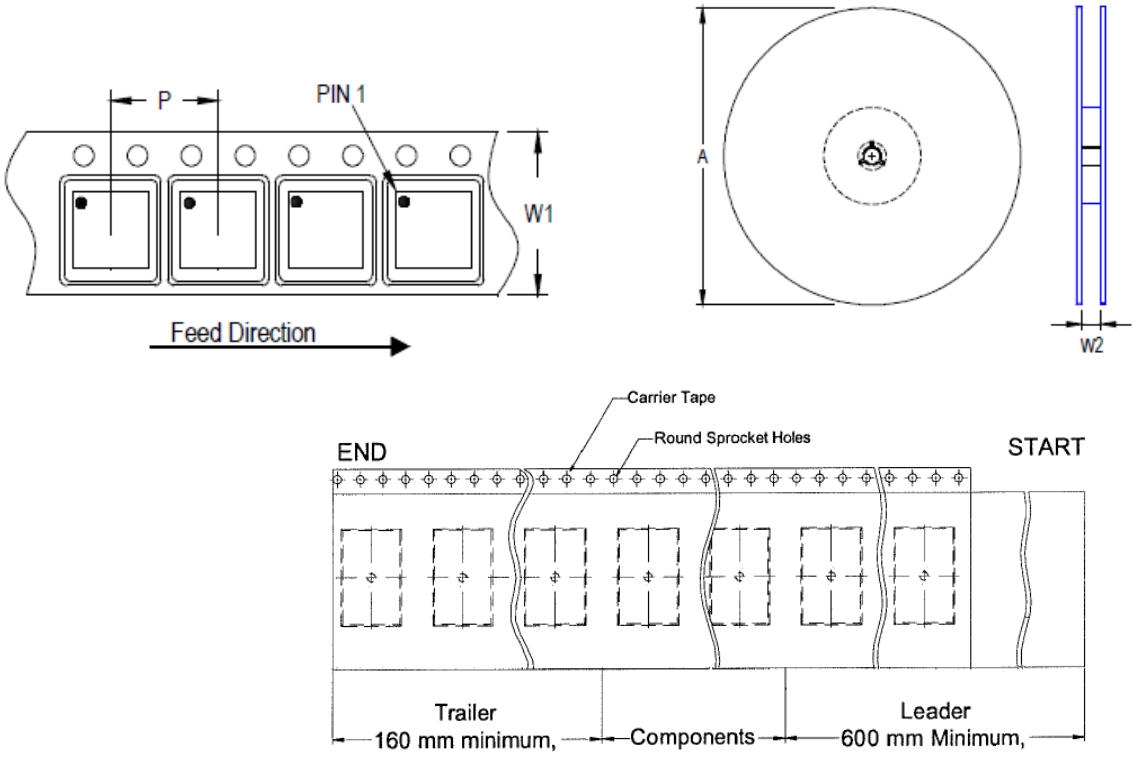
Footprint Information



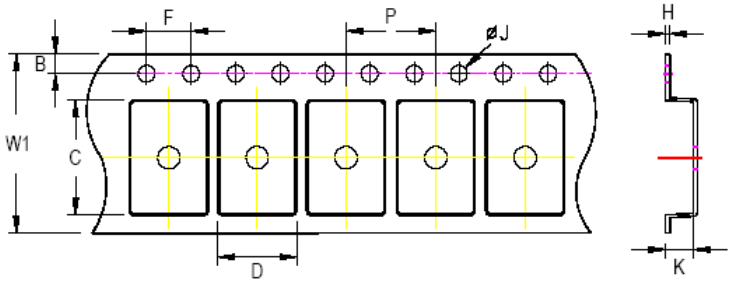
Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN6x6-48	Option1	48	0.40	6.80	6.80	5.10	5.10	0.85	0.20	4.40	4.40	±0.05
	Option2									4.50	4.50	
	Option3									4.70	4.70	
	Option4									4.60	4.60	

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 6x6	16	12	330	13	3,500	160	600	16.4/18.4



C, D and K are determined by component size.

The clearance between the components and

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton		
	Size	Units	Item	Weight(kg)	Reels	Units	Item	Boxes	Units
QFN and DFN 6x6	13”	3,500	Box G	1.11	1	3,500	Carton A	6	21,000

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/4/26	Final	Electrical Characteristics on P9 Typical Application Circuit on P12, 13, 14, 15 Initial Sequence (BTL Mode) on P18, 19 Initial Sequence (PBTL Mode) on P20, 21, 22 Detailed Signal Path on P31 EQ Block Diagram and Description on P43 Application Information on P70, 71, 79 to 126