1A, 5.5V, Ultra Low Dropout Linear Regulator

1 General Description

The RT9085 is a high-performance positive voltage regulator with a separated bias voltage (V_{BIAS}), designed for applications requiring low input voltage and ultra-low dropout voltage, with output current up to 1A. The ultra-low dropout voltage feature is ideal for applications where the output voltage is very close to the input voltage. The input voltage can be as low as 0.8V, and the output voltage is adjustable via an external resistive divider. The RT9085 features very low quiescent current consumption for portable applications. The device is available in the WL- CSP-6B 0.8x1.2 (BSC) and ZWL-CSP-6B 0.8x1.2 (BSC) packages. The recommended junction temperature range is –40°C to 125°C.

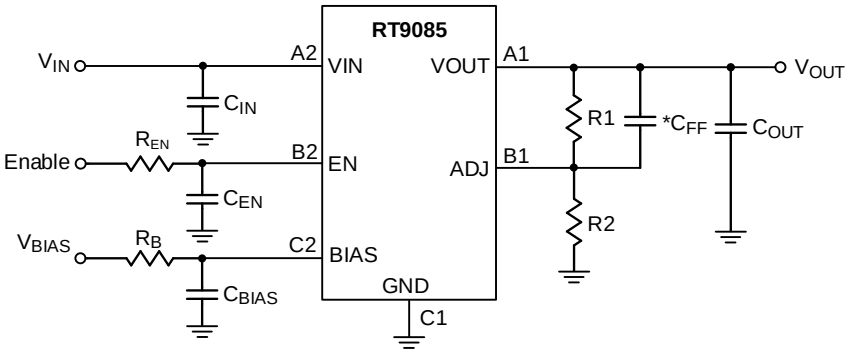
2 Applications

- Battery-Powered Systems
- Portable Electronic Devices
- Digital Set-Top Boxes

3 Features

- **Input Voltage Range: 0.8V to 5.5V**
- **Bias Voltage Range: 3V to 5.5V**
- **Available in Fixed and Adjustable (0.5V to 3V)**
- **Ultra Low Dropout Voltage: 60mV at 1A**
- **Accurate Output Voltage Accuracy Over Line/Load/Temperature**
  - **1% @ –40ºC to 85ºC**
  - **2% @ –40ºC to 125ºC**
- **Low Bias Input Current**
  - **Typ. 35μA in Operating Mode**
  - **Typ. 0.5μA in Shutdown Mode**
- **Output Active Discharge Function**
- **Enable Control**
- **Stable with a 10μF Output Ceramic Capacitor**

4 Simplified Application Circuit



5 Ordering Information

Product No.	Nominal Output Voltage	Package (Note 1)
RT9085A-07WSC	0.70V	WL-CSP-6B 0.8x1.2 (BSC)
RT9085A-0GWSC	0.75V	
RT9085A-08WSC	0.80V	
RT9085A-0HWSC	0.85V	
RT9085A-09WSC	0.90V	
RT9085A-0JWSC	0.95V	
RT9085A-10WSC	1.00V	
RT9085A-1KWSC	1.05V	
RT9085A-11WSC	1.10V	
RT9085A-1AWSC	1.15V	
RT9085A-12WSC	1.20V	
RT9085A-1BWSC	1.25V	
RT9085A-13WSC	1.30V	
RT9085A-15WSC	1.50V	
RT9085A-18WSC	1.80V	
RT9085AWSC	Adjustable	
RT9085EWTC	Adjustable	ZWL-CSP-6B 0.8x1.2 (BSC)

Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

6 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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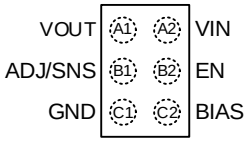
7 Pin Configuration

(TOP VIEW)



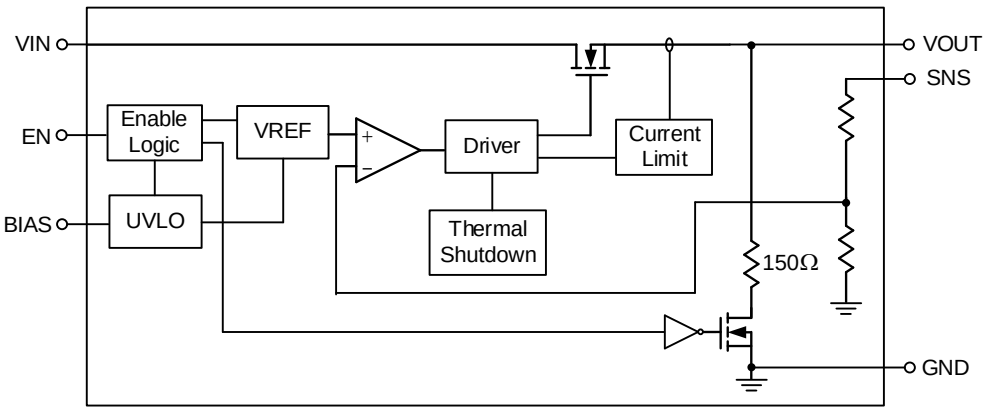
ZWL-CSP-6B 0.8x1.2 (BSC) /
WL-CSP-6B 0.8x1.2 (BSC)

8 Functional Pin Description

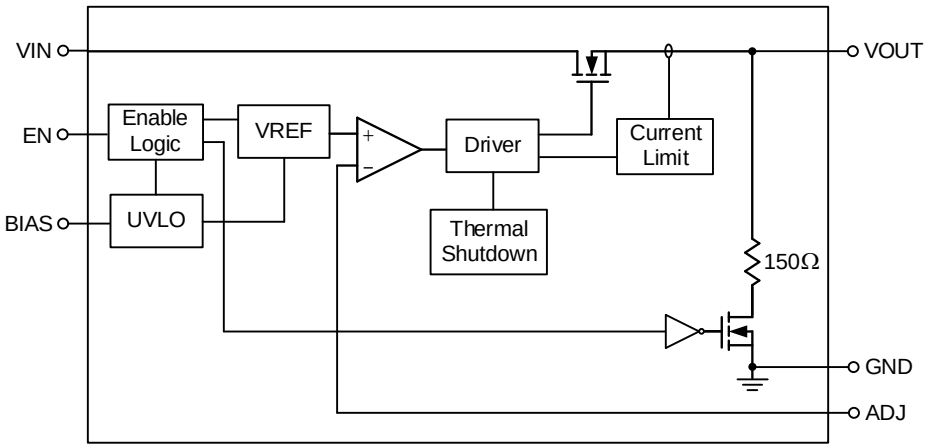
Pin No.	Pin Name	Pin Function
A1	VOUT	Regulator output pin. A 10μF capacitor should be placed directly at this pin.
A2	VIN	Regulator input pin. A 4.7μF capacitor should be placed directly at this pin.
B1	ADJ/SNS	• Adjustable output voltage feedback input pin. • Output voltage sensing input, connect to the output terminal on the PCB.
B2	EN	Chip enable pin. Pulling this pin below 0.54V turns the regulator off, reducing the quiescent current to a fraction of its operating value. This pin must not be left unconnected; connect to an RC filter after BIAS if not being used. If EN is an external signal, it is recommended to connect an RC filter for proper operation. Keep V_{EN} < V_{BIAS} + 0.5V to prevent malfunction.
C1	GND	Ground pin. This pin must be connected to ground.
C2	BIAS	Supply V_{BIAS} ripple should be less than 30mV (5mV/μs) to secure safe stabilization of the internal control circuitry. Apply an RC filter consisting of (500 to 1k) Ω + 1μF at the pin input. The V_{BIAS} must be higher than 3V and ensure $V_{BIAS} \geq V_{OUT}$ + 1.6V for normal operation.

9 Functional Block Diagram

9.1 VOUT Fixed Version



9.2 VOUT Adjustable Version



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 6V
- Enable Input Voltage, EN ---------- –0.3V to 6V
- All Other Pins ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 0.8V to 5.5V
- Supply Input Voltage, BIAS ---------- 0.8V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see the Electrical Characteristics table.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WL-CSP-6B 0.8x1.2 (BSC)	ZWL-CSP-6B 0.8x1.2 (BSC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	73.3	60.4	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	43.3	42.4	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	8.1	3.7	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	98.7	97.5	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	0.8	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.4	49.8	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity two-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

($V_{BIAS} \geq 3V$, and $V_{BIAS} \geq V_{OUT} + 1.6V$, $V_{IN} = V_{OUT} + 0.3V$, $I_{OUT} = 1mA$, $V_{EN} = 1V$, $C_{IN} = 4.7\mu F$, $C_{OUT} = 10\mu F$, $C_{BIAS} = 1\mu F$, $T_A = 25°C$, unless otherwise specified.) (Note 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Input Voltage	V_{IN}		0.8	--	5.5	V
Bias Voltage Range	V_{BIAS}		3	--	5.5	V
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{BIAS} rising	--	1.6	--	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}	Hysteresis	--	0.2	--	V
Reference Voltage (V_{OUT} Adjustable Version)	V_{REF}		--	0.5	--	V
Output Voltage Accuracy (Note 7)	V_{OUT_ACC}	V_{OUT} = 0.5V, no load	–0.5	--	0.5	%
		1. $V_{OUT(NOM)} + 0.3V \leq V_{IN} \leq V_{OUT(NOM)} + 1V$ 2. $V_{BIAS} \geq 3V$ and $V_{OUT(NOM)} + 1.6V \leq V_{BIAS} \leq 5.5V$ 3. $1mA \leq I_{OUT} \leq 1A$ 4. $–40°C \leq T_J \leq 85°C$	–1	--	1	%
		1. $V_{OUT(NOM)} + 0.3V \leq V_{IN} \leq V_{OUT(NOM)} + 1V$ 2. $V_{BIAS} \geq 3V$ and $V_{OUT(NOM)} + 1.6V \leq V_{BIAS} \leq 5.5V$ 3. $1mA \leq I_{OUT} \leq 1A$ 4. $–40°C \leq T_J \leq 125°C$	–2	--	2	%
V_{IN} Line Regulation	$V_{VIN\_LINE\_REG}$	$V_{OUT(NOM)} + 0.3V \leq V_{IN} \leq 5V$	--	0.01	--	%/V
V_{BIAS} Line Regulation	$V_{VBIAS\_LINE\_REG}$	$V_{BIAS} \geq 3V$ and $V_{OUT(NOM)} + 1.6V \leq V_{BIAS} \leq 5.5V$	--	0.01	--	%/V
Load Regulation	V_{LOAD_REG}	I_{OUT} = 1mA to 1A	--	2	--	mV
V_{IN} Dropout Voltage	V_{VIN_DROP}	I_{OUT} = 1A (Note 11)	--	60	75	mV
V_{BIAS} Dropout Voltage	V_{BIAS_DROP}	I_{OUT} = 1A, $V_{IN} = V_{BIAS}$ (Note 9 and Note 10)	--	1.05	1.5V	V
Output Current Limit	I_{LIM}	V_{OUT} = 90% of $V_{OUT(NOM)}$, $–40°C \leq T_J \leq 85°C$	1.4	--	2.7	A
		V_{OUT} = 90% of $V_{OUT(NOM)}$, $–40°C \leq T_J \leq 125°C$	1.3	--	2.7	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADJ Pin Operating Current (V_{OUT} Adjustable Version)	I_{ADJ}		--	0.1	0.5	μA
Bias Pin Quiescent Current	I_{BIAS_Q}	V_{BIAS} = 3V	--	35	50	μA
Bias Pin Shutdown Current	I_{BIAS_SHDN}	$V_{EN} \leq 0.4V$	--	0.5	1	μA
V_{IN} Pin Shutdown Current	I_{VIN_SHDN}	$V_{EN} \leq 0.4V$	--	0.5	1	μA
EN Input Voltage Rising Threshold	V_{EN_R}		0.69	0.81	0.93	V
EN Input Voltage Falling Threshold	V_{EN_F}		0.54	0.68	0.87	
EN Pull Down Current	I_{EN}	V_{EN} = 5.5V, V_{BIAS} = 5.5V	--	0.3	--	μA
Turn-On Time	t_{ON}	From assertion of V_{EN} to V_{OUT} = 90% of $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1V	--	150	--	μs
Power Supply Rejection Ratio (Note 12)	PSRR_V_{IN}	V_{IN} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, VIN ≥ V_{OUT} + 0.5V	--	70	--	dB
	PSRR_V_{BIAS}	V_{BIAS} to V_{OUT}, f = 1kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ + 0.5V	--	70	--	dB
Output Noise Voltage (Fixed Volt.) (Note 12)	V_{n_FIXED}	V_{IN} = V_{OUT} +0.5 V, $V_{OUT(NOM)}$ = 1V, f = 10Hz to 100kHz	--	30	--	μV_{RMS}
Output Noise Voltage (Adj devices) (Note 12)	V_{n_ADJ}	V_{IN} = V_{OUT} + 0.5V, f = 10Hz to 100kHz	--	15 x V_{OUT}/ V_{REF}	--	μV_{RMS}
Over-Temperature Protection Threshold	T_{OTP}	Shutdown temperature	--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
Discharge Resistor	R_{DISCHG}	$V_{EN} \leq 0.4V$, V_{OUT} = 0.5V	--	150	--	Ω

Note 7. Adjustable devices tested at 0.5V; external resistor tolerance is not taken into account.

Note 8. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

Note 9. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.

Note 10. For output voltages below 0.9V, VBIAS dropout voltage does not apply due to a minimum Bias operating voltage of 3V.

Note 11. For adjustable devices, VIN dropout voltage tested at $V_{OUT(NOM)}$ = 2 x V_{REF}.

Note 12. Guaranteed by design.

15 Typical Application Circuit

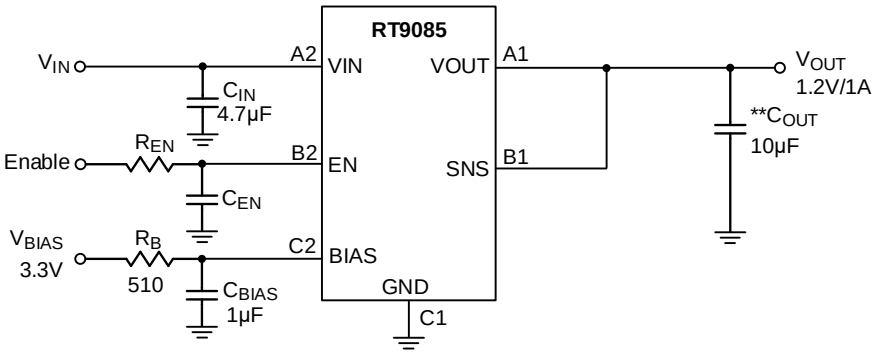


Figure 1. Fixed Voltage Regulator

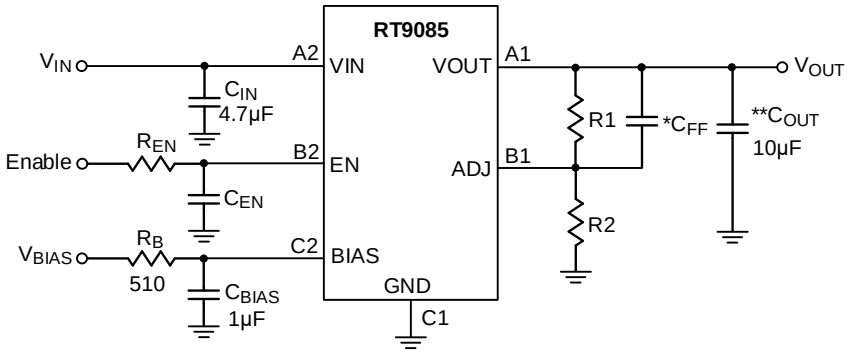


Figure 2. Adjustable Voltage Regulator

Table 1. Recommended External Components

Component	Description	Vendor P/N
C_{BIAS}	1µF, 16V, X5R, 0402	CGB2A1X5R1C105M033BC(TDK) GRM155R61C105MA12D(Murata)
C_{IN}	4.7µF, 10V, X5R, 0603	C1608X5R1A475K080AE(TDK) GRM155R61A475MEAA(Murata)
**C_{OUT}	10µF, 6.3V, X5R, 0603	GRM185R60J106ME15(Murata) 0603X106M6R3(WASLIN)

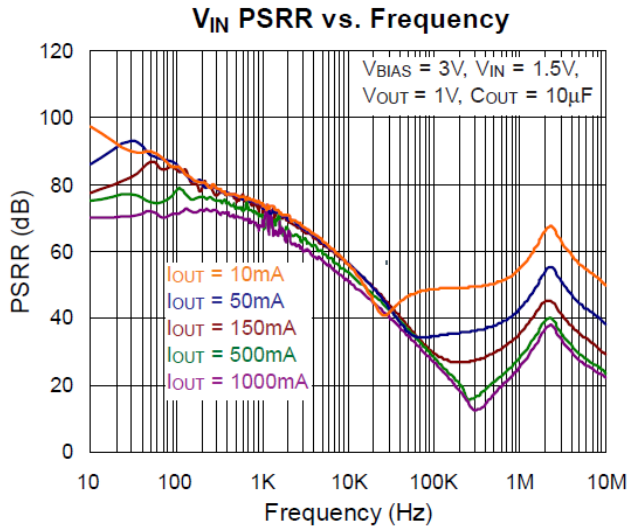
**: Considering the effective capacitance derated with biased voltage levels, the C_{OUT} component needs satisfy the effective capacitance at least 4.7µF or above at the targeted output level to ensure stable and normal operation.

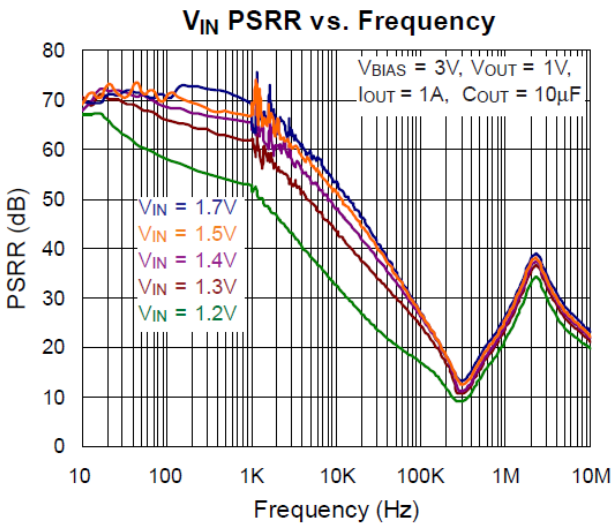
Table 2. Suggested Component Values

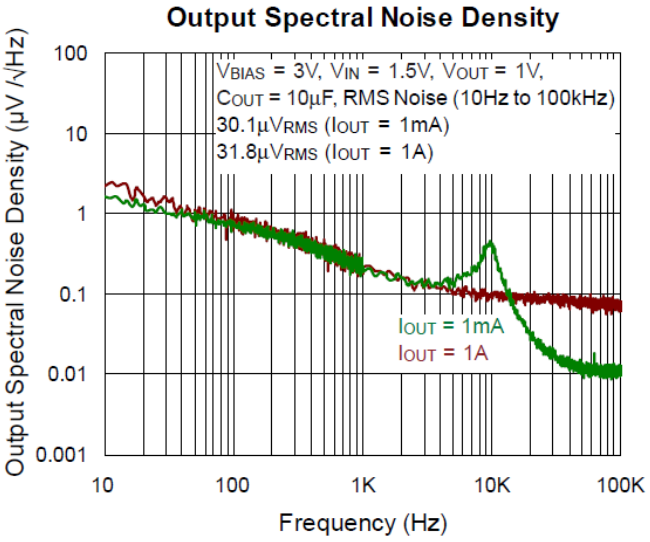
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	*C_{FF} (pF)
0.75	20	40	120
1	20	20	120
1.8	20	7.69	120
2.5	20	5	--

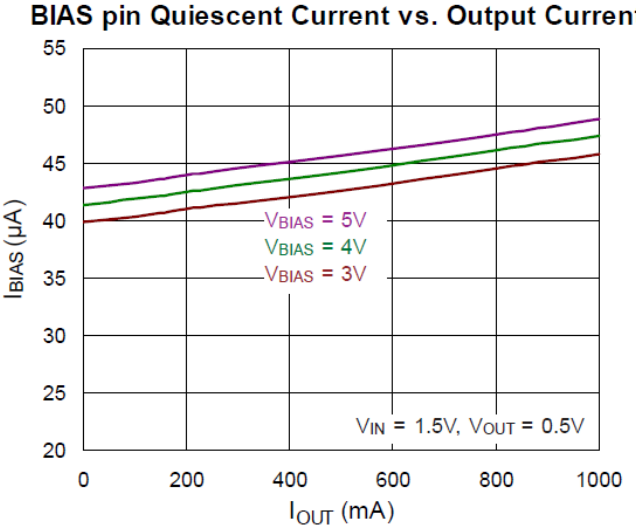
*: The feedforward capacitor C_{FF} is optional for the optimization of transient response by increasing bandwidth and acceptable phase margin.

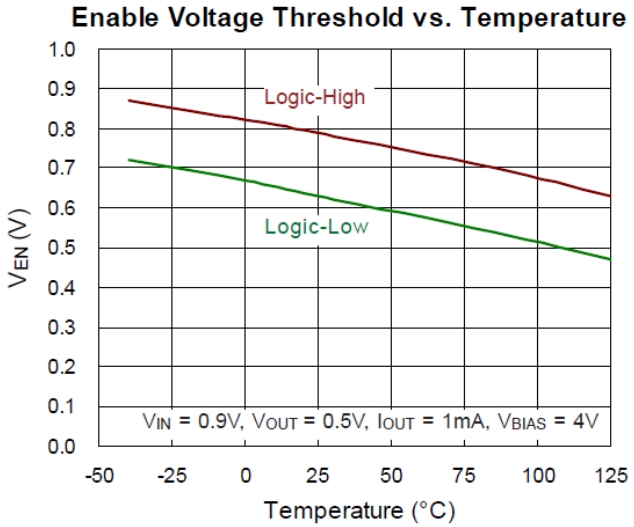
16 Typical Operating Characteristics

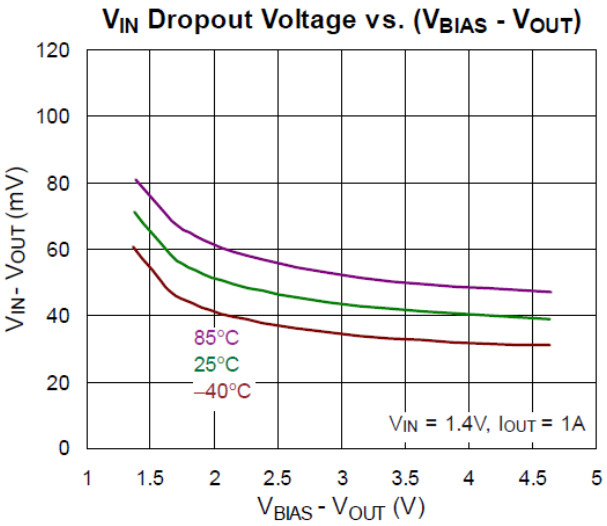




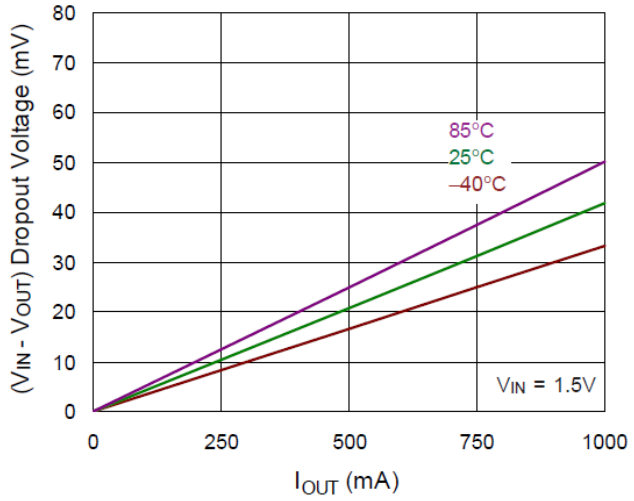




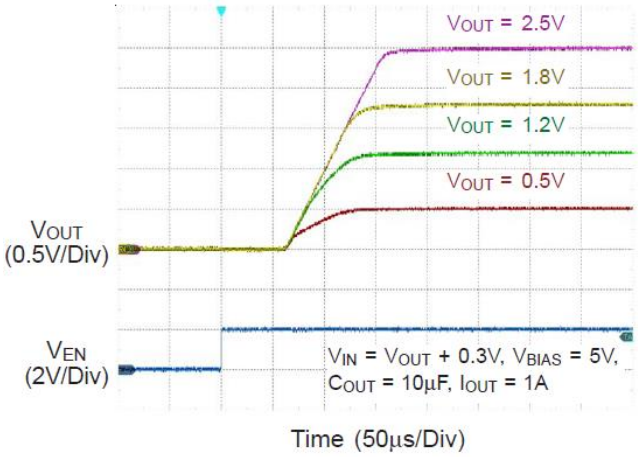




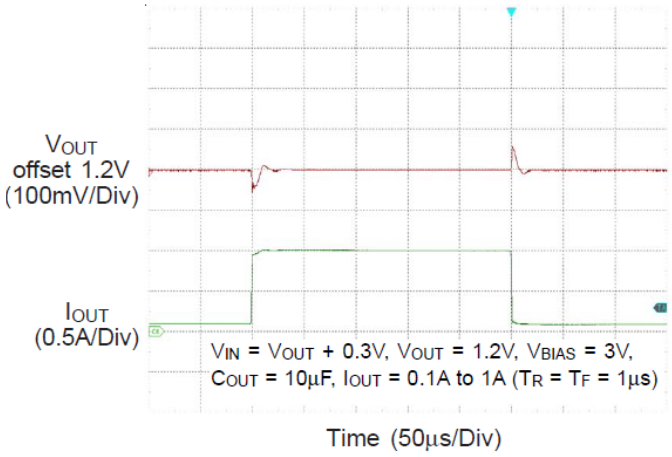
Dropout Voltage vs. Output Current



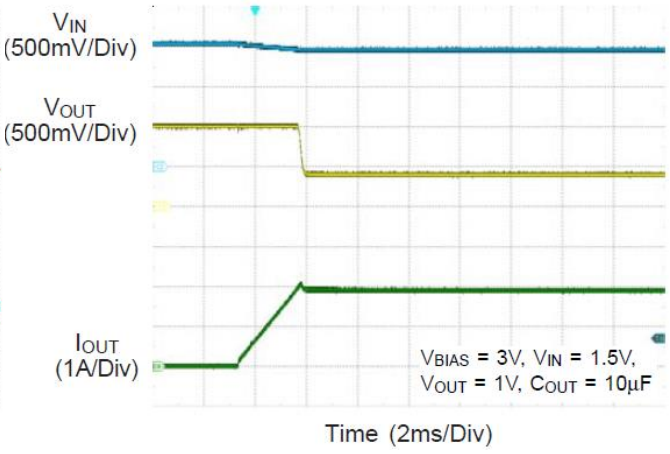
VOUT Start Up with EN



Load Transient Response



Output Current Limit Protection



17 Operation

The RT9085 uses an N-MOSFET pass transistor for output voltage regulation from the VIN voltage. The separated bias voltage (V_{BIAS}) powers the low-current internal control circuit for applications requiring low input voltage and ultra-low dropout voltage.

In steady-state operation, the feedback voltage is regulated to the reference voltage by the internal regulator. When the feedback voltage signal is less than the reference voltage, the output current passing through the power MOSFET increases. The additional current is sent to the output until the voltage level at the ADJ pin returns to the reference voltage. On the other hand, if the feedback voltage is higher than the reference voltage, the power MOSFET current decreases. The excess charge at the output can be released by the loading current.

17.1 Chip Enable and Shutdown

The RT9085 provides an EN pin, as an external chip enable control, to enable or disable the device. When the voltage at VEN is below 0.54V, the regulator is turned off and enters the shutdown mode. When V_{EN} is above 0.93V, the regulator is turned on. When the regulator is shutdown, the ground current is reduced to a maximum of 1μA.

17.2 Output Active Discharge

When the RT9085 is operating in shutdown mode, the device utilizes an internal active pull-down circuit that connects the output to GND through a 150Ω resistor for output discharging purpose.

17.3 Current Limit

The RT9085 continuously monitors the output current to protect the pass transistor from abnormal operations. When an overload or short circuit is encountered, the current limit circuitry controls the pass transistor's gate voltage to keep the output within the predefined range.

17.4 Over-Temperature Protection (OTP)

The RT9085 includes over-temperature protection (OTP) circuitry to prevent overheating. When the junction temperature exceeds the OTP threshold (T_{OTP}), the device is disabled. It will automatically resume normal operation once the junction temperature decreases by the amount of OTP hysteresis (T_{OTP_HYS}). Additionally, continuous operation at or into thermal shutdown, or maintaining a junction temperature above 160°C, may diminish the reliability of the RT9085.

Note that the over-temperature protection is designed to protect the device during temporary overload conditions. It serves as a secondary fail-safe mechanism and is activated when operating conditions exceed the absolute maximum range. It should not be used as a substitute for proper thermal design in normal operation. Continuously operating the device above the specified absolute maximum junction temperature can compromise device reliability or result in permanent damage.

18 Application Information

(Note 13)

The RT9085 is a low voltage, low dropout linear regulator with input voltage V_{IN} from 0.8V to 5.5V, V_{BIAS} range from 3V to 5.5V, and adjustable output voltage from 0.5V to (V_{IN} – V_{VIN_DROP}). Keep V_{EN} < V_{BIAS} + 0.5V to prevent malfunction.

18.1 Output Voltage Setting

For the RT9085, the voltage on the ADJ pin sets the output voltage and is determined by the values of R1 and R2. The values of R1 and R2 can be calculated for any voltage using the following formula:

$$V_{OUT}=0.5V\times\left(\frac{R_1+R_2}{R_2}\right)$$

Using lower values for R1 and R2 is recommended to reduce the noise injected from the ADJ pin. Note that R1 is connected from the VOUT pin to the ADJ pin, and R2 is connected from ADJ to GND.

18.2 BIAS Pin Input

The V_{BIAS} supply rail that powers the LDO control circuit, sinks a very low current (approximately the quiescent current of the LDO). The V_{BIAS} must be higher than 3V and ensure $V_{BIAS} \geq V_{OUT}$ + 1.6V for normal operation.

18.3 Dropout Voltage

The VIN dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at a specific output current. The VIN dropout voltage V_{VIN_DROP} can also be expressed as the voltage drop on the pass-FET at a specific output current (I_{RATED}) while the pass-FET is fully operating in the Ωic region. The pass-FET can be characterized as a resistance $R_{DS(ON)}$. Thus, the dropout voltage can be defined as V_{VIN_DROP} = V_{IN} - V_{OUT} = $R_{DS(ON)}$ x I_{RATED}. For normal operation, the suggested LDO operating range is V_{IN} > V_{OUT} + V_{VIN_DROP} for good transient response and PSRR ability. Conversely, operating in the Ωic region will severely degrade performance.

18.4 C_{IN} and C_{OUT} Selection

The RT9085 is designed specifically to work with low ESR ceramic output capacitor for space saving and performance consideration. Using a ceramic capacitor with effective capacitance range from 4.7μF to 22μF on the RT9085 output ensures stability. The input capacitor must be located at a distance of no more than 0.5 inch from the input pin of the chip. However, a capacitor with larger value and lower ESR (Equivalent Series Resistance) is recommended since it will provide better PSRR and line transient response. Any good quality ceramic capacitor can be used, C_{IN} = 4.7μF or greater is recommended. V_{BIAS} pin is suggested connecting with a 510Ω resistor and C_{BIAS} = 1μF as a low-pass filter for good noise immunity.

18.5 Feedback Network with Feed-forward Capacitor

The feed-forward capacitor (C_{FF}) introduces one zero and one pole within the feedback loop, which is optional for the optimization of transient response by increasing bandwidth and acceptable phase margin. The RT9085 is designed to be stable without the external feed-forward capacitor. However, an external feed-forward capacitor can also be used. Adding a 120pF external feed-forward capacitor optimizes the transient, noise, and PSRR performances.

18.6 Sequencing Requirements

The RT9085 supports powering on the input V_{IN}, V_{BIAS}, and EN pins in any order without damaging the device. However, for the output soft-start procedure to work as intended, it is mandatory to ensure $V_{IN} \geq V_{OUT}$ + 0.1V before $V_{BIAS} \geq V_{OUT}$ + 1.6V, and the device is enabled by V_{EN} (V_{EN} > V_{EN_R}) eventually. The BIAS pin supplies

voltage for the LDO control circuit, and powering up V_{BIAS} first will ensure that the turn-on time (t_{ON}) and output voltage accuracy to follow datasheet specifications.

Figure 3 also shows the use of an RC-delay circuit that holds off V_{EN} until V_{BIAS} has ramped up to the target value. This technique can also be used to drive V_{EN} from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

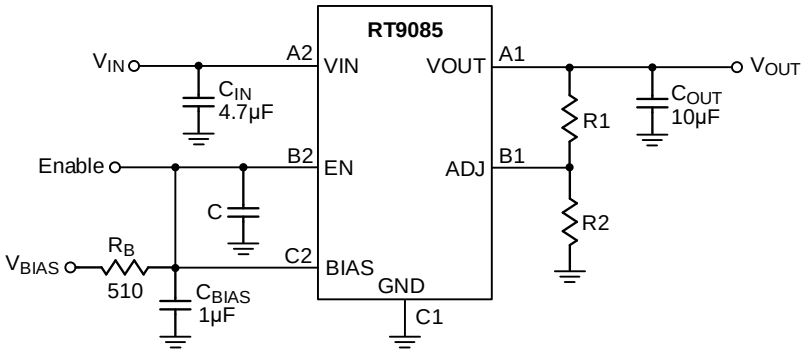


Figure 3. Soft-Start Delay Using an RC Circuit to Enable the Device

18.7 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WL-CSP-6B 0.8x1.2 (BSC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 98.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a ZWL-CSP-6B 0.8x1.2 (BSC) package, the thermal resistance, $\theta_{JA(EVB)}$, is 97.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board.

For a ZWL-CSP-6B 0.8x1.2 (BSC) package, the thermal resistance, $\theta_{JA(EVB)}$, is TBD °C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (98.7°C/W) = 1.01W for a WL-CSP-6B 0.8x1.2 (BSC) package.

$P_{D(MAX)}$ = (125°C – 25°C) / (97.5°C/W) = 1.03W for a ZWL-CSP-6B 0.8x1.2 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curve in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

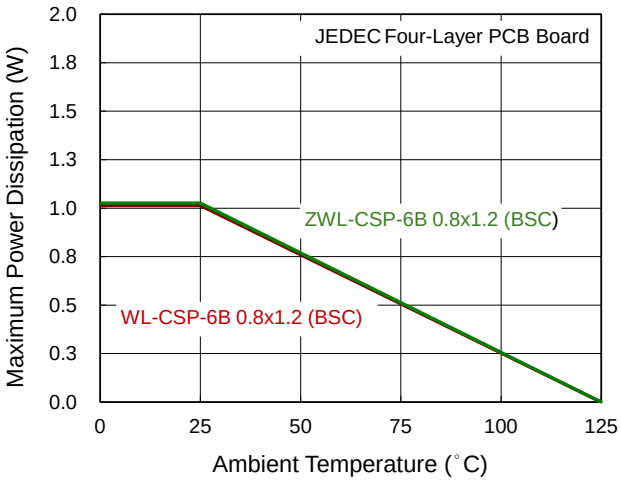


Figure 4. Derating Curve of Maximum Power Dissipation

18.8 Layout Considerations

For the best performance of the RT9085, the following PCB layout suggestions are highly recommended:

- Place all circuit components on the same side and as close to the respective LDO pin as possible. Connect the ground return path to the input and output capacitors.
- Connect the ground plane with a wide copper surface for good thermal dissipation.
- Avoid using vias and long power traces for the connection of input and output capacitors, as they can negatively affect performance.

Figure 5 shows an example of the layout reference that reduces conduction trace loops, minimizes inductive parasitics, reduces load transients, and ensures good circuit stability.

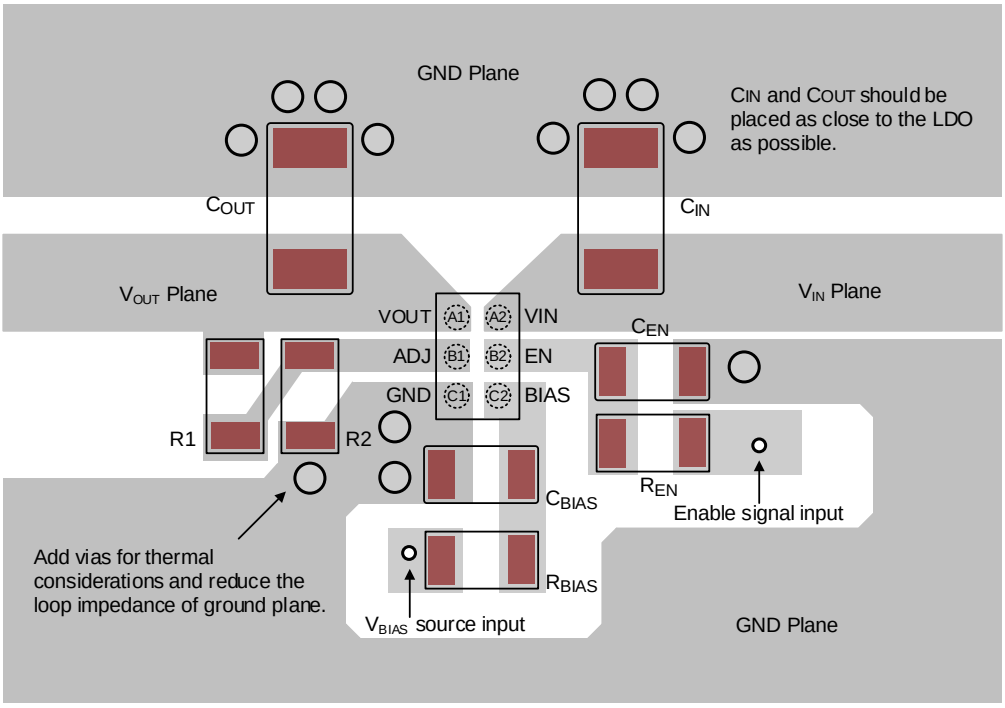
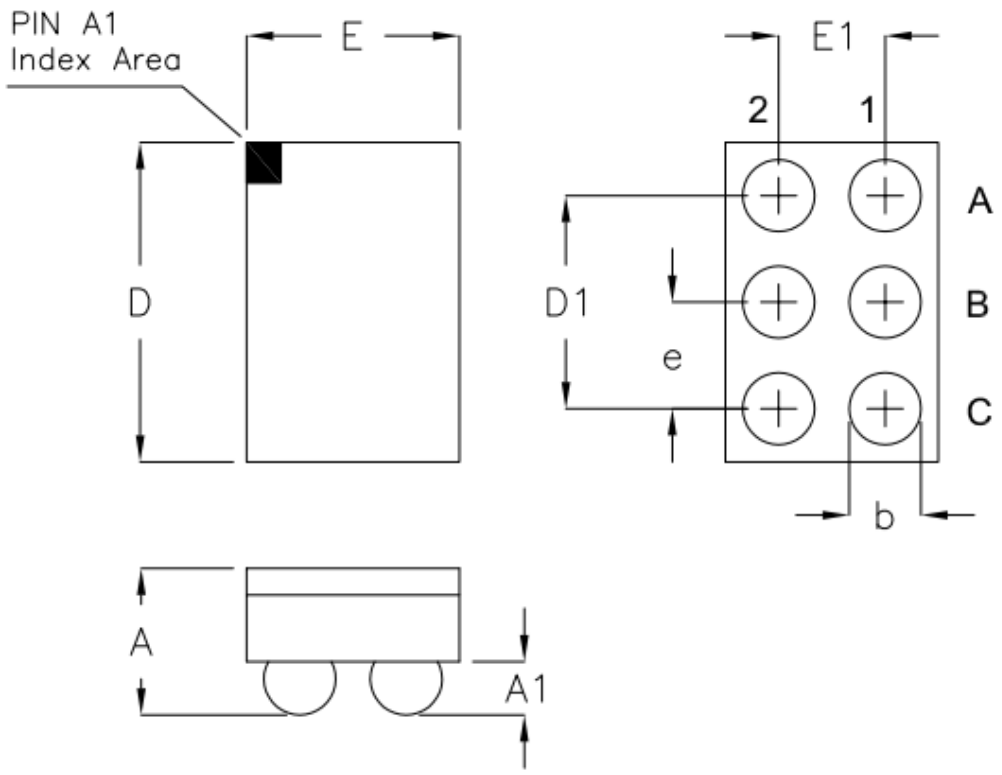


Figure 5. PCB Layout Guide

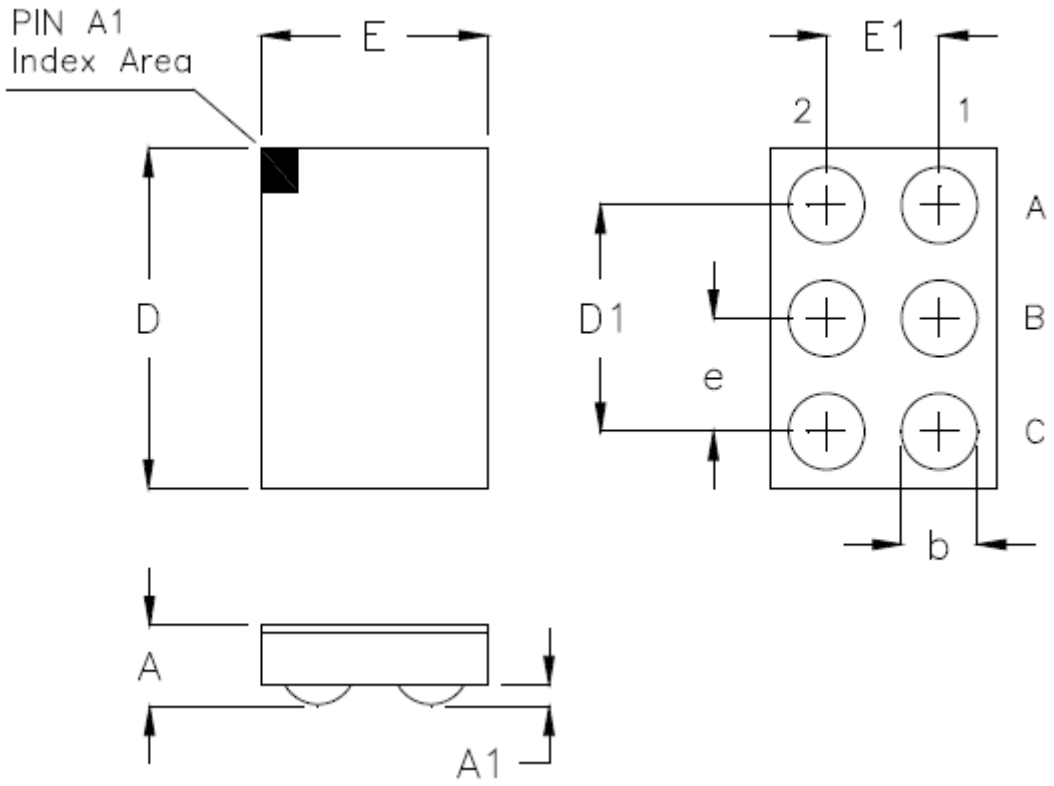
Note 13. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.160	1.240	0.046	0.049
D1	0.800		0.031	
E	0.760	0.840	0.030	0.033
E1	0.400		0.016	
e	0.400		0.016	

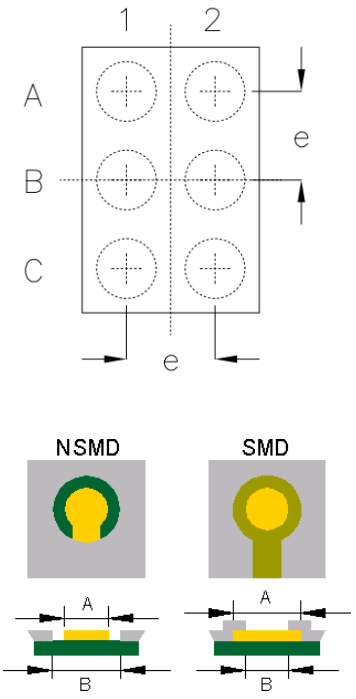
6B WL-CSP 0.8x1.2 Package (BSC)



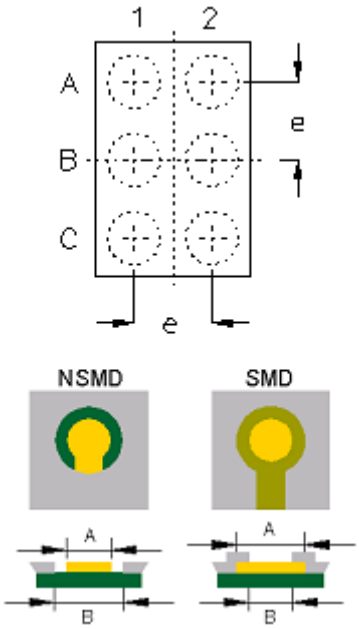
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.250	0.330	0.010	0.013
A1	0.060	0.080	0.002	0.003
b	0.220	0.280	0.009	0.011
D	1.150	1.250	0.045	0.049
D1	0.800		0.031	
E	0.750	0.850	0.030	0.033
E1	0.400		0.016	
e	0.400		0.016	

6B ZWL-CSP 0.8x1.2 Package (BSC)

20 Footprint Information



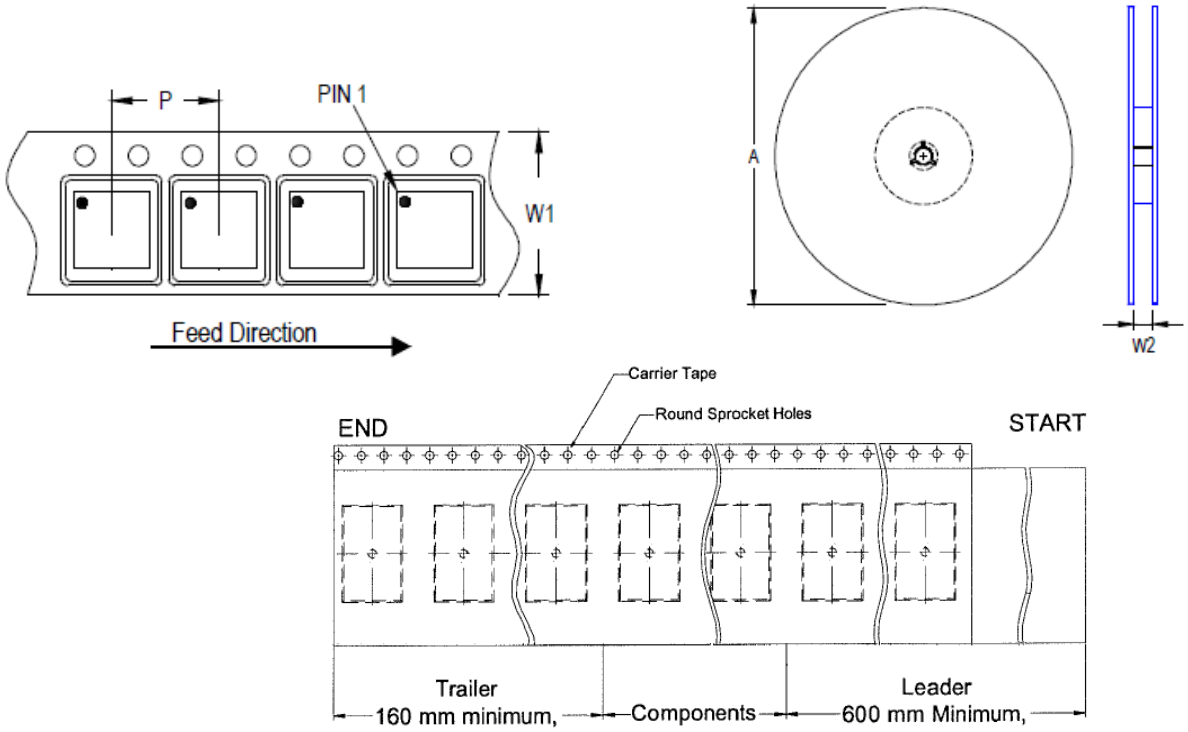
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP0.8*1.2-6(BSC)	6	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	



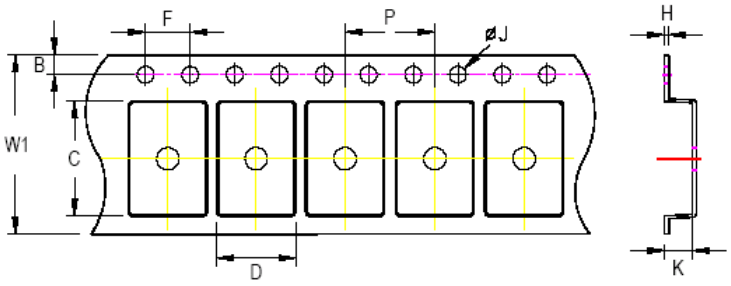
Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
ZWL-CSP0.8X1.2-6(BSC)	6	NSMD	0.400	0.250	0.350	±0.025
		SMD		0.220	0.250	

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
WL-CSP 0.8x1.2	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 12 inner boxes per outer box
2	 Packing by Anti-Static Bag	5	 Outer box **Carton A**
3	 3 reels per inner box **Box A**	6	

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
WL-CSP 0.8x1.2	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
06T00	2024/9/20	Modify	*Merge RT9085A/E* *Ordering Information on page 2*