Source/Sink DDR Termination Regulator

General Description

The RT9066 is a source/sink tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT9066 possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 30µF of ceramic output capacitance. The RT9066 supports remote sensing functions and all features required to power the DDRII / DDRIII and Low Power DDRIII / DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT9066 provides an open drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications .

The RT9066 is available in the thermal efficient package WDFN-16L 5x3.

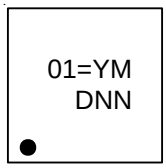
Features

- **VIN Input Voltage Range : 1.1V to 2V**
- **VCNTL Input Voltage Range : 2.375V to 5.5V**
- **Output Current Up to 4.5A**
- **MLCC Stable**
- **PGOOD to Monitor Output Regulation**
- **±10mA Reference (REFOUT)**
- **Meet DDRII JEDEC Spec and Support DDRIII, Low Power DDRIII / DDRIV VTT Application**
- **Soft-Start Function**
- **UVLO and OCP Protection**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV ,Copier/Printer, Set-Top Box

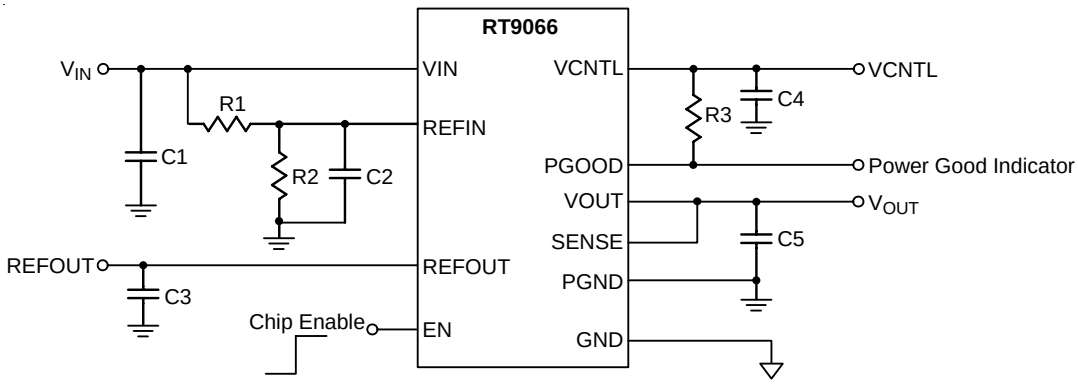
Marking Information



01= : Product Code

YMDNN : Date Code

Simplified Application Circuit



Ordering Information

RT9066□□

Package Type
QW : WDFN-16L 5x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)

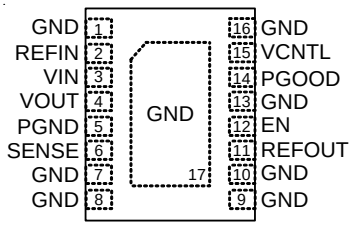
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

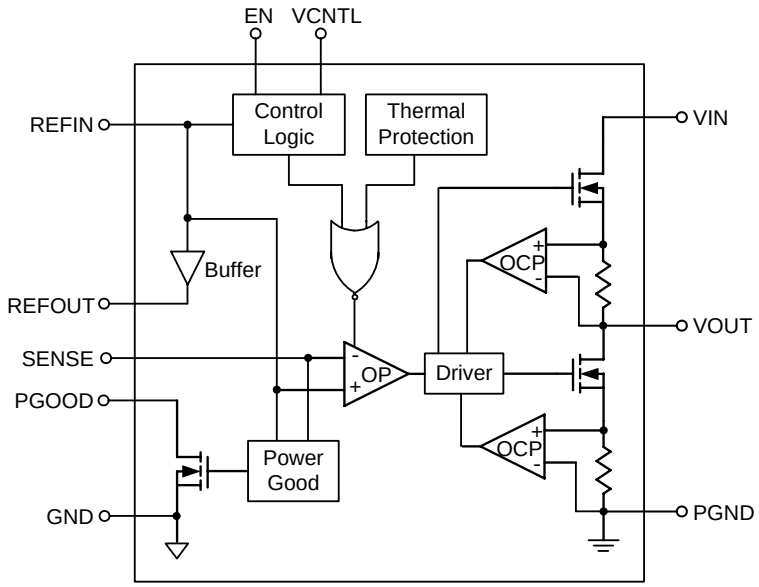


WDFN-16L 5x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 7, 8, 9, 10, 13, 16, 17 (Exposed Pad)	GND	Signal Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2	REFIN	Reference Voltage Input.
3	VIN	Supply Voltage Input.
4	VOUT	Power Output.
5	PGND	Power Ground.
6	SENSE	Voltage Sense Input. Connect to positive terminal of the output capacitor or the load.
11	REFOUT	Reference Voltage Output. Connect a 0.1μF ceramic capacitor to GND.
12	EN	Chip Enable. For DDR VTT application, connect EN to SLP_S3. For any other application(s), use EN as the ON/OFF function.
14	PGOOD	PGOOD Open Drain Output. Connect a 100kΩ pull-high resistor to VCNTL.
15	VCNTL	2.5V, 3.3V or 5V Power Supply. A ceramic decoupling capacitor with a value between 1μF and 4.7μF is required.

Function Block Diagram



Operation

The RT9066 is a linear sink/source DDR termination regulator with current capability up to 4.5A. The RT9066 builds in a high side N-type power MOSFET which provides current sourcing and a low side N-type power MOSFET which provides current sinking. All the control circuits are supplied by the power VCNTL. In normal operation, the error amplifier OP adjusts the gate driving voltage of the power MOSFET to achieve SENSE voltage well tracking the REFIN voltage.

Both the source and sink currents are detected by the internal sensing resistor, and the OCP function will work to limit the current to a designed value when overload happens. Furthermore, the current will be folded back to be one half if VOUT is out of the power good window.

Buffer

This function provides REFOUT output equal to REFIN with 10mA source/sink current capability.

Power Good

When the SENSE voltage is in the power good window and lasts for a certain delay time, the PGOOD pin will be high impedance, and the PGOOD voltage will be pulled high by the external resistor.

Control Logic

This block includes VCNTL UVLO, REFIN UVLO and Enable/Disable function, provides logic control to the whole chip.

Thermal Protection

Both the high side and low side power MOSFET will be turned off when the junction temperature is higher than typically 160°C, and released to normal operation when junction temperature falls below typically 120°C.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VCNTL ---------- –0.3V to 6V
- Input Voltage, EN, REFIN, SENSE ---------- –0.3V to 6V
- Output Voltage, VOUT, REFOUT, PGOOD ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-16L 5x3 ---------- 3.333W
- Package Thermal Resistance (Note 2)
  WDFN-16L 5x3, θ_{JA} ---------- 30°C/W
  WDFN-16L 5x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Control Input Voltage, VCNTL ---------- 2.375V to 5.5V
- Supply Input Voltage, VIN ---------- 1.1V to 2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 1.5V, V_{EN} = V_{CNTL} = 5V, V_{REFIN} = V_{SENSE} = 0.75V, C_{OUT} = 10µF x 5, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{EN} = V_{CNTL}, No Load	--	1.5	2	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{EN} = 0V, V_{REFIN} = 0V, No Load	--	65	80	µA
		V_{EN} = 0V, V_{REFIN} > 0.4V, No Load	--	200	400	µA
VIN Supply Current	I_{VIN}	V_{EN} = V_{CNTL}, No Load	--	--	10	mA
VIN Shutdown Current	I_{SHDN_VIN}	V_{EN} = 0V, No Load	--	0.1	50	µA
Output						
Output DC Voltage	V_{SENSE}	V_{IN} = 1.8V, V_{REFIN} = 0.9V (DDRII), I_{OUT} = 0A	--	0.9	--	V
			–10	--	10	mV
		V_{IN} = 1.5V, V_{REFIN} = 0.75V (DDRIII), I_{OUT} = 0A	--	0.75	--	V
			–10	--	10	mV
Output Voltage Tolerance to REFIN	V_{VOTOL}	–4.3A < I_{OUT} < 4.3A	–20	--	20	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Source Current Limit	$I_{LIM\_VOUT\_SR}$	VOUT in PGOOD window	5	--	9	A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_SK}$	VOUT in PGOOD window	5	--	9	A
VOUT Discharge Resistance	$R_{DISCHARGE}$	V_{REFIN} = 0V, V_{OUT} = 0.3V, V_{EN} = 0V	--	18	25	Ω
Power Good Comparator						
PGOOD Threshold	V_{TH_PGOOD}	V_{SENSE} lower threshold with respect to V_{REFIN}	–23.5	–20	–17.5	%
		V_{SENSE} upper threshold with respect to V_{REFIN}	17.5	20	23.5	
		PGOOD Hysteresis	--	5	--	
PGOOD Start-Up Delay	$T_{PGDELAY1}$	Start-up rising edge, V_{SENSE} within 15% of V_{REFIN}	--	2	--	ms
Output Low Voltage	V_{LOW_PGOOD}	I_{SINK} = 4mA	--	--	0.2	V
PGOOD Bad Delay	$T_{PGDELAY2}$	V_{SENSE} is outside of ±20% PGOOD window	--	10	--	μs
Leakage Current	$I_{LEAKAGE\_PGOOD}$	V_{SENSE} = V_{REFIN} (PGOOD high impedance), V_{PGOOD} = V_{CNTL} + 0.2V	--	--	1	μA
REFIN and REFOUT						
REFIN Input Current	I_{REFIN}	V_{EN} = V_{CNTL}	--	--	1	μA
REFIN Voltage Range	V_{REFIN}		0.5	--	1.8	V
REFIN Under Voltage Lockout	V_{UVLO_REFIN}	REFIN Rising	360	390	420	mV
		Hysteresis	--	20	--	
REFOUT Voltage Tolerance to VREFIN	V_{TOL_REFOUT}	–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.9V	–15	--	15	mV
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.75V	–15	--	15	
		–10mA < I_{REFOUT} < 10mA, V_{REFIN} = 0.6V	–15	--	15	
REFOUT Source Current Limit	$I_{LIM\_REFOUT\_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit	$I_{LIM\_REFOUT\_SK}$	V_{REFOUT} = V_{IN}	10	40	--	mA
UVLO/EN Logic Threshold						
UVLO Threshold	V_{UVLO_VCNTL}	Rising	2.2	2.3	2.375	V
		Hysteresis	--	100	--	mV
Enable High-Level Input Voltage	V_{IN_H}		1.7	--	--	V
Enable Low-Level Input Voltage	V_{IN_L}		--	--	0.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable Hysteresis Voltage	V_{EN_HYS}		--	0.5	--	V
Enable Logic Input Leakage Current	$I_{LEAKAGE\_EN}$		–1	--	1	μA
Thermal Shutdown						
Thermal Shutdown Threshold	TSD	Shutdown Temperature	--	160	--	°C
		Hysteresis	--	40	--	

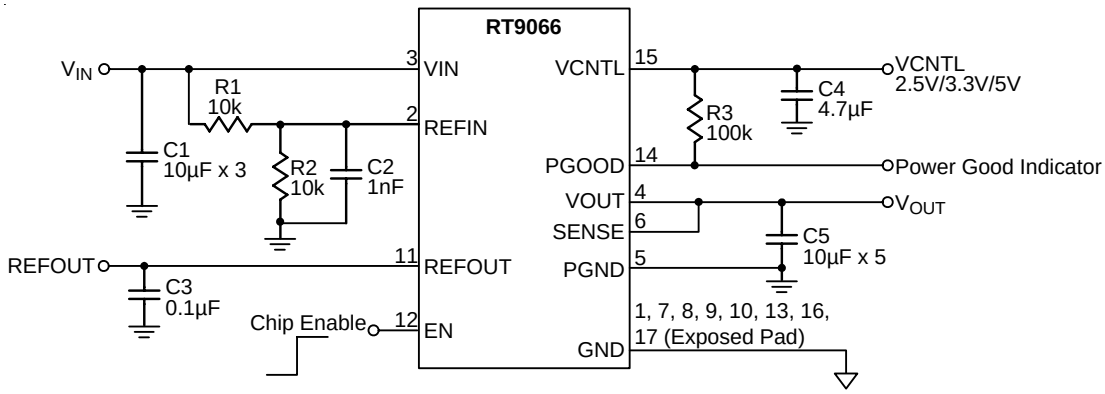
Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

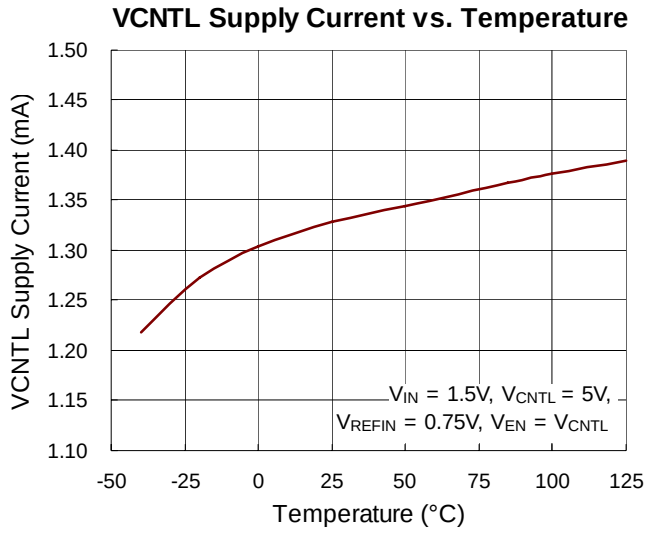
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

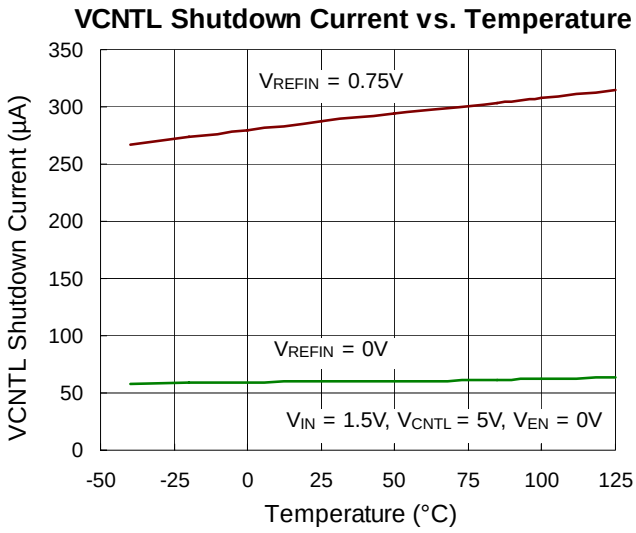
Note 4. The device is not guaranteed to function outside its operating conditions.

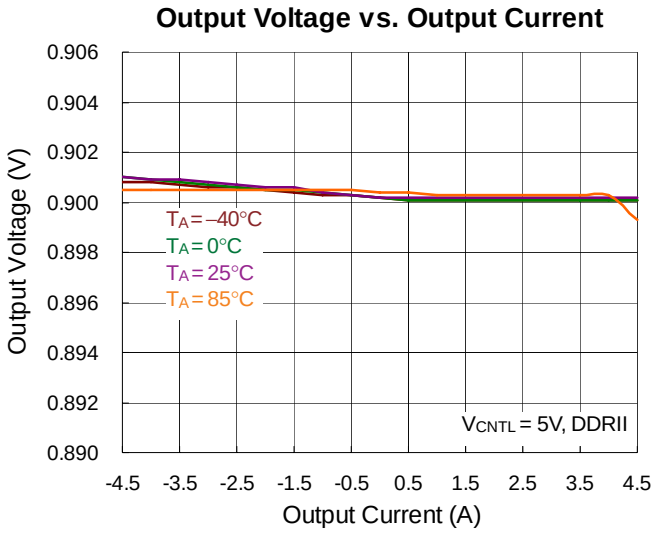
Typical Application Circuit

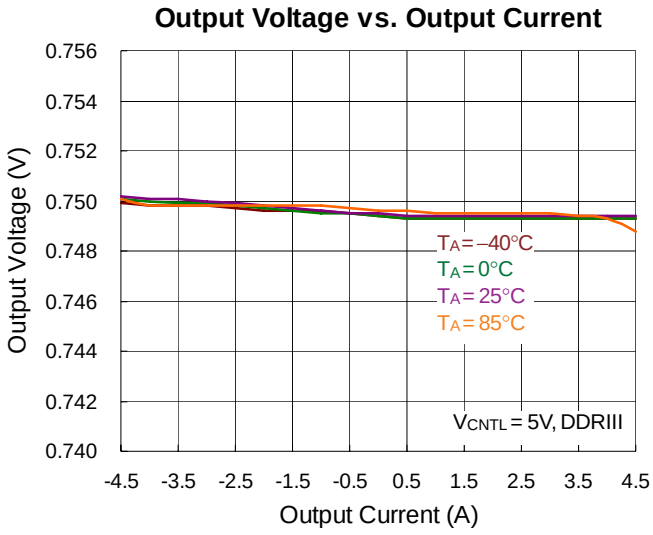


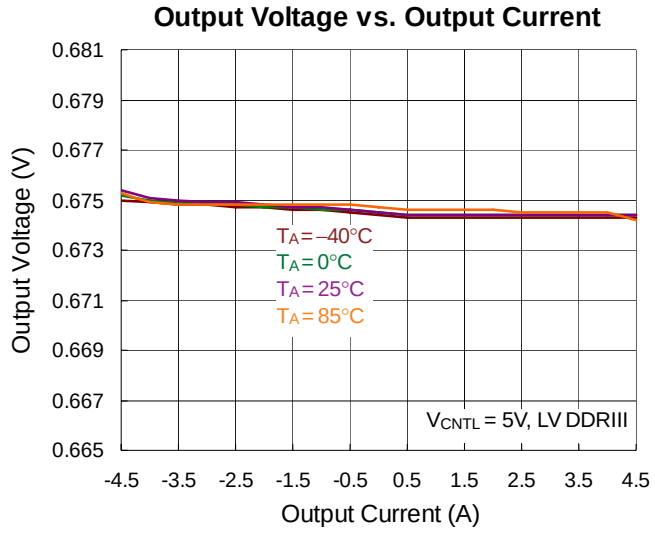
Typical Operating Characteristics

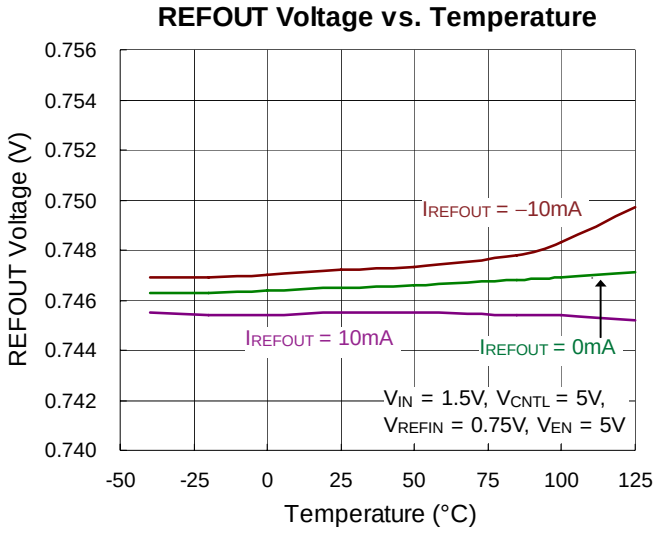




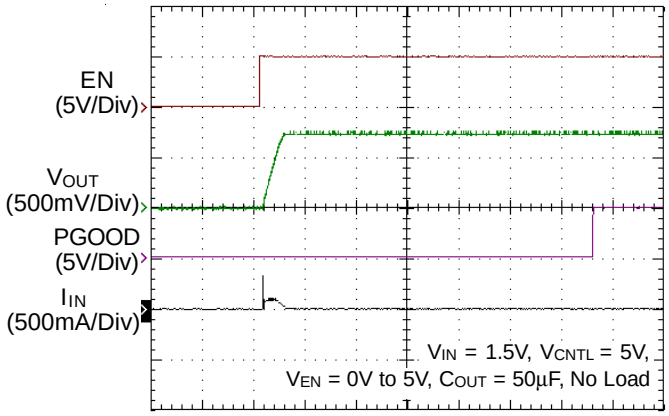




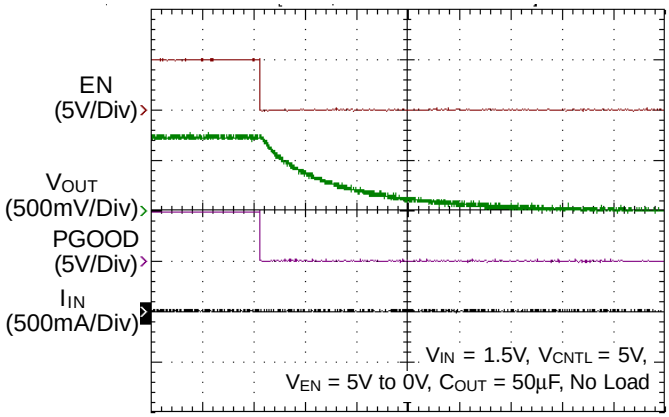




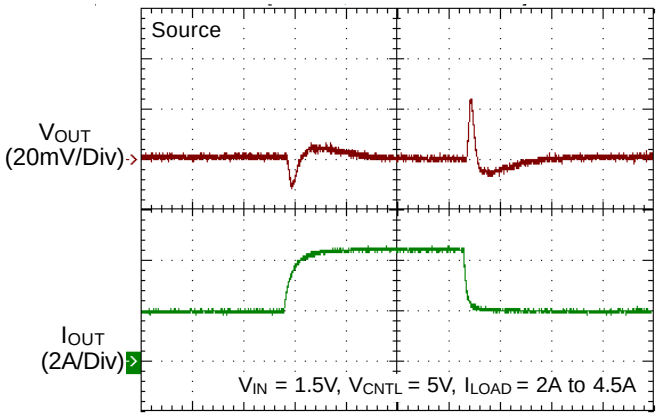
EN Turn On Response



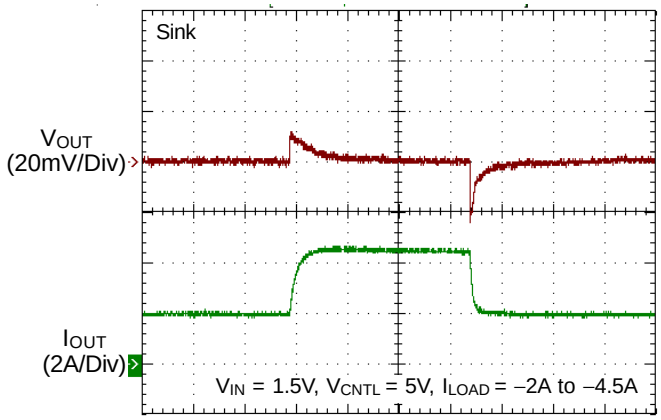
EN Turn Off Response



Load Transient Response



Load Transient Response



Application Information

The RT9066 is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems such as notebook PC applications. The RT9066 possesses a high speed operating amplifier that provides fast load transient response and only requires three 10μF ceramic input capacitors and five 10μF ceramic output capacitors.

REFOUT Regulator

REFOUT is a reference output voltage with source/sink current capability up to 10mA. To ensure stable operation, a 0.1μF ceramic capacitor connected between REFOUT and GND is recommended.

Capacitor Selection

To achieve best performance of the RT9066, it is recommended to follow the following descriptions for capacitor selection.

VCNTL Capacitor

Add a ceramic capacitor 4.7μF placed to VCNTL pin as close as possible to stabilize the supply voltage (2.5V, 3.3V or 5V rail) from any parasitic impedance from the supply.

VIN Capacitor

Good bypassing is recommended from VIN to GND to improve transient response. It is recommended to place three 10μF or greater input capacitors as close as possible to the IC and the distance must be less than 0.5 inch from the VIN pin.

VOUT Capacitor

For stable operation, the total capacitance of the VTT output terminal must be greater than 30μF. The RT9066 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. Five 10μF ceramic capacitors are used in the typical application circuit. The output capacitor should be located near the VOUT pin as close as possible.

Operation State Setting

The EN pin can be connected to SLP_S3 signal for DDR VTT application. Both VOUT and REFOUT are turned on in normal state (EN = High, REFIN > 0.39V). In standby state (EN = Low, REFIN > 0.39V), REFOUT voltage is kept alive and VOUT voltage is turned off and discharged via internal MOSFET. When EN = Low and REFIN < 0.39V, the RT9066 enters shutdown state, and VOUT and REFOUT are turned off and discharged to ground via internal MOSFETs. Table 1 summarizes the above-mentioned operation state setting, and Figure 1 shows a typical start-up and shutdown timing diagram.

Table 1. Operation State Setting

State	EN	REFIN	VOUT	REFOUT
Normal	High	> 0.39V	On	On
Standby	Low	> 0.39V	Off	On
Shutdown	Low	< 0.39V	Off	Off

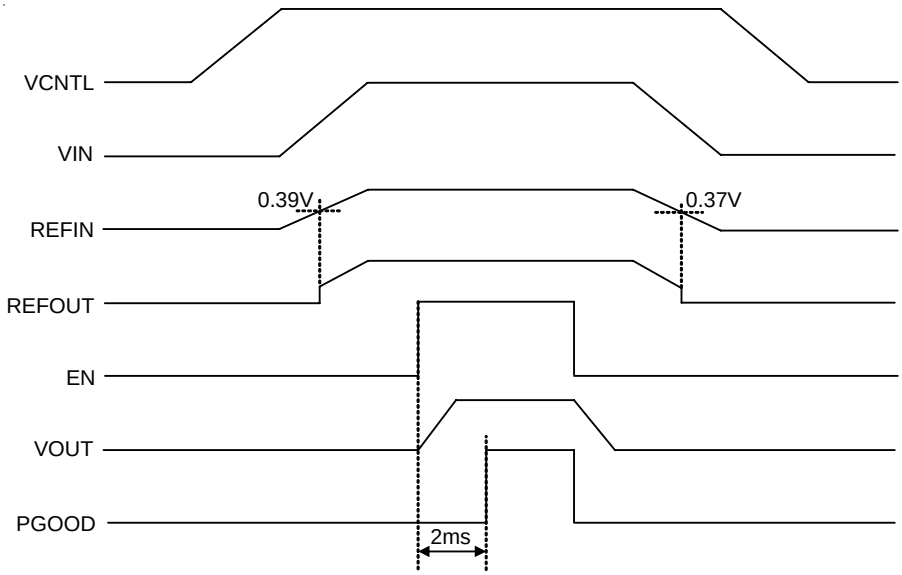


Figure 1. Typical Start-up and Shutdown Timing Diagram

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-16L 5x3 package, the thermal resistance θ_{JA} is 30°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.333W for WDFN-16L 5x3

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

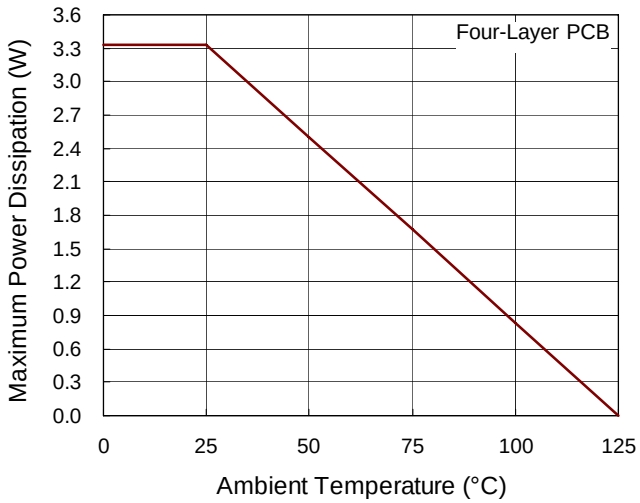
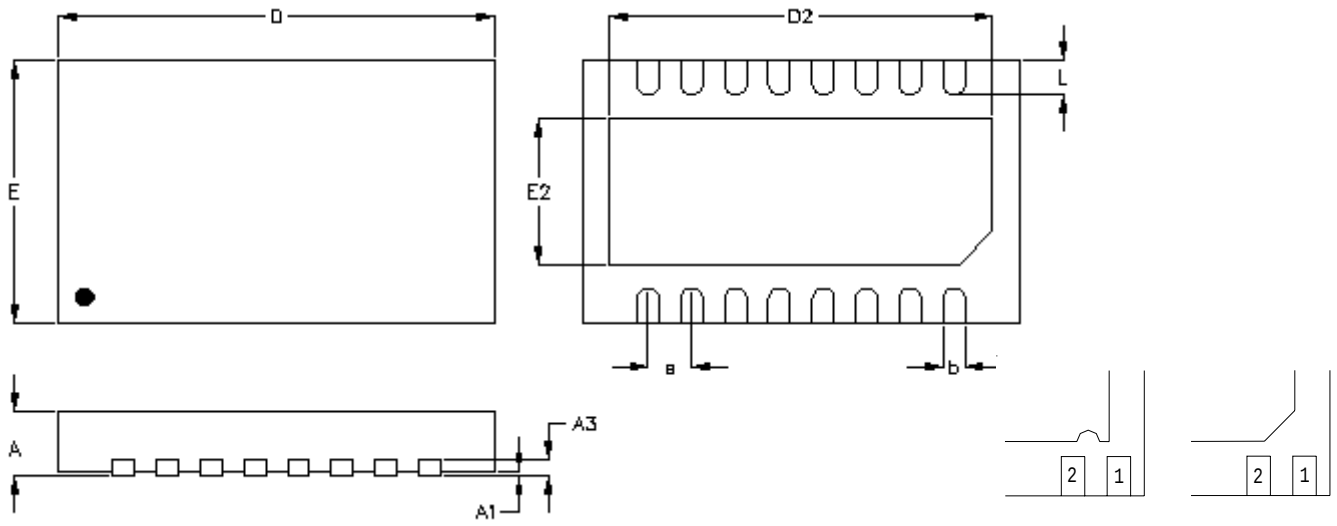


Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	4.350	4.450	0.171	0.175
E	2.950	3.050	0.116	0.120
E2	1.600	1.700	0.063	0.067
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L DFN 5x3 Package

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