RICHTEK®

RT9059

3A Ultra-Low Dropout Voltage Regulator

1 General Description

The RT9059 is a high-performance positive voltage regulator designed for applications requiring very low input voltage and very low dropout voltage at up to 3A. It operates with a VIN as low as 1V and a 3V VDD, with a programmable output voltage as low as 0.8V. The RT9059 features ultra-low dropout, making it ideal for applications where VOUT is very close to VIN. Additionally, the RT9059 has an enable pin to further reduce power dissipation during shutdown. The RT9059 provides excellent regulation over variations in line, load, and temperature. The RT9059 also provides a power-good signal to indicate if the voltage level of VO reaches 90% of its rated value. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

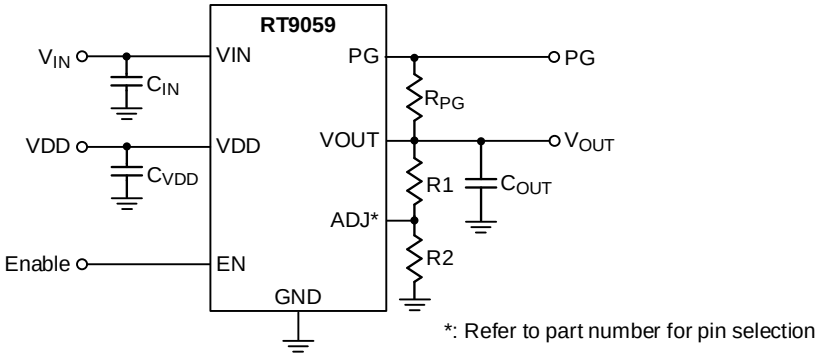
2 Features

- **Output Current up to 3A**
- **High Accuracy ADJ Voltage (1.5%)**
- **Dropout Voltage: 350mV @ 3A (Typical)**
- **VOUT Power-Good Signal**
- **VOUT Pull Low Resistance when Disabled**
- **Current-Limit Protection**
- **Over-Temperature Protection**

3 Applications

- Notebook PC Applications
- Motherboard Applications

4 Simplified Application Circuit



*: Refer to part number for pin selection

5 Ordering and Marking Information

Version (Adjustable Output Fixed Output Voltage Code)	Product Code	Lead Plating System	Package(1)		Fixed Output Voltage Accuracy		VDD Pin Shutdown Current Max.	
			WDFN-10L 3x3 (W-Type)	SOP-8 (Exposed Pad-Option 1)	±1.5%	±1%	1μA	30μA
RT9059GQW	0Q=	G: Green (Halogen Free and Pb Free)	V		V		V	
RT9059-15GQW	1E=		V		V		V	
RT9059-18GQW	18=		V		V		V	
RT9059-25GQW	8F=		V		V		V	
RT9059GSP	RT9059GSP			V	V		V	
RT9059-15GSP	RT905915GSP			V	V		V	
RT9059-18GSP	RT905918GSP			V	V		V	
RT9059-25GSP	RT905925GSP			V	V		V	
RT9059AGQW	4S=		V		V			V
RT9059BGQW	PS=		V			V	V	
RT9059CN-A	V1=		V		V		V	

Note 1. Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

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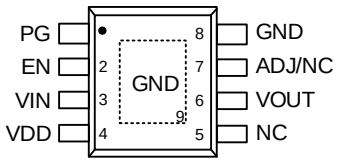
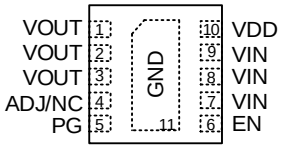
6 Pin Configuration

(TOP VIEW)



SOP-8 (Exposed Pad)



WDFN-10L 3x3

7 Functional Pin Description

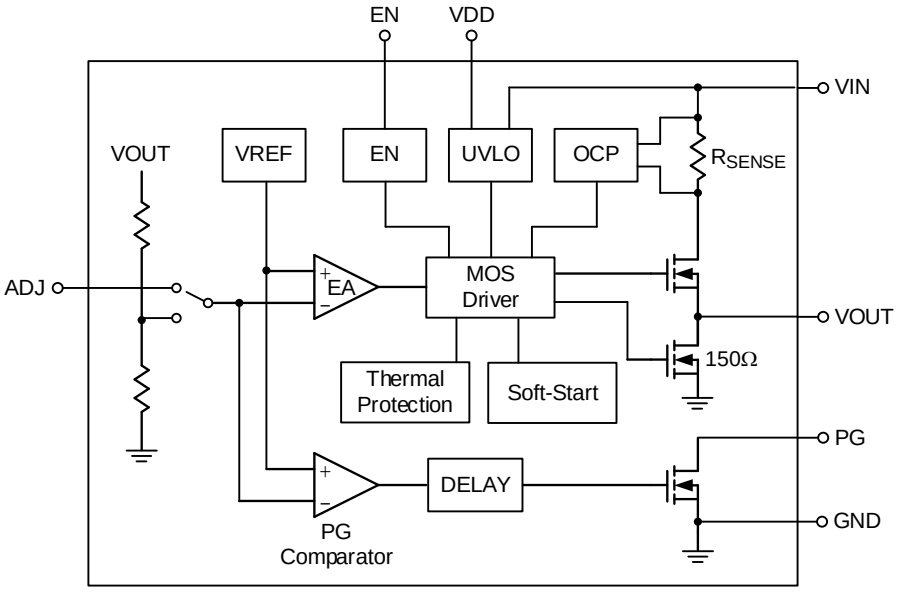
7.1 SOP-8 Package

Pin No.		Pin Name	Pin Function
Adjustable Output Voltage	Fixed Output Voltage		
1	1	PG	Power-good indicator. This open-drain output pin is pulled high when the VOUT or FB voltage is within the target range. It is pulled to ground under protection conditions, EN shutdown, or during the soft-start period.
2	2	EN	Enable control input. A logic-high enables the converter, while a logic-low forces the device into shutdown mode. Connect this pin to the VIN pin to conserve the system's power rail, or connect this pin to an external power rail for power sequence control. It is recommended to apply the enable voltage after the VIN pin voltage is ready for correct soft-start function. Do not leave this pin floating.
3	3	VIN	Supply voltage input. The input voltage range is from 1V to 5.5V. A suitable input capacitor should be placed close to this pin to minimize voltage spikes and noise, ensuring a stable input voltage.
4	4	VDD	Supply voltage of the control circuit. This pin provides the necessary power for the internal control logic and analog circuitry. It is important to ensure that the VDD voltage is stable and within the specified range to guarantee proper operation of the device.
5	5, 7	NC	No internal connection. Connect this pin to the GND plane of the top layer to extend the GND copper area to enhance the thermal performance.
6	6	VOUT	LDO output pin. Connect a ceramic capacitor with a capacitance of at least 10μF as close as possible from this pin to GND to minimize the output impedance.
7	--	ADJ	Feedback voltage input. This pin is used to set the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.8V (typical). Place the resistive voltage divider as close to the FB pin as possible. Do not leave this pin floating.
8, 9 (Exposed Pad)	8, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

7.2 WDFN-10L 3x3 Package

Pin No.		Pin Name	Pin Function
Adjustable Output Voltage	Fixed Output Voltage		
1, 2, 3	1, 2, 3	VOUT	LDO output pin. Connect a ceramic capacitor with a capacitance of at least 10μF as close as possible from this pin to GND to minimize the output impedance.
--	4	NC	No internal connection. Connect this pin to the GND plane of the top layer to extend the GND copper area to enhance the thermal performance.
4	--	ADJ	Feedback voltage input. This pin is used to set the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.8V (typical). Place the resistive voltage divider as close to the FB pin as possible. Do not leave this pin floating.
5	5	PG	Power-good indicator. This open-drain output pin is pulled high when the VOUT or FB voltage is within the target range. It is pulled to ground under protection conditions, EN shutdown, or during soft-start period.
6	6	EN	Enable control input. A logic-high enables the converter, while a logic-low forces the device into shutdown mode. Connect this pin to the VIN pin to conserve the system's power rail and connect this pin to the external power rail for power sequence control. It is recommended to apply the enable voltage after the VIN pin voltage is ready for correct soft-start function. Do not leave this pin floating.
7, 8, 9	7, 8, 9	VIN	Supply voltage input. The input voltage range is from 1V to 5.5V. A suitable input capacitor should be placed close to this pin to minimize voltage spikes and noise, ensuring a stable input voltage.
10	10	VDD	Supply voltage of the control circuit. This pin provides the necessary power for the internal control logic and analog circuitry. It is important to ensure that the VDD voltage is stable and within the specified range to guarantee proper operation of the device.
11 (Exposed Pad)	11 (Exposed Pad)	GND	Ground: The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN to GND
  - DC ---------- –0.3V to 6V
  - < 10ms ---------- –0.3V to 7V
- Control Voltage, VDD to GND
  - DC ---------- –0.3V to 6V
  - < 10ms ---------- –0.3V to 7V
- VOUT, EN, ADJ, PG ---------- –0.3V to 6V
- Supply Input Voltage, VIN to GND ---------- –0.3V to 7V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

10 ESD Ratings

(Note 3)

- ESD Susceptibility
- HBM (Human Body Model)----------2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 1V to 5.5V
- Control Voltage VDD (V_{DD} > V_{OUT} + 1.5V) ---------- 3V to 5.5V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 85°C

Note 4. The device is not guaranteed to function outside its operating conditions.

12 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WDFN-10L 3x3	SOP-8 (Exposed Pad)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	55	47	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	63.3	75.3	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	6	6	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	37.4	35.2	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.14	4.52	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.3	20.6	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are simulated on a high effective-thermal-conductivity four-layer test board, which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

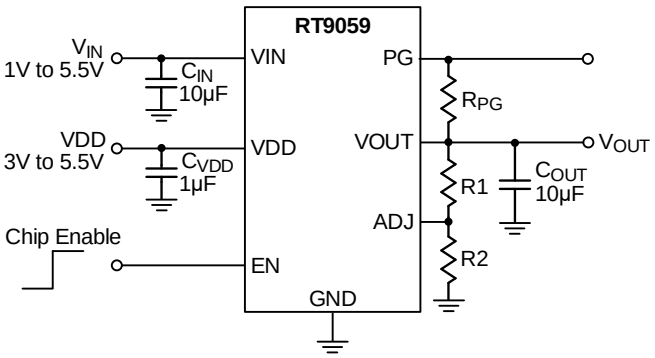
13 Electrical Characteristics

(V_{DD} = 5V, C_{IN} = C_{OUT} = 10μF, C_{VDD} = 1μF, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Operation Range	V_{DD}		3	--	5.5	V
VDD POR Threshold	V_{POR_VDD}	VDD Rising	2.4	2.7	3	V
VDD POR Falling Hysteresis	$V_{POR\_HYS\_POR}$	VDD Falling	0.15	0.2	--	V
Input Voltage Range	V_{IN}		1	--	5.5	V
VIN POR Threshold	V_{POR_VIN}	VIN Rising	0.7	0.8	0.9	V
VIN POR Falling Hysteresis	$V_{POR\_HYS\_VIN}$	VIN Falling	0.15	0.2	0.25	V
Quiescent Curren	I_Q	I_{OUT} = 0A	--	0.6	1.2	mA
Reference Voltage	V_{REF}		0.788	0.8	0.812	V
Fixed Output Voltage Accuracy	V_{OUT_ACC}	RT9059 series, RT9059A	–1.5	--	1.5	%
		RT9059B	–1	--	1	
VOUT Load Regulation	V_{LOAD_REG}	I_{OUT} = 1mA to 3A, V_{IN} = V_{OUT} + 1V	--	0.5	1	%
OUT Line Regulation	V_{LINE_REG}	V_{DD} = 3.6V to 5.5V, V_{IN} = V_{OUT} + 1V to 5V, I_{OUT} = 1mA	--	0.2	0.6	%
Dropout Voltage	V_{DROP}	I_{OUT} = 2A	--	250	350	mV
		I_{OUT} = 3A	--	350	450	
Current Limit	I_{LIM}	V_{IN} = 3.6V	3.1	3.6	4.2	A
Short Circuit Current	I_{SC}	V_{OUT} < 0.2V	1	1.4	1.8	A
Discharge Resistor	R_{DISCHG}	V_{EN} = 0V	--	150	--	Ω
Over-Temperature Protection Temperature	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	70	--	°C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PG Rising Threshold	V_{PG}	Threshold, V_{PG} from low to high		--	90	--	%
PG Hysteresis	V_{PG_HYS}	Hysteresis, V_{PG} from high to low		--	10	--	%
PG Delay Time	t_{PG_DE}			0.2	1	1.5	ms
PG Sink Capability	V_{PG_L}	I_{PG_SNK} = 10mA		--	0.2	0.4	V
EN Input Voltage Rising Threshold	V_{EN_R}	Logic-high		1.2	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}	Logic-low		--	--	0.4	
EN Delay Time	t_{EN_DE}			0.3	0.85	1.4	ms
EN Input Current	I_{EN}	V_{EN} = 5V		--	12	--	μA
VDD Pin Shutdown Current	I_{SHDN_VDD}	V_{EN} = 0V	RT9059 series, RT9059B	--	--	1	μA
			RT9059A	--	15	30	
VIN Pin Shutdown Current	I_{SHDN_VIN}	V_{EN} = 0V, V_{IN} = 5V		--	--	1	μA
Inrush Current	I_{INRUSH}	V_{OUT} = 1.8V, C_{OUT} = 10μF, I_{OUT} = 1A		--	0.5	--	A
Soft-Start Time	t_{SS}			1.9	2.8	3.75	ms

14 Typical Application Circuit



V_{OUT} = 0.8 x (R1+R2)/R2

Figure 1. Adjustable Voltage Regulator

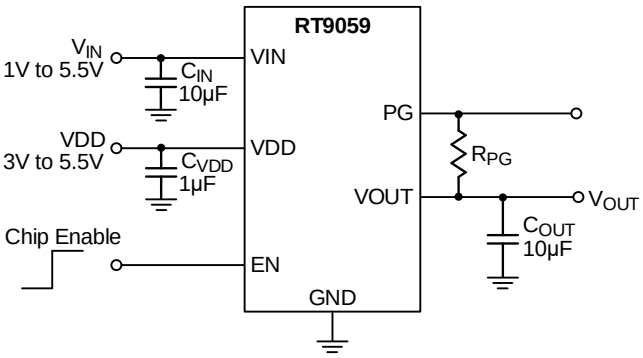
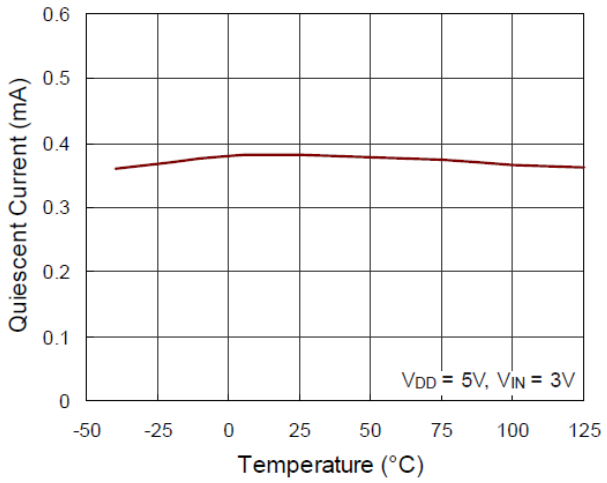


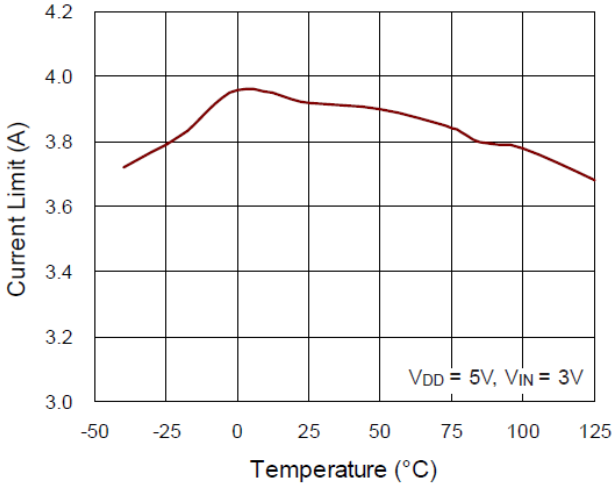
Figure 2. Fixed Voltage Regulator

15 Typical Operating Characteristics

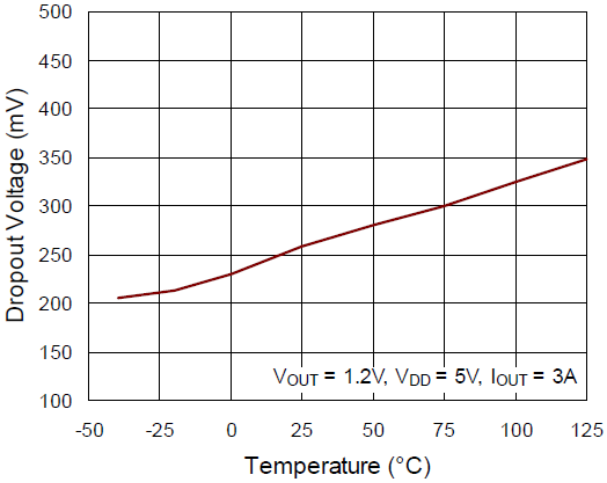
Quiescent Current vs. Temperature



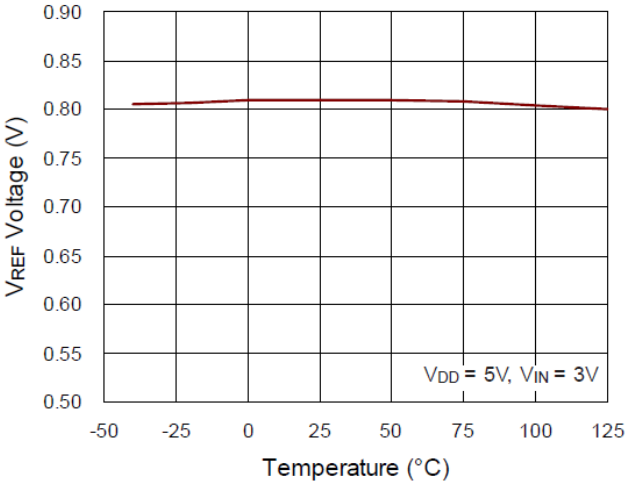
Current Limit vs. Temperature



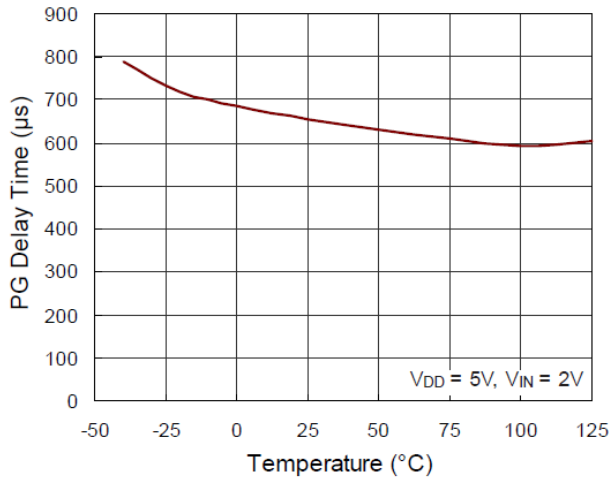
Dropout Voltage vs. Temperature



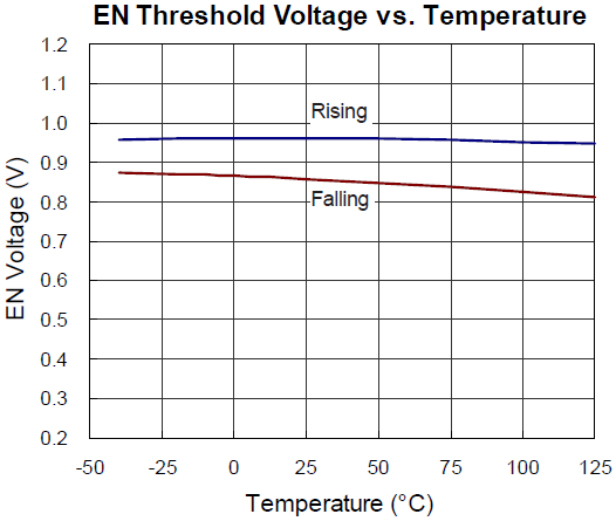
V_{REF} Voltage vs. Temperature



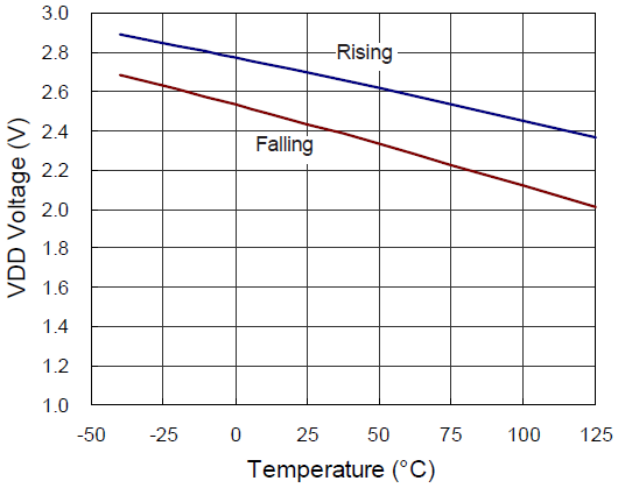
PG Delay Time vs. Temperature



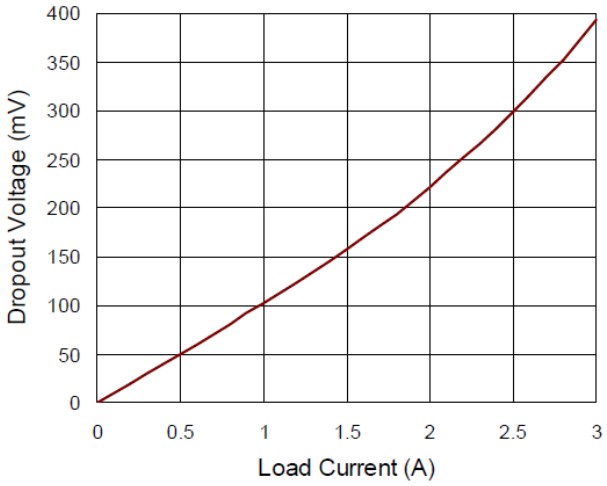
EN Threshold Voltage vs. Temperature



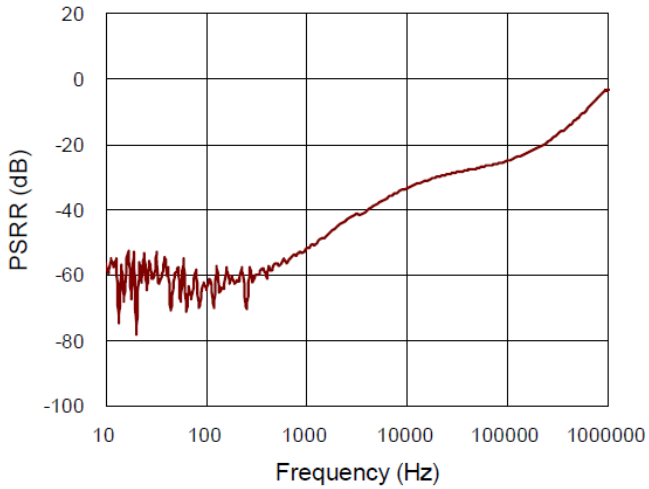
VDD POR Threshold Voltage vs. Temperature



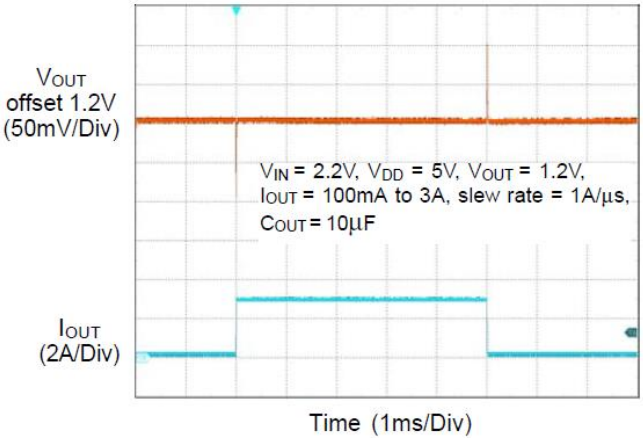
Dropout Voltage vs. Load Current



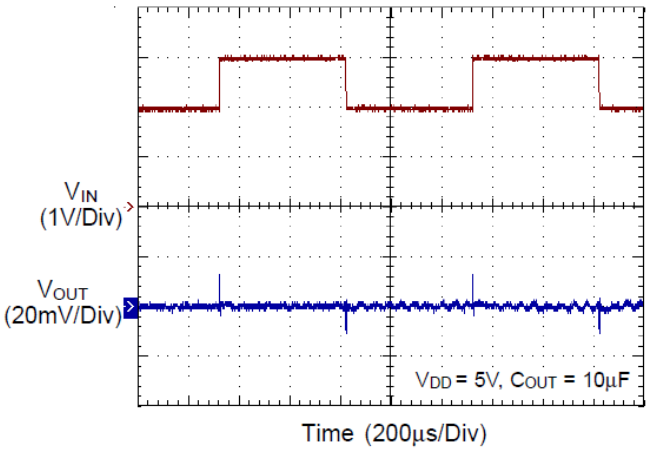
PSRR vs. Frequency



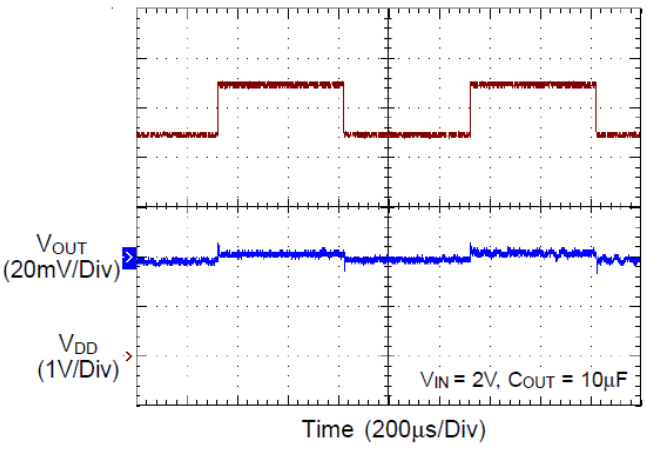
Load Transient Response



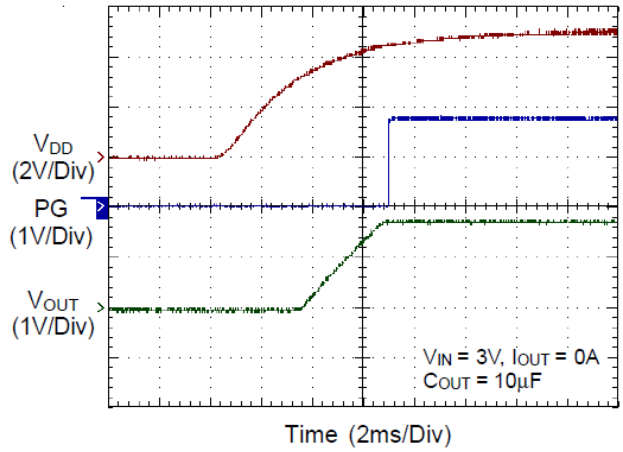
VIN Line Transient Response



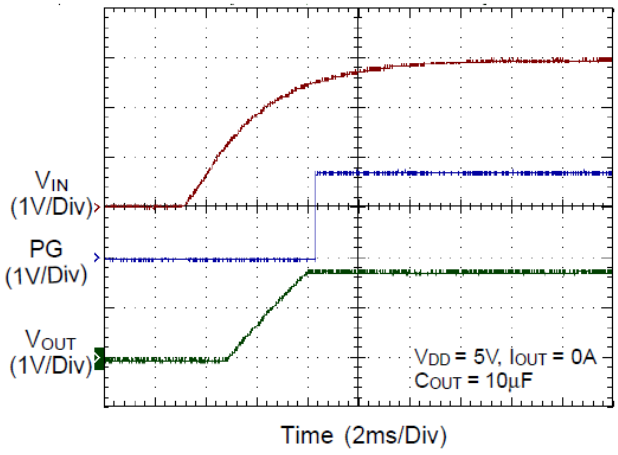
VDD Line Transient Response



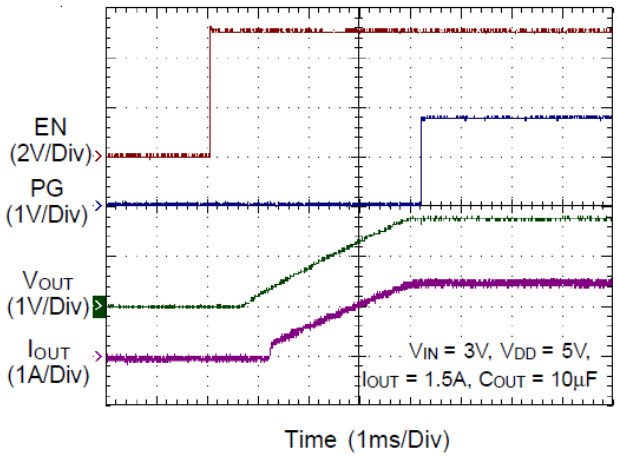
Start Up from V_{DD}



Start Up from V_{IN}



Start Up from Enable and PG Delay



16 Application Information

(Note 7)

16.1 Adjustable Mode Operation

The output voltage of the RT9059 is adjustable from 0.8V to VIN using external voltage divider resistors, as shown in the Typical Application Circuit (Figure 1). The values of resistors R1 and R2 should be more than 10kΩ to reduce power loss. The output voltage can be calculated using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the reference voltage (typically 0.8V).

16.2 Enable

The RT9059 enters shutdown mode when the EN pin is in a logic low condition. In this state, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to a typical 1μA. The RT9059 enters operation mode when the EN pin is in a logic high condition. If the EN pin is floating, note the RT9059's internal initial logic level. For the RT9059, the EN pin function pulls to a low level internally, so the regulator will be turned off when the EN pin is floating.

16.3 Input Capacitor

Good bypassing is recommended from input to ground to improve AC performance. A 10μF or greater input capacitor, located as close as possible to the IC, is recommended.

16.4 Output Capacitor

The output capacitor must meet both the minimum capacitance and ESR requirements in all LDO applications. The RT9059 is designed specifically to work with low ESR ceramic output capacitors for space-saving and performance considerations. Using a ceramic capacitor with a value of at least 10μF on the RT9059 output ensures stability. The RT9059 also works well with output capacitors of other types due to the wide stable ESR range. Output capacitors with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located no more than 0.5 inches from the VOUT pin of the RT9059 and returned to a clean analog ground.

16.5 Current Limit

The RT9059 includes an independent current limit and short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, minimally limiting the output current to 3.1A (typical). When the output voltage drops below 0.2V, the short circuit current protection activates the current foldback function and maintains the load current at a maximum of 1.8A. The output can be shorted to ground indefinitely without damaging the device.

16.6 Power-Good Function

The power good function is an open-drain output. Connect a 100kΩ pull-up resistor to VOUT to obtain an output voltage. The PG pin will output high immediately after the output voltage reaches 90% of the normal output voltage.

16.7 Over- Temperature Protection

Over-Temperature Protection limits power dissipation to prevent the RT9059 overheating. When the operating junction temperature exceeds 160°C, the circuit activates the over-temperature protection function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 70°C.

16.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA(EVB)}$, is 37.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a SOP-8 (Exposed Pad) package, the thermal resistance, $\theta_{JA(EVB)}$, is 35.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (37.4°C/W) = 2.67W for a WDFN-10L 3x3 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (35.2°C/W) = 2.84W for a SOP-8 (Exposed Pad) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in Figure 3 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

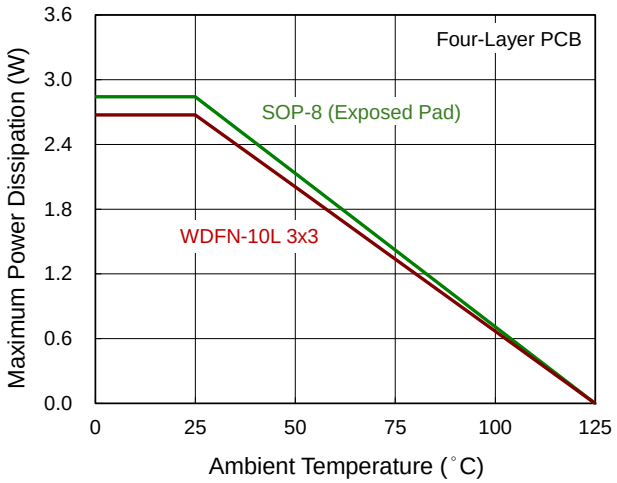
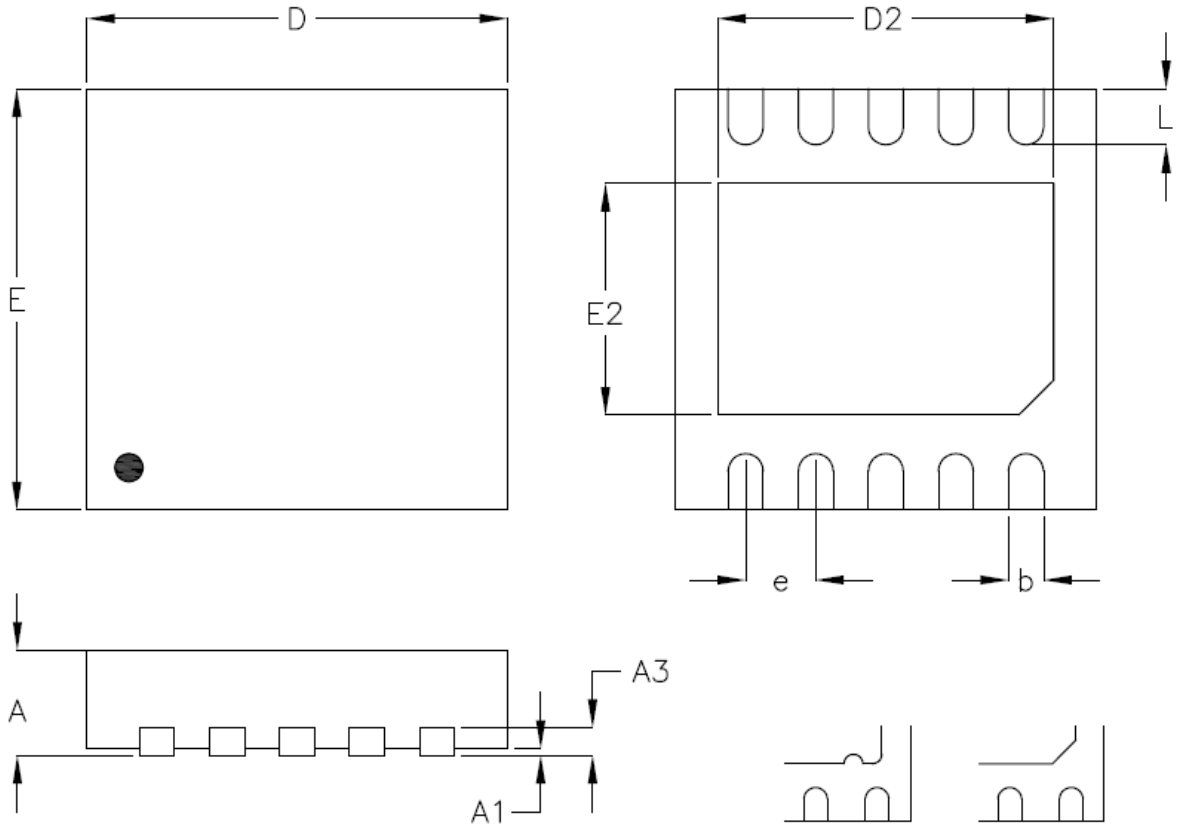


Figure 3. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension

17.1 WDFN-10L 3x3 Package

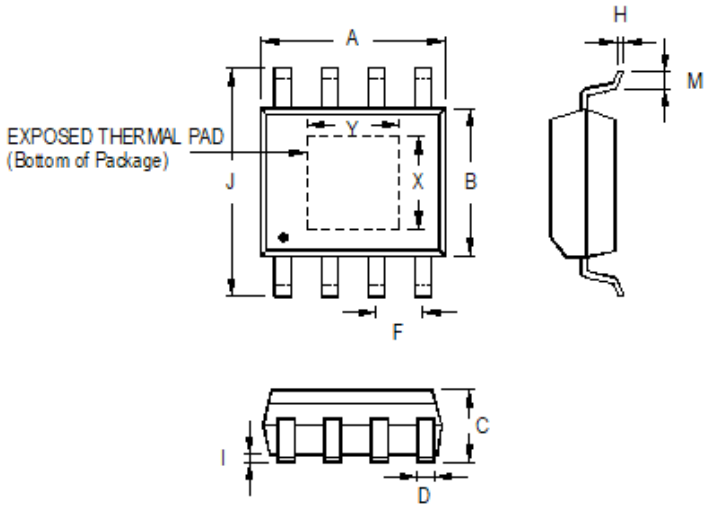


Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

17.2 SOP-8 (Exposed Pad) Package



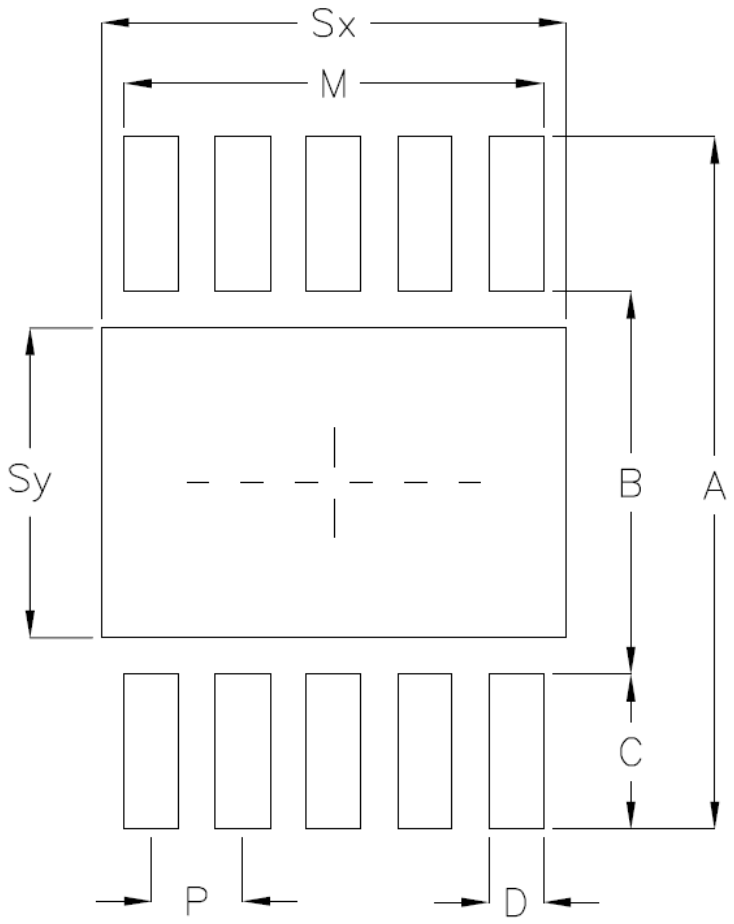
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 8. The package of the RT9059 uses Option 2.

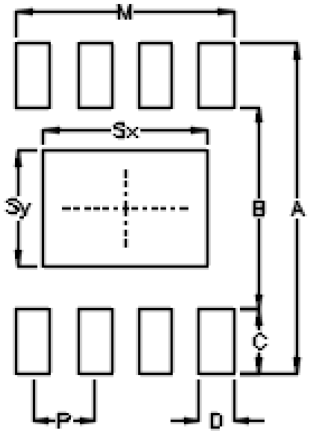
18 Footprint Information

18.1 WDFN-10L 3x3 Package



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

18.2 SOP-8 (Exposed Pad) Package



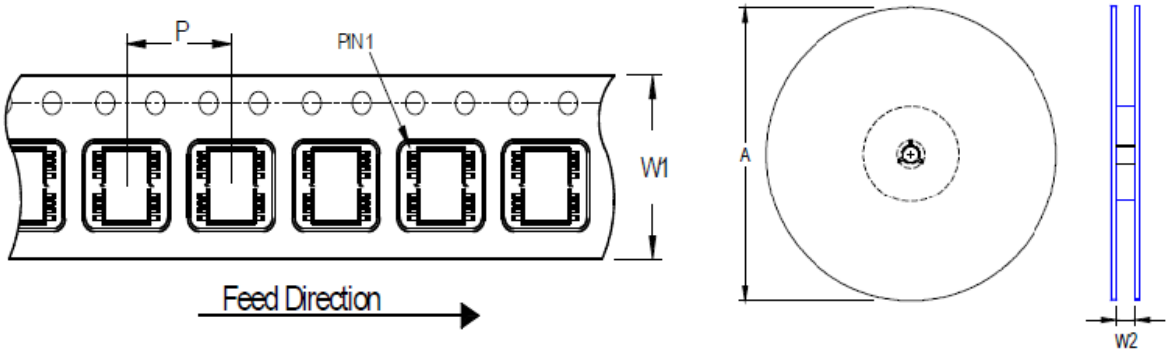
Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

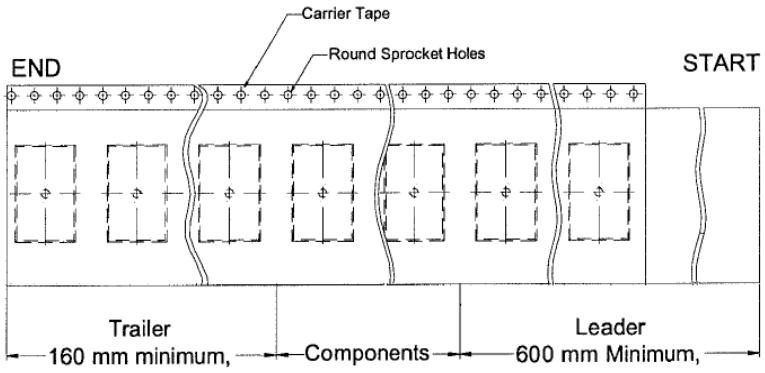
Note 9. The package of the RT9059 uses Option 2.

19 Packing Information

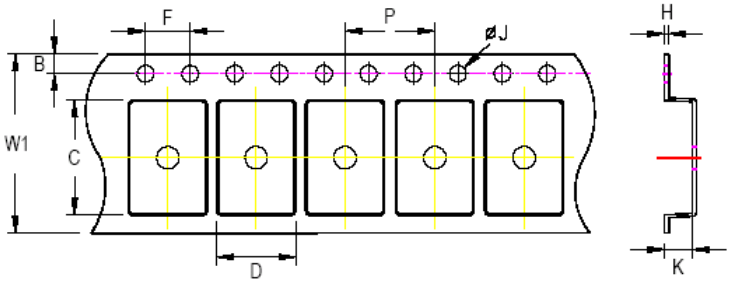
19.1 Tape and Reel Data

19.1.1 SOP-8 (Exposed Pad)





Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



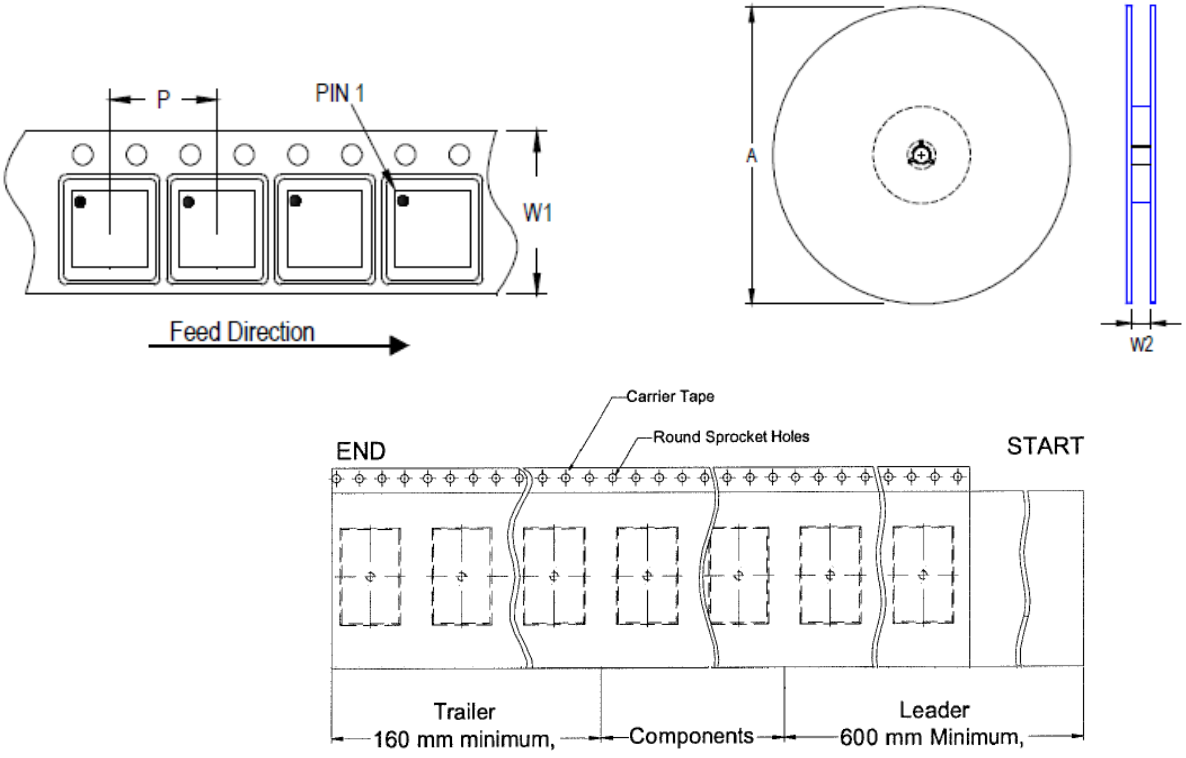
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

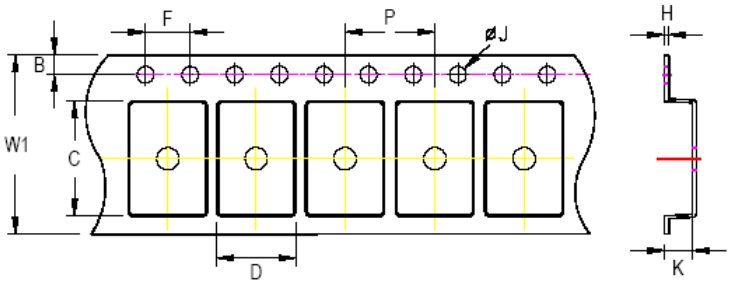
Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm

19.1.2 WDFN-10L 3x3

19.1.2.1 Units per Reel: 1500



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



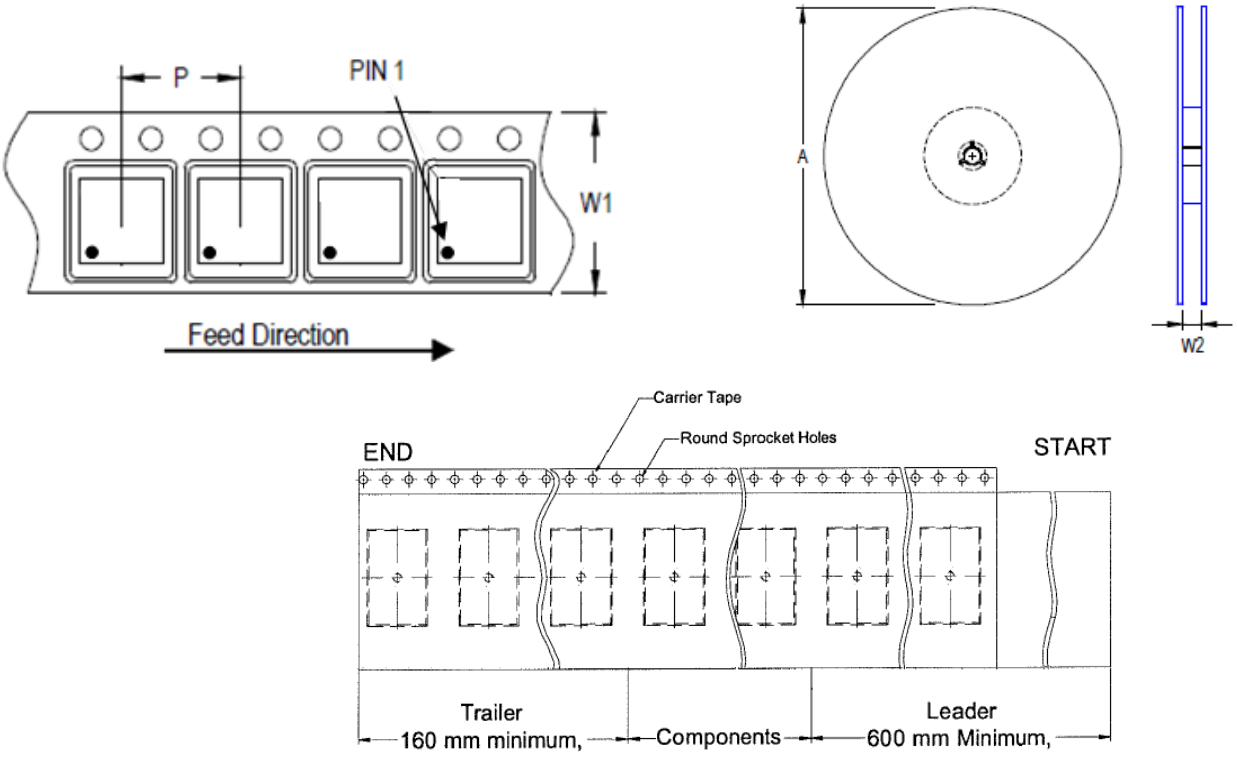
C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

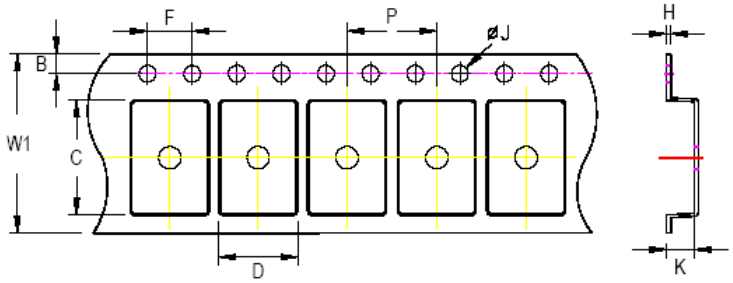
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.1.2.2 Units per Reel: 3000



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 Tape and Reel Packing

19.2.1 SOP-8 (Exposed Pad)

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

19.2.2 WDFN-10L 3x3

19.2.2.1 Units per Reel: 1500

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.2.2.2 Units per Reel: 3000

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
13	2023/5/29	Modify	*Ordering and Marking Information on page 1* *Electrical Characteristics on page 5* *Typical Operating Characteristics on page 7* *Packing Information on page 13 to 19*
14	2024/12/26	Modify	*Changed the pin names to PG.* *General Description on page 1* *Simplified Application Circuit on page 1* *Pin Configuration on page 4* *Functional Pin Description on page 4, 5* *Functional Block Diagram on page 7* *Absolute Maximum Ratings on page 7* *ESD Ratings on page 7* *Recommended Operating Conditions on page 7* *Thermal Information on page 8* *Electrical Characteristics on page 8, 9* *Typical Application Circuit on page 10* *Application Information on page 14, 15* *Footprint Information on page 18, 19* - Added Footprint Information