Multi-Phase PWM Controller with PWM-VID Reference

General Description

The RT8845A is a 4/3/2/1 phase synchronous Buck PWM controller which is optimized for high performance graphic microprocessor and computer applications. The RT8845A adopts G-NAVP^{TM} (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control. By utilizing the G-NAVP^{TM} topology, the operating frequency of the RT8845A varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP^{TM} with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The RT8845A provides complete fault protection functions including Over-Voltage (OV), Negative Voltage (NV), Over-Current (OC) and Under-Voltage Lockout (UVLO). The RT8845A is available in the WQFN-40L 5x5 package.

The RT8845A features external reference input and PWM-VID dynamic output voltage control, in which the feedback voltage is regulated and tracks external input reference voltage. Other features include adjustable switching frequency, dynamic phase number control, internal/external soft- start, power good indicator, and enable functions.

Ordering Information

RT8845A□□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

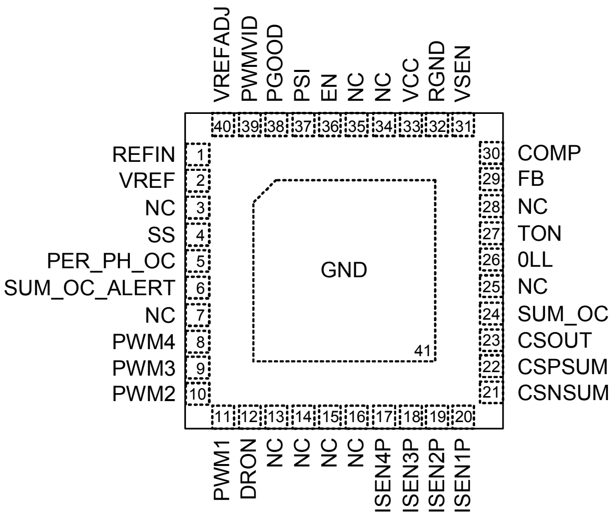
- **Multi-Phase PWM Controller**
- **Power State Indicator**
  - **1P-CCM/4P-CCM/1P-DEM**
- **Support 1.8V PWM-VID Interface**
- **External Reference Input Control**
- **PWM-VID Dynamic Voltage Control**
- **Dynamic Phase Number Control**
- **Internal/External Soft-Start**
- **Adjustable Current Limit Threshold**
- **Adjustable Switching Frequency**
- **UVP/OVP Protection**
- **Support an Ultra-Low Output Voltage as Standby Voltage**
- **Thermal Shutdown**
- **Power Good Indicator**

Applications

- GPU Core Supply for nVidia OVR4 + Spec.

Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

Marking Information

RT8845A
GQW
YMDNN

RT8845AGQW : Product Number

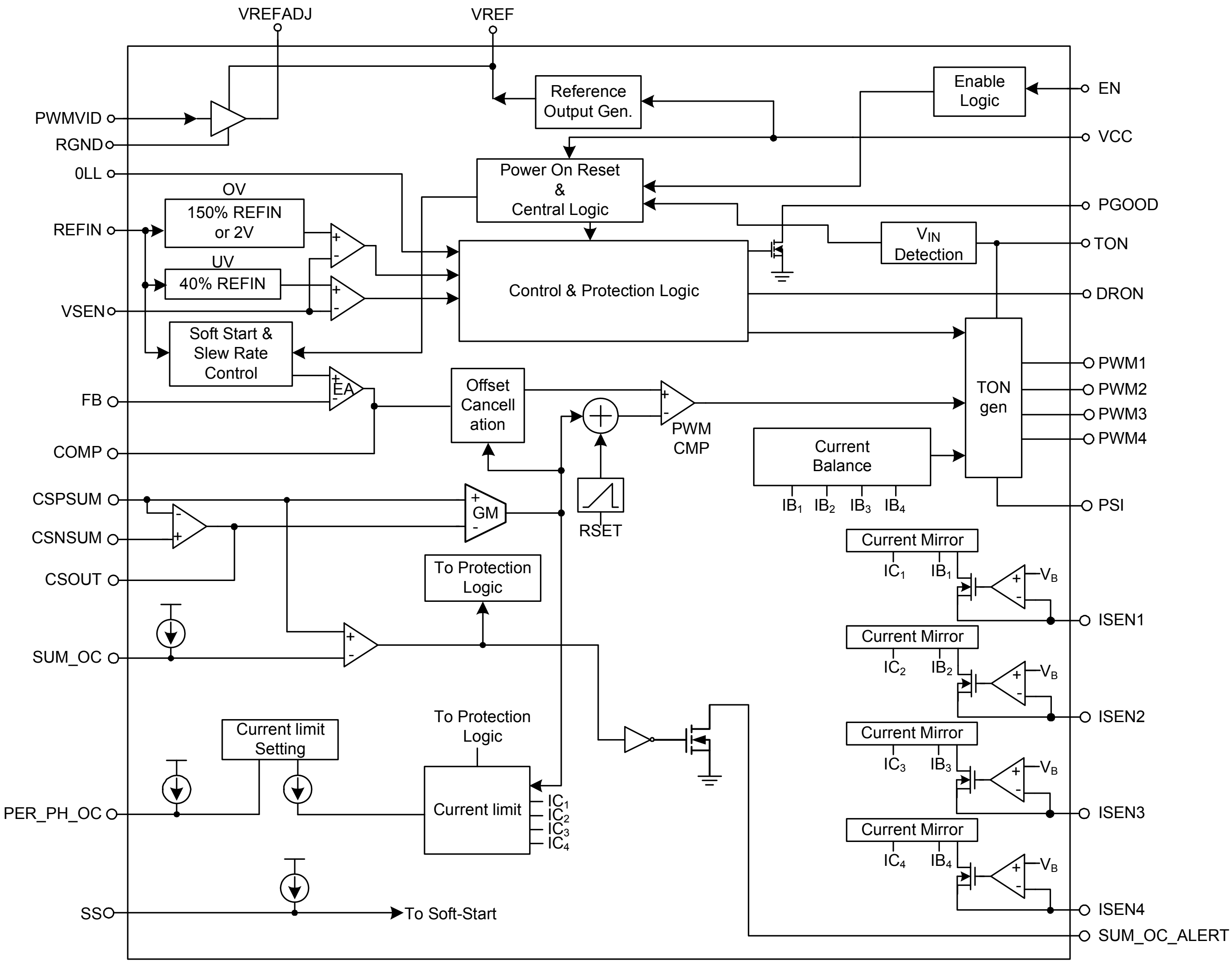
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	REFIN	External reference input.
2	VREF	Reference voltage output. This is a high precision voltage reference (2V) from the VREF pin to RGND pin.
3, 7,13, 14, 15, 16, 25, 28, 34, 35	NC	No internal connection.
4	SS	Soft-start time setting. Connect an external capacitor to adjust soft-start time. When the external capacitor is removed, the internal soft-start function will be chose.
5	PER_PH_OC	Per phase current limit setting. Connect a resistor from PER_PH_OC to GND to set the per phase current limit threshold.
6	SUM_OC_ALERT	Sum OC alert. Active high open drain output.
8	PWM4	PWM output for 4th phase.
9	PWM3	PWM output for 3rd phase.
10	PWM2	PWM output for 2nd phase.
11	PWM1	PWM output for 1st phase.
12	DRON	Bidirectional gate driver enable for external drivers.
20,19,18,17	ISEN[1:4]	Current sense inputs of phase1, 2, 3 and 4.
21	CSNSUM	Sum current sense negative pin.
22	CSPSUM	Sum current sense positive pin. Connect NTC network between this pin and CSOUT pin for thermal compensation. The CSPSUM to CSOUT pin differential voltage must be less than 450mV.
23	CSOUT	Sum current sense output pin. Connect NTC network between this pin and CSPSUM pin for thermal compensation. The CSPSUM to CSOUT pin differential voltage must be less than 450mV.

Pin No.	Pin Name	Pin Function
24	SUM_OC	SUM over current threshold setting. Connect a resistor from SUM_OC to CSOUT to set the sum current limit threshold. Any time, do “not” drive this pin voltage higher than V_{VCC} and do “not” leave this pin floating.
26	0LL	Zero load line enable input.
27	TON	On-time setting. An on-time setting resistor is connected from this pin to input voltage.
29	FB	Negative input of the error amplifier. This pin is output voltage feedback to controller.
30	COMP	This pin is the error amplifier output pin.
31	VSEN	Voltage sense input. This pin is connected to the terminal of output voltage.
32	RGND	Return ground. This pin is the negative node of the differential remote voltage sensing.
33	VCC	Supply voltage input. Connect this pin to a 5V bias supply. Place a high quality bypass capacitor from this pin to GND.
36	EN	Enable control input. Active high input. When VCC POR, the input voltage must not be over VCC.
37	PSI	Power saving interface. When the voltage is pulled below 0.4V, the device will operate into 1 phase DEM. When the voltage is between 0.8V to 1.2V, the device will operate into 1 phase force CCM. When the voltage is between 1.6V to 5.5V, the device will operate into 4 phase force CCM.
38	PGOOD	Power good indicator output. Active high open-drain output. A 150kΩ pull high resistor is needed.
39	PWMVID	Programming output voltage control input. Refer to PWM-VID Dynamic Voltage Control.
40	VREFADJ	Reference adjustment output. Refer to PWM-VID Dynamic Voltage Control.
41 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT8845A adopts G-NAVP^{TM} (Green-Native Adaptive Voltage Positioning), which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control. The load line can be easily programmed by setting the DC gain of the error amplifier. It also features best noise immunity, high output accuracy, and fast load transient response.

The G-NAVP^{TM} controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches COMP signal, the RT8845A generates an on-time width to achieve PWM modulation.

The RT8845A also features a PWM-VID dynamic voltage control circuit driven by the pulse width modulation method. This circuit reduces the device pin count and enables a wide dynamic voltage range.

VCC POR (Power on Reset)

Detecting the VCC voltage and issue POR signal as it exceeds than POR threshold (typical 4.1V). When VCC less than UVLO threshold (typical 3.8V), the control logic inhibits TON gen to deliver PWM signal.

Soft-Start and Slew Rate Control

An internal current source charges an external capacitor from SS pin to GND to build the soft-start ramp voltage. If the external capacitor is removed, an internal current source charges internal soft start capacitor to build the internal soft-start ramp. The output voltage will track the soft start ramp voltage during soft-start interval.

PGOOD

The power good output is an open-drain architecture. When the soft-start is finished, the PGOOD open-drain output will be high impedance.

TON GEN

Generate the PWM1 to PWM4 sequentially according to the phase control signal from the Control & Protection Logic. Pulse width is determined by current balance result and TON pin setting.

Current Balance

Each phase current sense signal is sent to the Current Balance circuit which adjusts the on-time of each phase to optimize current sharing.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

Current Limit

The current limit circuit employs a unique “valley” current sensing algorithm. If the magnitude of the current sense signal at ISENx is above the current limit threshold, the PWM is not allowed to initiate a new cycle. Thus, the current to the load exceeds average output inductor current, the output voltage falls and eventually crosses the under-voltage protection threshold, inducing IC shutdown.

Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The output voltage is continuously monitored through VSEN pin for over-voltage and under-voltage protection. When the output voltage exceeds OVP threshold, high-side MOSFET is turned off and low-side MOSFET is turned on. When output voltage is less than UVP threshold, under-voltage protection is triggered and then both high-side and low-side MOSFET are turned off. The controller is latched until VCC is re-supplied and exceeds the POR rising threshold voltage or EN is reset.

Absolute Maximum Ratings (Note 1)

- TON to GND -- −0.3V to 30V
- VCC to GND -- −0.3V to 6V
- RGND to GND --- −0.7V to 0.7V
- Other Pins -- −0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN−40L 5x5 -- 2.778W
- Package Thermal Resistance (Note 2)
  WQFN−40L 5x5, θ_{JA} -- 36°C/W
  WQFN−40L 5x5, θ_{JC} -- 6°C/W
- Junction Temperature -- 150°C
- Lead Temperature (Soldering, 10 sec.) --- 260°C
- Storage Temperature Range -- −65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) -- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} --- 7V to 24V
- Supply Voltage, V_{VCC} -- 4.5V to 5.5V
- Junction Temperature Range --- −40°C to 125°C
- Ambient Temperature Range --- −40°C to 85°C

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
VCC Supply Voltage	V_{VCC}		4.5	--	5.5	V
VCC Supply Current	I_{SUPPLY}	V_{EN} = 1.8V, 1Phase DEM mode, not switching, VREF external R = 40k	--	5	--	mA
VCC Shutdown Current	I_{SHDN}	EN = 0V	--	--	10	μA
VCC POR Threshold			3.8	4.1	4.4	V
POR Hysteresis			--	0.3	--	V
Error Amplifier						
DC Gain	A_{DC}	R_{LOAD} = 47kΩ	--	80	--	dB
Gain Bandwidth	G_{BW_EA}	C_{LOAD} = 5pF	--	5	--	MHz
Slew Rate	SREA	C_{LOAD} = 10pF (Gain = −4, R_F = 47kΩ, V_{OUT} = 0.5V to −3V)	5	--	--	V/μs
Output Voltage Range	V_{COMP}	R_{LOAD} = 47kΩ	0.5		3.6	V
Max Source/Sink Current	I_{O_EA}	V_{COMP} = 2V	--	5	--	mA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Load Line Current Gain Amplifier							
Input Offset Voltage		V_{ILOFS}	V_{CSPSUM} = 1V	–5	0	5	mV
Current Gain		AILGAIN	$V_{CSPSUM} – V_{CSOUT}$ = 0.4V $V_{FB} = V_{COMP}$ = 1V	--	1	--	A/A
CSSA Amplifier							
Input Offset Voltage		V_{CSSA_OFS}		–1.5	--	1.5	mV
DC Gain		A_{DC}		70	--	--	MΩ
Gain-Bandwidth Product		G_{BW}	C_{LOAD} = 5pF	4	5	--	MHz
Output Voltage Range		V_{CSOUT}	R_{LOAD} = 47kΩ	0.5	--	3.6	V
Maximum Source Current		I_{CSSA_SRC}		--	2	--	mA
Maximum Sink Current		I_{CSSA_SNK}		--	3	--	mA
TON Setting							
TON Pin Voltage		V_{TON}	I_{TON} = 26.8μA, V_{REFIN} = 1V	0.9	1	1.1	V
On-Time Setting		t_{ON}	I_{RTON} = 26.8μA, V_{REFIN} = 1V	189	210	231	ns
Input Current Range		I_{TON}	V_{REFIN} = 1V	6	--	70	μA
Minimum Off-Time		t_{OFF_MIN}	V_{REFIN} = 1V	--	300	--	ns
EN Input Voltage							
1.8V GPIO EN Input Voltage	Logic-High	V_{EN_H}		1.2		5.5	V
	Logic-Low	V_{EN_L}				0.55	V
0LL Input Voltage							
0LL Input Voltage	Logic-High	V_{0LL_H}		1.2		5.5	V
	Logic-Low	V_{0LL_L}				0.55	V
PSI Input Voltage							
4 Phase CCM Input voltage				1.6	1.8	5.5	V
1 Phase CCM Input voltage				0.8	1	1.2	V
1 Phase DEM Input voltage				--	--	0.4	V
VID Input Voltage							
1.8V GPIO VID Input Voltage	Logic-High	V_{VID_H}		1.2	--	--	V
	Logic-Low	V_{VID_L}		--	--	0.6	V
Protection Function							
Relative Over-Voltage Protection Threshold			$V_{REFIN} \geqq$ 1.33V	145	150	155	%
Absolute Over-Voltage Protection Threshold			$V_{REFIN} \leqq$ 1.33V	1.9	2	2.1	V
OV Fault Delay			FB forced above OV threshold		5		μs
Relative Under-Voltage Protection Threshold		V_{UVP}		35	40	45	%
Under-Voltage Fault Delay			FB forced above UV threshold		3		μs
Thermal Shutdown Threshold		T_{SD}			150		°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Soft-Start (PGOOD Blanking Time)		From EN = high to VOUT regulation point, V_{REFIN} = 1V	--	1000	--	μs
Over-Current Protection						
Per PHASE Current Limit Setting Current	$I_{PER\_PH\_OC}$		9	10	11	μA
Current Limit Setting Current Temperature Coefficient				4700		ppm/°C
Per PHASE Current Limit Threshold		R_{OCSET} = 100k, V_{ISENX} = 40mV	--	60	--	mV
SUM_OC Threshold Setting Current	I_{SUM_OC}		9	10	11	μA
SUM_OC Threshold		V_{SUM_OC} - V_{CSPSUM}	--	0	--	mV
Reference Voltage						
Reference Voltage	V_{REF}	Sourcing current = 1mA, VID no switching	1.98	2	2.02	V
PWM Driving Capability						
PWM Source Resistance	R_{PWM_SRC}			30		Ω
PWM Sink Resistance	R_{PWM_SNK}			10		Ω
PWM Tri-state Voltage	V_{PWM_Tri}	V_{CC} = 5V (Note 6)	1.6	1.95	2.2	V

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Not production tested. Test condition is V_{IN} = 8V, V_{OUT} = 1V, I_{OUT} = 20A using application circuit.

Note 6. Pull PWM to HIZ voltage 200ns when PWM enter HIZ.

Typical Application Circuit

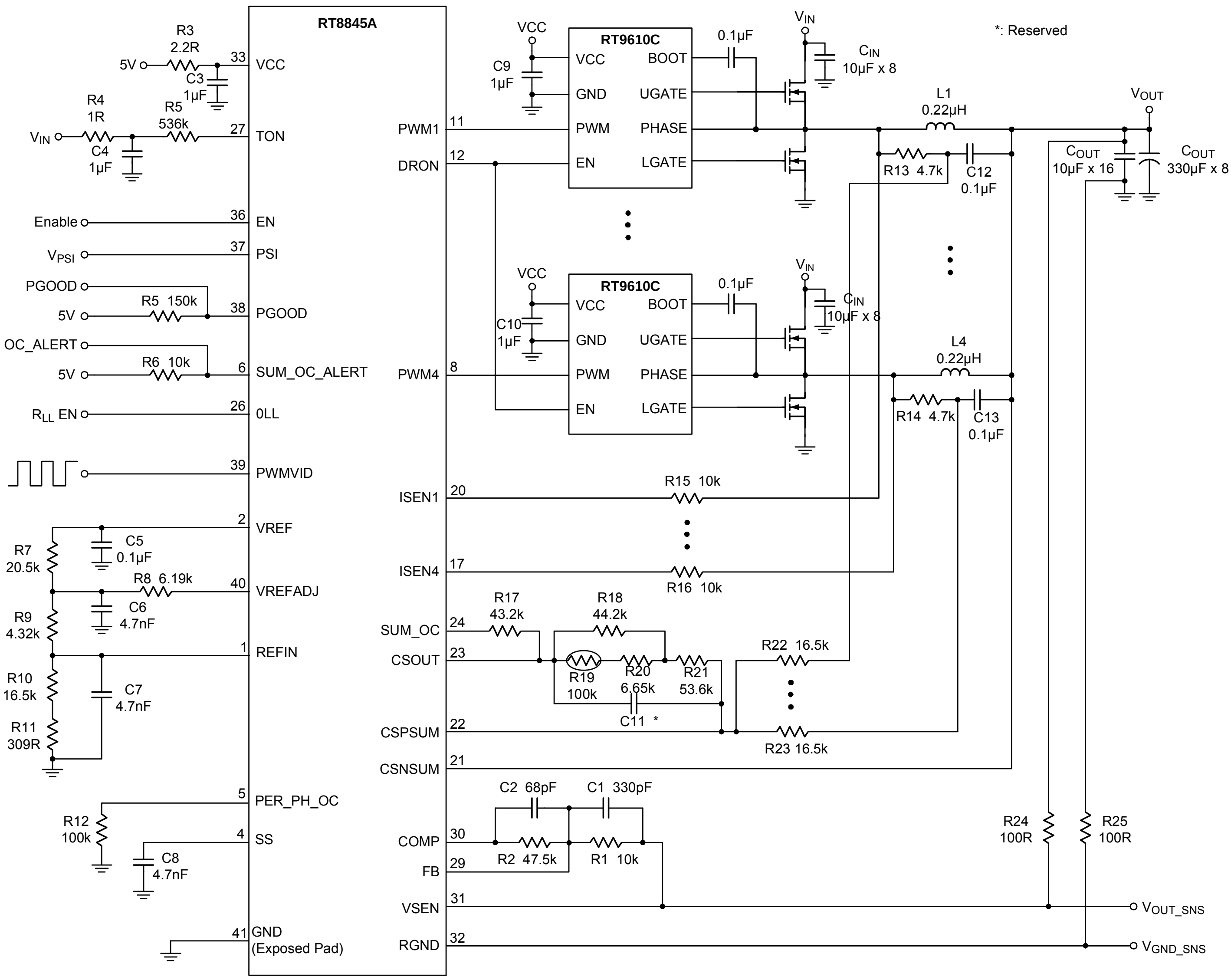


Figure 1. 4 Active Phase Configuration

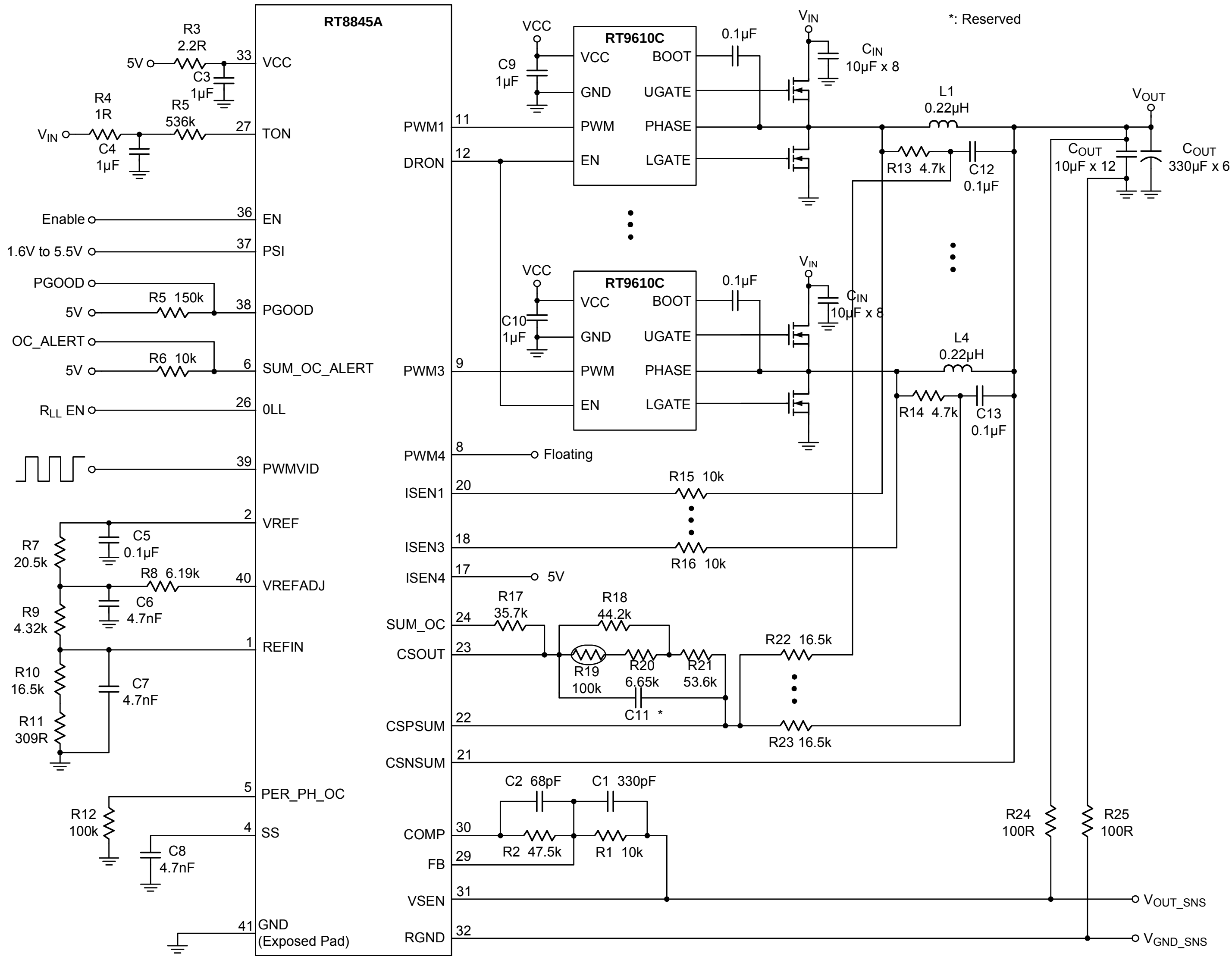


Figure 2. 3 Active Phase Configuration

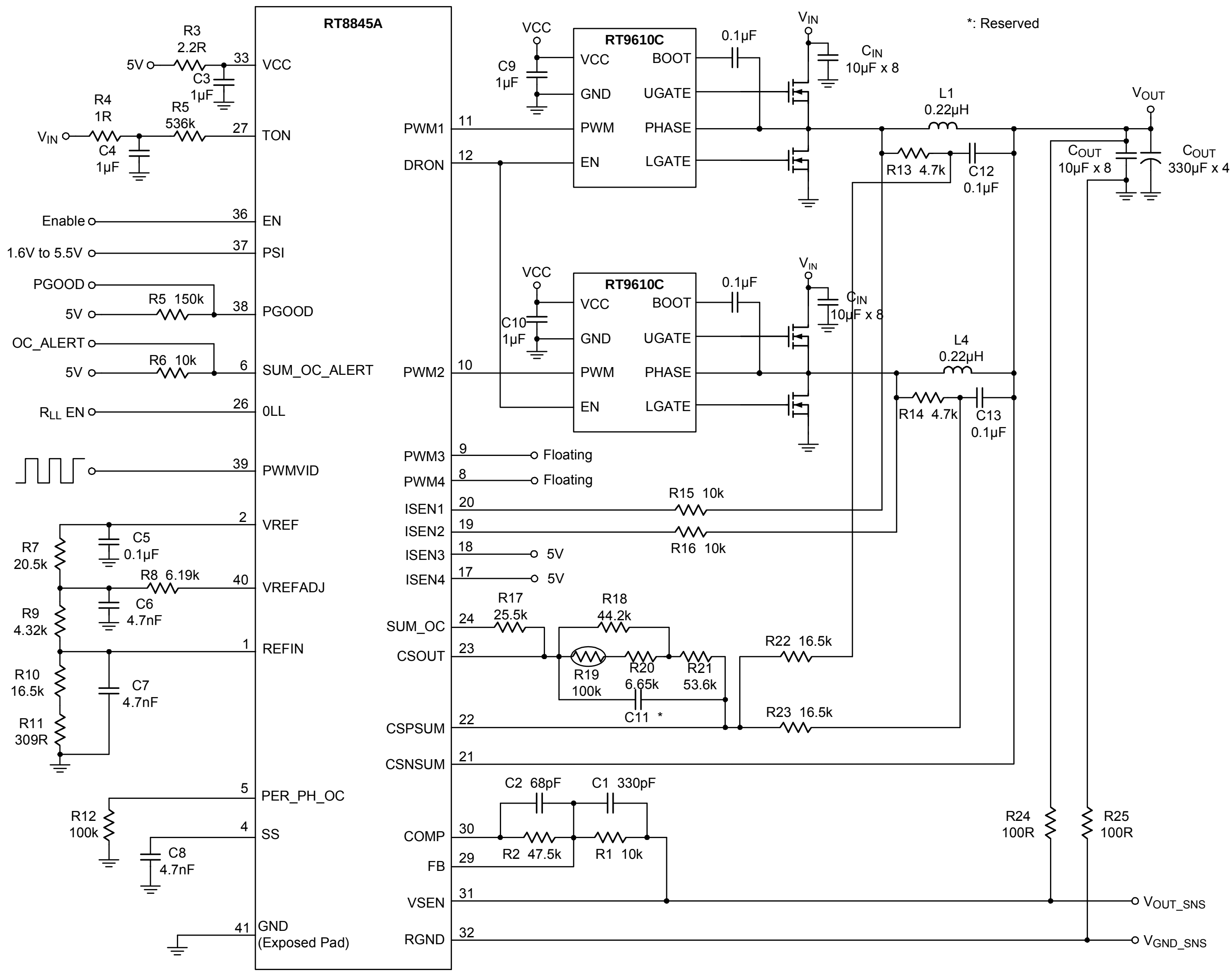
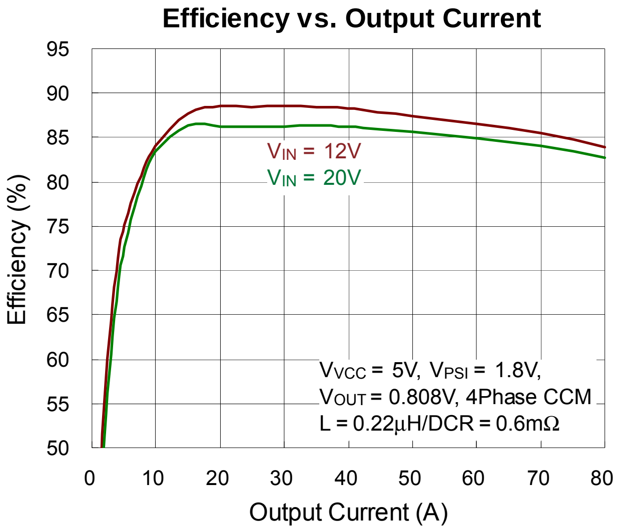
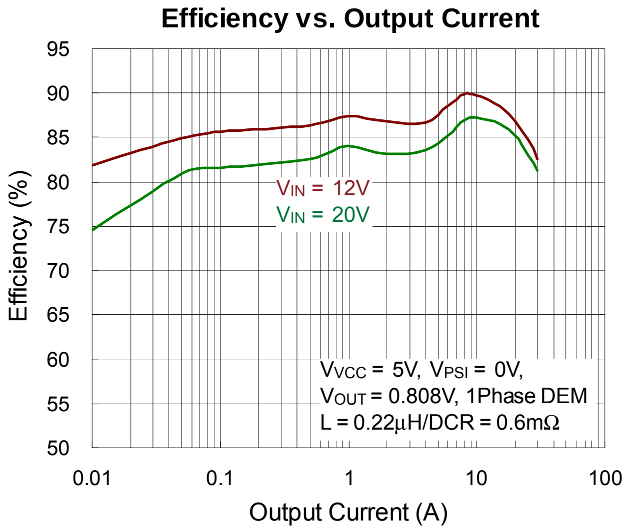
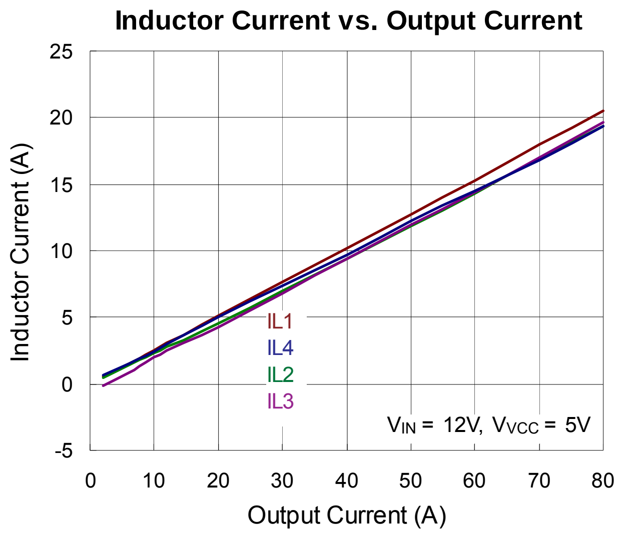


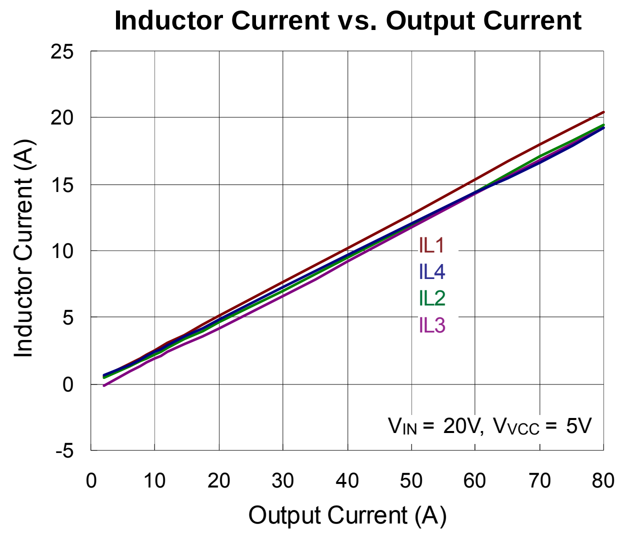
Figure 3. 2 Active Phase Configuration

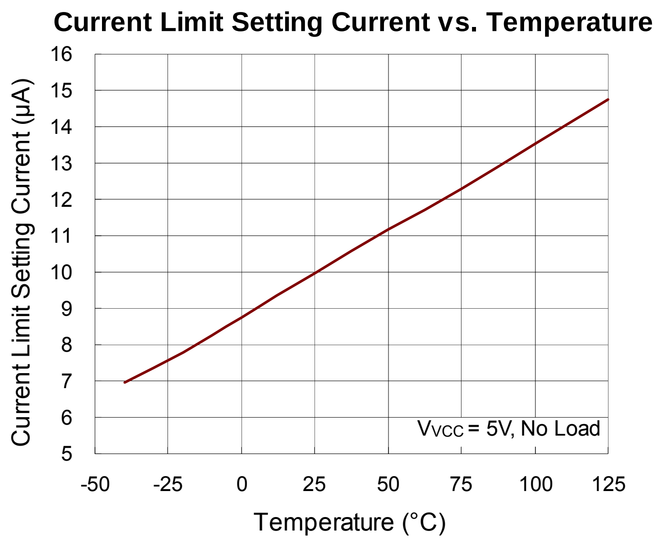
Typical Operating Characteristics

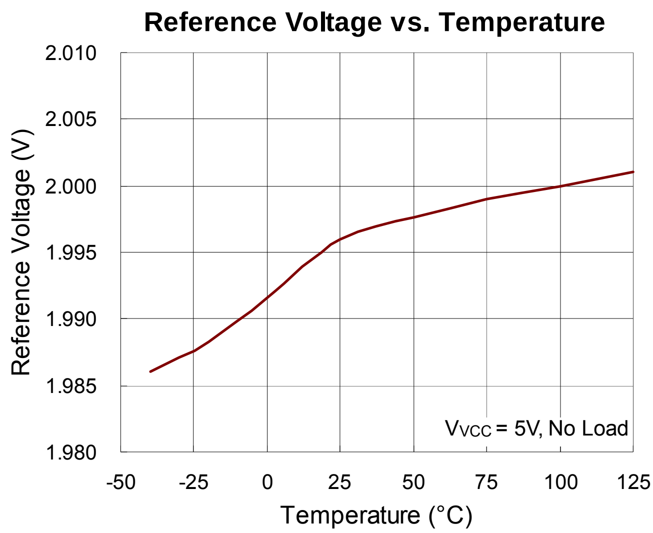




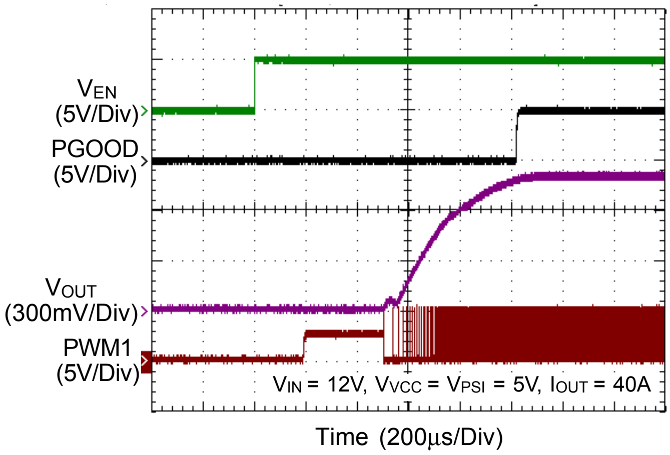




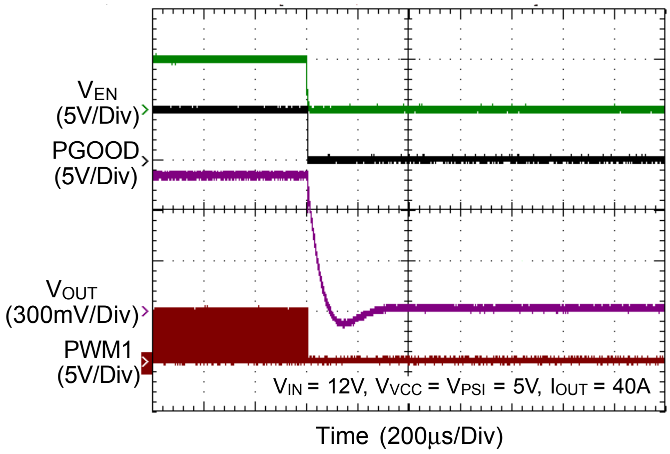




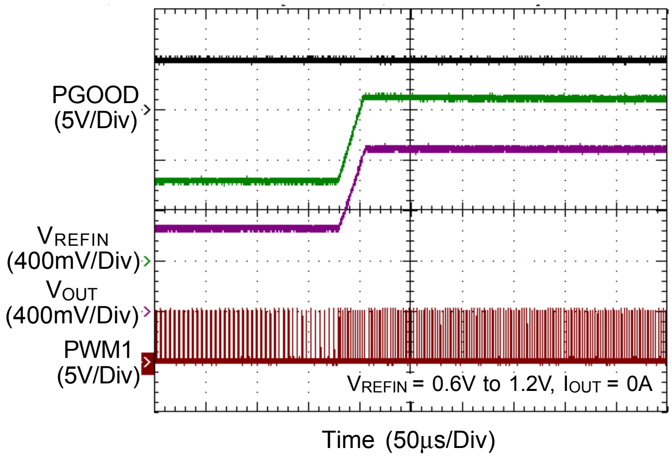
Power On from EN



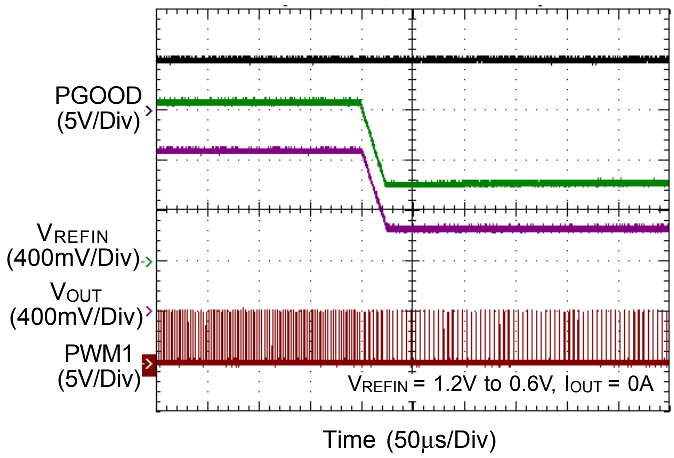
Power Off from EN



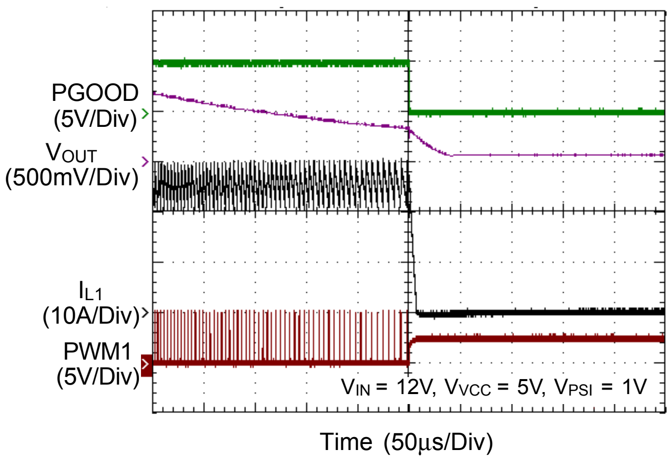
Dynamic Output Voltage Control



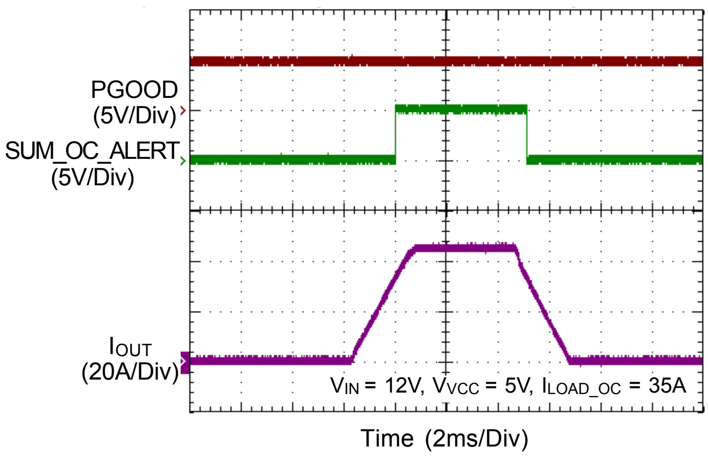
Dynamic Output Voltage Control



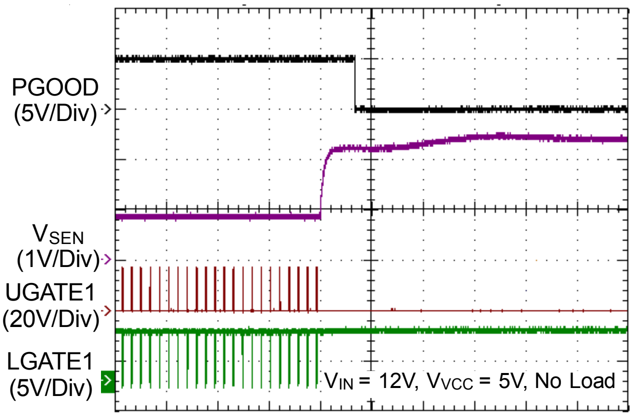
Per Phase Current Limit and UVP



Sum Over Current Alert

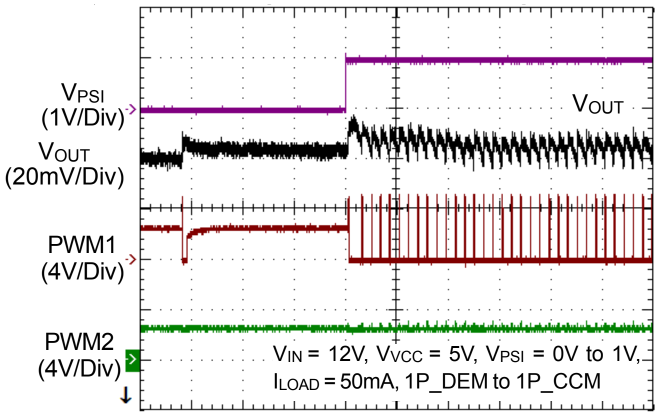


OVP



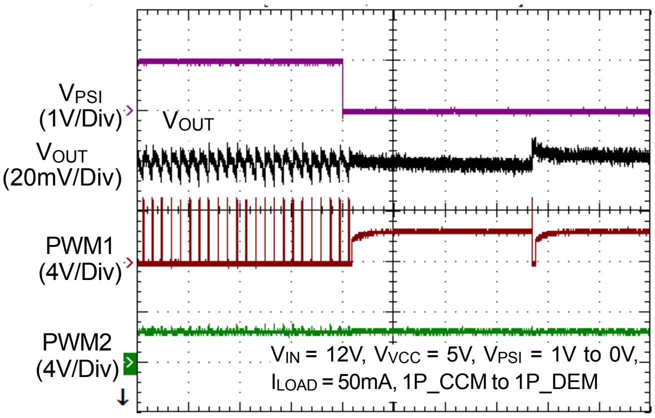
Time (20μs/Div)

Mode Transition



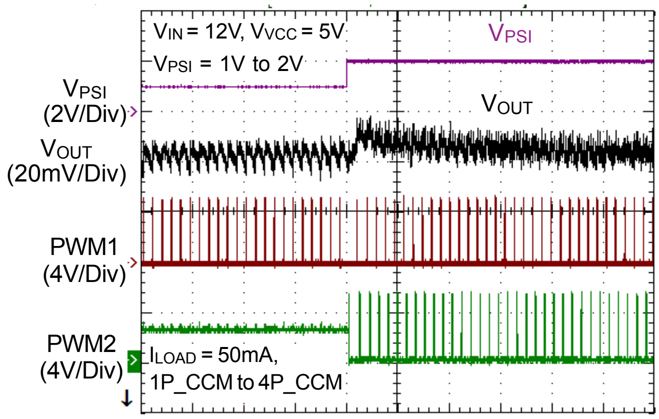
Time (20μs/Div)

Mode Transition



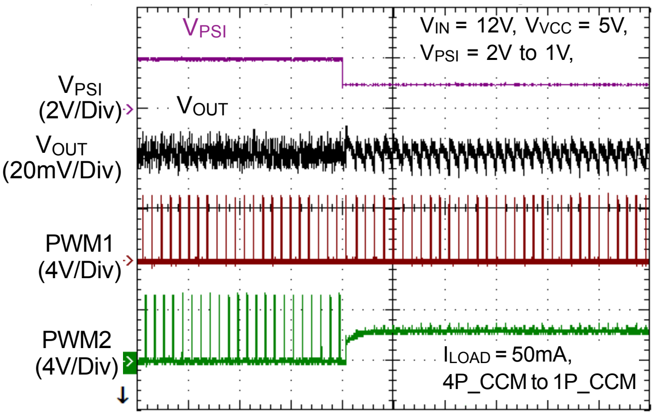
Time (20μs/Div)

Mode Transition



Time (20μs/Div)

Mode Transition



Time (20μs/Div)

Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The RT8845A is a four-phase synchronous Buck PWM

Controller which is optimized for high-performance graphic microprocessor and computer applications.

The RT8845A adopts G-NAVP^{TM} (Green-Native Adaptive Voltage Positioning), which is Richtek's proprietary topology derived from finite DC gain compensator with current mode control. The load line can be easily programmed by setting the DC gain of the error amplifier. It also features best noise immunity, high output accuracy, and fast load transient response.

The RT8845A provides the PWMVID control operation. By entering a PWM signal to the PWMVID pin, the controller can convert the external reference voltage. The feedback voltage will accurately track the external reference voltage. Therefore, the dynamic output voltage can be adjusted by changing the PWM signal.

The RT8845A also integrates complete fault protection functions including over voltage, under voltage, current limit and thermal shutdown.

Power On Reset (POR), UVLO

Power On Reset (POR) occurs when V_{VCC} rises above to approximately 4.1V (typical), the RT8845A will reset the fault latch circuit and prepare for PWM operation. When the V_{VCC} is lower than 3.8V (typical), the Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping PWMx signal low.

Enable and Disable

The EN pin is a high impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8845A remains in shutdown if the EN pin is lower than 550mV. When the EN voltage rises above the 1.2V high level threshold, the RT8845A will begin a new initialization and soft-start cycle.

Soft-Start

The RT8845A provides internal soft-start function and external soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered up. The soft-start function automatically begins once the chip is enabled. There is a delay time around 400µs from EN goes high to V_{OUT} begins to ramp-up.

If external capacitor from SS pin to GND is removed, the internal soft-start function will be chosen. An internal current source charges the internal soft-start capacitor so that the internal soft-start voltage ramps up linearly. The output voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft-start voltage exceeds the REFIN voltage, the output voltage no longer tracks the internal soft-start voltage but follows the REFIN voltage. Therefore, the duty cycle of the PWM signal as well as the input current at power up are limited.

The soft-start process is finished until the internal SSOK go high and protection is not triggered. Figure 4 shows the internal soft-start sequence.

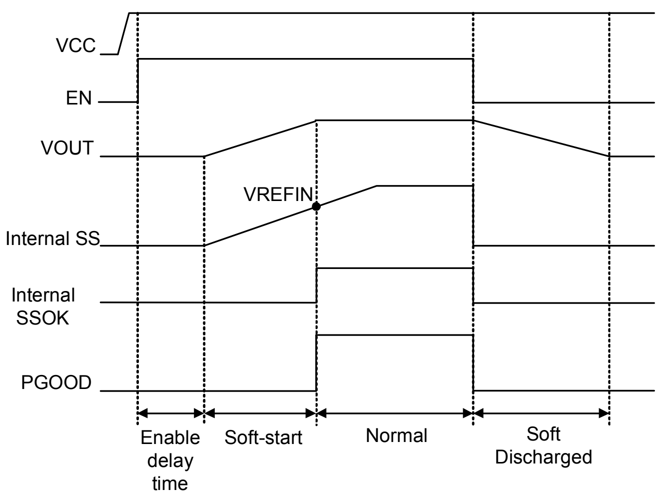


Figure 4. Internal Soft-Start Sequence

The RT8845A also provides a proximate external soft-start function, and the external soft-start sequence is shown in Figure 5, an additional capacitor can be connected from SS pin to GND. The external capacitor will be charged by internal current source to build soft-start voltage ramp. If external soft-start function is chosen, the external soft-start time should be set longer than internal soft-start time to avoid output voltage tracking the internal soft-start ramp, the external soft-start time setting is shown in Figure 6, the recommend external soft-start slew rate is 0.1V/ms to 0.4V/ms.

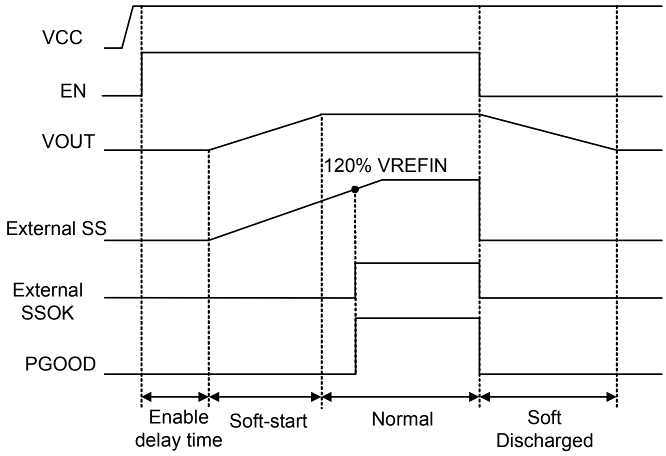


Figure 5. External Soft-Start Sequence

The soft-start time can be calculated as :

$$t_{SS} = \frac{V_{REFIN} \times C_{SS}}{I_{SS}}$$

where I_{SS} = 4μA (typ.), V_{REFIN} is the voltage of REFIN pin, and C_{SS} is the external capacitor placed from SS pin to GND.

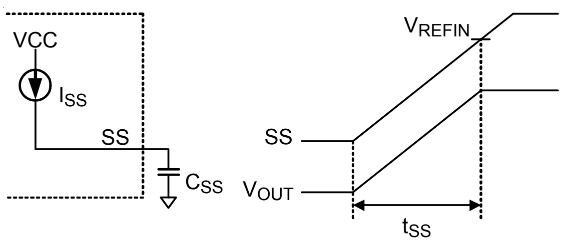


Figure 6. External Soft-Start Time Setting

Power Good Output (PGOOD)

The PGOOD pin is an open-drain output, and it requires a 150kΩ pull-up resistor. During soft-start, the PGOOD is held low and is allowed to be pulled high after V_{OUT} achieved over UVP threshold and under OVP threshold. In additional, if any protection is triggered during operation, the PGOOD will be pulled low immediately.

Active Phase Circuit Setting

The RT8845A can operate into 4 phases with force CCM, 1 phase with force CCM, and 1 phase with DEM according to PSI voltage setting. If PSI voltage is pulled below 0.4V, the controller will operate into 1 phase with DEM. In DEM operation, the RT8845A automatically reduces the operation frequency at light load conditions for saving power loss. If PSI voltage is pulled between 0.8V to 1.2V, the controller will switch operation into 1 phase with force CCM. If PSI voltage is pulled between 1.6V to 5.5V, the controller will switch operation into 4 phase with force CCM. The operation mode is summarized in Table 1.

Moreover, the PSI pin is valid after POR of VR.

Table 1.

Operation Phase	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.8V to 1.2V
4phase with CCM	1.6V to 5.5V

Switching Frequency Setting

Connecting a resistor R_{TON} between input terminal and TON pin to set the on-time width.

$$T_{ON} = \frac{R_{TON} \times 4.73p \times 1.2}{V_{IN} - V_{REFIN}} \quad (V_{REFIN} < 1.2)$$

$$T_{ON} = \frac{R_{TON} \times 4.73p \times V_{REFIN}}{V_{IN} - V_{REFIN}} \quad (V_{REFIN} \geq 1.2)$$

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$f_{SW(MAX)} = \frac{V_{REFIN} + \frac{IccTDC}{N} \cdot \left(DCR + \frac{R_{ON\_LS,max}}{n_{LS}} - N \cdot R_{LL} \right)}{\left[V_{IN(MAX)} + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON\_LS,max}}{n_{LS}} - \frac{R_{ON\_HS,max}}{n_{LS}} \right) \right] \cdot \left(T_{ON} - T_D + T_{ON,VAR} \right) + \frac{IccTDC}{N} \cdot \left(\frac{R_{ON\_LS,max}}{n_{LS}} \right) \cdot T_D}$$

Where $f_{SW(MAX)}$ is the maximum switching frequency, V_{REFIN} is the reference input voltage, $V_{IN(MAX)}$ is the maximum application input voltage, I_{CC}TDC is the thermal design current of application, N is the phase number. The $R_{ON\_HS,max}$ is the maximum equivalent high-side R_{DS_ON}, and n_{HS} is the number of high-side MOSFETs; $R_{ON\_LS,max}$ is the maximum equivalent low-side R_{DS_ON}, and n_{LS} is the number of low-side MOSFETs. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting.

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

PWM VID and Dynamic Output Voltage Control

The RT8845A features a PWM VID input for dynamic output voltage control as shown in Figure 7, which reduces the number of device pin and enables a wide dynamic voltage range. The output voltage is determined by the applied voltage on the REFIN pin. The PWM duty cycle determines the variable output voltage at REFIN.

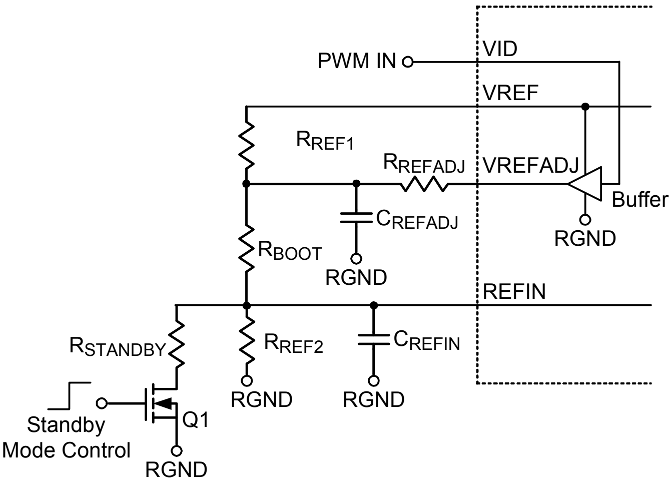


Figure 7. PWM VID Analog Circuit Diagram

With the external circuit and VID control signal, the controller provides three operation modes shown as Figure 8.

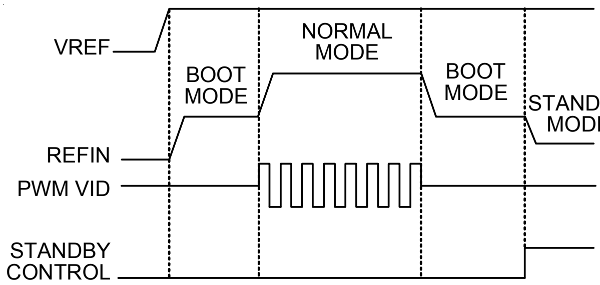


Figure 8. PWM VID Time Diagram

BOOT Mode

VID is not driven, and the buffer output is tri-state. At this time, turn off the switch Q1 and connect a resistor divider as shown in Figure 7 that can set the REFIN voltage to be V_{BOOT} as the following equation :

$$V_{BOOT} = V_{VREF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

where V_{VREF} = 2V (typ.)

Choose R_{REF2} to be approximately 10kΩ, and the R_{REF1} and R_{BOOT} can be calculated by the following equations :

$$R_{REF1} + R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}}$$

$$R_{REF1} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{BOOT}$$

$$R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{REF1}$$

Standby Mode

An external control can provide a very low voltage to meet V_{OUT} operating in standby mode. If the VID pin is floating and switch Q1 is enabled as shown in Figure 7, the REFIN pin can be set for standby voltage according to the calculation below :

$$V_{STANDBY} = V_{VREF} \times \frac{R_{REF2} \,//\, R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} \,//\, R_{STANDBY})}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the $R_{STANDBY}$ can be calculated by the following equation :

$$R_{STANDBY} = \frac{R_{REF2} \times (R_{REF1} + R_{BOOT}) \times V_{STANDBY}}{R_{REF2} \times V_{REF} - V_{STANDBY} \times (R_{REF1} + R_{REF2} + R_{BOOT})} - R_{REF1}$$

Normal Mode

If the VID pin is driven by a PWM signal and switch Q1 is disabled as shown in Figure 7, the V_{REFIN} can be adjusted from V_{min} to V_{max} , where V_{min} is the voltage at zero percent PWM duty cycle and V_{max} is the voltage at one hundred percent PWM duty cycle. The V_{min} and V_{max} can be set by the following equations :

$$V_{min} = V_{VREF} \times \frac{R_{REF2}}{R_{REF2} + R_{BOOT}} \times \frac{R_{REFADJ} \,//\, (R_{BOOT} + R_{REF2})}{R_{REF1} + [R_{REFADJ} \,//\, (R_{BOOT} + R_{REF2})]}$$

$$V_{max} = V_{VREF} \times \frac{R_{REF2}}{(R_{REF1} \,//\, R_{REFADJ}) + R_{BOOT} + R_{REF2}}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the R_{REFADJ} can be calculated by the following equation :

$$R_{REFADJ} = \frac{R_{REF1} \times V_{min}}{V_{max} - V_{min}}$$

The relationship between VID duty and V_{REFIN} is shown in Figure 9, and V_{OUT} can be set according to the calculation below :

$$V_{OUT} = V_{min} + N \times V_{STEP}$$

where V_{STEP} is the resolution of each voltage step1 :

$$V_{STEP} = \frac{(V_{max} - V_{min})}{N_{max}}$$

where N_{max} is the number of total available voltage steps and N is the number of step at a specific V_{OUT} . The dynamic voltage VID period (T_{vid} = T_u x N_{max}) is determined by the unit pulse width (T_u) and the available step number (N_{max}). The recommended T_u is 27ns.

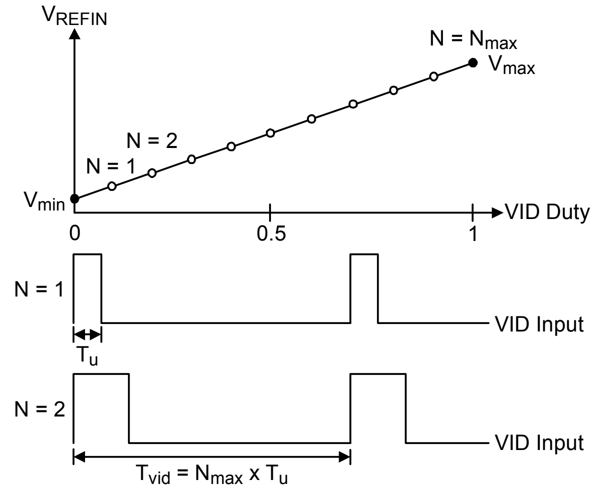


Figure 9. PWM VID Analog Output

VID Slew Rate Control

In the RT8845A, the V_{REFIN} slew rate is proportional to PWM VID duty, the rising time and falling time are the same. In normal mode, the V_{REFIN} slew rate SR can be estimated by C_{REFADJ} or C_{REFIN} as the following equation :

When choose C_{REFADJ} :

$$SR = \frac{(V_{REFIN\_Final} - V_{REFIN\_initial}) \times 80\%}{2.2 R_{SR} C_{REFADJ}}$$

$$R_{SR} = [(R_{REF1} \,//\, R_{REFADJ})] \,//\, (R_{BOOT} + R_{REF2})$$

When choose C_{REFIN} :

$$SR = \frac{(V_{REFIN\_Final} - V_{REFIN\_initial}) \times 80\%}{2.2 R_{SR} C_{REFIN}}$$

$$R_{SR} = [(R_{REF1} \,//\, R_{REFADJ}) + R_{BOOT}] \,//\, R_{REF2}$$

The recommend SR is estimated by C_{REFADJ}.

Remote Sense

The RT8845A uses the remote sense path (VSEN and RGND) to overcome voltage drops in the power lines by sensing the voltage directly at the end of GPU. Normally, to protect remote sense path disconnecting, there are two resistors (R_{Local}) connecting between local sense path and remote sense path. That is, in application with remote sense, the R_{Local} is recommended to be 10Ω to 100Ω. If no need of remote sense, the R_{Local} is recommended to be 0Ω.

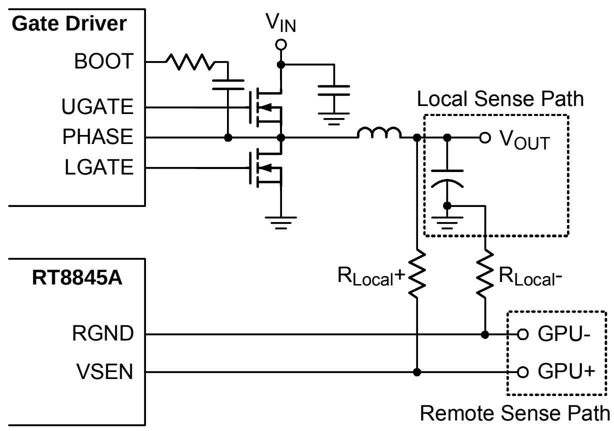


Figure 10. Output Voltage Sensing

Sum Current Sensing

The RT8845A adopts the sum current sensing topology to sense total inductor current as shown in Figure 11. The sum current signal then is used to generate load line, and sum over current protection. The sum current sensing circuitry uses an op amp as an adder to sum the DCR sensing capacitor voltages. The total inductor current can be obtained by sensing the V_{SUM} voltage. This current sense topology needs only three pins to sense the total inductor current, which greatly reduces the number of pins. To design the current sensing circuit, the DCR sensing parameter must be obtained first. To set a given C_X, the design is to first obtain R_X and R_S according to the following equation :

$$\frac{L_X}{DCR} = \left(\frac{R_X \times R_S}{R_X + R_S}\right) \times C_X$$

And the current sensing voltage (V_{SUM}) can be obtained by below equation :

$$V_{SUM} = \left(\frac{R_{SUM}}{R_X + R_S}\right) \times DCR \times I_{LOAD}$$

The resistance ratio between R_{SUM} and (R_X + R_S) should be set as 4 for the phase margin of sum current sensing OPA consideration.

Make sure that the maximum value of V_{SUM} must be less than 450mV.

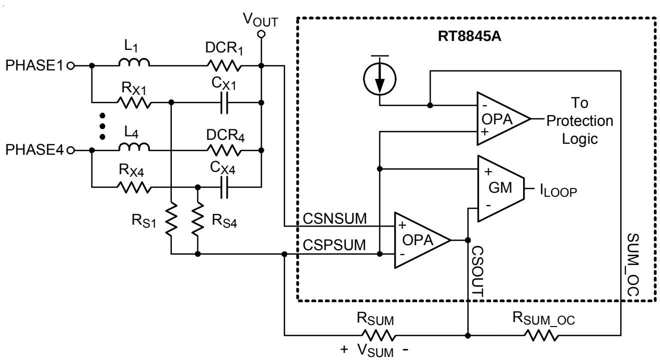


Figure 11. Sum Current Sensing Circuit

Thermal Compensation Network for Sum Current Sensing Architecture

Since the copper wire of inductor has a positive temperature coefficient, the DCR value will be affected by the temperature. In consideration of DCLL and current reporting accuracy, a resistor network with NTC thermistor compensation connecting between the CSPSUM and CSOUT pins is necessary to compensate the positive temperature coefficient of inductor DCR. Figure 12 shows the thermal compensation network for sum current sensing architecture. Using the following equations, the thermal compensation network R_{SUM_S1}, R_{SUM_S2} and R_{SUM_P} can be calculated.

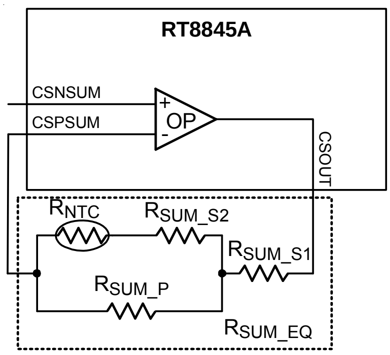


Figure 12. Thermal Compensation Network for Sum Current Sensing Architecture

Define the system temperature T_L, T_R and T_H, and implement the thermal compensation described as

$$DCR(T_L) \times \frac{R_{SUM\_EQ}(T_L)}{R_X + R_S} = \frac{R_{SUM\_EQ}(T_R)}{R_X + R_S} \times DCR(25°C)$$

$$DCR(T_R) \times \frac{R_{SUM\_EQ}(T_R)}{R_X + R_S} = \frac{R_{SUM\_EQ}(T_R)}{R_X + R_S} \times DCR(25°C)$$

$$DCR(T_H) \times \frac{R_{SUM\_EQ}(T_H)}{R_X + R_S} = \frac{R_{SUM\_EQ}(T_R)}{R_X + R_S} \times DCR(25°C)$$

The relationship between DCR and temperature is as follows :

$$DCR(T) = DCR(25°C) \times [1 + 0.00393 \times (T - 25)]$$

$R_{SUM\_EQ}(T)$ is the equivalent resistor of the thermal compensation resistor network with a NTC thermistor.

$$R_{SUM\_EQ}(T) = R_{SUM\_S1} + \{R_{SUM\_P} // [R_{SUM\_S2} + R_{NTC}(T)]\}$$

The relationship between NTC and temperature is as follows, where β is varied with different NTC thermistor.

$$R_{NTC}(T) = R_{NTC}(25°C) \times e^{\beta\left(\frac{1}{T+273} - \frac{1}{298}\right)}$$

With above equation, three equations and three unknowns, R_{SUM_S1}, R_{SUM_S2} and R_{SUM_P} can be found out unique solution.

$$R_{SUM\_P} = \sqrt{\alpha 2 \times [kR + R_{NTC}(T_R)] \times [kR + R_{NTC}(T_H)]}$$

$$R_{SUM\_S2} = kR - R_{SUM\_P}$$

$$R_{SUM\_S1} = R_{SUM\_EQ}(T_R) - \frac{R_{SUM\_P} \times [R_{SUM\_S2} + R_{NTC}(T_R)]}{R_{SUM\_P} + R_{SUM\_S2} + R_{NTC}(T_R)}$$

$$\alpha 1 = \frac{R_{SUM\_EQ}(T_L) - R_{SUM\_EQ}(T_R)}{R_{NTC}(T_L) - R_{NTC}(T_R)}$$

$$\alpha 2 = \frac{R_{SUM\_EQ}(T_R) - R_{SUM\_EQ}(T_H)}{R_{NTC}(T_R) - R_{NTC}(T_H)}$$

$$kR = \frac{\frac{\alpha 2}{\alpha 1} \times R_{NTC}(T_H) - R_{NTC}(T_L)}{1 - \frac{\alpha 2}{\alpha 1}}$$

Sum Over Current Alert

The RT8845A provides sum over current alert function. System can get over load information through by SUM_OC_ALERT pin pulled high. Connecting a resistor (R_{SUM_OC}) from SUM_OC pin to CSOUT pin to set the sum over current threshold. When the voltage across R_{SUM} (V_{SUM}) is greater than the setting threshold, the SUM_OC_ALERT pin will indicate "high". The sum over current threshold can be obtained according to bellow equation :

$$R_{SUM\_OC} = \frac{V_{SUM}}{I_{SUM\_OC}} = \frac{R_{SUM}}{R_X + R_S} \times \frac{DCR}{10\mu} \times I_{LOAD\_OC}$$

Where the I_{LOAD_OC} is the desired sum over current threshold.

Loop Control

The RT8845A adopts Richtek's proprietary G-NAVP™ topology. G-NAVP™ is based on the finite-gain peak current mode with CCRCOT (Constant Current Ripple Constant On Time; CCRCOT) topology. The control loop consists of PWM modulators with power stages, current sense amplifiers and an error amplifier as shown in Figure 13.

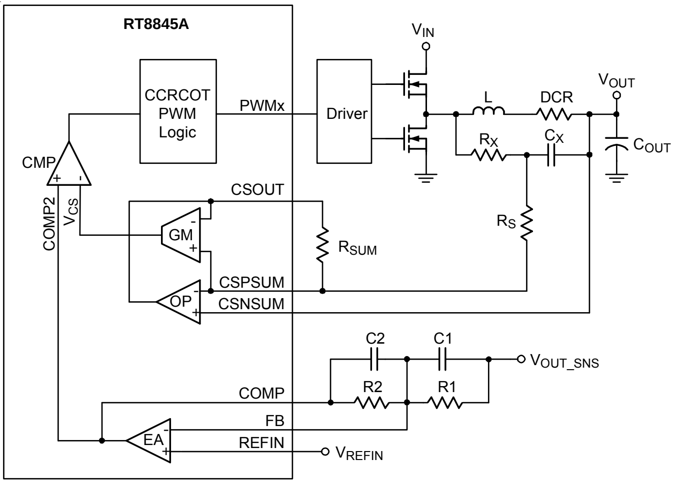


Figure 13. Simplified Schematic for Droop and Remote Sense in CCM

Similar to the peak current mode control with finite compensator gain, the HS_FET on-time is determined by the CCRCOT ON-Time generator. When the load current increases, V_{CS} increases, the steady state COMP voltage also increases and V_{OUT} decreases, achieving Active Voltage Positioning (AVP). The RT8845A internally cancels the inherent output offset of the finite gain peak current mode controller.

Droop Setting

The G-NAVP™ topology can set load-line (droop) via the current loop and the voltage loop, the load-line is a slope between load current and output voltage. Once the load-line is enabled, the output voltage will become as the following equation :

$$V_{OUT} = V_{REFIN} - I_{LOAD} \times R_{LL}$$

The load-line is obtained by the following equation :

$$R_{LL} = \frac{R_{SUM} \times DCR}{R_X + R_S} \times \frac{R1}{R2}$$

The load-line can be disabled by pulled high 0LL pin voltage.

Loop Compensation

Optimized compensation of the RT8845A allows for best possible load step response of the regulator's output. A type-I compensator with a single pole and single zero is adequate for a proper compensation. Figure 13 shows the compensation circuit. Prior design procedure shows how to determine the resistive feedback components of the error amplifier gain, C1 and C2 must be calculated for the compensation. The target is to achieve the constant resistive output impedance over the widest possible frequency range. The pole frequency, f_P, of the compensator must be set to compensate the output capacitor ESR zero :

$$f_P = \frac{1}{2\pi \times R_C \times C}$$

where C is the capacitance of the output capacitor, and R_C is the ESR of output capacitor. C2 can be calculated as follows :

$$C2 = \frac{R_C \times C}{R2}$$

The zero of compensator has to be placed at half of the switching frequency to filter the switching related noise, such that,

$$C1 = \frac{1}{R1 \times \pi \times f_S}$$

Current Balance

The RT8845A senses per phase current signal through ISENx pins and compares it with the average current. If the sensed current of any particular phase is higher than average current, the on-time of this phase will be adjusted to be shorter.

The current balance accuracy is major related with on-resistance of low-side MOSFET (R_{LG,DS_ON}). That is, in practical application, using lower R_{LG,DS_ON} will reduce the current balance accuracy.

Per Phase Current Limit Setting

The RT8845A incorporates per phase current limit mechanism to prevent over current event. The per phase current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at ISENx is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The per phase current limit threshold can be set by a resistor ($R_{PER\_PH\_OC}$) between PER_PH_OC pin and GND. Once VCC exceeds the POR threshold and chip is enabled, an internal current source $I_{PER\_PH\_OC}$ flows through $R_{PER\_PH\_OC}$. The voltage across $R_{PER\_PH\_OC}$ is stored as the per phase current limit protection threshold $V_{PER\_PH\_OC}$. The threshold range of $V_{PER\_PH\_OC}$ is 10mV to 300mV. $R_{PER\_PH\_OC}$ can be calculated according to the following equation :

$$V_{PER\_PH\_OC} = I_{L\_VALLEY} \times R_{DS\_ON}$$

$$R_{PER\_PH\_OC} = \frac{(I_{L\_VALLEY} \times R_{DS\_ON}) + 40mV}{I_{PER\_PH\_OC}} \times 10$$

where I_{L_VALLEY} represents the desired pre-phase inductor limit current (valley inductor current) and $I_{PER\_PH\_OC}$ is current limit setting current which has a temperature coefficient to compensate the temperature dependency of the R_{DS_ON}.

If $R_{PER\_PH\_OC}$ is not present, there is no current path for $I_{PER\_PH\_OC}$ to build the current limit threshold. In this situation, the current limit threshold is internally preset to 300mV.

Output Over-Voltage Protection (OVP)

The output voltage can be continuously monitored through VSEN pin for over-voltage protection. If REFIN voltage is lower than 1.33V, the over voltage threshold follows to absolute over voltage 2V. If REFIN voltage is higher than 1.33V, the over voltage threshold follows relative over voltage 1.5 x V_{REFIN} . When OVP is triggered, the high-side MOSFET is turned off and the low-side MOSFET is turned on to discharge the output capacitor energy. The RT8845A is latched once OVP is triggered and can only be released by VCC or EN power on reset. A 5μs delay is used in OVP detection circuit to prevent false trigger.

Output Under-Voltage Protection (UVP)

The output voltage can be continuously monitored through VSEN pin for under-voltage protection. When the output voltage is less than 40% of its set voltage, under voltage protection is triggered and then both of the high-side and low-side MOSFETs are turned off. There is a 3μs delay built in the UVP circuit to prevent false transitions. During soft-start, the UVP blanking time is equal to PGOOD blanking time.

Inductor Selection

The switching frequency and ripple current determine the inductor value as follows :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{I_{RIPPLE(MAX)}} \times T_{ON}$$

where T_{ON} is the UGATE turn on period.

Higher inductance results in achieves lower ripple current and hence in higher efficiency but with a slower load transient response as a, trade off. Thus, a need for more output capacitors may be required, driving the cost up. The RT8845A adopts inductor DCR sensing for droop and sum over current alert circuit. For ensure the accuracy of DCR sensing signal, the minimum DC resistance of inductor must be greater than 0.3mΩ. The core must be large enough not to be saturated at the peak inductor current.

Output Capacitor Selection

Output capacitors are used to maintain high performance for the output beyond the bandwidth of the converter itself. Two different kinds of output capacitors can be found, bulk capacitors closely located to the inductors and ceramic output capacitors in close proximity to the load. Latter ones are for mid frequency decoupling with especially small ESR and ESL values while the bulk capacitors have to provide enough stored energy to overcome the low-frequency bandwidth gap between the regulator and the GPU.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (36°C/W) = 2.778W for a WQFN-40L 5x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 14 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

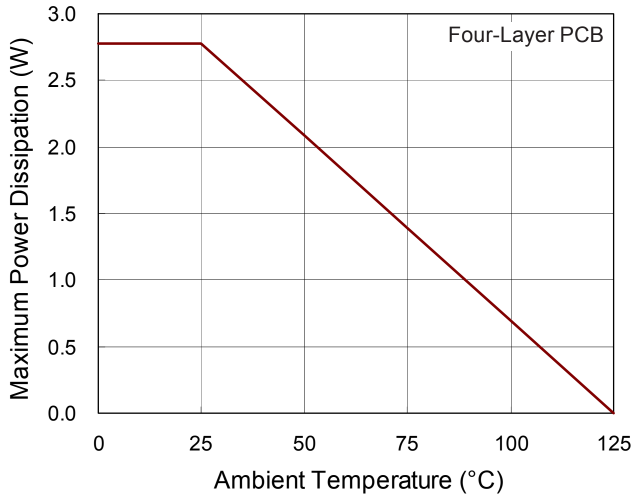


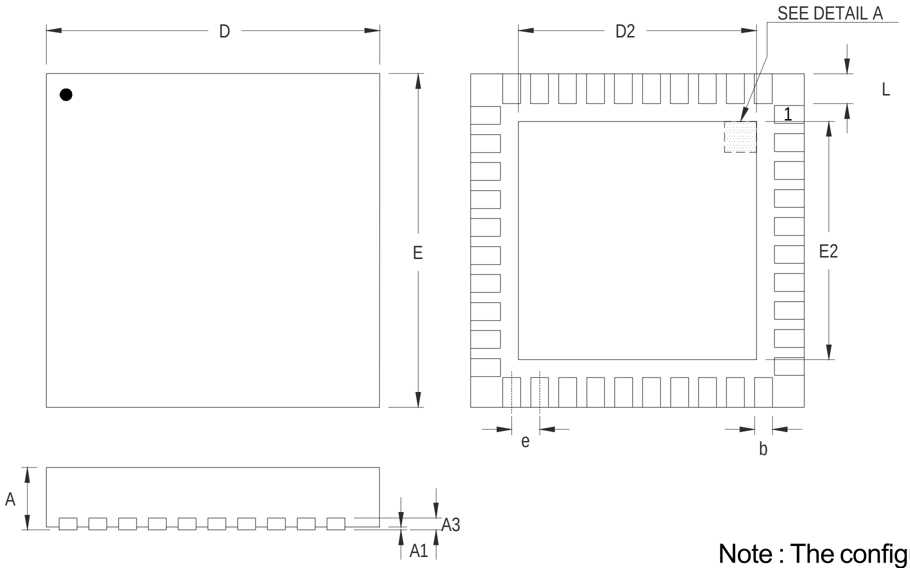
Figure 14. Derating Curve of Maximum Power Dissipation

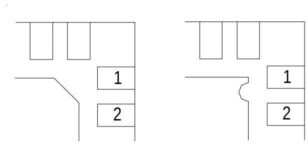
Layout Considerations

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for optimum PC board layout :

- Keep the high current paths short, especially at the ground terminals.
- Keep the power traces and load connections short. This is essential for high efficiency.
- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharging path.
- Place the current sense components close to the controller. CSPSUM and CSNSUM connections for current limit and voltage positioning must be made using Kelvin sense connections to guarantee the current sense accuracy. The PCB trace from the sense nodes should be paralleled back to the controller.
- Route high speed switching nodes away from sensitive analog areas (COMP, FB, CSPSUM, CSNSUM, CSOUT, etc.)

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

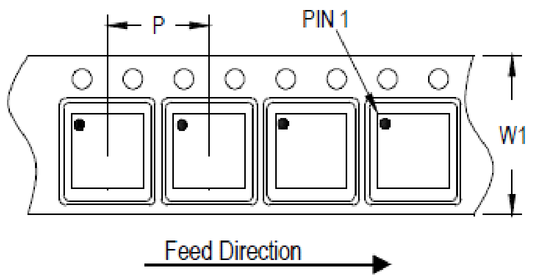
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

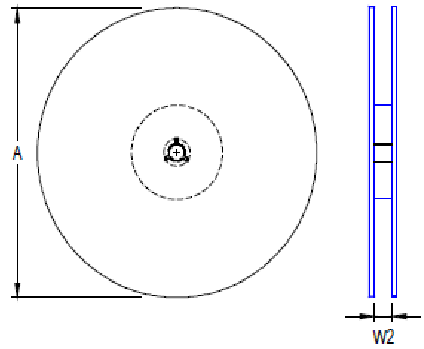
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

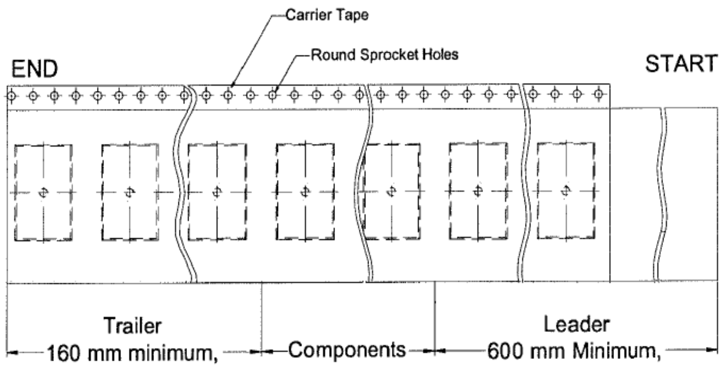
W-Type 40L QFN 5x5 Package

Packing Information

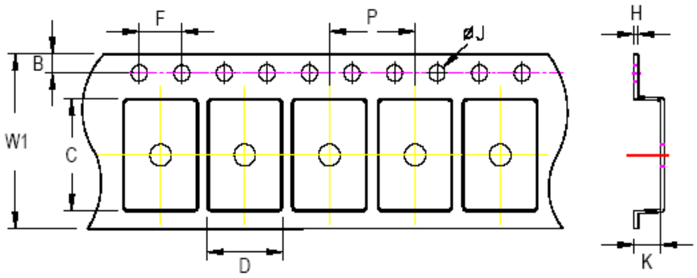
Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box					Carton			
	Size	Units	Item	Size(cm)	Weight(Kg)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN/DFN 5x5	7”	1,500	Box A	18.3*18.3*8.0	0.1	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	0.03	1	1,500	For Combined or Un -full Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 ~ 10^{11}**	**10^4 ~ 10^{11}**	**10^4 ~ 10^{11}**	**10^4 ~ 10^{11}**	**10^4 ~ 10^{11}**	**10^4 ~ 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
03	2022/12/15	Modify	Electrical Characteristics on P8 Note 6 on P8 Application Information on P15 Packing Information on P25, 26, 27