RICHTEK®

RT8816A

Dual-Phase PWM Controller with PWM-VID Reference

1 General Description

The RT8816A is a 2/1 dual-phase synchronous buck PWM controller optimized for high-performance graphic microprocessors and supports the nVidia OVR2 specification with a PWM-VID interface. The IC integrates a Constant On-Time (COT) PWM controller, two MOSFET drivers with internal bootstrap diodes, and channel current balance. It also includes comprehensive protection functions, including overvoltage protection (OVP), undervoltage protection (UVP), current limit, and over-temperature protection, all within a WQFN-20L 3x3 package.

The RT8816A adopts an $R_{DS(ON)}$ current sensing technique for current limit, which is accomplished through continuous inductor current sensing, while $R_{DS(ON)}$ current sensing is used for accurate channel current balance. This method of current sampling utilizes the best advantages of each technique.

Features of the RT8816A include an external reference input and PWM-VID dynamic output voltage control, where the feedback voltage is regulated to track an external input reference voltage. Other features include an adjustable switching frequency, dynamic phase number control, internal soft-start, power-good indicator, and enable functions. The recommended junction temperature range is $-10°C$ to $105°C$.
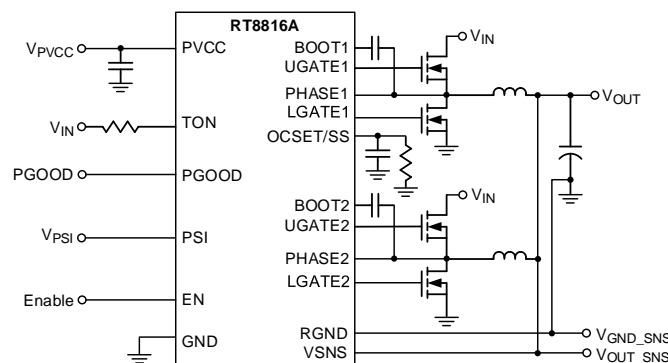
2 Features

- **Dual-Phase PWM Controller**
- **Power-State Indicator**
  - **1P-CCM/2P-CCM/1P-DEM/2P-DEM**
- **Two Embedded MOSFET Drivers and Embedded Switching Boot Diode**
- **Support a 1.8V PWM-VID Interface**
- **External Reference Input Control**
- **PWM-VID Dynamic Voltage Control**
- **Dynamic Phase Number Control**
- **Lossless $R_{DS(ON)}$ Current Sensing for Current Balance**
- **Internal/External Soft-Start**
- **Adjustable Current-Limit Threshold**
- **Adjustable Switching Frequency**
- **UVP/OVP Protection**
- **Shoot Through Protection and Short Pulse Free Technology**
- **Support an Ultra-Low Output Voltage as Standby Voltage**
- **Over-Temperature Protection**
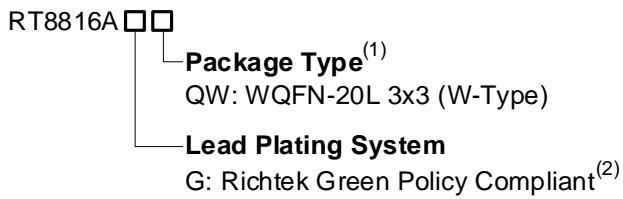- **Power-Good Indicator (EN to PGOOD High = 500µs)**

3 Applications

- CPU/GPU Core Power Supply
- Desktop PC Memory, VTT Power
- Chipset/RAM Power Supply
- Generic DC-DC Power Regulator
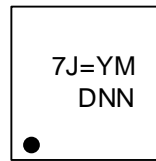
4 Simplified Application Circuit

5 Ordering Information

RT8816A☐☐

└─ **Package Type**(1)
  QW: WQFN-20L 3x3 (W-Type)

└─ **Lead Plating System**
  G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.

- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.
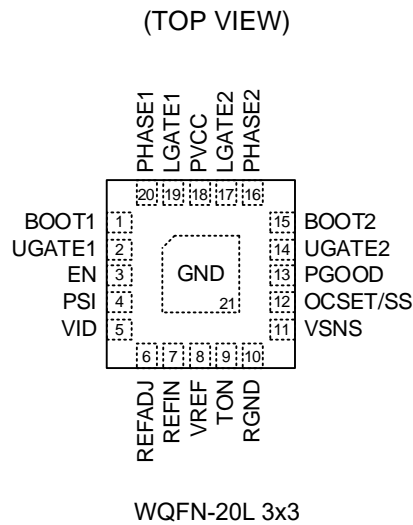
6 Marking Information

7J=YM
DNN
●

7J=: Product Code
YMDNN: Date Code

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7 Pin Configuration

(TOP VIEW)

WQFN-20L 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT1	Bootstrap supply for PWM1. This pin powers the high-side MOSFET driver.
2	UGATE1	High-side gate driver of PWM1. This pin provides the gate drive for the converter's high-side MOSFET. Connect this pin to the gate of the high-side MOSFET.
3	EN	Enable control input. Active high input. When PVCC is under Power-On Reset (POR), the input voltage must not exceed PVCC.
4	PSI	Power saving interface. When the voltage is pulled below 0.4V, the device operates into 1-phase DEM. When the voltage is between 0.7V to 0.88V, the device operates into 1-phase forced CCM. When the voltage is between 1.08V to 1.35V, the device operates into 2-phase DEM. When the voltage is between 1.6V to 5.5V, the device operates into 2-phase forced CCM.
5	VID	Programming output voltage control input. Refer to PWM VID and Dynamic Output Voltage Control.
6	REFADJ	Reference adjustment output. Refer to PWM VID and Dynamic Output Voltage Control.
7	REFIN	External reference input.
8	VREF	Reference voltage output. Connect a $0.1\mu F/0603$ decoupling capacitor between VREF and GND. The reference voltage is 2V.
9	TON	On-time/switching frequency adjustment input. Connecting a 100pF ceramic capacitor between C_{TON} and ground is optional for noise immunity enhancement.
10	RGND	Negative remote sense input. Connect this pin to the ground of the output load.
11	VSNS	Positive remote sense input. Connect this pin to the positive terminal of the output load.
12	OCSET/SS	Current limit setting. Connect a resistor from OCSET/SS to GND to set the current- limit threshold. The external soft-start time also can be set by connecting a capacitor from the OCSET/SS pin to GND.
13	PGOOD	Power-good indicator output. Active high open-drain output.

Pin No.	Pin Name	Pin Function
14	UGATE2	High-side gate driver of PWM2. This pin provides the gate drive for the converter's high-side MOSFET. Connect this pin to the gate of the high-side MOSFET.
15	BOOT2	Bootstrap supply for PWM2. This pin powers the high-side MOSFET driver.
16	PHASE2	Switch node for PWM2. This pin is the return node of the high-side driver of PWM 2. Connect this pin to the source of the high-side MOSFET, along with the drain of the low-side MOSFET and the inductor.
17	LGATE2	Low-side gate driver of PWM2. This pin provides the gate drive for the converter's low-side MOSFET. Connect this pin to the gate of the low-side MOSFET.
18	PVCC	Supply voltage input. Connect this pin to a 5V bias supply. Place a high-quality bypass capacitor from this pin to GND.
19	LGATE1	Low-side gate driver of PWM1. This pin provides the gate drive for the converter's low-side MOSFET. Connect this pin to the gate of the low-side MOSFET.
20	PHASE1	Switch node for PWM1. This pin is the return node of the high-side driver of PWM 1. Connect this pin to the source of the high-side MOSFET, along with the drain of the low-side MOSFET and the inductor.
21 (Exposed Pad)	GND	Ground. The exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.

9 Functional Block Diagram
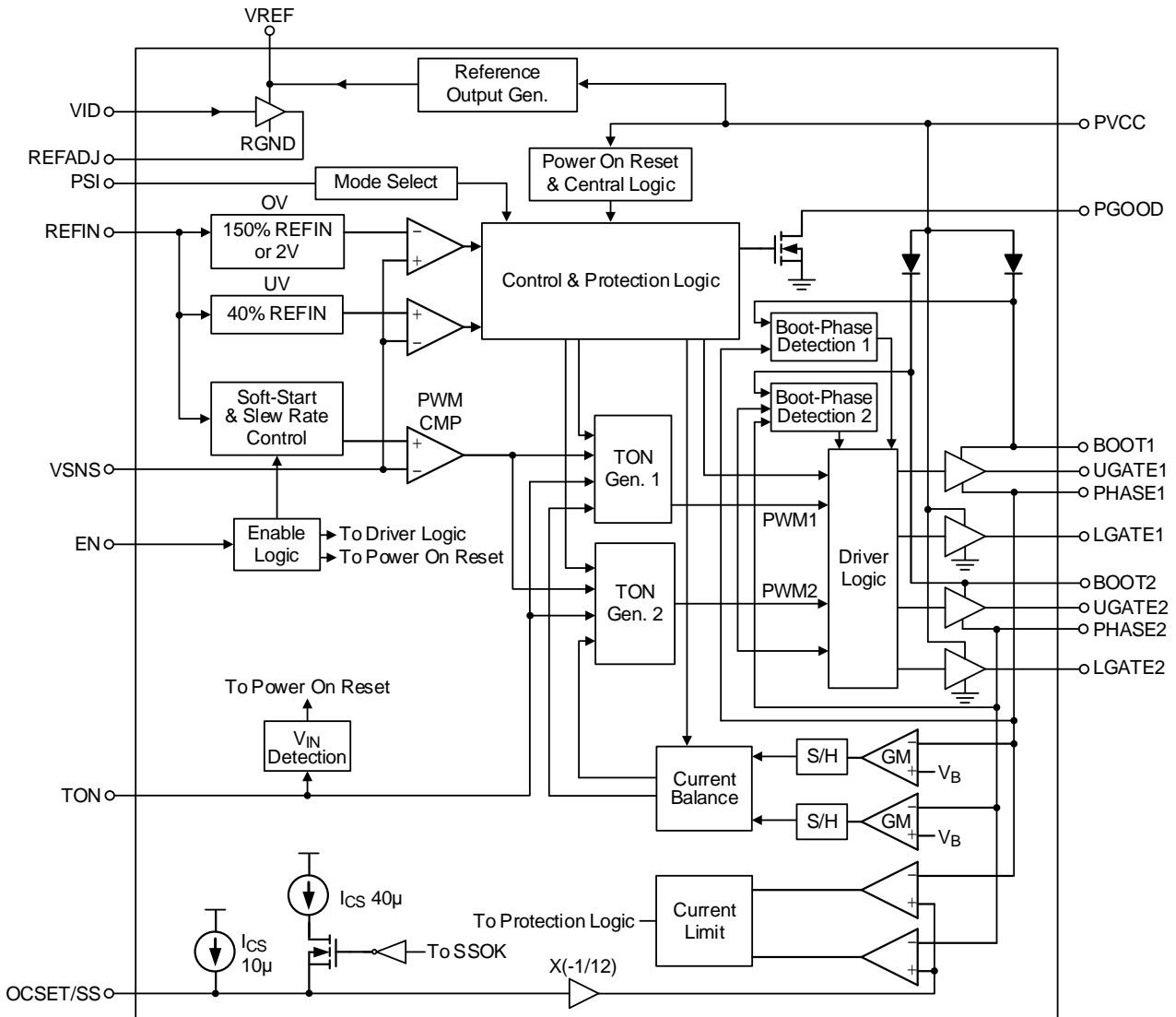
10 Absolute Maximum Ratings

([Note 2](#))

- TON to GND --- −0.3V to 30V
- RGND to GND-- −0.7V to 0.7V
- BOOTx to PHASEx
  DC--- −0.3V to 6V
  <100ns --- −5V to 7.5V
- BOOTx to GND
  DC--- −0.3V to 36V
  <100ns --- −5V to 42V
- PHASEx to GND
  DC--- −5V to 30V
  <100ns --- −10V to 42V
- UGATEx to GND
  DC--- −5V to 36V
  <100ns --- −10V to 42V
- UGATEx to PHASEx
  DC--- −0.3V to 6V
  <100ns --- −5V to 7.5V
- LGATEx to GND
  DC--- −0.3V to 6V
  <100ns --- −5V to 7.5V
- Other Pins --- −0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 3x3--- 2.67W
- Package Thermal Resistance   ([Note 3](#))
  WQFN-20L 3x3, θ_{JA}--- 30°C/W
  WQFN-20L 3x3, θ_{JC} --- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature --- 150°C
- Storage Temperature Range --- −65°C to 150°C
- ESD Susceptibility   ([Note 4](#))
  HBM (Human Body Model)-- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

([Note 5](#))

- Input Voltage, VIN --- 2.5V to 26V
- Supply Voltage, PVCC --- 4.5V to 5.5V
- Junction Temperature Range-- −10°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{PVCC} = 5V, typical values are referenced to T_A = T_J = 25°C, Min and Max values are referenced to T_A = T_J from −10°C to 105°C, unless other noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
PVCC Supply Input Voltage	V_{PVCC}		4.5	--	5.5	V
PVCC Supply Input Current	I_{PVCC}	V_{EN} = 3.3V, 1-phase DEM mode, not switching, VREF external R = 40k	--	0.4	--	mA
PVCC Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	10	μA
PVCC POR Threshold	V_{POR}		3.8	4.1	4.4	V
POR Hysteresis	V_{POR_HYS}		--	0.3	--	V
Switching Frequency	f_{SW}	R_{TON} = 500kΩ ([Note 6](#))	270	300	330	kHz
Minimum On-Time	t_{ON_MIN}		--	70	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	300	--	ns
EN Input Voltage						
EN Input Voltage Rising Threshold	V_{EN_R}		1.2	--	5.5	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.55	V
Mode Decision						
2-Phase CCM	V_{PSI}		1.6	1.8	5.5	V
2-Phase DEM	V_{PSI}		1.08	1.2	1.35	V
1-Phase CCM	V_{PSI}		0.7	0.8	0.88	V
1-Phase DEM	V_{PSI}		--	0	0.4	V
PWM-VID Input Voltage for 1.8V GPIO Setting						
PWM-VID Input Voltage Logic H	$V_{PWM-VID\_H}$		1.2	--	--	V
PWM-VID Input Voltage Logic L	$V_{PWM-VID\_L}$		--	--	0.6	V
PWM-VID Tri-State Voltage	$V_{PWM-VID\_Tr}$		0.8	--	1.05	V
Protection Function						
Zero Current Crossing Threshold	V_{ZC}		−8	--	8	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current-Limit Setting Current	I_{OCSET}	$T_A = T_J = 25°C$	9	10	11	μA
Current-Limit Setting Current Temperature Coefficient	I_{OCSET_TC}		--	4700	--	ppm/°C
Current-Limit Threshold	V_{OCSET}	$R_{OCSET} = 120k$	--	100	--	mV
Absolute Overvoltage Protection Threshold	$V_{OVP\_Absolute}$	$V_{REFIN} \leq 1.33V$	1.9	2	2.1	V
Relative Overvoltage Protection Threshold	$V_{OVP\_Relative}$	$V_{REFIN} > 1.33V$	145	150	155	%
Overvoltage Fault Delay	t_{DLY_OV}	FB forced above OV threshold	--	5	--	μs
Relative Undervoltage Protection Threshold	V_{UVP}	UVP	35	40	45	%
Undervoltage Fault Delay	t_{DLY_UV}	FB forced above UV threshold	--	3	--	μs
Over-Temperature Threshold	T_{OTP}		--	150	--	°C
VOUT Soft-Start (PGOOD Blanking Time)	t_{PGOODB}	From V_{EN} = high to VOUT regulation point, $V_{REFIN} = 1V$	--	0.5	--	ms
PWM Comparator						
VSNS Comparator Offset Voltage (Valley)	V_{CMP_OFFSET}	$V_{REFIN} = 1V$	−11	−6	−1	mV
Reference						
Reference Voltage	V_{REF}	Sourcing current = 1mA, VID no switching	1.98	2	2.02	V
Driver On-Resistance						
UGATE Driver Source Impedance	R_{SRC_UGATE}	BOOTx − PHASEx forced to 5V	--	2	4	Ω
UGATE Driver Sink Impedance	R_{SNK_UGATE}	BOOTx − PHASEx forced to 5V	--	1	2	Ω
LGATE Driver Source Impedance	R_{SRC_LGATE}	LGATEx, high state	--	1.5	3	Ω
LGATE Driver Sink Impedance	R_{SNK_LGATE}	LGATEx, low state	--	0.7	1.5	Ω
UGATE Propagation Delay Time	t_{DLY_UG}	From LGATE falling to UGATE rising	--	30	--	ns
LGATE Propagation Delay Time	t_{DLY_LG}	From UGATE falling to LGATE rising	--	20	--	ns
Internal Boost Diode Resistance	R_{BOOT}	PVCC to BOOTx, $I_{BOOT} = 10mA$	--	80	--	Ω

Note 6. Not production tested. Test condition is $V_{IN} = 8V$, $V_{OUT} = 1V$, $I_{OUT} = 20A$ using application circuit.
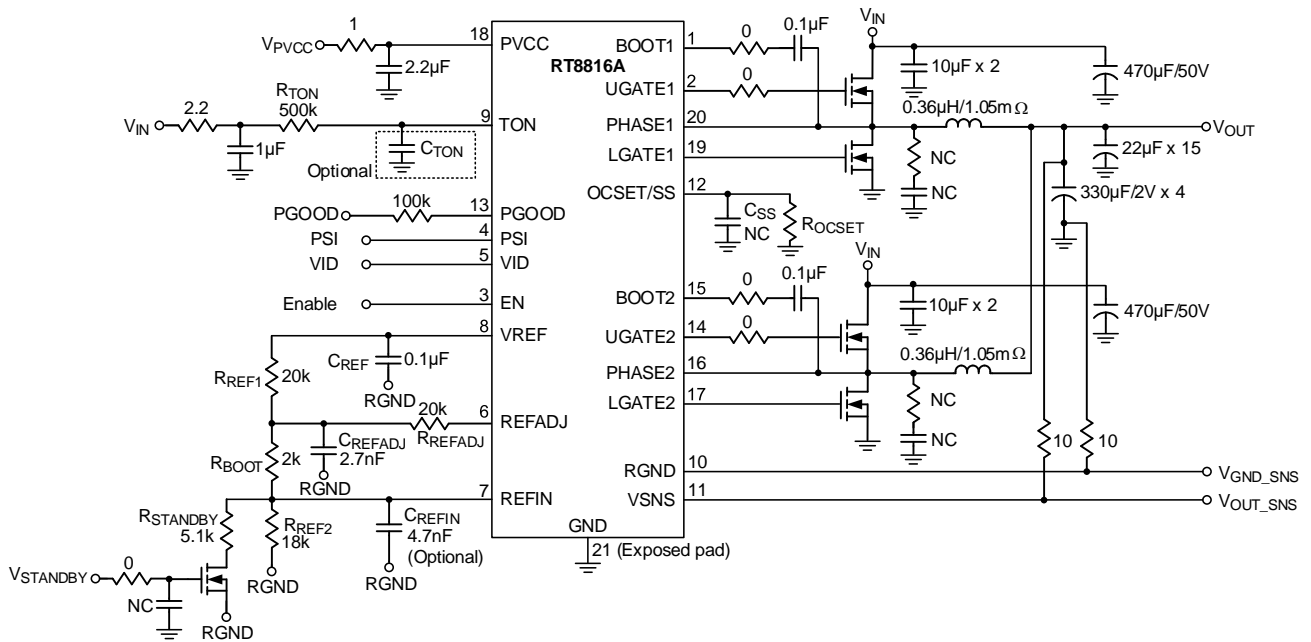
13 Typical Application Circuit
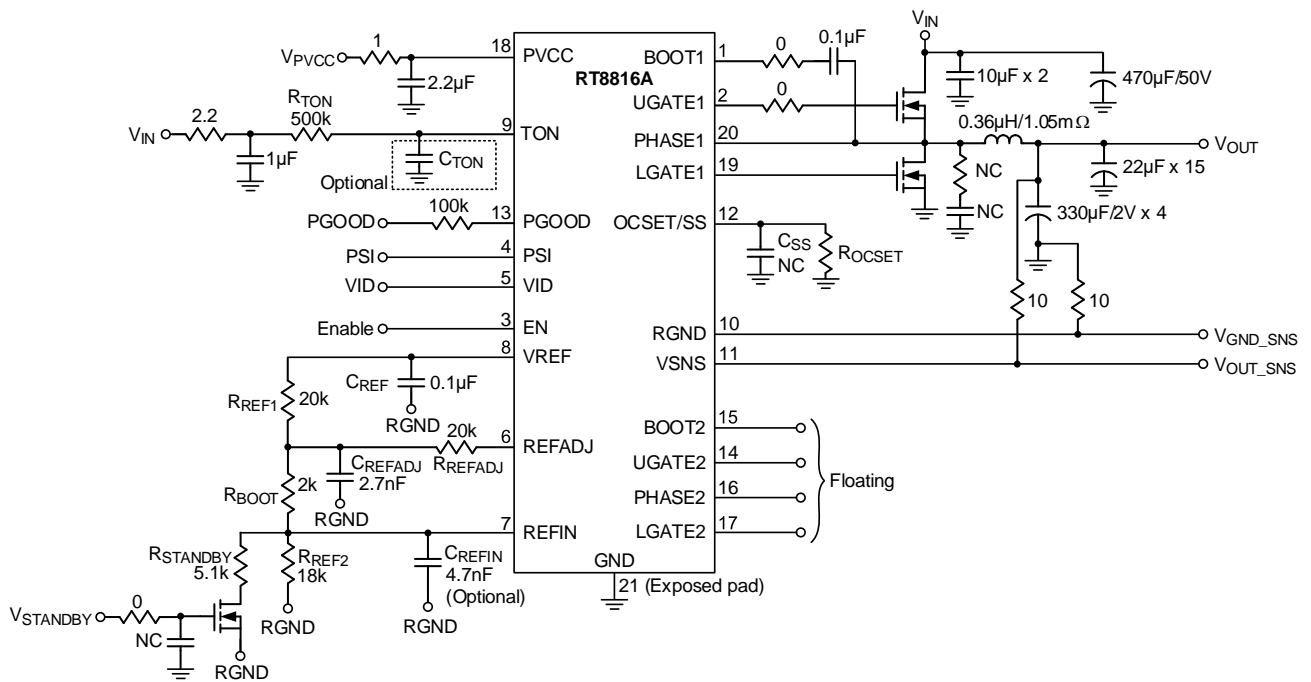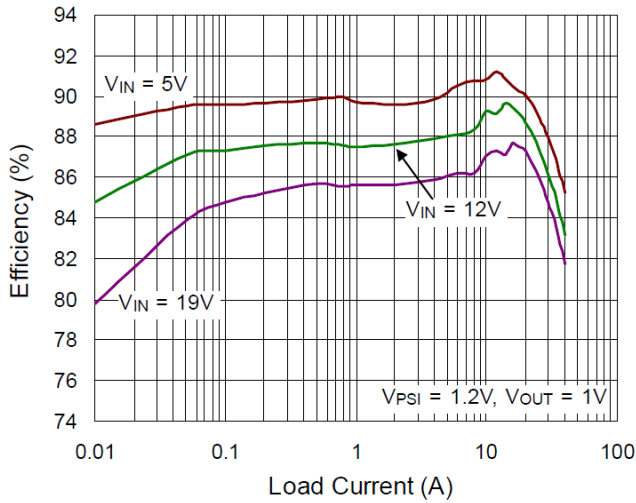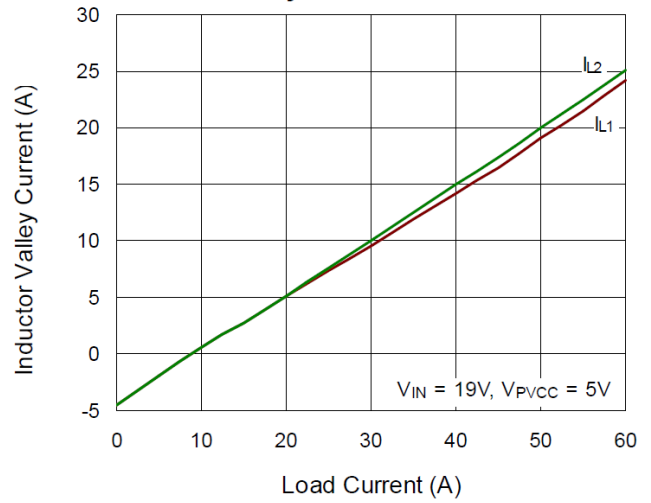

Figure 1. Two Active Phase Configuration

Figure 2. One Active Phase Configuration
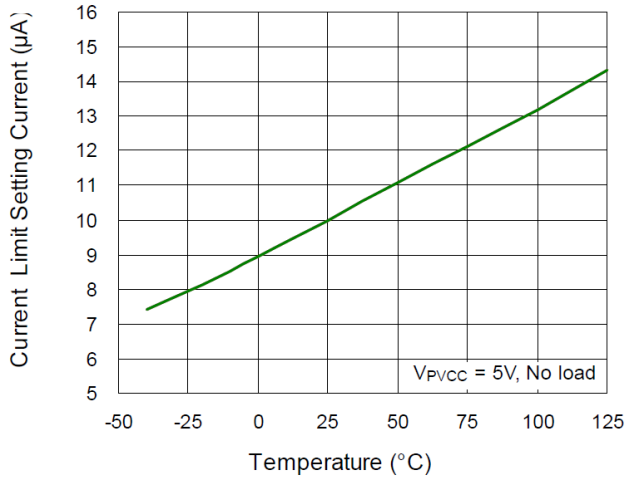
14 Typical Operating Characteristics
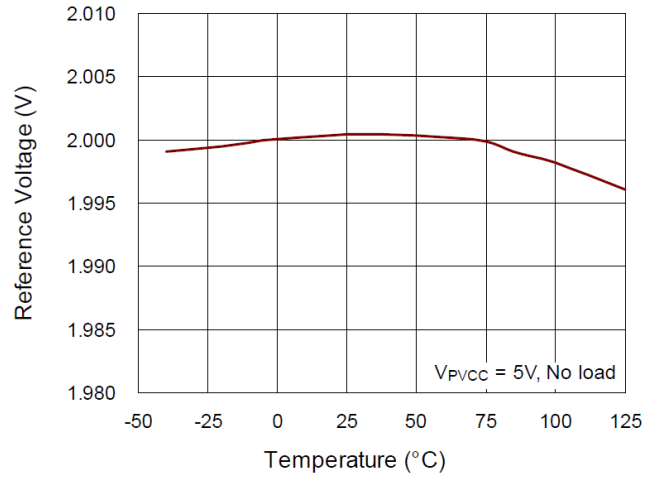
Efficiency vs. Load Current
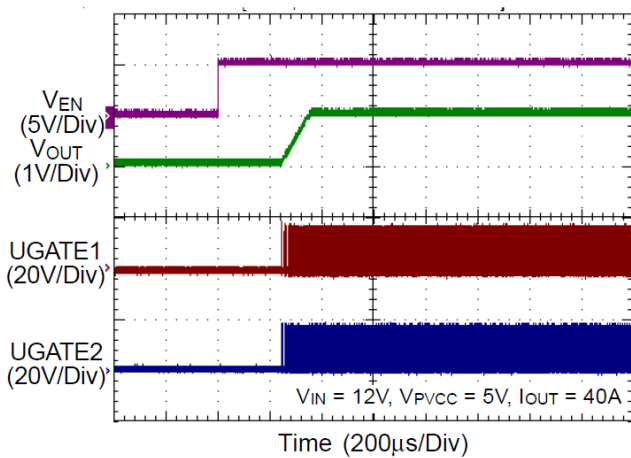

Inductor Valley Current vs. Load Current

Current Limit Setting Current vs. Temperature

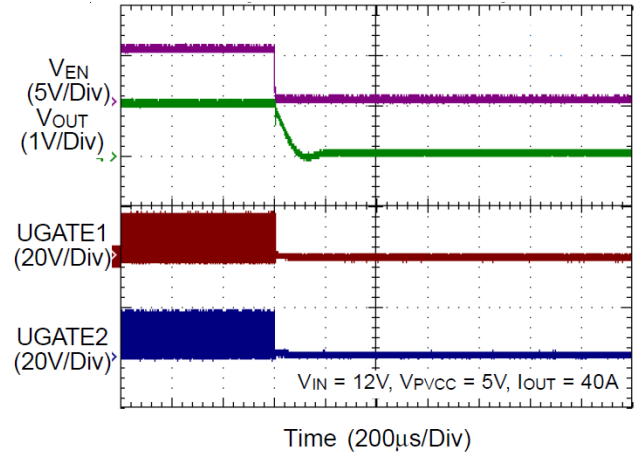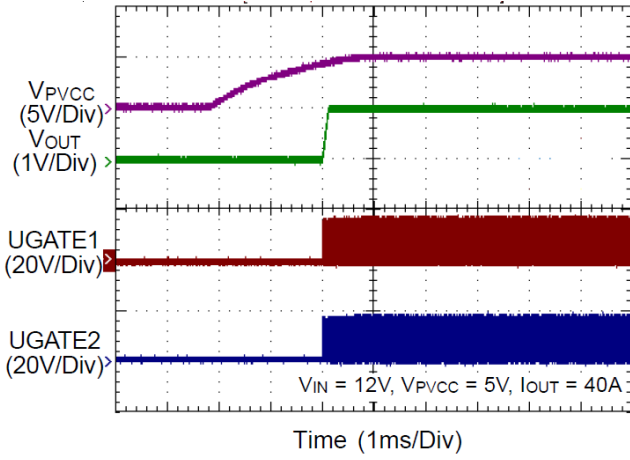**Reference Voltage vs. Temperature**
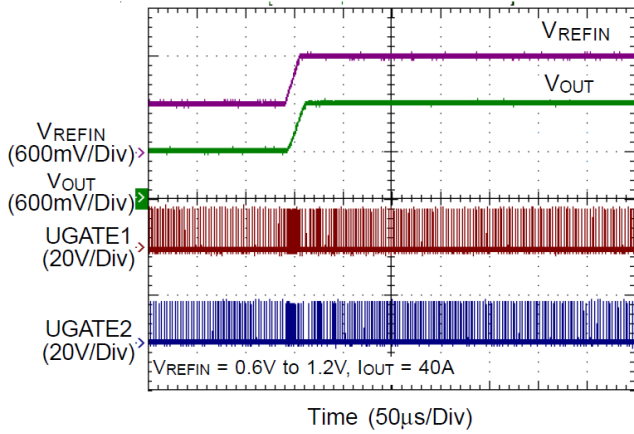

Power On from EN

Power Off from EN

Power On from PVCC

V_{PVCC} (5V/Div)
V_{OUT} (1V/Div)
UGATE1 (20V/Div)
UGATE2 (20V/Div)

V_{IN} = 12V, V_{PVCC} = 5V, I_{OUT} = 40A

Time (1ms/Div)

Power Off from VCC

V_{PVCC} (5V/Div)
V_{OUT} (1V/Div)
UGATE1 (20V/Div)
UGATE2 (20V/Div)

PVCC
V_{OUT}

V_{IN} = 12V, V_{PVCC} = 5V, I_{OUT} = 40A

Time (20ms/Div)

Dynamic Output Voltage Control

V_{REFIN}
V_{OUT}
V_{REFIN} (600mV/Div)
V_{OUT} (600mV/Div)
UGATE1 (20V/Div)
UGATE2 (20V/Div)

V_{REFIN} = 0.6V to 1.2V, I_{OUT} = 40A

Time (50µs/Div)

Dynamic Output Voltage Control

V_{REFIN}
V_{OUT}
V_{REFIN} (600mV/Div)
V_{OUT} (600mV/Div)
UGATE1 (20V/Div)
UGATE2 (20V/Div)

V_{REFIN} = 1.2V to 0.6V, I_{OUT} = 40A

Time (50µs/Div)

Load Transient Response

V_{OUT} (40mV/Div)
I_{OUT} (20A/Div)
UGATE1 (20V/Div)
UGATE2 (20V/Div)

V_{IN} = 12V, V_{OUT} = 1V

Time (10µs/Div)

Load Transient Response

V_{OUT} (40mV/Div)
I_{OUT} (20A/Div)
UGATE1 (20V/Div)
UGATE2 (20V/Div)

V_{IN} = 12V, V_{OUT} = 1V

Time (10µs/Div)

Current Limit and UVP

V_OUT (500mV/Div)

V_IN = 12V, V_PVCC = 5V

4->

I_L1 (10A/Div)
UGATE1 (20V/Div)
LGATE1 (5V/Div)

Time (100µs/Div)

OVP

V_SNS (500mV/Div)

3->

UGATE1 (20V/Div)
LGATE1 (5V/Div)

V_IN = 12V, V_PVCC = 5V, No Load

Time (100µs/Div)

15 Operation

The RT8816A is a dual-phase synchronous buck PWM controller with integrated drivers, optimized for high-performance graphics microprocessors and computer applications. The IC integrates a Constant On-Time (COT) PWM controller, two MOSFET drivers, as well as output current monitoring and protection functions. According to Functional Block Diagram of the TON Genx, the synchronous UGATE driver is activated at the beginning of each cycle. Once the internal one-shot timer expires, the UGATE driver is deactivated. The duration of this one-shot pulse is determined by the converter's input voltage and the output voltage to maintain a relatively constant frequency across the input voltage range and the output voltage. Another one-shot timer establishes a minimum off-time.

Additionally, the RT8816A features a PWM-VID dynamic voltage control circuit, which utilizes the pulse width modulation method. This circuit reduces the number of device pins required and supports a wide dynamic voltage range.

15.1 Soft-Start Function

For the soft-start (SS) function, an internal current source charges an internal capacitor to build the soft-start ramp voltage. The output voltage will track the internal ramp voltage during soft-start interval.

15.2 Power-Good Indicator

The power-good output is an open-drain architecture.

When the soft-start is finished, the PGOOD open-drain output is high impedance.

15.3 Current Balance

The RT8816A implements an internal current balance mechanism in the current loop. The RT8816A senses per-phase current and compares it with the average current. If the sensed current of any particular phase is higher than the average current, the on-time of this phase is adjusted to be shorter.

15.4 Current Limit

The current-limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. Thus, if the current to the load exceeds the average output inductor current, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

15.5 Overvoltage Protection (OVP) and Undervoltage Protection (UVP)

The output voltage is continuously monitored for overvoltage and undervoltage protections. When the output voltage exceeds its set voltage threshold (if $V_{REFIN} \leq 1.33V$, OV = 2V; or if $V_{REFIN} > 1.33V$, OV = 1.5 x V_{REFIN}), UGATE goes low and LGATE is forced high. When it is less than 40% of its set voltage, the undervoltage protection is triggered and then both UGATE and LGATE gate drivers are forced low. The controller is latched until PVCC is re-supplied and exceeds the POR rising threshold voltage, or EN is reset.

16 Application Information

([Note 7](#))

The RT8816A is a dual-phase synchronous buck PWM controller with integrated drivers, optimized for high performance graphics microprocessors and computer applications. A COT (Constant On-Time) PWM controller and two MOSFET drivers with internal bootstrap diodes are integrated to simplify the external circuit and reduce the component count.

The topology solves the poor load transient response timing problems associated with fixed-frequency mode PWM and avoids the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The IC supports a dynamic mode transition function with various operating states, which include single phase with CCM, dual-phase with CCM, single phase with diode emulation mode, and dual-phase with diode emulation mode operations. These different operating states enhance the system efficiency.

The RT8816A provides a PWM-VID dynamic control operation, where the feedback voltage is regulated to track an external input reference voltage. It also features comprehensive fault protection functions, including overvoltage, undervoltage, and current limit protections.

16.1 Remote Sense

The RT8816A uses the remote sense path (VSNS and RGND) to overcome voltage drops in the power lines by sensing the voltage directly at the end of GPU. Normally, to protect remote sense path disconnecting, there are two resistors (R_{Local}) connecting between local sense path and remote sense path. That is, in applications with remote sensing, it is recommended that the R_{Local} be between 10Ω to 100Ω. If remote sensing is not required, R_{Local} is recommended to be 0Ω.
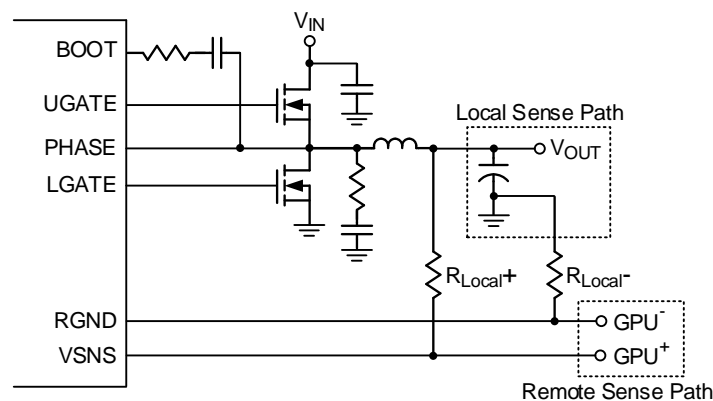

Figure 3. Output Voltage Sensing

16.2 PWM Operation

The RT8816A integrates a Constant On-Time (COT) PWM controller, and the controller provides the PWM signal based on the comparison of the output ripple voltage with an internal reference voltage, as shown in [Figure 4](#). According to [Functional Block Diagram](#) of the TON Genx, the synchronous UGATE driver is turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver is turned off. The duration of this one-shot pulse width is determined by the converter input voltage and the output voltage to keep a relatively constant frequency across the input and output voltage range. Another one-shot mechanism sets a minimum off-time.
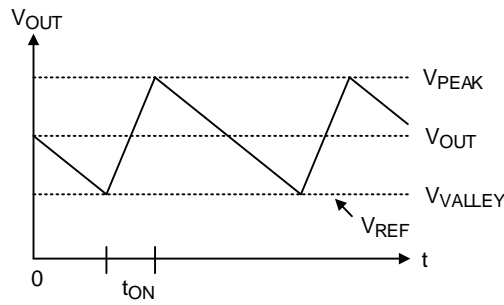
Figure 4. Constant On-Time PWM Control

16.3 On-Time Control

The on-time one-shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to V_{OUT}, thereby making the on-time of the high-side switch directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need for a clock generator.

$$T_{ON} = \frac{2 \times V_{OUT} \times 3.2p}{V_{IN} - 0.5} \times R_{TON}$$

and then the switching frequency f_S is:

$f_S = V_{OUT} / (V_{IN} \times T_{ON})$

R_{TON} is a resistor connected from the V_{IN} to the TON pin.

The recommended operation frequency range is from 250kHz to 750kHz.

16.4 Active Phase Circuit Setting

The RT8816A can be set for 2-phase or 1-phase operation by hardware circuit. For 1-phase operation, the UGATE2, BOOT2, PHASE2, and LGATE2 pins are floating, and the voltage of the PSI pin must be set to the 1-phase operation threshold. Refer to Table 1 for details.

16.5 Mode Selection

The RT8816A can operate into 2-phase with forced CCM, 1-phase with forced CCM, 1-phase with DEM and 2-phase with DEM, depending on the PSI voltage setting. If the PSI voltage is pulled below 0.4V, the controller operates into 1-phase with DEM. In DEM operation, the RT8816A automatically reduces the operation frequency at light load conditions for saving power loss. If the PSI voltage is pulled between 0.7V to 0.88V, the controller switches to 1-phase with forced CCM. If the PSI voltage is pulled between 1.08V to 1.35V, the controller switches to 2-phase with DEM. If the PSI voltage is pulled between 1.6V to 5.5V, the controller switches to 2-phase with forced CCM. The operation modes are summarized in Table 1. Moreover, the PSI pin is valid after POR of VR.

Table 1

Operation Phase Number	PSI Voltage Setting
1-phase with DEM	0V to 0.4V
1-phase with CCM	0.7V to 0.88V
2-phase with DEM	1.08V to 1.35V
2-phase with DEM	1.6V to 5.5V

16.6 Diode-Emulation Mode

In diode-emulation mode, the RT8816A automatically reduces the switching frequency at light-load conditions to maintain high efficiency. As the output current decreases from a heavy-load condition, the inductor current also reduces. This reduction continues until the inductor current's valley reaches zero, making the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low-side MOSFET allows only partial of the negative current when the inductor freewheeling current reaches a negative value. As the load current further decreases, it takes longer to discharge the output capacitor to the level that requires the next "ON" cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction condition. The transition load point to the light load operation is shown in Figure 5 and can be calculated as follows:

$$I_{LOAD(SKIP)} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$
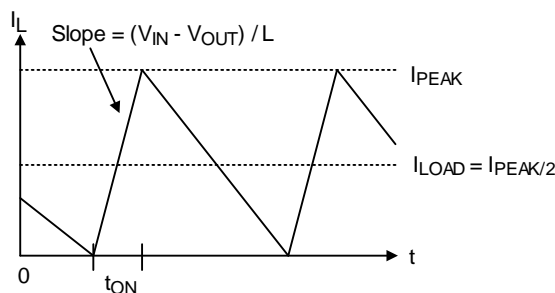
where t_{ON} is on-time.

Figure 5. Boundary Condition of CCM/DEM

The switching waveforms may be noisy and asynchronous in light loading diode-emulation operation conditions, but this is a normal operating condition that results in high light-load efficiency. A trade-off between DEM noise and light-load efficiency is made by varying the inductor value. Generally, lower inductor values produce a broad high efficiency range versus load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include a larger physical size and degraded load-transient response (especially at low input voltage levels).

16.7 Forced-CCM Mode

The low noise, forced-CCM mode disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate drive waveform to be the complement of the high-side gate drive waveform, which in turn causes the inductor current to reverse at light loads as the PWM loop maintains a duty ratio of V_{OUT}/V_{IN}. The benefit of forced-CCM mode is to keep the switching frequency fairly constant.

16.8 Enable and Disable

The EN pin is a high-impedance input that allows power sequencing between the controller bias voltage and another voltage rail. The RT8816A remains in shutdown if the EN pin is lower than 550mV. When the EN voltage rises above the 1.2V high-level threshold, the RT8816A begins a new initialization and soft-start cycle.

16.9 Power On Reset (POR) and UVLO

A Power On Reset (POR) occurs when V_{PVCC} rises above approximately 4.1V (typical), the RT8816A resets the fault latch circuit and prepares for PWM operation. When the V_{PVCC} is lower than 3.8V (typical), the undervoltage-lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low.

16.10 Soft-Start Function

The RT8816A provides both internal and external soft-start functions. The soft-start function is used to prevent large inrush current and output voltage overshoot during power-up. The soft-start function automatically begins once the IC is enabled. There is a delay time around 200μs from when EN goes high to when V_OUT begins to ramp-up.

If the external capacitor from the OCSET/SS pin to GND is removed, the internal soft-start function is chosen. An internal current source charges the internal soft-start capacitor so that the internal soft-start voltage ramps up linearly. The output voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft-start voltage exceeds the REFIN voltage, the output voltage no longer tracks the internal soft-start voltage but follows the REFIN voltage. Therefore, the duty cycle of the UGATE signal, as well as the input current at power-up are limited.

The soft-start process is finished when the internal SSOK goes high, and no protection is triggered.

Furthermore, it is important to pay attention to the CREF, as the value of the CREF will affect the ramp-up speed of the VREF voltage. It is recommended to place a 0.1μF capacitor on the RT8816A to avoid unexpected soft-start behavior.
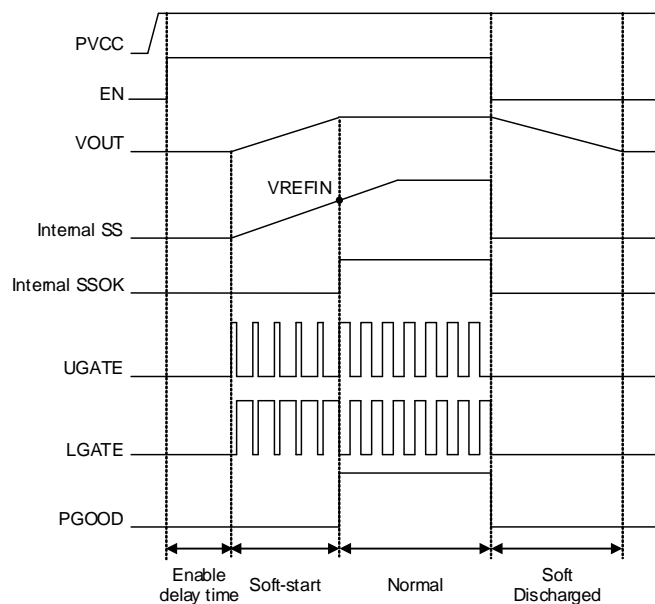
Figure 6 shows the internal soft-start sequence.

Figure 6. Internal Soft-Start Sequence

The RT8816A also provides an external soft-start function, and the external soft-start sequence is shown in Figure 7, by connecting an additional capacitor from the OCSET/SS pin to GND. The external capacitor is charged by an internal current source to build the soft-start voltage ramp. If the external soft-start function is chosen, the external soft-start time should be set longer than the internal soft-start time to avoid output voltage tracking the internal soft-start ramp. The external soft-start time setting is shown in Figure 8 and the recommended external soft-start slew rate is from 0.1V/ms to 0.4V/ms.
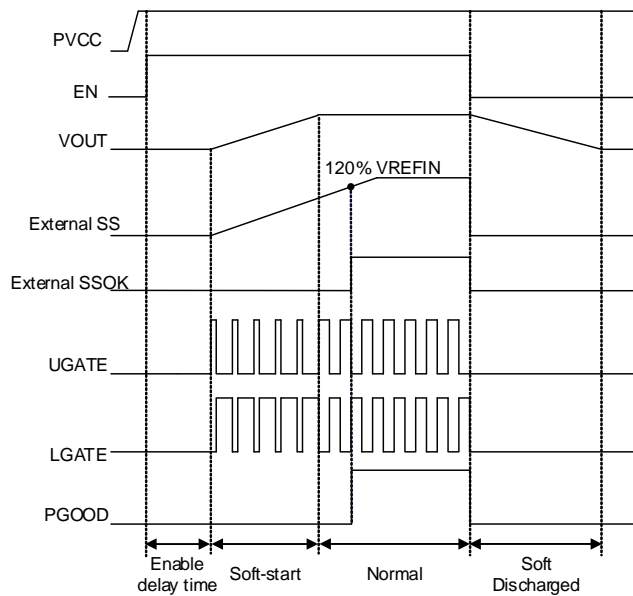
Figure 7. External Soft-Start Sequence

The soft-start time can be calculated as:

$$t_{SS} = -(C_{SS} \times R_{OCSET}) \times \ln\left[1 - \left(\frac{V_{REFIN}}{I_{SS} \times R_{OCSET}}\right)\right]$$

where I_{SS} = 50μA (typical), V_{REFIN} is the voltage of the REFIN pin, R_{OCSET} is the current limit setting resistor, and C_{SS} is the external capacitor connected from the OCSET/SS pin to GND.
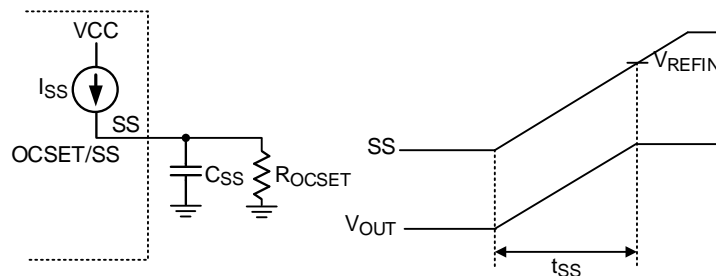

Figure 8. External Soft-Start Setting

For ensuring the soft-start function works normally, the following setting limitation must be followed:

R_{OCSET} x 50μA > 1.2 x V_{REFIN}

16.11 Power Good Output (PGOOD)

The PGOOD pin is an open-drain output, and it requires a pull-up resistor. During soft-start, the PGOOD pin is held low and is allowed to be pulled high after VOUT exceeds the UVP threshold and is under OVP threshold. In addition, if any protection is triggered during operation, the PGOOD pin is pulled low immediately.

16.12 PWM VID and Dynamic Output Voltage Control

The RT8816A features a PWM VID input for dynamic output voltage control, as shown in Figure 9, which reduces the number of device pins and enables a wide dynamic voltage range. The output voltage is determined by the applied voltage on the REFIN pin. The PWM duty cycle determines the variable output voltage at REFIN.
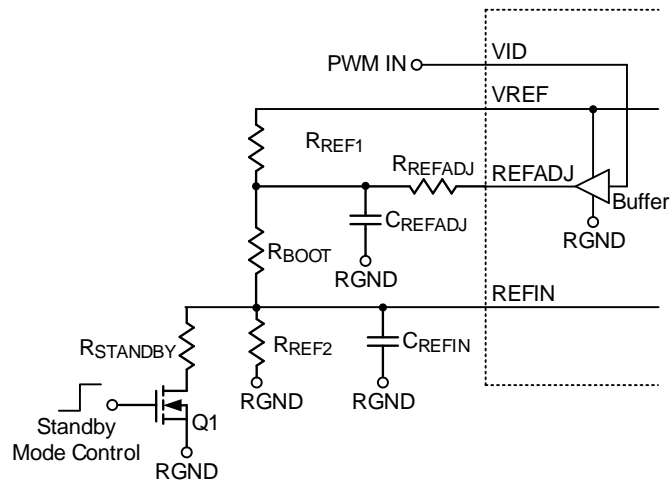
Figure 9. PWM VID Analog Circuit Diagram

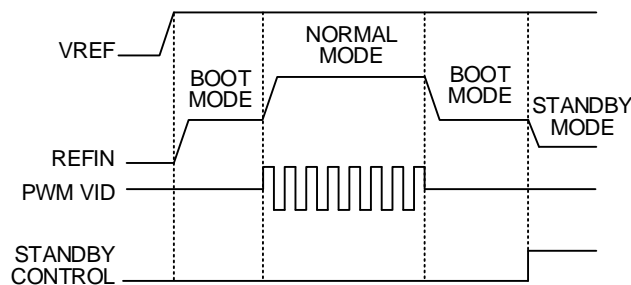With the external circuit and VID control signal, the controller provides three operation modes, shown as Figure 10.

Figure 10. PWM VID Time Diagram

16.13 Boot Mode

When VID is not driven, the buffer output is in a tri-state condition. At this time, turn off the switch Q1 and connect a resistor divider, as shown in Figure 9, that can set the REFIN voltage to be V_{BOOT} using the following equation:

$$V_{BOOT} = V_{VREF} \times \left(\frac{R_{REF2}}{R_{REF1} + R_{REF2} + R_{BOOT}} \right)$$

where V_{VREF} = 2V (typical)

Choose R_{REF2} to be approximately 10kΩ, and the R_{REF1} and R_{BOOT} can be calculated using the following equations:

$$R_{REF1} + R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}}$$

$$R_{REF1} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{BOOT}$$

$$R_{BOOT} = \frac{R_{REF2} \times (V_{VREF} - V_{BOOT})}{V_{BOOT}} - R_{REF1}$$

16.14 Standby Mode

An external control can provide a very low voltage to meet VOUT operating in standby mode. If the VID pin is floating and switch Q1 is enabled, as shown in Figure 9, the REFIN pin can be set for standby voltage according to the calculation below:

$$V_{STANDBY} = V_{VREF} \times \frac{R_{REF2} \; // \; R_{STANDBY}}{R_{REF1} + R_{BOOT} + (R_{REF2} \; // \; R_{STANDBY})}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the $R_{STANDBY}$ can be calculated using the following equation:

$$R_{STANDBY} = \frac{R_{REF2} \times (R_{REF1} + R_{BOOT}) \times V_{STANDBY}}{R_{REF2} \times V_{VREF} - V_{STANDBY} \times (R_{REF1} + R_{REF2} + R_{BOOT})}$$

16.15 Normal Mode

If the VID pin is driven by a PWM signal and switch Q1 is disabled, as shown in Figure 9, the V_{REFIN} can be adjusted from V_{min} to V_{max}, where V_{min} is the voltage at zero percent PWM duty cycle and V_{max} is the voltage at one hundred percent PWM duty cycle. The V_{min} and V_{max} can be set using the following equations:

$$V_{min} = V_{VREF} \times \frac{R_{REF2}}{R_{REF2} + R_{BOOT}} \times \frac{R_{REFADJ} \; // \; (R_{BOOT} + R_{REF2})}{R_{REF1} + \left[R_{REFADJ} \; // \; (R_{BOOT} + R_{REF2}) \right]}$$

$$V_{max} = V_{VREF} \times \frac{R_{REF2}}{(R_{REF1} \; // \; R_{REFADJ}) + R_{BOOT} + R_{REF2}}$$

By choosing R_{REF1}, R_{REF2}, and R_{BOOT}, the R_{REFADJ} can be calculated using the following equation:

$$R_{REFADJ} = \frac{R_{REF1} \times V_{min}}{V_{max} - V_{min}}$$

The relationship between VID duty and V_{REFIN} is shown in Figure 11, and V_{OUT} can be set according to the calculation below:

$$V_{OUT} = V_{min} + N \times V_{STEP}$$

where V_{STEP} is the resolution of each voltage step 1:

$$V_{STEP} = \frac{(V_{max} - V_{min})}{N_{max}}$$

where Nmax is the number of total available voltage steps and N is the number of steps at a specific V_{OUT}. The dynamic voltage VID period ($T_{vid} = T_u \times N_{max}$) is determined by the unit pulse width (T_u) and the available step number (N_{max}). The recommended T_u is 27ns.
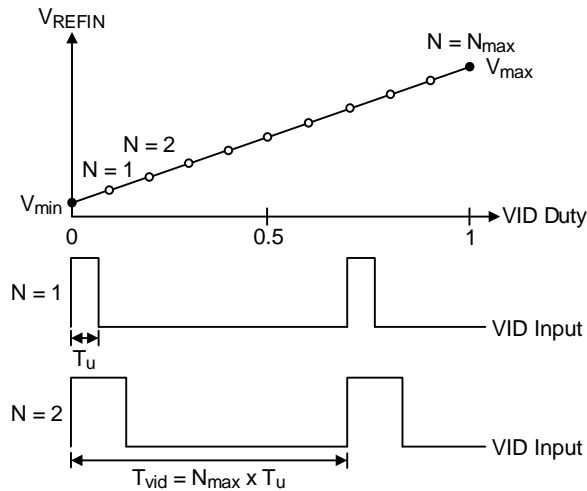
Figure 11. PWM VID Analog Output

16.16 VID Slew Rate Control

In the RT8816A, the V_{REFIN} slew rate is proportional to the PWM VID duty, and the rising time and falling time are the same. In normal mode, the V_{REFIN} slew rate SR can be estimated by C_{REFADJ} or C_{REFIN} using the following equation:

When choosing C_{REFADJ}:

$$SR = \frac{(V_{REFIN\_Final} - V_{REFIN\_initial}) \times 80\%}{2.2 R_{SR} C_{REFADJ}}$$

$$R_{SR} = [(R_{REF1} \mathbin{/\!/} R_{REFADJ})] \mathbin{/\!/} (R_{BOOT} + R_{REF2})$$

When choosing C_{REFIN}:

$$SR = \frac{(V_{REFIN\_Final} - V_{REFIN\_initial}) \times 80\%}{2.2 R_{SR} C_{REFIN}}$$

$$R_{SR} = [(R_{REF1} \mathbin{/\!/} R_{REFADJ}) + R_{BOOT}] \mathbin{/\!/} R_{REF2}$$

The recommended SR is estimated by C_{REFADJ}.

16.17 Current Limit

The RT8816A provides cycle-by-cycle current-limit control by detecting the PHASE voltage drop across the low-side MOSFET when it is turned on. The current-limit circuit employs a unique "valley" current sensing algorithm, as shown in Figure 12. If the magnitude of the current sense signal at PHASE is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.

In order to provide both good accuracy and a cost-effective solution, the RT8816A supports temperature compensated MOSFET $R_{DS(ON)}$ sensing.
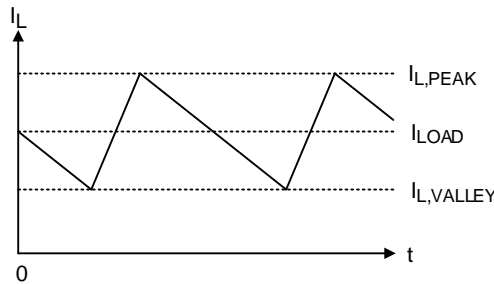
Figure 12. "Valley"Current Limit

In an overcurrent condition, the current to the load exceeds the average output inductor current. Thus, the output voltage falls and eventually crosses the undervoltage protection threshold, inducing IC shutdown.

16.18 Current Limit Setting

The RT8816A adopts per-phase current-limit protection. The current-limit threshold can be set by a resistor (R_{OCSET}) between the OCSET/SS pin and GND. Once PVCC exceeds the POR threshold and the IC is enabled, an internal current source IOCSET flows through R_{OCSET}. After the soft-start ends, I_{OCSET} is 10μA. The voltage across R_{OCSET} is stored as the current-limit protection threshold V_{OCSET}. The threshold range of V_{OCSET} is 20mV to 200mV. It can be calculated according to the following equation:

$$V_{OCSET} = \frac{I_{OCSET} \times R_{OCSET}}{12}$$

R_{OCSET} can be determined using the following equation:

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{DS\_ON} \times 12}{I_{OCSET}}$$

where I_{VALLEY} represents the desired per-phase inductor limit current (valley inductor current) and I_{OCSET} is the current-limit setting current, which has a temperature coefficient to compensate the temperature dependency of the $R_{DS(ON)}$.

If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the current-limit threshold. In this situation, the current-limit threshold is internally preset to 200mV.

16.19 Negative Current Limit

The RT8816A supports cycle-by-cycle negative current limit. The absolute value of the negative current-limit threshold is the same as the positive current-limit threshold. If negative inductor current is rising to trigger negative current limit, the low-side MOSFET is turned off, and the current flows to the input side through the body diode of the high-side MOSFET. At this time, the output voltage tends to rise because this protection limits current to discharge the output capacitor. In order to prevent shutdown because of the overvoltage protection, the low-side MOSFET is turned on again 400ns after it is turned off. If the device hits the negative current-limit threshold again before the output voltage is discharged to the target level, the low-side MOSFET is turned off, and the process repeats. It ensures the maximum allowable discharge capability when the output voltage continues to rise. Conversely, if the output is discharged to the target level before the negative current-limit threshold is reached, the low-side MOSFET is turned off, the high-side MOSFET is then turned on, and the device keeps normal operation.

16.20 Current Balance

The RT8816A implements a current balance mechanism in the current loop. The RT8816A senses per-phase current signal and compares it with the average current. If the sensed current of any particular phase is higher than the average current, the on-time of this phase is decreased.

The current balance accuracy is mainly related to the on-resistance of the low-side MOSFET ($R_{LG,DS(ON)}$). That is, in practical application, using lower $R_{LG,DS(ON)}$ will reduce the current balance accuracy.

16.21 Output Overvoltage Protection (OVP)

The output voltage can be continuously monitored for overvoltage protection. If the REFIN voltage is lower than 1.33V. The overvoltage threshold follows the absolute overvoltage of 2V. If the REFIN voltage is higher than 1.33V, the overvoltage threshold follows the relative overvoltage of 1.5 x V_{REFIN}. When OVP is triggered, UGATE goes low and LGATE is forced high. The RT8816A is latched once OVP is triggered and can only be released by a PVCC or EN power on reset. A 5μs delay is used in the OVP detection circuit to prevent false trigger.

16.22 Output Undervoltage Protection (UVP)

The output voltage can be continuously monitored for undervoltage protection. When the output voltage is less than 40% of its set voltage, undervoltage protection is triggered and then all UGATE and LGATE gate drivers are forced low. There is a 3μs delay built in the UVP circuit to prevent false transitions. During soft-start, the UVP blanking time is equal to the PGOOD blanking time.

16.23 MOSFET Gate Driver

The RT8816A integrates high current gate drivers for the MOSFETs to obtain high-efficiency power conversion in a synchronous buck topology. A dead-time is used to prevent the cross conduction for the high-side and low-side MOSFETs. Because both two gate signals are off during the dead-time, the inductor current freewheels through the body diode of the low-side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to power losses in the converter. The RT8816A employs an adaptive dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, an elaborate logic circuit is implemented to prevent cross conduction. For high output current applications, two power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. A gate driver with a lower source/sink current capability results in longer rising/falling times in gate signals and higher switching losses. The RT8816A embeds high current gate drivers to obtain high efficiency power conversion.

16.24 MOSFET Selection

The majority of power loss in the buck power conversion is due to the loss in the power MOSFETs. For low-voltage high-current applications, the duty cycle of the high-side MOSFET is low, making its switching loss a primary concern. Power MOSFETs with a lower total gate charge are preferred in such applications.

However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, the MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET is connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

16.25 Inductor Selection

The inductor plays an important role in buck converters because the energy from the input power rail is stored in it and then released to the load. For efficiency, the DC Resistance (DCR) of the inductor should be as small as possible to minimize the copper loss. In addition, the inductor occupies most of the board space, so its size is important. Low profile inductors can save board space, especially when the height is limited. However, low DCR and low-profile inductors are usually not cost effective.

Additionally, the higher inductance results in lower ripple current, which means the lower power loss. However, the inductor current rising time increases with the inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size, and cost.

In general, inductance is designed to let the ripple current ranges between 20% to 40% of the full load current. The inductance can be calculated using the following equation:

$$L_{min} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_rated}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between the inductor ripple current and the rated output current.

16.26 Input Capacitor Selection

The voltage rating and current rating are the key parameters in selecting an input capacitor. Generally, the input capacitor voltage rating should be 1.5 times greater than the maximum input voltage for a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for the RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing a ceramic capacitor close to the drain of the high-side MOSFET is helpful in reducing the input voltage ripple at heavy load.

16.27 Output Capacitor Selection

The output filter capacitor must have an ESR low enough to meet the output ripple and load transient requirements, yet have a high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full load to no load condition without triggering the OVP circuit. Organic semiconductor capacitor(s) or special polymer capacitor(s) are recommended.

16.28 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 105°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-20L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board.

The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (105°C - 25°C) / (30°C/W) = 2.67W for a WQFN-20L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 13 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.
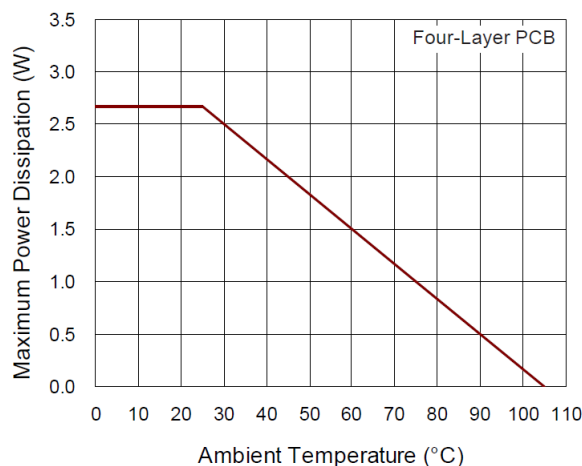
Figure 13. Derating Curve of Maximum Power Dissipation

16.29 Layout Considerations

Layout is very important in high-frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to the converter instability. The following layout guidelines must be considered before starting a layout for the RT8816A.

- ▶ Place the RC filter as close as possible to the PVCC pin.
- ▶ Keep the current-limit setting network as close as possible to the IC. The routing of the network should avoid coupling to the high voltage switching node.
- ▶ Connections from the drivers to the respective gates of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.
- ▶ All sensitive analog traces and components such as VSNS, RGND, EN, PSI, VID, PGOOD, VREF, TON, REFADJ, and REFIN should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- ▶ Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the IC power ground connections). Power components should be placed to minimize loops and reduce losses.

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension

DETAIL A

Pin #1 ID and Tie Bar Mark Options
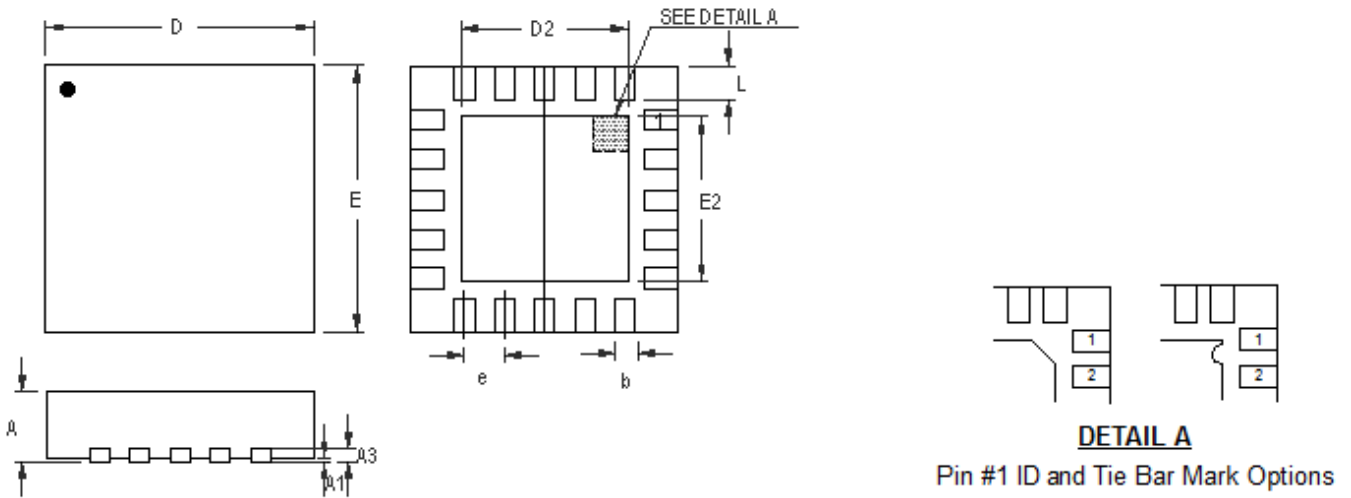
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

18 Footprint Information
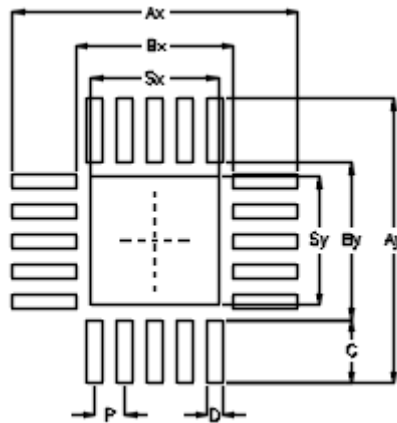
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-20	20	0.40	3.80	3.80	2.10	2.10	0.85	0.20	1.70	1.70	±0.05

19 Packing Information

19.1   Tape and Reel Data
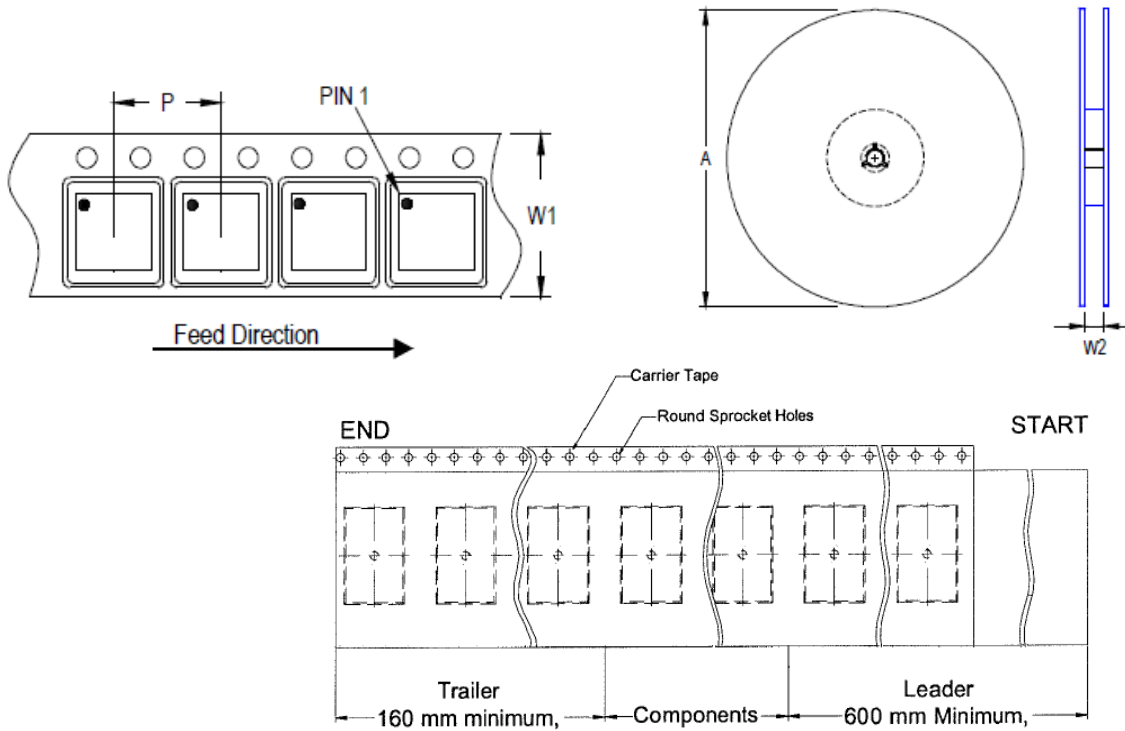
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4
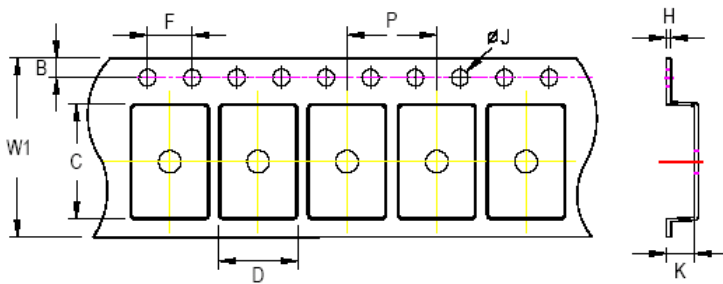
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7"	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7"	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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20 Datasheet Revision History

Version	Date	Description	Item
00	2024/2/23	Modify	*General Description on page 1* *Ordering Information on page 2* *Electrical Characteristics on page 9, 10* *Application Information on page 16* *Footprint Information on page 29* *Packing Information on page 30, 31, 32*
01	2024/5/7	Modify	*Ordering Information on page 2* *Functional Pin Description on page 4* *Typical Application Circuit on page 10* *Application Information on page 18, 26* *Packing Information on page 30*
02	2025/1/3	Modify	*Application Information on page 19* *Packing Information on page 29, 30*

DS8816A-10 January 2025