RICHTEK®

RT8250

3A, 23V, 340kHz Synchronous Step-Down Converter

1 General Description

The RT8250 is a high-efficiency synchronous step-down converter that can deliver up to 3A output current from a 4.5V to 23V input supply. The RT8250's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitors. Cycle-by-cycle current-limit protection protects against shorted outputs, and soft-start eliminates input current surges during start-up. The RT8250 also provides output undervoltage protection and over-temperature protection. The low current (<3μA) shutdown mode provides output disconnection, enabling easy power management in battery-powered systems. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT8250 □□

Package Type(1)
SP: SOP-8 (Exposed Pad)
(Exposed Pad: Option 1)

Lead Plating System
G: Richtek Green Policy Compliant(2)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **4.5V to 23V Input Voltage Range**
- **1.5% High Accuracy Feedback Voltage**
- **3A Output Current**
- **Integrated N-MOSFET Switches**
- **Current Mode Control**
- **Fixed Frequency Operation: 340kHz**
- **Output Adjustable from 0.925V to 20V**
- **Up to 95% Efficiency**
- **Programmable Soft-Start Time**
- **Stable with Low-ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Current-Limit Protection**
- **Input Undervoltage-Lockout**
- **Output Undervoltage Protection**
- **Over-Temperature Protection**
- **Thermally Enhanced SOP-8 (Exposed Pad) Package**

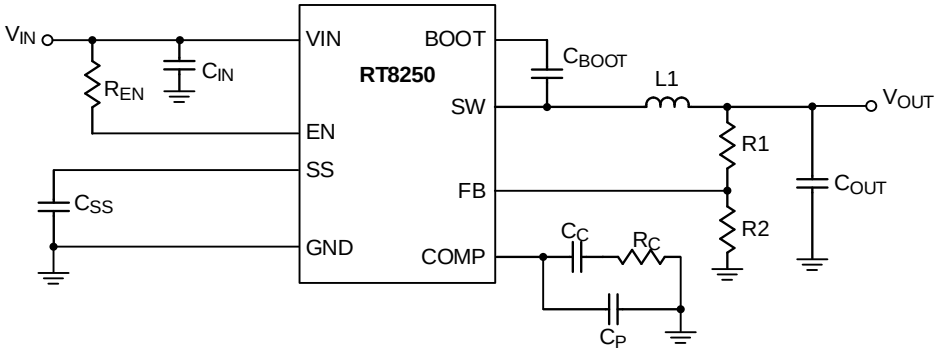
4 Applications

- Automotive Infotainment Displays
- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation of High-Performance DSPs, FPGAs, and ASICs.

5 Marking Information

RT8250GSP: Product Code
YMDNN: Date Code

6 Simplified Application Circuit



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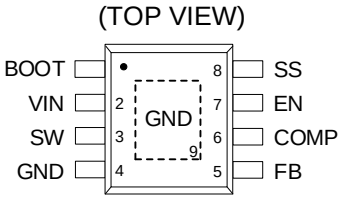
7 Pin Configuration

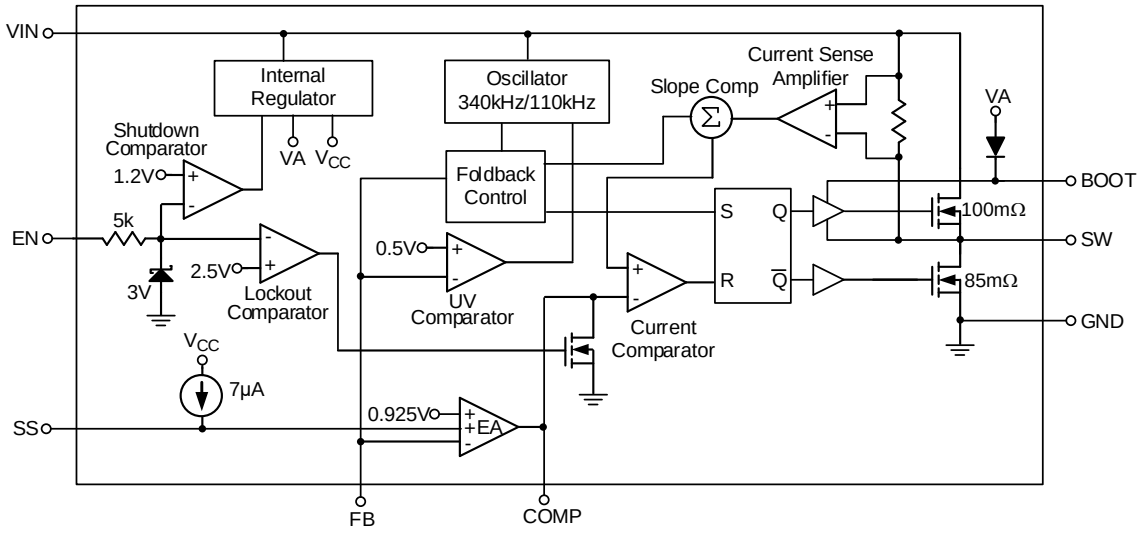


SOP-8 (Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap, supply for high-side gate driver. Connect a 10nF ceramic capacitor between the BOOT and SW pins.
2	VIN	Input voltage. Support 4.5V to 23V input voltage. It is recommended to place equal-value input capacitors on each side of the IC and as close to the VIN and PGND pins as possible.
3	SW	Switch node. Connect to the power inductor. Return path for the internal high-side MOSFET gate driver bootstrap capacitor. Connect a capacitor from BOOT to this pin.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	FB	Feedback input. The pin is used to set the output voltage of the converter via a resistor divider. It is recommended to place the FB resistor divider as close to the FB pin and GND as possible.
6	COMP	Compensation Node. This pin is used for compensating the regulation control loop. A series RC network is required to be connected from COMP to GND. If needed, an additional capacitor should be connected from COMP to GND.
7	EN	Enable Input. A logic high enables the converter, while a logic low forces the converter into shutdown mode, reducing the supply current to less than 3μA. For automatic startup, connect this pin to VIN with a 100kΩ pull-up resistor.
8	SS	Soft-Start Control Input. The soft-start period can be set by connecting a capacitor from SS to GND. A 0.1μF capacitor typically sets the soft-start period to 13ms.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN ---------- –0.3V to 24V
- Switching Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
  <20ns ---------- –0.3V to (V_{IN} + 3V)
- BOOT Voltage ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- The Other Pins ---------- VIN – 7.2V to VIN
- All other pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 3)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 28°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Mode) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 4.5V to 23V
- Enable Voltage, EN ---------- 0V to 5.5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.3	3	μA
Supply Current	I_Q	V_{EN} = 3 V, V_{FB} = 1V	--	0.7	1.2	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	0.911	0.925	0.939	V
Error Amplifier Transconductance	gm	ΔIC = ±10μA	--	1250	--	μA/V
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	100	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	85	--	mΩ
High-Side Switch Leakage Current	I_{LK_H}	V_{EN} = 0V, V_{SW} = 0V	--	0	10	μA
High-Side Switch Current Limit	I_{LIM_H}	Min. Duty Cycle V_{BOOT} – V_{SW} = 4.8V	--	5.5	--	A
Low-Side Switch Current Limit	I_{LIM_L}	From Drain to Source	--	1.4	--	A
COMP to Current Sense Transconductance	G_{CS}		--	5.2	--	A/V
Oscillation Frequency	f_{OSC1}		300	340	380	kHz
Short Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V	--	110	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.8V	--	90	--	%
Minimum On-Time	t_{ON_MIN}		--	200	--	ns
EN Input Voltage Rising Threshold	V_{EN_R}		2.7	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	V_{IN} Rising	3.8	4.2	4.4	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}		--	200	--	mV
Soft-Start Current	I_{SS}	V_{SS} = 0V	--	7	--	μA
Soft-Start Time	t_{SS}	C_{SS} = 0.1μF	--	13	--	ms
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C

13 Typical Application Circuit

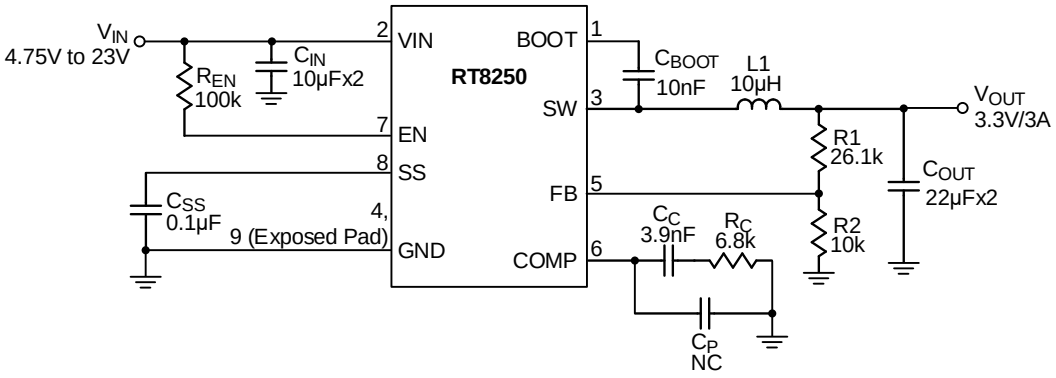
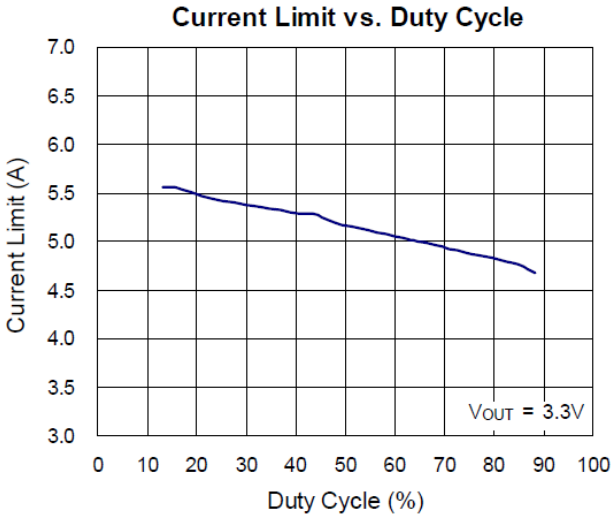
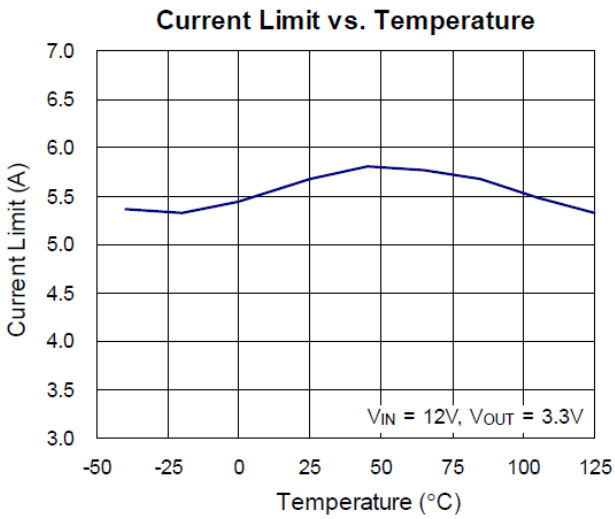


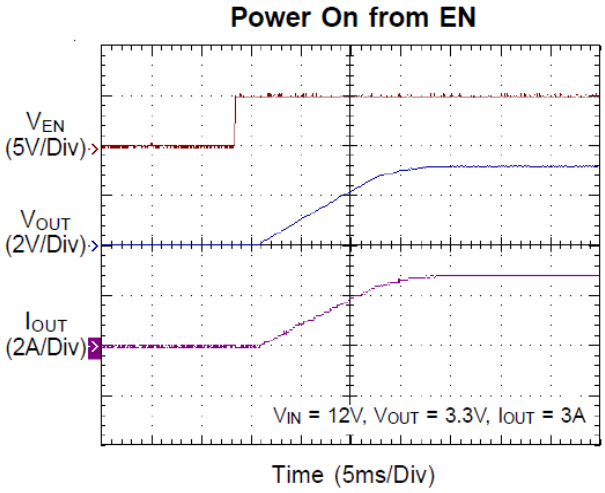
Table 1. Recommended Component Selection

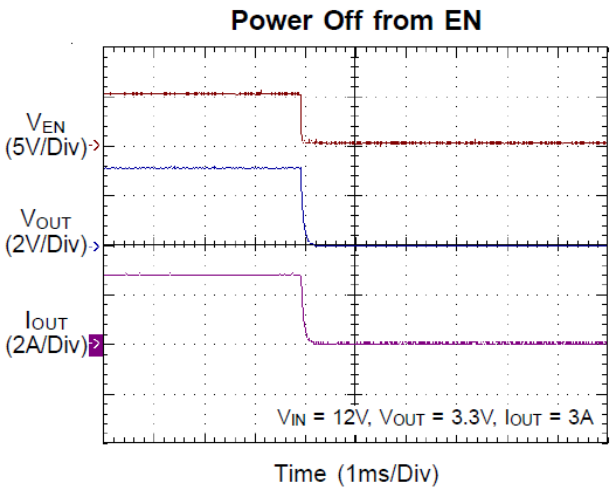
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L (µH)	C_{OUT} (µF)
15	153	10	30	3.9	33	22 x 2
10	97.6	10	20	3.9	22	22 x 2
8	76.8	10	15	3.9	22	22 x 2
5	45.3	10	13	3.9	15	22 x 2
3.3	26.1	10	6.8	3.9	10	22 x 2
2.5	16.9	10	6.2	3.9	6.8	22 x 2
1.8	9.53	10	4.3	3.9	4.7	22 x 2
1.2	3	10	3	3.9	3.6	22 x 2

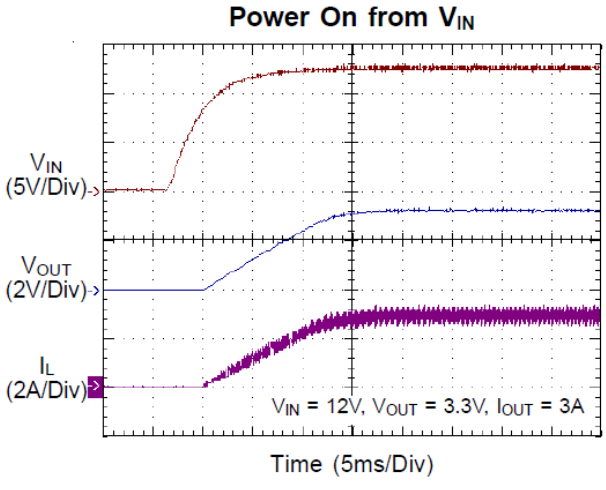
14 Typical Operating Characteristics

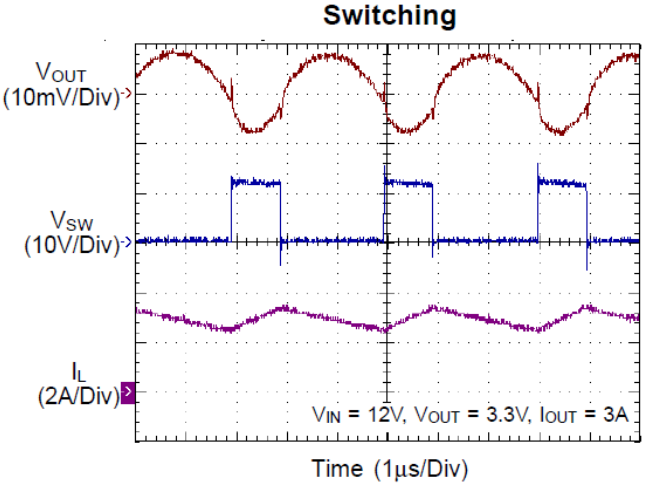




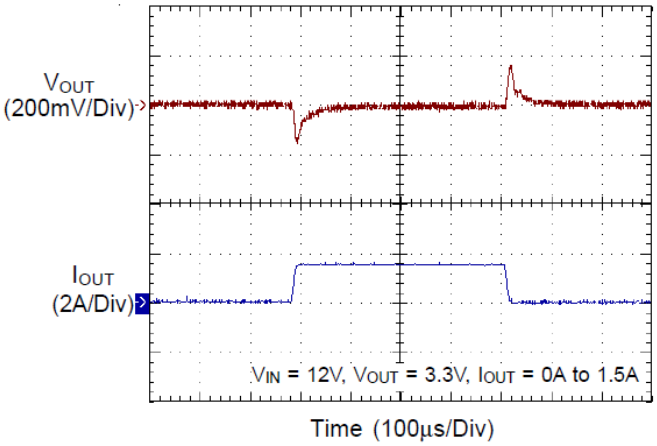




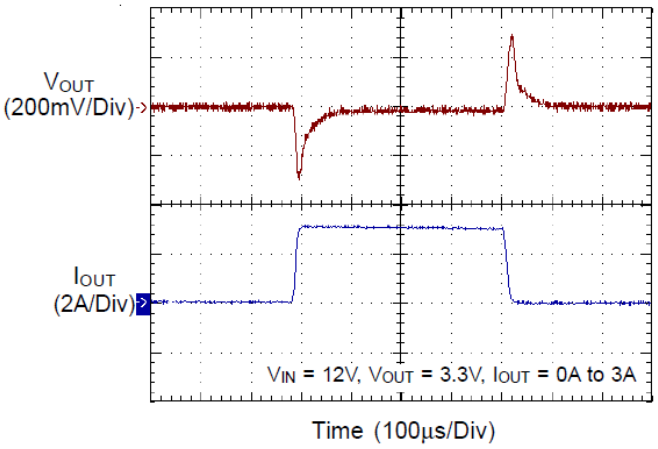




Load Transient Response



Load Transient Response



15 Application Information

(Note 6)

The RT8250 is a synchronous high-voltage converter that supports an input voltage range from 4.5V to 23V, and an output current of up to 3A.

15.1 Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage, as shown in Figure 1.

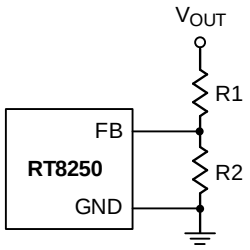


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive divider according to the following equation:

$$V_{FB} = (1 + \frac{R1}{R2})$$

where V_{FB} is the feedback voltage (0.925 V typical).

15.2 External Bootstrap Diode

Connect a 10nF low ESR ceramic capacitor between the BOOT pin and the SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET. It is recommended to add an external bootstrap diode between an external 5V supply and the BOOT pin for efficiency improvement when the input voltage is lower than 5.5V, or the duty ratio is higher than 65%. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a 5V fixed input from the system or a 5V output of the RT8250. Note that the external boot voltage must be lower than 5.5V.

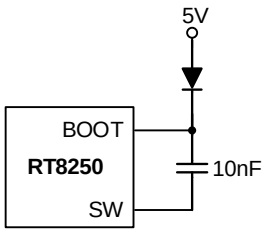


Figure 2. External Bootstrap Diode

15.3 Soft-Start

The RT8250 contains an external soft-start clamp that gradually increases the output voltage. The soft-start timing can be programmed using the external capacitor between the SS pin and GND. The chip provides a 7μA charge current for the external capacitor. If a 0.1μF capacitor is used to set the soft-start, the period will be 13ms (typical).

15.4 Inductor Selection

The inductor value and operating frequency determine the ripple current according to the specific input and output voltage. The ripple current (ΔI_L) increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = [\frac{V_{OUT}}{f \times L}] \times [1 - \frac{V_{OUT}}{V_{IN}}]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For ripple current selection, a value of ΔI_L = 0.2375 × I_{MAX} is a reasonable starting point. The largest ripple current occurs at the highest VIN. To ensure that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}] \times [1 - \frac{V_{OUT}}{V_{IN(MAX)}}]$$

15.5 Inductor Core Selection

The type of the inductor must be selected once the value for L is determined. Generally, high-efficiency converters cannot afford the core loss found in low-cost powdered iron cores. Therefore, more expensive ferrite or mollypermalloy cores will be a better choice.

The selected inductance, rather than the core size for a fixed inductor value, is the key for actual core loss. As the inductance increases, core losses decrease. Unfortunately, increasing the inductance requires more turns of wire, and therefore the copper losses will increase.

Ferrite designs are preferred at high switching frequencies due to their very low core losses. Therefore, design goals can focus on reducing copper loss and preventing of saturation.

Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This situation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy. However, they are usually more expensive than similar powdered iron inductors.

The rule for inductor choice mainly depends on the price versus size requirement and any radiated field/EMI requirements.

15.6 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor with a higher temperature rating than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 10µF x 2 low ESR ceramic capacitor is recommended. For the recommended capacitor, refer to Table 3 for more details. The selection of C_{OUT} is determined by the required

ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response, as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \times [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple will be highest at the maximum input voltage since ΔIL increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR values. However, they provide lower capacitance density than other types. Although tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, they can be used in cost-sensitive applications for ripple current rating and long-term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors, combined with trace inductance, can also lead to significant ringing.

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken for loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

15.7 Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators require several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}(ESR). This also begins to charge or discharge C_{OUT}, generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing, which may indicate a stability issue.

15.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for a SOP-8 (Exposed Pad) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

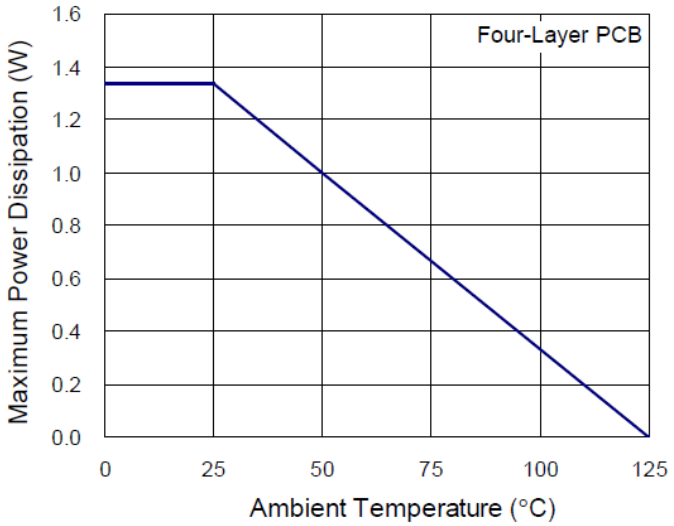


Figure 3. Derating Curve of Maximum Power Dissipation

15.9 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8250.

- Keep the traces of the main current paths as short and wide as possible.
- Place the input capacitor as close as possible to the device pins (VIN and GND).
- The SW node has a high-frequency voltage swing and should be kept to a small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- Place the feedback components as close as possible to the FB pin and COMP pin.
- The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

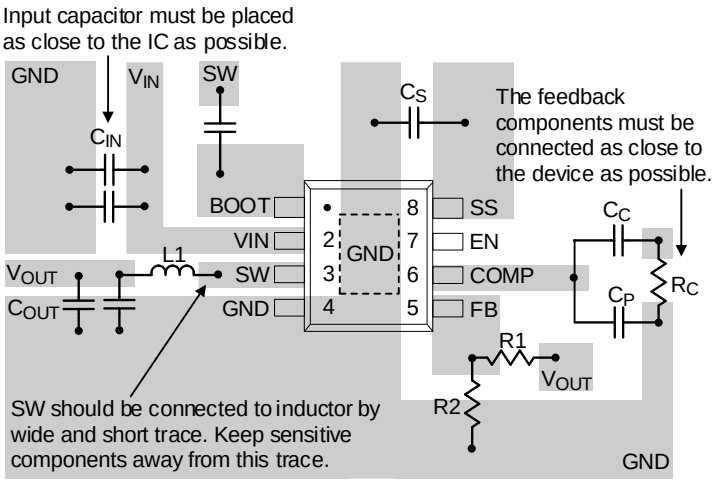


Figure 4. PCB Layout Guide

Table 2. Suggested Inductors for Typical Application Circuit

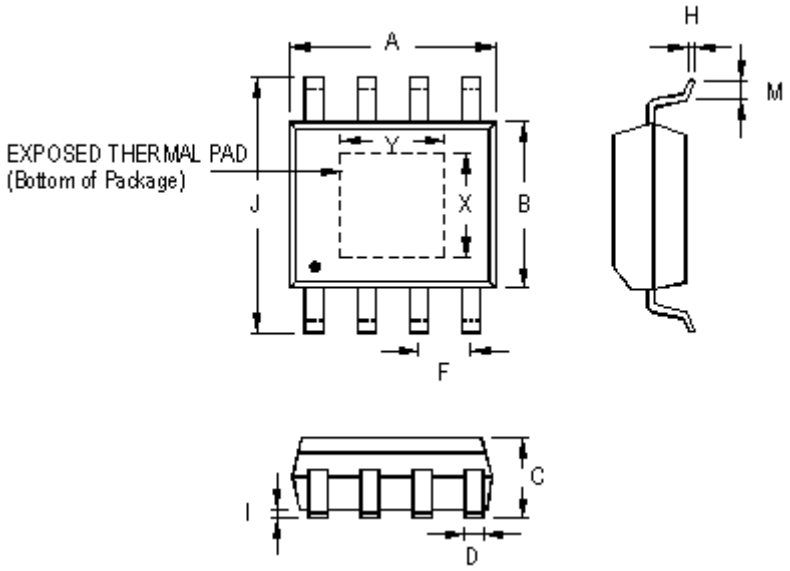
Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TAIYO YUDEN	NR8040	8x8x4

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
MURATA	GRM31CR61E106K	10	1206
TDK	C3225X5R1E106K	10	1206
TAIYO YUDEN	TMK316BJ106ML	10	1206
MURATA	GRM31CR60J476M	47	1206
TDK	C3225X5R0J476M	47	1210
TAIYO YUDEN	EMK325BJ476MM	47	1210
MURATA	GRM32ER71C226M	22	1210
TDK	C3225X5R1C226M	22	1210

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

16 Outline Dimension

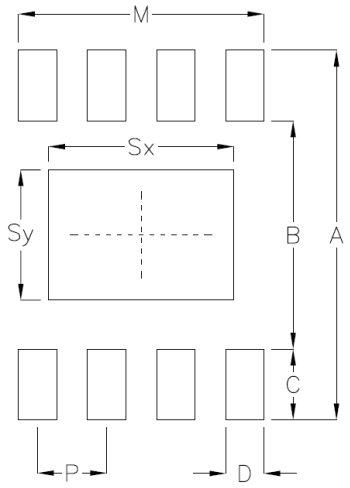


Symbol		Dimensions In		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 7. The package of the RT8250 uses Option 1.

17 Footprint Information

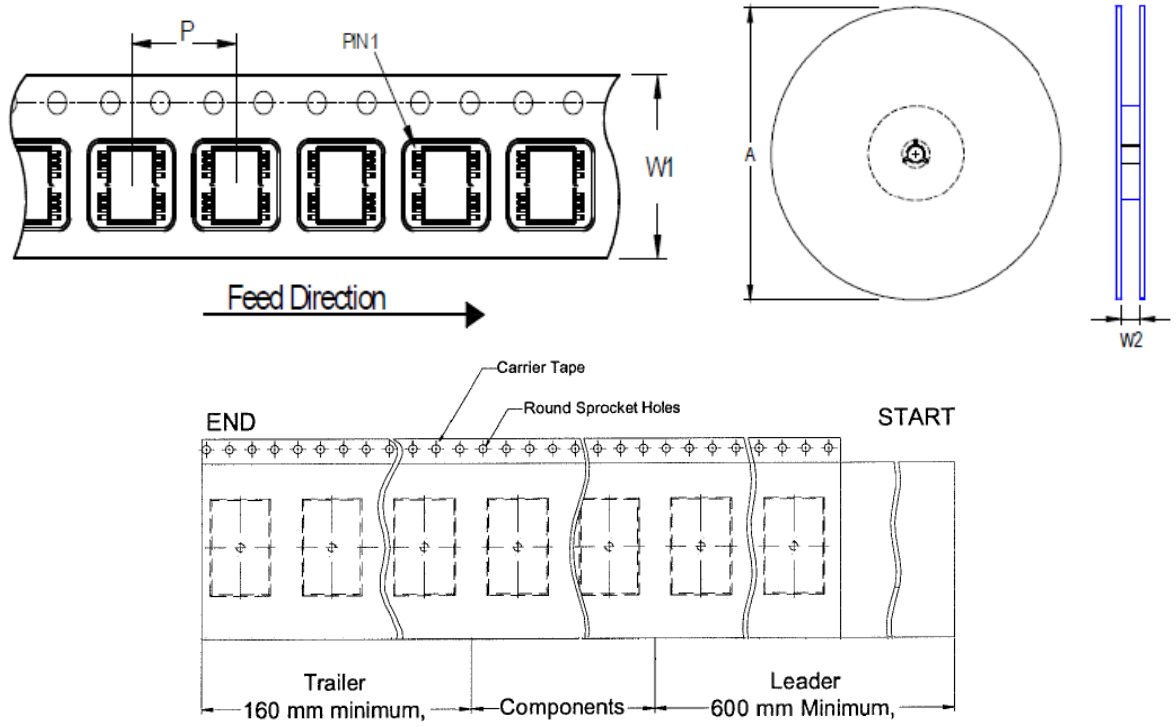


Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

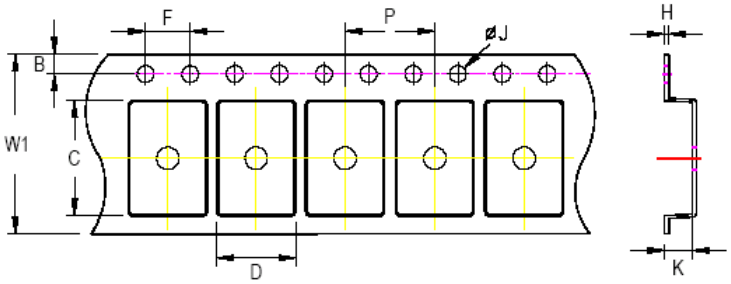
Note 8. The package of the RT8250 uses Option 1.

18 Packing Information

18.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
06	2024/12/12	Modify	*General Description on page 1* *Features on page 1* *Ordering Information on page 1* *Simplified Application Circuit on page 1* - Added Simplified Application Circuit *Functional Pin Description on page 3* *Electrical Characteristics on page 5* *Application Information on page 9 to 13* *Footprint Information on page 15* - Added Footprint Information *Packing Information on page 16, 17, 18* - Added packing information