5V to 12V Single Synchronous Buck PWM Controller

General Description

The RT8124A is a single-phase synchronous buck PWM DC-DC controllers designed to drive two N-MOSFETs. It provides a highly accurate, programmable output voltage precisely regulated to low voltage requirement with an internal 0.6V reference.

The RT8124A uses a single feedback loop voltage mode PWM control for fast transient response. The high driving capability makes it suitable for large output current applications. An oscillator with fixed frequency 300kHz reduces the component size of the external inductor and capacitor for saving PCB board area and cost.

The RT8124A integrates complete protection functions such as OCP, OVP and OTP UVP into a WDFN-10L 3x3 package.

Ordering Information

RT8124A□□

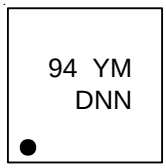
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



94 : Product Code

YMDNN : Date Code

Features

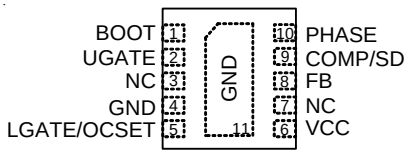
- **Single IC Supply Voltage (5V to 12V)**
- **Drive Two N-MOSFETs**
- **Fixed Operating Frequency at 300kHz**
- **Voltage Mode PWM Control with External Feedback Loop Compensation**
- **Over Current Protection by Sensing MOSFET $R_{DS(ON)}$**
- **Hardware Pin for On/Off Control**
- **Full 0 to 90% Duty Cycle**
- **Fast Transient Response**
- **RoHS Compliant and Halogen Free**

Applications

- Mother Boards and Desktop Servers
- Graphic Cards
- Switching Power Supply
- Generic DC/DC Power Regulator

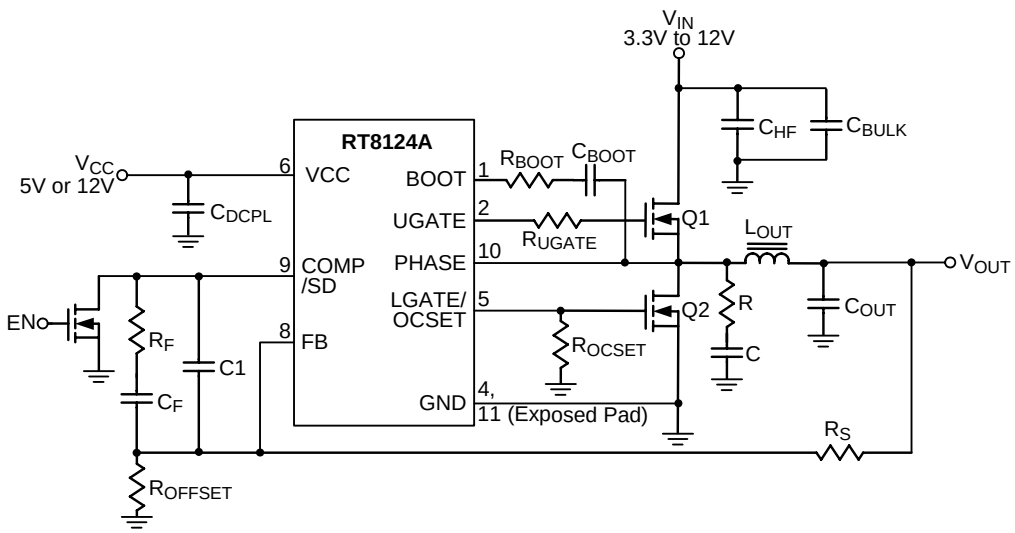
Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

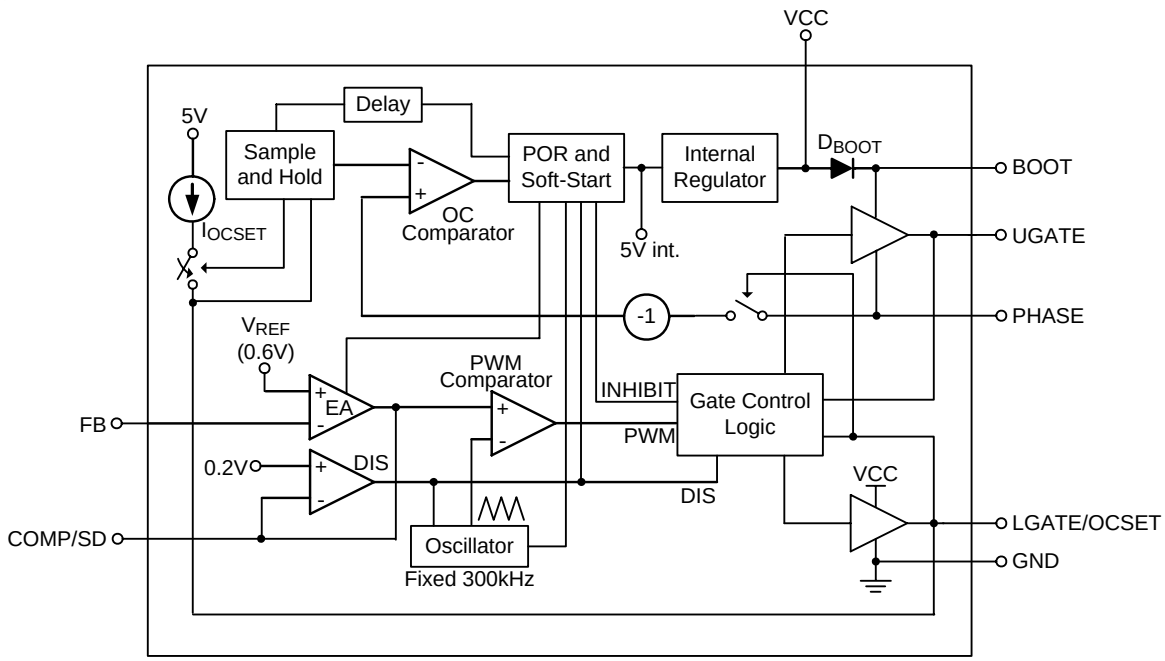
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap Supply Pin for the Upper Gate Driver. Connect the bootstrap capacitor between BOOT and PHASE pins.
2	UGATE	Upper Gate Driver Output. Connect this pin to gate of the high side power N-MOSFET.
3, 7	NC	No Internal Connection.
4, 11 (Exposed Pad)	GND	Both Signal and Power Ground for the IC. Tie this pin directly to the low side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	LGATE/OCSET	Low Side Gate Drive. It also acts as over current setup pin by adjusting the resistor connecting to GND.
6	VCC	Connect this Pin to a Well-Decoupled 5V or 12V Bias Supply. It is also the positive supply for the lower gate driver.
8	FB	Feedback of the Output Voltage.
9	COMP/SD	Feedback Compensation and Enable/Shutdown Control Pin.
10	PHASE	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC} ---------- 16V
- BOOT to PHASE ---------- 15V
- PHASE to GND
  - DC ---------- –0.5V to 15V
  - <20ns ---------- –5V to 30V
- UGATE Voltage ---------- (V_{PHASE} – 0.3V) to (V_{BOOT} + 0.3V)
  - <20ns ---------- (V_{PHASE} – 5V) to (V_{BOOT} + 5V)
- LGATE Voltage ---------- (GND – 0.3V) to (V_{CC} + 0.3V)
  - <20ns ---------- (GND – 5V) to (V_{CC} + 5V)
- Other Input or Output Voltages ---------- (GND – 0.3V) to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{CC} ---------- 5V ± 5%, 12V ± 10%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Voltage	V_{CC}		4.75	--	13.2	V
Supply Current	I_{CC}	UGATE, LGATE Open	--	2.5	10	mA
Shutdown Current	I_{SHDN}	UGATE, LGATE Open	--	2	--	mA
Power-On Reset (POR)						
POR Threshold	V_{CC_RTH}	V_{CC} Rising	3.8	4	4.3	V
Power On Reset Hysteresis	V_{CC_HYS}		--	0.4	--	V
Oscillator						
PWM Frequency	F_{SW}		250	300	350	kHz
Ramp Amplitude	ΔV_{OSC}		--	1.5	--	V_{P-P}

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference						
Reference Voltage	V_{REF}		0.594	0.6	0.606	V
PWM Controller						
Open Loop DC Gain	A_O		--	88	--	dB
Gain Bandwidth	GBW		--	15	--	MHz
Maximum Duty	D_{MAX}		--	90	--	%
PWM Controller Gate Driver						
Upper Gate Source	$I_{UGATEsr}$	$V_{BOOT} - V_{PHASE}$ = 12V	1	1.2	--	A
Upper Gate Sink	$R_{UGATEsk}$	$V_{UGATE} - V_{PHASE}$ = 0.1V, I = 50mA	--	2.25	4	Ω
Lower Gate Source	$I_{LGATEsr}$		1	1.2	--	A
Lower Gate Sink	$R_{LGATEsk}$	V_{LGATE} = 0.1V, I = 50mA	--	1	2	Ω
Protection						
Under Voltage Protection (UVP)	V_{FB_UVP}	Sweep V_{FB}	68	75	82	%
Over Voltage Protection	V_{FB_OVP}	Sweep V_{FB} (After POR)	115	125	130	%
Over Voltage Protection	V_{pre_OVP}	Sweep V_{FB} (Before POR)	--	130	--	%
LGATE OC Setting Current	I_{OCSET}		22	25	28	μA
Over Temperature Protection	T_{OTP}		--	165	--	°C
Soft-Start Interval	T_{SS}	Measure FB from 10% to 90%	1	3	5	ms
COMP/SD Shutdown Threshold	V_{SD}		--	--	0.2	V

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

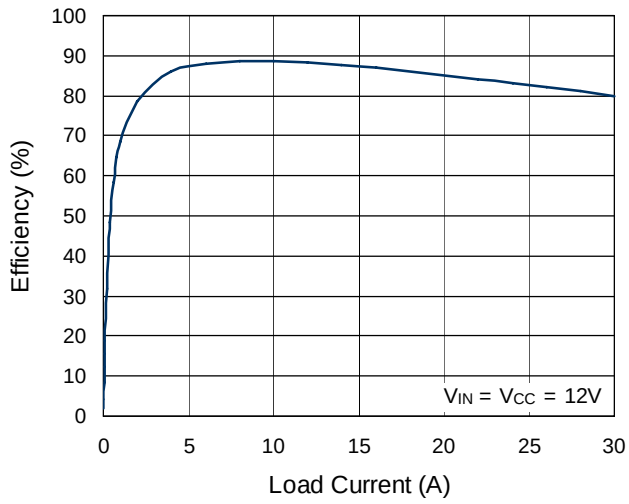
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

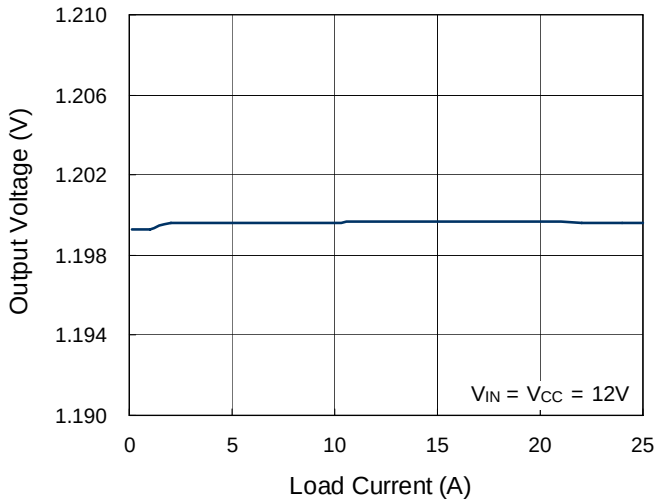
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

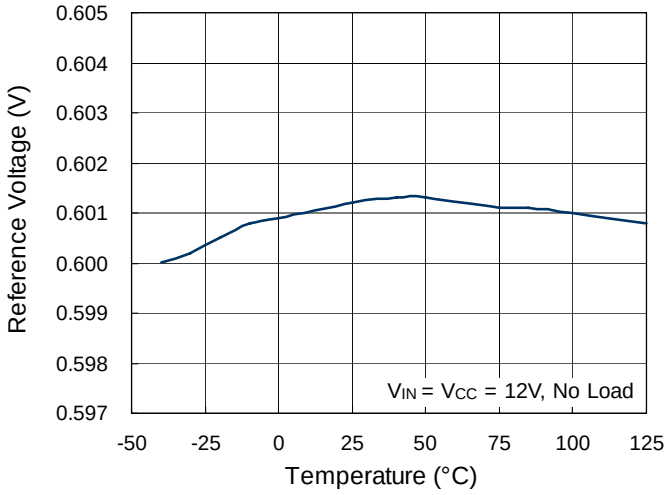
Efficiency vs. Load Current



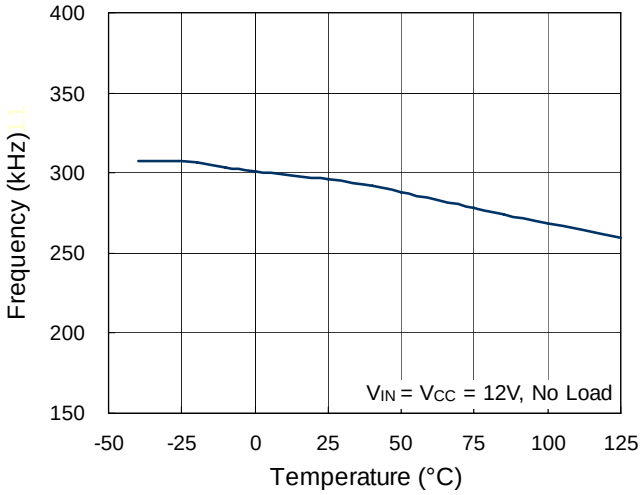
Output Voltage vs. Load Current



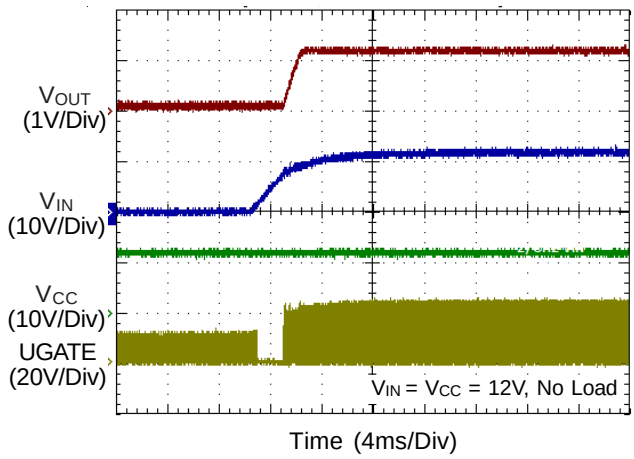
Reference Voltage vs. Temperature



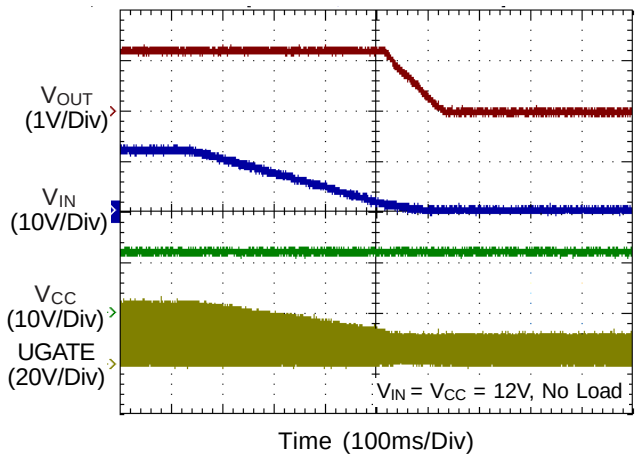
Frequency vs. Temperature



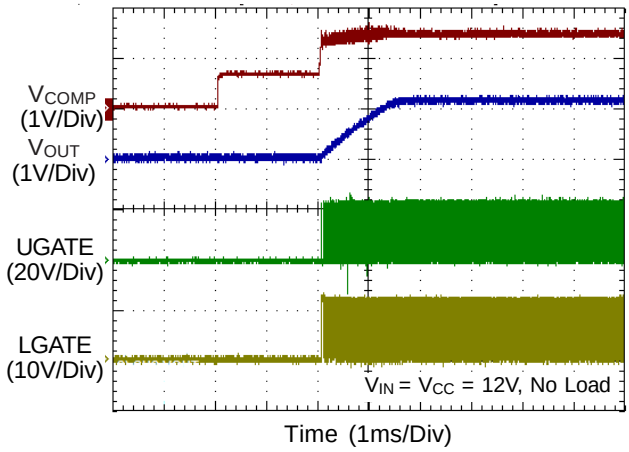
Power On from V_{IN}



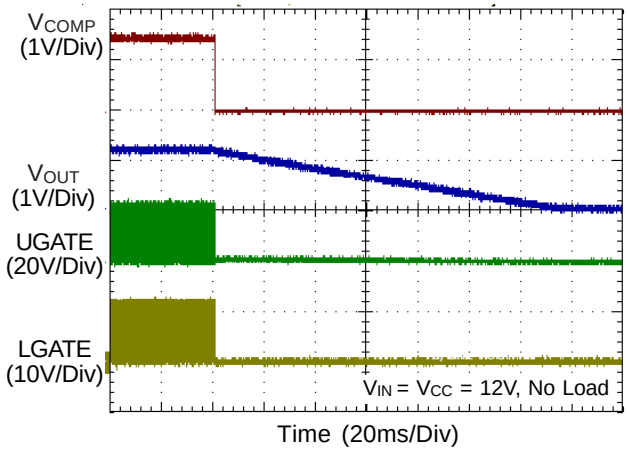
Power Off from V_{IN}



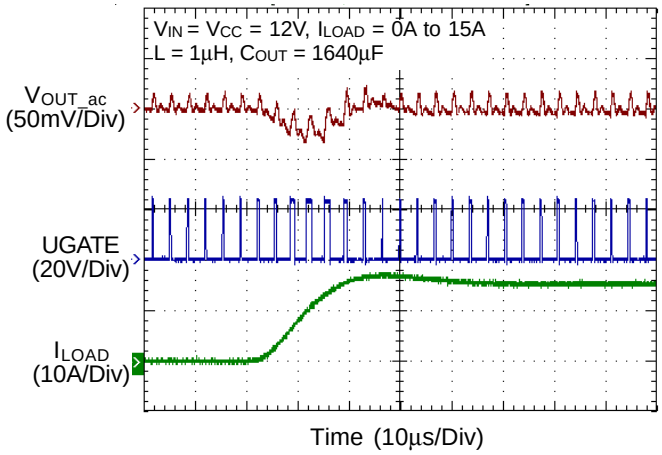
Power On from COMP/SD



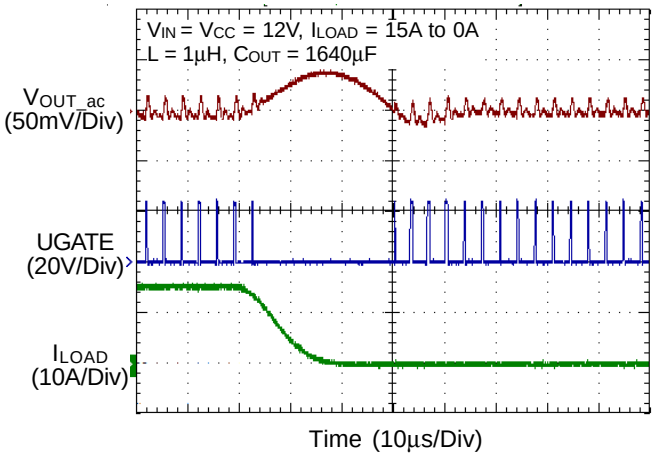
Power Off from COMP/SD



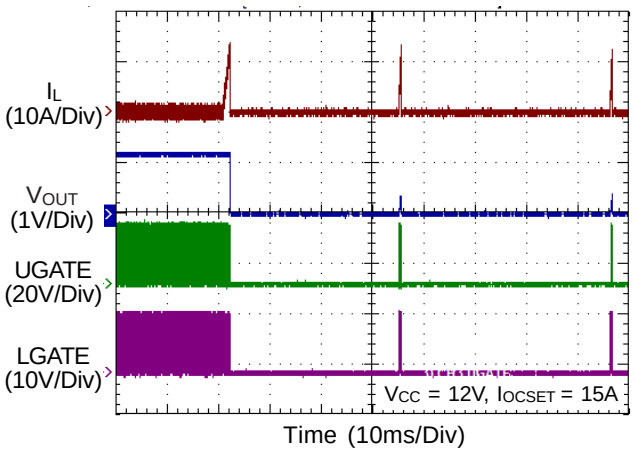
Load Transient Response



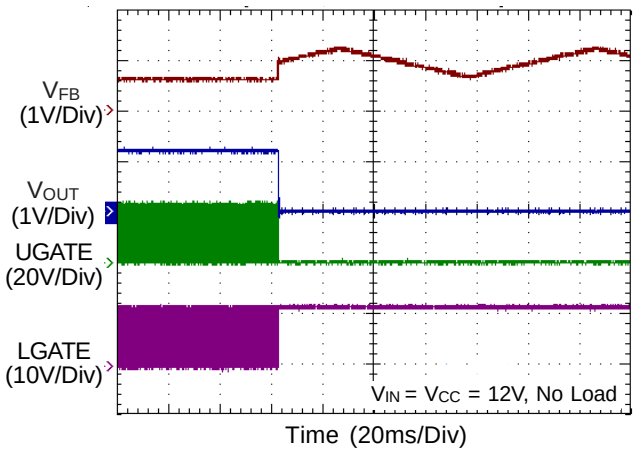
Load Transient Response



Over Current Protection



Over Voltage Protection



Application Information

Function Description

The RT8124A is a single-phase synchronous buck PWM controllers with embedded MOSFET drivers. The MOSFET drivers are designed with high-current driving capability to support up to 12V + 12V bootstrapped voltage for high efficiency power conversion. The RT8124A utilizes voltage mode control scheme, which is implemented with a voltage error amplifier to provide a simple control loop. A fixed frequency oscillator (300kHz, typical) is integrated to eliminate external component count. The soft-start function is also integrated to eliminate the external timing capacitor. The RT8124A provides full protection functions to protect the load. The feedback voltage at the FB pin is monitored for over voltage protection and under voltage protection. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. An elaborately designed control circuit allows the converter to power up with pre-biased output voltage to avoid negative voltage damage to the load. The RT8124A uses $R_{DS(ON)}$ current sensing technique, which is lossless and cost effective. Inductor current information is monitored by the voltage across $R_{DS(ON)}$ of the low side MOSFET for over current protection.

Power Up

The Power On Reset (POR) circuit monitors the supply voltage of the controller (VCC). If VCC exceeds the POR rising threshold voltage, the controller is initiated. The controller sets the over current protection threshold prior to the beginning of soft start. If VCC falls below the POR falling threshold during normal operation, all MOSFETs stop switching and the controller is reset. The POR rising and falling threshold has a hysteresis to prevent noise-caused reset.

Soft-Start

The RT8124A provides soft-start function internally. The soft-start function is used to prevent the large inrush current while the converter is powered-up. An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up in a monotone. The FB voltage will track the internal soft-start voltage during the soft-start interval. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but follows the reference voltage. Therefore, the duty cycle of the UGATE signal at power up is limited and so does the input current.

Power Up with Pre-biased Voltage

Generally, if the output voltage is not initially zero at power up, or the output capacitor is pre-charged, the voltage at FB pin is not equal to zero. The controller will turn on the low side MOSFET to discharge the output capacitor, forcing the feedback voltage to follow the reference voltage. Large current is then drawn from the output capacitor while discharging. The discharge current depends on the inductance and the output capacitance. Output voltage may oscillate and be negative.

The negative output voltage could damage the load. The RT8124A implements elaborate control circuits to prevent the negative voltage when the converter is powered-up with pre-biased voltage on the output capacitor. Figure 1 shows the waveform that converter is powered-up at no load with pre-biased output voltage. The output voltage rises from its pre-charged initial value during soft-start without being pulled down.

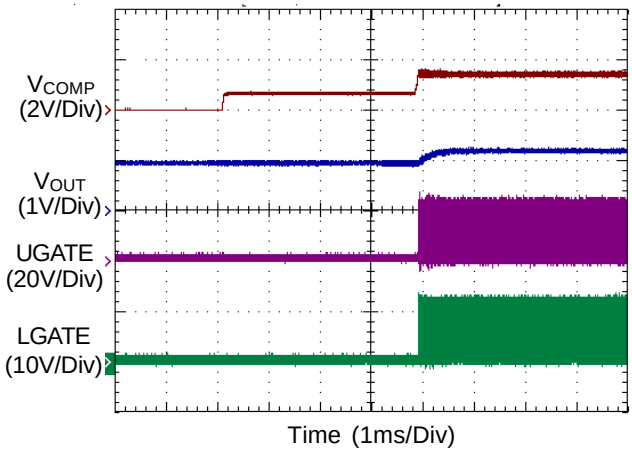


Figure 1. Power Up with Pre-Biased Output Voltage

COMP/SD Enable/Disable

The COMP/SD pin can also be used to enable or to disable the controller. Pull down COMP/SD pin below the shutdown level V_{SHDN} can disable the controller. When the controller

is disabled, UGATE signal goes low first and then LGATE signal also goes low after a short delay time. In practical applications, connect a small signal MOFSET to COMP/SD pin to pull down the COMP/SD voltage to implement the enable/disable function.

Over Voltage Protection (OVP)

The output voltage is scaled by the divider resistors and fed back to the FB pin. The voltage on the FB pin will be compared to the internal reference voltage V_{REF} for voltage-related protection functions, including over voltage protection and under voltage protection. If the FB voltage is higher than the OVP threshold during operation, OVP will be triggered. When OVP is triggered, UGATE will go low and LGATE will go high to discharge the output capacitor. Once OVP is triggered, controller will be latched unless VCC POR is detected again.

Besides, the also provides OVP even if VCC is below the POR threshold. This can protect the load even if the high-side MOSFET is shorted before the power-on-reset. If the FB voltage is higher than the OVP threshold while VCC rises but not exceeds the POR threshold, OVP will be triggered. The LGATE signal will go high to discharge the output capacitor.

Under Voltage Protection (UVP)

The voltage on the FB pin is also monitored for under voltage protection. If the FB voltage is lower than the UVP threshold during normal operation, UVP will be triggered. When UVP is triggered, both UGATE and LGATE go low. Unlike OVP, UVP is not a latched protection. The controller will begin soft start again after a specific period of time (~40ms). Furthermore, the controller will enter the hiccup mode and always try to restart if UVP situation is not removed. The UVP is reset by detecting VCC POR again. Unlike OVP, the output voltage is monitored for UVP only after soft-start completes.

Over Current Protection (OCP)

The senses output current through low side MOSFET $R_{DS(ON)}$ for over current protection. When the LGATE is turned on, the controller monitors voltage across the low side MOSFET. The lossless $R_{DS(ON)}$ current sensing technique is cost-effective, because no external component is required. The utilizes cycle-by-cycle peak current sensing, the voltage across the low side MOSFET is sampled and held after low side MOSFET is turned on. This sampled and held voltage represents the inductor peak current and is compared to the user-programmed protection level.

Once the inductor current exceeds the protection level, OCP will be triggered. When the OCP is triggered, both UGATE and LGATE go low to stop the energy transferring to the load. Like UVP, the OCP is a continuing hiccupped protection. The soft start will be initiated again after a specific period of time (4*Tss, typical). If OCP situation is not removed, controller will always try to restart.

OCP Setting

The employs an elaborate topology for OCP setting, which eliminates controller pin count. Connect a resistor from LGATE to GND to set the OCP level as shown in Figure 2.

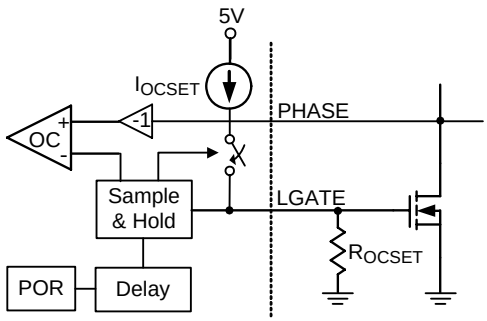


Figure 2. OCP Setting

When the V_{CC} exceeds the POR threshold at power up, LGATE is internally floating and enters tri-state. An internal current source I_{OCSET} then flows through R_{OCSET} to determine the OCP threshold voltage. The voltage across the R_{OCSET} is stored as the over current level for OCP. After that, the current source is switched off, and LGATE leaves the tri-state and prepared for the soft-start. Therefore, no extra pin is required to set the OCP threshold. The internal current source I_{OC} is only active for a short period of time after V_{CC} POR. The R_{OCSET} can be determined using the following equation.

$$R_{OCSET} = \frac{R_{DS(ON)} \times I_{MAX}}{2 \times I_{OCSET}}$$

where I_{OCSET} is 25μA (typical), I_{MAX} represents the allowed maximum inductor peak current.

MOSFET Drivers

The RT8124A integrate high current gate drivers for MOSFETs to obtain high efficiency power conversion in synchronous buck topology. A dead time is used to prevent the crossover conduction for the high side and low side MOSFETs. Because both the two gate signals are off during the dead time, the inductor current freewheels through the body diode of the low side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to the power loss. The employs a constant dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, an elaborate logic circuit is implemented to prevent the cross-conduction between MOSFETs.

For high output current applications, two or more power MOSFETs are paralleled to have reduced $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/ sink current capability results in longer rising/ falling time in gate signals, and therefore the higher switching loss.

The employs embedded high current gate drivers to obtain high efficiency power conversion. The embedded drivers contribute to the majority of the controller power dissipation. If no gate resistor is used, the power dissipation of the controller can be approximately calculated using the following equation.

$$P_{SW} = F_{SW} \times (Q_{g\_High\ Side} \times V_{BOOT} + Q_{g\_Low\ Side} \times V_{Drive\_Low\ Side})$$

where V_{BOOT} represents the voltage across the bootstrap capacitor.

It is important to ensure the package can dissipate the switching loss and have enough room for safe operation.

Inductor Selection

Inductor plays an importance role in the buck converter because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of inductor should be as small as possible because inductor carries current all the time. Using inductor that has lower DCR can obtain higher efficiency. In addition, because inductor cost most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation.

Additionally, larger inductance results in lower ripple current, and therefore the lower power loss. However, the inductor current rising time increases with inductance value. This means the inductor will have a longer charging time before its current reaches the required output current. Since the response time is increased, the transient response performance will be decreased. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is designed such that the ripple current ranges between 20% to 30% of full load current. The inductance can be calculated using the following equation.

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is 0.2 to 0.3.

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitor. The voltage rating must be 1.25 times greater than the maximum input voltage to ensure enough room for safe operation. Generally, input capacitor has a voltage rating of 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Refer to the manufacturer's databook for RMS current rating to select proper capacitor. Use more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is popular. Besides, placing ceramic capacitor close to the drain of the high side MOSFET is helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the buck topology. The electrolytic capacitor is usually used because it can provide large capacitance value.

In steady state condition, the output capacitor supplies only AC ripple current to the load. The ripple current flows into/out of the capacitor results in ripple voltage, which can be determined using the following equation.

$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$

In addition, the output voltage ripple is also influenced by the switching frequency and the capacitance value.

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times F_{SW}}$$

The total output voltage ripple is the sum of V_{OUT_ESR} and V_{OUT_C}.

If the specification for steady-state output voltage ripple is known, the ESR can be determined using the above equations.

Another parameter that has influence on the output voltage undershoot is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, ESL contributes to part of the voltage undershoot. Use capacitor that has low ESL to obtain better transient performance. Generally, use several capacitors connected in parallel can have better transient performance than use single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, use a mixed combination of electrolytic capacitor and ceramic capacitor can also have better transient performance.

Feedback Loop Compensation

Figure 3 shows the voltage mode control loop for a buck converter. The control loop consists of the modulator, output LC filter and the compensator. The modulator is composed of the PWM comparator and power MOSFETs. The PWM comparator compares the error amplifier EA output (COMP) with the oscillator (OSC) sawtooth wave to generate a PWM signal. The MOSFETs is then switched on and off according to the duty cycle of the PWM signal. The voltage presented at PHASE node is a square wave of 0V to Vin.

The PHASE voltage is filtered by the output filter L_{OUT} and C_{OUT} to produce output voltage V_{OUT}, which is feedback to the inverting input of the error amplifier. The output voltage is then regulated according to the reference voltage V_{REF}.

In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (greater than 45 degrees) and the highest 0dB crossing frequency. It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of –20dB/dec.

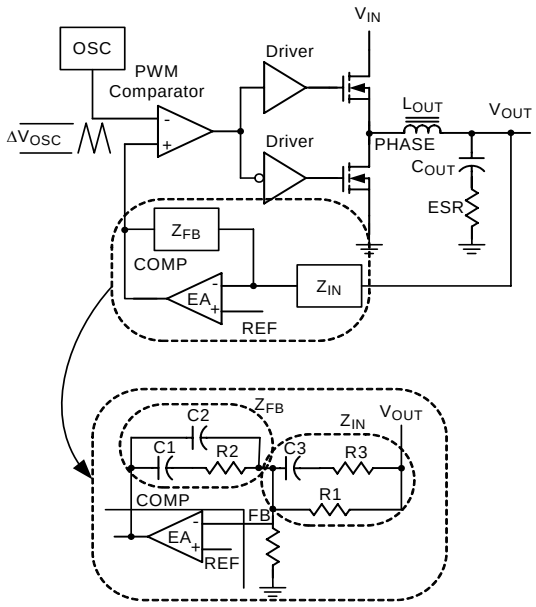


Figure 3. Control Loop for Voltage Mode Buck Converter

1) Modulator and Output LC filter

Referring to Figure 3, the modulator gain is the input voltage V_{IN} divided by the peak to peak oscillator voltage V_{OSC} as shown as following Equation :

$$Modulator_{Gain} = \frac{V_{IN}}{\Delta V_{OSC}}$$

where ΔV_{OSC} = 1.5V (typ.)

The output LC filter introduces a double pole to the transfer function, creating –40dB/decade gain slope above its corner frequency, with a phase lag of 180 degrees. The frequency at the double-pole of LC filter is expressed as follows.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

In addition, the ESR of the output capacitor introduces a zero to the transfer function, creating a +20dB/dec gain slope with a phase shift of 90 degree. The frequency of the ESR zero is expressed as follows.

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

2) Compensator

Figure 4 illustrates the type II compensator, which consists of the error amplifier and the impedance Z_C and Z_F.

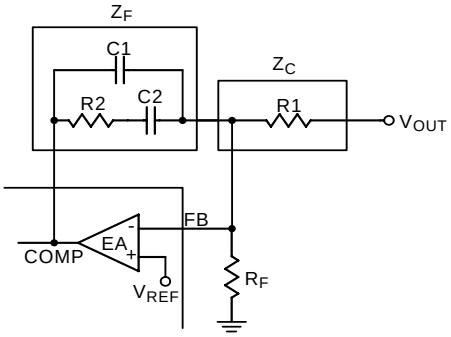


Figure 4. Type II Compensator

Type II compensator provides two poles and one zero to the system. The first pole is located at low frequency to increase the dc gain for regulation accuracy. The location of the other pole and the zero is expressed as follows.

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

Figure 5 shows the Bode plot for the gain of system. The compensation gain determined by Z_C and Z_F should be designed to have high crossover frequency (bandwidth) with sufficient phase margin. In order to make the gain crosses over 0dB at a slope of –20dB/dec, place the zero before the LC double-pole frequency. Empirically, f_{z1} is placed at 75% of the LC double-pole frequency. Furthermore, the bandwidth of the system is the factor that affects the converter's transient performance. High bandwidth results in fast transient response, but it often jeopardizes the system stability. The bandwidth should be designed to be less than 1/5 of the switching frequency. Properly adjust R1 and R2 to change the mid-frequency gain to obtain the required bandwidth. The pole at f_{p1} is usually placed at half of the switching frequency to have sufficient phase margin and attenuation at high frequency.

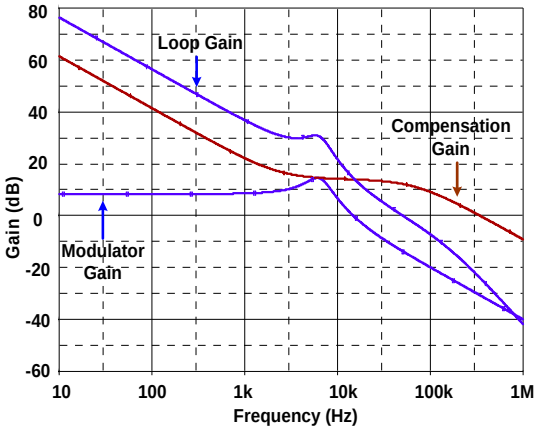


Figure 5. System Gain Bode Plot

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for

WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

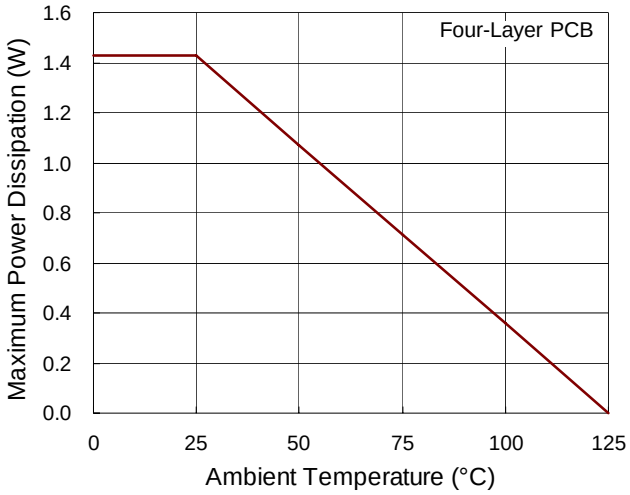


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

PCB layout is critical to high current high frequency switching converter designs. A good layout can help the controller to function properly and achieve expected performance. On the other hand, PCB without a carefully layout can radiate excessive noise, having more power loss and even malfunction in the controller. In order to avoid the above condition, the following general guidelines must be followed in PCB layout.

- Power stage components should be placed first. Place the input bulk capacitors close to the high side power MOSFETs, and then locate the output inductor and finally the output capacitors.
- Place the ceramic capacitor physically close to the drain of the high side MOSFET. This can reduce the input voltage drop when high side MOSFET is turned on. If more than one MOSFET is paralleled, each should have its own individual ceramic capacitor.
- Keep the high current loops as short as possible. During high speed switching, the current transition between MOSFETs usually causes di/dt voltage spike due to the parasitic components on PCB trace. Therefore, making the trace length between power MOSFETs and inductors wide and short can reduce the voltage spike and EMI.
- Make MOSFET gate driver path as short as possible. Since the gate driver uses narrow-width high current pulses to switch on/off the power MOSFET, the driver path must be short to reduce the trace inductance. This is especially important for low side MOSFET, because this can reduce the possibility of shoot-through.
- Providing enough copper area around the power MOSFETs to help heat dissipation. Using thick copper also reduces the trace resistance and inductance to have better performance.
- The output capacitors should be placed physically close to the load. This can minimize the trace parasitic components and improve transient response.
- All small signal components should be located close to the controller. The small signal components include the feedback voltage divider resistors, compensator, function setting components and high-frequency bypass capacitors. The feedback voltage divider resistor and the compensator must be placed close to FB pin and COMP pin, because these pins are inherently noise-sensitive.
- Voltage feedback path must be kept away from the switching nodes. The noisy switching node is, for example, the interconnection between high side MOSFET, low side MOSFET and inductor. The feedback path must be kept away from this kind of noisy node to avoid noise pick-up.
- A multi-layer PCB design is recommended. Make use of one single layer as the ground and have separate layers for power rail or signal that is suitable for PCB design.

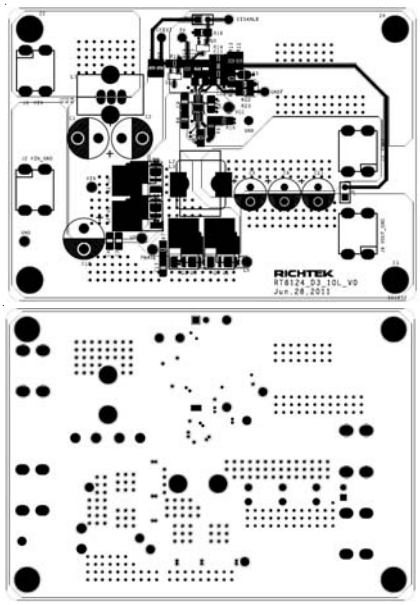
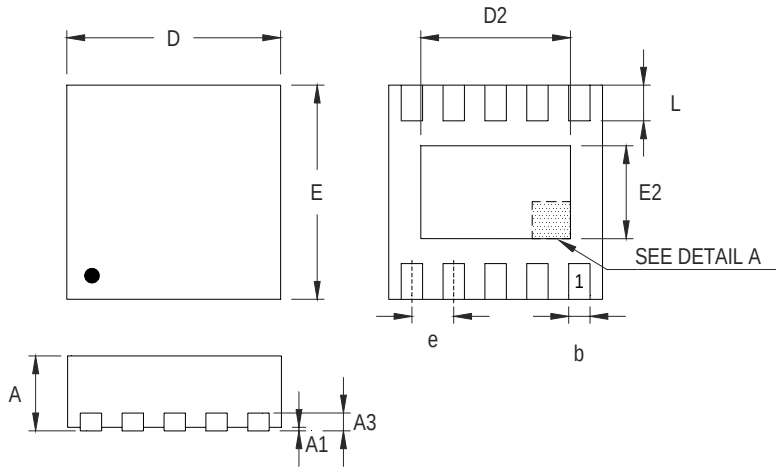
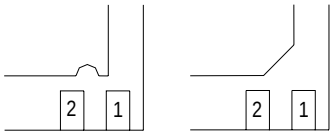


Figure 7. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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