RICHTEK®

RT8096B

1A, 1.5MHz, 6V CMCOT Synchronous Step-Down Converter

1 General Description

The RT8096B is a high-efficiency synchronous step-down converter. It operates within an input voltage range from 2.5V to 6V and provides an adjustable regulated output voltage from 0.6V to 3.4V, while delivering up to 1A output current.

The converter's internal synchronous power switches feature low on-resistance, which enhances efficiency and eliminates the need for an external Schottky diode. The Current Mode Constant On-time (CMCOT) operation coupled with internal compensation allows for optimized transient response across a wide range of loads and output capacitors. The RT8096B is available in T/SOT-23-5 and T/SOT-23-6 packages.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Ordering Information

RT8096B □□□

Package Type(1)
B: SOT-23-5
E: SOT-23-6
J5: TSOT-23-5
J6: TSOT-23-6

Lead Plating System
G: Richtek Green Policy Compliant(2)

UVP Trim Option
H: Hiccup

B: Forced PWM

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

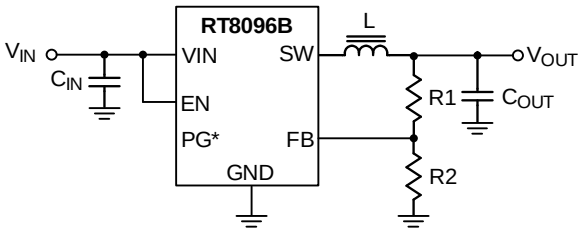
3 Features

- **Up to 95% efficiency with integrated 160mΩ and 110mΩ FETs**
- **Input Voltage Range: 2.5V to 6V**
- **Output Voltage Range: 0.6V to 3.4V**
- **High-Accuracy Internal Reference Voltage: 0.6V ± 2%**
- **CMCOT™ Control for Fast Transient Response**
- **1.5MHz Switching Frequency**
- **Default Forced PWM Mode**
- **Fixed Soft-Start Time: 1.2ms**
- **Power-Good Indicator (T/SOT-23-6 Package Only)**
- **Input Undervoltage-Lockout (UVLO)**
- **Output Undervoltage Protection (Hiccup Mode)**
- **Cycle-by-Cycle Overcurrent Protection**
- **Over-Temperature Protection**
- **T/SOT-23-5 and T/SOT-23-6 Packages**

4 Applications

- Mobile Phones and Handheld Devices
- Set-Top Box, Cable Modem, and xDSL Platforms
- LCD TV Power Supply and Metering Platforms
- General Purpose Point of Load (POL)

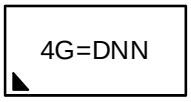
5 Simplified Application Circuit



*: For T/SOT-23-6 Package Only

6 Marking Information

RT8096BHGB



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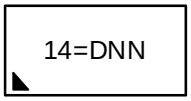
DNN : Date Code

RT8096BHGE



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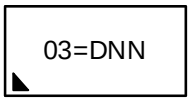

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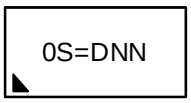

0S= : Product Code
DNN : Date Code

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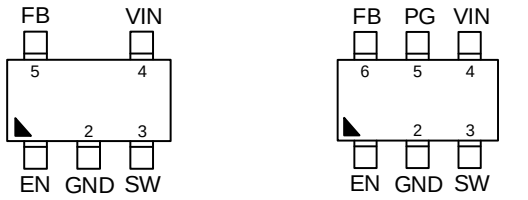
7 Pin Configuration

(TOP VIEW)

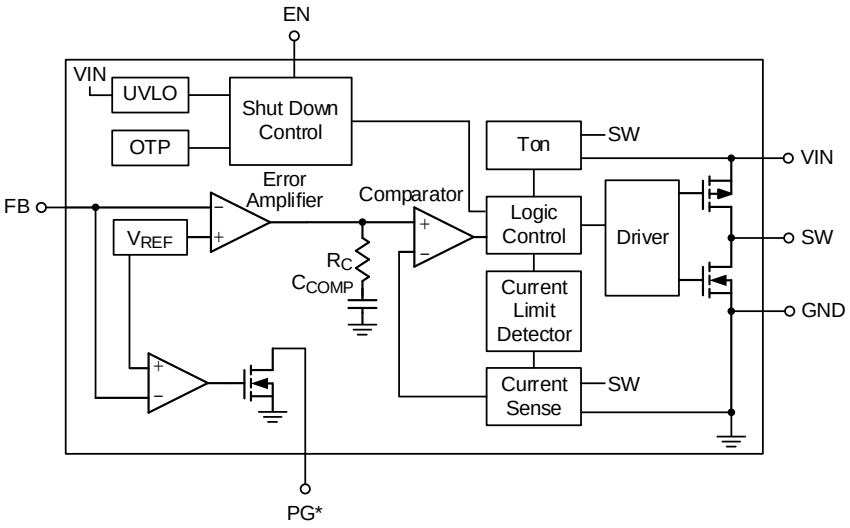


TSOT-23-5/SOT-23-5 TSOT-23-6/SOT-23-6

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
T/SOT-23-5	T/SOT-23-6		
1	1	EN	Enable control input. A logic-high enables the converter, while a logic-low forces the device into shutdown mode. Do not leave this pin floating.
2	2	GND	Power ground.
3	3	SW	Switch node. Connect this pin to power inductor.
4	4	VIN	Supply voltage input. The input voltage range is from 2.5V to 6V. Connect an input bypass capacitor (typically greater than 10μF) between this pin and GND. The bypass capacitor should be placed as close to the IC as possible.
5	6	FB	Feedback voltage input. This pin is used to set the output voltage via an external resistive voltage divider. Place the resistive voltage divider as close to the FB pin as possible. Do not leave this pin floating.
--	5	PG	Power-good indicator. This open-drain output pin is pulled high when the FB voltage is within the target range. It is pulled to ground under protection conditions, EN shutdown, or during soft-start process.

9 Functional Block Diagram



*: For T/SOT-23-6 Package Only

10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage ---------- –0.3V to 6.5V
- SW Pin Switch Voltage ---------- –0.3V to (V_{IN} + 0.3V)
  <20ns ---------- –4.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  T/SOT-23-5 ---------- 0.43W
  T/SOT-23-6 ---------- 0.5W
- Package Thermal Resistance (Note 3)
  T/SOT-23-5, θ_{JA} ---------- 230.6°C/W
  T/SOT-23-6, θ_{JA} ---------- 197.4°C/W
  T/SOT-23-5, θ_{JC} ---------- 21.8°C/W
  T/SOT-23-6, θ_{JC} ---------- 18.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. The first layer of copper area is filled. θ_{JC} is measured at the top of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage ---------- 2.5V to 6V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

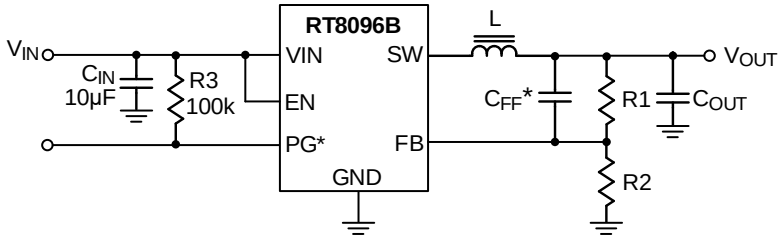
Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		2.5	--	6	V
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Pin Current	I_{FB}	V_{FB} = 0.6V	--	--	0.1	μA
Quiescent Current	I_Q	Active, V_{FB} = 0.63V, not switching	--	300	--	μA
Shutdown Current	I_{SHDN}	Shutdown	--	--	1	μA
Switching Leakage Current	I_{SW_LK}		--	--	1	μA
Switching Frequency	f_{SW}		--	1.5	--	MHz
On-Resistance of High-Side MOSFET	R_{DSON_H}	I_{SW} = 0.3A	--	160	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}	I_{SW} = 0.3A	--	110	--	mΩ
Valley Current Limit	I_{LIM_L}		1.1	1.5	2	A
Undervoltage-Lockout Rising Threshold	V_{UVLO_R}	VDD rising	--	2.25	2.5	V
Undervoltage Lockout Falling Threshold	V_{UVLO_F}	VDD falling	--	2	--	V
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
EN Input Voltage Rising Threshold	V_{EN_R}		1.5	--	--	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	
PG Voltage Rising Threshold	V_{PG_R}	FB rising	--	90	--	%
PG Voltage Falling Threshold	V_{PG_F}	FB falling	--	85	--	
PG Pull-Up Resistance	R_{PG_PU}	PG = Low	--	--	100	Ω
Soft-Start Time	t_{SS}		--	1.2	--	ms
Minimum Off-Time	t_{OFF_MIN}		--	120	--	ns
Discharge Resistance	R_{DISCHG}		--	1.8	--	kΩ

13 Typical Application Circuit



*For T/SOT-23-6 Package Only

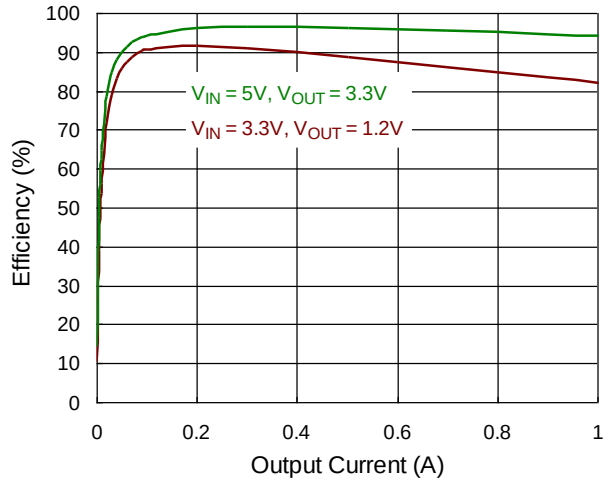
*C_{FF}: Optional for performance fine-tuning

Table 1. Suggested Component Values

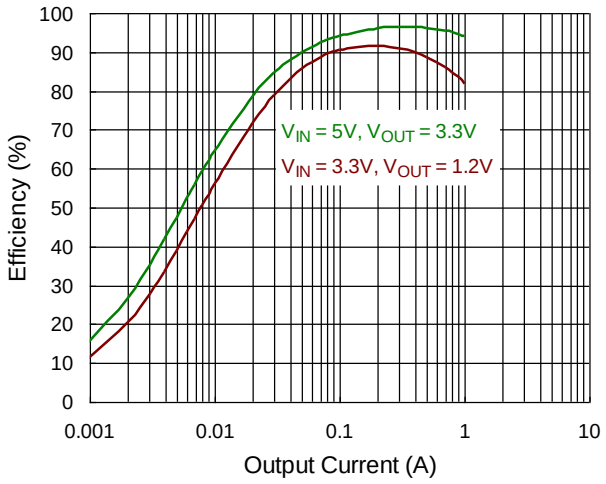
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)
3.3	90	20	1.5	10
1.8	100	50	1.5	10
1.5	100	66.6	1.5	10
1.2	100	100	1.5	10
1.05	100	133	1.5	10
1	100	148	1.5	10

14 Typical Operating Characteristics

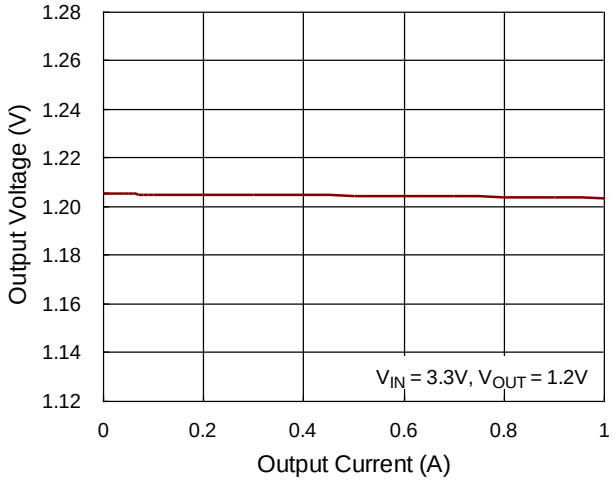
Efficiency vs. Output Current



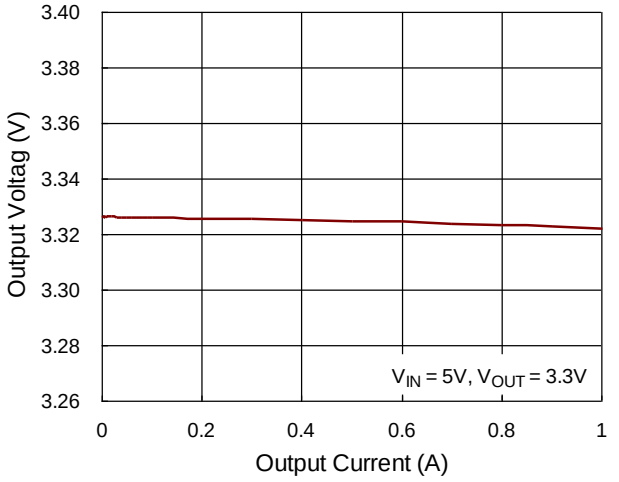
Efficiency vs. Output Current



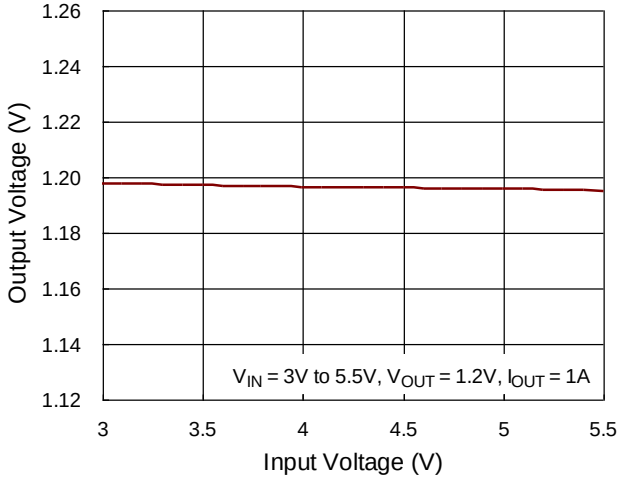
Output Voltage vs. Output Current



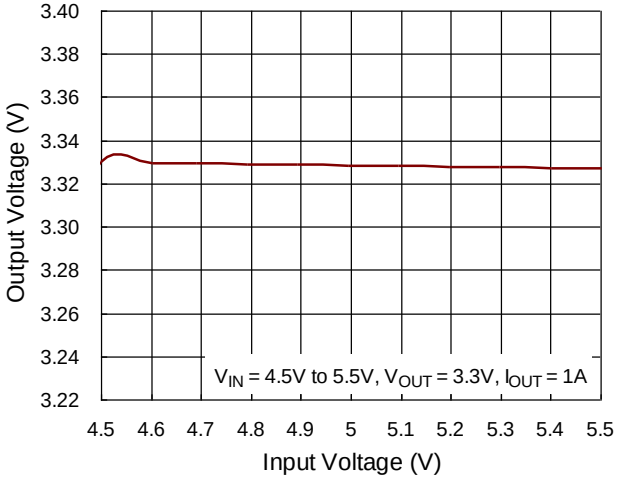
Output Voltage vs. Output Current



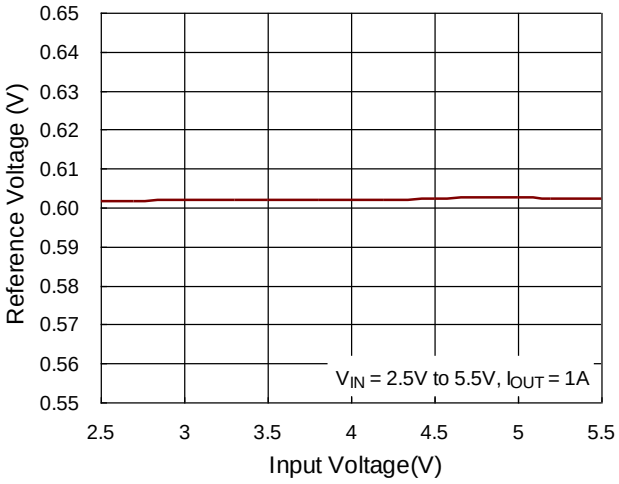
Output Voltage vs. Input Voltage



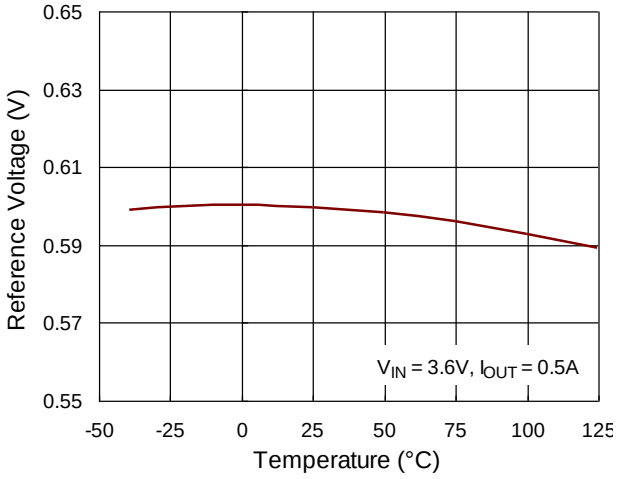
Output Voltage vs. Input Voltage



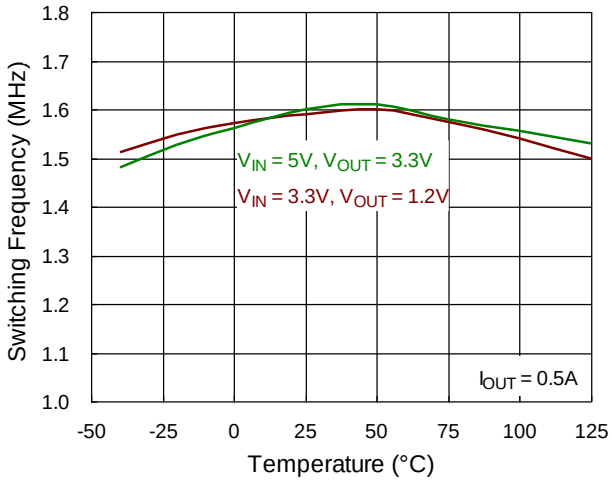
Reference Voltage vs. Input Voltage



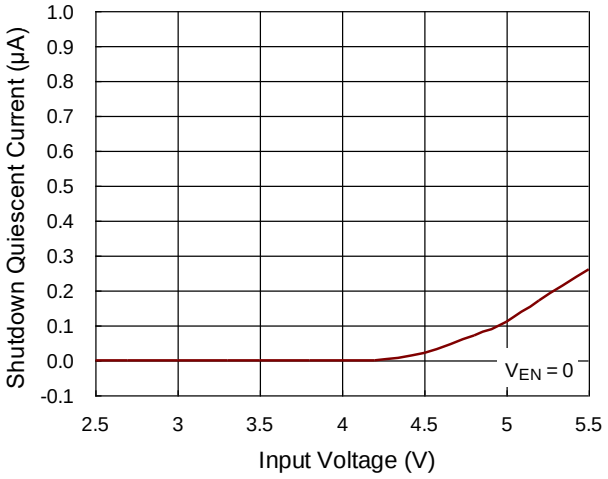
Reference Voltage vs. Temperature



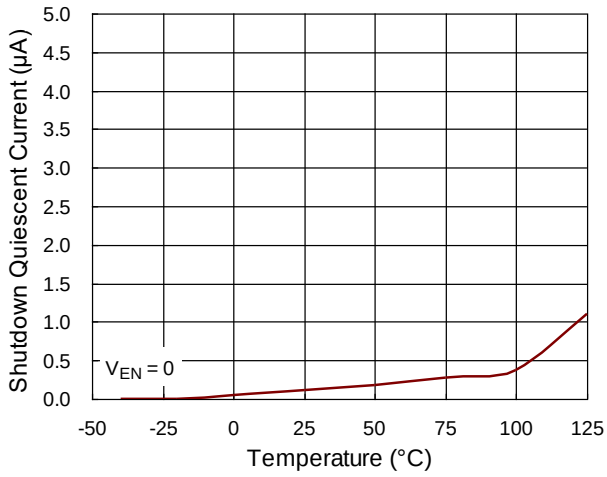
Switching Frequency vs. Temperature



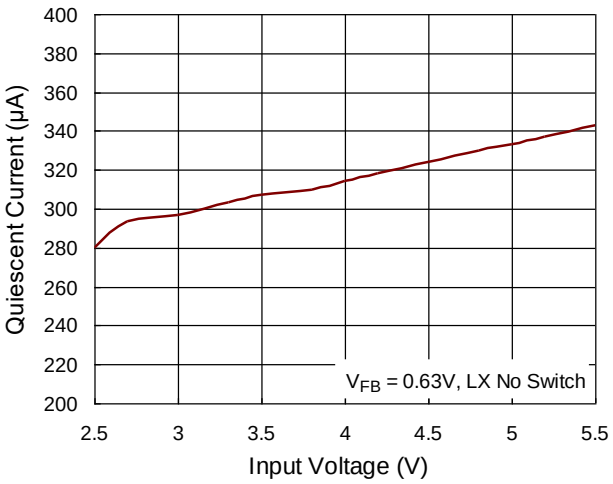
Shutdown Quiescent Current vs. Input Voltage



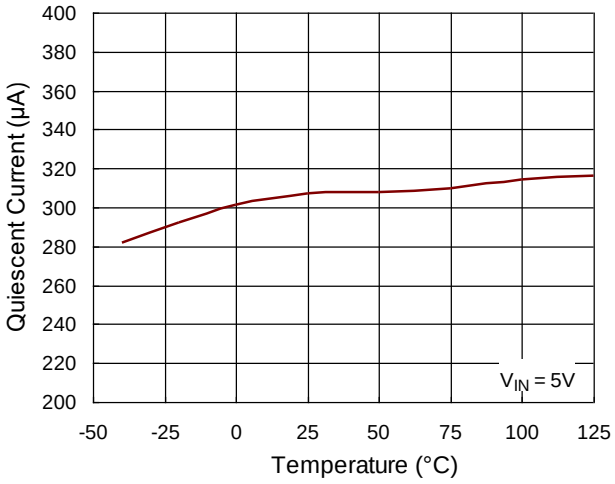
Shutdown Quiescent Current vs. Temperature



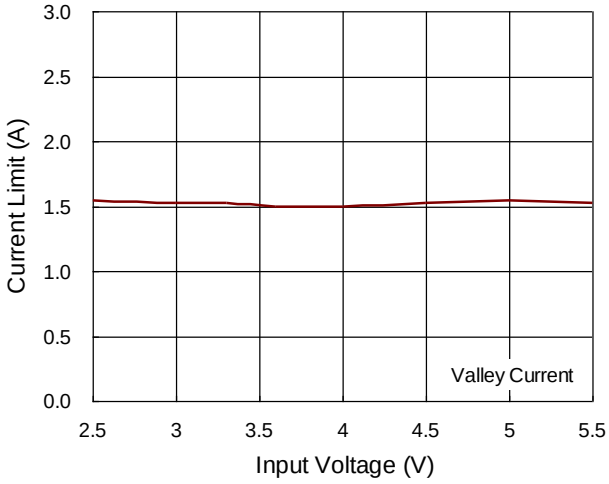
Quiescent Current vs. Input Voltage



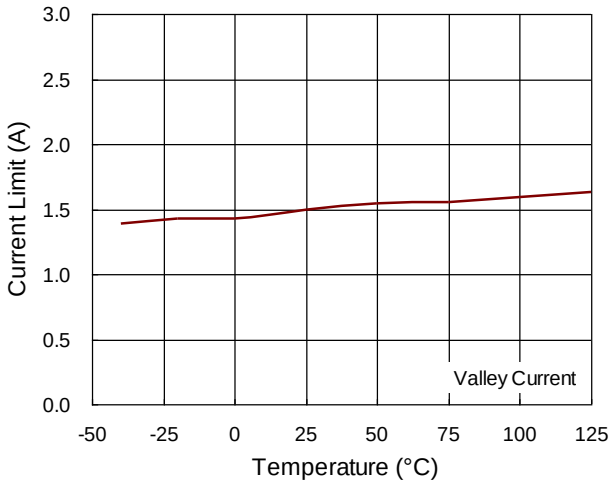
Quiescent Current vs. Temperature



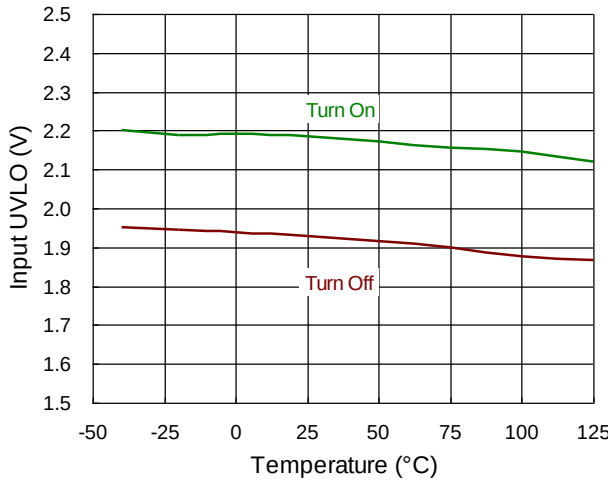
Current Limit vs. Input Voltage



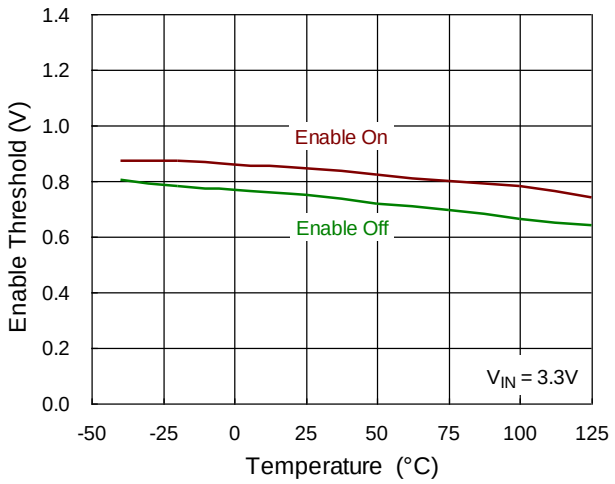
Current Limit vs. Temperature



Input UVLO vs. Temperature

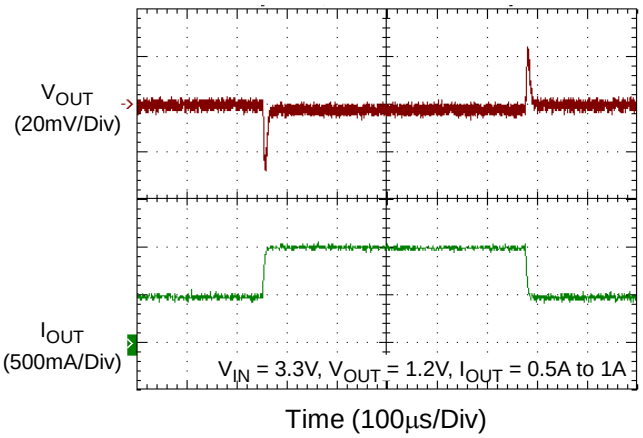


Enable Threshold vs. Temperature

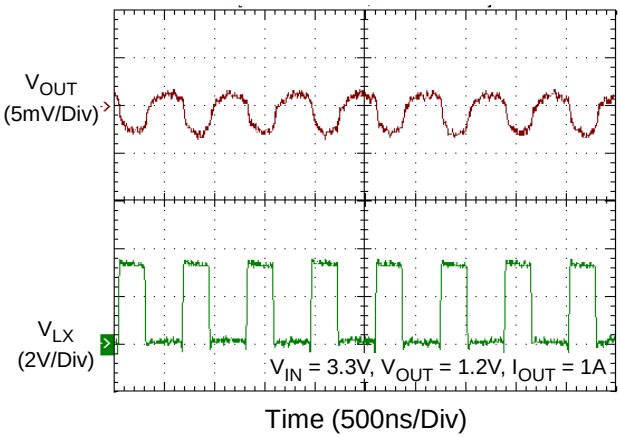


Load Transient Response

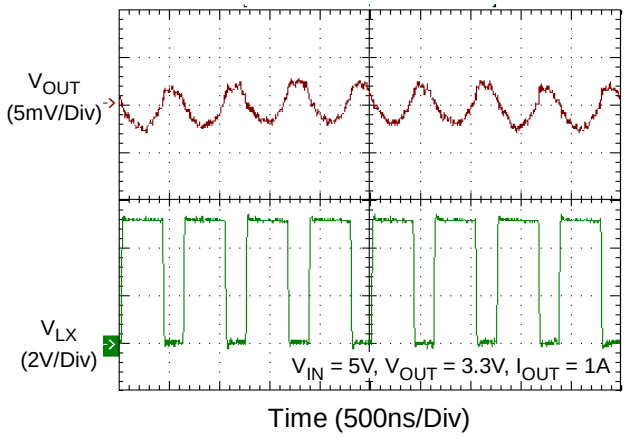
Load Transient Response



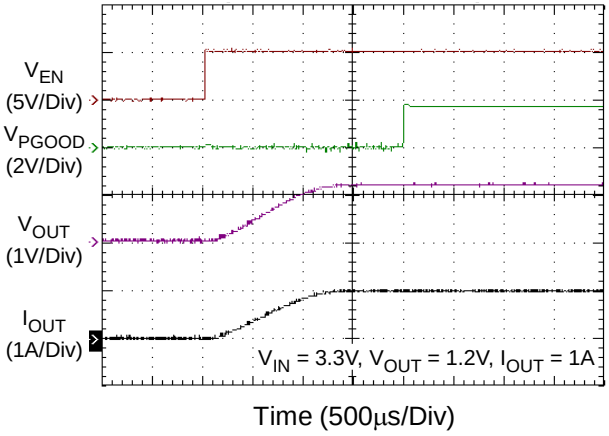
Voltage Ripple



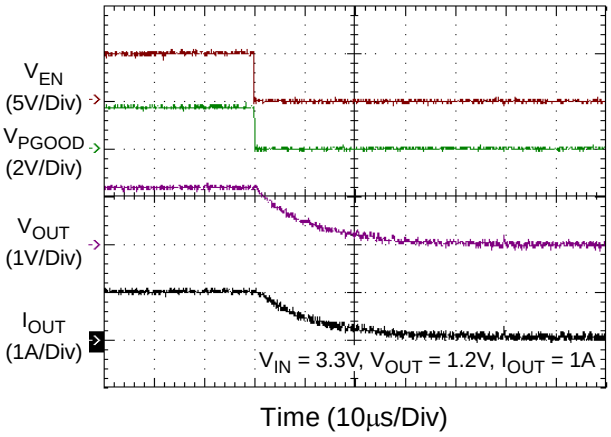
Voltage Ripple



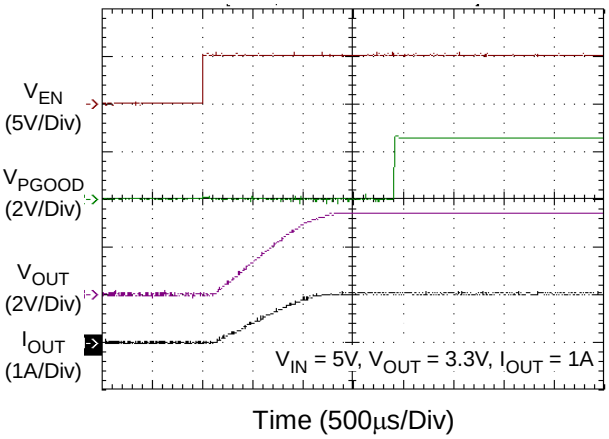
Power On from EN



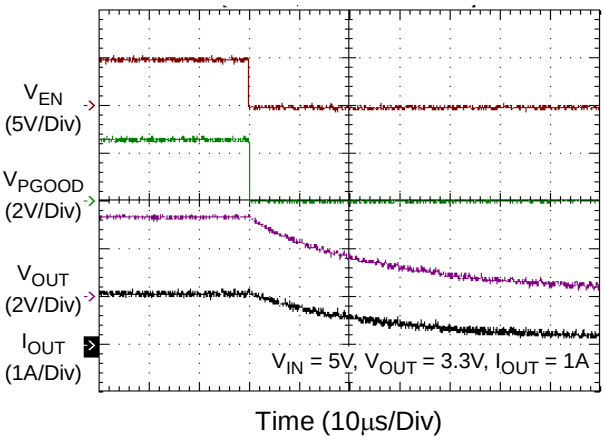
Power Off from EN



Power On from EN



Power Off from EN



15 Operation

The RT8096B is a synchronous low-voltage step-down converter that supports an input voltage range from 2.5V to 6V and can deliver an output current up to 1A. It adopts the current mode constant on-time architecture for optimal transient response and robust loop stability when using ceramic capacitors.

The FB pin voltage is compared with the internal reference voltage to generate an error signal. This error signal is internally compensated and then compared with the inductor current, which is sensed through the internal sense resistor at the SW pin.

When the signal sensed from the inductor current falls below the compensated error signal, the internal high-side P-MOSFET is activated for a constant on-time duration to make the inductor current ramp up. At the end of the on-time interval, the internal high-side P-MOSFET is deactivated and the internal low-side N-MOSFET is activated until the FB pin voltage falls below the internal reference voltage, initiating the next switching cycle.

15.1 UVLO, Enable Control and Soft-Start

The RT8096B features undervoltage-lockout (UVLO) protection to prevent insufficient input voltage by monitoring the VIN pin. When the input voltage falls below the UVLO threshold, the RT8096B stops switching.

The RT8096B provides an EN pin to enable or disable the device externally. When the EN pin voltage falls below the falling threshold voltage (V_{EN_F}), the RT8096B enters shutdown mode, even if the VIN pin voltage is above the UVLO threshold (V_{UVLO}). In shutdown mode, the supply current is reduced to a maximum 1μA (I_{SHDN}). Once the EN pin voltage rises above the rising threshold voltage (V_{EN_R}) and the VIN pin voltage is higher than the UVLO threshold, the internal digital circuits and MOSFET gate drivers are enabled for normal operation. In addition, the EN pin can be directly connected to the VIN pin to save the system's power rail.

The RT8096B implements internal soft-start function to prevent large inrush current and output voltage overshoot during power-up. During soft-start interval, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the FB pin voltage, causing PWM pulse width to increase gradually to reduce the input surge current. The internal 0.6V reference takes over the loop control once the ramping voltage exceeds 0.6V. The internal soft-start time is fixed to 1.2ms.

15.2 Output Voltage Setting

Based on the typical application circuit, the RT8096B's output voltage can be adjusted from 0.6V to 3.4V. By connecting a resistive voltage divider between VOUT and GND, the output voltage can be calculated using the equation below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typical).

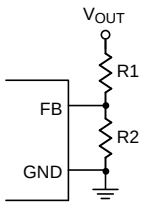


Figure 1. Setting V_{OUT} with a Voltage Divider

15.3 Forced PWM Mode

The default operation mode of the RT8096B is forced PWM mode. In this mode, the internal ZCD circuitry is disabled, and the switching frequency is fixed at 1.5MHz (typically) under any load condition. While forced PWM mode may reduce efficiency under light-load conditions, it benefits the system with minimal output voltage ripple, tight output voltage regulation, and a stable switching frequency.

15.4 Power-Good Indicator (T/SOT-23-6 Package Only)

The RT8096B features a power-good indicator with open-drain output capability to show the status of the output voltage. When the FB pin voltage exceeds 90% of the internal reference voltage, the PG pin remains in a high-impedance state. The delay time from EN to PG is 2ms, and the internal pull-up resistance for the PG pin is 100Ω.

15.5 Output Undervoltage Protection (UVP)

The RT8096B features output undervoltage protection (UVP) to protect against overload or short-circuit conditions by constantly monitoring the FB pin voltage. If the FB pin voltage drops below 0.2V, the internal high-side P-MOSDET will be turned-off, and the internal low-side N-MOSFET will be turned on to discharge the output voltage. This protection mechanism operates in hiccup mode.

15.6 Output Overcurrent Protection (OCP)

The RT8096B features overcurrent protection (OCP) to prevent catastrophic damage to the IC in the event of output short-circuit, overcurrent or inductor saturation conditions. If the sensed valley inductor current exceeds the OCP trip threshold (typically 1.5A), the OCP will be activated. Then, the internal high-side P-MOSDET will be turned off, and the internal low-side N-MOSFET will be turned on until UVP is triggered. This protection mechanism operates in hiccup mode.

15.7 Over-Temperature Protection (OTP)

The RT8096B features over-temperature protection (OTP) circuitry to prevent the device from overheating. If the junction temperature exceeds the thermal shutdown threshold of 150°C, both the internal MOSFETs will stop switching. The device will then resume normal operation once the junction temperature decreases by 20°C. This protection mechanism operates in hiccup mode.

16 Application Information

(Note 6)

The RT8096B is a single-phase step-down converter designed with a single feedback loop and constant on-time current mode control to achieve fast transient response. An internal 0.6V reference enables precise regulation of the output voltage, making it suitable for low output voltage applications. The device features a fixed switching frequency of 1.5MHz, and internal compensation to minimize the need for external components. Protection features include undervoltage protection (UVP), overcurrent protection (OCP), and over-temperature protection (OTP).

16.1 Inductor Selection

The inductor selection makes trade-offs among size, cost, power conversion efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductor value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). A good compromise between inductor size and power loss is achieved with a peak-to-peak ripple current that is 30% to 50% of the average inductor current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value for normal operation as follows:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

where ΔI_L is the peak-to-peak inductor ripple current.

Larger inductance values result in lower output ripple voltage and higher efficiency but may slightly degraded load transient response. This result in additional phase lag in the loop and reduce the crossover frequency. Conversely, lower inductance values allow for a smaller case size but increases the AC losses in the inductor. To enhance the power conversion efficiency, choose a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. The inductor value not only determines the ripple current but also the load-current value at which the transition between discontinuous conduction mode (DCM) and continuous conduction mode (CCM) occurs. The selected inductor should be large enough to avoid saturation at the peak inductor current (I_{L_PEAK}):

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \times \Delta I_L$$

The current flowing through the inductor consists of the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current may rise above the previously calculated peak inductor current level. For this reason, the most conservative approach is to specify an inductor with a saturation current rating that is equal to or greater than the peak inductor current.

16.2 Input Capacitor Selection

Since the input current operates in discontinuous conduction mode, the input capacitor (C_{IN}) is required to filter the pulsating current at the drain terminal of an internal high-side P-MOSFET, thereby preventing a large variation in the input voltage. Thus, the peak-to-peak voltage ripple on the input capacitor can be estimated using the equation below:

$$\Delta V_{CIN} = I_{OUT} \times \left(\frac{D \times (1-D)}{C_{IN} \times f_{SW}} + ESR_{CIN} \right)$$

where $D = V_{OUT}/V_{IN}$, and ESR_{CIN} is the equivalent series resistance of the input capacitor.

The input decoupling capacitor is recommended to be greater than 10μF with thermal specification of X5R or X7R ceramic capacitors for less capacitance variation and more temperature stability. For filtering high frequency noise, additional small capacitor of 1μF with an 0603 size should be placed close to the part. Additionally, the input

capacitor needs to have a low ESR and must be rated to handle the worst-case RMS input current. The RMS input ripple current (I_{CIN_RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and maximum output current (I_{OUT_MAX}) as the following equation:

$$I_{CIN\_RMS} \cong I_{OUT\_MAX} \times \sqrt{D \times (1-D)}$$

The worst condition occurs when duty cycle = 50%, at which point V_{IN} = 2 x V_{OUT}, and the maximum RMS input ripple current will be 0.5 x I_{OUT_MAX}.

For optimal PCB layout placement, the input capacitor should be placed as close as possible to the VIN and the GND pins.

Note that a ceramic capacitor has a very low equivalent series resistance (ESR) and provides the best ripple performance. However, temperature, DC bias voltage and switching frequency can influence the variation of the capacitance value. This means that the capacitance value decreases as the DC bias voltage across the capacitor increases. In most cases, the ceramic capacitors will lose 50% or more of their rated value when DC bias voltage across the capacitor is near their rated voltage. Thus, it is important to carefully choose the value and case size of ceramic capacitors by considering the voltage coefficient.

16.3 Output Capacitor Selection

The output capacitor (C_{OUT}) is selected to satisfy the requirements for output voltage ripple and the load transient response. The peak-to-peak voltage ripple on output capacitor (ΔV_{COUT}) can be calculated using the equation below:

$$\Delta V_{COUT} = \Delta I_L \times \left(\frac{1}{8 \times C_{OUT} \times f_{SW}} + ESR_{COUT} \right)$$

where ΔI_L is the peak-to-peak inductor ripple current, and ESR_{COUT} is the equivalent series resistance of the output capacitor.

Since the ΔI_L increases with larger input voltage, the output voltage ripple in steady-state will be largest under the condition of maximum input voltage. For the output voltage variation in load transient response condition, the output sag/soar can be calculated using the equation below:

$$V_{SAG} = V_{SOAR} = \frac{\Delta I_{OUT}}{2 \times \pi \times C_{OUT} \times f_C}$$

where f_C is the crossover frequency factor of PWM.

The output capacitor is recommended to be greater than 10μF with thermal specification of X5R or X7R ceramic capacitors for less capacitance variation and more temperature stability. For filtering high frequency noise, additional small capacitor of 1μF with an 0603 size should be placed close to the part.

For optimal PCB layout placement, the output capacitor should be placed as close as possible to the VOUT and the GND pins.

Note that a ceramic capacitor has a very low equivalent series resistance (ESR) and provides the best ripple performance. However, temperature, DC bias voltage and switching frequency can influence the variation of the capacitance value. This means that the capacitance value decreases as the DC bias voltage across the capacitor increases. In most cases, the ceramic capacitors will lose 50% or more of their rated value when DC bias voltage across the capacitor is near their rated voltage. Thus, it is important to carefully choose the value and case size of ceramic capacitors by considering the voltage coefficient.

16.4 Thermal Considerations

For continuous operation, the absolute maximum junction temperature should not be exceeded. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, the rate of surrounding airflow, and the difference between junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For T/SOT-23-5 package, the thermal resistance, θ_{JA}, is 230.6°C/W on a standard four-layer thermal test board. For T/SOT-23-6 package, the thermal resistance, θ_{JA}, is 197.4°C/W on a standard four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated using the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (230.6°C/W) = 0.43W for T/SOT-23-5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (197.4°C/W) = 0.5W for T/SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

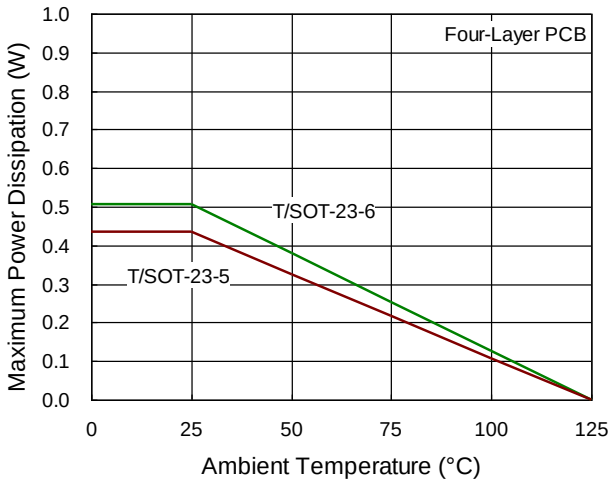
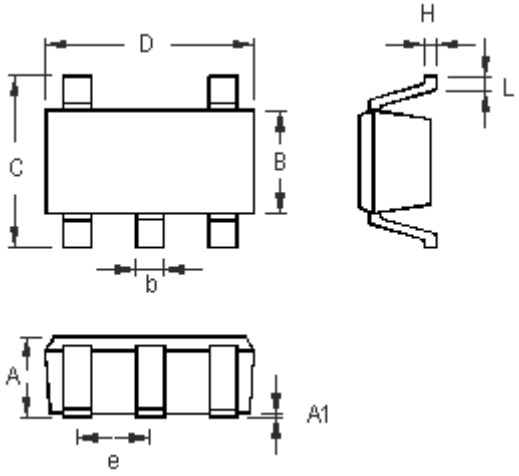


Figure 2. Derating Curve of Maximum Power Dissipation

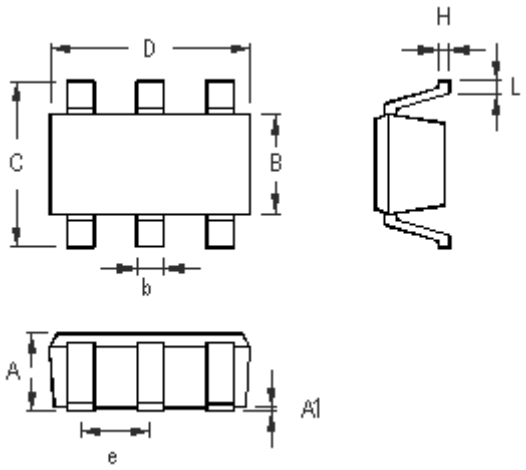
Note 6. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension



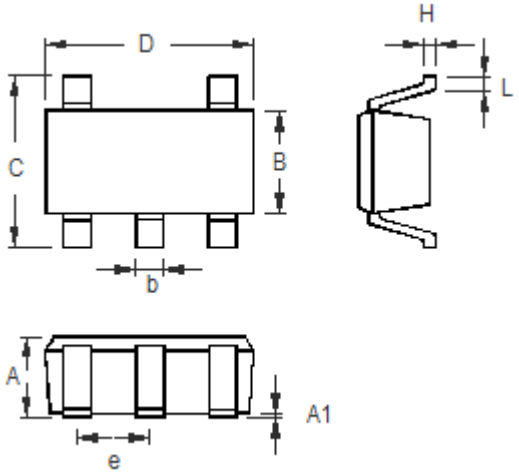
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package



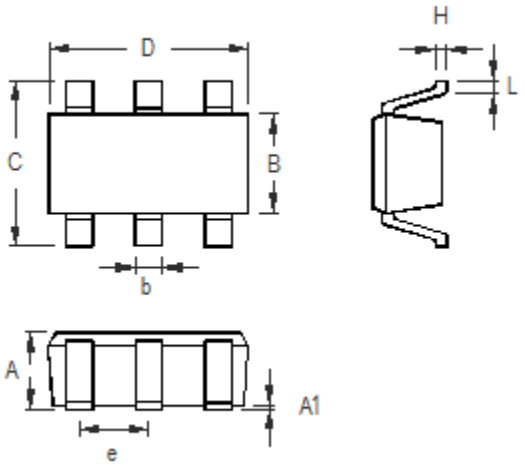
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

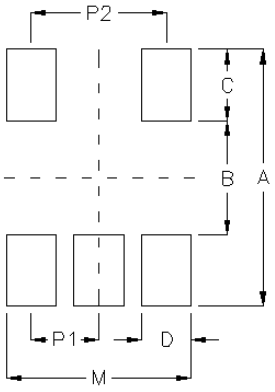
TSOT-23-5 Surface Mount Package



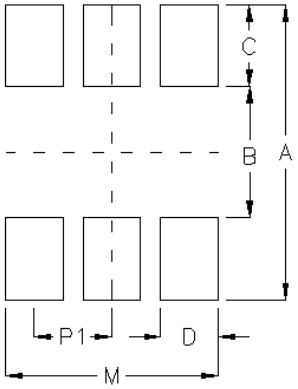
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-6 Surface Mount Package

18 Footprint Information



Package	Number of Pin	Footprint Dimension (mm)							Tolerance
		P1	P2	A	B	C	D	M	
TSOT-25/TSOT-25(FC)/SOT-25	5	0.95	1.90	3.60	1.60	1.00	0.70	2.60	±0.10

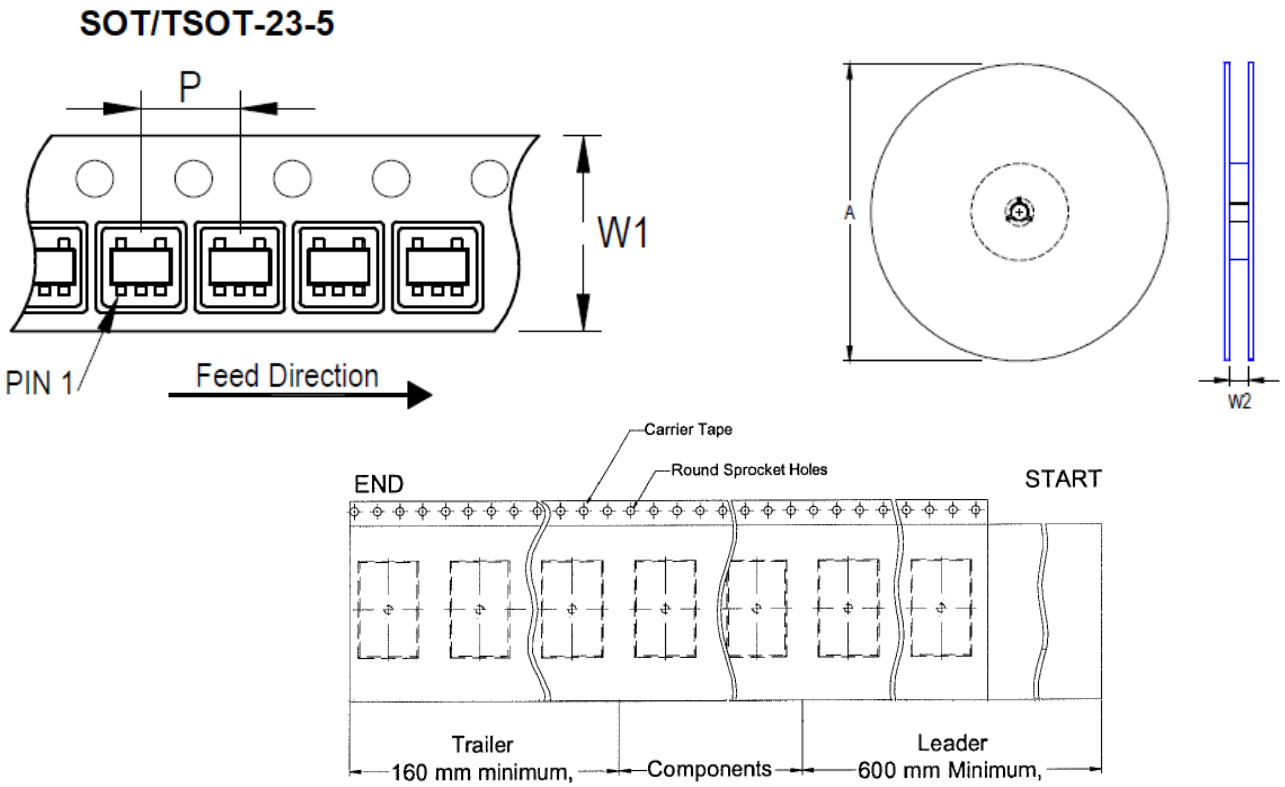


Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26/SOT-26(COL)	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

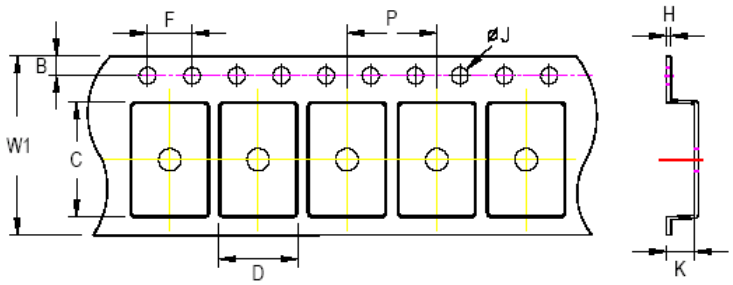
19 Packing Information

19.1 Tape and Reel Data

19.1.1 SOT-23-5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9

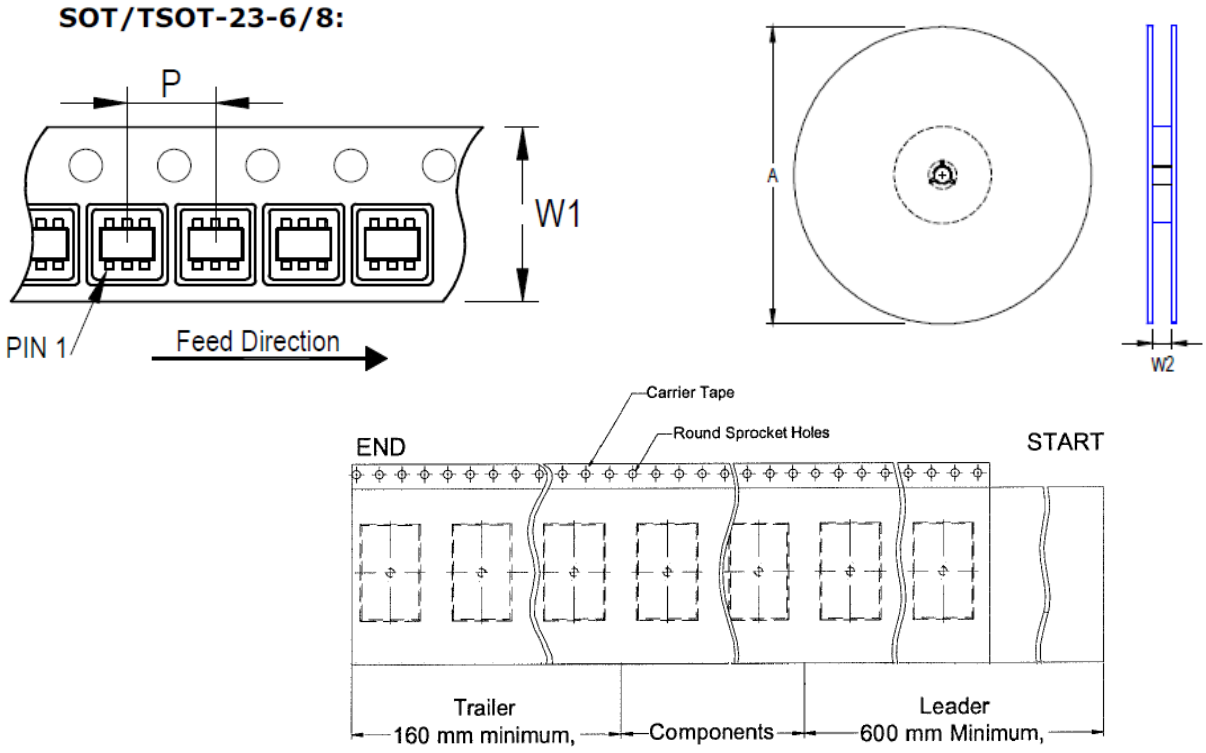


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

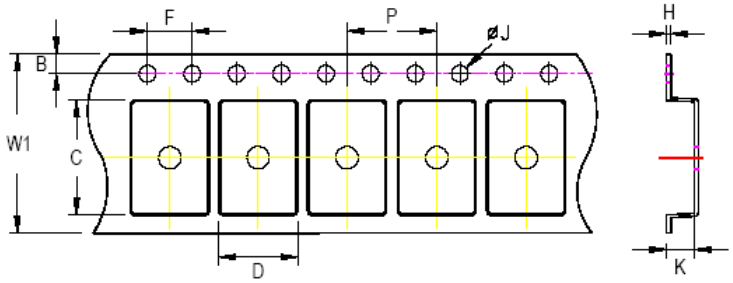
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.3mm	1.7mm	0.6mm

19.1.2 SOT-23-6



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT-23-6	8	4	180	7	3,000	160	600	8.4/9.9



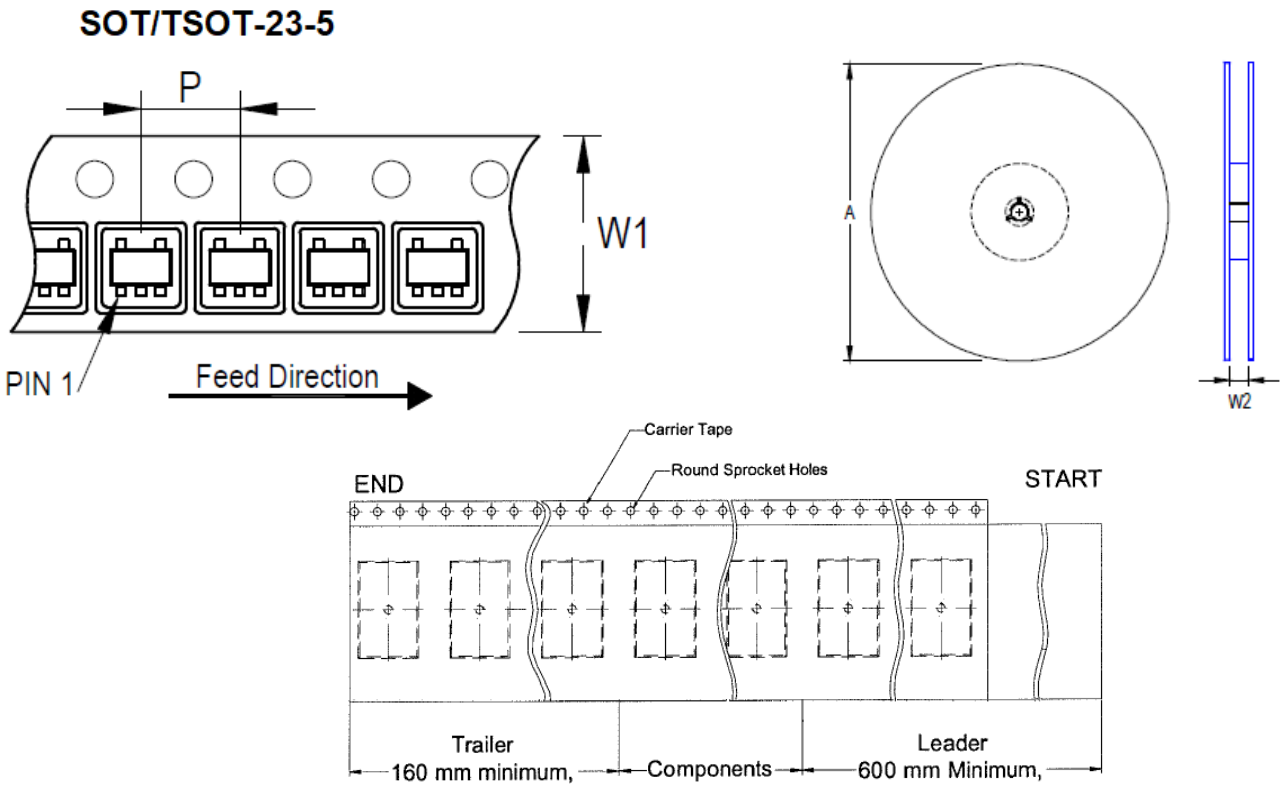
C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

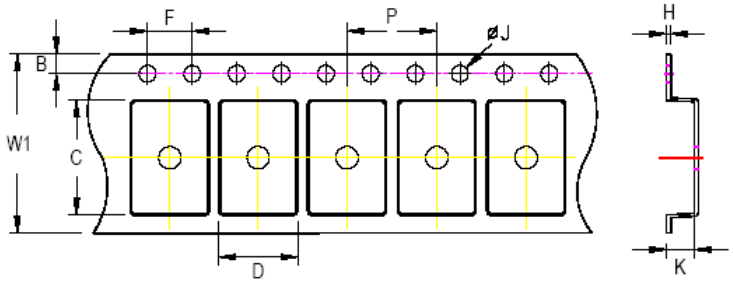
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.3mm	1.7mm	0.6mm

19.1.3 TSOT-23-5



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
TSOT-23-5	8	4	180	7	3,000	160	600	8.4/9.9



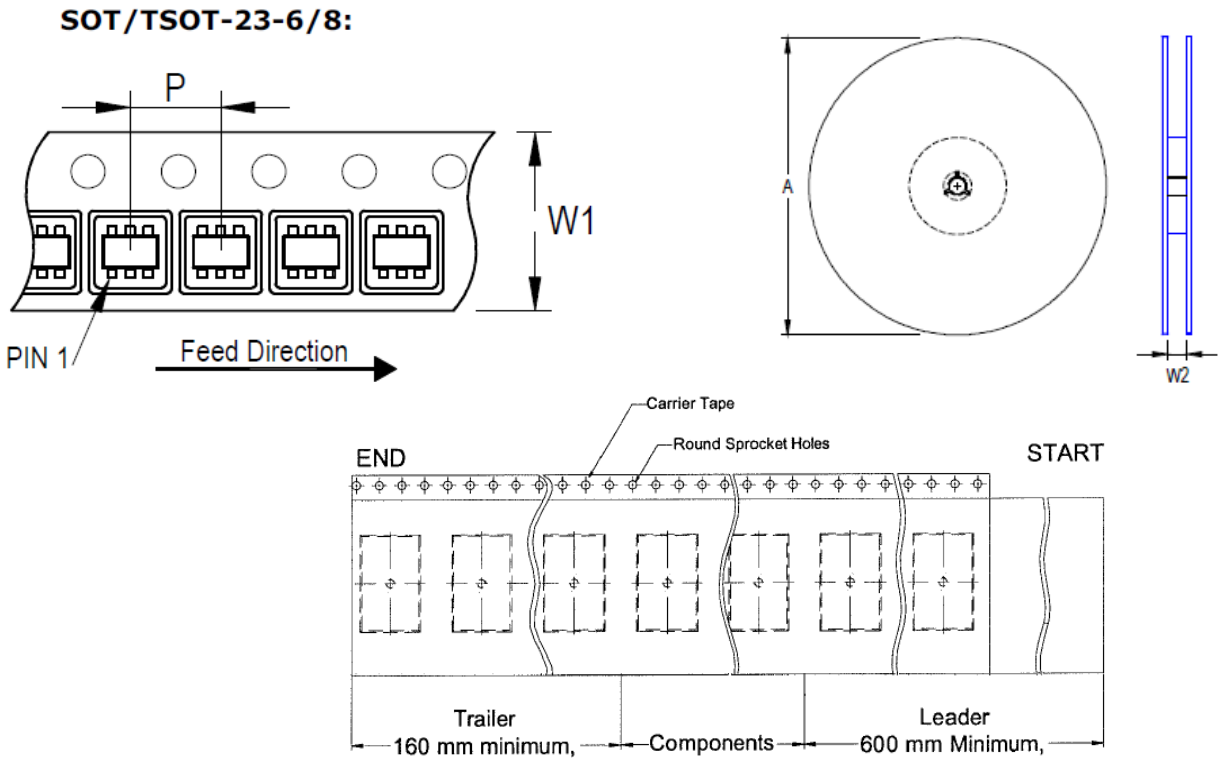
C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

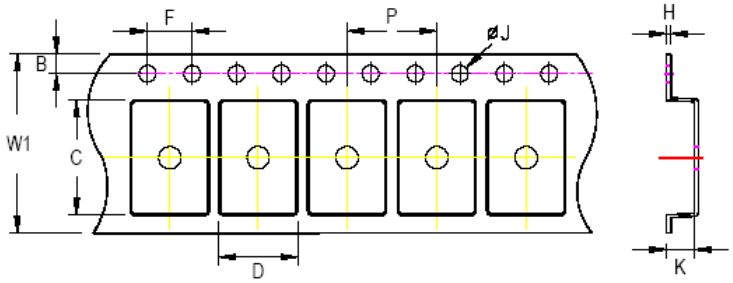
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.2mm	0.6mm

19.1.4 TSOT-23-6



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
TSOT-23-6	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1mm	1.2mm	0.6mm

19.2 Tape and Reel Packing

19.2.1 SOT-23-5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-23-5	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.2.2 SOT-23-6

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
SOT-23-6	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.2.3 TSOT-23-5

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-23-5	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.2.4 TSOT-23-6

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
TSOT-23-6	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

20 Datasheet Revision History

Version	Date	Description	Item
07	2024/8/26	Modify	*Changed the names of pin 3 to SW.* *General Description on page 1* *Features on page 1* *Ordering Information on page 1* *Functional Pin Description on page 4* *Functional Block Diagram on page 4* *Electrical Characteristics, page 7* *Operation on page 14, 15* *Application Information on page 16, 17, 18* *Footprint Information on page 22, 23* - Added footprint information *Packing Information on page 24 to 32* - Added packing information