RICHTEK®

RT8016

1.5MHz, 1A, High-Efficiency PWM Step-Down DC-DC Converter

1 General Description

The RT8016 is a high-efficiency Pulse-Width-Modulated (PWM) step-down DC-DC converter. Capable of delivering 1A output current over a wide input voltage range from 2.5V to 5.5V, the RT8016 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources such as portable instruments and hand-held devices.

Two operating modes are available: PWM/low-dropout auto switch and shut-down modes. The internal synchronous rectifier with low R_{DSON} dramatically reduces conduction loss in PWM mode. No external Schottky diode is required in practical applications.

The RT8016 enters low-dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the high-side MOSFET. The RT8016 enters shut-down mode and consumes less than 0.1μA when the EN pin is pulled low. The RT8016 also offers a range of 1V to 3.3V with 0.1V per step or adjustable output voltage by two external resistors.

The switching ripple is easily smoothed out by small package filtering elements due to a fixed operating frequency of 1.5MHz. This, along with the small WDFN-6L 2x2 package, provides a small PCB area application. Other features include soft-start, lower internal reference voltage with 2% accuracy, over-temperature protection, and overcurrent protection.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

3 Features

- **2.5V to 5.5V Input Range**
- **Adjustable Output from 0.6V to V_{IN}**
- **1A Output Current**
- **95% Efficiency**
- **No Schottky Diode Required**
- **1.5MHz Fixed Frequency PWM Operation**
- **Small 6-Lead WDFN Package**

4 Applications

- Handheld Devices
- Personal Information Appliances
- Portable Instruments

5 Ordering Information

RT8016-□□□□

Package Type(1)
QW: WDFN-6L 2x2 (W-Type)

Lead Plating System
P: Pb Free
G: Richtek Green Policy Compliant(2)

Output Voltage
Default: Adjustable
10: 1.0V
11: 1.1V
:
32: 3.2V
33: 3.3V

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Device Information

See the Product Status section for details on Active devices and End of Life (EOL) devices.

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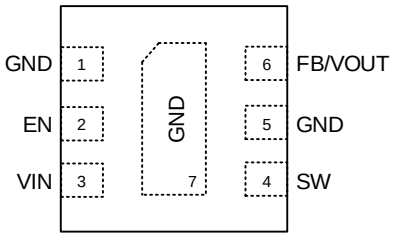
7 Pin Configuration

(TOP VIEW)

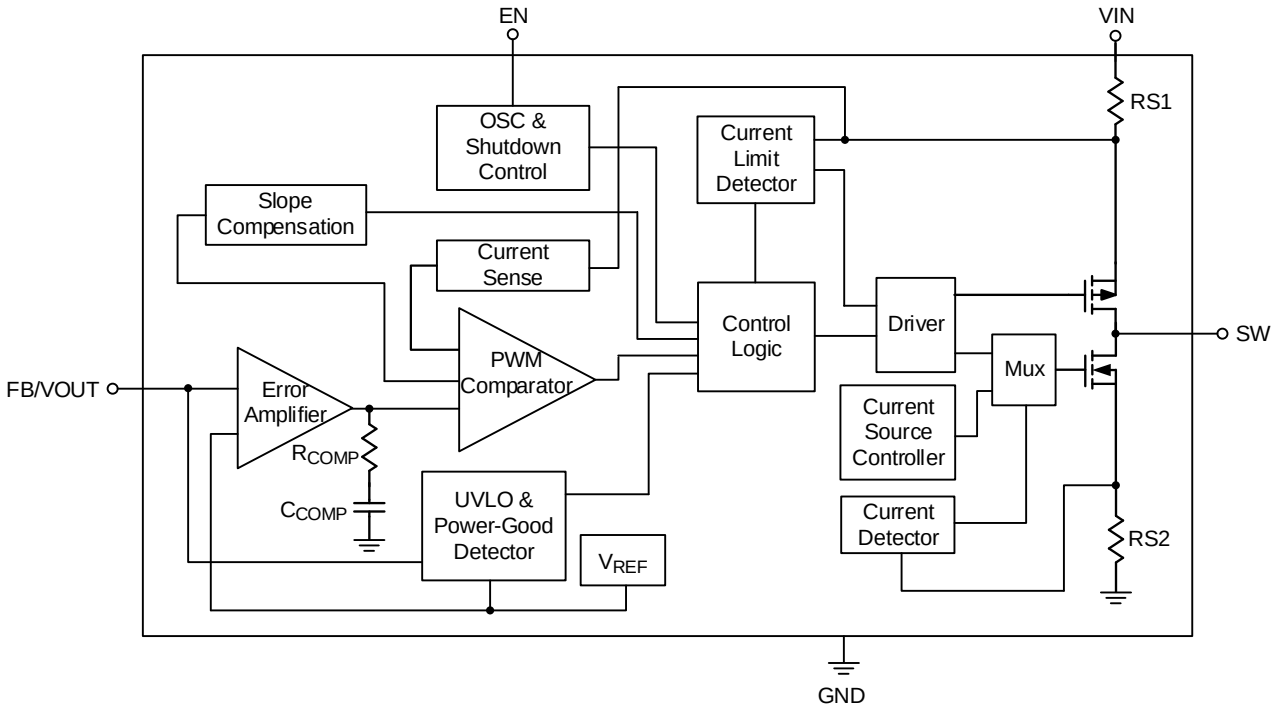


WDFN-6L 2x2

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
2	EN	Enable pin (active high).
3	VIN	Power input.
4	SW	Switch pin.
1, 5	GND	Ground pin.
6	FB/VOUT	Feedback/output voltage pin.
7 (Exposed Pad)	NC	No internal connection. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage ---------- 6.5V
- EN, FB Pin Voltage ---------- –0.3V to V_{IN}
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-6L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 3)

  WDFN-6L 2x2, θ_{JA} ---------- 165°C/W

  WDFN-6L 2x2, θ_{JC} ---------- 20°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured at T_A = 25°C on a single-layer and four-layer test board of JEDEC 51. The measurement case position of θ_{JC} is on the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, V_{REF} = 0.6V, L = 2.2µH, C_{IN} = 4.7µF, C_{OUT} = 10µF, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage	V_{IN}		2.5	--	5.5	V
Quiescent Current	I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%	--	50	70	µA
Shutdown Current	I_{SHDN}	EN = GND	--	0.1	1	µA
Reference Voltage	V_{REF}	For Adjustable Output Voltage	0.588	0.600	0.612	V
Adjustable Output Range	V_{OUT}	(Note 6)	V_{REF}	--	V_{IN} – 0.2V	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Fixed Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = (V_{OUT} + V_{OUT_ACC}) to 5.5V or V_{IN} > 2.5V whichever is larger. (Note 6)		–3	--	3	%
Adjustable Output Voltage Accuracy		V_{IN} = V_{OUT} + V_{OUT_ACC} to 5.5V (Note 6) 0A < I_{OUT} < 1A		–3	--	3	
The FB Pin Current	I_{FB}	V_{FB} = V_{IN}		–50	--	50	nA
On-Resistance of High-Side MOSFET	R_{DSON_H}	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.28	--	Ω
			V_{IN} = 2.5V	--	0.38	--	
On-Resistance of Low-Side MOSFET	R_{DSON_L}	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.25	--	Ω
			V_{IN} = 2.5V	--	0.35	--	
High-Side Switch Current Limit	I_{LIM_H}	V_{IN} = 2.5V to 5.5V		1.4	2	2.6	A
EN Input Voltage Rising Threshold	V_{EN_R}			1.5	--	V_{IN}	V
EN Input Voltage Falling Threshold	V_{EN_F}			--	--	0.4	V
Undervoltage-Lockout Falling Threshold	V_{UVLO_F}			--	1.8	--	V
Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}			--	0.1	--	V
Oscillator Frequency	f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA		1.2	1.5	1.8	MHz
Over-Temperature Protection	T_{OTP}			--	160	--	°C
Maximum Duty Cycle	D_{MAX}			100	--	--	%
SW Current Source	I_{SW}	V_{IN} = 3.6V, V_{SW} = 0V or V_{SW} = 3.6V		1	--	100	μA
Minimum On-Time	t_{ON_MIN}			--	120	140	ns

Note 6. V_{OUT_ACC} = I_{OUT} x R_{DSON_H}

Note 7. Guaranteed by design.

Note 8. The start-up time is about 300μs.

13 Typical Application Circuit

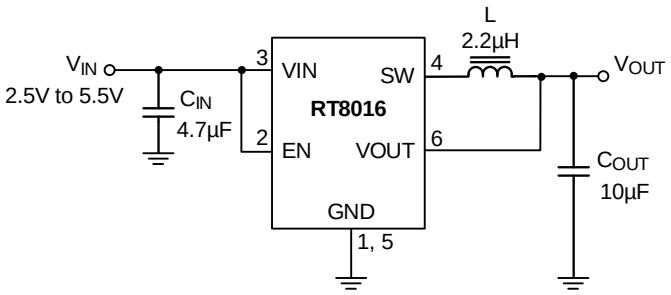
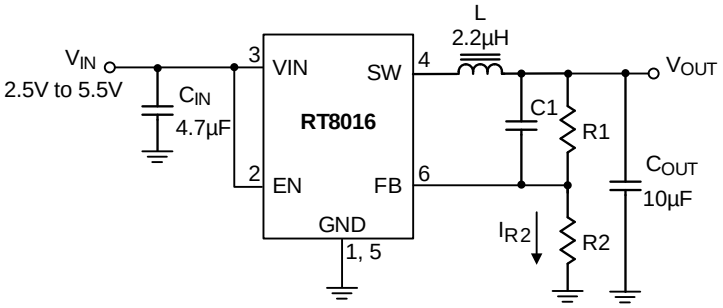


Figure 1. Fixed Voltage Regulator



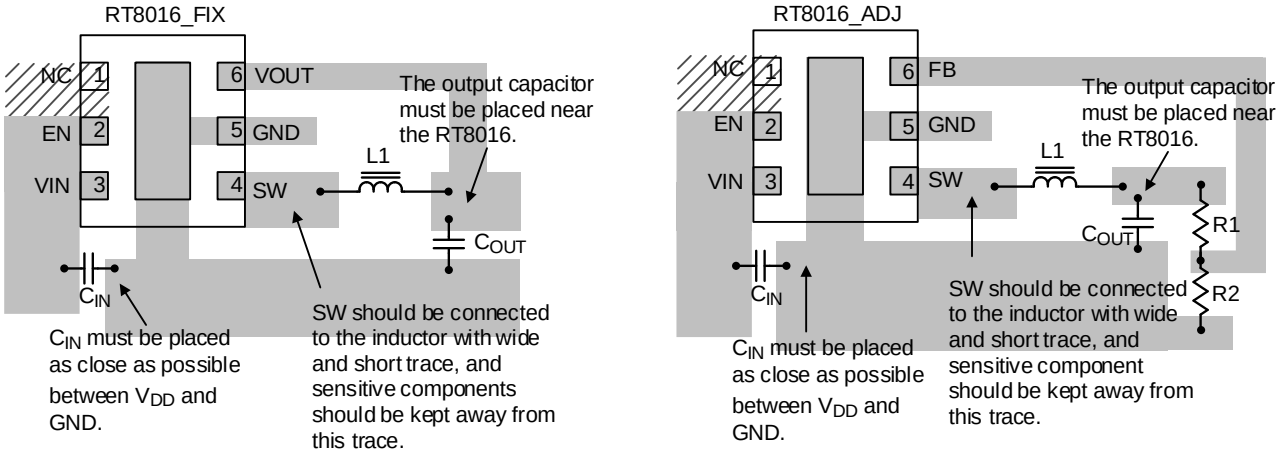
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 = 300kΩ to 60kΩ, so the I_{R2} = 2µA to 10µA

(R1 x C1) should be in the range between $3x10^{-6}$ and $6x10^{-6}$ for component selection.

Figure 2. Adjustable Voltage Regulator

13.1 Layout Guide



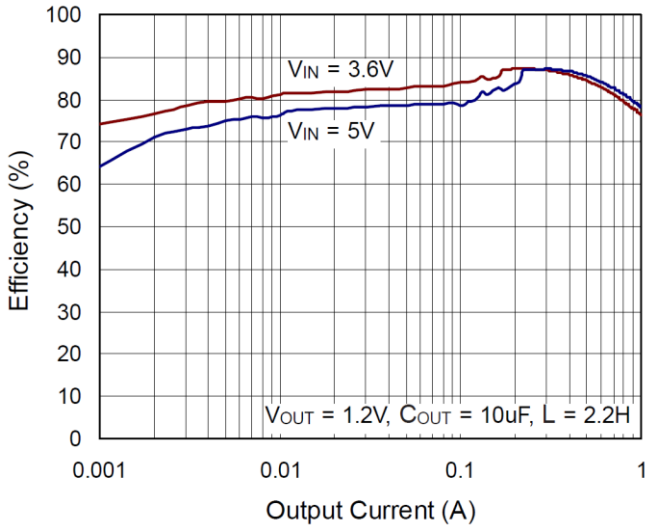
Note 9.

- The distance between C_{IN} and V_{IN} should be as short as possible (under 2mm).
- C_{OUT} should be placed near the RT8016.

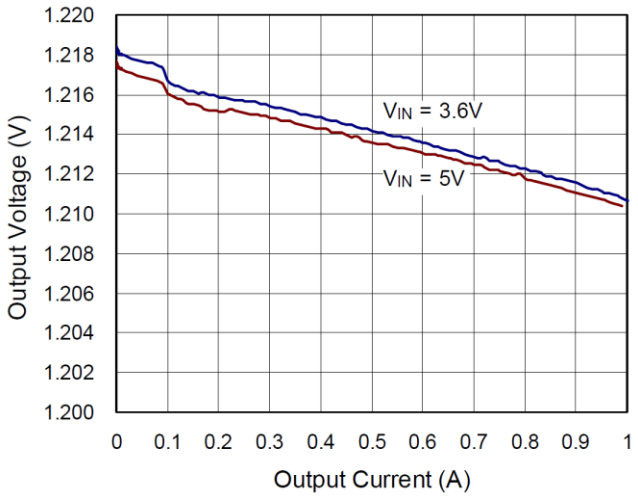
Figure 3. Layout Guide for the RT8016

14 Typical Operating Characteristics

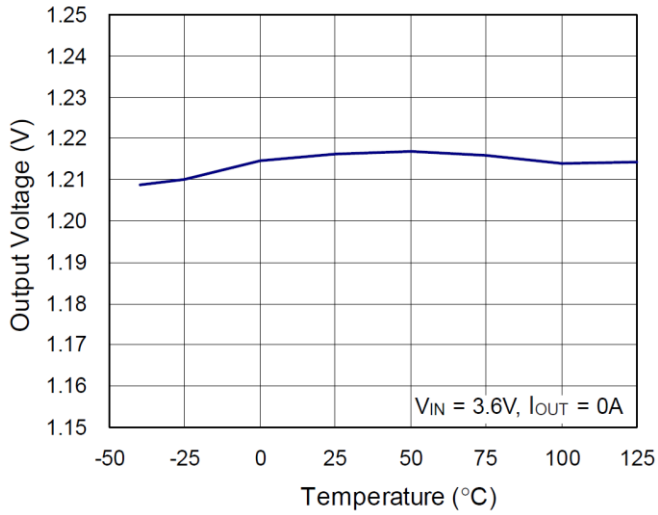
Efficiency vs. Output Current



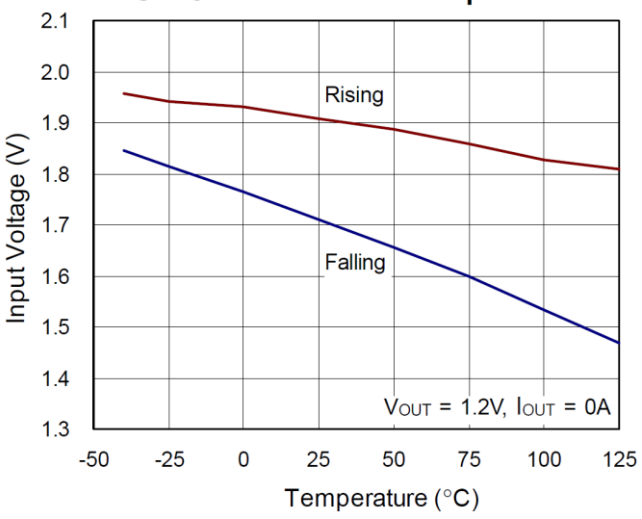
Output Voltage vs. Output Current



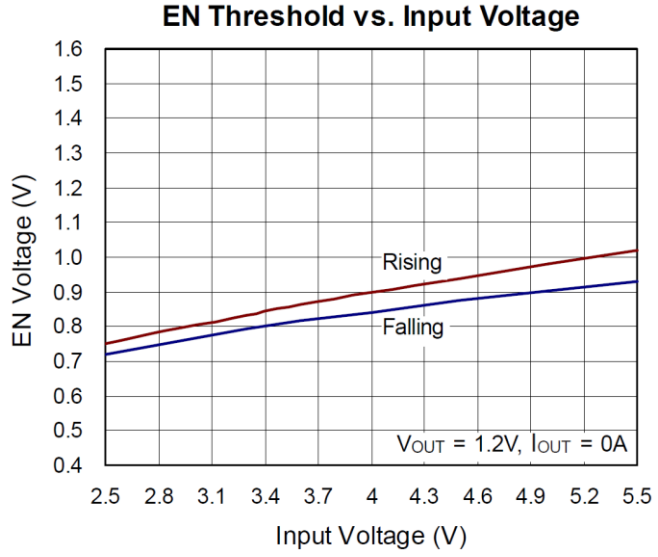
Output Voltage vs. Temperature



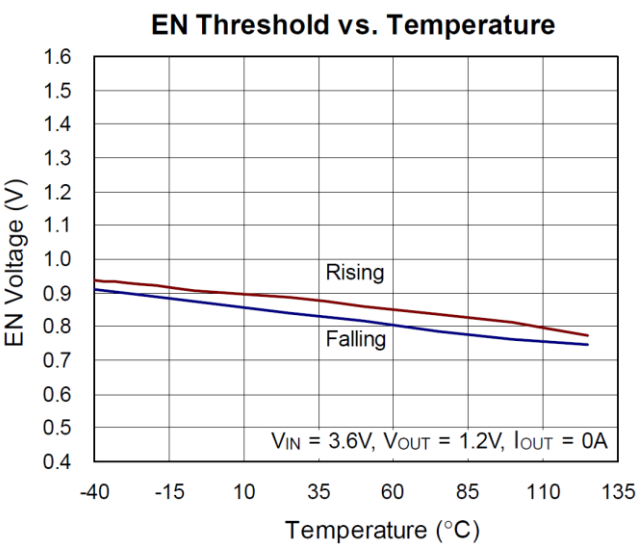
UVLO Threshold vs. Temperature



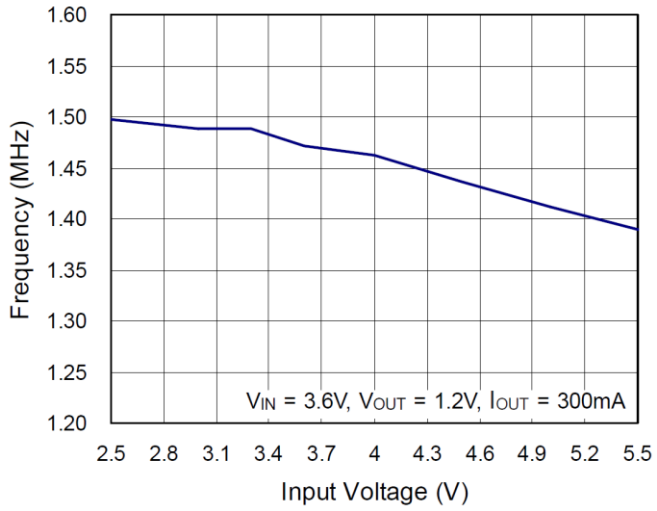
EN Threshold vs. Input Voltage



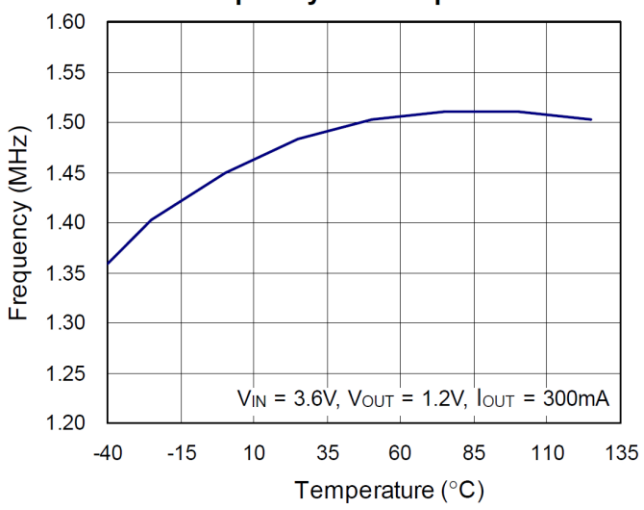
EN Threshold vs. Temperature



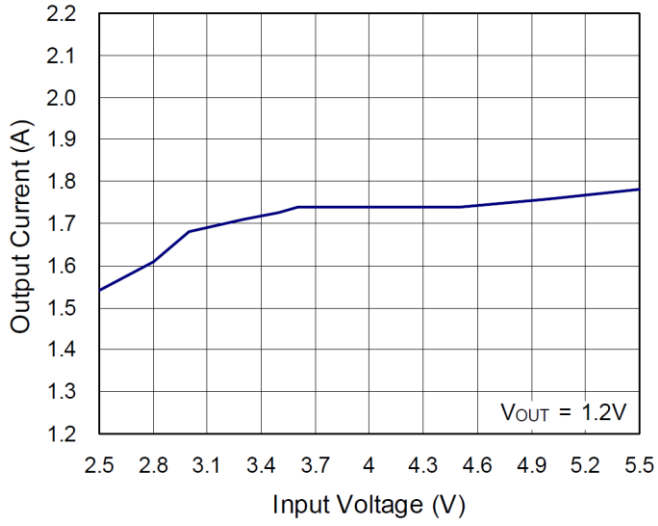
Frequency vs. Input Voltage



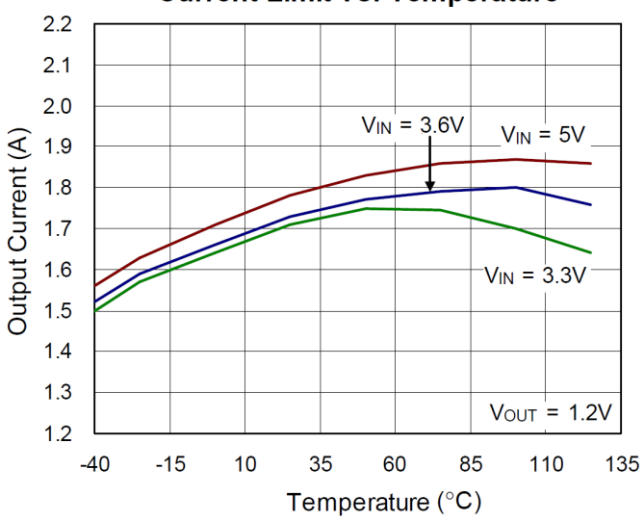
Frequency vs. Temperature



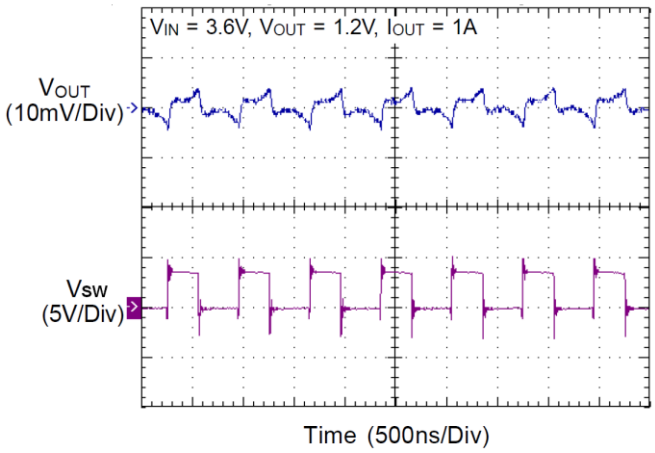
Current Limit vs. Input Voltage



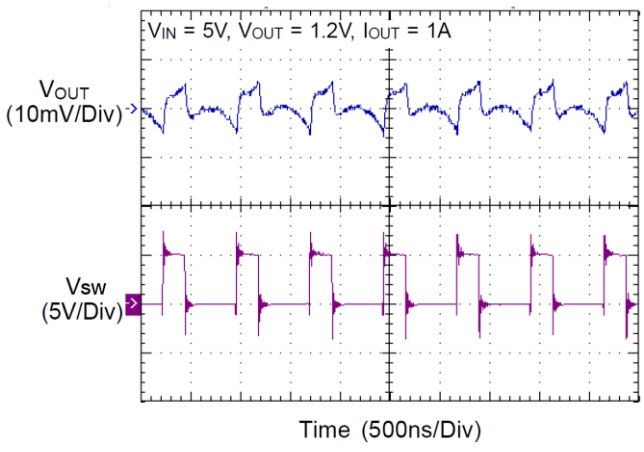
Current Limit vs. Temperature



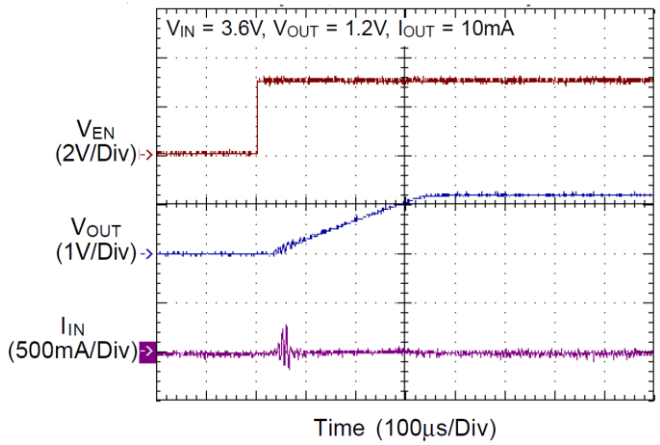
Output Ripple Voltage



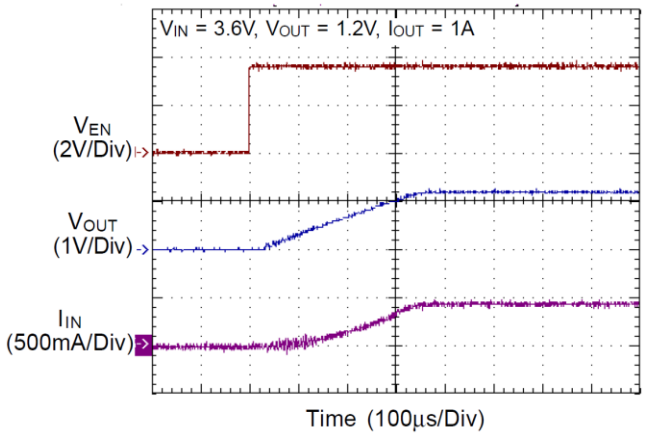
Output Ripple Voltage



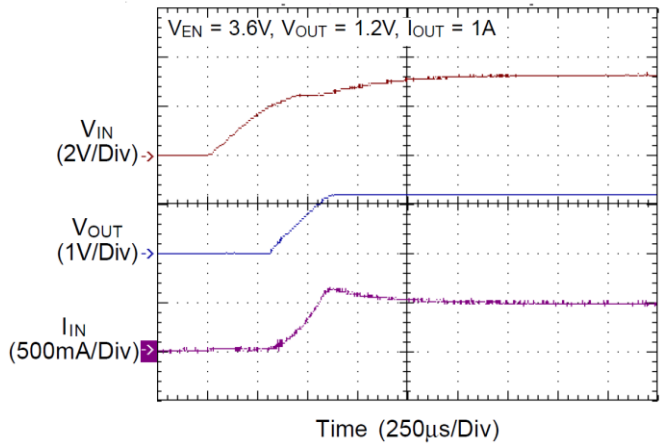
Power On from EN



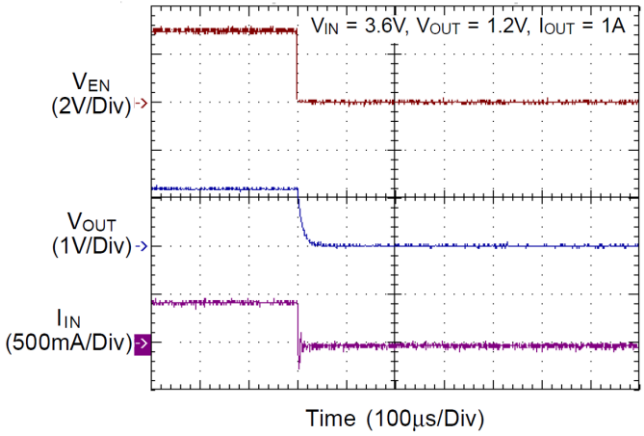
Power On from EN



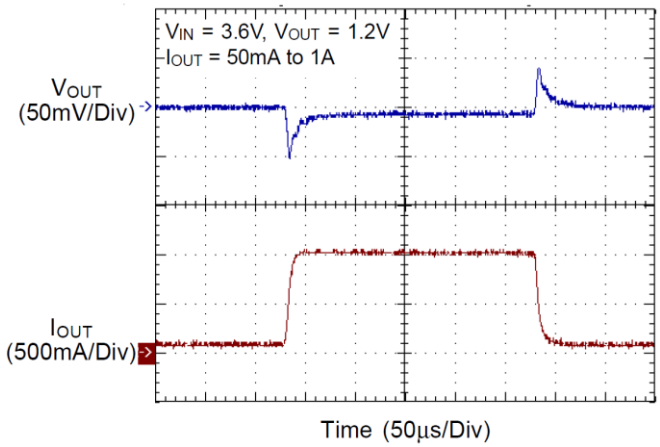
Power On from VIN



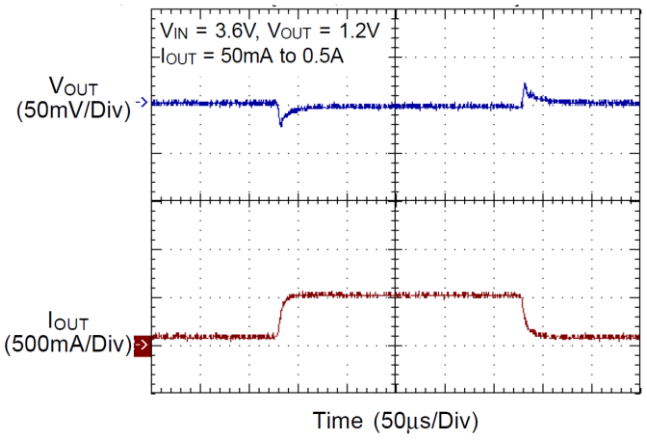
Power Off from EN

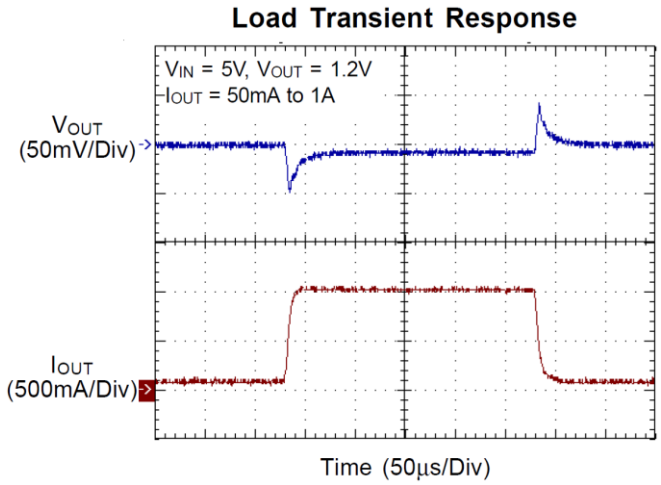


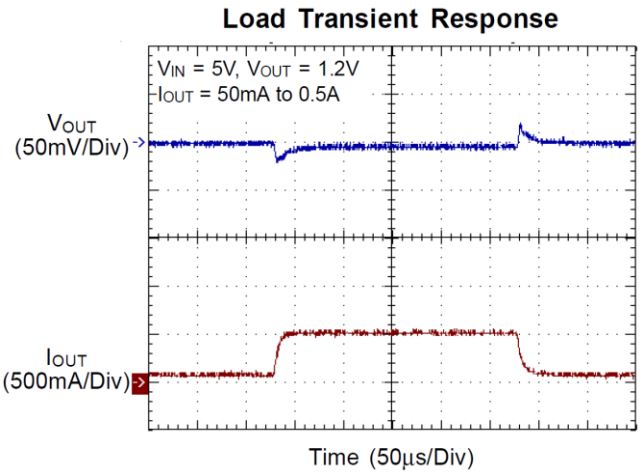
Load Transient Response



Load Transient Response







15 Application Information

(Note 10)

The basic RT8016 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency, followed by C_{IN} and C_{OUT}.

15.1 Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current (ΔI_L) increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. The highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is ΔI_L = 0.4 (I_{MAX}). The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

15.2 Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low-cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard” which means that once the magnetic flux density exceeds a certain level, the inductance drops rapidly, and the core cannot store much more energy. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Different core materials and shapes will change the size/ current and price/current relationship of an inductor.

Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

15.3 C_{IN} and C_{OUT} Selection

The input capacitance, CIN, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much difference. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

15.4 Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

15.5 Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 4.

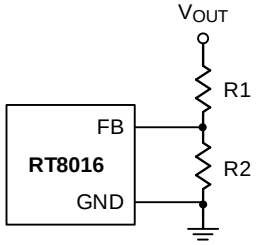


Figure 4. Setting the Output Voltage

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = V_{REF}(1+\frac{R1}{R2})$$

where V_{REF} is the internal reference voltage (0.6V typical).

15.6 Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L_{loss1} + L_{loss2} + L_{loss3} + ...)

where L_{loss1}, L_{loss2}, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses.

The VIN quiescent current loss dominates the efficiency loss at light load currents whereas the I^2R loss dominates the efficiency loss at medium to heavy currents. In a typical efficiency plot, the efficiency curve at light load currents can be misleading since the actual power lost is of no consequence.

1. The VIN quiescent current appears due to two factors: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground.

The resulting ΔQ/Δt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode,

$I_{GATECHG}$ = f(Q_T + Q_B)

where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor R_L. In continuous mode, the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both high-side MOSFET (R_{DSON_H}) and low-side MOSFET (R_{DSON_L}) and the duty cycle (D) as follows:

R_{SW} = R_{DSON_H} x D + R_{DSON_L} x (1 – D)

The R_{DSON} for both the high-side and low-side MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% of the total loss.

15.7 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)}$ = ($T_{J(MAX)}$ – T_A) / θ_{JA}

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-6L 2x2 package, the thermal resistance, θ_{JA}, is 165°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for a WDFN-6L 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

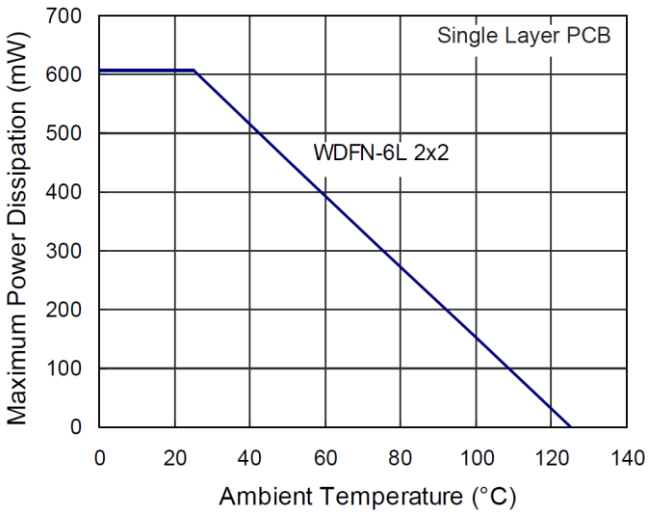


Figure 5. Derating Curve of Maximum Power Dissipation

15.8 Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

15.9 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8016.

- For the main current paths as indicated in bold lines in Figure 6, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- The SW node has a high-frequency voltage swing and should be kept to a small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect the feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8016.
- Connect all analog grounds to a common node and then connect the common node to the power ground behind the output capacitors.
- An example of a 2-layer PCB layout is shown in Figure 7 to Figure 8 for reference.

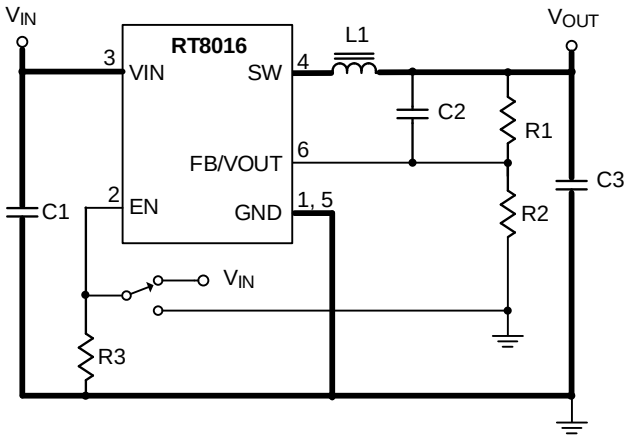


Figure 6. EVB Schematic

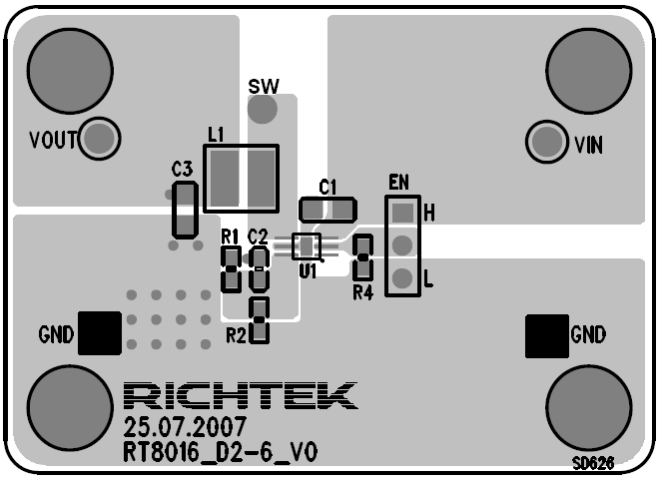


Figure 7. Top Layer

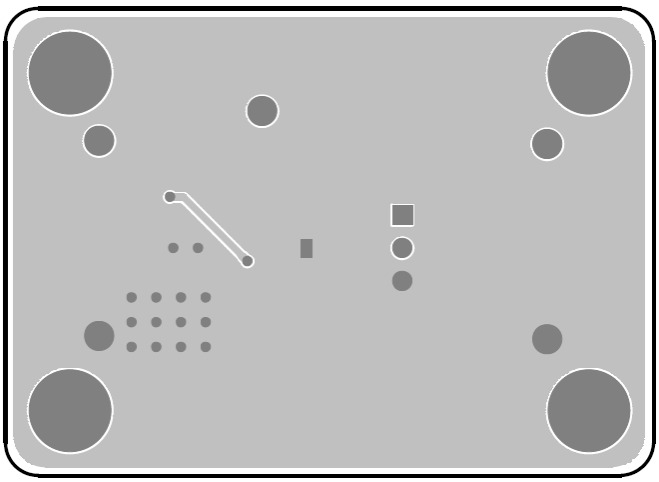


Figure 8. Bottom Layer

Table 1. Recommended Inductors

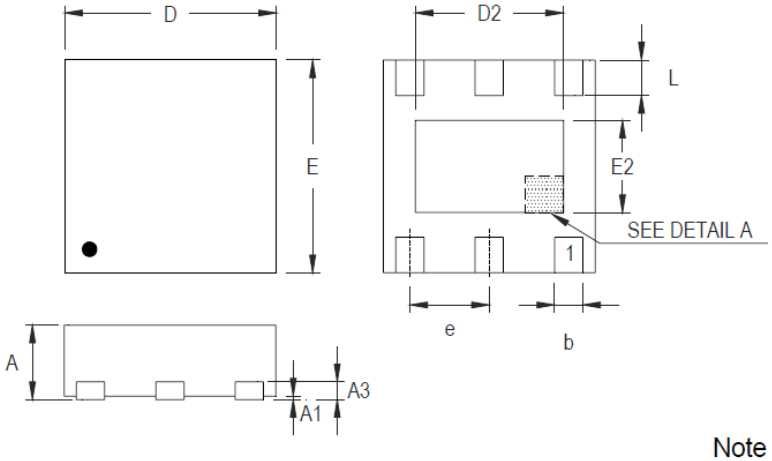
Supplier	Inductance (μH)	Current Rating (mA)	DCR (mΩ)	Dimensions (mm)	Series
TAIYO YUDEN	2.2	1480	60	3.00 x 3.00 x 1.50	NR 3015
GOTREND	2.2	1500	58	3.85 x 3.85 x 1.80	GTSD32
Sumida	2.2	1500	75	4.50 x 3.20 x 1.55	CDRH2D14
Sumida	4.7	1000	135	4.50 x 3.20 x 1.55	CDRH2D14
TAIYO YUDEN	4.7	1020	120	3.00 x 3.00 x 1.50	NR 3015
GOTREND	4.7	1100	146	3.85 x 3.85 x 1.80	GTSD32

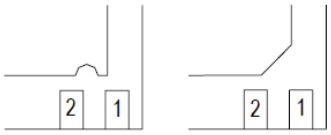
Table 2. Recommended Capacitors for C_{IN} and C_{OUT}

Supplier	Capacitance (μF)	Package	Part Number
TDK	4.7	603	C1608JB0J475M
MURATA	4.7	603	GRM188R60J475KE19
TAIYO YUDEN	4.7	603	JMK107BJ475RA
TAIYO YUDEN	10	603	JMK107BJ106MA
TDK	10	805	C2012JB0J106M
MURATA	10	805	GRM219R60J106ME19
MURATA	10	805	GRM219R60J106KE19
TAIYO YUDEN	10	805	JMK212BJ106RD

Note 10. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

16 Outline Dimension





DETAIL A

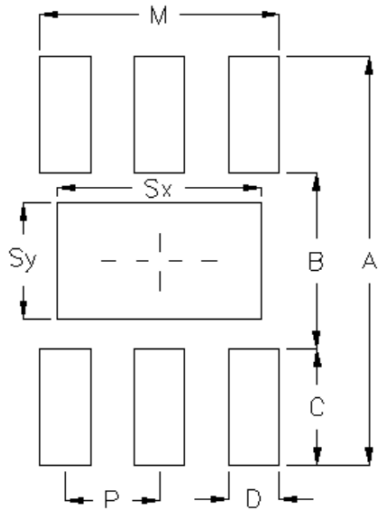
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

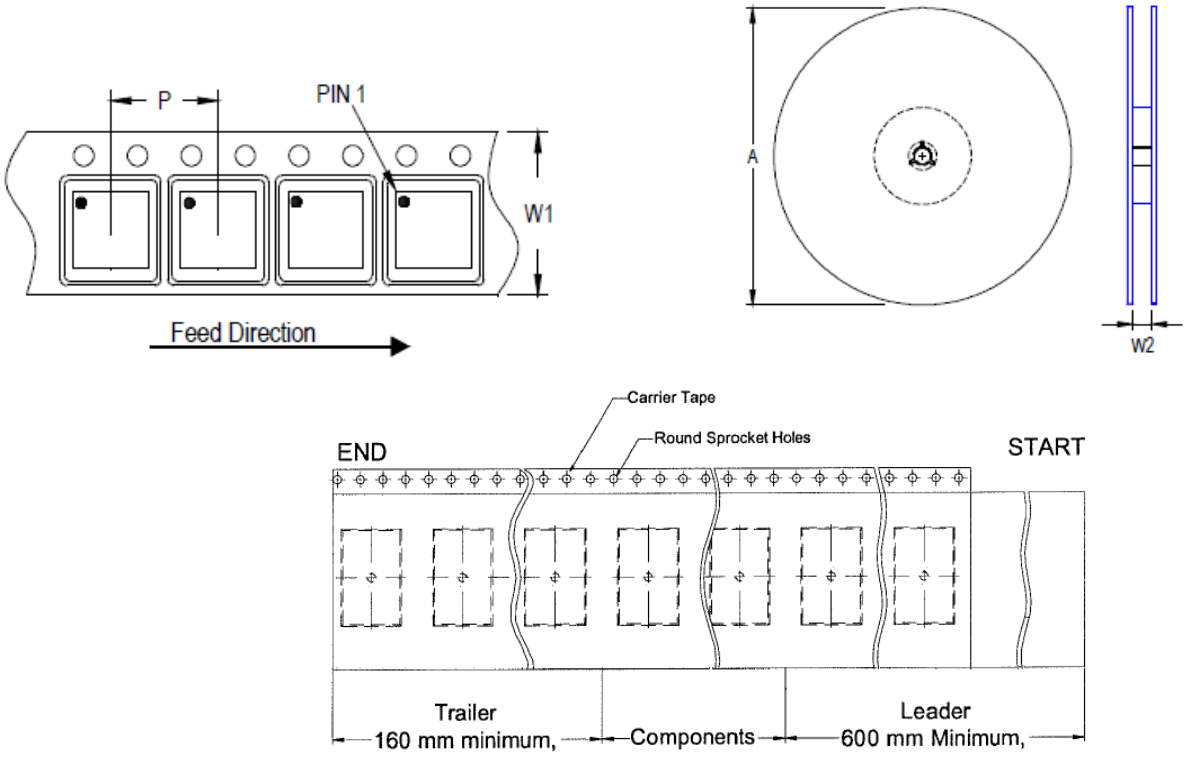
17 Footprint Information



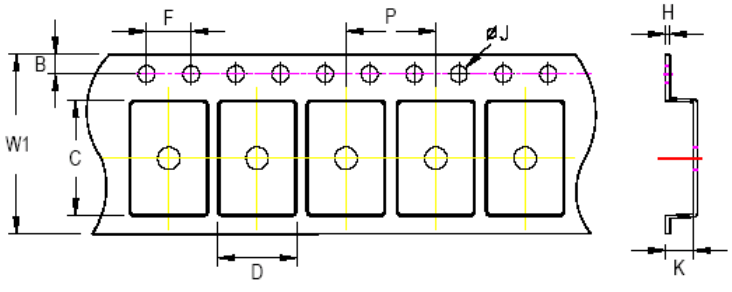
Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-6	6	0.65	2.80	1.20	0.80	0.35	1.40	0.80	1.65	±0.05

18 Packing Information

18.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

18.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
05	2024/10/17	Modify	*Changed the name of pin 4 to SW.* *General Description on page 1* -Added Temperature range *Ordering Information on page 1* -Modified description *Electrical Characteristics on page 4, 5* -Updated description and symbol *Application Information on page 16* -Added the declaration *Footprint Information on page 18* -Added footprint information *Packing Information on page 19, 20, 21* -Added packing information

20 Product Status

Part No.	Status	Package Type	Lead Plating System
RT8016XXGQW	Active	WDFN-6L 2x2 (W-Type)	Richtek Green Policy Compliant
RT8016XXPQW	EOL	WDFN-6L 2x2 (W-Type)	Pb Free

The product status values are defined as follows:

- **Active**: The device is in production and is recommended for new designs.
- **NRND**: Not recommended for new designs.
- **Last Time Buy**: The device will be discontinued, and a lifetime-buy period is in effect.
- **EOL**: Richtek has discontinued the production of the device.