RICHTEK®

RT8010/A

1.5MHz, 1A, High-Efficiency PWM Step-Down DC-DC Converter

1 General Description

The RT8010/A is a high-efficiency Pulse-Width-Modulated (PWM) step-down DC-DC converter, capable of delivering 1A output current over a wide input voltage range from 2.5V to 5.5V. The RT8010/A is ideally suited for portable electronic devices powered by a single-cell Li-ion battery or other power sources, such as cellular phones and hand-held devices.

Two operating modes are available: PWM/Low-Dropout auto-switch mode and shutdown mode. The internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss in PWM mode. No external Schottky diode is required for practical applications.

The RT8010/A enters Low-Dropout mode when normal PWM cannot provide a regulated output voltage by continuously turning on the upper P-MOSFET. The RT8010/A enters shutdown mode and consumes less than 0.1μA when the EN pin is pulled low.

The switching ripple is easily smoothed out by small package filtering elements due to a fixed operating frequency of 1.5MHz. This, along with the small WDFN-6L 2x2 and WQFN-16L 3x3 packages, provides for a small PCB area application. Other features include soft-start, a lower internal reference voltage with 2% accuracy, over-temperature protection, and overcurrent protection.

2 Applications

- Mobile Phones
- Personal Information Appliances
- Wireless Devices
- Portable Instruments

3 Features

- **2.5V to 5.5V Input Range**
- **Output Voltage (Adjustable Output from 0.6V to V_{IN})**
  - **RT8010: 1V, 1.2V, 1.5V, 1.6V, 1.8V, 2.5V and 3.3V Fixed Output Voltage/Adjustable Output Voltage**
  - **RT8010A Adjustable Output Voltage Only**
- **1A Output Current**
- **95% Efficiency**
- **No Schottky Diode Required**
- **1.5MHz Fixed-Frequency PWM Operation**
- **Small 6-Lead WDFN and 16-Lead WQFN Package**

4 Ordering Information

RT8010/A(-□□)□□□

Pin 1 Orientation
(3): Quadrant 3, Follow EIA-481
(Empty means Pin1 orientation is Quadrant 1)
(For RT8010AGQW Only)

Package Type(1)
QW : WDFN/WQFN (W-Type)

Lead Plating System
P: Pb Free
G: Richtek Green Policy Compliant(2)

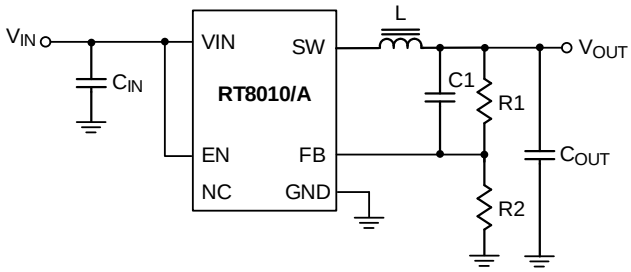
Output Voltage
Default : Adjustable (RT8010/A)
Fixed (RT8010)
10 : 1.0V
12 : 1.2V
15 : 1.5V
16 : 1.6V
18 : 1.8V
25 : 2.5V
33 : 3.3V

WQFN-16L 3x3
WDFN-6L 2x2

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

5 Simplified Application Circuit



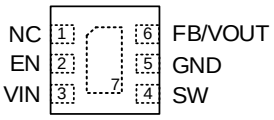
6 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

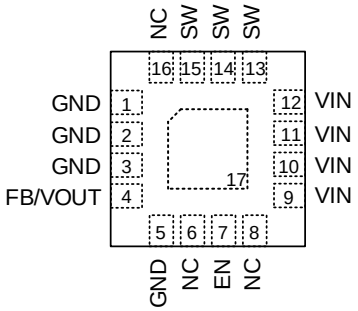
Table of Contents

7 Pin Configuration

(TOP VIEW)



WDFN-6L 2x2 (RT8010)

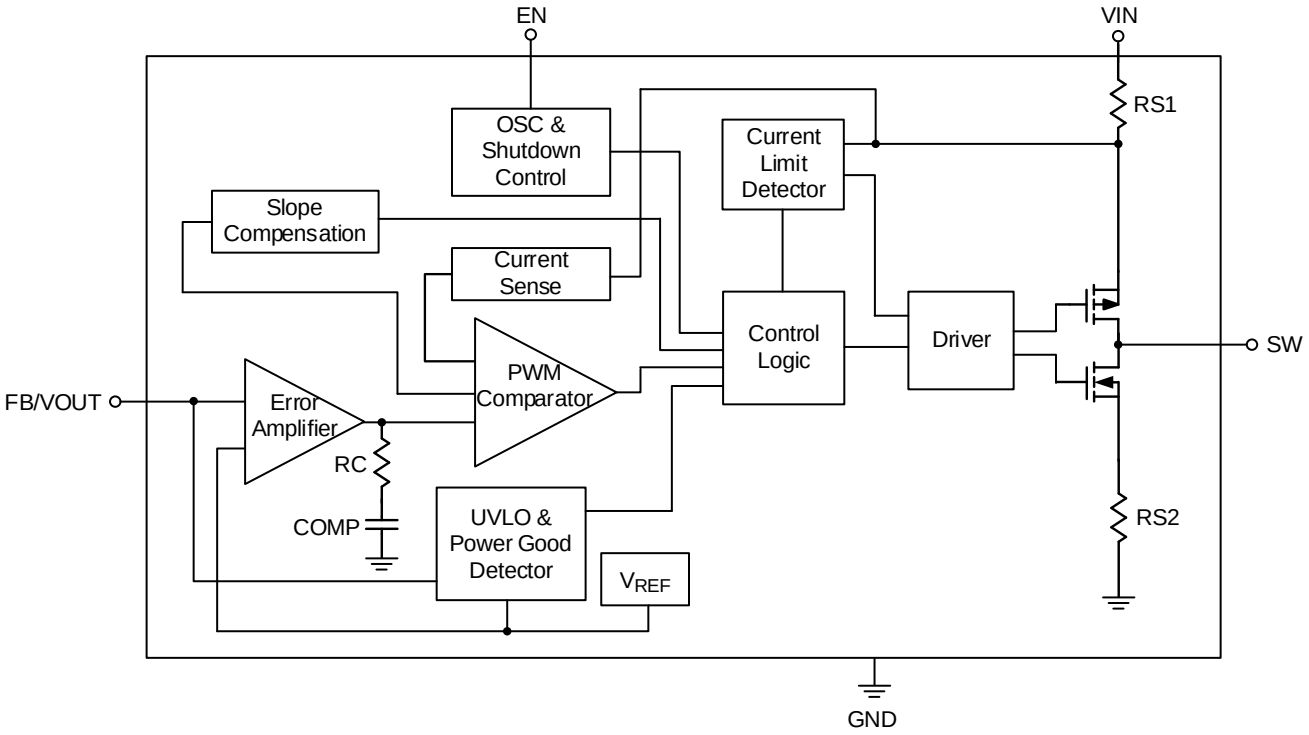


WQFN-16L 3x3 (RT8010A)

8 Functional Pin Description

Pin No.		Pin Name	Pin Function
RT8010	RT8010A		
1	6, 8, 16	NC	Internal connection. Leave this pin floating and do not connect to the IC pin.
2	7	EN	Enable control input. Logic high enables the converter.
3	9, 10, 11, 12	VIN	Power input. Support 2.5V to 5.5V input voltage. It is suggested to place decoupling input capacitors as close to the VIN and GND pins as possible. (For the RT8010A, Pins 9 and 10 must be connected to Pin 11).
4	13, 14, 15	SW	Switch node. Output switching state between high-side MOSFET and low-side MOSFET of the power converter. Connect the SW pin to the external inductor. (For the RT8010A, Pin 13 must be connected to Pin 14).
5	1, 2, 3, 5	GND	Ground.
6	4	FB/VOUT	Feedback/output voltage input pin. The pin is used to set the output voltage of the converter via a resistor divider. It is suggested to place the FB resistor divider as close to the FB pin as possible.
7 (Exposed Pad)	17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage ---------- 6.5V
- EN, FB Pin Voltage ---------- –0.3V to V_{IN}
- SW Pin Switch Voltage ---------- –0.3V to (V_{IN} + 0.3V
  <20ns ---------- –4.5V to 7.5V
- SW Pin Switch Current ----------2A
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-6L 2x2 ---------- 0.833W
  WQFN-16L 3x3---------- 1.47W
- Package Thermal Resistance (Note 3)
  WDFN-6L 2x2, θ_{JA} ---------- 120°C/W
  WDFN-6L 2x2, θ_{JC} ---------- 20°C/W
  WQFN-16L 3x3, θ_{JA}---------- 68°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model)---------- 2Kv

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 2.5V, L = 2.2μH, C_{IN} = 4.7μF, C_{OUT} = 10μF, T_A = 25°C, I_{MAX} = 1A unless otherwise specified.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
VIN Supply Input Voltage		V_{IN}			2.5	--	5.5	V
Quiescent Current		I_Q	I_{OUT} = 0mA, V_{FB} = V_{REF} + 5%		--	50	70	μA
Shutdown Current		I_{SHDN}	EN = GND		--	0.1	1	μA
Reference Voltage		V_{REF}	For adjustable output voltage		0.588	0.6	0.612	V
Adjustable Output Range		V_{OUT}	(Note 6)		V_{REF}	--	V_{IN} – 0.2V	V
Output Voltage Accuracy	Fix	ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1V 0A < I_{OUT} < 1A		–3	--	3	%
		ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.2V 0A < I_{OUT} < 1A		–3	--	3	
		ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.5V 0A < I_{OUT} < 1A		–3	--	3	
		ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.6V 0A < I_{OUT} < 1A		–3	--	3	
		ΔV_{OUT}	V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.8V 0A < I_{OUT} < 1A		–3	--	3	
Output Voltage Accuracy	Fix	ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 7) V_{OUT} = 2.5V, 0A < I_{OUT} < 1A		–3	--	3	%
		ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 7) V_{OUT} = 3.3V, 0A < I_{OUT} < 1A		–3	--	3	
	Adjustable	ΔV_{OUT}	V_{IN} = V_{OUT} + ΔV to 5.5V (Note 7) 0A < I_{OUT} < 1A		–3	--	3	%
FB Input Current		I_{FB}	V_{FB} = V_{IN}		–50	--	50	nA
On-Resistance of P-MOSFET		$R_{DS(ON)\_P}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.28	--	Ω
				V_{IN} = 2.5V	--	0.38	--	
On-Resistance of N-MOSFET		$R_{DS(ON)\_N}$	I_{OUT} = 200mA	V_{IN} = 3.6V	--	0.25	--	Ω
				V_{IN} = 2.5V	--	0.35	--	
P-Channel Current Limit		I_{LIM_P}			1.4	2.1	3.2	A
EN Input Voltage Rising threshold		V_{EN_R}	V_{IN} = 2.5V to 5.5V		1.5	--	--	V
EN Input Voltage Falling threshold		V_{EN_F}	V_{IN} = 2.5V to 5.5V		--	--	0.4	
Undervoltage Lockout threshold		V_{UVLO}			--	1.8	--	V
Undervoltage Lockout threshold Hysteresis					--	0.1	--	V
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V, I_{OUT} = 100mA		1.2	1.5	1.8	MHz
Over-Temperature Protection Threshold		T_{OTP}			--	160	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Duty Cycle			100	--	--	%
SW Leakage Current		V_{IN} = 3.6V, V_{SW} = 0V or V_{SW} = 3.6V	–1	--	1	μA

Note 6. Guaranteed by design.

Note 7. $\Delta V = I_{OUT} \times P_{RDS(ON)}$.

13 Typical Application Circuit

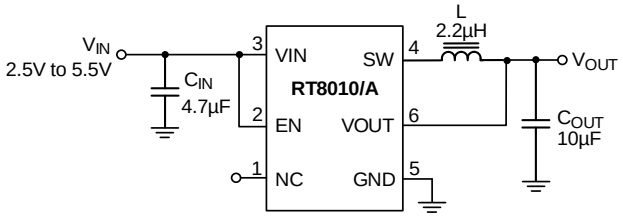


Figure 1. Fixed Voltage Regulator

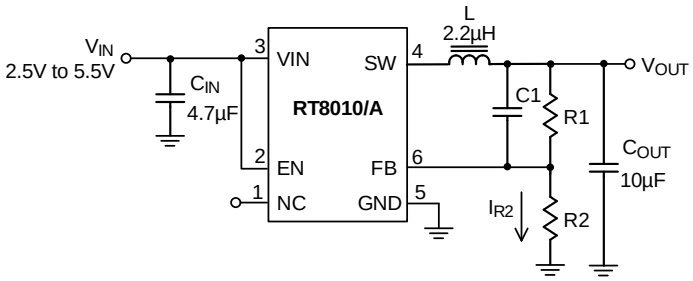


Figure 2. Adjustable Voltage Regulator

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 = 300kΩ to 60kΩ, the I_{R2} = 2µA to 10µA

(R1 x C1) should be in the range between $3x10^{-6}$ and $6x10^{-6}$ for component selection.

13.1 Layout Guide

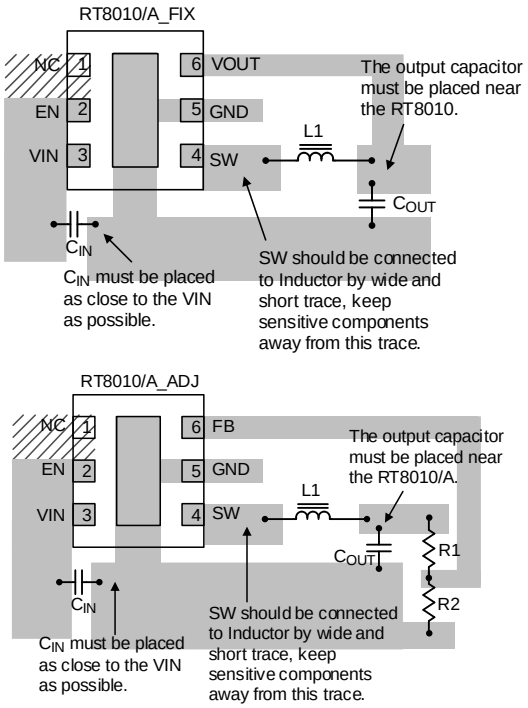


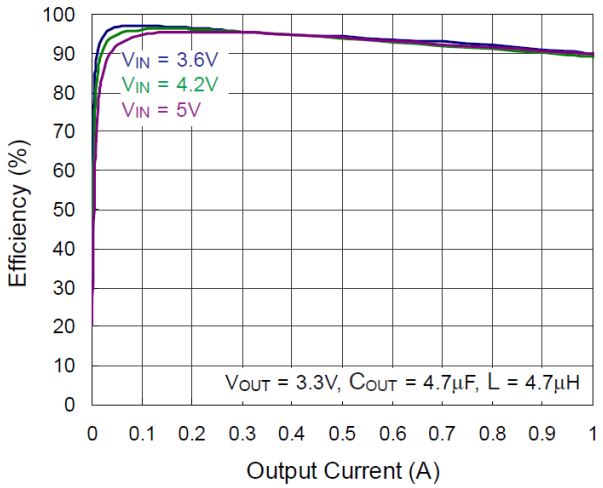
Figure 3

Layout note:

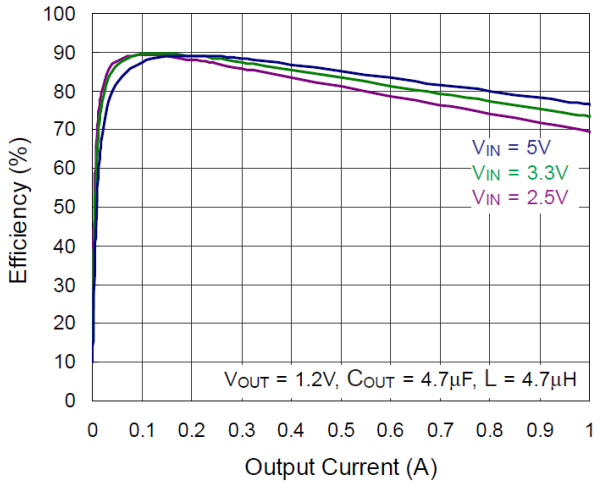
1. The distance between C_{IN} and V_{IN} should be as close as possible (under 2mm)
2. C_{OUT} should be placed near RT8010/A.

14 Typical Operating Characteristics

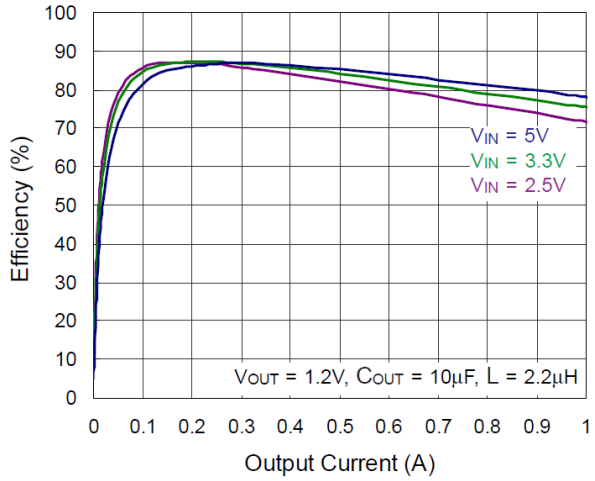
Efficiency vs. Output Current



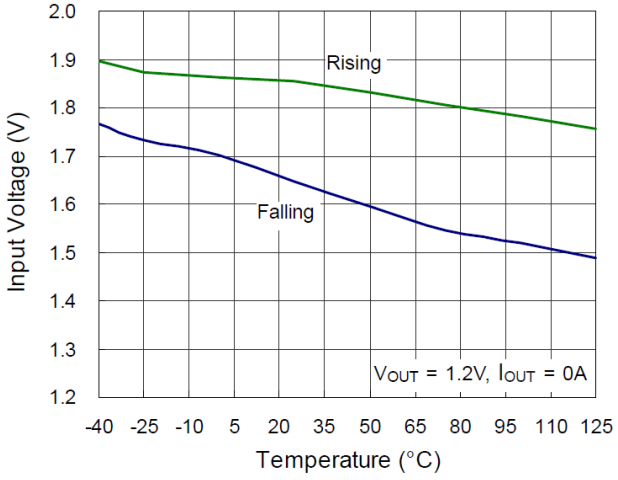
Efficiency vs. Output Current



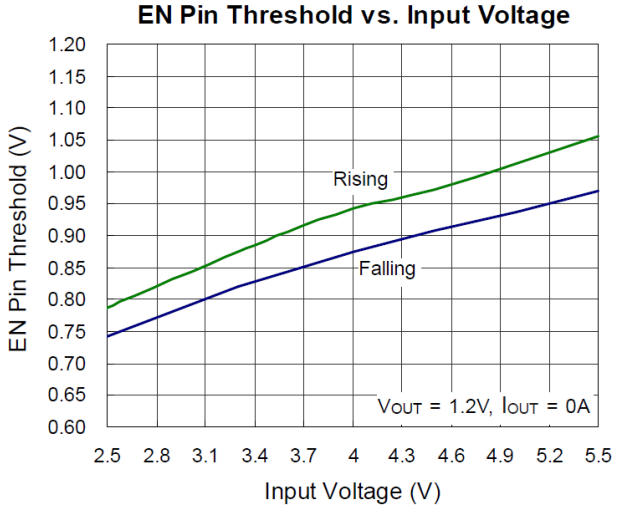
Efficiency vs. Output Current



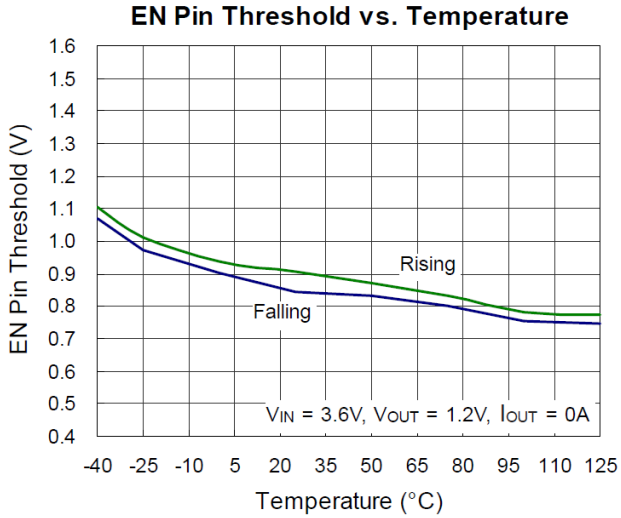
UVLO Voltage vs. Temperature



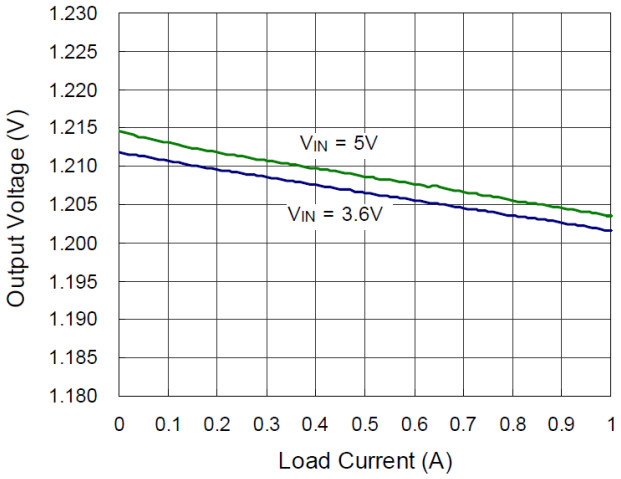
EN Pin Threshold vs. Input Voltage



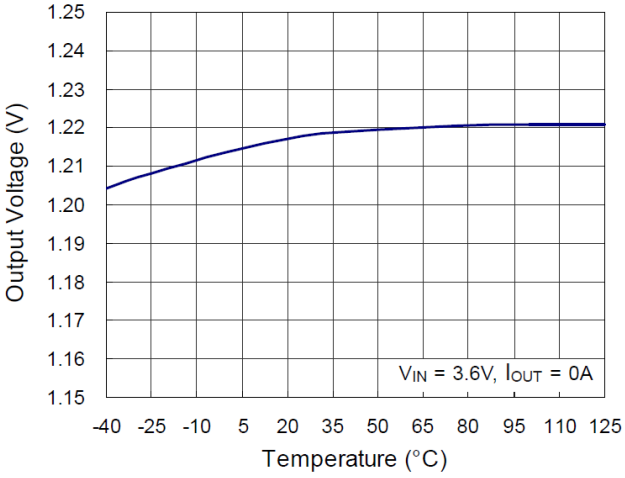
EN Pin Threshold vs. Temperature



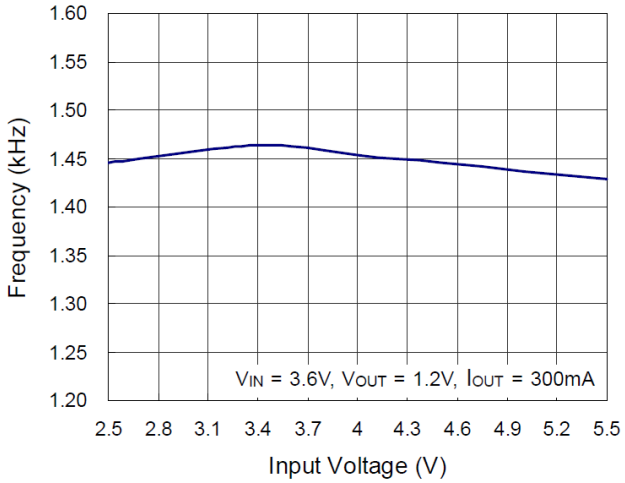
Output Voltage vs. Load Current



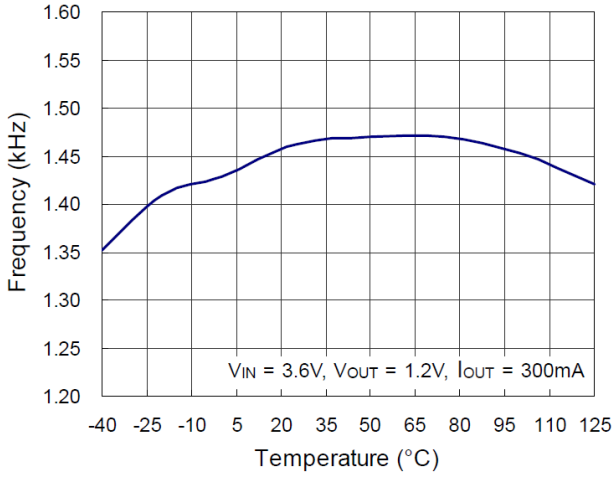
Output Voltage vs. Temperature



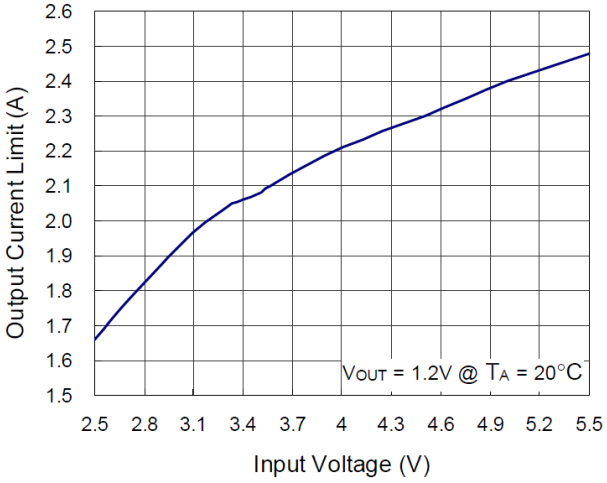
Frequency vs. Input Voltage



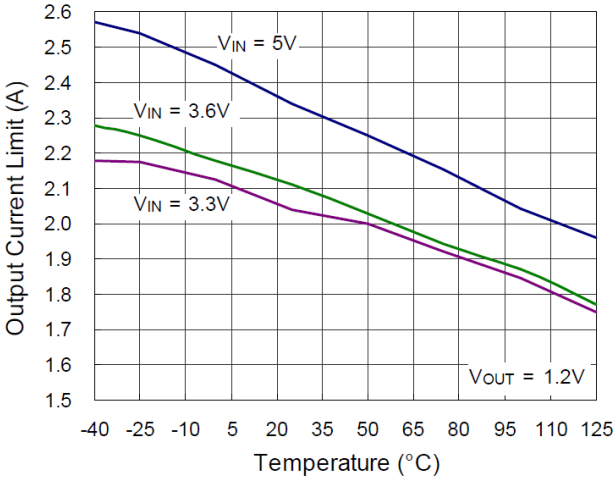
Frequency vs. Temperature



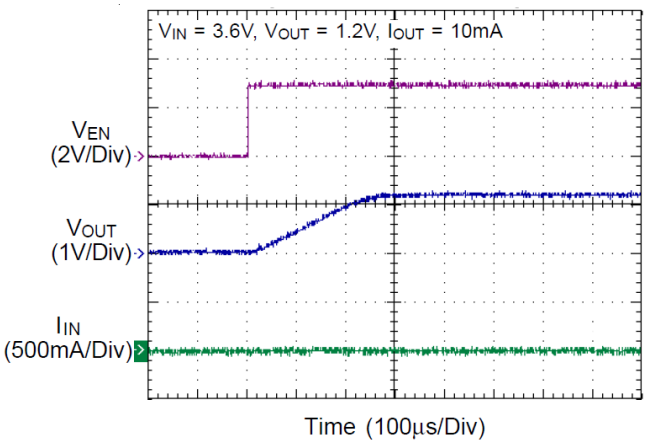
Output Current Limit vs. Input Voltage



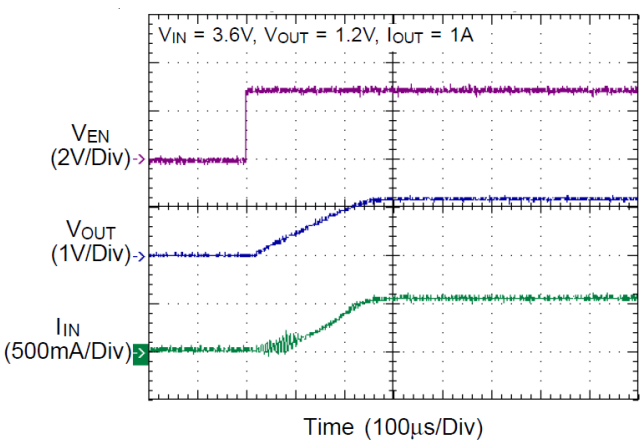
Output Current Limit vs. Temperature



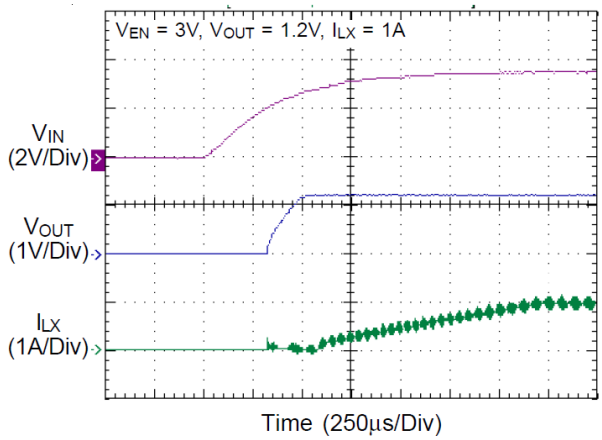
Power On from EN



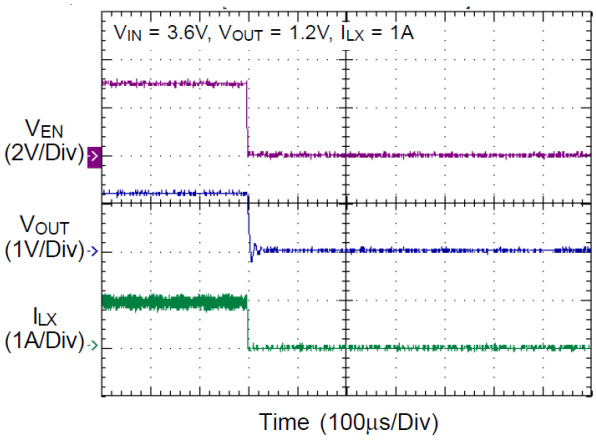
Power On from EN



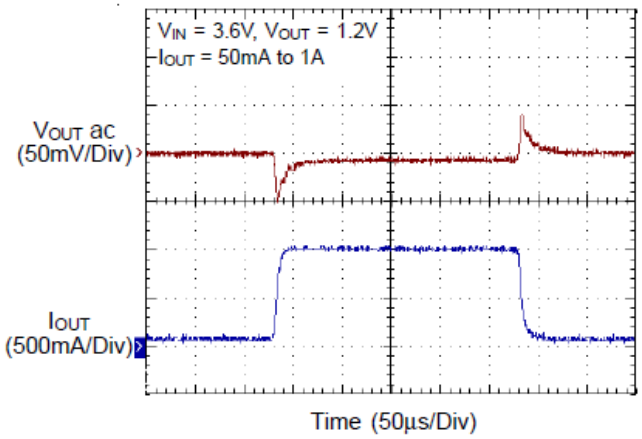
Power On from VIN



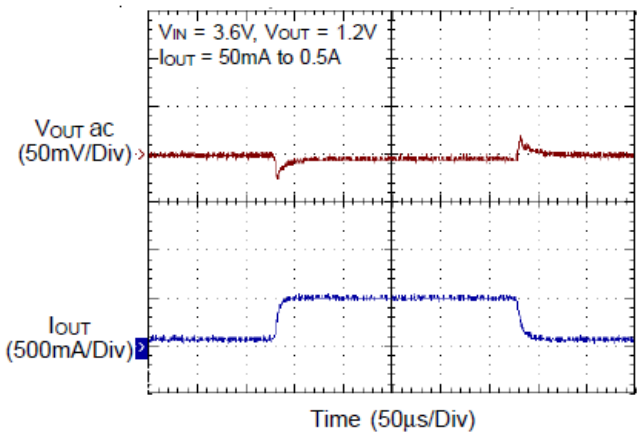
Power Off from EN



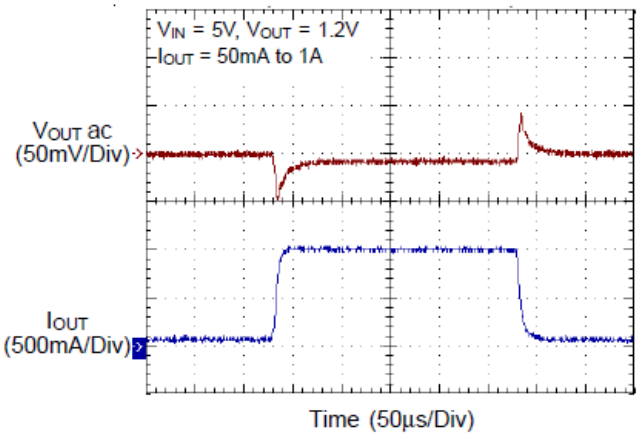
Load Transient Response



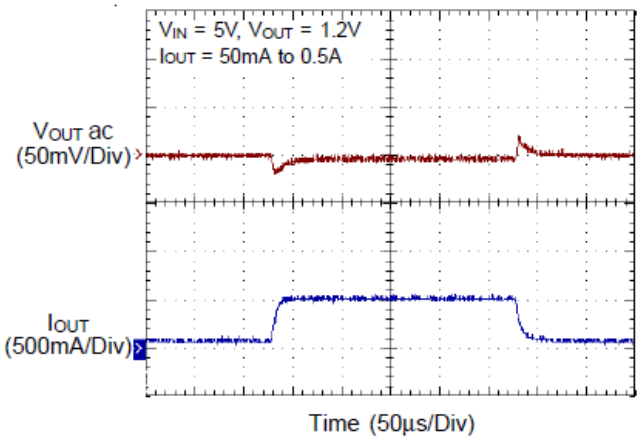
Load Transient Response



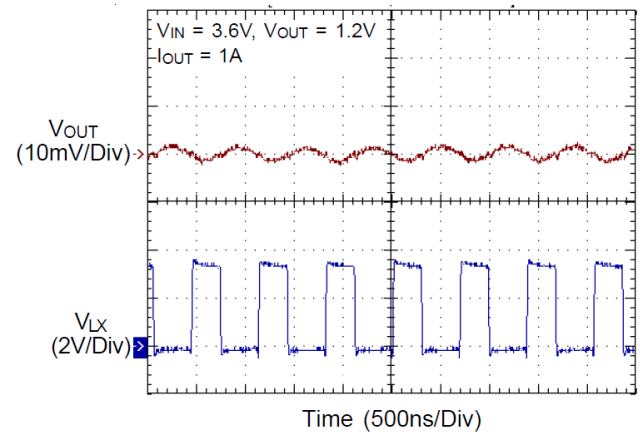
Load Transient Response



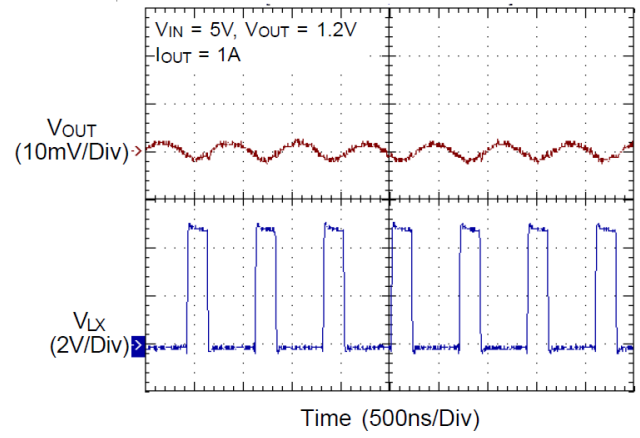
Load Transient Response



Output Ripple Voltage



Output Ripple Voltage



15 Application Information

(Note 8)

The basic RT8010/A application circuit is shown in Typical Application Circuit section. The selection of external components is determined by the maximum load current, starting with the choice of inductor value and operating frequency, followed by the selection of C_{IN} and C_{OUT}.

15.1 Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with a higher inductance value.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. The highest efficiency operation is achieved at a low frequency with a small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN} condition. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

15.2 Inductor Core Selection

Once the value of inductor is known, the type of inductor must be selected. High-efficiency converters generally cannot afford the core loss found in low-cost powdered iron cores, which necessitates the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is highly dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and, therefore, copper losses will increase.

Ferrite cores are indeed known for their low core losses at high switching frequencies, which makes them suitable for high-efficiency power converters where minimizing copper loss and avoiding core saturation are critical design goals. Ferrite core materials exhibit "hard" saturation characteristics, meaning that their inductance can collapse abruptly when the peak design current is exceeded. This can lead to a significant increase in inductor ripple current and subsequent output voltage ripple, which is undesirable in power converter applications. Therefore, it is crucial to design the power converter in such a way that the core does not reach saturation under normal operating conditions.

Different core materials and shapes will change the size/current and price/current relationship of an inductor.

Toroid or shielded pot cores made of ferrite or permalloy materials are small and do not radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style of inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements.

15.3 C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low-ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula reaches a maximum when $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is

commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings from capacitor manufacturers are often based on only 2,000 hours of life, which makes it advisable to further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the Equivalent Series Resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response, as described in a later section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at the maximum input voltage since the ripple current (ΔI_L) increases with the input voltage. Multiple capacitors placed in parallel may be required to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface-mount packages. Special polymer capacitors offer very low ESR but have a lower capacitance density compared to other types. Tantalum capacitors have the highest capacitance density, but it is crucial to use only types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications, provided that ripple current ratings and long-term reliability are carefully considered. Ceramic capacitors have excellent low ESR characteristics but can exhibit a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors, combined with trace inductance, can also lead to significant ringing.

15.4 Considerations When Using Ceramic Input and Output Capacitors

Higher-value, lower-cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current capacity, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken for loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the component.

15.5 Output Voltage Programming

The resistive divider allows the FB pin to sense a fraction of the output voltage, as shown in Figure 4.

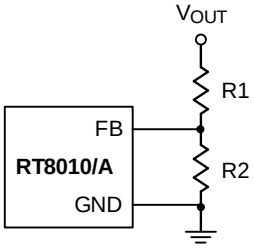


Figure 4. Output Voltage Setting

For adjustable voltage mode, the output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = V_{REF} \left(1 + \frac{R1}{R2} \right)$$

where V_{REF} is the internal reference voltage (0.6V typical)

15.6 Detailed Analysis of Efficiency Losses in Switching Regulators

The efficiency of a switching regulator is equal to the output power divided by the input power, multiplied by 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change will produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1+ L2+ L3+ ...)

where L1, L2, etc., represent the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: VIN quiescent current and I^2R losses.

The VIN quiescent current loss predominates in the efficiency loss at very low load currents, whereas the I^2R loss is the main contributor to efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading, as the actual power lost is negligible.

1. The VIN quiescent current arises due to two factors: the DC bias current, as specified in the electrical characteristics, and the gate charge currents of the internal main switch and synchronous switch. The gate charge current is the result of switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low and back to high, a packet of charge ΔQ is transferred from V_{IN} to ground.

The resulting $\Delta Q/\Delta t$, which is the current out of VIN, is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_{SW} (Q_T + Q_B)$,

where Q_T and Q_B represent the gate charges of the internal top and bottom switches, respectively. Both the DC bias and gate charge losses are proportional to VIN, and thus their effects will be more pronounced at higher supply voltages

2. I^2R losses are calculated from the resistances of the internal switches, denoted as R_{SW}, and the external inductor, denoted as R_L. In continuous mode, the average output current flowing through inductor L is 'chopped' between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both the top and bottom MOSFET $R_{DS(ON)}$ and the Duty Cycle (DC), as follows:

$R_{SW} = R_{DS(ON)\_H} \times DC + R_{DS(ON)\_L} \times (1 - DC)$

The $R_{DS(ON)}$ values for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves in the datasheet. Thus, to calculate the I^2R losses, simply add the resistance of the internal switches, R_{SW}, to the resistance of the external inductor, R_L, and multiply the result by the square of the average output current.

Other losses, including those due to the ESR of input and output capacitors (C_{IN} and C_{OUT}) and inductor core losses, generally account for less than 2% of the total loss.

15.7 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-6L 2x2 package, the thermal resistance, θ_{JA}, is 120°C/W on a standard JEDEC 51-7 high effective-thermal-

conductivity four-layer test board. For a WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 68°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for a WDFN-6L 2x2 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C /W) = 1.47W for a WQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 5 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

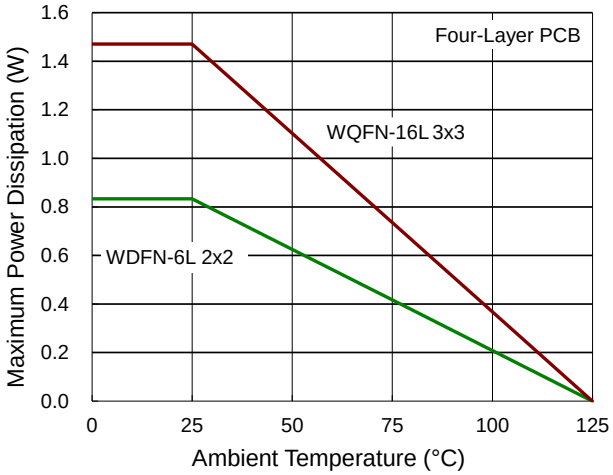


Figure 5. Derating Curve of Maximum Power Dissipation

15.8 Evaluating Load Transient Response

The regulator's loop response can be evaluated by examining the load transient response. Switching regulators typically require several cycles to adjust to a step change in load current. When a load step occurs, the output voltage (V_{OUT}) immediately shifts by an amount equal to the ΔI_{LOAD}(ESR), where ESR is the equivalent series resistance of C_{OUT}. Concurrently, ΔI_{LOAD} starts to charge or discharge C_{OUT}, which generates a feedback error signal that the regulator uses to bring V_{OUT} back to its steady-state value. During the period of recovery, V_{OUT} can be monitored for overshoot or ringing, as these can be indicators of stability issues.

15.9 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT8010/A.

- For the main current paths as indicated in bold lines in Figure 6, keep their traces short and wide.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- The SW node experiences high-frequency voltage swings and should have a small area to minimize parasitic effects. Keep analog components away from the SW node to prevent the pickup of stray capacitive noise.
- Connect the feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8010/A.

An example of 2-layer PCB layout is shown in Figure 7 to Figure 8 for reference.

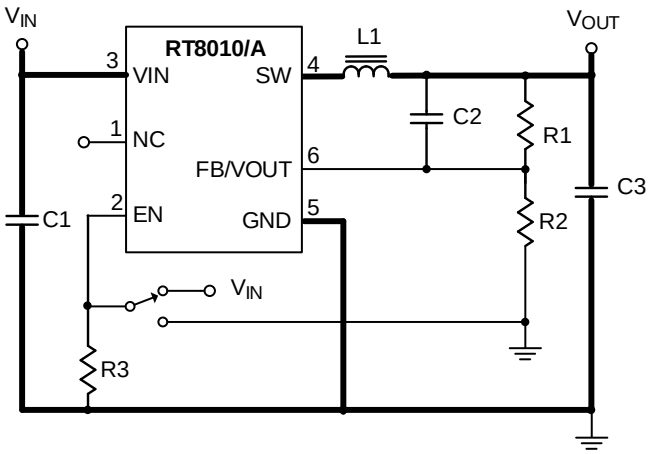


Figure 6. EVB Schematic

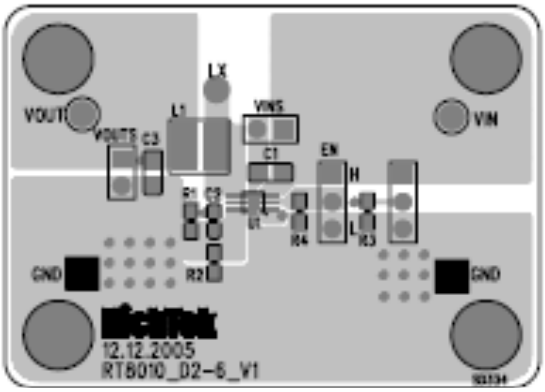


Figure 7. Top Layer

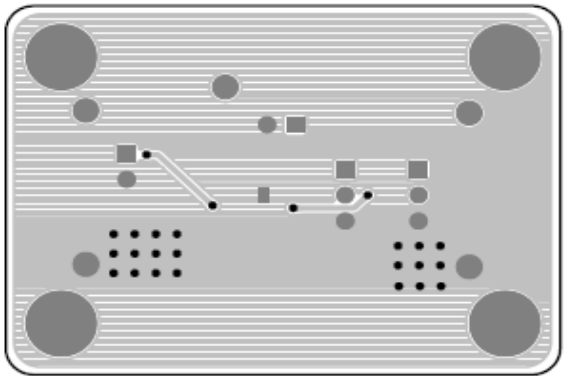


Figure 8. Bottom Layer

Table 1. Recommended Inductors

Supplier	Inductance (μH)	Current Rating (mA)	DCR (mΩ)	Dimensions (mm)	Series
TAIYO YUDEN	2.2	1480	60	3.00 x 3.00 x 1.50	NR 3015
GOTREND	2.2	1500	58	3.85 x 3.85 x 1.80	GTSD32
Sumida	2.2	1500	75	4.50 x 3.20 x 1.55	CDRH2D14
Sumida	4.7	1000	135	4.50 x 3.20 x 1.55	CDRH2D14
TAIYO YUDEN	4.7	1020	120	3.00 x 3.00 x 1.50	NR 3015
GOTREND	4.7	1100	146	3.85 x 3.85 x 1.80	GTSD32

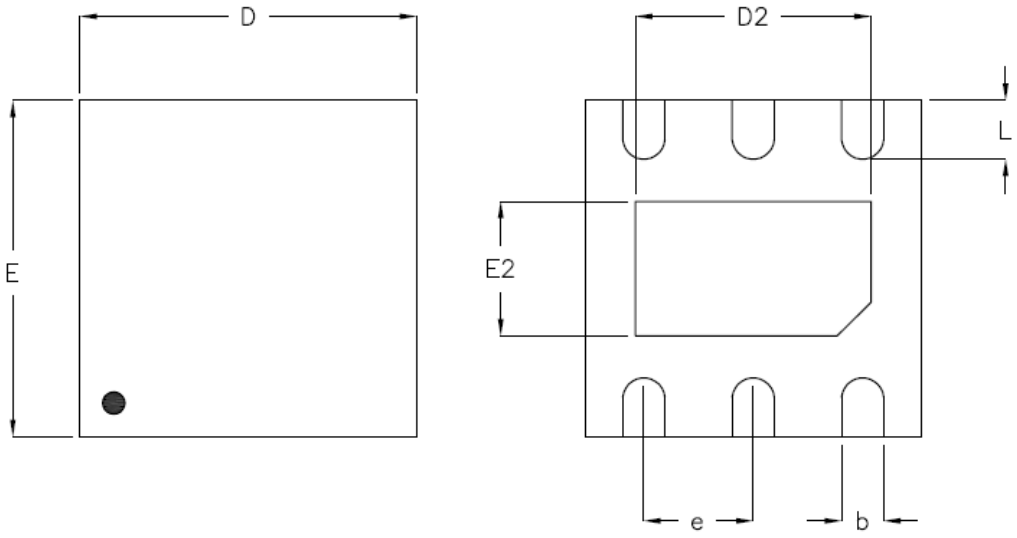
Table 2. Recommended Capacitors for C_{IN} and C_{OUT}

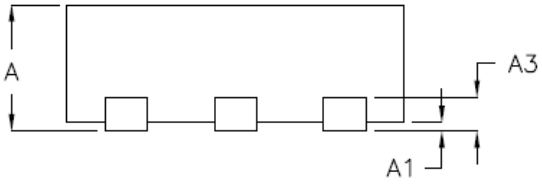
Supplier	Capacitance (μF)	Package	Part Number
TDK	4.7	0603	C1608JB0J475M
MURATA	4.7	0603	GRM188R60J475KE19
TAIYO YUDEN	4.7	0603	JMK107BJ475RA
TAIYO YUDEN	10	0603	JMK107BJ106MA
TDK	10	0805	C2012JB0J106M
MURATA	10	0805	GRM219R60J106ME19
MURATA	10	0805	GRM219R60J106KE19
TAIYO YUDEN	10	0805	JMK212BJ106RD

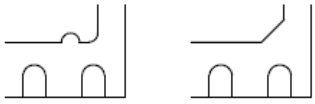
Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

16 Outline Dimension

16.1 WDFN-6L 2x2







DETAILA

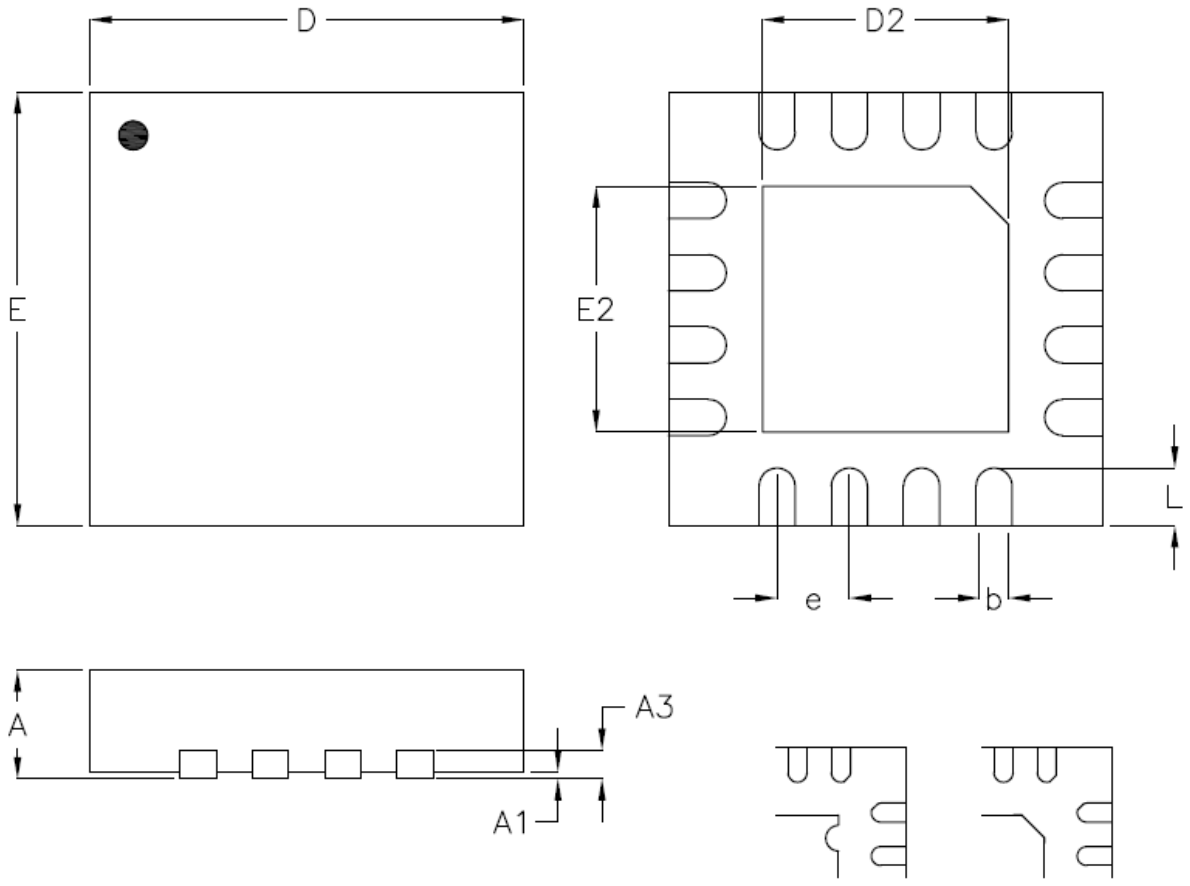
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package

16.2 WQFN-16L 3x3



DETAILA
Pin #1 ID and Tie Bar Mark Options

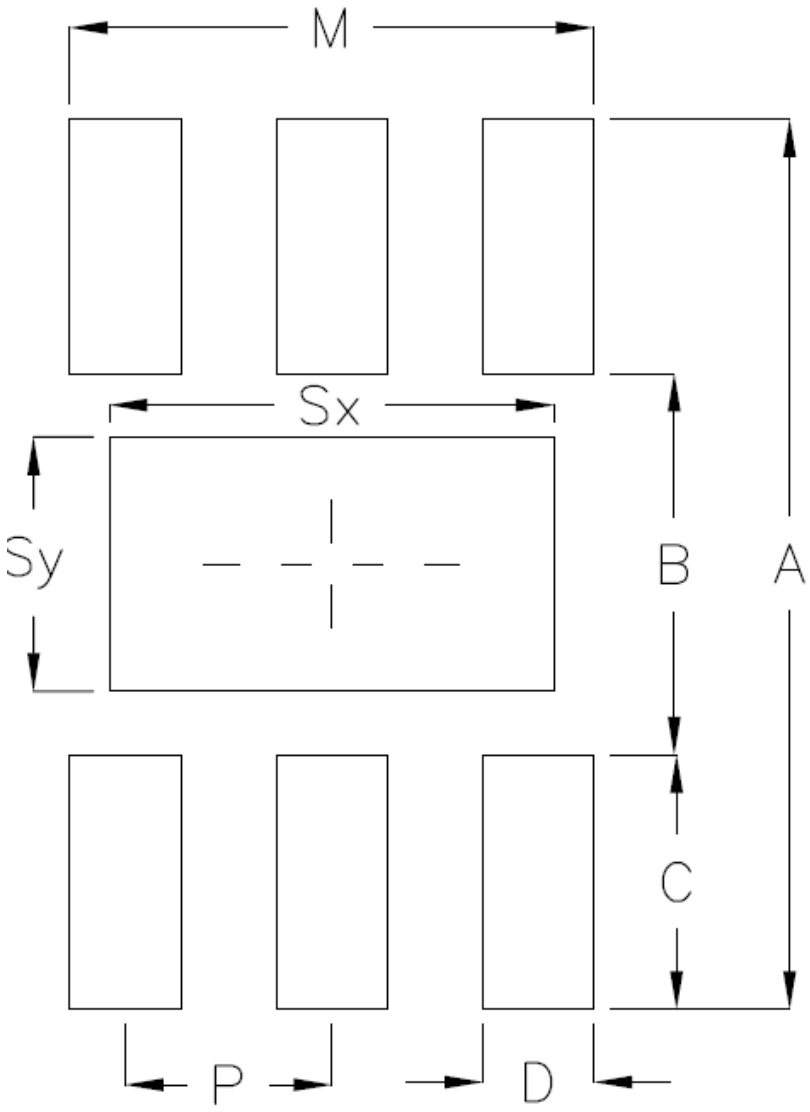
Note : The configuration of the Pin #1 Identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

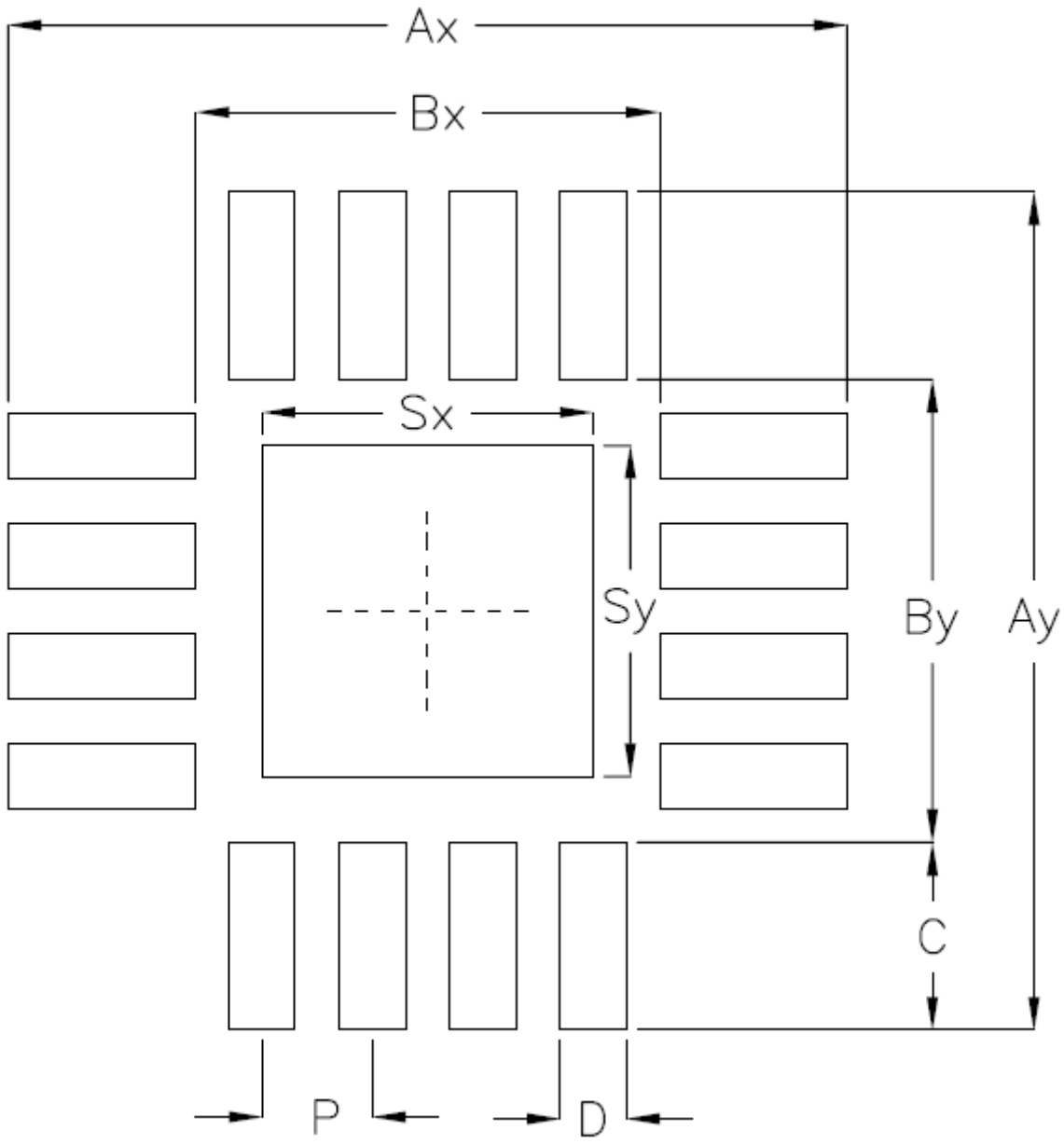
17 Footprint Information

17.1 WDFN-6L 2x2



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-6	6	0.65	2.80	1.20	0.80	0.35	1.40	0.80	1.65	±0.05

17.2 WQFN-16L 3x3



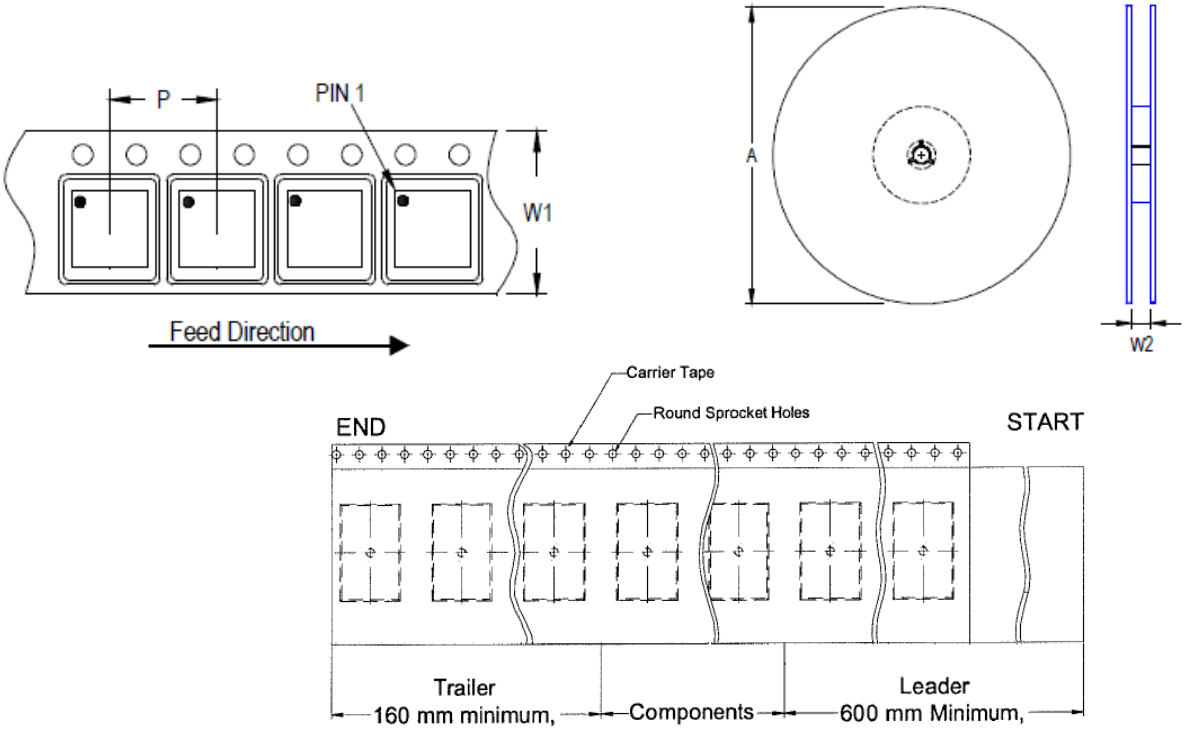
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05

18 Packing Information

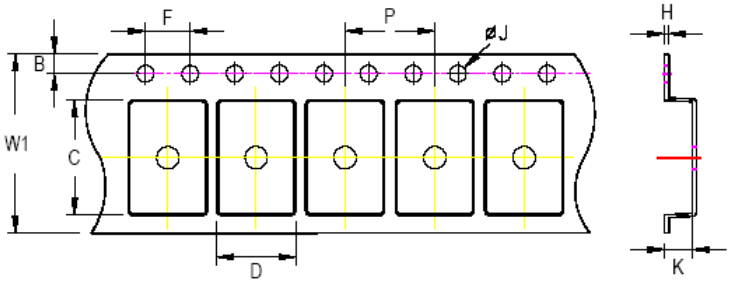
18.1 Tape and Reel Data

18.1.1 WDFN-6L 2x2

18.1.1.1 2500 Units per Reel



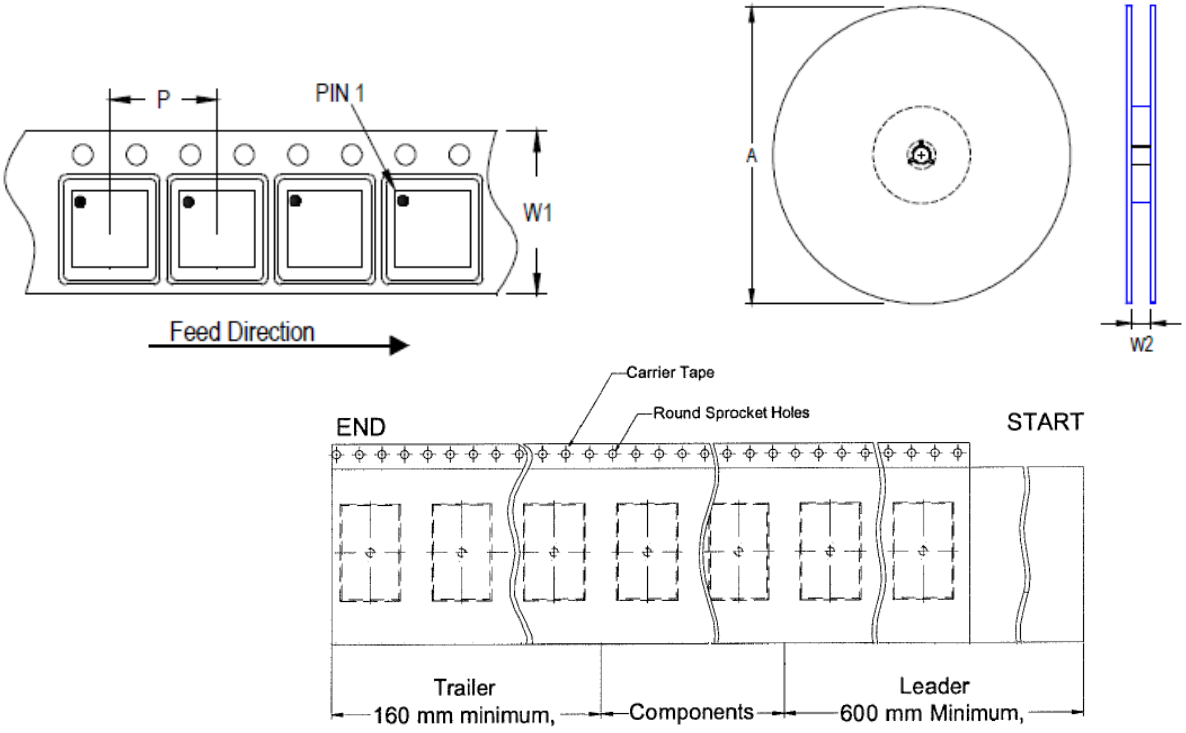
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



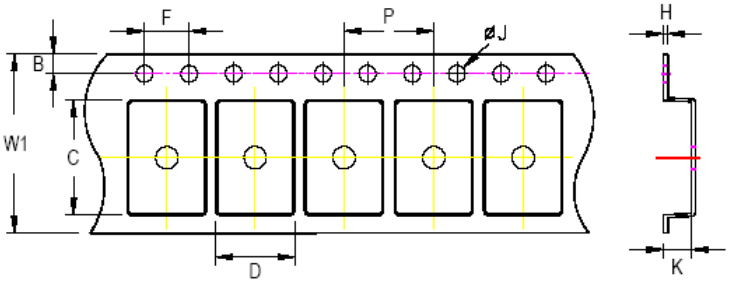
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.1.1.2 3000 Units per Reel



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 2x2	8	4	180	7	3,000	160	600	8.4/9.9

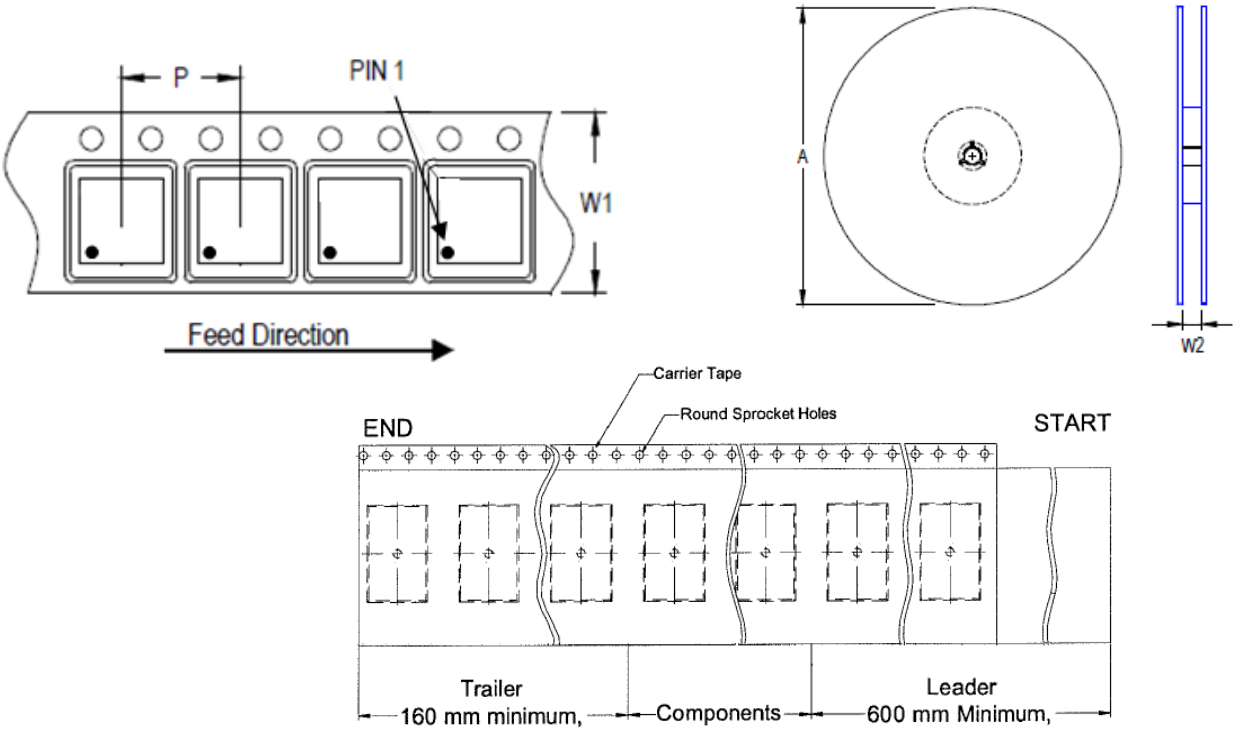


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

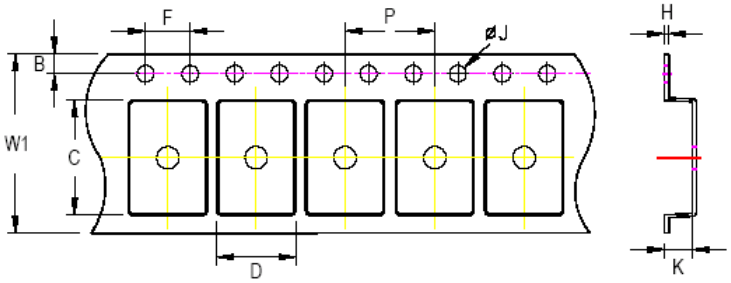
Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.1.2 WQFN-16L 3x3

18.1.2.1 1500 Units per Reel



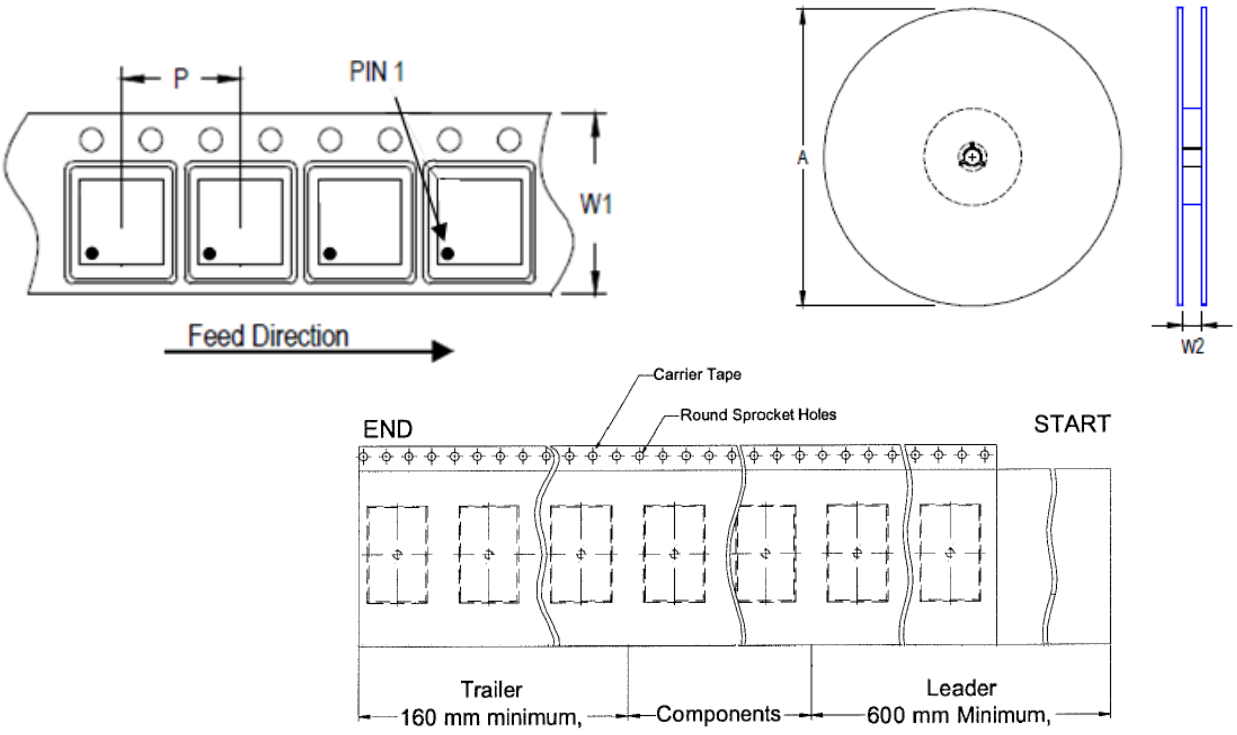
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



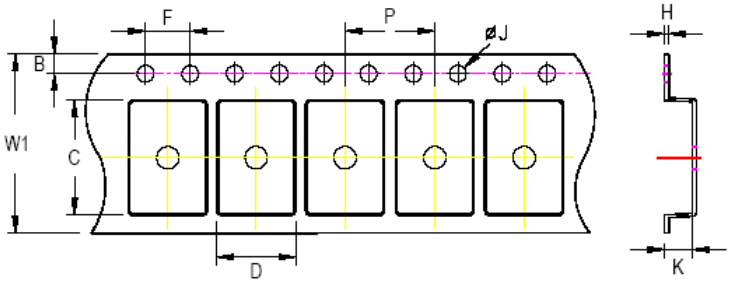
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.1.2.2 2500 Units per Reel



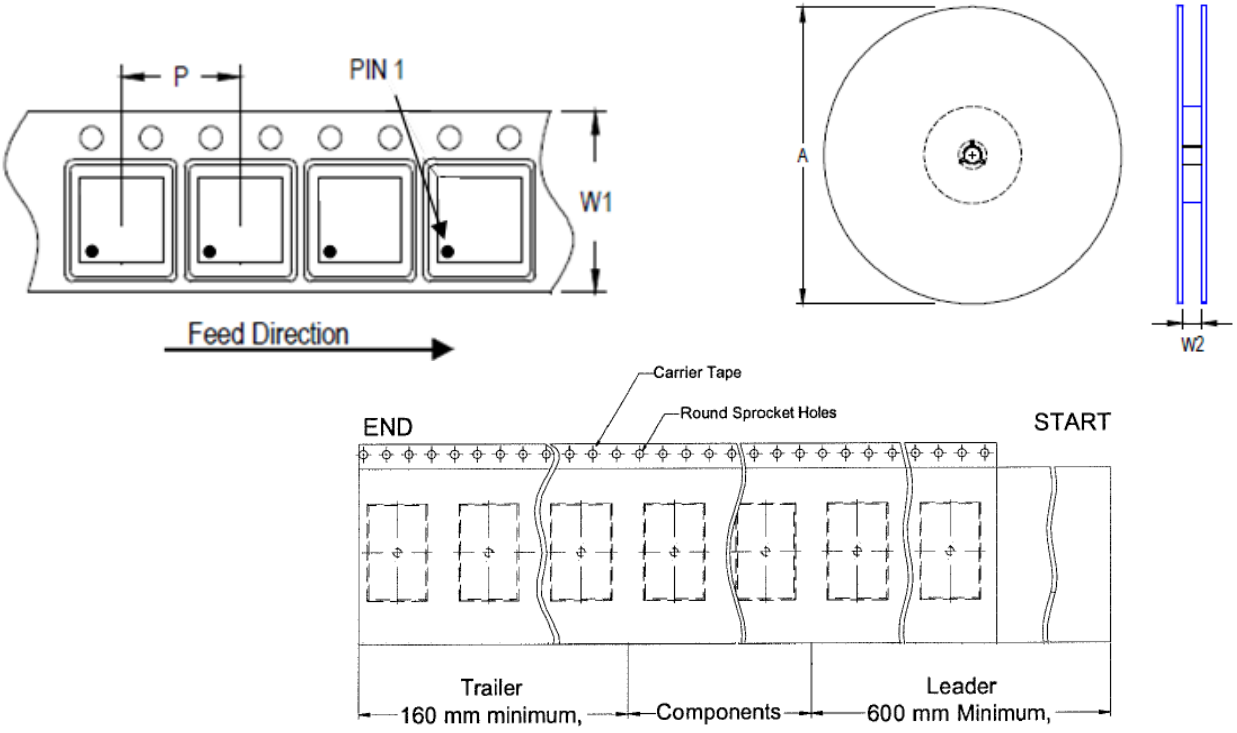
Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	8	4	180	7	2,500	160	600	8.4/9.9



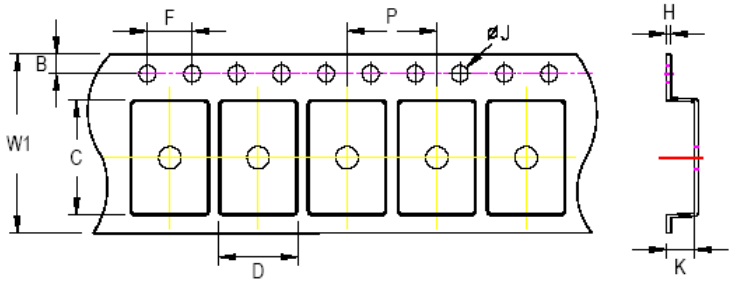
C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.1.2.3 3000 Units per Reel



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader(mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

18.2 Tape and Reel Packing

18.2.1 WDFN-6L 2x2

18.2.1.1 2500 Units per Reel

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

18.2.1.2 3000 Units per Reel

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 2x2	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

18.2.2 WQFN-16L 3x3

18.2.2.1 1500 Units per Reel

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

18.2.2.2 2500 Units per Reel

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x3	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

18.2.2.3 3000 Units per Reel

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN & DFN 3x3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

18.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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19 Datasheet Revision History

Version	Date	Description	Item
13	2024/3/21	Modify	General Description on P1 Features on P1 Ordering Information on P1 Simplified Application Circuit on P1 Pin Configuration on P4 Functional Pin Description on P4 Functional Block Diagram on P5 Absolute Maximum Ratings on P6 Electrical Characteristics on P7, P8 Typical Application Circuit on P9 Application Information on P14 to P19 Packing Information on P24 to P34