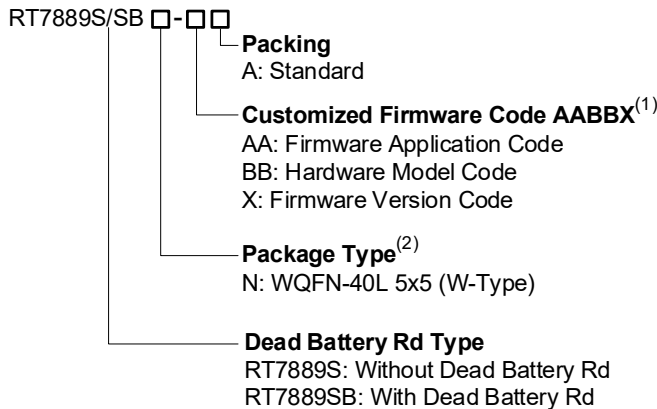


MCU Based Single Port USB Type-C EPR PD Controller

1 General Description

The RT7889S/RT7889SB is a highly integrated single port USB type-C EPR PD controller featuring a 3:1 SBU MUX, MCU, VCONN load switches, and single-port PD control circuitry. The IC incorporates an ARM Cortex-M0 MCU controller, which handles various functions of protocol communication, smart control of external DC-DC power, firmware-based protections, and customized functions. The RT7889S/RT7889SB provides robust protections for VCONN and SBU1/2. The IC is available in a compact WQFN 5x5 package. The recommended junction temperature range is -40°C to 125°C, and the ambient temperature range is -40°C to 85°C.

2 Ordering Information



Note 1.

- Marked with ⁽¹⁾ indicates that if the firmware code is empty, this field will be removed.
- Marked with ⁽²⁾ indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

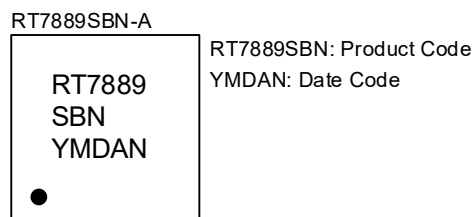
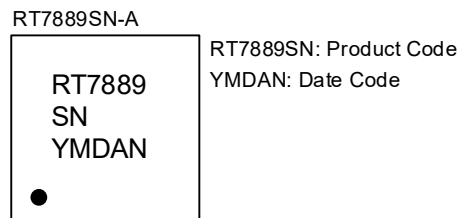
3 Applications

- Docking Stations
- Monitors
- Notebook Computers

4 Features

- **Integrated USB Type-C Power Delivery (PD) Controller**
 - Support 28V Extended Power Range (EPR) for Both Sink and Source Devices
 - Compliant with USB PD 3.2 Specification
 - Fast Role Swap
 - 2 Slave I²C Interfaces (I²C1, I²C2)
 - 2 Master/Slave I²C Interfaces (I²C3, I²C4)
- **Featured Function**
 - RT7889S: Without Dead Battery Rd
 - RT7889SB: With Dead Battery Rd
- **CC1/2 and SBU1/2 Withstand Voltage to 28V**
- **Integrated VCONN Switch for CC1/2, Supply Power up to 1.5W**
- **Port Protection for VCONN and SBU1/2**
 - Support VCONN RVP, OCP, OVP, and OTP Detection
 - Support SBU1/2 OVP Detection
- **256kB Flash Memory with Dual-Bank Operation**
- **3:1 SBU MUX with Level Shift for Alternate Mode and Debug Mode Operation**
- **Support USB Full-Speed Device**
- **Support SHA-256 and ECDSA**
- **Support Firmware Update via USB PD (CC1/2), DP/DM, and I²C Interface**
- **21 Configurable GPIOs**
- **Programmable PWM LED Controller**

5 Marking Information



6 Simplified Application Circuit

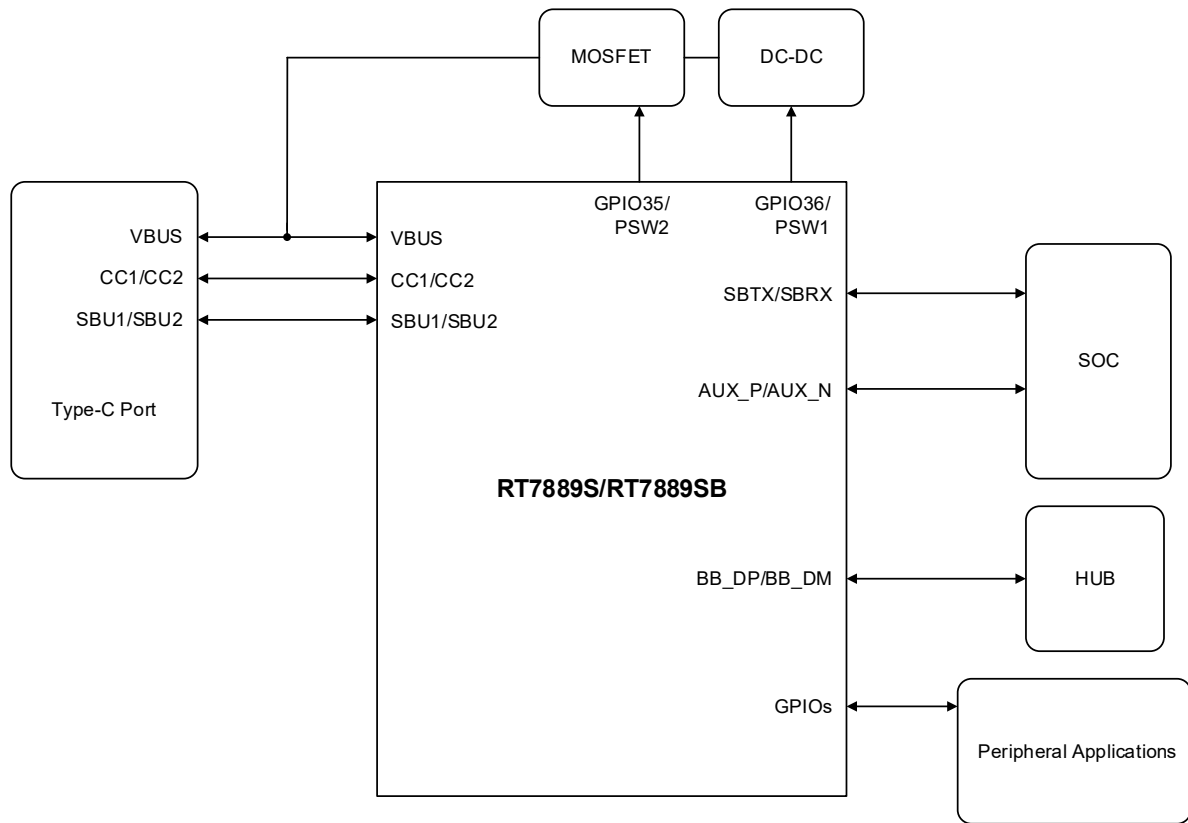
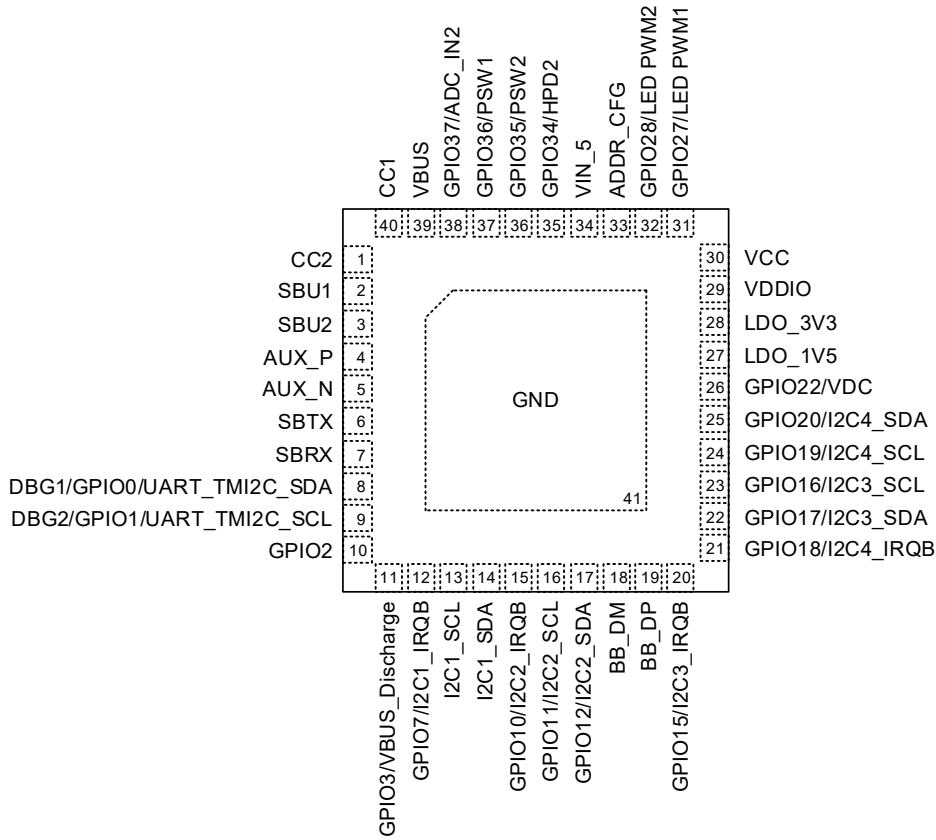


Table of Contents

1	General Description	1	14.2	Wake-Up Interrupt Controller.....	23
2	Ordering Information	1	14.3	Power-On System.....	23
3	Applications	1	14.4	USB-PD Physical Layer.....	25
4	Features	1	14.5	VCONN Switch.....	25
5	Marking Information	1	14.6	SBU MUX.....	25
6	Simplified Application Circuit	2	14.7	USB 2.0 Full-Speed PHY.....	26
7	Pin Configuration	4	14.8	11-Bit SAR ADC.....	27
8	Functional Pin Description	5	14.9	Water Detection.....	27
9	Functional Block Diagram	7	14.10	DisplayPort Hot-Plug Detect (HPD).....	27
	9.1 RT7889SB (With Dead Battery Rd).....	7	14.11	Over-Temperature Protection.....	27
	9.2 RT7889S (Without Dead Battery Rd).....	8	14.12	GPIO Application.....	28
10	Absolute Maximum Ratings	9	14.13	I ² C Interface.....	28
11	Recommended Operating Conditions	9	14.14	Thermal Considerations.....	30
12	Electrical Characteristics	10	14.15	Layout Considerations.....	31
13	Typical Application Circuit	19	15	Outline Dimension	32
	13.1 The RT7889S/RT7889SB Used in		16	Footprint Information	33
	Source or DRP Application Circuits.....	19	17	Packing Information	34
	13.2 The RT7889S/RT7889SB Used in		17.1	Tape and Reel Data.....	34
	Sink Application Circuits.....	20	17.2	Tape and Reel Packing.....	35
14	Application Information	22	17.3	Packing Material Anti-ESD Property.....	36
	14.1 CPU and Memory.....	22	18	Datasheet Revision History	37

7 Pin Configuration

(TOP VIEW)



WQFN-40L 5x5

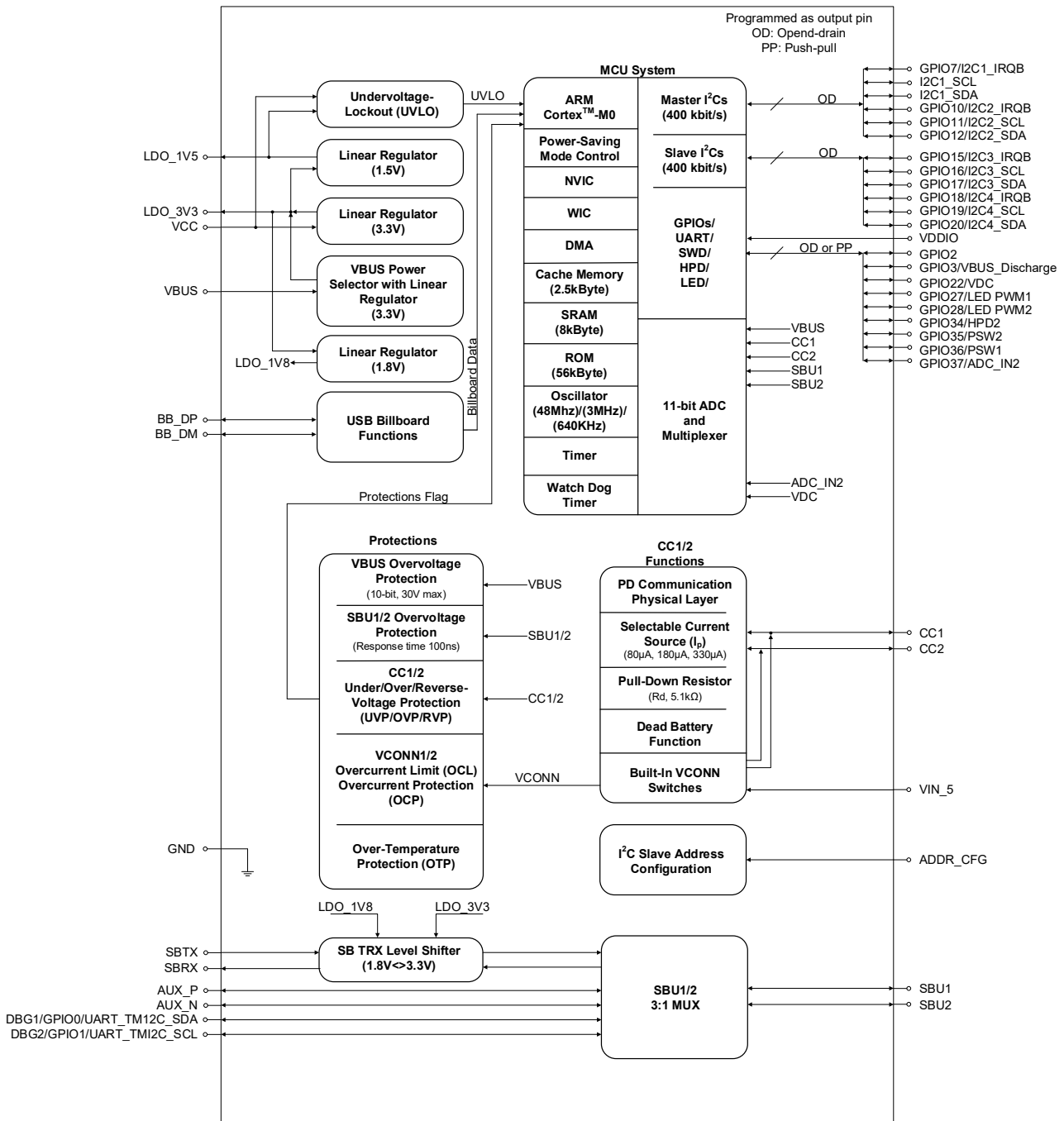
8 Functional Pin Description

Pin No.	Pin Name	Application	Pin Function
1	CC2	PD	Type-C connector configuration channel 2. Connect this pin to Type-C connector CC2 terminal.
2	SBU1	SBU	SBU1 signal for SBU mux. Connect this pin to Type-C connector SBU1 terminal.
3	SBU2	SBU	SBU2 signal for SBU mux. Connect this pin to Type-C connector SBU2 terminal.
4	AUX_P	SBU	AUX_P signal from SBU mux.
5	AUX_N	SBU	AUX_N signal from SBU mux.
6	SBTX	SBU	SBTX signal from SBU mux. Connect this pin to SBTX of AP.
7	SBRX	SBU	SBRX signal from SBU mux. Connect this pin to SBRX of AP.
8	DBG1/GPIO0/ UART_TMI2C_SDA	SBU	General-purpose input/output. SBU mux output connected to SBU1 during debug mode.
9	DBG2/GPIO1/ UART_TMI2C_SCL	SBU	General-purpose input/output. SBU mux output connected to during debug mode.
10	GPIO2	GPIO	Push-pull general-purpose input/output.
11	GPIO3/VBUS_ Discharge	GPIO	Push-pull general-purpose input/output. External VBUS discharge.
12	GPIO7/I2C1_IRQB	I ² C	Open-drain general-purpose input/output. IRQB signal of slave I ² C1 interface.
13	I2C1_SCL	I ² C	SCL signal of slave I ² C1 interface. If unused, connect to 1.8V or 3.3V with 1kΩ resistor. Support FW update.
14	I2C1_SDA	I ² C	SDA signal of slave I ² C1 interface. If unused, connect to 1.8V or 3.3V with 1kΩ resistor. Support FW update.
15	GPIO10/I2C2_IRQB	I ² C	Open-drain general-purpose input/output. IRQB signal of slave I ² C2 interface.
16	GPIO11/I2C2_SCL	I ² C	Open-drain general-purpose input/output. SCL signal of slave I ² C2 interface.
17	GPIO12/I2C2_SDA	I ² C	Open-drain general-purpose input/output. SDA signal of slave I ² C2 interface.
18	BB_DM	USB	USB 2.0 full speed PHY DM.
19	BB_DP	USB	USB 2.0 full speed PHY DP.
20	GPIO15/I2C3_IRQB	I ² C	Open-drain general-purpose input/output. IRQB signal of master/slave I ² C3 interface.
21	GPIO18/I2C4_IRQB	I ² C	Open-drain general-purpose input/output. IRQB signal of master/slave I ² C4 interface.
22	GPIO17/I2C3_SDA	I ² C	Open-drain general-purpose input/output. SDA signal of master/slave I ² C3 interface.
23	GPIO16/I2C3_SCL	I ² C	Open-drain general-purpose input/output. SCL signal of master/slave I ² C3 interface.
24	GPIO19/I2C4_SCL	I ² C	Open-drain general-purpose input/output. SCL signal of master/slave I ² C4 interface.
25	GPIO20/I2C4_SDA	I ² C	Open-drain general-purpose input/output. SDA signal of master/slave I ² C4 interface.

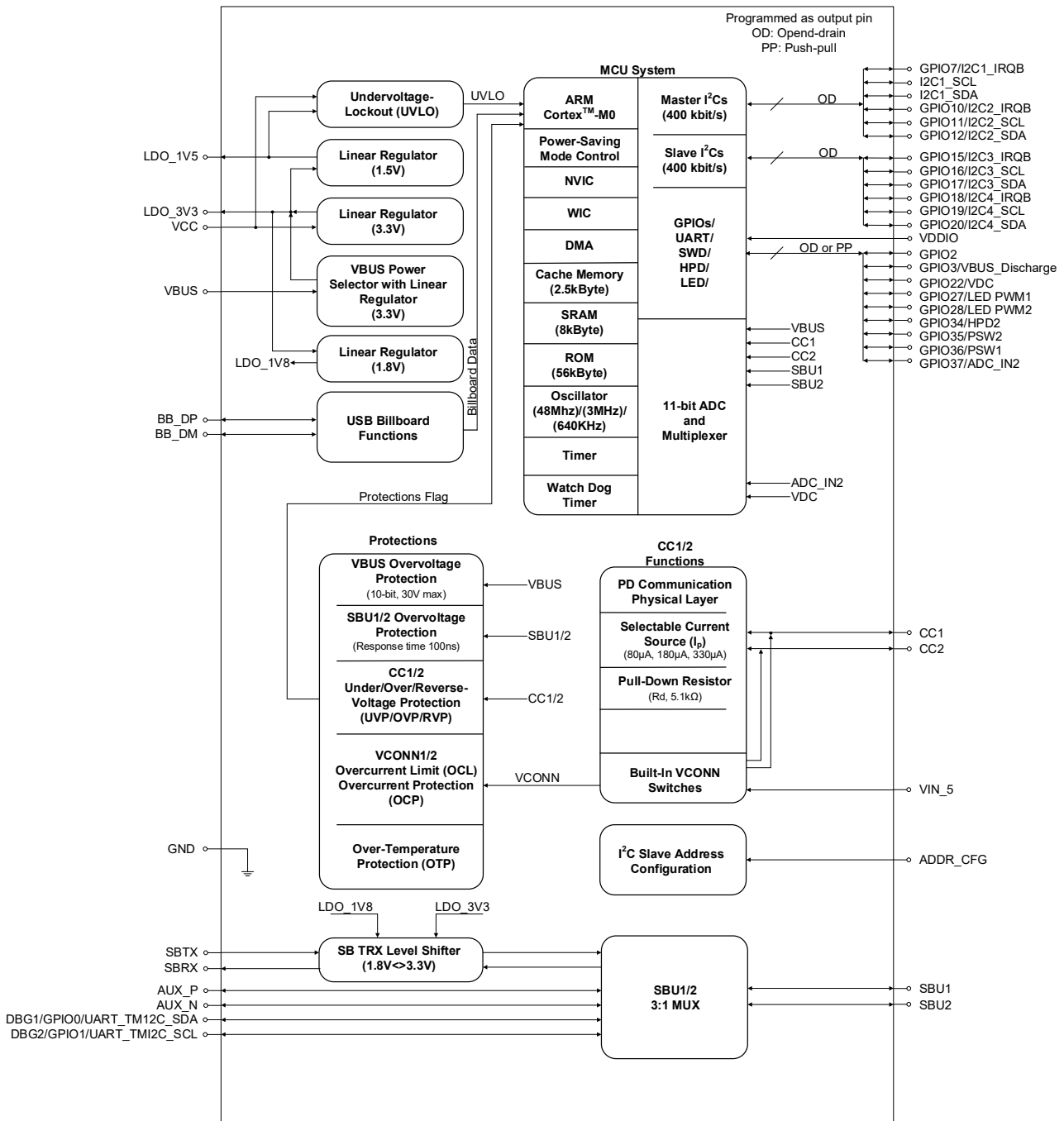
Pin No.	Pin Name	Application	Pin Function
26	GPIO22/VDC	GPIO	Push-pull general-purpose input/output. DC power input detection pin.
27	LDO_1V5	Power	1.5V LDO output. Connect 1 μ F capacitor at LDO_1V5.
28	LDO_3V3	Power	3.3V LDO output. Connect 10 μ F capacitor at LDO_3V3. The 10 μ F bypass capacitor must be placed close to the IC pins in the PCB layout.
29	VDDIO	Power	Power input for GPIO. Connect 1 μ F capacitor at VDDIO.
30	VCC	Power	Power input for chip. Place a 1 Ω series resistor and a 4.7 μ F bypass capacitor at the VCC pin. VCC must be supplied with 5V.
31	GPIO27/LED PWM1	GPIO	Push-pull general-purpose input/output. Programmable PWM LED controller.
32	GPIO28/LED PWM2	GPIO	Push-pull general-purpose input/output. Programmable PWM LED controller.
33	ADDR_CFG	GPIO	Slave address configure.
34	VIN_5	Power	Power input for VCONN. Connect 10 μ F capacitor at VIN_5.
35	GPIO34/HPD2	GPIO	Open-drain general-purpose input/output. HPD for DisplayPort application.
36	GPIO35/PSW2	PD	Push-pull general-purpose input/output. External DC-DC enable control.
37	GPIO36/PSW1	PD	Push-pull general-purpose input/output. External DC-DC enable control.
38	GPIO37/ADC_IN2	GPIO	Open-drain general-purpose input/output. ADC measurement pin (up to 6V.)
39	VBUS	PD	One of power input for the RT7889S/RT7889SB. Connect this pin to Type-C connector VBUS terminal.
40	CC1	PD	Type-C connector configuration channel 1. Connect this pin to Type-C connector CC1 terminal.
41 (Exposed Pad)	GND	Power	Analog ground. The exposed pad must be connected to GND and be well soldered to a large copper PCB for maximum power dissipation.

9 Functional Block Diagram

9.1 RT7889SB (With Dead Battery Rd)



9.2 RT7889S (Without Dead Battery Rd)



10 Absolute Maximum Ratings

(Note 2)

• VCC to GND -----	-0.3V to 6V
• LDO_3V3 to GND -----	-0.3V to 3.6V
• LDO_1V5 to GND -----	-0.3V to 1.65V
• VDDIO to GND -----	-0.3V to 6V
• VBUS to GND -----	-0.3V to 36V
• CC1, CC2 to GND -----	-0.3V to 36V
• SBU1, SBU2 to GND -----	-0.3V to 36V
• BB_DP, BB_DM to GND -----	-0.3V to LDO_3V3 + 0.5V
• VIN_5 to GND -----	-0.3V to 6V
• AUX_P, AUX_N to GND -----	-0.3V to 6V
• SBTX, SBRX to GND -----	-0.3V to LDO_3V3 + 0.5V
• DBG1/GPIO0/UART_TMI2C_SDA, DBG2/GPIO1/ UART_TMI2C_SCL to GND -----	-0.3V to 6V
• Others -----	-0.3V to 6V
• Power Dissipation, Pd @ TA = 25°C	
WQFN-40L 5x5 -----	2.8W
• Package Thermal Resistance (Note 3)	
WQFN-40L 5x5, θJA -----	35.77°C/W
WQFN-40L 5x5, θJC -----	5.22°C/W
• Lead Temperature -----	260°C
• Junction Temperature -----	150°C
• Storage Temperature Range -----	-65°C to 150°C
• ESD Susceptibility (Note 4)	
HBM (Human Body Model) -----	2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θJA is simulated under natural convection (still air) at TA = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θJC is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

• VBUS Power Supply, VBUS -----	4V to 30V
• System Power Supply, VCC -----	3.3V to 5.5V
• IO Power Supply, VDDIO -----	1.8V to 5.5V
• VCONN Power Supply, VIN_5 -----	4V to 5.5V
• CC1/CC2 -----	0V to 5.5V
• SBU1/SBU2/AUX_P/AUX_N/SBTX/SBRX/BB_DP/BB_DM -----	0V to 3.6V
• Other pins -----	0V to 5.5V
• Junction Temperature Range -----	-40°C to 125°C
• Ambient Temperature Range -----	-40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Consumption						
VCC Power-On, Shutdown Current	I _{VCC_SHDN}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	43	61	79	μA
VCC Power-On, Port in Low Power Mode	I _{VCC_UATTACH_DRP_Toggle_RP_LP}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	53	76	100	μA
VCC Power-On, Port is Sink in Idle Mode	I _{VCC_ATTACH_IDE}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	99	141	184	μA
VCC Power-On, Port is Sink in Idle Mode. VCONN Output Voltage and All Vconn Function Enabled	I _{VCC_ATTACH_VCONN_ON_IDE}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	133	190	247	μA
VCC Power-On, Port is Sink in Normal Mode	I _{VCC_ATTACH_NOR}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	1380	1971	2563	μA
VCC Power-On, Port us Sink in Normal Mode. Billboard Enabled	I _{VCC_ATTACH_BILLBOARD_ON_NOR}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	2020	2880	3750	μA
VCC Power-On, Port is Sink in Normal Mode. VCONN Output Voltage and All Vconn Function Enabled	I _{VCC_ATTACH_VCONN_ON_NOR}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	1455	2078	2701	μA
VCC Power-On, Port is Sink in Normal Mode. VCONN Output Voltage and All Vconn Function Enabled. CC Enable TX for Communication	I _{VCC_ATTACH_VCONN&TX_ON_NOR}	VCC = 3.3V, VBUS = 0V, measure the input current of VCC	3285	4693	6101	μA
VBUS Power Selector						
VBUS Power-Good High Voltage Threshold	V _{VBUS_PG}		3.4	3.55	3.7	V
VBUS Power-Good High Voltage Hysteresis	V _{VBUS_PG_HYS}		0.1	0.2	0.3	V
VCC Power-Good High Voltage Threshold	V _{VCC_PG}		3	3.1	3.2	V
VCC Power-Good High Voltage Hysteresis	V _{VCC_PG_HYS}		0.28	0.33	0.38	V
VBUS LDO Output Voltage	V _{VBUS_LDO_OUT}	VBUS = 4.6V, I _{lead} = 30mA	3.06	3.4	3.74	V
VBUS LDO Output Current Limit	I _{VBUS_LDO_LIM}		40	--	65	mA
VCC LDO Output Voltage	V _{VCC_LDO_OUT}		2.97	3.3	3.63	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO1V5 Output Voltage	V1V5_LDO_OUT		1.5	1.575	1.65	V
Type-C Port Control and CC Detection						
DFP 80 μ A CC Current	IRp80 μ _NOR	VCC = 3.3 to 5.5V	64	80	96	μ A
DFP 180 μ A CC Current	IRp180 μ _NOR	VCC = 3.3 to 5.5V	166	180	194	μ A
DFP 330 μ A CC Current	IRp330 μ _NOR	VCC = 3.3 to 5.5V	304	330	356	μ A
UFP Ra	Ra	VCC = 3.3 to 5.5V	0.8	1	1.2	k Ω
UFP Rd	Rd	VCC = 3.3 to 5.5V	4.59	5.1	5.61	k Ω
UFP Pull-Down Voltage in Dead Battery under DFP 80 μ A	V80 μ A_DB	VCC = 0V, apply a current source of 80 μ A (RT7889SB)	0.25	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 180 μ A	V180 μ A_DB	VCC = 0V, apply a current source of 180 μ A (RT7889SB)	0.45	--	1.5	V
UFP Pull-Down Voltage in Dead Battery under DFP 330 μ A	V330 μ A_DB	VCC = 0V, apply a current source of 330 μ A (RT7889SB)	0.85	--	2.45	V
CC Fast Role Swap Tx	RFRSSwapTx		0	--	5	Ω
PD CC TRX Communication						
Bit Rate	fBitRate_PD	VCC = 3.3 to 5.5V	270	300	330	Kbps
Maximum Difference between the Bit-Rate during the Part of the Packet following the Preamble and the Reference Bit-Rate	pBitRate	VCC = 3.3 to 5.5V	--	--	0.25	%
Fall Time	tFall	VCC = 3.3 to 5.5V	300	--	--	ns
Rise Time	tRise	VCC = 3.3 to 5.5V	300	--	--	ns
Voltage Swing	VSwing	VCC = 3.3 to 5.5V	1.05	1.125	1.2	V
Transmitter Output Impedance	ZDriver	VCC = 3.3 to 5.5V	33	50	75	Ω
Receiver Input Impedance	ZBmcRx	VCC = 3.3 to 5.5V	1	--	--	M Ω
VCONN Switch						
VCONN OVP	VVCONN_OVP		5.6	5.75	5.9	V
Hysteresis on VCONN OVP	VVCONN_OVP_HYS		50	75	100	mV
OVP Response Time on the CC Pins. Time from OVP Asserted until OVP FETs Turn Off	tVCONN_OVP_Response		--	100	--	ns
VCONN Present	VVCONN_Present	VCC = 3.3 to 5.5V	2.28	2.4	2.52	V
VCONN Invalid	VVCONN_Invalid	VCC = 3.3 to 5.5V	2.565	2.7	2.835	V
VCONN Safe0V	VVCONN_Safe0v	VCC = 3.3 to 5.5V	--	0.4	0.8	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Hysteresis of VCONN Present	VVCONN_Present_HYS	VCC = 3.3 to 5.5V	50	100	150	mV
Hysteresis of VCONN Invalid	VVCONN_Invalid_HYS	VCC = 3.3 to 5.5V	50	100	150	mV
Hysteresis of VCONN Safe0v	VVCONN_Safe0v_HYS	VCC = 3.3 to 5.5V	50	100	150	mV
VCONN RVP	VVCONN_RVP		0.115	0.3	0.5	V
Release of VCONN RVP	VVCONN_RVP_HYS		0	50	115	mV
RVP response time on the CC Pins. Time from OVP Asserted until OVP FETs Turn Off	tVCONN_RVP_Response		--	300	--	ns
VCONN OCP Range (Shutdown)	IVCONN_OCP_1		180	200	220	mA
VCONN OCP Range (Shutdown)	IVCONN_OCP_2		270	300	330	mA
VCONN OCP Range (Shutdown)	IVCONN_OCP_3		360	400	440	mA
VCONN OCP Range (Shutdown)	IVCONN_OCP_4		450	500	550	mA
VCONN OCP Range (Shutdown)	IVCONN_OCP_5		540	600	660	mA
VCONN OCP Range (Shutdown)	IVCONN_OCP_6		630	700	770	mA
VCONN OCL Range (Limit)	IVCONN_OCL_1		140	200	260	mA
VCONN OCL Range (Limit)	IVCONN_OCL_2		240	300	360	mA
VCONN OCL Range (Limit)	IVCONN_OCL_3		320	400	480	mA
VCONN OCL Range (Limit)	IVCONN_OCL_4		400	500	600	mA
VCONN OCL Range (Limit)	IVCONN_OCL_5		480	600	720	mA
VCONN OCL Range (Limit)	IVCONN_OCL_6		560	700	840	mA
Ron for VCONN Switch	RON_VCONN	VIN_5 = 5V, VCC = 3.3 to 5.5V CC1/CC2 sink a 600mA loading	--	1	1.3	Ω
Power-Off Leakage Current of VCONN	IOFF_VCONN_5.5V	VIN_5 = 5.5V, VCC = 3.3V	-1	--	1	μA
Off Leakage Current of VCONN	IOZ_VCONN_5.5V	VIN_5 = 5.5V, VCC = 0V	-1	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Detection						
VREF_VBUS_FRS	VVBUS_FRS_0		4.512	4.8	5.088	V
	VVBUS_FRS_1		4.5872	4.88	5.1728	V
	VVBUS_FRS_2		4.7376	5.04	5.3424	V
	VVBUS_FRS_3		4.8128	5.12	5.4272	V
	VVBUS_FRS_4		4.888	5.2	5.512	V
	VVBUS_FRS_5		4.9632	5.28	5.5968	V
	VVBUS_FRS_6		5.1136	5.44	5.7664	V
	VVBUS_FRS_7		5.1888	5.52	5.8512	v
VREF_VBUS_FRS HYS	VVBUS_FRS_HYS		0.3	0.43	0.56	V
VBUS Force Discharge	RVBUS_FDIS		0.28	0.4	0.52	kΩ
VBUS Bleed Discharge	RVBUS_BDIS		2.8	4	5.2	kΩ
SBU OVP Switch Mux						
On Leakage Current of SBU Switch	I _{ON_SBU_CON_AUX_3.6V}	VCC = 3.3 to 5.5V, SBUX = 3.6 V, AUXP/AUXN/DBG1/DBG2 is floating	-3.6	--	3.6	μA
On Leakage Current of SBU Switch	I _{ON_SBU_CON_SBTRX_3.3V}	VCC = 3.3 to 5.5V, SBUX = 3.3 V, SBTX/SBRX is floating and at level shifter = 3.3V setting	-3.3	--	3.3	μA
Off Leakage Current of SBU Connector Side	I _{OZ_SBU_CON_3.6V}	VCC = 3.3 to 5.5V, SBUX = 3.6 V	-3.6	--	3.6	μA
Off Leakage Current of SBU Connector Side	I _{OZ_SBU_CON_28V}	VCC = 3.3 to 5.5V, SBUX = 28V	--	--	150	μA
Power-Off Leakage Current SBU Connector Side	I _{OFF_SBU_CON_3.6V}	VCC = 0V, SBUX = 3.6V	-3	--	3	μA
On Leakage Current of SBU Host Side	I _{ON_SBU_HOST_3.6V}	VCC = 3.3 to 5.5V, SBUX = floating, AUXP/AUXN/DBG1/DBG2 is 3.6V	-3	--	3	μA
Off Leakage of SBU Host Side	I _{OZ_SBU_HOST_3.6V}	VCC = 3.3 to 5.5V, SBUX = floating, AUXP/AUXN/DBG1/DBG2 is 3.6V	-3	--	3	μA
Power-Off Leakage Current of SBU Host Side	I _{OFF_SBU_HOST_3.6V}	VCC = 0V, SBUX = floating, AUXP/AUXN/DBG1/DBG2 is 3.6V	-1	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Off Leakage Current of SBU_CON to SBU Host Side	I _{OFF_SBU_CON_28V to SBU_HOST}	VCC = 3.3 to 5.5V, SBUX = 28V, AUXP/AUXN/DBG1/DBG2 are set to 0V, measure leakage out of AUXP/AUXN/DBG1/DBG2 pins	-1	--	1	μA
SBU Input OVP Lockout	V _{SBU_OVP}		4.25	4.5	4.75	V
SBU Input OVP Hysteresis	V _{SBU_OVP_HYS}		35	60	85	mV
SBU Pins OVP Response Time	t _{SBU_OVP}		30	60	120	ns
SBUx to AUXP/N Switch On-Resistance	R _{ON_SBU_AUX}	V _{sw} = 0V to 3.6V, I _{sw} = 10mA	--	3.5	6	Ω
SBUx to AUXP/N Switch On-Resistance Flatness	R _{ON_SBU_FLAT}		--	--	500	mΩ
SBUx to DBGx Switch On-Resistance	R _{ON_SBU_DEBUG}	V _{sw} = 0V to 3.6V, I _{sw} = 10mA	--	8	16	Ω
SBU MUX Switch Turn-On Time	t _{SBU_ON}	SBUX = 2.5 V, R _L = 1kΩ	150	250	400	μs
SBU MUX Switch Turn-Off Time	t _{SBU_OFF}	SBUX = 2.5 V, R _L = 1kΩ	0	--	1	μs
AUX Channel -3dB Bandwidth	BW_SBU		175	--	--	MHz
Crosstalk for SBU	X _{talk_SBU}		--	-40	--	dB
Off Isolation for SBU	OIRR_SBU		--	-40	--	dB
Pull-Down Resistance of 100kΩ on AUXP	R _{AUXP_PD100k}		60	80	100	kΩ
Pull-Up Resistance of 100kΩ on AUXN	R _{AUXN_PU100k}		60	80	100	kΩ
Pull-Up Resistance of 1MΩ on AUXP	R _{AUXP_PU1M}		0.9	1.1	1.3	MΩ
Pull-Down Resistance of 1MΩ on AUXN	R _{AUXN_PD1M}		0.9	1.1	1.3	MΩ
Pull-Down Resistance of 0.47MΩ on AUXP	R _{AUXP_PD0.47M}		0.25	0.47	0.75	MΩ
Pull-Down Resistance of 4.7MΩ on AUXN	R _{AUXN_PD4.7M}		2.5	4.7	7.5	MΩ
SBTX Level Shifter Output High Voltage	V _{SBTX_OH}		2.4	--	3.47	V
SBTX Level Shifter Output Low Voltage	V _{SBTX_OL}		-0.05	--	0.4	V
SBTX Level Shifter Output Impedance	R _{SBTX_OUT}		25	--	90	Ω
SBTX Output Pull-Up Resistor	R _{SBTX_PU}		7	8.75	10.5	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SBTX Level Shifter Input High Voltage for 1.8V Mode	V _{SBTX_IH_1.8V}		1.26	--	1.98	V
SBTX Level Shifter Input Low Voltage for 1.8V Mode	V _{SBTX_IL_1.8V}		-0.3	--	0.54	V
SBTX Level Shifter Input High Voltage for 3.3V Mode	V _{SBTX_IH_3.3V}		2.31	--	3.6	V
SBTX Level Shifter Input Low Voltage for 3.3V Mode	V _{SBTX_IL_3.3V}		-0.3	--	0.99	V
SBTX Level Shifter Input High Leakage	I _{SBTX_LK_INH}	VDD3V3 = 3.3V, SBTX = 3.3V	-1	--	1	μA
SBTX Level Shifter Input Low Leakage	I _{SBTX_LK_INL}	VDD3V3 = 3.3V, SBTX = 0V	-1	--	1	μA
SBTX Input Pull-Up Resistor	R _{SBTX_PD}		7	8.75	10.5	kΩ
SBRX Level Shifter Output Impedance	R _{SBRX_OUT}		25	--	90	Ω
SBRX Level Shifter Output High Voltage for 1.8V Mode	V _{SBRX_OH_1.8V}	I _{OH} = 2mA at 1.8V VDD with output impedance of RX	1.44	--	3.6	V
SBRX Level Shifter Output Low Voltage for 1.8V Mode	V _{SBRX_OL_1.8V}	I _{OL} = 2mA at 1.8V VDD with output impedance of RX	-0.3	--	0.36	V
SBRX Level Shifter Output High Voltage for 3.3V Mode	V _{SBRX_OH_3.3V}	I _{OH} = 3mA at 3.3V VDD with output impedance of RX	2.64	--	3.6	V
SBRX Level Shifter Output Low Voltage for 3.3V Mode	V _{SBRX_OL_3.3V}	I _{OL} = 3mA at 3.3V VDD with output impedance of RX	-0.3	--	0.66	V
SBRX Level Shifter Input High Voltage	V _{SBRX_IH}		2	--	3.72	V
SBRX Level Shifter Input Low Voltage	V _{SBRX_IL}		-0.3	--	0.65	V
SBRX Level Shifter Input High Leakage	I _{SBRX_LK_INH}	VDD3V3=3.3V, SBU_CON = 3.3V	-3.3	--	3.3	μA
SBRX Level Shifter Input Low Leakage	I _{SBRX_LK_INL}	VDD3V3 = 3.3V, SBU_CON = 0V	-1	--	1	μA
SBRX Input Pull-Down Resistor	R _{SBRX_PD}		0.7	0.875	1.05	MΩ
ADC						
ADC Resolution	RES_ADC	VCC = 3.3 to 5.5V	--	11	--	bit
VBUS Measurement Range	V _{VBUS_ADC_RANGE}	VCC = 3.3 to 5.5V	0	--	34	V

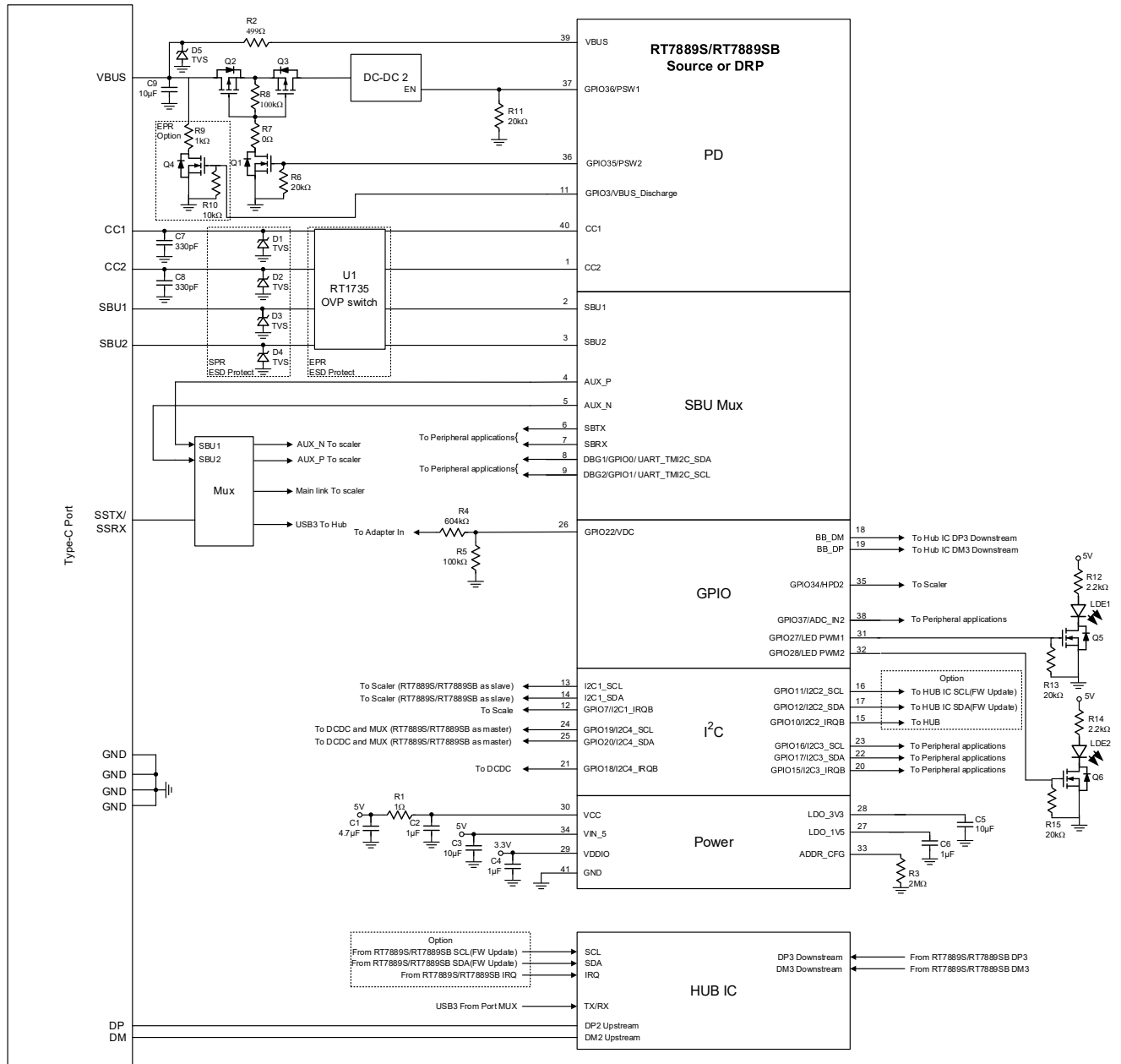
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS Resolution	VVBUS_ADC_RES	VCC = 3.3 to 5.5V	--	17.2	--	mV
VBUS Accuracy	VVBUS_ADC_ACC	VCC = 3.3 to 5.5V	-175	--	175	mV
CCx Measurement Range	VCCx_ADC_RANGE	VCC = 3.3 to 5.5V	0	--	6	V
CCx Resolution	VCCx_ADC_RES	VCC = 3.3 to 5.5V	--	4	--	mV
CCx Accuracy	VCCx_ADC_ACC	VCC = 3.3 to 5.5V	-40	--	40	mV
SBUx Measurement Range	VSBUx_ADC_RANGE	VCC = 3.3 to 5.5V	0	--	6	V
SBUx Resolution	VSBUx_ADC_RES	VCC = 3.3 to 5.5V	--	4	--	mV
SBUx Accuracy	VSBUx_ADC_ACC	VCC = 3.3 to 5.5V	-40	--	40	mV
VDC Measurement Range	VSBUx_ADC_RANGE	VCC = 3.3 to 5.5V	0	--	6	V
VDC Resolution	VSBUx_ADC_RES	VCC = 3.3 to 5.5V	--	4	--	mV
VDC Accuracy	VSBUx_ADC_ACC	VCC = 3.3 to 5.5V	-40	--	40	mV
ADC_IN Measurement Range	VADCx_ADC_RANGE	VCC = 3.3 to 5.5V	0	--	6	V
ADC_IN Resolution	VADCx_ADC_RES	VCC = 3.3 to 5.5V	--	4	--	mV
ADC_IN Accuracy	VADCx_ADC_ACC	VCC = 3.3 to 5.5V	-40	--	40	mV
ADDR						
ADDR Threshold Address = 00 Resistor	RADDR1	VCC = 3.3 to 5.5V	--	--	110	kΩ
ADDR Threshold Address = 01 Resistor	RADDR2	VCC = 3.3 to 5.5V	180	--	320	kΩ
ADDR Threshold Address = 10 Resistor	RADDR3	VCC = 3.3 to 5.5V	460	--	1020	kΩ
ADDR Threshold Address = 11 Resistor	RADDR4	VCC = 3.3 to 5.5V	1420	--	--	kΩ
IRQB						
Output Low Threshold	VIRQB_OL	IOL = 4mA at VCC = 3.5V to 5.5V	--	--	0.4	V
Input Voltage High Level	VIRQB_IH	VCC = 3.3V to 5.5V	1.26	--	--	V
Input Voltage Low Level	VIRQB_IL	VCC = 3.3V to 5.5V	--	--	0.54	V
Input Leakage Current	IIRQB_LK	VIO = 0 to 0.4V, 1 to 5.5V	-1	--	1	μA
GPIO						
Input Voltage High Level	VGPIO_IH	VCC = 3.3V to 5.5V	1.26	--	--	V
Input Voltage Low Level	VGPIO_IL	VCC = 3.3V to 5.5V	--	--	0.54	V
Output Voltage High Level	VGPIO_OH	I _{OH} = -2mA at VCC = 3.3V to 5.5V	VDDIO - 0.4	--	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Low Level	VGPIO_OL	I _{OL} = 4mA at VCC = 3.3V to 5.5V	--	--	0.4	V
Input Pull-Up Resistor	RGPIO_PU		50	80	120	kΩ
Input Pull-Low Resistor	RGPIO_PD		50	80	120	kΩ
Input Leakage Current	IGPIO_LK	V _{IO} = 0 to 0.4V, 1 to 5.5V	-1	--	1	μA
HPD						
Output Voltage Low Level	VHPD_OL	I _{OL} = 4mA at VCC = 3.3V to 5.5V	--	--	0.4	V
Hot Plug Detect Threshold	VHPD_R		2	--	--	V
Hot Unplug Detect Threshold	VHPD_F		--	--	0.8	V
HPD Pull-Up to LDO_3V3 Resistor	RHPD_PU		--	10	20	kΩ
HPD Pull-Low to GND Resistor	RHPD_PD		100	150	200	kΩ
Input Leakage Current	IHPD_LK	VCC = 3.3 to 5.5V, V _{IO} = 0 to 5.5V	-1	--	1	μA
I²C						
I ² C Pull-High			1.8	--	5.5	V
Low-Level Input Voltage	V _{IL_I2C}	VCC = 3.3 to 5.5V	--	--	0.54	V
High-Level Input Voltage	V _{IH_I2C}	VCC = 3.3 to 5.5V	1.26	--	--	V
Low-Level Output Voltage	V _{OL_I2C}	I _{OL} = 4mA at VCC = 2.5V to 5.5V	--	--	0.4	V
Input Current Each IO Pin	I _{IL_I2C}	V _{IO} = 0 to 0.4V, 1 to 5.5V	-10	--	10	μA
SCL Clock Frequency	f _{SCL}	VCC = 3.3 to 5.5V CB ≤ 100pF	400	--	1000	kHz
Rise Time of both SDA and SCL Signals	t _R	VCC = 3.3 to 5.5V CB ≤ 100pF	--	--	120	ns
Fall Time of Both SDA and SCL Signals	t _F	VCC = 3.3 to 5.5V CB ≤ 100pF	4	--	120	ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter (400k)	t _{SP}	VCC = 3.3 to 5.5V	--	--	50	ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter (1M)	t _{SP}	VCC = 3.3 to 5.5V	--	--	15	ns
Data Hold Time	t _{HD;DAT}	VCC = 3.3 to 5.5V	30	--	--	ns
Data Setup Time	t _{SU;DAT}	VCC = 3.3 to 5.5V	50	--	--	ns
VDC						
VDC 2V Low Voltage Detection Threshold	V _{VDC_2V}	VCC = 3.3 to 5.5V	1.8	2	2.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDC 2V Low Voltage Detection Threshold Hysteresis	VVDC_HYS_2V	VCC = 3.3 to 5.5V	--	40	--	mV
VDC 1.5V Low Voltage Detection Threshold	VVDC_1.5V	VCC = 3.3 to 5.5V	1.35	1.5	1.65	V
VDC 1.5V Low Voltage Detection Threshold Hysteresis	VVDC_HYS_1.5V	VCC = 3.3 to 5.5V	--	40	--	mV
VDC 0.9V Low Voltage Detection Threshold	VVDC_0.9V	VCC = 3.3 to 5.5V	0.81	0.9	0.99	V
VDC 0.9V Low Voltage Detection Threshold Hysteresis	VVDC_HYS_0.9V	VCC = 3.3 to 5.5V	--	40	--	mV
VDC 0.52V Low Voltage Detection Threshold	VVDC_0.52V	VCC = 3.3 to 5.5V	0.468	0.52	0.572	V
VDC 0.52V Low Voltage Detection Threshold Hysteresis	VVDC_HYS_0.52V	VCC = 3.3 to 5.5V	--	40	--	mV
Over-Temperature Protection						
Over-Temperature Protection Shutdown Threshold Rising	TOTP_150	VCC = 3.3 to 5.5V	140	150	160	°C
Over-Temperature Protection Shutdown Threshold Falling	TOTP_150_F	VCC = 3.3 to 5.5V	95	110	125	°C
Over-Temperature Protection Shutdown Threshold Rising	TOTP_120	VCC = 3.3 to 5.5V	110	120	130	°C
Over-Temperature Protection Shutdown Threshold Falling	TOTP_120_F	VCC = 3.3 to 5.5V	80	90	100	°C
BASE						
OSC48M Output Frequency	fOSC48M	VCC = 3.3 to 5.5V	47.04	48	48.96	MHz
OSC48M Output RMS Jitter	fOSC48M_Jitter	VCC = 3.3 to 5.5V	--	145	--	ps
OSC48M Output Start-Up Time	fOSC48M_Jitter	VCC = 3.3 to 5.5V	--	--	7	μs

13 Typical Application Circuit

13.1 The RT7889S/RT7889SB Used in Source or DRP Application Circuits



13.2 The RT7889S/RT7889SB Used in Sink Application Circuits

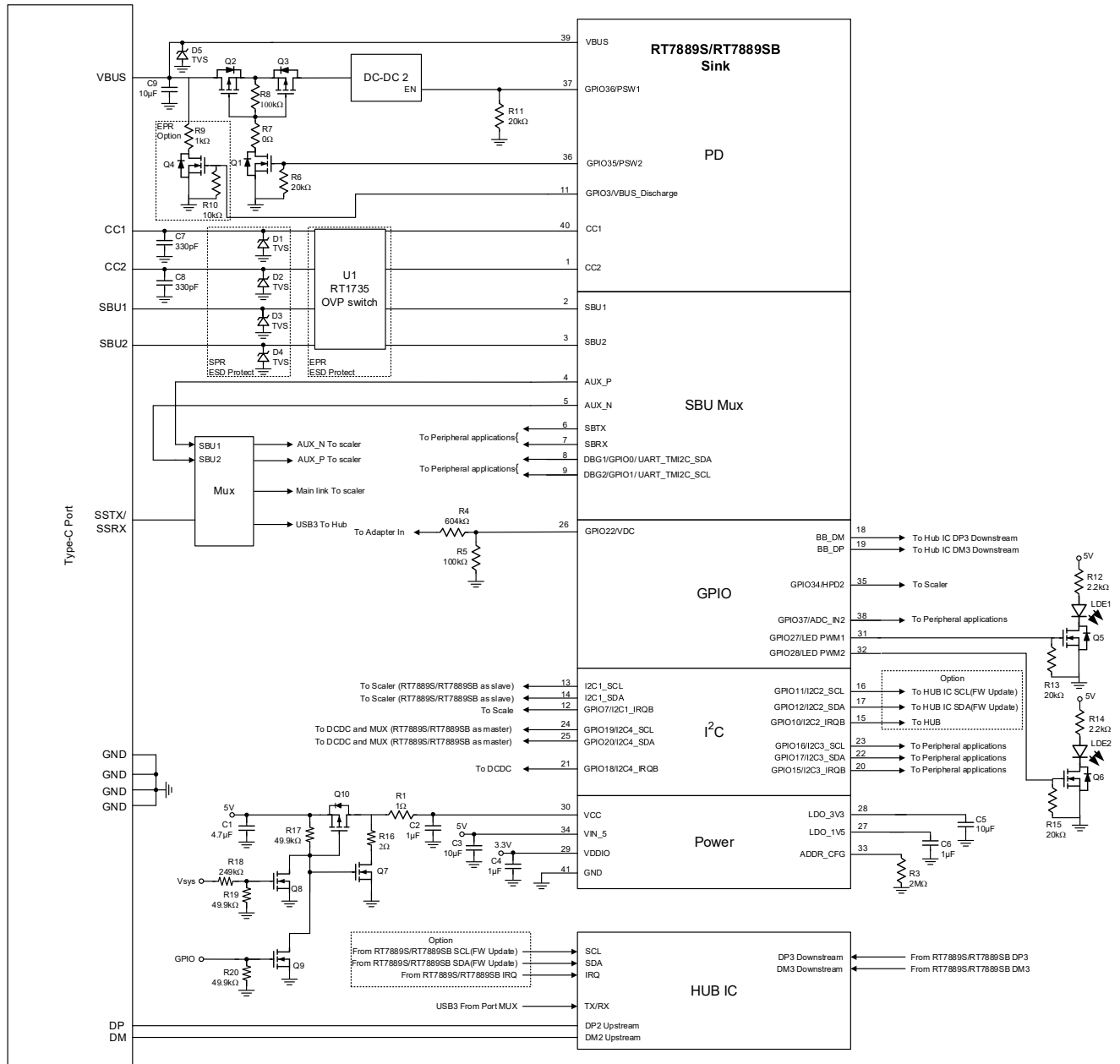


Table 1. Recommended Component Information

Pin	Part Number	Description	Package	Manufacturer	Power Range
VCC (C1)	GRM21BR61E475KA12K	4.7 μ F/25V/X5R (Note 6)	0805	muRata	-
VCC (C2)	GRM185R61A105KE26D	1 μ F/10V/X5R	0603	muRata	-
VCC (R1)	WR06W1R00FTL	1 Ω (Note 6)	0603	Walsin	-
VIN_5 (C3)	GRM21BR71A106KA73L	10 μ F/10V/X7R	0805	muRata	-
VDDIO (C4)	0603X105K250CT	1 μ F/25V/X5R	0603	Walsin	-
LDO_3V3 (C5)	GRM21BR71A106KA73L	10 μ F/10V/X7R	0805	muRata	-
LDO_1V5 (C6)	0603X105K250CT	1 μ F/25V/X5R	0603	Walsin	-
CC1 (C7) CC2 (C8)	0603N331J500CT	330pF/50V/NP0	0603	Walsin	-
CC1 (D1) CC2 (D2)	AZ4520-01F	TVS Diodes (Note 7)	DFN1610P2E	Amazing	SPR
SBU1 (D3) SBU2 (D4)	AZ4520-01F	TVS Diodes (Note 7)	DFN1610P2E	Amazing	SPR
CC1 (U1) CC2 (U1) SBU1 (U1) SBU2 (U1)	RT1735	OVP switch (Note 7)	WQFN-20L 3x3	Richtek	EPR
VBUS (D5)	ESD5401N	TVS Diodes	DFN1006-2	Will SEMI	-
VBUS (R2)	WR06X4990FTL	499 Ω	0603	Walsin	-
VCC (Q7) VCC (Q8) VCC (Q9)	2N7002	N-Channel MOSFET	SOT23	AOS	-
VCC (Q10)	AO3415	P-Channel MOSFET	SOT23	Onsemi	-
VCC (R16)	WR06W2R00FTL	2 Ω	0603	Walsin	-
VCC (R17) VCC (R19) VCC (R20)	WR06X4992FTL	49.9k Ω	0603	Walsin	-
VCC (R18)	WR06X2493FTL	249k Ω	0603	Walsin	-

Note 6. A 1 Ω series resistor and a 4.7 μ F bypass capacitor must be placed at the VCC pin.

Note 7. When the device power range is SPR, use the TVS AZ4520-01F; when the device power range is EPR, use the protection IC RT1735, so that PA_CC1, PA_CC2, PA_SBU1, PA_SBU2, PB_CC1, PB_CC2, PB_SBU1, and PB_SBU2 will pass IEC 61000-4-2: \pm 8kV contact discharge and \pm 15kV air discharge.

14 Application Information

(Note 9)

14.1 CPU and Memory

14.1.1 MCU

The RT7889S/RT7889SB integrates a 32-bit ARM Cortex-M0+ microcontroller, optimized for low-power operation through extensive clock gating. The core primarily utilizes 16-bit instructions and executes a subset of the Thumb-2 instruction set.

It includes a Nested Vectored Interrupt Controller (NVIC) with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC), which enables the processor to wake from deep sleep mode, allowing power to be switched off to the main processor during low-power states.

The CPU subsystem also includes a 16-channel DMA/Datawire block and a Serial Wire Debug (SWD) interface, a two-wire alternative to JTAG. The debug configuration for the RT7889S/RT7889SB supports four breakpoint comparators and two watchpoint comparators.

14.1.2 Flash

The RT7889S/RT7889SB has a 256kB flash module.

14.1.3 ROM

The device includes 64kB of supervisory ROM, which contains boot and configuration routines.

14.1.4 Cryptographic Accelerator

The integrated cryptographic accelerator supports the following requirements:

- SHA2 (256-bit)
- ECDSA
- CRC32

14.1.5 Power Mode

The RT7889S/RT7889SB supports three power modes: Active Mode, Idle Mode, and Deep Green Mode. Mode transitions are controlled by the system controller. The functions available in each mode are summarized in the table below.

Mode	48MHz	MCU	Function
Active	On	On	All functions
Idle	On	Off	More functions than in deep green mode: USB 2.0 Full Speed Billboard
Deep Green	Off	Off	I ² C1 to 4 IRQB1 to 4 GPIO as output HPD2 (GPIO34) VDC (GPIO22) USB PD USB 2.0 Full Speed Billboard Suspended SBU MUX ADC Alarm interrupt (at VBUS, ADC_IN2) Water Detection interrupt

In different power modes, the PD power-saving modes and USB 2.0 PHY functions are listed in the table below.

MCU	Port Status	USB 2.0 Full Speed Billboard	Port A TCPC
Deep Green Mode	no attached	Off	Auto low power
Deep Green Mode	attached	Off	Attached: Auto idle No attached: Auto low power
Idle Mode	attached	On	Attached: Auto idle No attached: Auto low power
Deep Green Mode	attached	Suspended command received	Attached: Auto idle No attached: Auto low power

14.2 Wake-Up Interrupt Controller

The RT7889S/RT7889SB integrates a Wake-Up Interrupt Controller (WIC) to enable wake from state-retention power-gating and from clock-gated states. The WIC is responsible for monitoring for assertion of interrupts when the processor is powered down in the idle or deep green operating mode. In these modes, the entire power domain is power-gated, and as such, the processor and NVIC are not available to check for interrupts. The WIC retains a copy of which peripheral interrupt sources to the NVIC were enabled when the processor entered idle or deep green mode. If an enabled interrupt detected while the CPU is powered down, the WIC asserts a wake request and performs a handshake with the system power controller to exit Idle or deep green mode so the CPU can service the interrupt. The WIC latches the event and presents a pending interrupt to the NVIC when CPU clocks are restored, ensuring the CPU observes the interrupt even if the peripheral’s raw status de-asserts before the CPU is fully powered.

Function	Pin Name	
I ² C Interrupt	I2C1_SCL	GPIO16/I2C3_SCL
	GPIO11/I2C2_SCL	GPIO19/I2C4_SCL
GPIO	GPIO7/I2C1_IRQB	GPIO15/I2C3_IRQB
	GPIO10/I2C2_IRQB	GPIO18/I2C4_IRQB
DisplayPort Hot-Plug Detect	GPIO34/HPD2	
Voltage Comparator	GPIO22/VDC	
USB PD	CC1	CC2
USB 2.0 Full Speed Billboard	BB_DP	BB_DM
ADC Alarm Interrupt	VBUS	GPIO37/ADC_IN2
Water Detection Interrupt	SBU1	SBU2

14.3 Power-On System

The RT7889S/RT7889SB can be powered from one of three possible external supply sources: VBUS (4.0V to 30V), or VCC (4V to 5.5V). The VBUS supply is regulated inside the chip with a HV low-dropout regulator (LDO) down to 3.3V and 1.5V level. The chip’s internal LDO_3V3 and LDO_1V5 rails seamlessly switch from the VBUS

regulator to VCC. However, when the internal power supply switches from VCC to the VBUS regulator, it causes the IC to reset, which limits the application.

The 5V VCC power supply in the product system is estimated to require 30mA to ensure that the RT7889S/RT7889SB can operate normally. VIN_5V must be capable of sourcing 300mA to support a 1.5 W VCONN load.

When additional power for the product system is required, the RT7889S/RT7889SB is powered by an external AC adapter. The system needs to supply power to VCC and VDDIO first, after which the RT7889S/RT7889SB can operate normally. Subsequently, when Type-C is connected, VIN_5 needs to be powered to enable the PD CC to output VCONN. Additionally, it can control peripheral circuits to enable VBUS, allowing them to provide power output as a PD source.

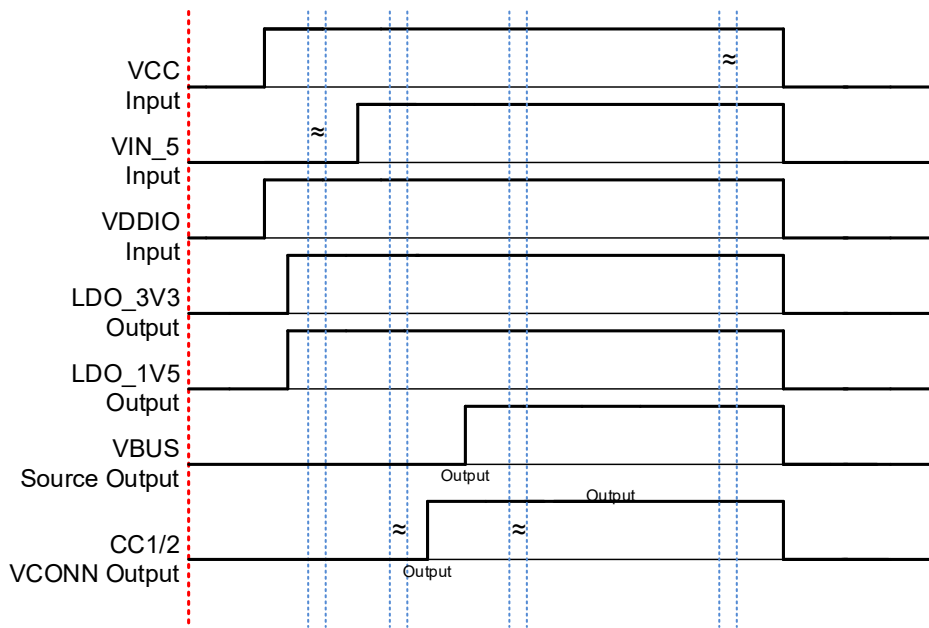


Figure 1. RT7889S/RT7889SB External Power Supply Timing Diagram

When the RT7889S/RT7889SB is in a dead battery condition, or in a system that requires power from the Type-C port, the device will begin normal operation after the Type-C port is connected, the CC line is attached, and power is supplied via VBUS. The system must supply power to VCC and VDDIO. Additionally, when the PD CC outputs VCONN, VIN_5 must be powered.

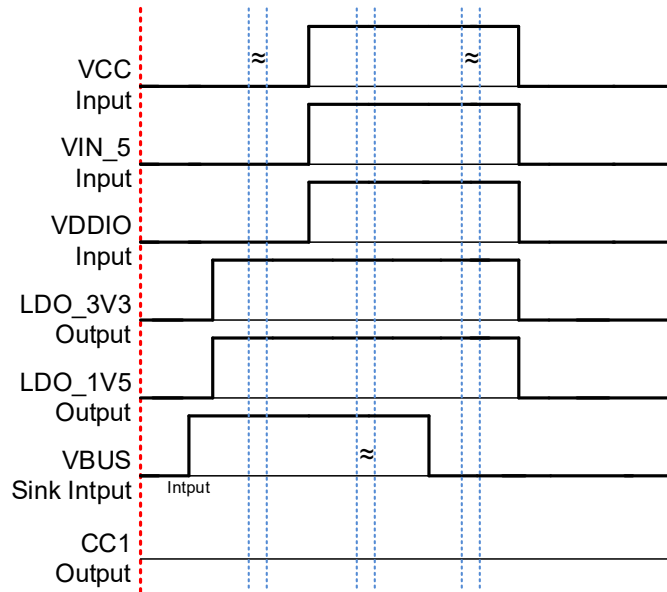


Figure 2. RT7889S/RT7889SB Requires Power from the Type-C Timing Diagram

14.4 USB-PD Physical Layer

The USB-PD subsystem includes the USB-PD physical layer block and its supporting circuits. The physical layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC in accordance with the PD 3.2 standard. All communication is conducted in a half-duplex manner. The physical layer (PHY) employs collision avoidance techniques to minimize communication errors on the channel.

14.5 VCONN Switch

The RT7889S/RT7889SB integrates two VCONN switches to power either the CC1 or CC2 pins. A dedicated VIN_5 power supply input pin provides power to E-marker cables through these VCONN switches. Each switch can deliver up to 1.5W per port over a valid VCONN voltage range of 4.85V to 5.5V on the CC1/2 pins for E-marker cables. The VCONN switches feature integrated protection circuits, including OVP, OCP, RVP, UVP, and short-to-GND protection, ensuring both normal operation and robust protection.

14.6 SBU MUX

The device features a 1:3 multiplexer (mux) for the SBU pins, allowing them to connect to different points within the system. Each RT7889S/RT7889SB provides outputs for the SBTX/RX (USB4/TBT) channel, AUX (DP) channel, and a debug channel. The SBTX/RX channel passes through an integrated level shifter, while the AUX and debug channels are passive pass-through connections.

An SBU OVP switch is connected to both the SBU-to-AUX and SBU-to-DBG paths. The ON resistance of this switch is included in the total resistance of each SBU channel (RON_SBU_AUX and RON_SBU_DEBUG). The SBTX/RX channel includes an integrated level shifter.

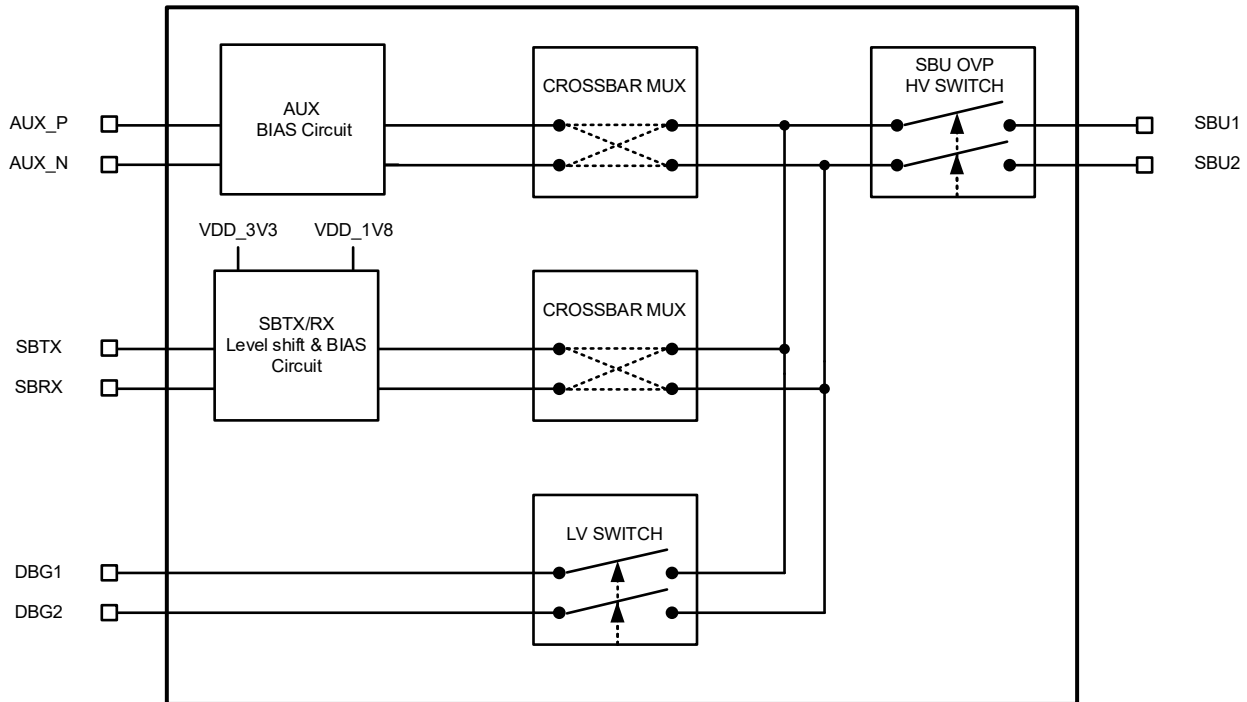


Figure 3. Diagram of SBU MUX and OVP Switch

14.6.1 SBU OVP

Each SBU pin includes an OVP comparator that disables the switch when an overvoltage condition is detected. If the SBU voltage exceeds 4.5V, the SBU OVP HV switch is disabled.

14.6.2 AUX Channel

The output from the SBU OVP module can be connected to either the AUX_P or AUX_N output through a crossbar multiplexer. Each output features bias circuits with configurable pull-down and pull-up resistors. When the SBU MUX is set to the AUX channel application, SBU1 is connected to AUX_P and SBU2 is connected to AUX_N by default.

14.6.3 SBTX/SBRX Channel

The USB4/TBT output from the SBU MUX passes through a level shifter, converting from SBU to SBTX/RX at VDD_3V3/VDD_1V8. Each output also includes a biasing resistor. When the SBU MUX is set to the SBTX/SBRX channel application, SBU1 is connected to SBTX and SBU2 is connected to SBRX by default.

14.6.4 Debug Channel

This passive mux channel can be used to pass signals such as I²C or UART, typically for system debugging purposes.

14.7 USB 2.0 Full-Speed PHY

The RT7889S/RT7889SB includes one USB 2.0 full-speed (12Mbps) device to support billboard class and HID class applications, such as firmware downloads. The device can utilize these widely available USB interfaces to transmit and receive data with USB hosts, typically PCs or laptops.

14.8 11-Bit SAR ADC

The RT7889S/RT7889SB features an 11-bit SAR (Successive Approximation Register) ADC, as shown in [Figure 4](#). The ADC uses an analog input multiplexer to support multiple inputs from various voltages and currents within the device. The ADC output can be read via I²C for customized requirements and also serves as an input for the automatic ADC monitor circuits. Additionally, the VBUS, and ADC_IN2 pins support the ADC Alarm interrupt function.

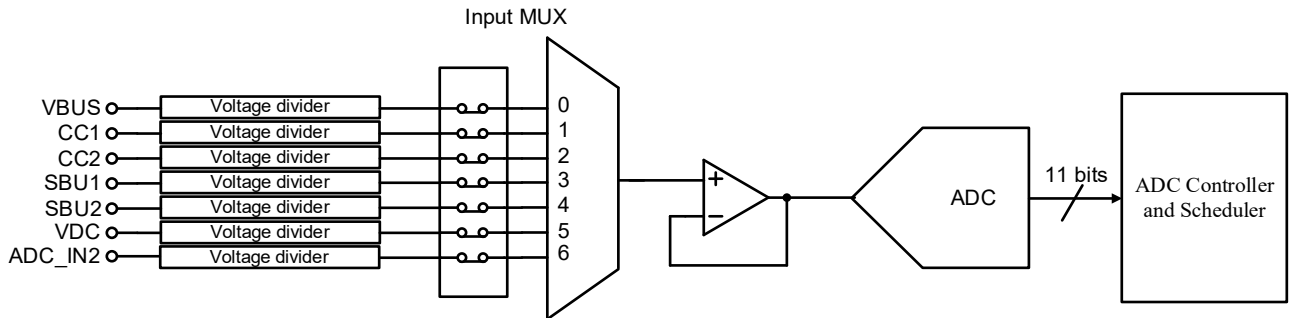


Figure 4. Diagram of ADC input

14.9 Water Detection

The RT7889S/RT7889SB integrates a water detection circuit on the SBU1 and BU2 pins to perform anomaly detection prior to device attachment.

14.10 DisplayPort Hot-Plug Detect (HPD)

The RT7889S/RT7889SB supports DisplayPort Alternate Mode as both a DP source and DP sink. It provides HPD converter functionality on the GPIO34/HPD2 pins, which can operate as either HPD TX or RX. The PD messaging events are translated to the corresponding HPD pin based on the selected the DP mode.

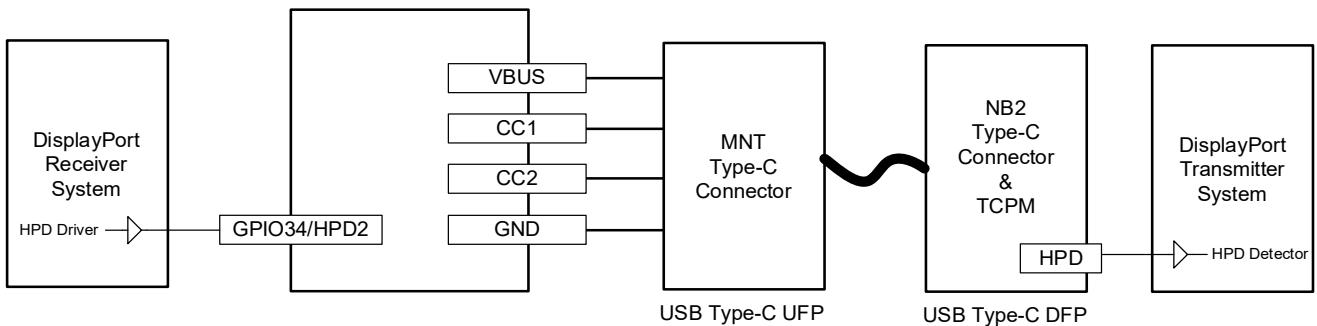


Figure 5. PD-to-HPD Converter: Passing HPD Signal in a DisplayPort System

14.11 Over-Temperature Protection

The RT7889S/RT7889SB monitors its internal temperature to prevent thermal failures. When the junction temperature reaches 120°C or 150°C, the chip disables the VCONN and SBU switches. The IC resumes normal operation once the junction temperature has decreased by 30°C or 40°C. Each port features a dedicated thermal shutdown monitor for its VCONN paths. If a port's VCONN path temperature exceeds 120°C or 150°C, the VCONN and SBU switches for that port are disabled. When the temperature drops below the threshold and the hysteresis is cleared, the VCONN paths resume normal operation.

14.12 GPIO Application

The following table lists the GPIO power domains and the describes the input/output types for various applications.

Pin Number	Pin Name	Power Domain	Output Stage	Input form
8	DBG1/GPIO0/UART_TMI2C_SDA	VDDIO	Push-pull	Polling
9	DBG2/GPIO1/UART_TMI2C_SCL	VDDIO	Push-pull	Polling
10	GPIO2	VDDIO	Push-pull	Polling
11	GPIO3/VBUS_Discharge	VDDIO	Push-pull	Polling
12	GPIO7/I2C1_IRQB	LDO_3V3	Open-drain	Interrupt
15	GPIO10/I2C2_IRQB	LDO_3V3	Open-drain	Interrupt
16	GPIO11/I2C2_SCL	LDO_3V3	Open-drain	Polling
17	GPIO12/I2C2_SDA	LDO_3V3	Open-drain	Polling
20	GPIO15/I2C3_IRQB	LDO_3V3	Open-drain	Interrupt
23	GPIO16/I2C3_SCL	LDO_3V3	Open-drain	Polling
22	GPIO17/I2C3_SDA	LDO_3V3	Open-drain	Polling
21	GPIO18/I2C4_IRQB	LDO_3V3	Open-drain	Interrupt
24	GPIO19/I2C4_SCL	LDO_3V3	Open-drain	Polling
25	GPIO20/I2C4_SDA	LDO_3V3	Open-drain	Polling
26	GPIO22/VDC	VDDIO	Push-pull	Polling
31	GPIO27/LED PWM1	VDDIO	Push-pull	Polling
32	GPIO28/LED PWM2	VDDIO	Push-pull	Polling
35	GPIO34/HPD2	LDO_3V3	Open-drain	Interrupt
36	GPIO35/PSW2	VDDIO	Push-pull	Polling
37	GPIO36/PSW1	VDDIO	Push-pull	Polling
38	GPIO37/ADC_IN_2	LDO_3V3	Open-drain	Polling

14.13 I²C Interface

The RT7889S/RT7889SB supports four channels of slave I²C. The I²C interface can be configured for up to 128 slave addresses by adjusting the resistance between the ADDR (pin 59) to GND, as well as through MCU register settings.

Table 2. I²C1, I²C2, I²C3, and I²C4 Slave Address (Note 8)

Address	MSB						LSB	R/W bit	R/W
	7	6	5	4	3	2			
ADDR Bit	7	6	5	4	3	2	1	1/0	--
How to Config	Fix	Fix	Fix	Fix	Fix	By ADDR	By ADDR	1/0	--
ADDR 10kΩ	0	1	0	0	1	0	0	1/0	49/48
ADDR 270kΩ	0	1	0	0	1	0	1	1/0	4B/4A
ADDR 750kΩ	0	1	0	0	1	1	0	1/0	4D/4C
ADDR 2MΩ	0	1	0	0	1	1	1	1/0	4F/4E

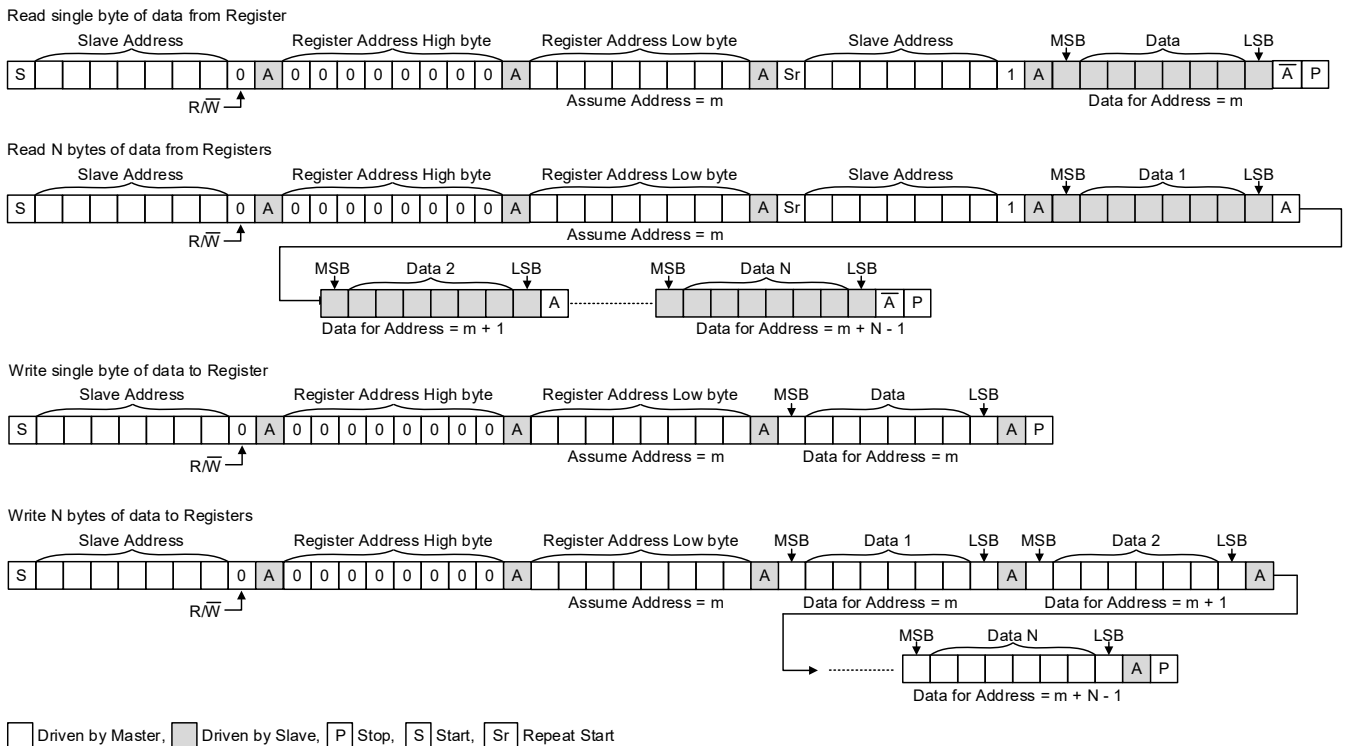
Note 8. The R/W field example is 0b'01001 with the MSB shown as an example.

When the RT7889S/RT7889SB operates with 4 slave I²C channels simultaneously, each channel supports a maximum speed of 400kHz. However, when only 2 slave I²C channels are used, one channel can operate at up to 1MHz, while the other supports up to 400kHz.

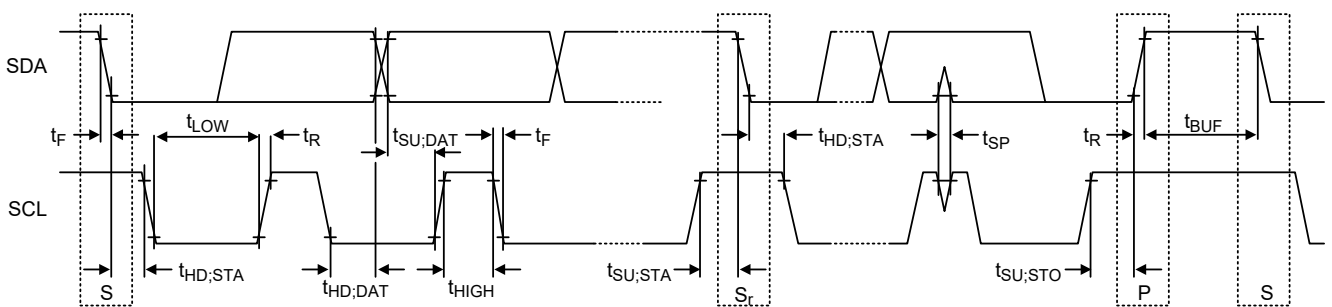
Each I²C bus interface must be connected to the power node through a 1kΩ pull-up resistor, with independent connections to the processor for each channel.

The I²C timing diagrams are provided below.

14.13.1 Read and Write Function



14.13.2 I²C Waveform Information



14.14 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-40L 5x5 package, the thermal resistance, θ_{JA} , is 35.77°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as follows:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (35.77^\circ\text{C/W}) = 2.8\text{W for a WQFN-40L 5x5 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curve in [Figure 6](#) allows the user to see the effect of rising ambient temperature on the maximum power dissipation.

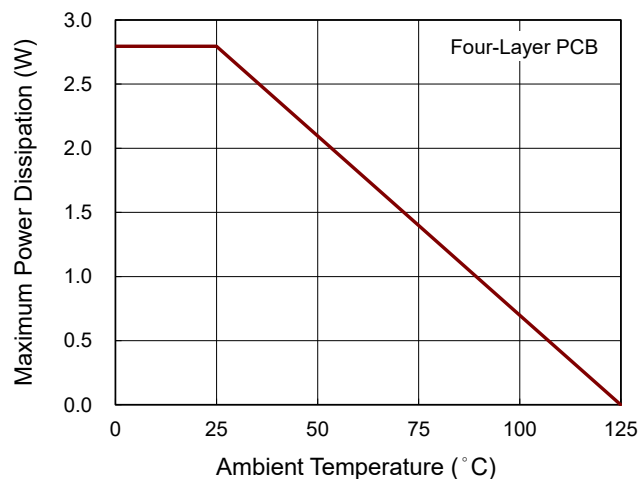


Figure 6. Derating Curve of Maximum Power Dissipation

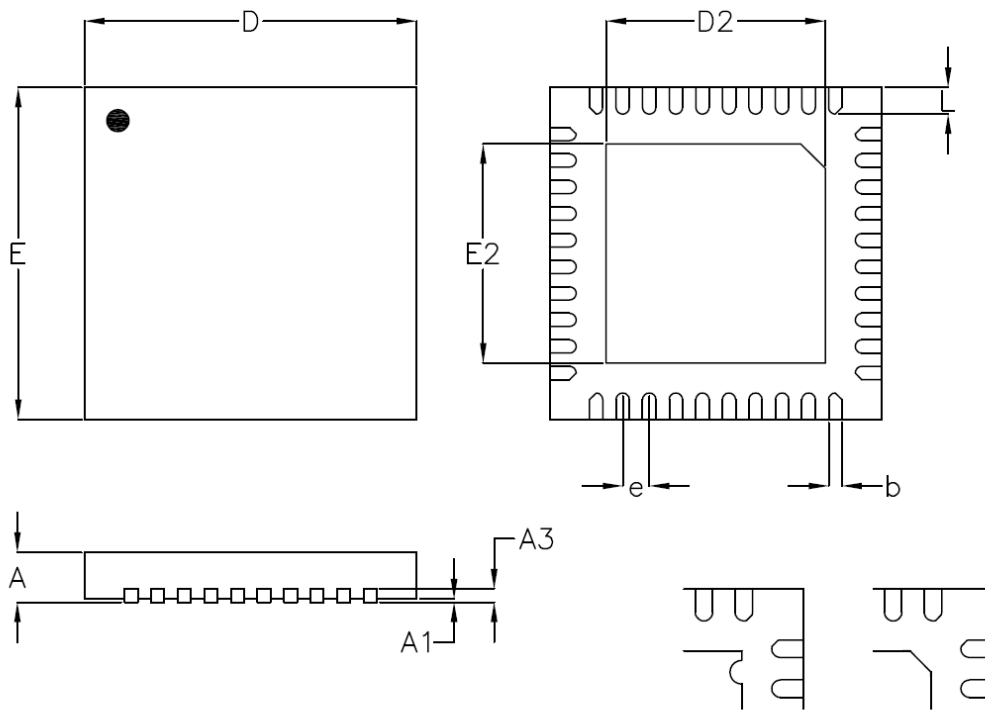
14.15 Layout Considerations

Appropriate routing and component placement are essential to maintain the signal integrity of the USB2.0, SBU, and CC signals. The following guidelines apply to the RT7889S/RT7889SB:

- Place bypass capacitors as close as possible to the VCC, VDDIO, LDO_3V3, LDO_1V5 and VIN_5 pins. Connect them to a solid ground plane using short, wide traces and multiple vias.
- Route USB 2.0 and SBU traces straight and short; minimize sharp bends and avoid stubs.
- To improve ESD immunity, place TVS diodes and MLCCs for CC1/2, SBU1/2, and BB_DP/DM as close as possible to the USB Type-C connector, with low-impedance paths to GND.

Note 9. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek’s product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

15 Outline Dimension



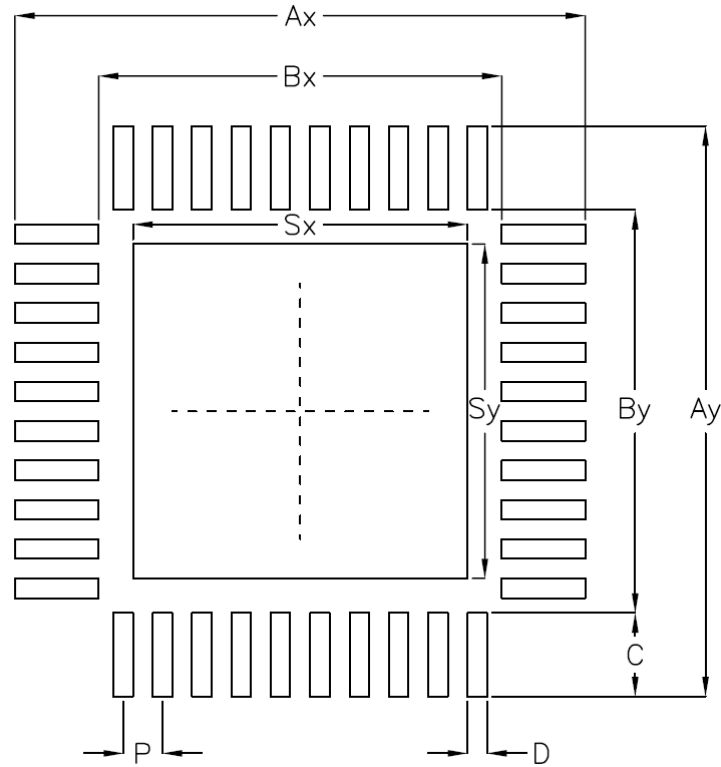
DETAILA
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
B	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

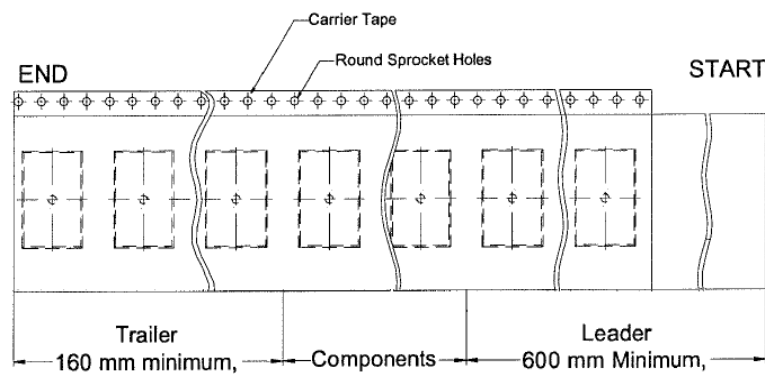
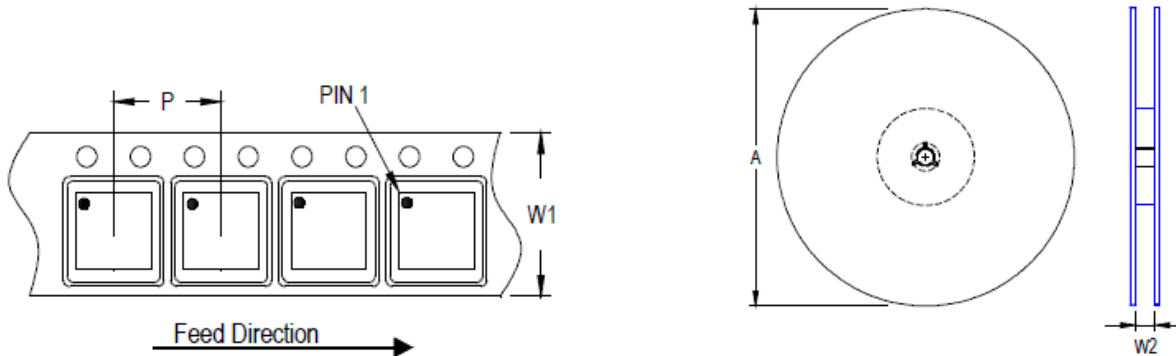
16 Footprint Information



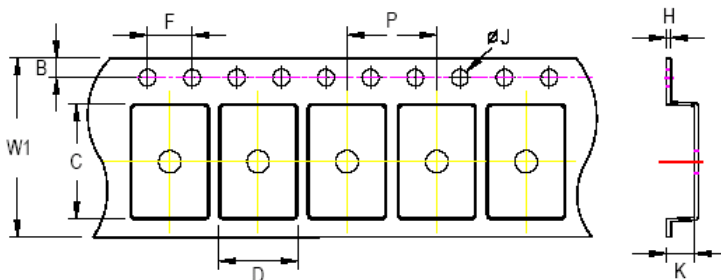
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN5*5-40	40	0.40	5.80	5.80	4.10	4.10	0.85	0.20	3.40	3.40	±0.05

17 Packing Information

17.1 Tape and Reel Data









Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 5x5	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

17.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 <p>Reel 7"</p>	4	 <p>3 reels per inner box Box A</p>
2	 <p>HIC & Desiccant (1 Unit) inside</p>	5	 <p>12 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Container Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W)	7"	1,500	Box A	3	4,500	Carton A	12	54,000
QFN/DFN 5x5			Box E	1	1,500	For Combined or Partial Reel.		

17.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

Richtek Technology Corporation

14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

Richtek products are sold by description only. Richtek reserves the right to change the circuitry and/or specifications without notice at any time. Customers should obtain the latest relevant information and data sheets before placing orders and should verify that such information is current and complete. Richtek cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Richtek product. Information furnished by Richtek is believed to be accurate and reliable. However, no responsibility is assumed by Richtek or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Richtek or its subsidiaries.

Copyright © 2026 Richtek Technology Corporation. All rights reserved. **RICHTEK** is a registered trademark of Richtek Technology Corporation.

18 Datasheet Revision History

Version	Date	Description
00	2026/4/9	First Edition