RICHTEK®

RT7272A

3A, 36V, 500kHz Synchronous Step-Down Converter

1 General Description

The RT7272A is a high efficiency, current mode synchronous step-down DC-DC converter that can deliver up to 3A output current over a wide input voltage range from 4.5V to 36V. The RT7272A integrates a 150mΩ On-Resistance of high-side MOSFET and an 80mΩ On-Resistance of low-side MOSFET to achieve high conversion efficiency up to 95%. The current mode control architecture supports fast transient response and simple compensation circuit.

A cycle-by-cycle current limit function provides protection against shorted output and an internal soft-start eliminates input current surge during start-up. The RT7272A provides complete protection functions such as input under-voltage lockout, output under-voltage protection, over-current protection and over-temperature protection.

The RT7272A is available in the thermal enhanced SOP-8 (Exposed Pad) package.

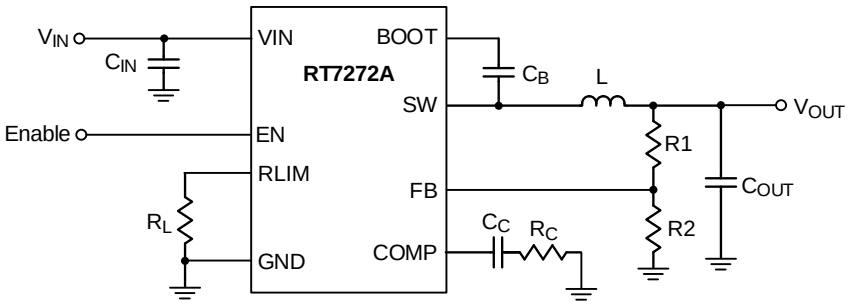
2 Features

- **4.5V to 36V Input Voltage Range**
- **3A Output Current**
- **Internal N-MOSFETs**
- **Current Mode Control**
- **Fixed Switching Frequency Operation: 500kHz**
- **Adjustable Output Voltage from 0.8V to 30V**
- **High Efficiency Up to 95%**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Current Limit**
- **Input Undervoltage Lockout**
- **Output Undervoltage Protection**
- **Over-Temperature Protection**
- **Adjustable Current Limit**

3 Applications

- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Notebook Computers
- Point of Load Regulator in Distributed Power System
- Digital Set-Top Boxes
- Personal Digital Recorders
- Broadband Communications
- Flat Panel TVs and Monitors
- Vehicle Electronics

4 Simplified Application Circuit



5 Ordering Information

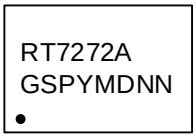
RT7272A□□

- Package Type[1]
  SP: SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  G: Richtek Green Policy Compliant [2]

Note 1.

- Marked with [1] indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with [2] indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information



RT7272AGSP : Product Code
YMDNN : Date Code

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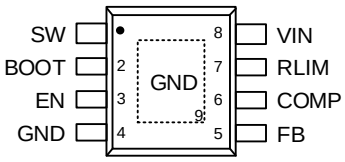
7 Pin Configuration

(TOP VIEW)

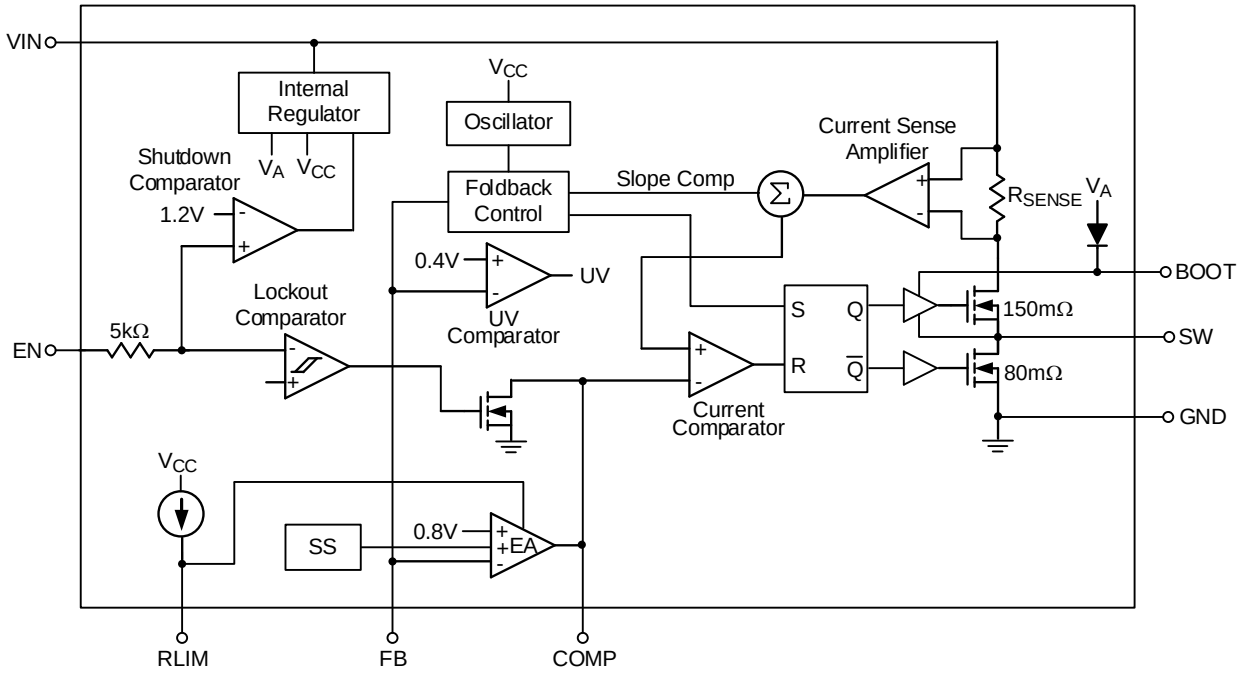


SOP-8(Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch node. Connect to external L-C filter.
2	BOOT	Bootstrap supply for high-side gate drive. A 100nF or greater capacitor is recommended to connect from BOOT pin to SW pin.
3	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
5	FB	Feedback input pin. The FB pin is connected to the converter output. It is used to set the output of the converter to regulate to the specific output voltage via a resistive divider.
6	COMP	Compensation node. The COMP pin is used to compensate the regulation control loop. Connect a series RC network from COMP to GND.
7	RLIM	Current limit setting. Connect a resistor from the RLIM pin to ground to set the current limit.
8	VIN	Power input. The input voltage range is from 4.5V to 36V. Must bypass with a suitable large ceramic capacitor.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- –0.3V to 40V
- Switch Voltage, SW ---------- –0.3V to 40.3V
  SW (t < 10ns) ---------- –5V to 46V
- V_{BOOT} - V_{SW} ---------- –0.3V to 6V
- Other Pins Voltage ---------- –0.3V to 40V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  HBM (Human Body Model)---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 36V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 85°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WET-WQFN-52L 6x6 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	39	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	61.5	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	2.94	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB) (Note 5)	37.97	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter (Note 6)	8.78	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (Note 6)	21.94	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 67mm x 47mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 12V, C_{IN} = 20µF, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	0.5	3	µA
Quiescent Current	I_Q	V_{EN} = 3V, V_{FB} = 0.9V	--	0.9	1.2	mA
Reference Voltage	V_{REF}	4.5V ≤ V_{IN} ≤ 36V	0.788	0.8	0.812	V
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	150	--	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	80	--	mΩ
High Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V	--	0	10	µA
High-Side Switch (Peak) Current Limit Range	I_{LIM_H}		1.9	--	7	A
High-Side Switch (Peak) Current Limit (Note 7)	I_{LIM_H}	Minimum duty cycle, R_{LIM} = 57.6kΩ	1.9	2.5	3.1	A
		Minimum duty cycle, R_{LIM} = 84.5kΩ	2.7	3.5	4.2	
		Minimum duty cycle, R_{LIM} = 137kΩ	4.8	5.5	6.3	
Low-Side Switch (Valley) Current Limit	I_{LIM_L}	From drain to source	--	1.5	--	A
Oscillator Frequency	f_{OSC}		450	500	550	kHz
Short Circuit Oscillation Frequency	f_{OSC_SC}	V_{FB} = 0V	--	75	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	--	90	--	%
Minimum On-Time	t_{ON_MIN}		--	100	--	ns
EN Input Voltage Logic-High	V_{EN_H}		1.4	1.65	2	V
EN Input Voltage Logic-Low	V_{EN_L}		1.2	1.45	1.9	V
EN Input Voltage Hysteresis	V_{EN_HYS}		--	0.2	--	V
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	V_{IN} rising	3.9	4.1	4.3	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}		--	250	--	mV
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
COMP to Current Sense Transconductance	g_{CS}	ΔI_{COMP} = ±10µA	--	4.7	--	A/V
Error Amplifier Transconductance	g_m		--	1000	--	µA/V
Load Regulation	V_{LOAD_REG}		--	--	0.05	%/A
Line Regulation	V_{LINE_REG}	V_{IN} = 4.5V to 36V	--	--	0.1	%

Note 7. R_{LIM} (kΩ) = [I_{LIM_H} x 24.14 x (1 + 0.024 x (I_{LIM_H} – 3.5)) – 1.3], where U_{OC} is desired upper switch peak current limit value.

15 Typical Application Circuit

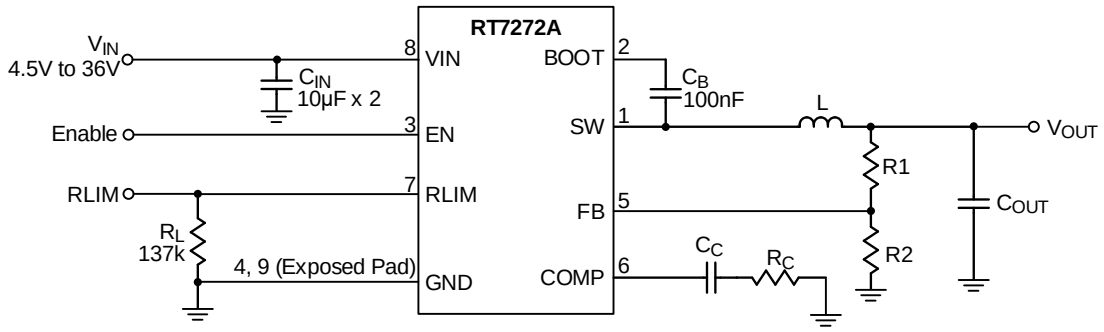


Figure 1. The Typical Application Circuit of the RT7272A

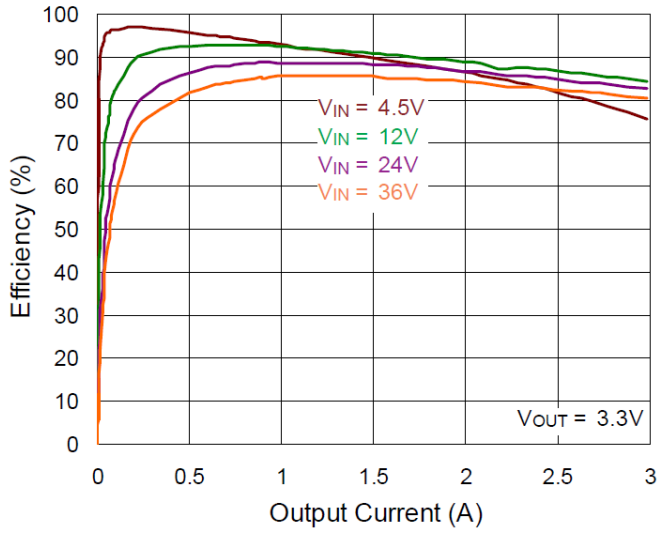
Table 1. Suggested Component Values (Note 8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	L (µH)	C_C (nF)	C_{OUT} (µF)
12	47	3.35	47	10	2.7	22 x 2
8	27	3	36	8.2	2.7	22 x 2
5	62	11.8	24	6.8	2.7	22 x 2
3.3	75	24	16	4.7	2.7	22 x 2
2.5	25.5	12	12	3.6	2.7	22 x 2
1.2	30	60	6.8	2.2	2.7	22 x 2

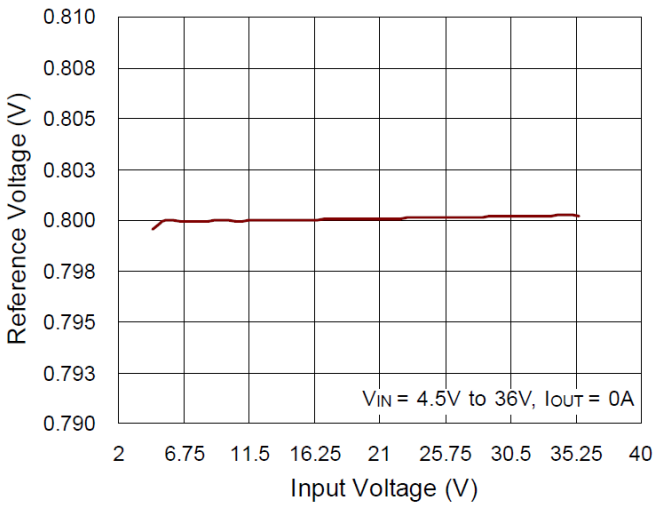
Note 8. All input and output capacitors are the suggested values, referring to the effective capacitances, which may be subject to any de-rating effect, like a DC bias.

16 Typical Operating Characteristics

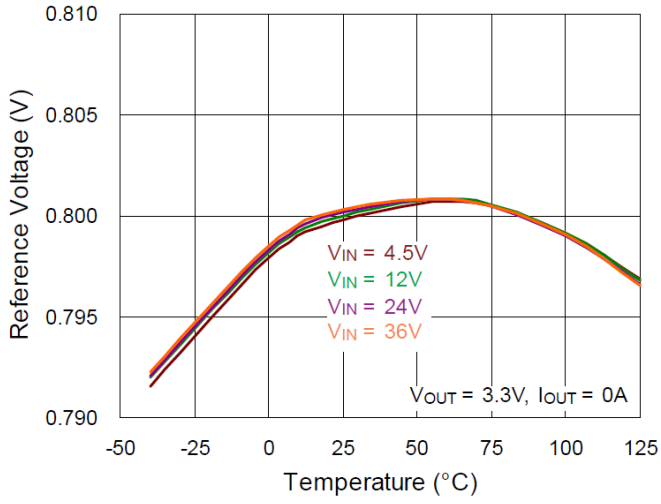
Efficiency vs. Output Current



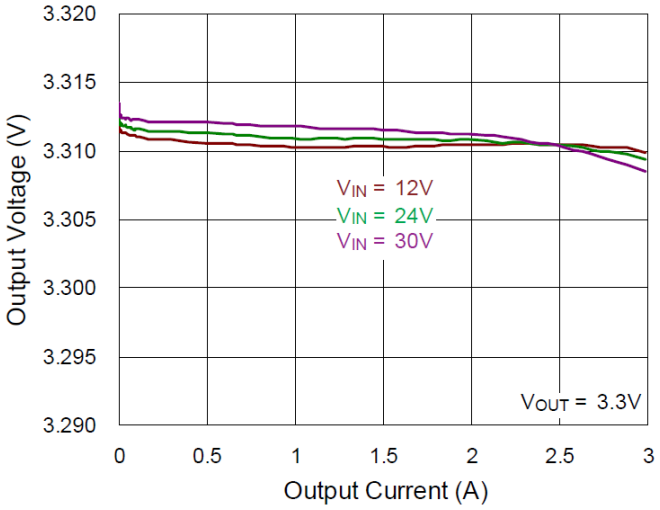
Reference Voltage vs. Input Voltage



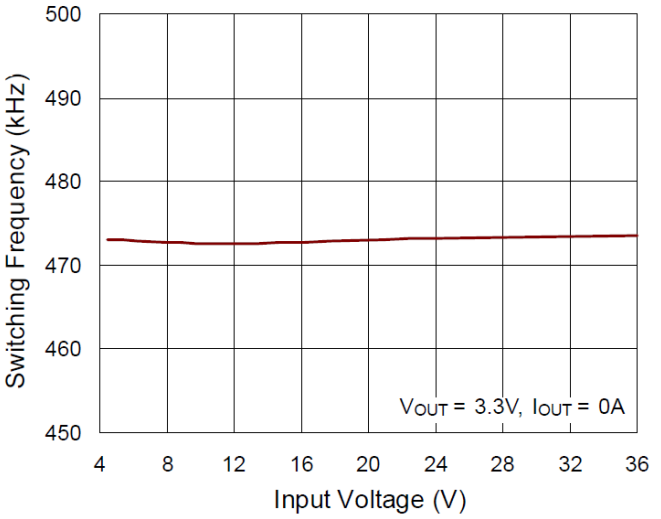
Reference Voltage vs. Temperature



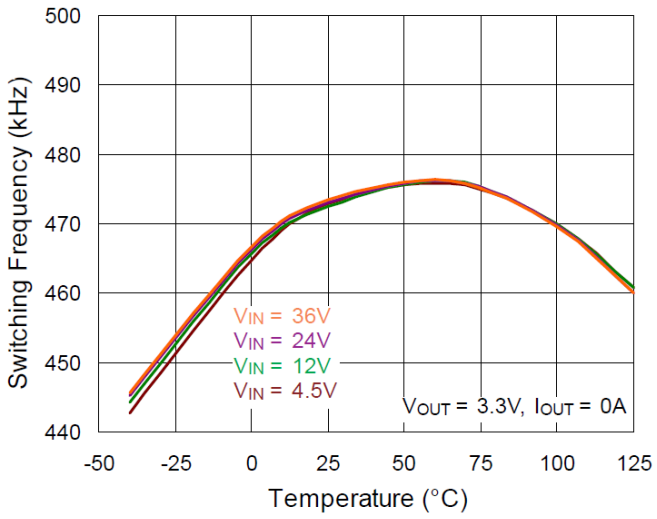
Output Voltage vs. Output Current



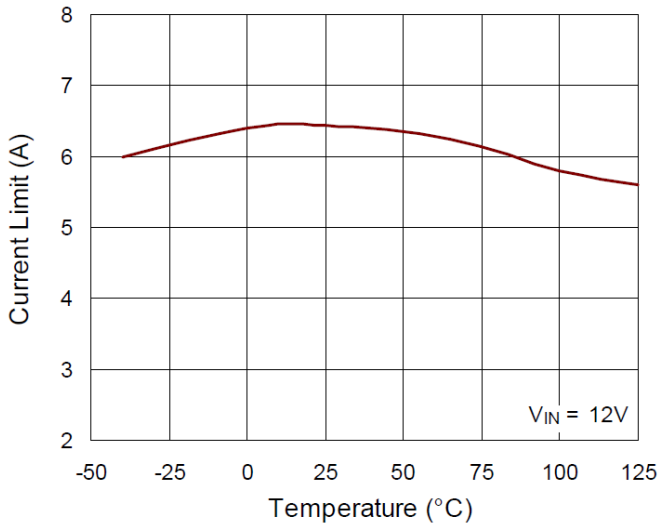
Switching Frequency vs. Input Voltage



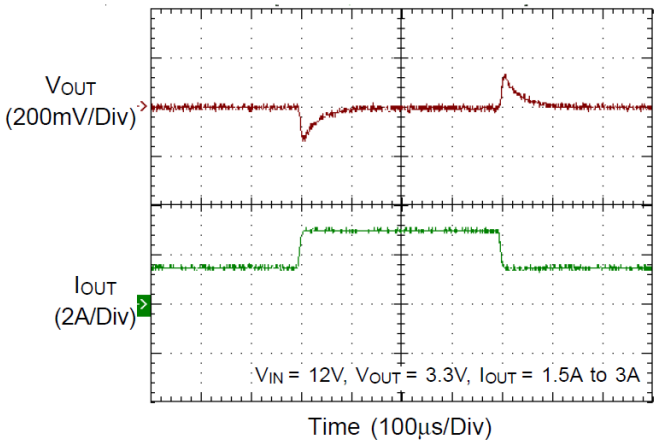
Switching Frequency vs. Temperature



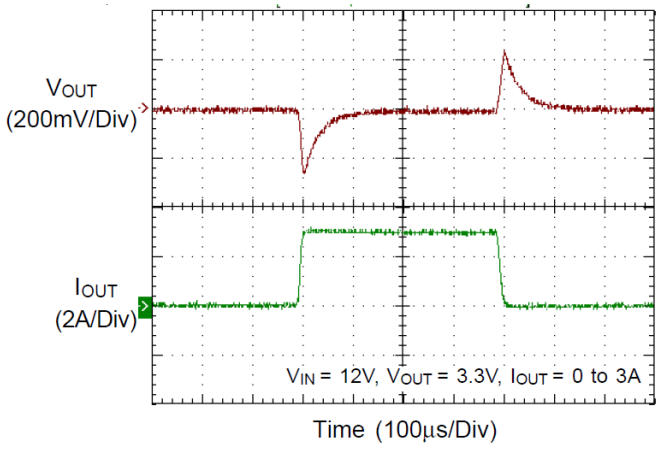
Current Limit vs. Temperature



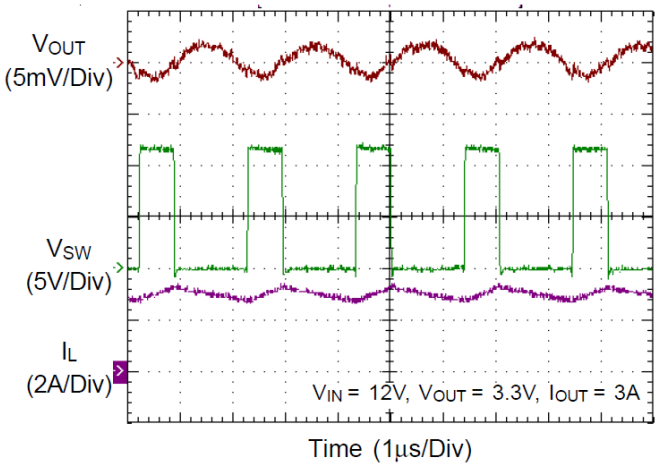
Load Transient Response



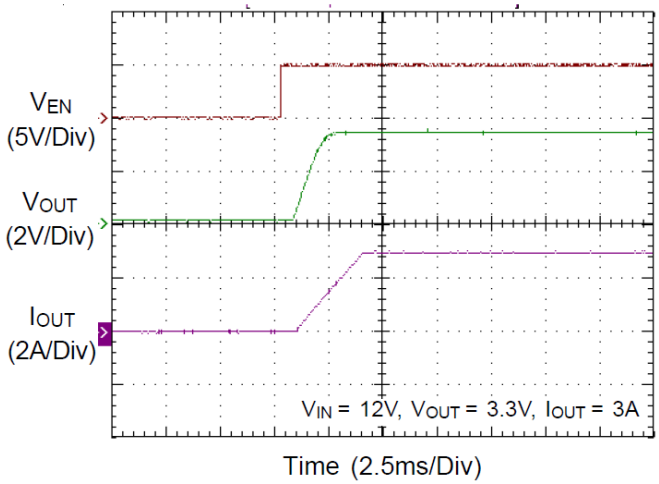
Load Transient Response



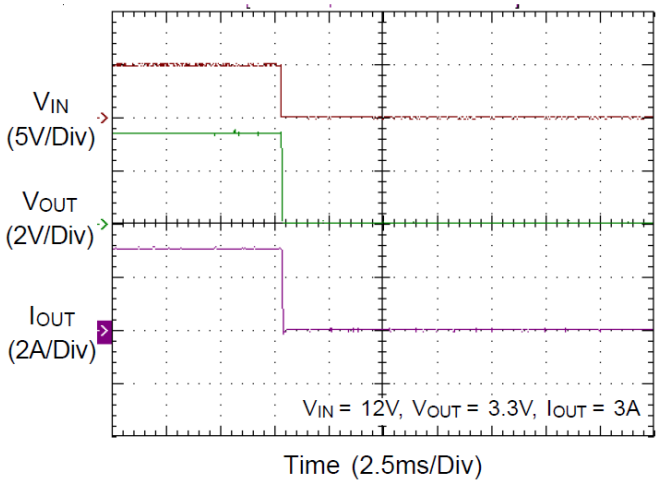
Switching



Power On from EN



Power Off from EN



17 Operation

The RT7272A is a constant frequency, current mode synchronous step-down converter. In normal operation, the high-side N-MOSFET is turned on when the S-R latch is set by the oscillator and turned off when the current comparator resets the S-R latch. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

17.1 Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal (FB pin voltage, V_{FB}) with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference. The error amplifier's output voltage then rises to allow higher inductor current to match the load current.

17.2 Oscillator

The internal oscillator runs at fixed frequency 500kHz. In short circuit condition, the frequency is reduced to 75kHz for low power consumption.

17.3 Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for high side gate driver.

17.4 Soft-Start (SS)

An internal current source charges an internal capacitor to build a soft-start ramp voltage. The FB pin voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 2ms.

17.5 Current Setting

The current limit of high-side MOSFET is adjustable by an external resistor connected to the RLIM pin. The current limit range is from 1.9A to 7A. When the inductor current reaches the current limit threshold, the COMP pin voltage will be clamped to limit the inductor current.

17.6 Undervoltage (UV) Comparator

If the feedback voltage (V_{FB}) is lower than 0.4V, the UV Comparator will go high to turn off the high-side MOSFET. The output undervoltage protection is designed to operate in hiccup mode. When the UV condition is removed, the converter will resume switching.

17.7 Over-Temperature Protection

The over-temperature protection will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will automatically resume switching.

18 Application Information

(Note 9)

18.1 Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 2.

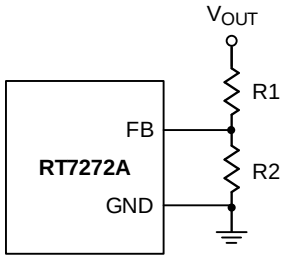


Figure 2. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the internal reference voltage (typical 0.8V).

18.2 External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin as shown in Figure 3. This capacitor provides the gate driver voltage for the high side MOSFET. It is recommended to add an external bootstrap diode between an external 5V and BOOT pin to improve efficiency when input voltage is lower than 5.5V or duty ratio is higher than 65%. Select the bootstrap diode with fast switching features, such as the IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7272A. Note that the external boot voltage must be lower than 5.5V

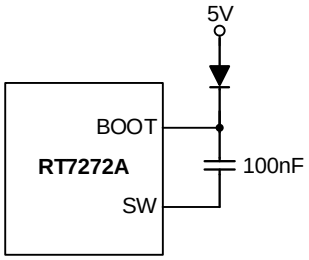


Figure 3. External Bootstrap Diode

18.3 Chip Enable Operation

The EN pin is used for the RT7272A enable control. Pull the EN pin voltage (V_{EN}) to logic-low voltage (V_{EN_L}) the RT7272A shuts down and enters to low quiescent current state about 3μA. The RT7272A starts switching again once pull the V_{EN} to logic-high voltage (V_{EN_H}). For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 4).

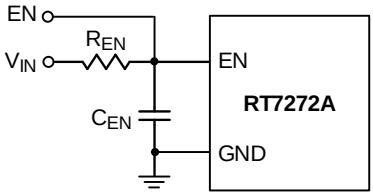


Figure 4. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 5. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

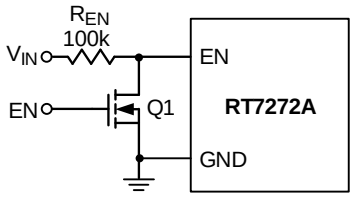


Figure 5. Digital Enable Control Circuit

18.4 Undervoltage Protection

The RT7272A provides Undervoltage Protection (UVP) with hiccup mode. When the V_{FB} voltage drops below 0.4V, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT7272A will restart automatically and the UVP is disabled during soft-start period as shown in Figure 6. When the UVP condition is removed, the converter will return to operate normally.

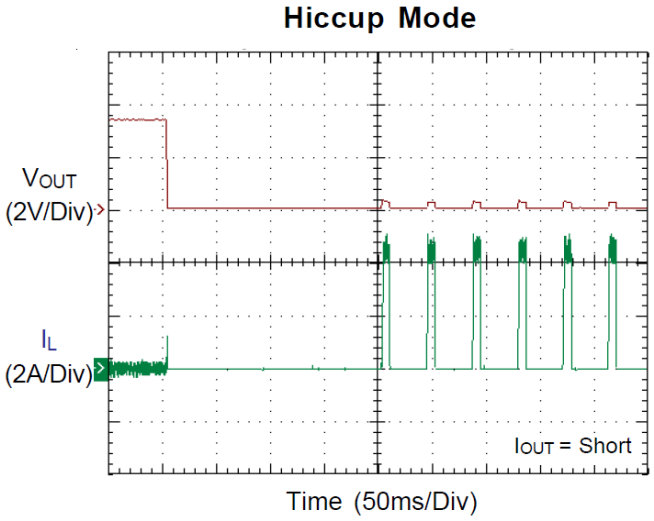


Figure 6. Hiccup Mode Undervoltage Protection

18.5 Over-Temperature Protection

The RT7272A features an Over-Temperature Protection (OTP) to prevent the device from overheating due to excessive power dissipation. The OTP will shut down the switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of the operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

18.6 Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{f \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of ΔI_L = 0.24(I_{MAX}) will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f \times 0.24 \times I_{(MAX)}} \right) \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient temperature) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions(mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

18.7 Input Capacitor and Output Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the Source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at V_{IN} = 2xV_{OUT}, where I_{RMS} = I_{OUT} / 2. The worst case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10μF low ESR ceramic capacitors are suggested. For the suggested capacitor, please refer to Table 3 for more details. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8 f C_{OUT}} \right)$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

18.8 Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

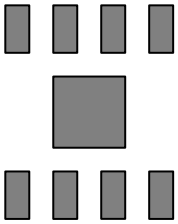
Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions of the RT7272A, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

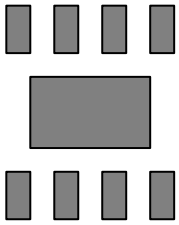
$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W (min. copper area PCB layout)

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.04W (70mm^2 copper area PCB layout)

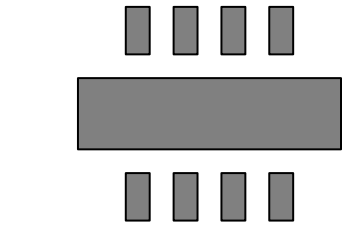
The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package. As shown in Figure 7, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 7.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 7.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm$_2$ (Figure 7.e) reduces the θ_{JA} to 49°C/W. The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 8 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.



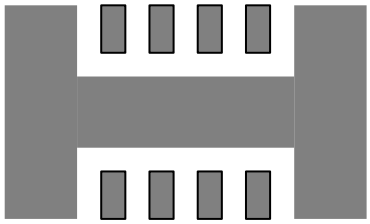
(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} =75°C/W



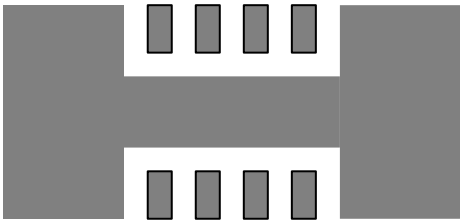
(b) Copper Area = 10 mm^2, θ_{JA} =64°C/W



(c) Copper Area = 30 mm^2, θ_{JA} =54°C/W



(d) Copper Area = 50 mm^2, θ_{JA} =51°C/W



(e) Copper Area = 70 mm^2, θ_{JA} =49°C/W

Figure 7. Thermal Resistance vs. Copper Area Layout Design

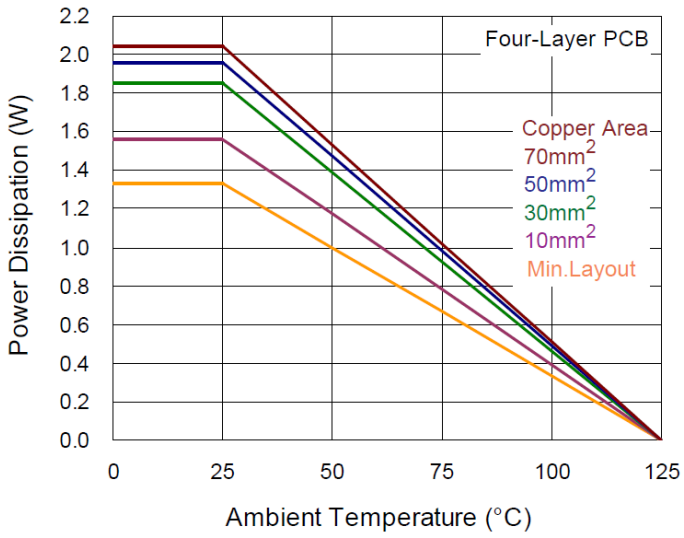


Figure 8. Derating Curve of Maximum Power Dissipation

18.9 Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB can radiate excessive noise and contribute to the converter instability. The following points must be considered before starting a layout for the RT7272A.

- Input capacitor must be placed as close to the IC as possible.
- SW should be connected to inductor by wide and short trace.

- The R_L resistor, compensator and feedback components must be connected as close to the device as possible.

Figure 9 shows the layout example for the RT7272A.

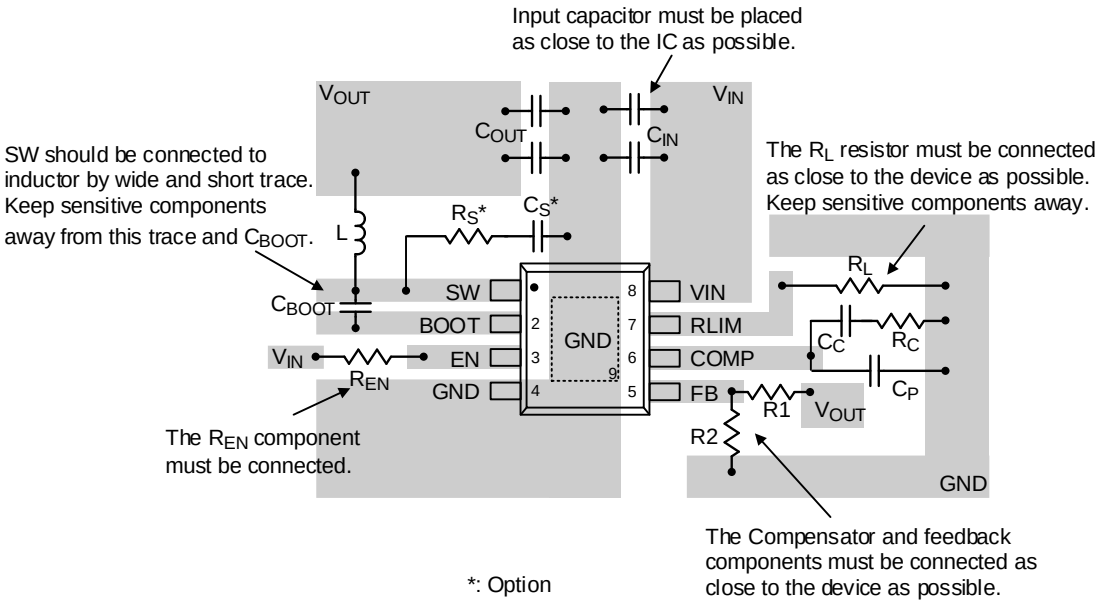


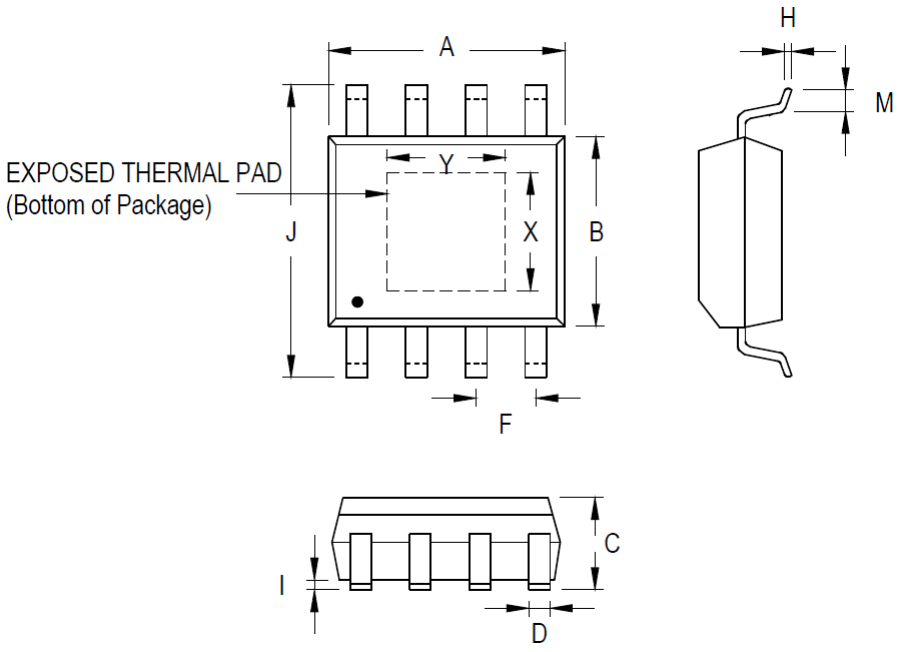
Figure 9. PCB Layout Guide

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
CIN	MURATA	GRM32ER71H475K	4.7	1206
CIN	TAIYO YUDEN	UMK325BJ475MM-T	4.7	1206
CIN	MURATA	GRM31CR61E106K	10	1206
CIN	TDK	C3225X5R1E106K	10	1206
CIN	TAIYO YUDEN	TMK316BJ106ML	10	1206
COUT	MURATA	GRM31CR60J476M	47	1206
COUT	TDK	C3225X5R0J476M	47	1210
COUT	MURATA	GRM32ER71C226M	22	1210
COUT	TDK	C3225X5R1C22M	22	1210

Note 9. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

19 Outline Dimension

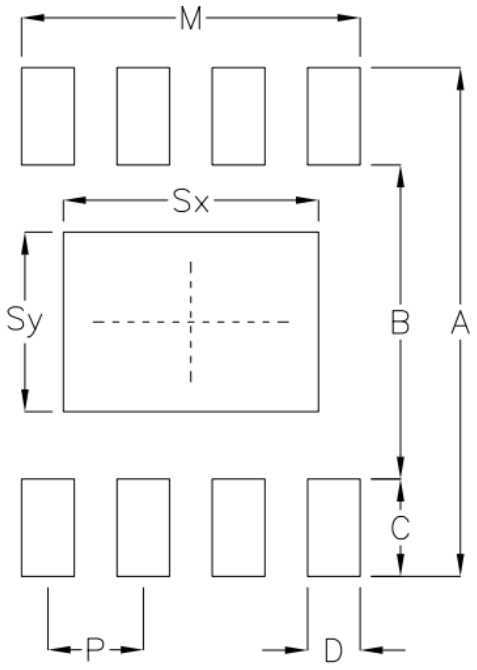


Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 10. The package of the RT7272A uses Option 2.

20 Footprint Information

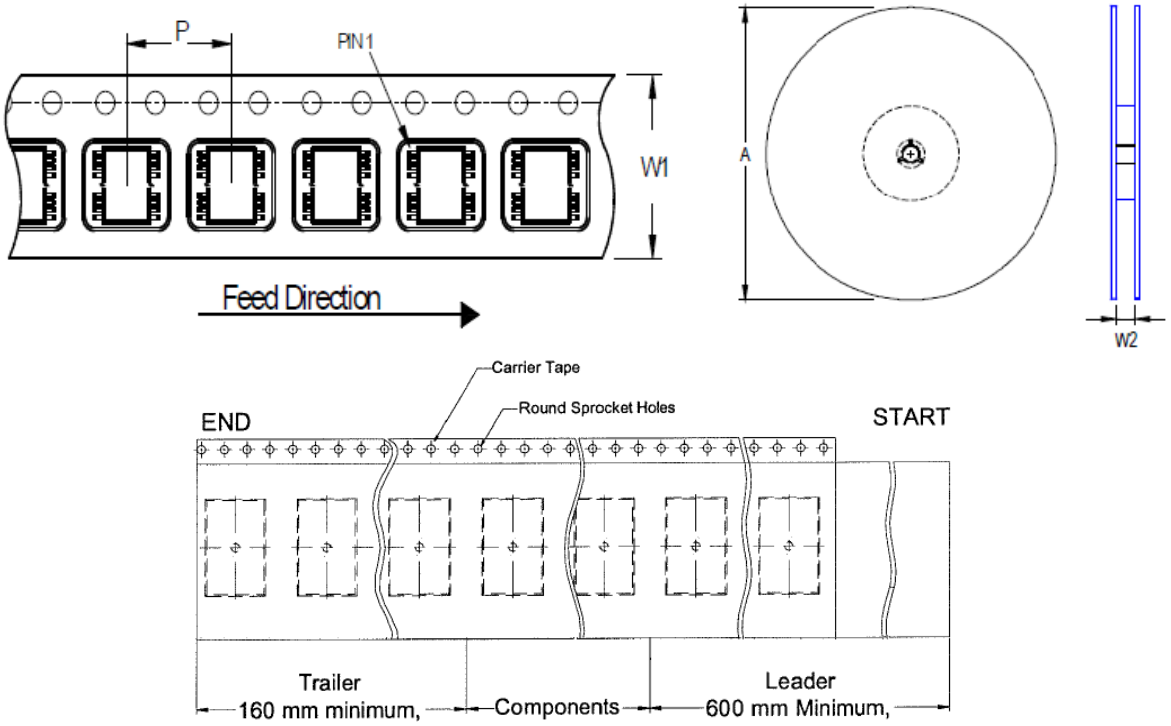


Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

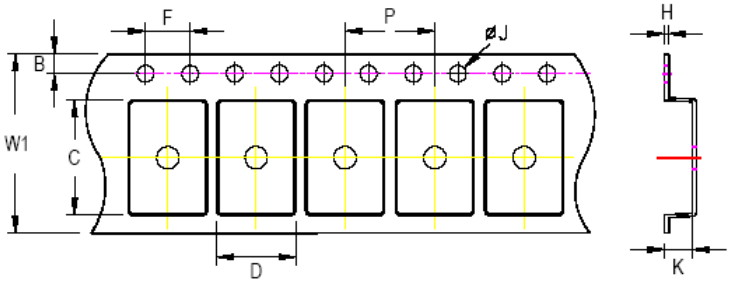
Note 11. The package of the RT7272A uses Option 2.

21 Packing Information

21.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}	10^4 to 10^{11}

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22 Datasheet Revision History

Version	Date	Description	Item
10	2024/5/20	Modify	Ordering Information on P2 Marking Information on P2 Absolute Maximum Ratings on P6 Recommended Operating Conditions on P6 Thermal Information on P6 Electrical Characteristics on P7 Operation on P11 Application Information on P17 Footprint Information on P19 Packing Information on P20, 21, 22