RICHTEK®

RT7257G

18V, 3A, 800kHz Synchronous Buck Converter

1 General Description

The RT7257G is a 18V, 3A, 800kHz, high-efficiency, synchronous buck DC-DC converter with an input-voltage range of 4.5V to 18V and a programmable output-voltage range of 0.8V to 12V. It features current-mode control to simplify external compensation and to optimize transient response with a wide range of inductors and output capacitors. High efficiency can be achieved through integrated N-MOSFETs, and pulse-skipping mode at light loads. With EN pin, power-up sequence can be more flexible, and shutdown quiescent current can be reduced to (<3μA). The RT7257G features cycle-by-cycle current limit for overcurrent protection against short-circuit outputs, and user-programmable soft-start time to prevent inrush current during startup. It also includes input undervoltage lockout, output undervoltage, and over-temperature protection to provide safe and smooth operation in all operating conditions. The RT7257G is available in the SOP-8 (Exposed Pad) package. The recommended junction temperature range is −40°C to 125°C, and the ambient temperature range is −40°C to 85°C.

2 Ordering Information

RT7257G□□□

Package Type(1)
SP: SOP-8 (Exposed Pad)
(Exposed Pad-Option 2)

Lead Plating System
Z: ECO (Ecological Element with Halogen Free and Pb free)(2)

H: UVP Hiccup
L: UVP Latch-Off

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Suitable for use in SnPb or Pb-free soldering processes.

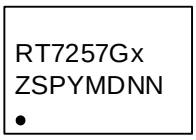
3 Features

- **±1.5% High Accuracy Reference Voltage**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **Integrated N-MOSFET Switches**
- **Current Mode Control**
- **Fixed Frequency Operation: 800kHz**
- **Output Adjustable from 0.8V to 12V**
- **Up to 95% Efficiency**
- **Programmable Soft-Start**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Current Limit**
- **Input Undervoltage Lockout**
- **Output Undervoltage Protection**
- **Over-temperature Protection**

4 Applications

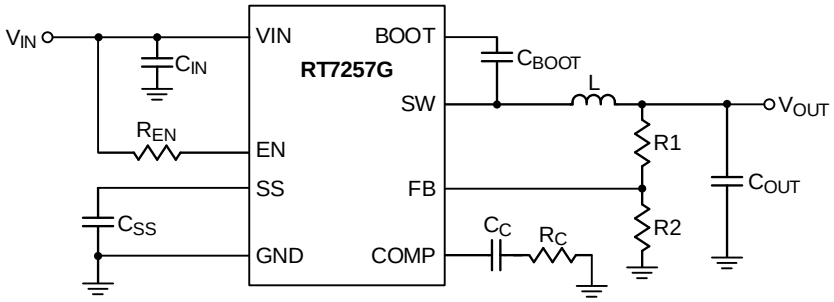
- Wireless AP/Rout
- Set-Top-Box
- Industrial and Commercial Low Power Systems
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation of High-Performance DSPs

5 Marking Information



RT7257GxZSP : Product Number
X : H or L
YMDNN : Date Code

6 Simplified Application Circuit



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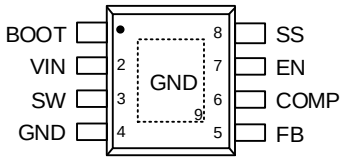
7 Pin Configuration

(TOP VIEW)

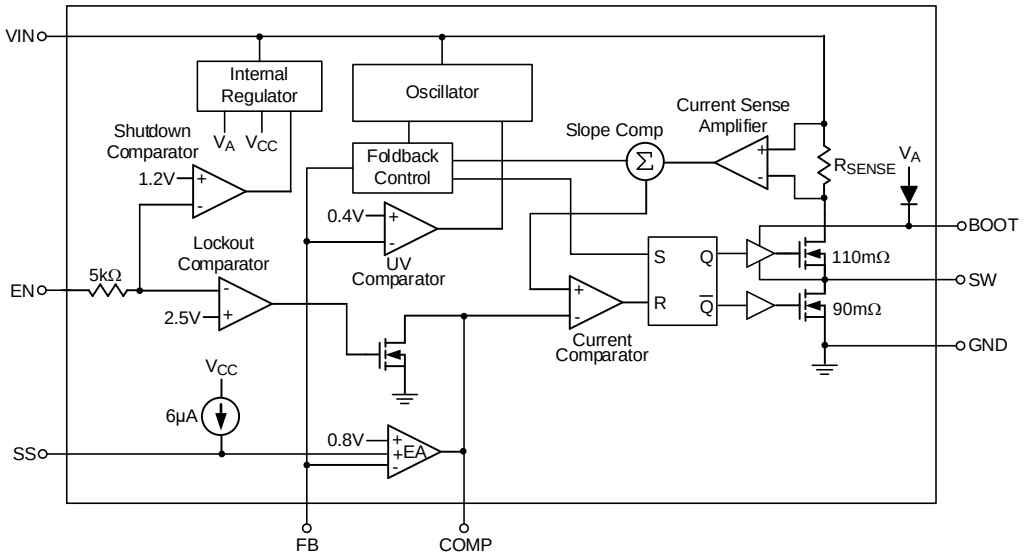


SOP-8 (Exposed Pad)

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap, supply for high-side gate driver. Connect a 0.1μF ceramic capacitor between BOOT and SW pins.
2	VIN	Input voltage. Support 4.5V to 18V input voltage. Place input capacitors next to the IC, as close to the VIN and GND pins as possible.
3	SW	Switch node. Connect to the power inductor. Return path for the internal high-side MOSFET gate driver bootstrap capacitor. Connect a capacitor from BOOT to this pin.
4, 9 (Exposed Pad)	GND	Ground return for the power stage. Use wide PCB traces to make the connections.
5	FB	Feedback Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider.
6	COMP	Compensation node for the compensation of the regulation control loop. Connect a series RC network from COMP to GND. In some cases, another capacitor from COMP to GND may be required.
7	EN	Enable control input. A logic high enables the converter; a logic low forces the converter into shutdown mode reducing the supply current to less than 3μA. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-start time control pin. Connect a capacitor between the SS pin and GND to set the soft-start time. A 0.1μF capacitor sets the soft-start period to 13.5ms.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN ---------- −0.3V to 20V
- Switch Voltage, SW ---------- −0.3V to (VIN + 0.3V)
- V_{BOOT} − V_{SW} ---------- −0.3V to 6V
- Other Pins Voltage ---------- −0.3V to 20V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 3)

  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W

  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.)- ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- −65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V	--	0.5	3	μA
Supply Current	I_Q	V_{EN} = 3V, V_{FB} = 0.9V	--	0.8	1.2	mA
Reference Voltage	V_{REF}	4.5V ≤ V_{IN} ≤ 18V	0.788	0.8	0.812	V
Error Amplifier Transconductance	G_{EA}	ΔIC = ±10μA	--	940	--	μA/V
High Side Switch On-Resistance	$R_{DS(ON)1}$		--	110	--	mΩ
Low Side Switch On-Resistance	$R_{DS(ON)2}$		--	90	--	mΩ
High Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V	--	0	10	μA
Upper Switch Current Limit	I_{LIM_H}	Min. Duty Cycle, V_{BOOT} – V_{SW} = 4.8V	--	5.1	--	A
COMP to Current Sense Transconductance	G_{CS}		--	5.1	--	A/V
Oscillation Frequency	f_{OSC1}		--	800	--	kHz
Short Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V	--	270	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	--	84	--	%
Minimum On-Time	t_{ON}		--	100	--	ns
EN Input Voltage Rising Threshold	V_{EN_R}		2.7	--	18	V
EN Input Voltage Falling Threshold	V_{EN_F}		--	--	0.4	V
Input Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	3.8	4.2	4.5	V
Input Undervoltage Lockout Hysteresis	ΔV_{UVLO}		--	320	--	mV
Soft-Start Current	I_{SS}	V_{SS} = 0V	--	6	--	μA
Soft-Start Period	t_{SS}	C_{SS} = 0.1μF	--	13.5	--	ms
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C

13 Typical Application Circuit

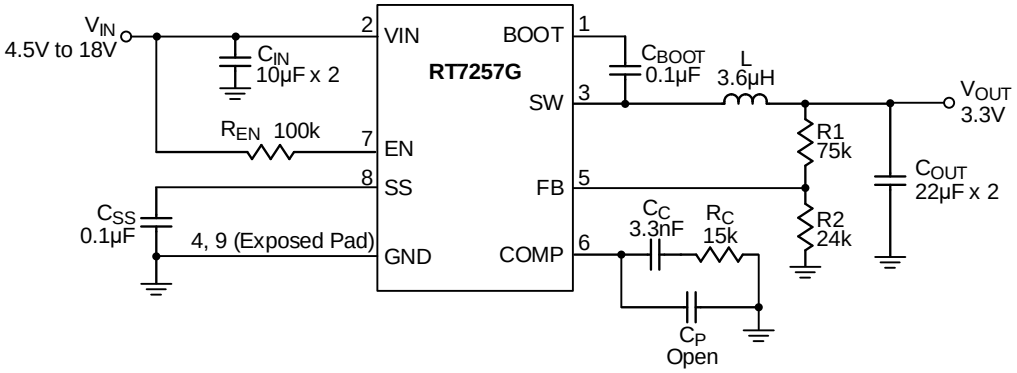
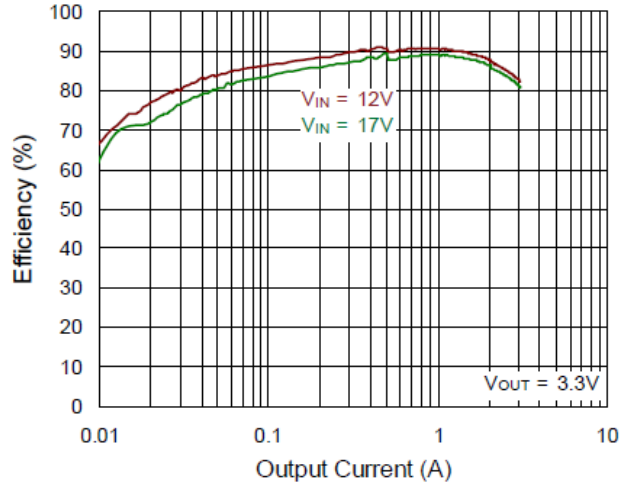


Table 1. Suggested Component Selection

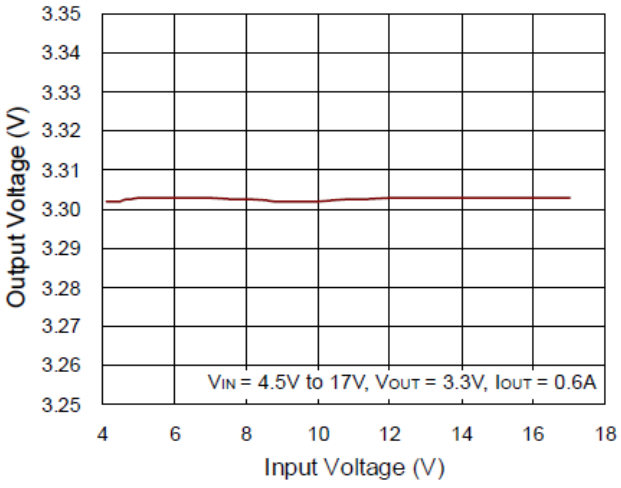
VOUT (V)	R1 (kΩ)	R2 (kΩ)	RC (kΩ)	CC (nF)	L (µH)	COUT (µF)
8	27	3	35	3.3	10	22 x 2
5	62	11.8	20	3.3	6.8	22 x 2
3.3	75	24	15	3.3	3.6	22 x 2
2.5	25.5	12	10	3.3	3.3	22 x 2
1.8	15	12	7	3.3	2.2	22 x 2
1.2	12	24	5	3.3	1.5	22 x 2
1	3	12	4	3.3	1.5	22 x 2

14 Typical Operating Characteristics

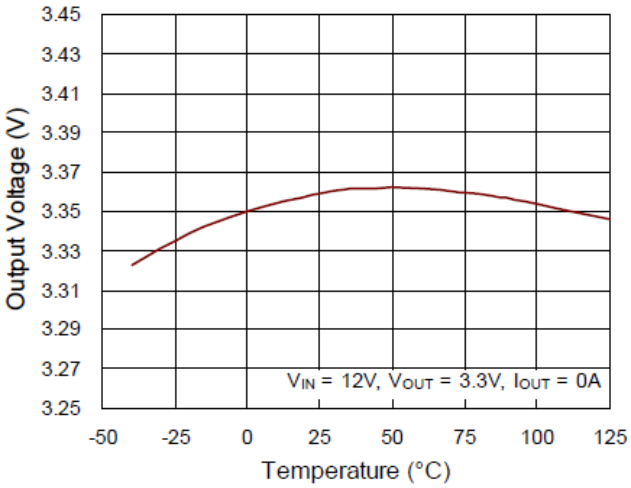
Efficiency vs. Output Current



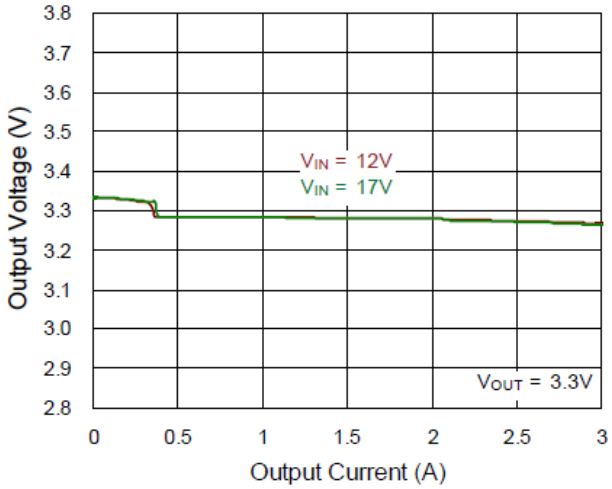
Output Voltage vs. Input Voltage



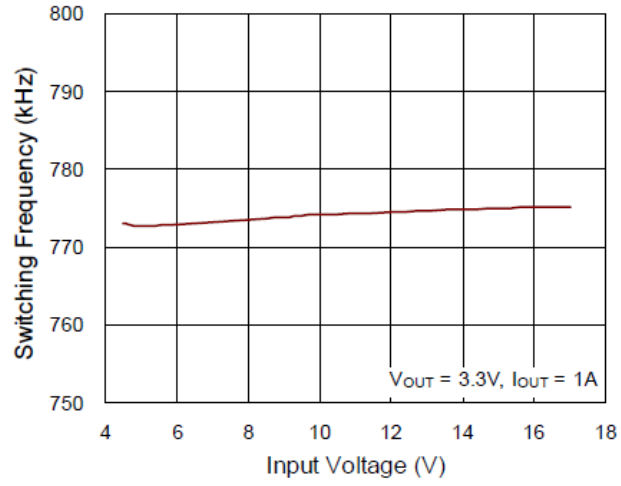
Output Voltage vs. Temperature



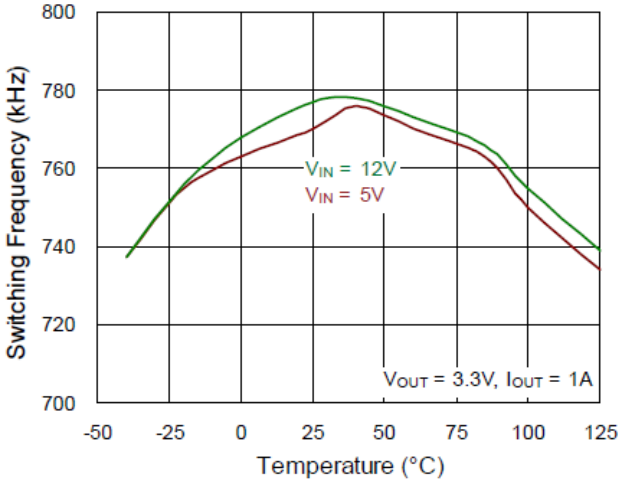
Output Voltage vs. Output Current



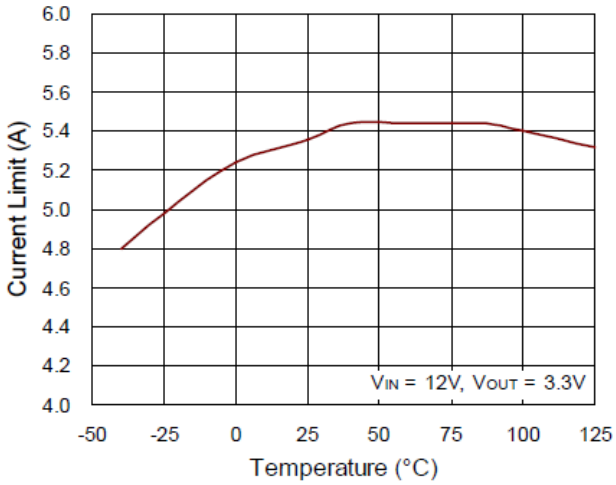
Switching Frequency vs. Input Voltage



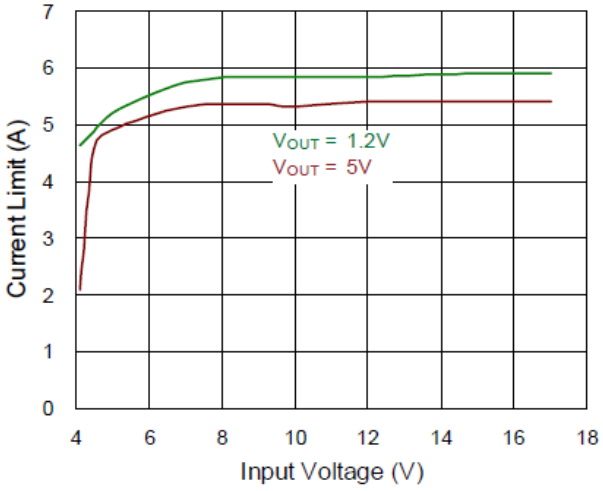
Switching Frequency vs. Temperature



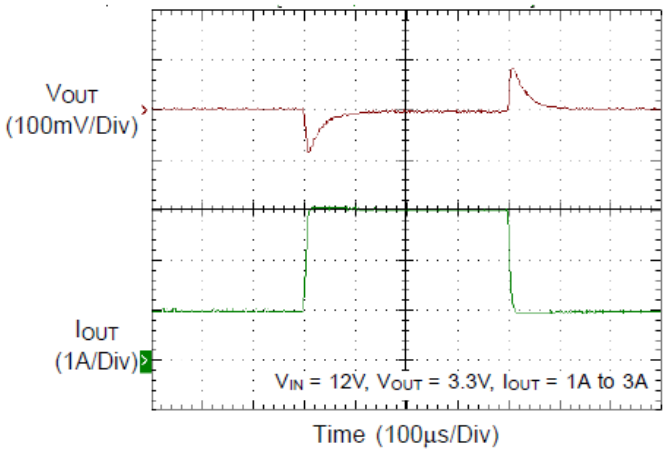
Current Limit vs. Temperature



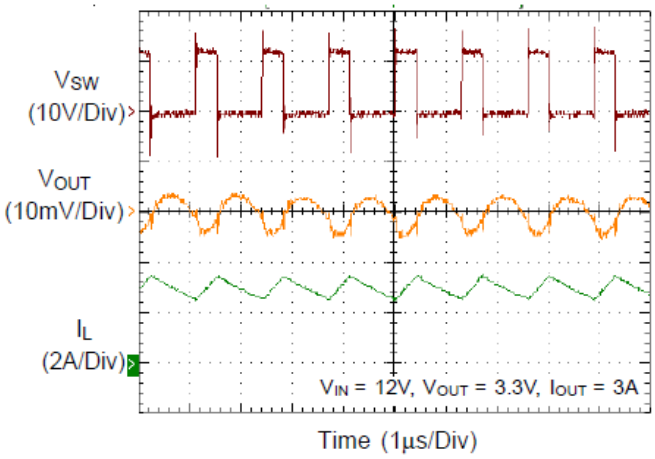
Current Limit vs. Input Voltage



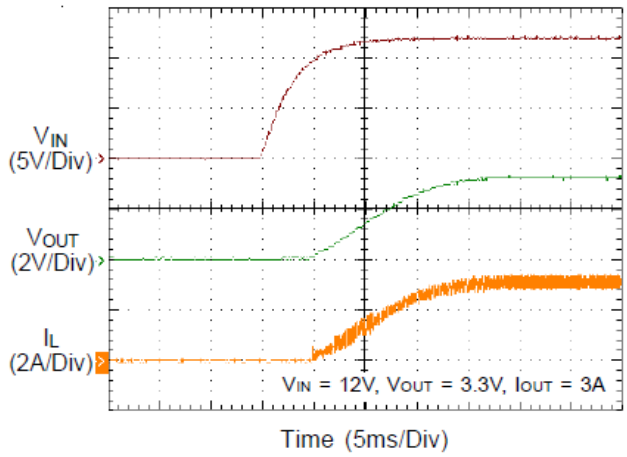
Load Transient Response



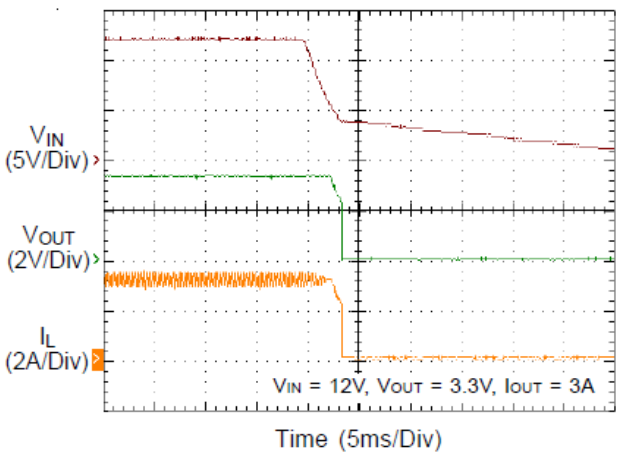
Output Ripple Voltage



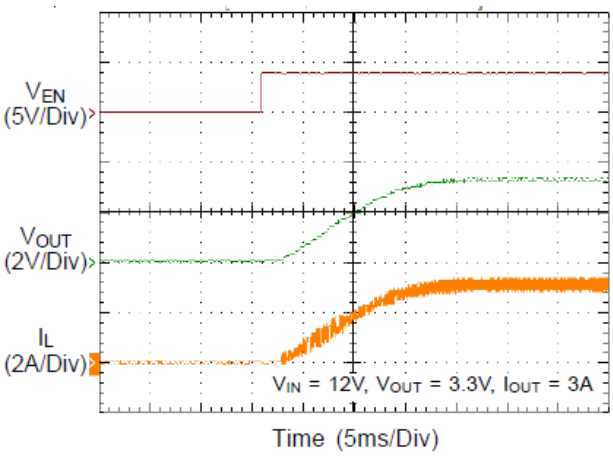
Power On from VIN



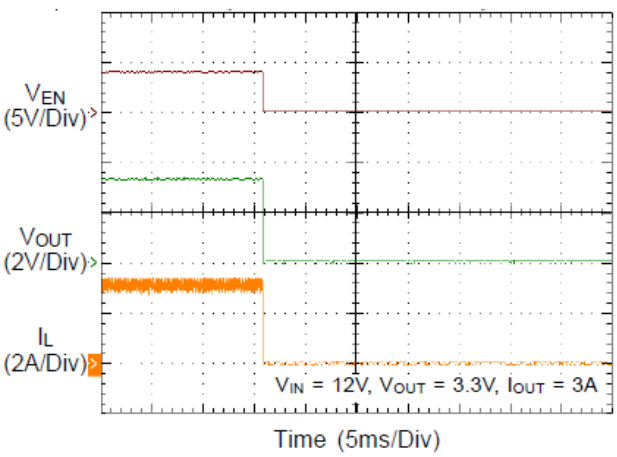
Power Off from VIN



Power On from EN



Power Off from EN



15 Operation

15.1 Control Loop

The RT7257G is a synchronous buck converter, integrating both high-side (HS) and low-side (LS) MOSFETs to reduce the number of external components. It is also equipped with a gate driver featuring dead-time control logic to prevent shoot-through conditions. The RT7257G employs constant frequency peak current mode control and includes slope compensation to ensure stability across all conversion cycles. During operation, the output voltage signal is divided by a voltage divider and sensed from the FB pin, then compared with the internal 0.8V reference voltage V_{REF}. In normal operation, when the rising edge of the internal oscillator output sets the S-R latch as the PWM clock, the high-side N-MOSFET is turned on. It is turned off when the S-R latch is reset by the output of the high-side current comparator, which compares the high-side sensed current signal with the current signal related to the COMP voltage. When the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on. If the output voltage is not established, the high-side power switch will be turned on again, starting another cycle.

15.2 Enable Control

The RT7257G provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{IL_EN}) of the enable input, the converter will enter shutdown mode; that is, the converter is disabled, and switching is inhibited even if the V_{IN} voltage is above input undervoltage lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (3μA) or below. If the EN voltage rises above the logic-high threshold voltage (V_{IH_EN}) while the V_{IN} voltage is higher than UVLO threshold, the device will be turned on (switching being enabled and soft-start sequence being initiated).

15.3 Soft-Start

The soft-start function prevents large inrush currents while the converter is being powered up. The RT7257G provides an SS pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor C_{SS} connected from the SS pin to GND. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically, 6μA) to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. If the output is for some reasons pre-biased to a certain voltage during start-up, the device will initially disable the switching of both high-side and low-side switches. And only when this ramp voltage is greater than the feedback voltage V_{FB}, the switching will be resumed. The output voltage can then ramp up smoothly to its target regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected and should not be linked to an external voltage source. The soft-start duration is determined by the RC time constant. The typical external soft-start time can be calculated by the equation below.

$$t_{SS}(ms) = \frac{V_{REF}(V) \times C_{SS}(nF)}{I_{SS}(\mu A)}$$

Where I_{SS} = 6μA, V_{REF} = 0.8V

15.4 Diode Emulation Mode

In diode emulation mode, the RT7257G automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the

inductor free-wheeling current becomes negative. As the load current is further decreased, it takes longer and longer time to discharge the output capacitor to the level that requires the next “ON” cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 1. and can be calculated as follows:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

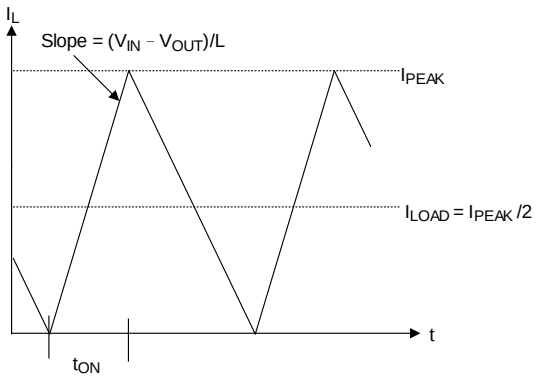


Figure 1. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light load causes diode emulation operation. This is normal and results in high efficiency. Trade-offs in DEM noise vs. light load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels). At boundary condition of discontinuous switching and continuous, the on-time is immediately increased to add “hysteresis” to discourage the IC from discontinuous switching back to continuous switching unless the load increases substantially. The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for designed switching frequency and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

15.5 High-Side Switch Peak Current-Limit Protection

The RT7257G also includes a cycle-by-cycle peak-type current-limit protection against the condition that the inductor current increases abnormally, even over the inductor saturation current rating. The inductor current through the high-side switch will only be measured after a certain amount of delay when the high-side switch is turned on. If an overcurrent condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current from exceeding the high-side switch peak-current limit (I_{LIM_H}).

15.6 Output Undervoltage Protection

The RT7257G includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 0.4V), the UV comparator output will go high to turn off both the internal high-side and low-side MOSFET switches.

15.7 Hiccup Mode

If the output undervoltage condition lasts for a period of time, the RT7257G will enter output undervoltage protection with hiccup mode. During hiccup mode, the device remains shut down. After a period of time, a soft-start sequence for auto-recovery will be initiated. Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then to resume normal operation as soon as the over-load or short-circuit condition is removed.

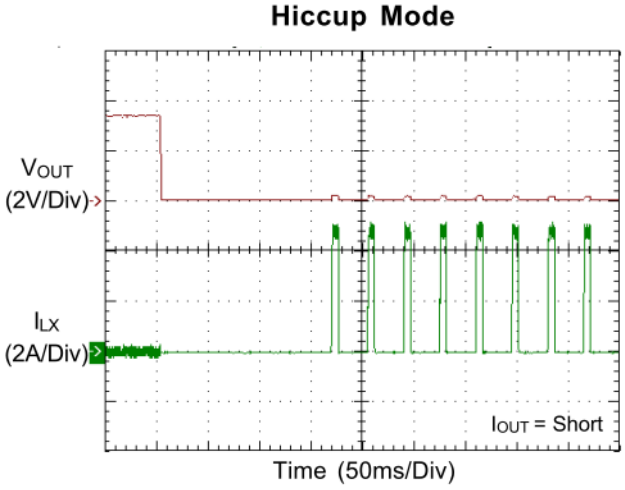


Figure 2. Hiccup Mode Undervoltage Protection

15.8 Latch-Off Mode

For the RT7257GL, it provides Latch-Off Mode Undervoltage Protection (UVP). When the FB voltage V_{FB} drops below the undervoltage protection trip threshold (typically 0.4V), UVP will be triggered and the RT7257GL will shut down in Latch-Off Mode. In shutdown condition, RT7257GL can only be reset by the EN pin or the power input VIN.

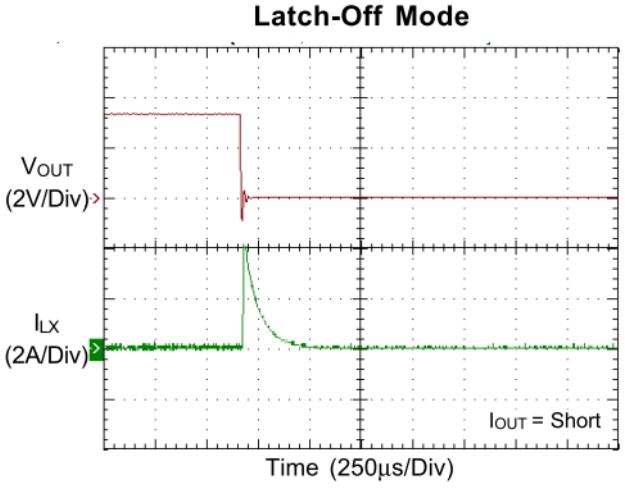


Figure 3. Latch-Off Mode Undervoltage Protection

15.9 Over-Temperature Protection

The RT7257G includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds a thermal shutdown threshold 150°C. Once the junction temperature cools down by a thermal shutdown hysteresis 20°C, the IC will resume normal operation with a complete soft-start.

16 Application Information

(Note 6)

16.1 Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 4.

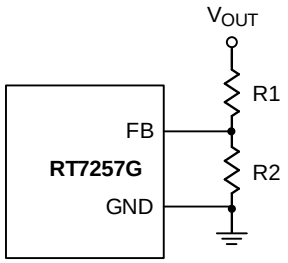


Figure 4. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where VREF is the reference voltage (0.8V typically).

16.2 External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high-side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65%. The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7257G. Note that the external boot voltage must be lower than 5.5V

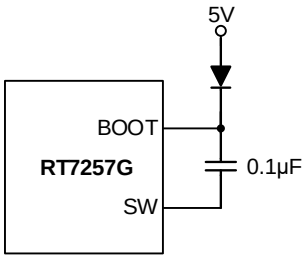


Figure 5. External Bootstrap Diode

16.3 Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT7257G quiescent current drops to lower than 3μA. Driving the EN pin high (>2.5V, <18V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and CEN capacitor from the VIN pin (see Figure 6).

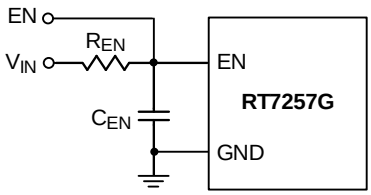


Figure 6. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 7. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

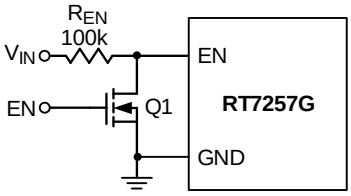


Figure 7. Digital Enable Control Circuit

16.4 Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher VIN and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

16.5 CIN and COUT Selection

The input capacitance, CIN, is needed to filter the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current is given:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10μF low ESR ceramic capacitors are suggested. For the suggested capacitor, please refer to Table 3 for more details. The selection of COUT is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for COUT selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔVOUT, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

16.6 Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$P_{D(MAX)}$ = (125°C − 25°C) / (75°C/W) = 1.333W (min.copper area PCB layout)

$P_{D(MAX)}$ = (125°C − 25°C) / (49°C/W) = 2.04W (70mm^{2}copper area PCB layout)

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it is useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 9, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 9. a), θ_{JA} is 75°C/W.

Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 9. b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 9. e) reduces the θ_{JA} to 49°C/W.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

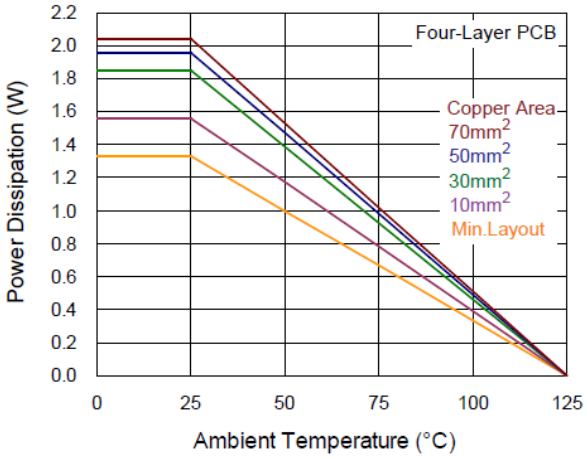
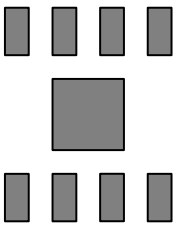
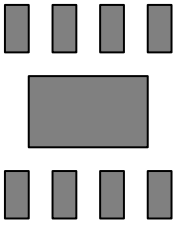


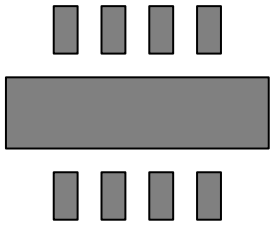
Figure 8. Derating Curve of Maximum Power Dissipation



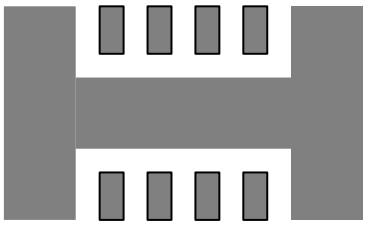
(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} = 75°C/W



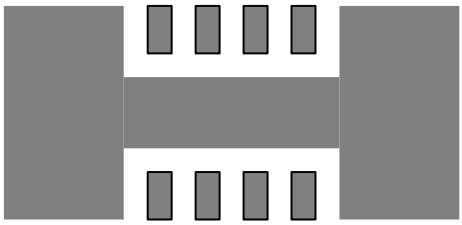
(b) Copper Area = 10mm^2, θ_{JA} = 64°C/W



(c) Copper Area = 30mm^2, θ_{JA} = 54°C/W



(d) Copper Area = 50mm^2, θ_{JA} = 51°C/W



(e) Copper Area = 70mm^2, θ_{JA} = 49°C/W

Figure 9. Thermal Resistance vs. Copper Area Layout Design

16.7 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT7257G.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT7257G.
- An example of PCB layout guide is shown in Figure 10 for reference.

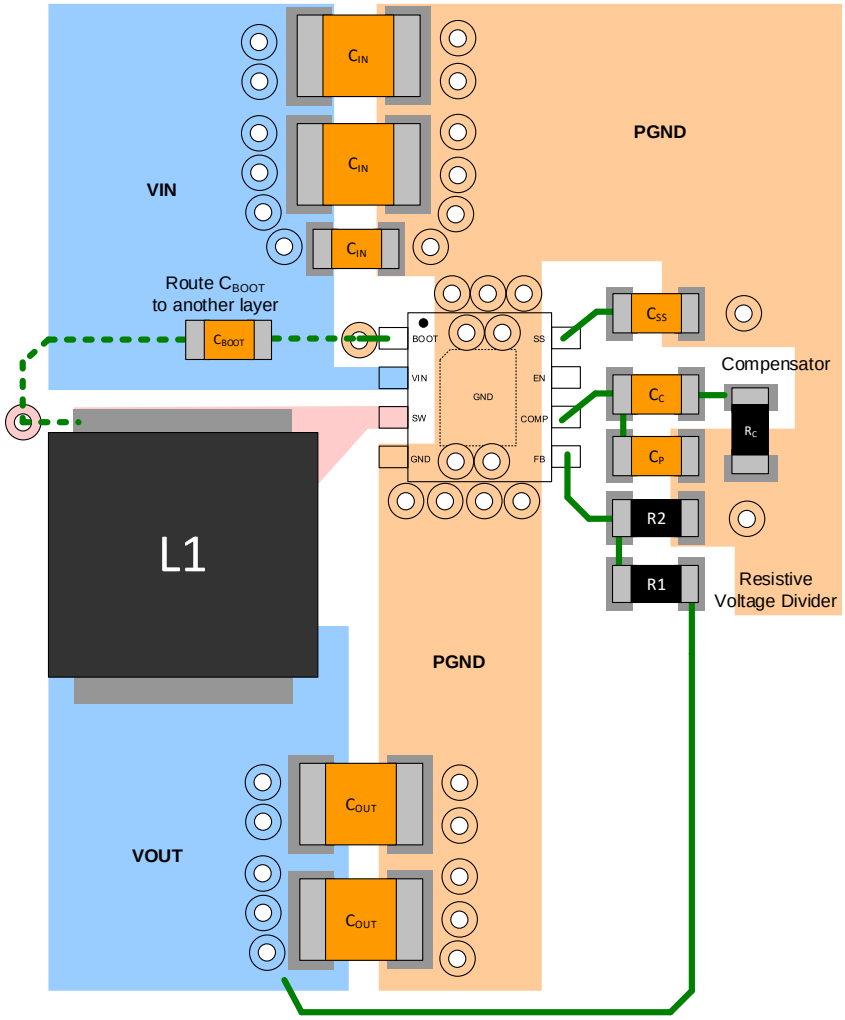


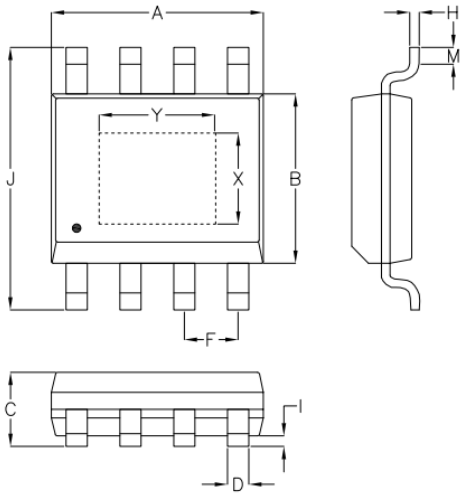
Figure 10. PCB Layout Guide

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (μF)	Case Size
CIN	MURATA	GRM31CR61E106K	10	1206
CIN	TDK	C3225X5R1E106K	10	1206
CIN	TAIYO YUDEN	TMK316BJ106ML	10	1206
COUT	MURATA	GRM31CR60J476M	47	1206
COUT	TDK	C3225X5R0J476M	47	1210
COUT	MURATA	GRM32ER71C226M	22	1210
COUT	TDK	C3225X5R1C22M	22	1210

Note 6. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension

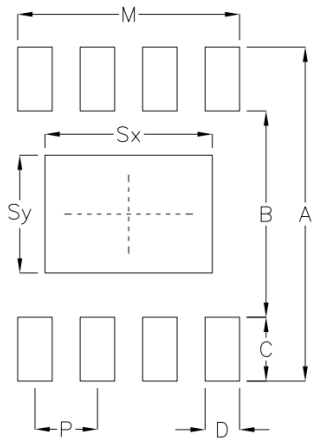


Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 7. The package of the RT7257G uses Option 2.

18 Footprint Information

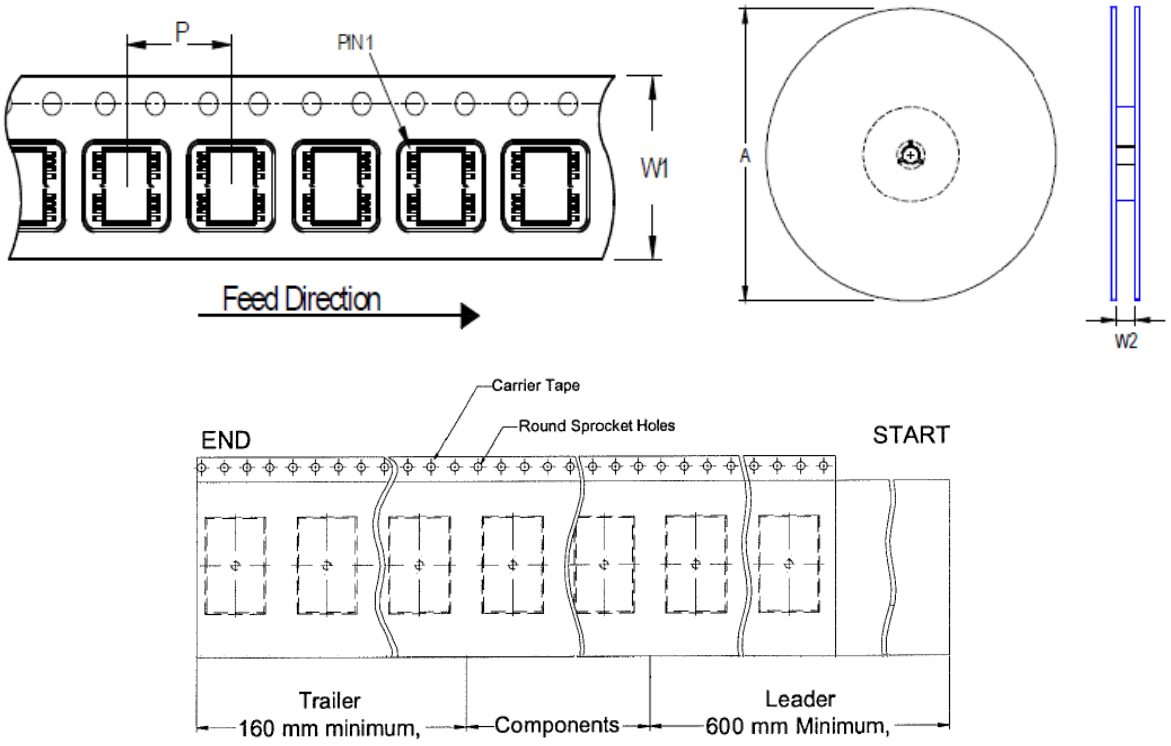


Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
PSOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

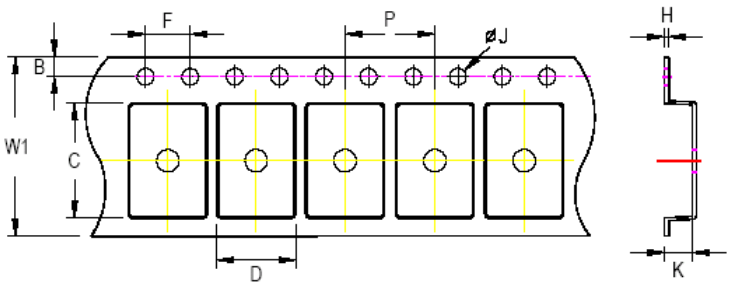
Note 8. The package of the RT7257G uses Option 2.

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
PSOP-8	12	8	330	13	2,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
PSOP-8	13”	2,500	Box G	1	2,500	Carton A	6	15,000

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
04	2024/12/3	Modify	*General Description on page 1* *Ordering Information on page 1* *Functional Pin Description on page 4* *Electrical Characteristics on page 6* *Operation on page 11 to 14* *Application Information on page 15 to 20* *Footprint Information on page 22* - Added Footprint Information *Packing Information on page 23 to 25* - Added packing information