# Synchronous Rectifier Controller with Zero Voltage Switching for Wide Output Voltage Operating Range

## 1 General Description

The RT7220D is a Synchronous Rectifier (SR) controller for Flyback converters operating in Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM) and Quasi-Resonant (QR) mode. The RT7220D will sense the drain voltage of MOSFET to determine SR gate on/off so as to minimize turn-off dead-time and enhance efficiency.

The RT7220D supports the wide output voltage range from 3V to 21V, and a HV LDO is especially built-in for the MOSFET gate driver at low output voltage. When it works with the primary-side controller RT7757, the Zero-Voltage-Switching (ZVS) control can be enabled to optimize the efficiency at high line.

Furthermore, the RT7220D provides a green mode operation in light load condition, which reduces operation current to be under 250μA.

The recommended junction temperature range is −40°C to 125°C, and the ambient temperature range is −40°C to 105°C.

## 2 Ordering Information

RT7220D □-□□□□

**Packing**
A: Standard

**Trim Code**
(Refer to Version Table)

**Package Type**(1)
N: WQFN-16L 3x3

**Note 1**.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

## 3 Features

- **Suitable for Flyback Converter in CCM, DCM, and Quasi-Resonant (QR) Mode**
- **Suitable for 3V to 21V $V_{OUT}$ Range**
- **ZVS Function to Optimize Efficiency (Work with the Primary-Side Controller RT7757)**
- **<1.65mA Operating Current in ZVS Mode**
- **<250μA Operating Current in Green Mode**
- **Built-In HV LDO to Supply SR Driver when $V_{OUT}$ is Lower than 5V**
- **Automatic Dead-Time Tracking Control to Optimize Efficiency**
- **Protection**
  - **SR Gate Driver with 6V Clamp**
  - **SR Gate Initial Pull-Low before Start-Up**
  - **SR Minimum Off-Time**
  - **Fast Turn-Off (<50ns) Gate Driver**

## 4 Applications

- USB PD Power Converters
- Fast-Charger Power Adapters
- General Purpose High-Efficiency and/or Compact-Size Flyback Power Converters

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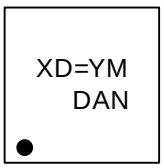
# 5 Marking Information

RT7220DN-HQA




XD=: Product Code
YMDAN: Date Code

RT7220DN-LPA

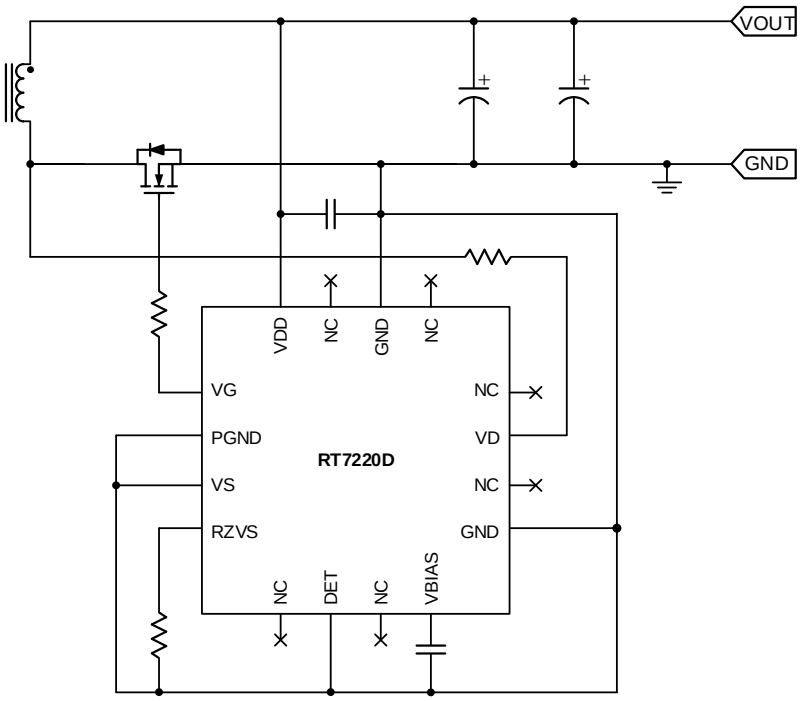

XE=: Product Code
YMDAN: Date Code

RT7220DN-LMA


XF=: Product Code
YMDAN: Date Code

# 6 Simplified Application Circuit

## 6.1 Simplified Circuit for Low-Side Application

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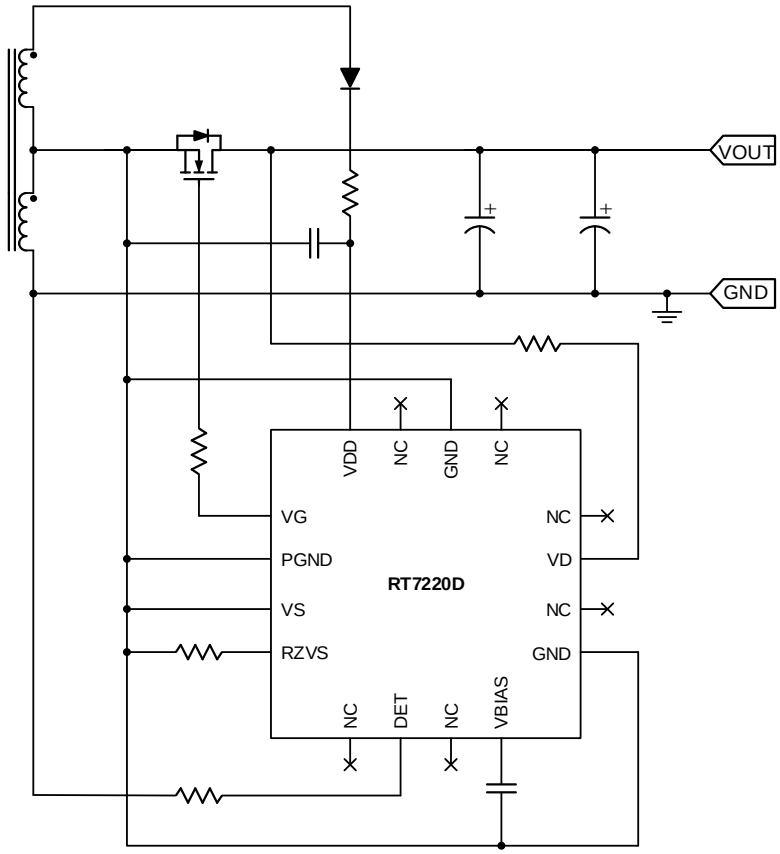
## 6.2 Simplified Circuit for High-Side Application

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## 7 RT7220D Version Table

| Version | RT7220DN-HQA (RT7220DHQGQW) | RT7220DN-LPA (RT7220DLPGQW) | RT7220DN-LMA |
|---|---|---|---|
| High/Low-Side Application | High-Side | Low-Side | Low-Side |
| VD Voltage Supported | 180V | 180V | 180V |
| Output Voltage Supported | 3V to 21V | 3V to 21V | 3V to 21V |
| Maximum Operation Frequency | 160kHz | 160kHz | 160kHz |
| HV LDO | 180V/65mA | 180V/65mA | 180V/65mA |
| ZVS Function | Enable | Enable | Enable |
| $V_{OUT}$ Range of Maximum Power Supported | 18V to 21V | 9V to 21V | 18V to 21V |
| Frequency Jitter Range of ZVS Mode | ±12% | ±12% | ±12% |
| Internal $R_{ZVS}$ (When the RZVS pin is short-circuited) | 360kΩ | 360kΩ | 480kΩ |
| DET Pin Connection | 300kΩ to System GND | Short to IC GND | Short to IC GND |
| Cooperated Primary-Side Controller (Note 2) | RT7757D-GEQA (RT7757GEQ) | RT7757D-GEPA (RT7757GEP) | RT7757D-AEMA |

**Note 2**. The last two characters in the part numbers of both the RT7220D and the RT7757 must be the same. Otherwise, the ZVS function will not operate normally. (For example, RT7757D-AE"MA" ↔ RT7220DN-L"MA").

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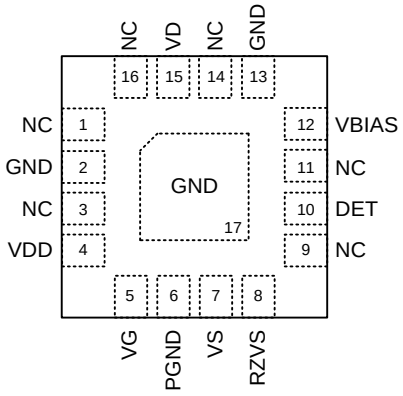
## 8 Pin Configuration

(TOP VIEW)




WQFN-16L 3x3

## 9 Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1, 3, 9, 11, 14, 16 | NC | No internal connection. |
| 2, 13, 17 (Exposed Pad) | GND | Ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation. |
| 4 | VDD | Supply voltage. |
| 5 | VG | Gate driver output for the SR MOSFET. |
| 6 | PGND | Ground of gate driver. |
| 7 | VS | Source voltage sensing node for the SR MOSFET. |
| 8 | RZVS | ZVS on-time setting. |
| 10 | DET | Output voltage detection for high-side SR MOSFET. |
| 12 | VBIAS | Regulated DC bias. |
| 15 | VD | Drain voltage sense node for the SR MOSFET. |

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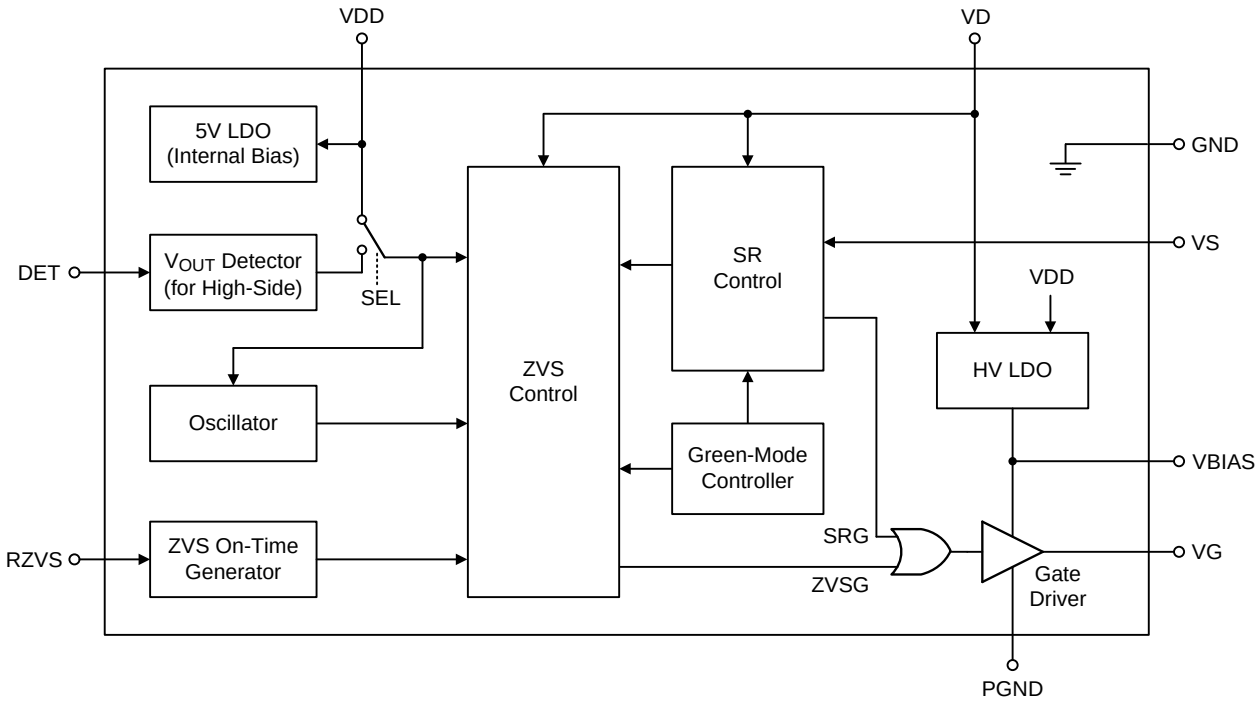
## 10 Functional Block Diagram

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## 11 Absolute Maximum Ratings

(Note 3)

- VD to GND ---------- –1V (pulse width 500ns) to 180V
- VDD to GND ---------- –0.3V to 40V
- VBIAS to GND ---------- –0.3V to 6.5V
- VG to GND ---------- –0.3V to $V_{BIAS}$ + 0.3V
- RZVS to GND ---------- –0.3V to 6.5V
- DET to GND ---------- –1V to 6.5V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C

  WQFN-16L 3x3---------- 2.35W
- Package Thermal Resistance (Note 4)

  WQFN-16L 3x3, $\theta_{JA}$ ---------- 42.5°C/W

  WQFN-16L 3x3, $\theta_{JC}$ ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.)---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---------- 2kV

**Note 3**. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 4**. $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard. $\theta_{JC}$ is measured at the bottom of the package.

**Note 5**. Devices are ESD sensitive. Handling precautions are recommended.

## 12 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage, VD ---------- –1V (pulse width 500ns) to 150V
- Supply Input Voltage, VDD---------- 3V to 36V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 105°C

**Note 6**. The device is not guaranteed to function outside its operating conditions.

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## 13 Electrical Characteristics

($T_A$ = 25°C, unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VDD Section** | | | | | | |
| VDD Turn-On Threshold Voltage | $V_{VDD\_ON}$ | | 3.1 | 3.25 | 3.4 | V |
| VDD Turn-Off Threshold Voltage | $V_{VDD\_OFF}$ | | 2.6 | 2.75 | 2.9 | V |
| Hysteresis Voltage for VDD Turn-On/VDD Turn-Off Threshold | $V_{VDD\_HYST}$ | | 0.4 | 0.5 | 0.6 | V |
| VDD Start-Up Current | $I_{DD\_START}$ | $V_{DD}$ = $V_{VDD\_ON}$ - 1V | -- | -- | 150 | μA |
| VDD Operating Current | $I_{DD\_OP}$ | $V_{DD}$ = 5V, the VG pin is open, only enable SR function. | -- | 1.2 | 1.5 | mA |
| VDD Operating Current | $I_{DD\_OP\_ZVS}$ | $V_{DD}$ = 5V, the VG pin is open, enable SR and ZVS function. | -- | 1.35 | 1.65 | mA |
| VDD Green-Mode Current | $I_{DD\_GREEN}$ | In green mode. $V_{DD}$ = 5V | -- | 200 | 250 | μA |
| **VBIAS Section** | | | | | | |
| VBIAS Output Voltage | $V_{BIAS}$ | $I_{LOAD}$ = 15mA, $V_{DD}$ > 6V | 5.5 | 6 | 6.5 | V |
| | | $I_{LOAD}$ = 5mA, 4.7V < $V_{DD}$ < 6V | $V_{DD}$ - 0.15 | -- | $V_{DD}$ | |
| | | $I_{LOAD}$ = 5mA, $V_{DD}$ < 4.7V, 9V < VD < 150V, VD duty > 20% at 200kHz. The power path for the SR driver is from the VD and cycle-by-cycle to detect VDD to change power source. | 4.5 | 4.7 | 4.9 | |
| VBIAS Load Regulation | | 1mA < $I_{VBIAS}$ < 15mA (Continuance) (Note 7) | -- | -- | 200 | mV |
| VBIAS Output Short Circuit Current | $I_{VBIAS\_SC}$ | | 50 | 65 | 80 | mA |
| **SR Driver Section** | | | | | | |
| Output High Voltage | $V_{OH\_VG}$ | $I_{LOAD}$ = 20mA | $V_{BIAS}$ - 0.3 | -- | $V_{BIAS}$ | V |
| Output Low Voltage | $V_{OL\_VG}$ | | -- | -- | 0.5 | V |
| Rise Time | $t_{R\_VG}$ | $C_L$ = 4nF, $V_G$ is from 1V to 4V | -- | 50 | 100 | ns |
| Turn-On Propagation Time | $t_{P\_ON}$ | From trigger VD falling edge to $V_G$ = 0.1V. | -- | -- | 80 | ns |
| Fall Time | $t_{F\_VG}$ | $C_L$ = 4nF, from 80% x $V_{OH\_VG}$ to 1V | -- | -- | 15 | ns |
| Turn-Off Propagation Time | $t_{P\_OFF}$ | | -- | -- | 30 | ns |
| Initial Output Low Clamping Voltage before Start-up | $V_{OL\_VG\_INI}$ | $C_{GD}$ = 330pF, $C_{GS}$ = 27pF, VD is from 0V to 40V, $t_R$ = 50ns, pulse width = 1μs. (Note 7) | -- | -- | 1.5 | V |
| Internal Pull-Low Resistor | $R_{GS\_LOW}$ | | 70 | 100 | 130 | kΩ |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VD Section** | | | | | | |
| $V_{DS}$ Scaling Ratio I | $K_{VDS\_I}$ | For SR function (Note 7) | -- | 2 | -- | % |
| $V_{DS}$ Scaling Ratio II | $K_{VDS\_II}$ | For ZVS function (Note 7) | -- | 15 | -- | |
| VD Sample and Hold Error | $E_{SH\_VD}$ | ($\lvert V_{VD\_HIGH} - V_{VD\_SH}\rvert / V_{VD\_SH}$) x 100 | -- | -- | ±5 | % |
| Threshold of VD Sample and Hold | $V_{VD\_SH}$ | $V_{TH\_SH} = K_{VD\_SH}$ x $V_{VD\_HIGH}[n-1]$ | -- | 0.7 | -- | -- |
| Mask Time | $t_{MASK}$ | $V_{VD} > V_{TH\_SH}$ (Note 7) | 100 | 120 | 140 | ns |
| Initial VD Blanking Time | $t_{BLANK\_VD\_INI}$ | VD blanking time is counted after $t_{MASK}$ | 0.2 | 0.3 | 0.4 | µs |
| $V_{IN}$ Low VD Blanking Time | $t_{BLANK\_VD\_VINL}$ | VD blanking time is counted after $t_{MASK}$ | 0.9 | 1.05 | 1.2 | µs |
| Low Level Threshold for Input Voltage | $K_{VIN\_LOW}$ | When $V_{DS} < K_{VIN\_LOW}$ x VDD, VD blanking time will be changed to $V_{IN}$ low blanking time and minimum off-time. | 2 | 2.2 | 2.4 | -- |
| Low Level Threshold for VD Falling Edge Detection | $V_{LOW\_FALLING}$ | | –0.4 | –0.3 | –0.2 | V |
| Dead Time Comparison High Threshold | $V_{TH\_DT}$ | | 0.4 | 0.5 | 0.6 | V |
| VG Fast Turn-Off Initial Threshold | $V_{TH\_VGOFF\_INI}$ | | –13 | –10 | –7 | mV |
| Maximum VG Fast Turn-Off Limit for Tracking Up/Down | $V_{VGOFF\_MAX}$ | With 8-bit tracking control | 17 | 20 | 23 | mV |
| VG Fast Turn-Off Step Limit for Tracking Up/Down | $\Delta V_{VGOFF}$ | $V_{TH\_VGOFF}[n] = V_{TH\_VGOFF}[n-1] \pm \Delta V_{VGOFF}$ | 0.062 | 0.078 | 0.094 | mV |
| VD Falling Time Threshold for VG Trigger | $t_{VD\_FALLING}$ | VD falling edge is from $V_{TH\_SH}$ to $V_{LOW\_FALLING}$. If VD falling time < $t_{VD\_FALLING}$ and disable VD falling edge debounce time, VG will be triggered immediately when VD < $V_{LOW\_FALLING}$. | 100 | 150 | 200 | ns |
| VD Edge Threshold for Exit Green Mode Detection | $V_{VD\_EDGE}$ | | –0.4 | –0.3 | –0.2 | V |
| Debounce Time for Exit/Enter Green Mode Detection | $t_{VD\_EDGE}$ | | 4 | 5 | 6 | ms |
| VD Cycle Number for Enter Green Mode | $N_{ENGR}$ | The number of VG pulses in $t_{VD\_EDGE}$ is less than $N_{ENGR}$. | -- | 16 | -- | -- |
| VD Cycle Number for Exit Green Mode | $N_{EXGR}$ | The number of VD pulses in $t_{VD\_EDGE}$ is greater than $N_{EXGR}$. | -- | 32 | -- | -- |
| VD Cycle Number for Fast Exit Green Mode | $N_{EXGR\_F}$ | The number of continuous VG pulses is greater than $N_{EXGR\_F}$. | -- | 8 | -- | -- |

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| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SR Control Section** | | | | | | | |
| VG Minimum On-Time | $t_{MINON\_VG}$ | From VG rising edge to VG falling edge. (Note 7) | RT7220DN-HQA, RT7220DN-LPA | 400 | 500 | 600 | ns |
| | | | RT7220DN-LMA | 800 | 1000 | 1200 | |
| Disable VG Minimum On- Time Threshold | $V_{MINON\_DIS}$ | When VD > $V_{MINON\_DIS}$ during $t_{MINON\_VG}$, VG will be disabled immediately. | | 0.4 | 0.5 | 0.6 | V |
| Initial VG Minimum Off-Time | $t_{MINOFF\_VG\_INI}$ | From VG falling edge to the next VG rising edge. | | 0.2 | 0.3 | 0.4 | µs |
| $V_{IN}$ Low VG Minimum Off-Time | $t_{MINOFF\_VG\_VINL}$ | From VG falling edge to the next VG rising edge. | | 0.9 | 1.05 | 1.2 | µs |
| VD Undervoltage Protection Threshold | $V_{VD\_UVP}$ | When $V_D$ < $V_{VD\_UVP}$, VG will be disabled. (Note 7) | | -- | -- | $V_{OUT}$ + 3.5 | V |
| **Automatic Tracking Section** | | | | | | | |
| Auto-Tracking Dead Time | $t_{DEAD\_TRACK}$ | From VG falling edge to VD = $V_{TH\_DT}$ | | 180 | 200 | 220 | ns |
| **Oscillator Section (Only for ZVS Function)** | | | | | | | |
| Maximum Frequency | $f_{OSC\_MAX}$ | $V_{CTL}$ > $V_{FR\_ET}$, Not including ZVS on-time. | | 110 | 120 | 130 | kHz |
| Minimum Frequency | $f_{OSC\_MIN}$ | $V_{CTL}$ < $V_{FR\_EX}$ | | 20 | 25 | 30 | kHz |
| Frequency Jittering Range | Δf | | | ±9 | ±12 | ±15 | % |
| Frequency Jittering Period | $t_{JIT}$ | (Note 7) | | -- | 512 | -- | cycle |
| Frequency Variation Versus Temperature Deviation | $f_{DT}$ | $T_A$ = –30°C to 105°C (Note 7) | | -- | -- | ±6 | % |
| Internal $R_{SET}$ for Frequency Reduction Mode Control Voltage Modulation | $R_{SET}$ | (Note 7) | RT7220DN-HQA | -- | 380 | -- | kΩ |
| | | | RT7220DN-LPA | -- | 240 | -- | |
| | | | RT7220DN-LMA | -- | 340 | -- | |
| $V_{OUT}$ Scaling Ratio | $K_{VO}$ | (Note 7) | | 14.5 | 15 | 15.5 | % |
| Accuracy of Frequency Reduction Mode Control Voltage | ΔVCTL | $V_{CTL}$ = ($10^{11}$ x $K_{VO}$ x $L_m$ x $I_{peak}$) / (3 x $N_{PS}$ x $R_{SET}$) | | -- | -- | ±7 | % |
| Boundary Voltage of Maximum Power | $V_{FRMOD\_MAX}$ | | RT7220DN-HQA, RT7220DN-LMA | 2.6 | 2.7 | 2.8 | V |
| | | | RT7220DN-LPA | 1.25 | 1.35 | 1.45 | |

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| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Boundary Voltage of Minimum Power | $V_{FRMOD\_MIN}$ | | RT7220DN-HQA, RT7220DN-LMA | 0.8 | 0.9 | 1 | V |
| | | | RT7220DN-LPA | 0.5 | 0.6 | 0.7 | |
| Entry Voltage of Frequency Reduction Mode | $V_{FR\_ET}$ | $K_{VO}$ x $V_{OUT}$ > $V_{FRMOD\_MAX}$ | RT7220DN-HQA, RT7220DN-LMA | 1.55 | 1.6 | 1.65 | V |
| | | $K_{VO}$ x $V_{OUT}$ < $V_{FRMOD\_MIN}$ | | 1.15 | 1.2 | 1.25 | |
| | | $K_{VO}$ x $V_{OUT}$ > $V_{FRMOD\_MAX}$ | RT7220DN-LPA | 1.4 | 1.45 | 1.5 | |
| | | $K_{VO}$ x $V_{OUT}$ < $V_{FRMOD\_MIN}$ | | 1.15 | 1.2 | 1.25 | |
| Exit Voltage of Frequency Reduction Mode | $V_{FR\_EX}$ | $K_{VO}$ x $V_{OUT}$ > $V_{FRMOD\_MAX}$ | RT7220DN-HQA, RT7220DN-LMA | 1.2 | 1.25 | 1.3 | V |
| | | $K_{VO}$ x $V_{OUT}$ < $V_{FRMOD\_MIN}$ | | 0.8 | 0.85 | 0.9 | |
| | | $K_{VO}$ x $V_{OUT}$ > $V_{FRMOD\_MAX}$ | RT7220DN-LPA | 1.05 | 1.1 | 1.15 | |
| | | $K_{VO}$ x $V_{OUT}$ < $V_{FRMOD\_MIN}$ | | 0.8 | 0.85 | 0.9 | |
| **ZVS Section** | | | | | | | |
| Maximum Count of PWM MOSFET Ringing Peak for ZVS Operation | $N_{PEAK}$ | Enable ZVS function when the number of VD valley < $N_{PEAK}$ (Note 7) | RT7220DN-HQA, RT7220DN-LPA | -- | 7 | -- | Peak |
| | | | RT7220DN-LMA | -- | 10 | -- | |
| ZVS Pulse Trigger Threshold | $V_{TH\_ZVS}$ | If VD ringing < $V_{TH\_ZVS}$, ZVS pulse will be triggered. | | 0.95 x $V_{OUT}$ | $V_{OUT}$ | 1.05 x $V_{OUT}$ | V |
| ZVS Pulse Trigger Debounce Time | $t_{D\_PEAK}$ | From VD < $V_{TH\_ZVS}$ to ZVS Pulse rising edge. | | 100 | 200 | 300 | ns |
| External $R_{ZVS}$ Range for ZVS On-Time Setting | $R_{ZVS}$ | The RZVS pin adds an external resistor, and a 1% resistor is suggested. (Note 7) | | 200 | -- | 500 | kΩ |
| Maximum ZVS On-Time | $t_{ON\_ZVS\_MAX}$ | (Note 7) | | 3.5 | 4.4 | 5.3 | μs |
| Minimum ZVS On-Time | $t_{ON\_ZVS\_MIN}$ | ZVS pulse at first peak of primary-side MOSFET $V_{DS}$ | RT7220DN-HQA, RT7220DN-LPA | 350 | 450 | 550 | ns |
| | | | RT7220DN-LMA | 700 | 900 | 1100 | |
| | | ZVS pulse at/after second peak of primary-side MOSFET $V_{DS}$ (Note 7) | | 350 | 450 | 550 | |

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| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ZVS On-Time Accuracy | $t_{ON\_ZVS}$ | $R_{ZVS}$ = 480kΩ, $V_D$ = 70V, $V_{OUT}$ = 6.5V | 2173 | 2557 | 2940 | ns |
| | | $R_{ZVS}$ = 360kΩ, $V_D$ = 70V, $V_{OUT}$ = 6.5V | 1588 | 1868 | 2148 | |
| | | $R_{ZVS}$ = 240kΩ, $V_D$ = 70V, $V_{OUT}$ = 6.5V | 901 | 1178 | 1455 | |
| | | $R_{ZVS}$ = 480kΩ, $V_D$ = 85V, $V_{OUT}$ = 15V | 957 | 1251 | 1545 | |
| | | $R_{ZVS}$ = 360kΩ, $V_D$ = 85V, $V_{OUT}$ = 10V | 1095 | 1432 | 1769 | |
| $V_{OUT}$ Threshold Voltage of Disable ZVS Operation | $V_{TH\_DISZVS}$ | If $V_{OUT}$ < $V_{TH\_DISZVS}$, ZVS function is disabled. | 3.8 | 4.3 | 4.8 | V |
| **DET Section (Only for RT7220DN-HxA)** | | | | | | |
| External $R_{DET}$ | $R_{DET}$ | 1% resistor is suggested. (Note 7) | -- | 300 | -- | kΩ |
| The DET Pin High-Level Clamping Voltage | $V_{DET\_CLAMP\_H}$ | | -- | -- | 5.5 | V |
| The DET Pin Low-Level Clamping Voltage | $V_{DET\_CLAMP\_L}$ | | –100 | 0 | 100 | mV |
| Maximum DET Sourcing Current | $I_{DET\_MAX}$ | | 100 | -- | -- | μA |

**Note 7**. Guaranteed by design.

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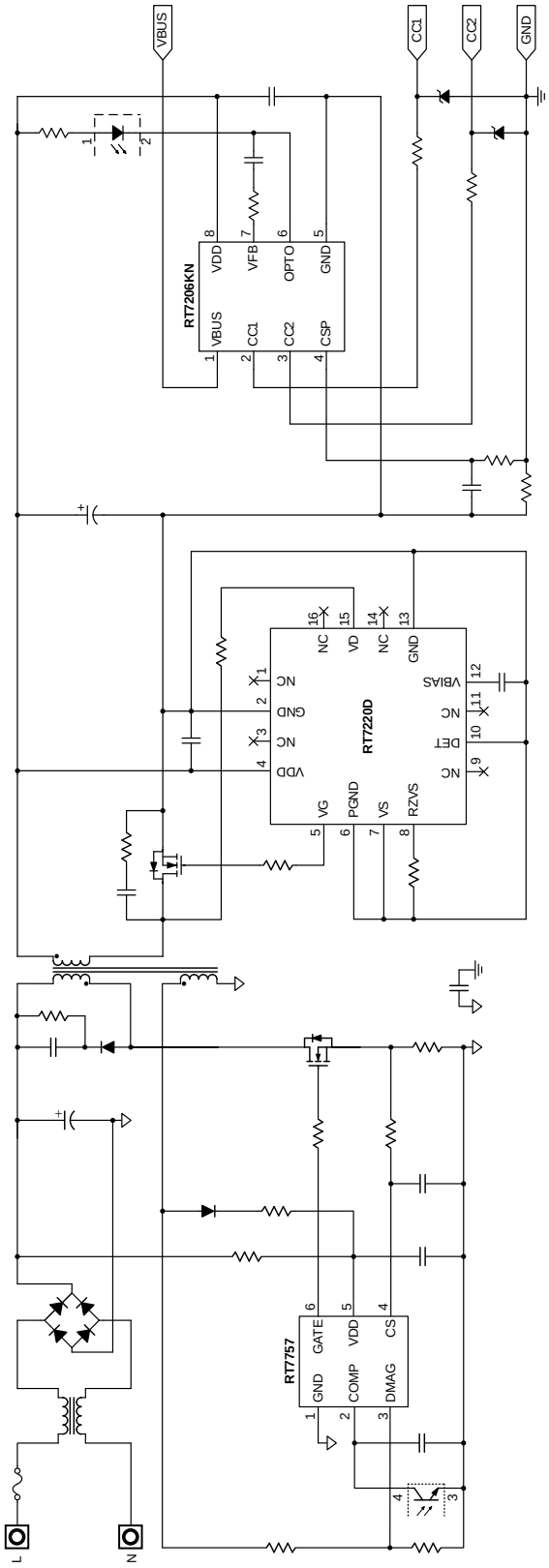
# 14 Typical Application Circuit

## 14.1 Typical Application Circuit for Low-Side Application

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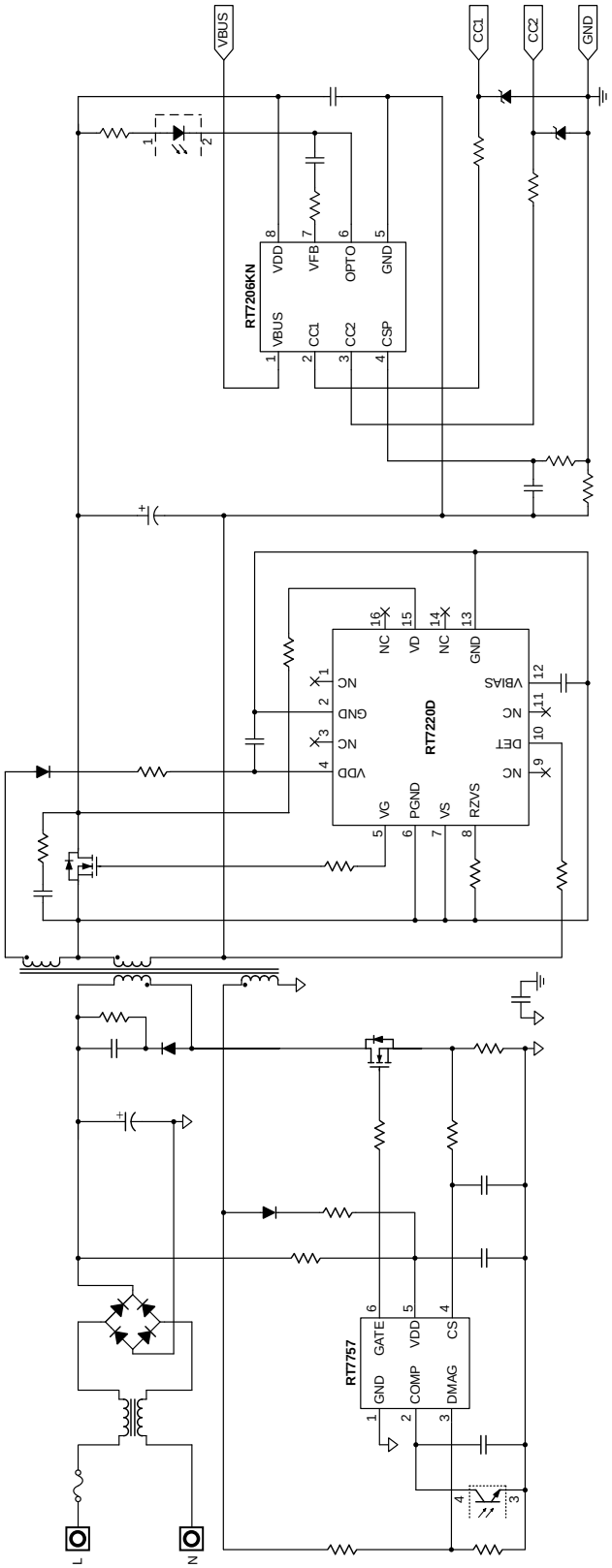
## 14.2 Typical Application Circuit for High-Side Application

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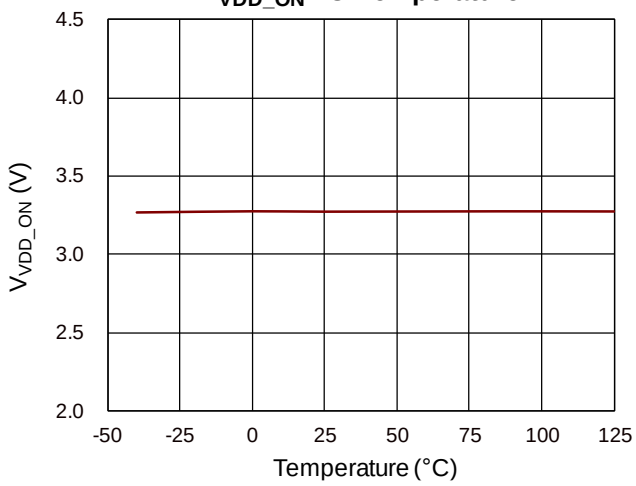
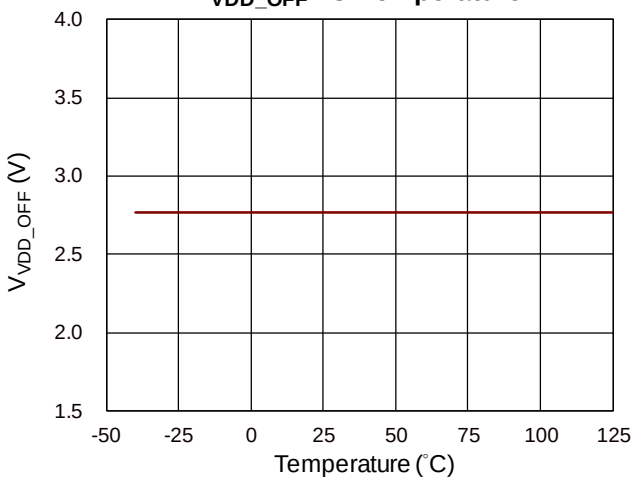
## 15 Typical Operating Characteristics

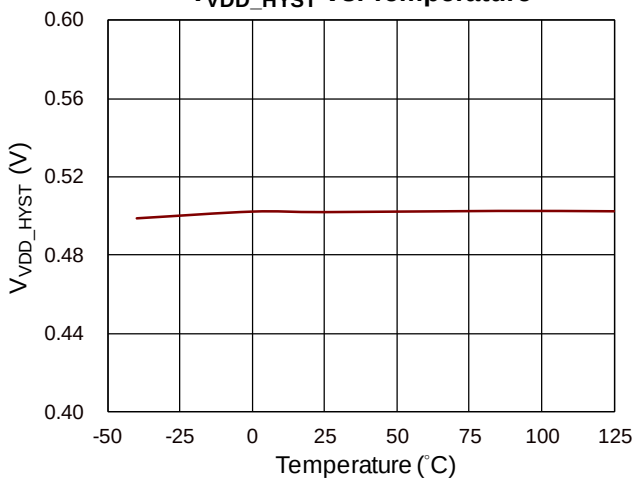
$V_{VDD\_ON}$ vs. Temperature



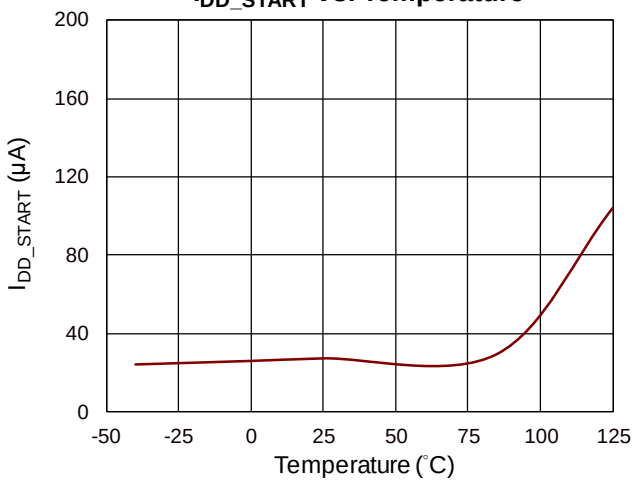

$V_{VDD\_OFF}$ vs. Temperature



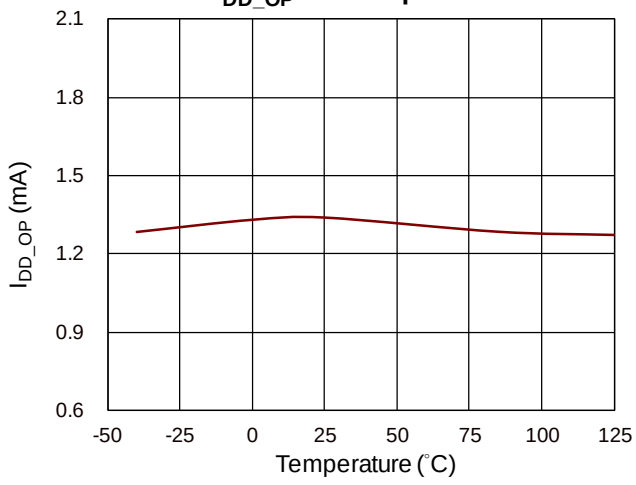

$V_{VDD\_HYST}$ vs. Temperature



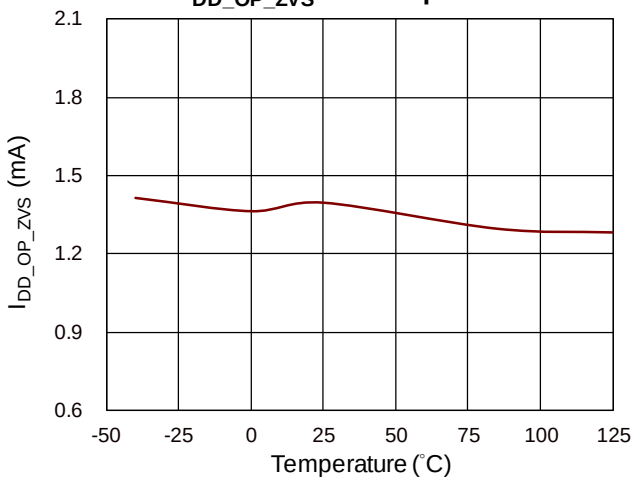

$I_{DD\_START}$ vs. Temperature




$I_{DD\_OP}$ vs. Temperature




$I_{DD\_OP\_ZVS}$ vs. Temperature

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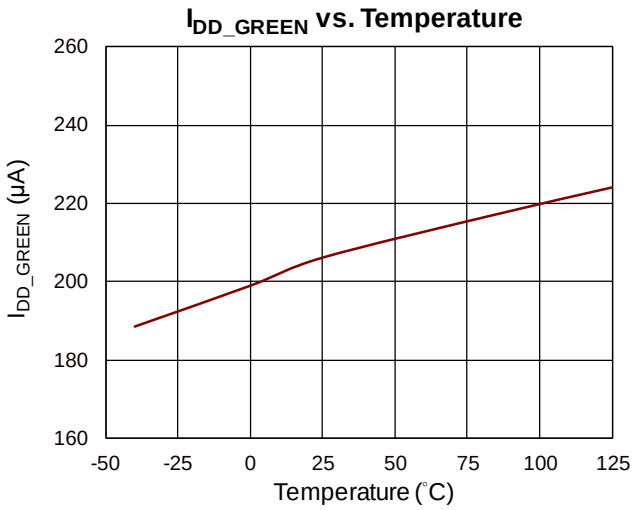


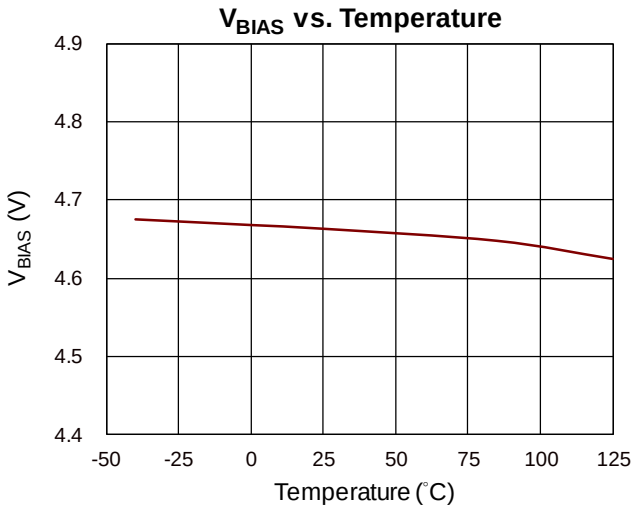


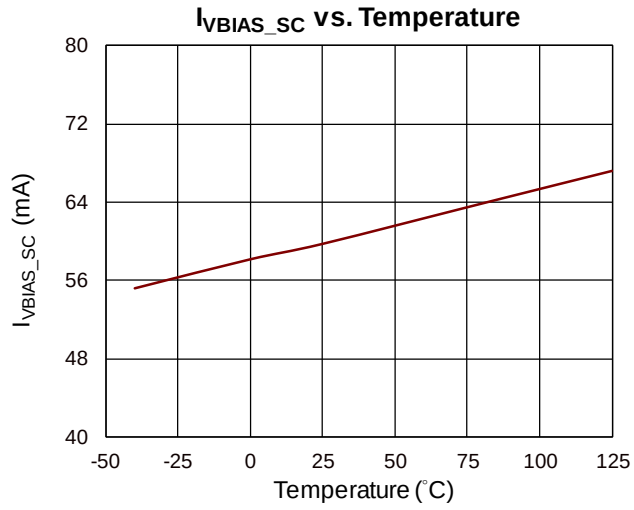


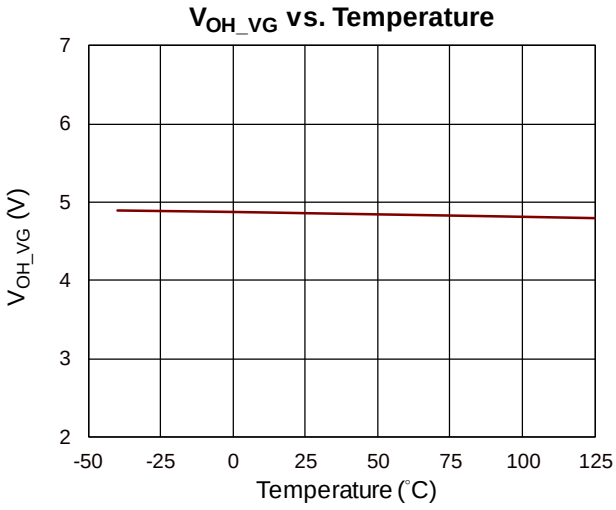


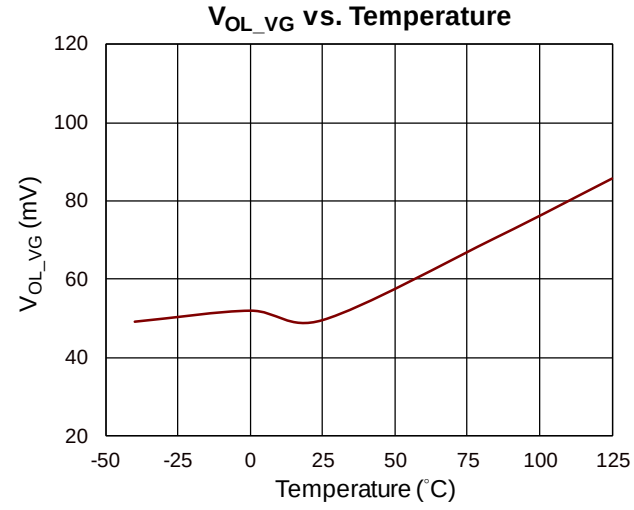


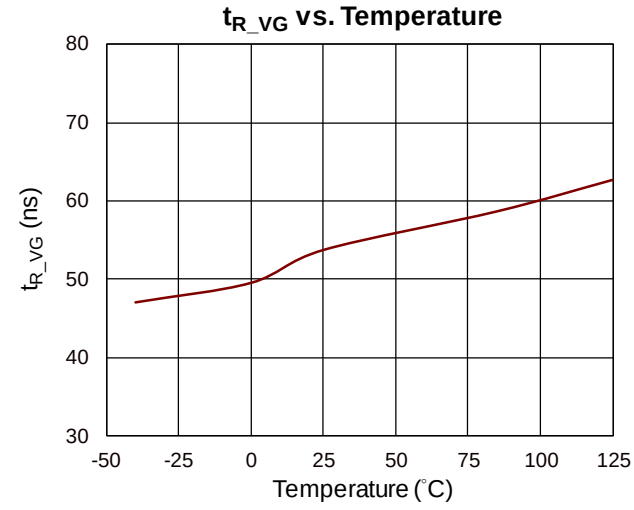


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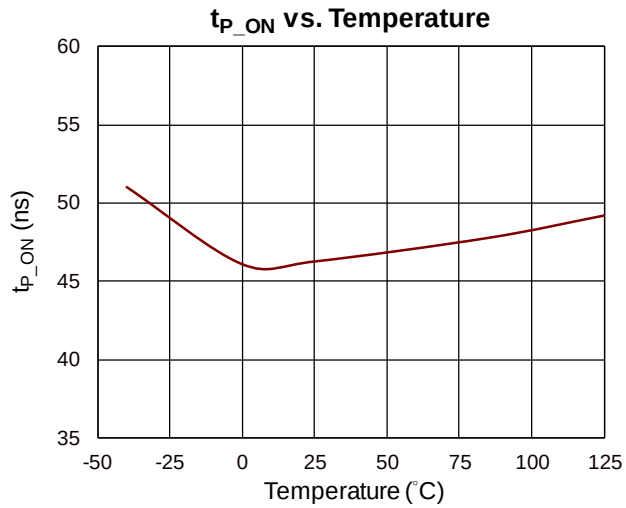


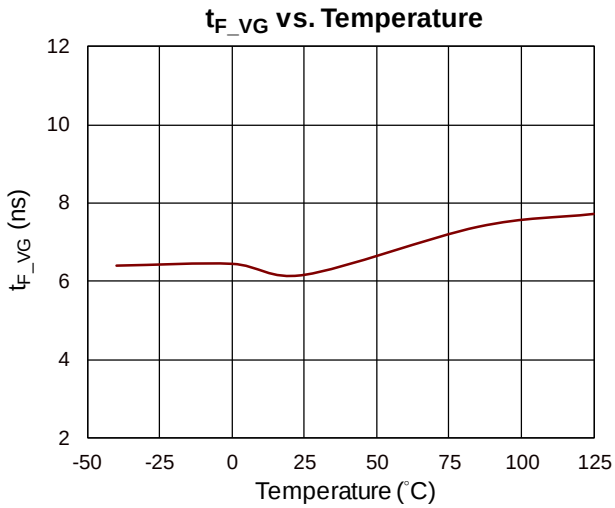


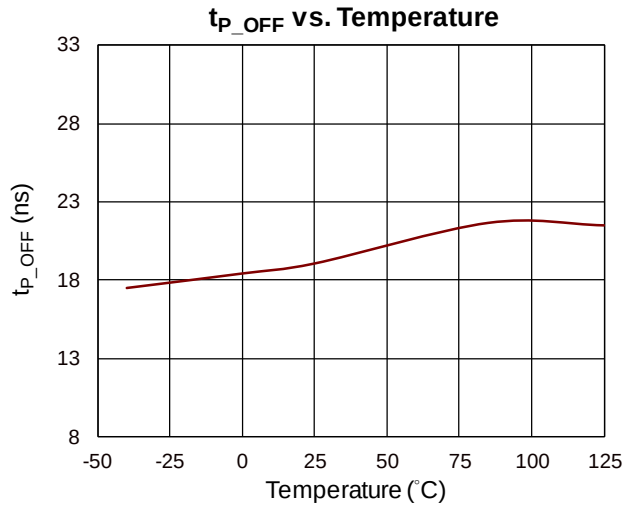


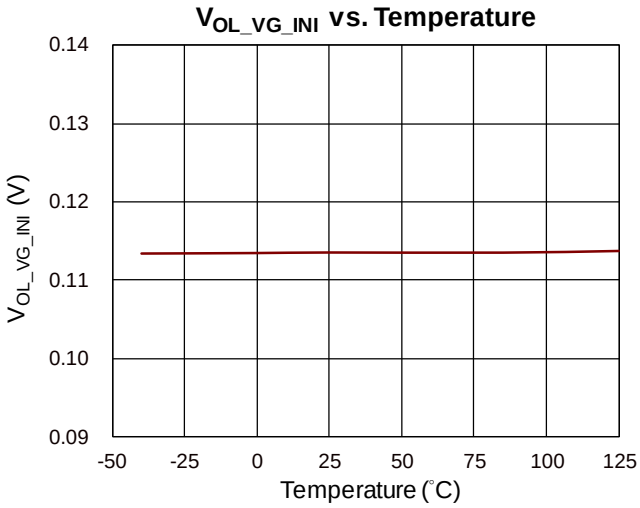


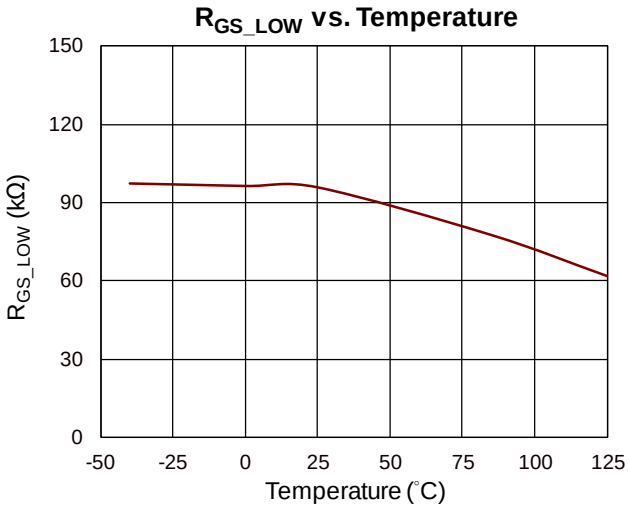


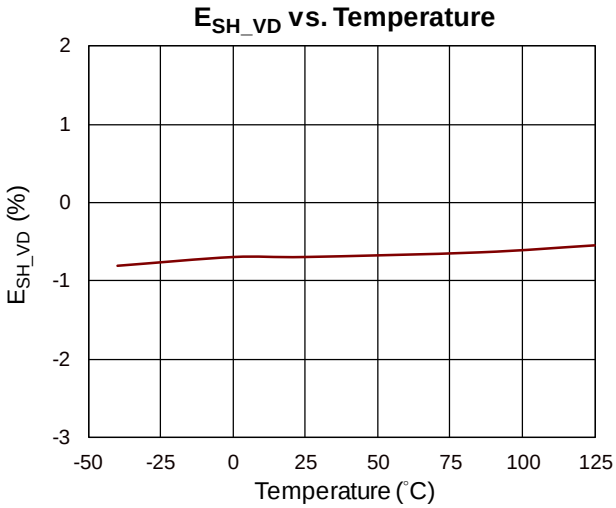


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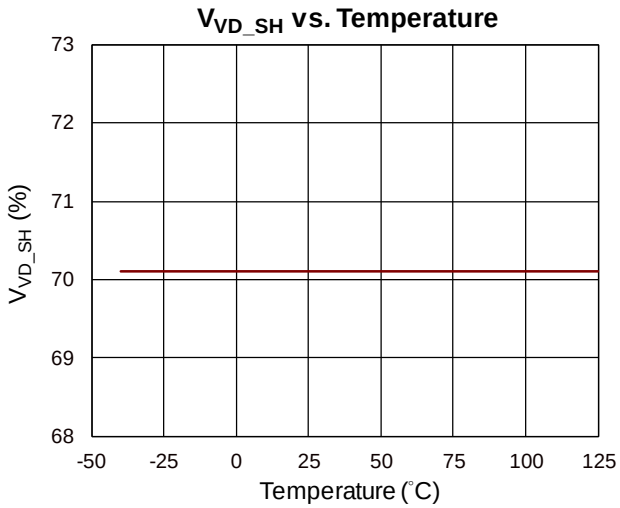


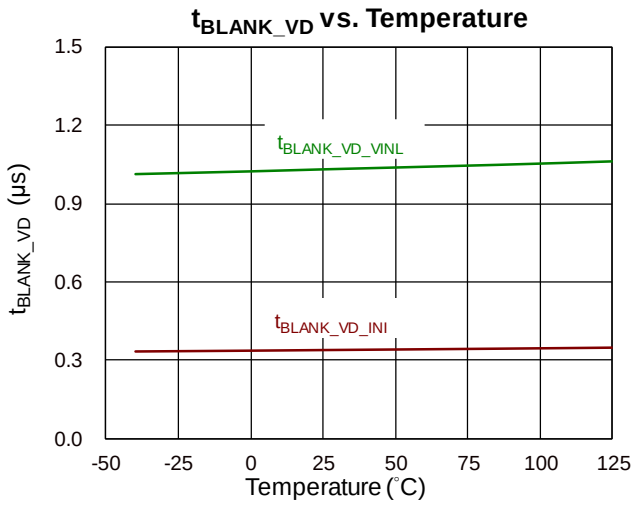


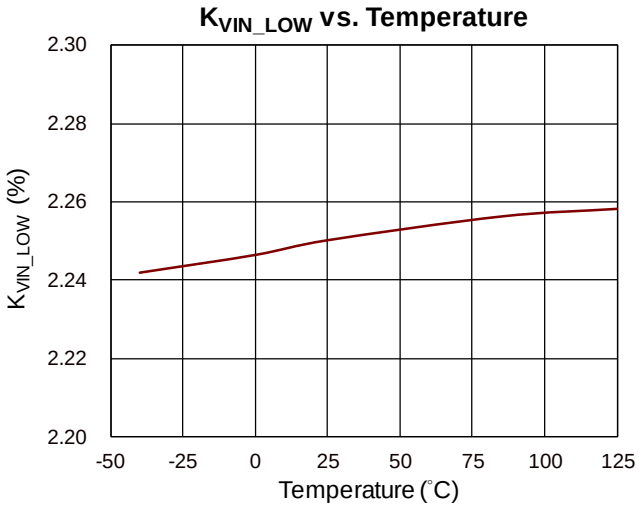


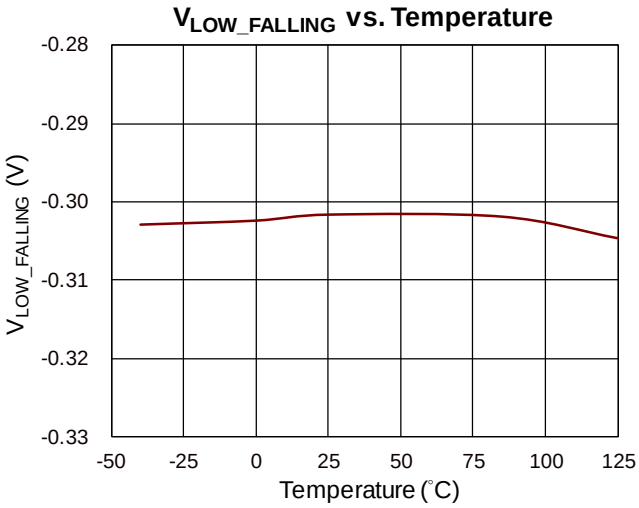


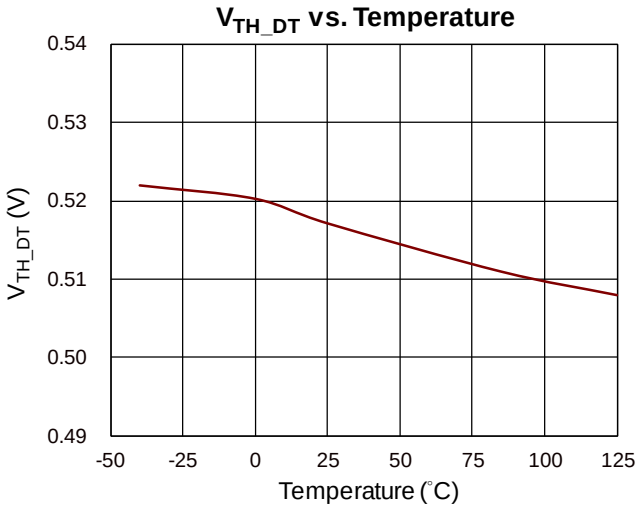


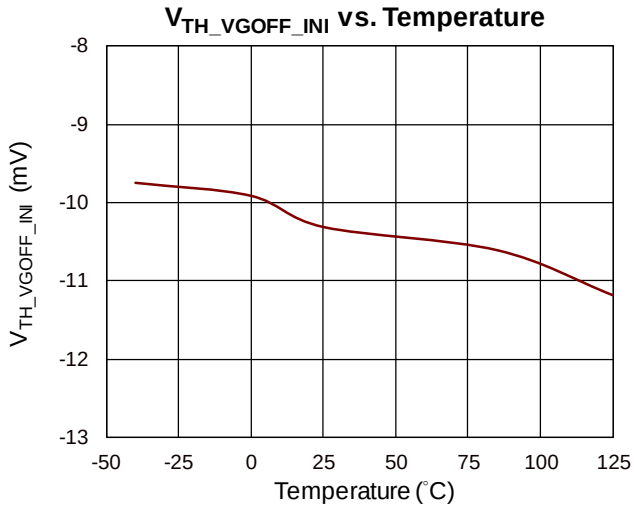


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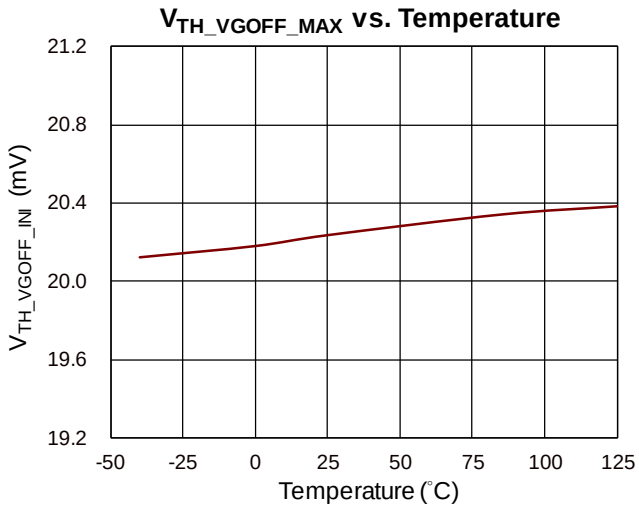


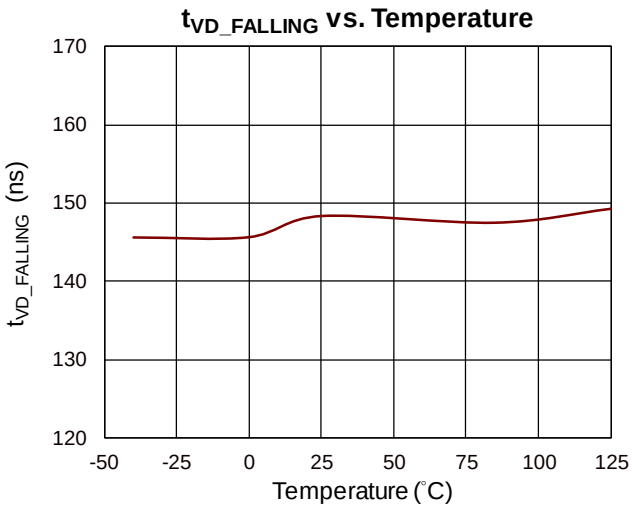


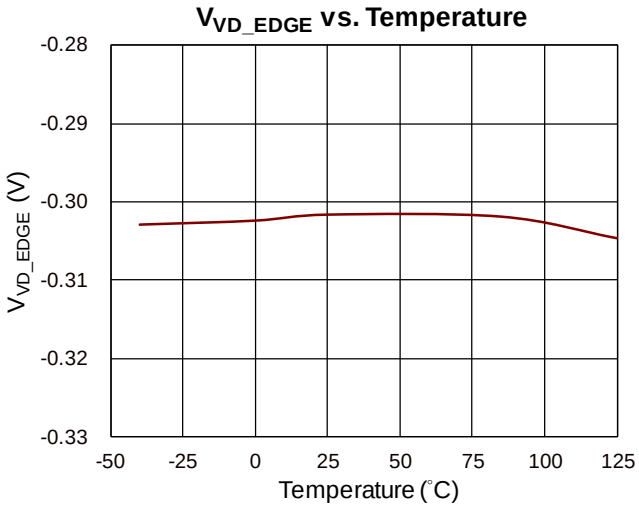


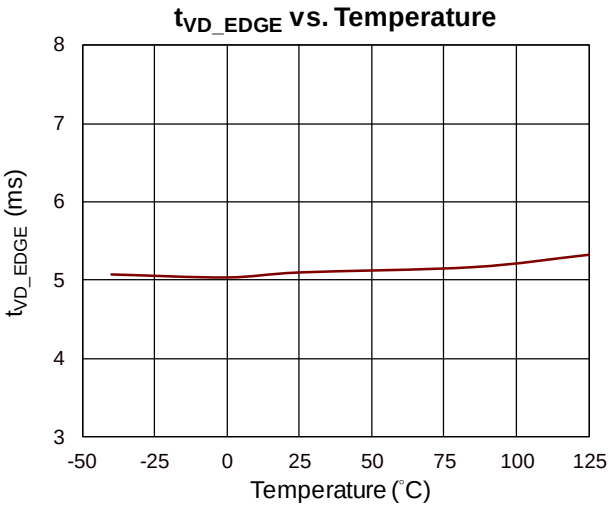


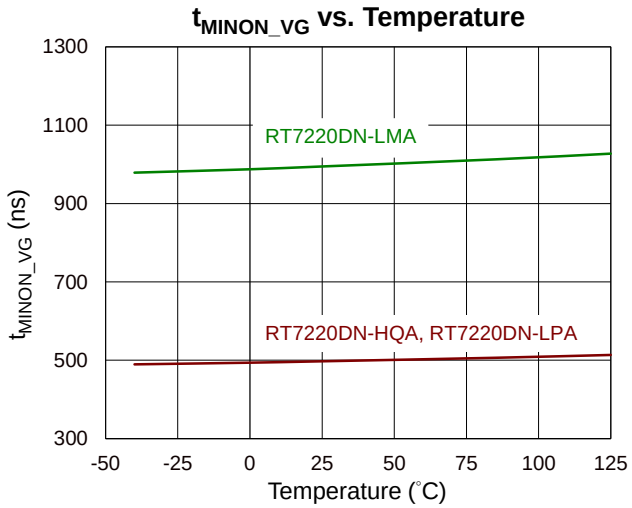


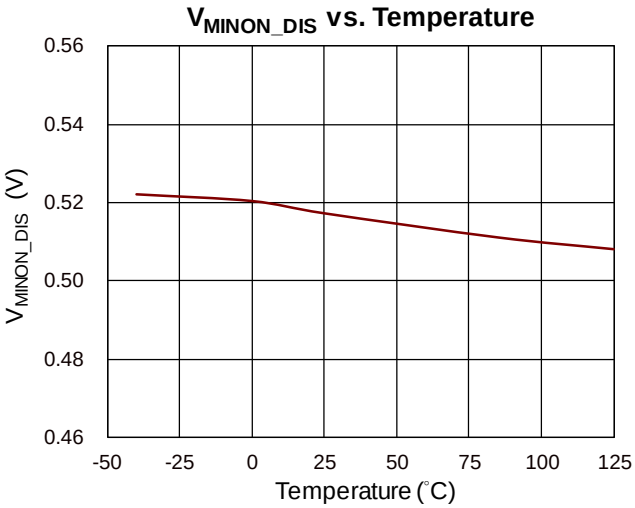


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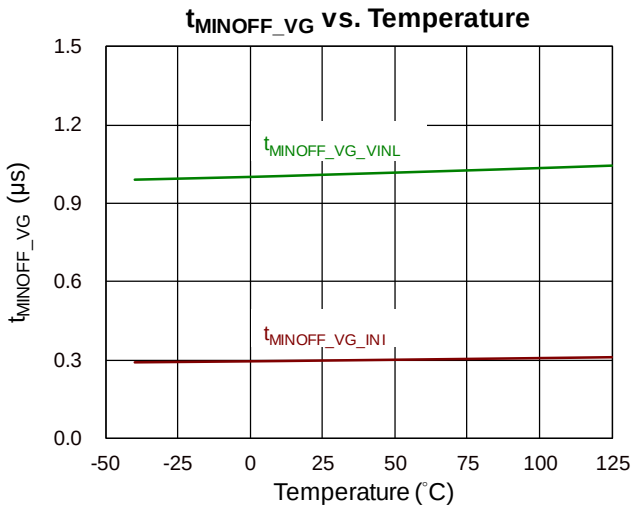


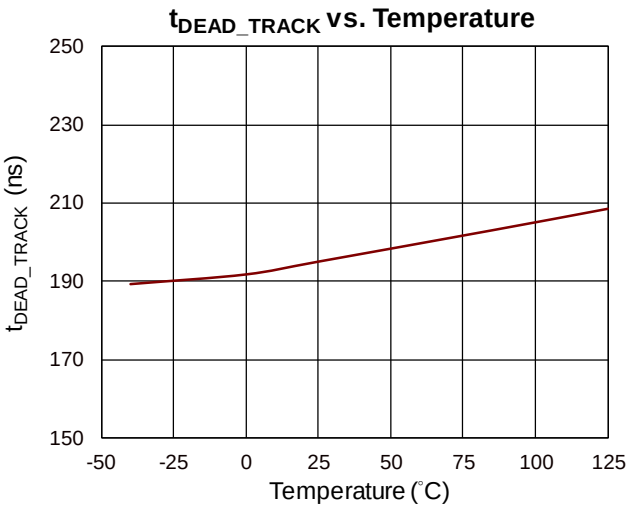


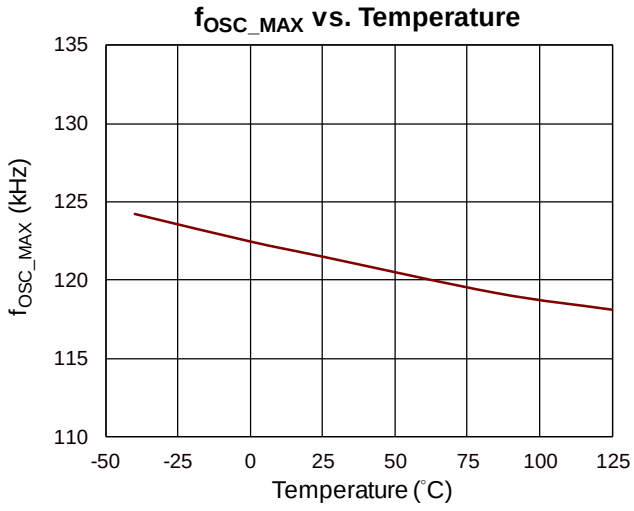


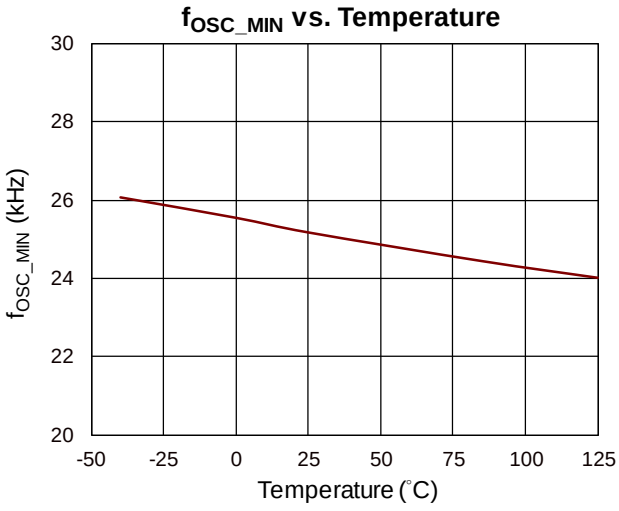


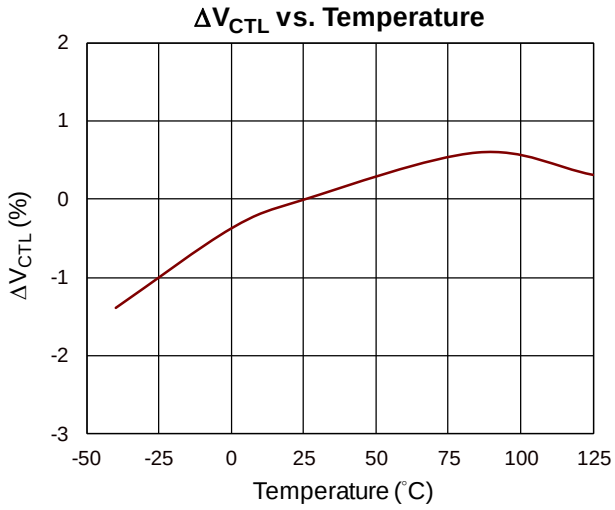


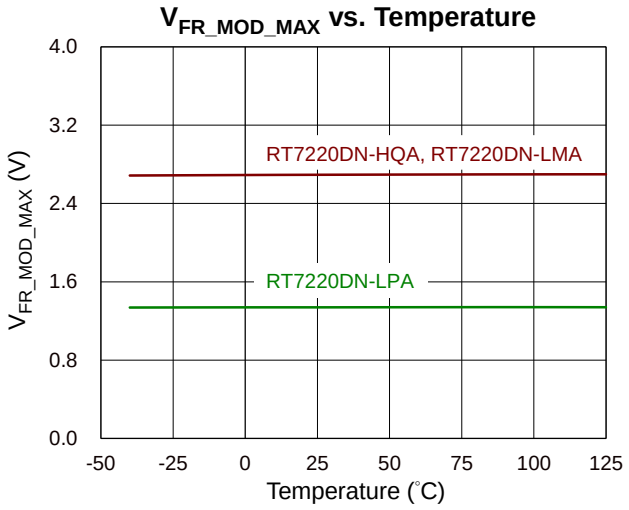


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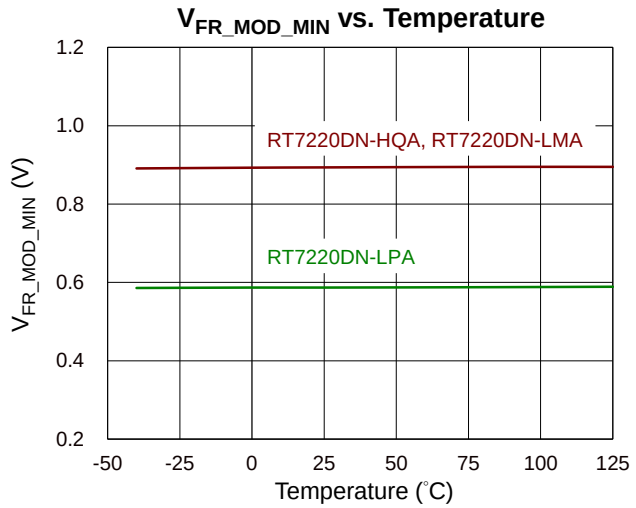


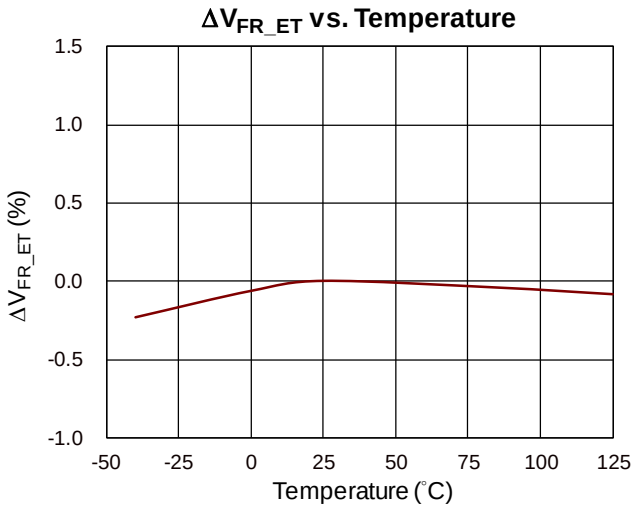


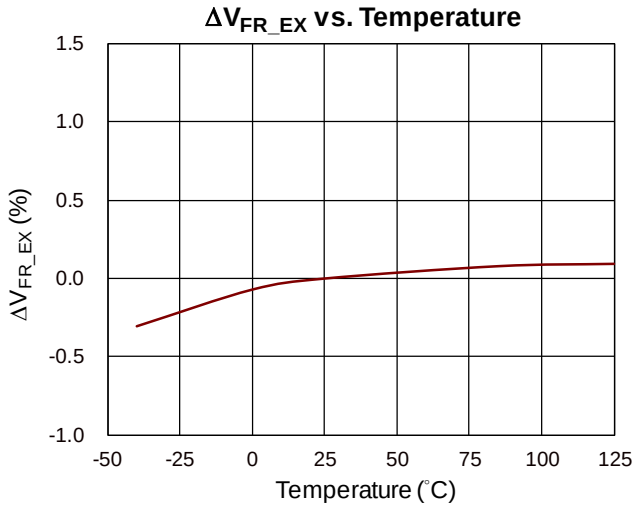


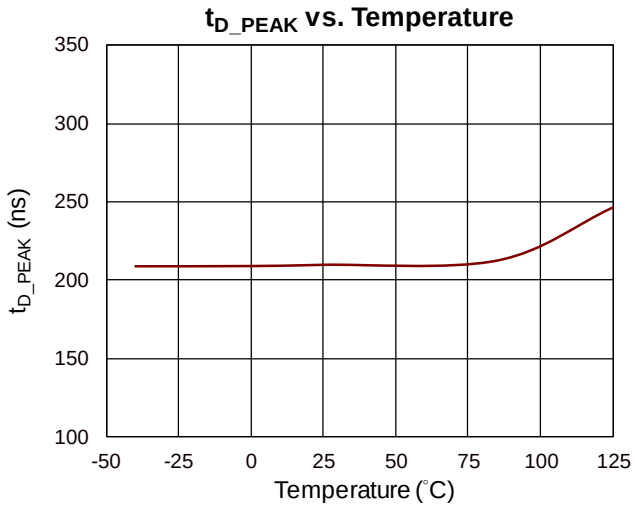


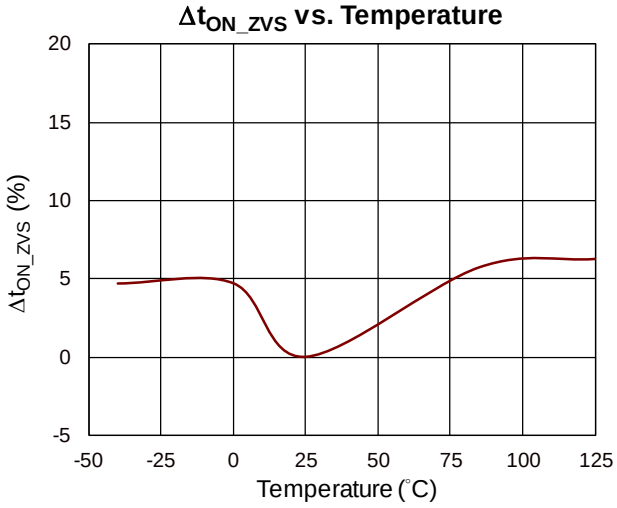


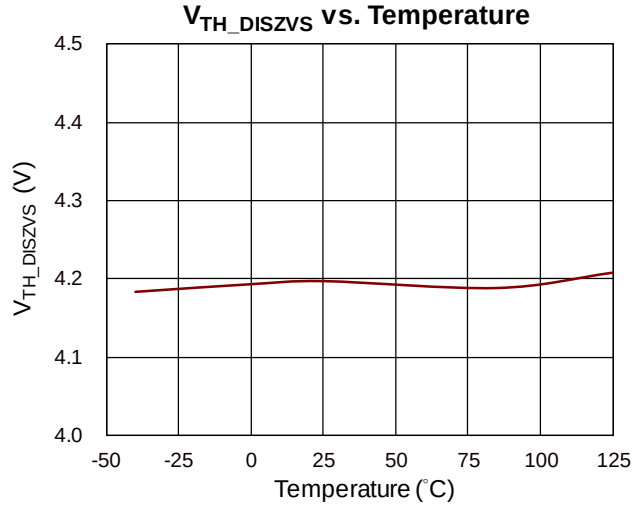


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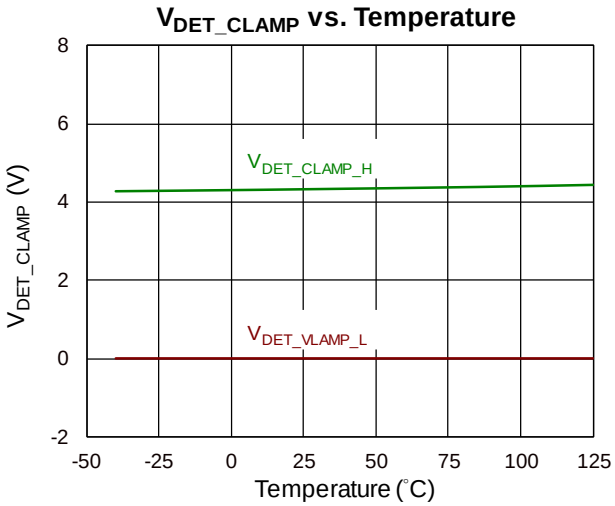


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# 16 Operation

The RT7220D is a secondary-side synchronous rectification controller for flyback converters operating in CCM, DCM, and QR modes. The RT7220D senses the MOSFET drain voltage to determine VG turn-on/off and modulates VG pulse width cycle-by-cycle to minimize turn-off dead time and thereby optimizing the efficiency.

## 16.1 Power Structure

The VDD pin supplies power to the IC and needs to be connected directly to the power supply output capacitor. The VDD pin supports a wide operating range, and the VBIAS is regulated from the LDO to supply the gate driver when output voltage is below 4.7V.

## 16.2 Drain Voltage Sense

The VD pin, connected to the MOSFET drain pin, is used to detect the VD signal as the VG turn-on/off criterion. The DC voltage is supplied from VD to VBIAS via a built-in HV LDO.

## 16.3 Gate Driver

The VG pin is a synchronous rectifier MOSFET driver, powered by either VDD or VBIAS to ensure the MOSFET can be fully turned on. In addition, the fast gate turn-off function provides reliable operation.

## 16.4 Source Voltage Sense

The source pin of MOSFET is connected to the input of the source voltage sensing (VS) pin. To make sure accurate sensing of the drain-sense voltage, it is strongly recommended that the sense node be directly connected to the source of the MOSFET.

## 16.5 ZVS Function

When the power converter operates at high input voltage, the RT7220D enables ZVS function to optimize the efficiency. The adaptive ZVS pulse on-time is modulated by $V_D$, $V_{OUT}$ and $R_{ZVS}$.

To enable the ZVS function, the RT7220D needs to work with the RT7757D. Therefore, the last two characters in the part numbers of both the RT7220D and the RT7757D must be the same. Otherwise, the ZVS function will not operate normally. (For example, RT7757D-AE”MA” ↔ RT7220DN-L”MA”)

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# 17 Application Information

(Note 8)

## 17.1 Power Selection

The RT7220D supports a wide output voltage range with the VDD pin directly connected to the power output of a converter. In addition, a built-in HV LDO is used to supply the gate drive VG for the MOSFET. When VDD is less than 4.7V, the VG voltage powered by VBIAS will be clamped at 4.7V and the ZVS function is disabled. When VDD is greater than 4.7V, the VG voltage will be proportional to VDD. Once VDD is greater than 6V, the VG voltage will be clamped at 6V to ensure fast turn-off time. The power selection circuit is shown in Figure 1.

Moreover, the RT7220D provides an initial pull-low function to avoid the gate of the SR MOSFET being falsely turned on by parasitic capacitance during start-up.

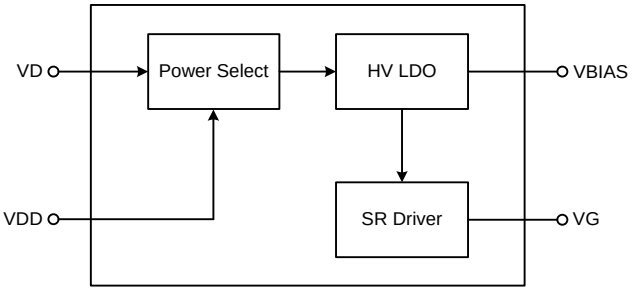


Figure 1. Power Selection Circuit

### VG Turn-On

As shown in Figure 2, when the VD voltage is greater than $V_{VD\_UVP}$ and the VD falling time (from 0.7 x $V_{VD\_SH}$ to $V_{LOW\_FALLING}$) is less than $t_{VD\_FALLING}$ (150ns typ.), VG will be turned on immediately as soon as VD falls below $V_{LOW\_FALLING}$.

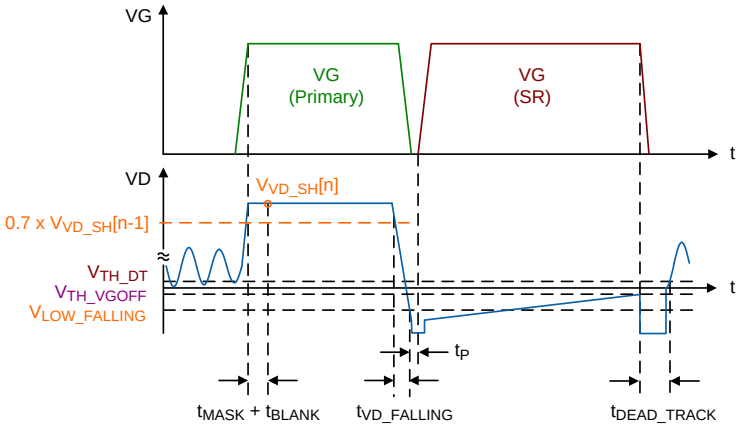


Figure 2. SR Turn-On/Off

## 17.2 VG Turn-Off

As shown in Figure 2, VG will be turned off as the VD voltage rises to $V_{TH\_VGOFF}$. The RT7220D modulates and optimizes the turn-off dead-time $t_{DEAD\_TRACK}$ cycle-by-cycle to provide the reliable and high efficiency operation. For the corrected dead-time modulation, the turn-off delay time of MOSFET ($t_{OFF\_DELAY}$), as shown in Figure 3, should be less than 50% x $t_{DEAD\_TRACK}$.

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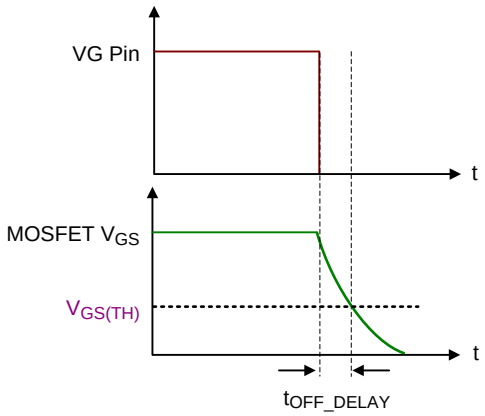


Figure 3. VG Turn-Off Delay Time

### 17.3 VG Minimum On-Time

The RT7220D provides a minimum on-time function to prevent incorrect turn-off due to ringing or voltage spikes. The VG turn-off threshold is blanked during $t_{MINON\_VG}$, as shown in Figure 4.

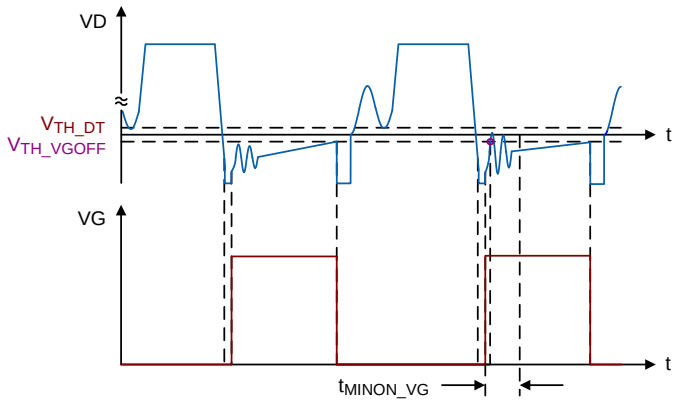


Figure 4. VG Minimum On-Time

### 17.4 VG Minimum Off-Time

The minimum off-time is counted from the falling edge of VG to the next rising edge of VG. During this period, the SR gate cannot be turned on to avoid false triggering of VG by the DCM ringing. The minimum off-time is shown in Figure 5.

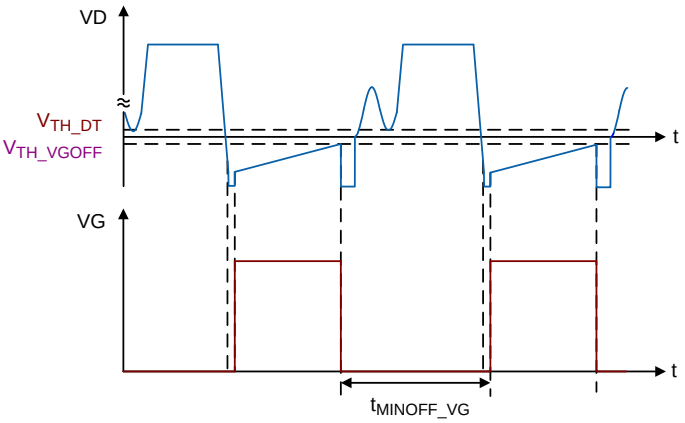


Figure 5. VG Minimum Off-Time

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### 17.5 Green Mode Operation

To improve efficiency under light load conditions, the RT7220D features the green mode operation that disables the SR MOSFET and reduces the device operating current. The green mode is determined by detecting the number of VD and VG pulses, respectively. If VG pulses are less than 16 cycles in the period of $t_{VD\_EDGE}$, the RT7220D disables the VG output and enters green mode, as shown in Figure 6.

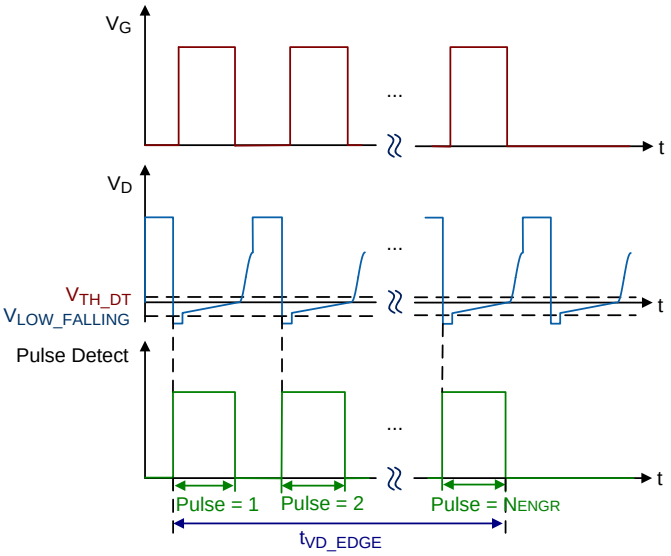


Figure 6. Entry Green Mode

Once VD pulses are greater than 32 cycles in the period of $t_{VD\_EDGE}$, the RT7220D exits from green mode and resumes normal operation immediately, as shown in Figure 7.

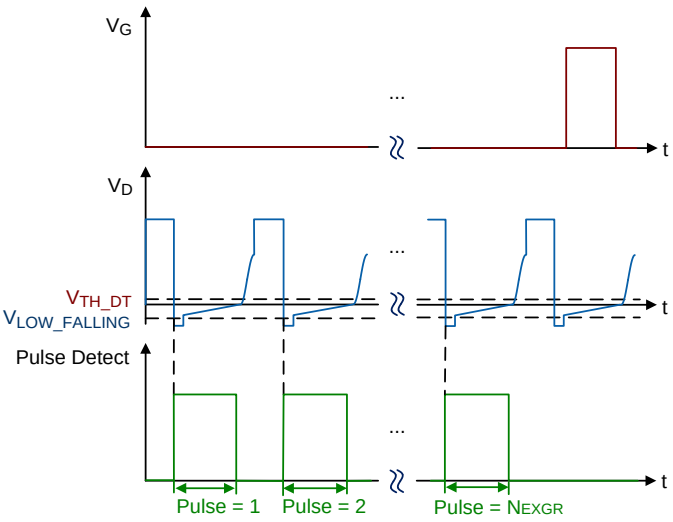


Figure 7. Exit Green Mode

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### 17.6 Output Voltage Sense for High-Side Application

For high-side applications, since the RT7220D GND and the power converter's GND are not the same, the VDD pin cannot sense the output voltage. Therefore, the DET pin is used to detect the output voltage.

During the SR MOSFET on-time, the DET pin outputs a clamping current that is proportional to $V_{OUT}$.

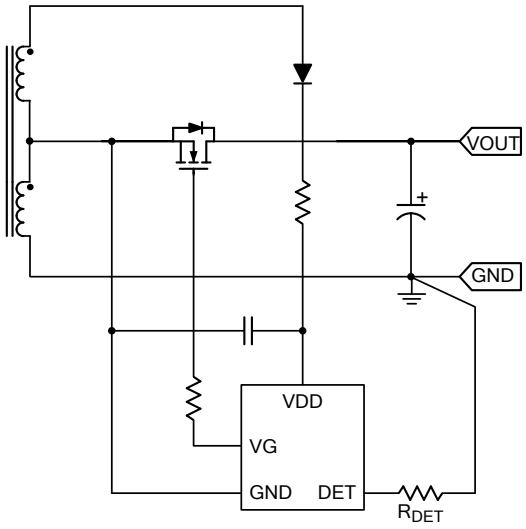


Figure 8. $V_{OUT}$ Sense for High-Side Applications

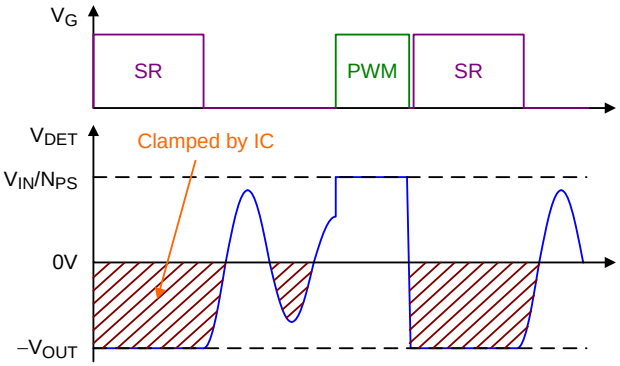


Figure 9. DET Pin Waveform

The resistance of $R_{DET}$ is 300kΩ and a 1% tolerance resistor is recommended. In the low-side applications, the DET pin function is disabled and should be connected to the RT7220D GND.

### 17.7 VD Undervoltage Protection

To avoid the RT7220D from mis-triggering VG during the AC OFF period, the SR function will be disabled when $V_D$ is lower than $V_{VD\_UVP}$. Since VD is equal to ($V_{OUT}$ + $V_{IN}/N_{PS}$), the boundary $V_{IN}$ of VD undervoltage protection ($V_{IN\_BOUNDARY}$) can be obtained according to the following equation:

$V_{IN\_BOUNDARY} = N_{PS} \times (V_{VD\_UVP} - V_{OUT})$

where $N_{PS}$ is the primary-to-secondary turn ratio.

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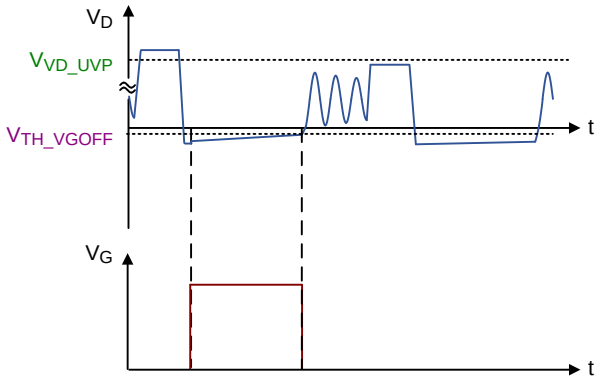


Figure 10. VD Undervoltage Protection

### 17.8 Frequency Control Method

When the power converter operates at high input voltage, higher output voltage and heavy load, the system will operate in ZVS mode, and the switching frequency is determined by the RT7220D. Before the primary-side MOSFET is turned on, the secondary-side MOSFET will be turned on shortly to generate a circulating current for achieving ZVS in primary-side MOSFET.

The RT7220D determines the switching frequency using a control voltage that includes the magnetic inductor $L_m$, the primary-to-secondary turn ratio $N_{PS}$, the $V_{OUT}$ scaling ratio $K_{VO}$, the inductor peak current $I_{peak}$ and the internal setting resistor $R_{SET}$. $V_{CTL}$ can be expressed by the following equation:

$V_{CTL} = (10^{11} \times K_{VO} \times L_m \times I_{peak}) / (3 \times N_{PS} \times R_{SET})$

The internal $R_{SET}$ can be calculated by the following equations:

$$\begin{cases} \frac{1}{2} \times L_m \times (I_{peak})^2 \times f_{SW} \times Eff. = P_O \\ f_{SW} = f_{OSC\_MIN} + 271.4(kHz/V) \times (V_{CTL} - V_{FR\_EX}) \\ V_{CTL} = \frac{10^{11} \times K_{VO} \times L_m \times I_{peak}}{3 \times N_{PS} \times R_{SET}} \end{cases}$$

### 17.9 ZVS Operation

When the converter operates in ZVS mode, the RT7220D detects the VD ringing to perform the ZVS operation. Once the VD ringing decreases to $V_{OUT}$ for the debounce time $t_{D\_PEAK}$, the ZVS pulse is turned on. The adaptive ZVS pulse on-time is modulated by VD, $V_{OUT}$ and $R_{ZVS}$.

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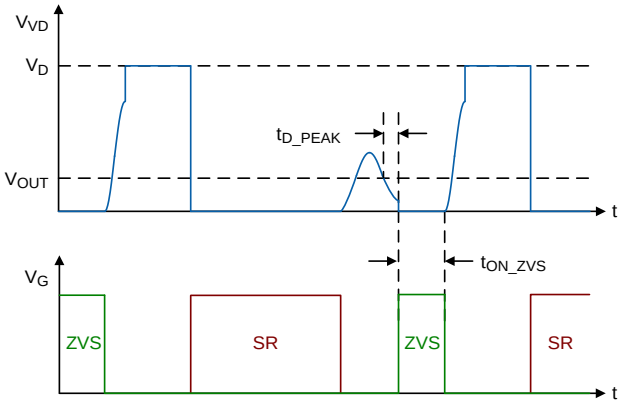


Figure 11. ZVS Operation

The external $R_{ZVS}$ ranges from 200kΩ to 500kΩ, and a 1% tolerance resistor is recommended. The on-time of the ZVS pulse is limited from 450ns to 4.4μs, and it can be expressed by the following equation:

$t_{ON\_ZVS} = (V_D \times R_{ZVS}) / (1875 \times V_{OUT}) - 200$ (ns)

### 17.10 Design Considerations and PCB Layout Guide

- The bypass capacitor of VDD and VBIAS should be placed as close as possible to the RT7220D. It is recommended to use a low ESR MLCC capacitor of 1μF or more to reduce ripple.
- The resistor between the VD pin and the drain of the SR MOSFET is necessary. It is recommended to use a 47Ω resistor with a package larger than 0603.
- To avoid IR voltage drop affecting the output voltage detection, the VDD pin must be connected to the output capacitor independently.
- To detect $V_{DS}$ accurately, VS, GND and PGND must be connected to the source of the SR MOSFET independently. The ground of $C_{VBIAS}$ and $R_{ZVS}$ should be connected to the exposed GND pad of RT7220D for noise isolation and the exposed GND should be connected to the other GND pins.
- The SR MOSFET drive loop should be as short as possible to reduce EMI.
- For high-side applications, the auxiliary winding for VDD is required, and the VDD capacitor must be larger than 4.7μF.
- For high-side applications, to detect the output voltage accurately, the DET pin resistor must be connected to the GND of the output capacitor independently. The resistor $R_{DET}$ between the DET pin and GND should be 300kΩ with a package of 0603 or larger.
- Keep the IC out of the power loop to prevent abnormal operation from noise coupling. For four-layer PCB layout, the power loop should not pass through the 2nd and 3rd PCB layers under the RT7220D chip.

### 17.11 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

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where $T_{J(MAX)}$ is the maximum junction temperature; $T_A$ is the ambient temperature; and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WQFN-16L 3x3 package, the thermal resistance, $\theta_{JA}$, is 42.5°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (42.5°C/W) = 2.35W for a WQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curve in Figure 12 allows the designer to inspect the effect of rising ambient temperature on the maximum power dissipation.

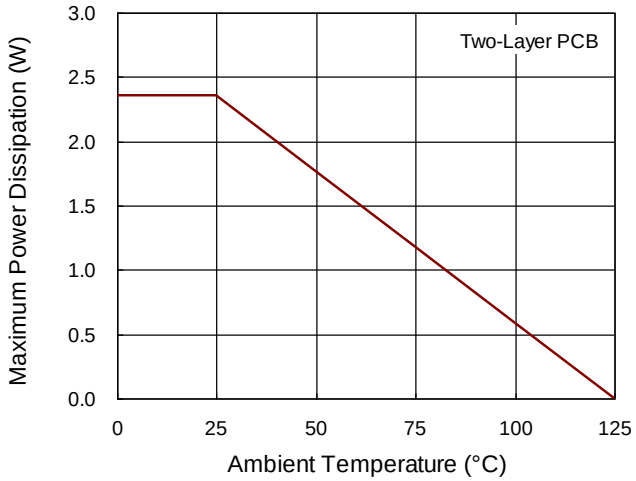


Figure 12. Derating Curve of Maximum Power Dissipation

**Note 8**. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

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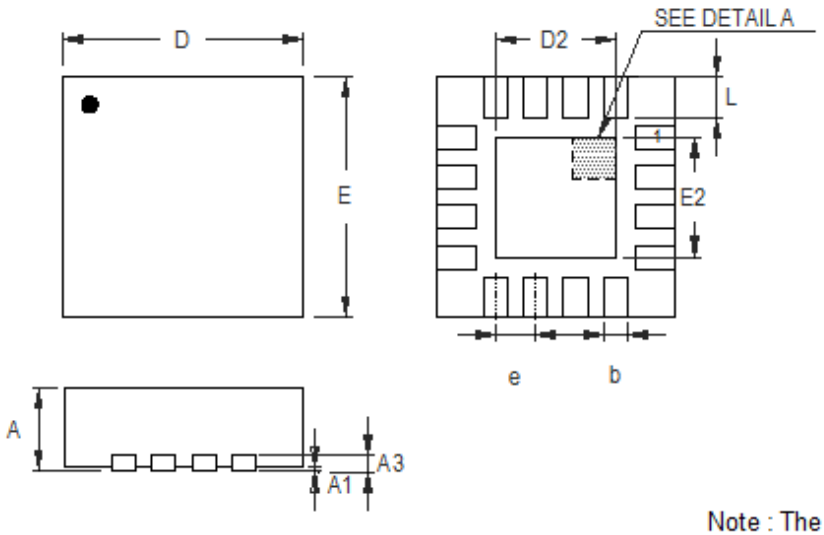
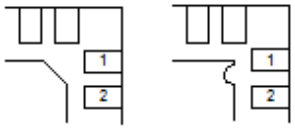
## 18 Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| D | 2.950 | 3.050 | 0.116 | 0.120 |
| D2 | 1.300 | 1.750 | 0.051 | 0.069 |
| E | 2.950 | 3.050 | 0.116 | 0.120 |
| E2 | 1.300 | 1.750 | 0.051 | 0.069 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

**W-Type 16L QFN 3x3 Package**

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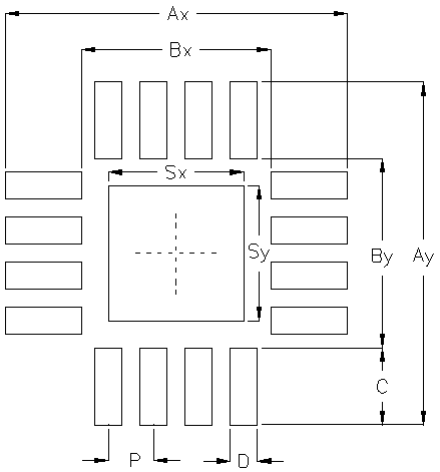
## 19 Footprint Information




| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | | | Tolerance |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | P | Ax | Ay | Bx | By | C | D | Sx | Sy | |
| V/W/U/XQFN3*3-16 | 16 | 0.50 | 3.80 | 3.80 | 2.10 | 2.10 | 0.85 | 0.30 | 1.50 | 1.50 | ±0.05 |

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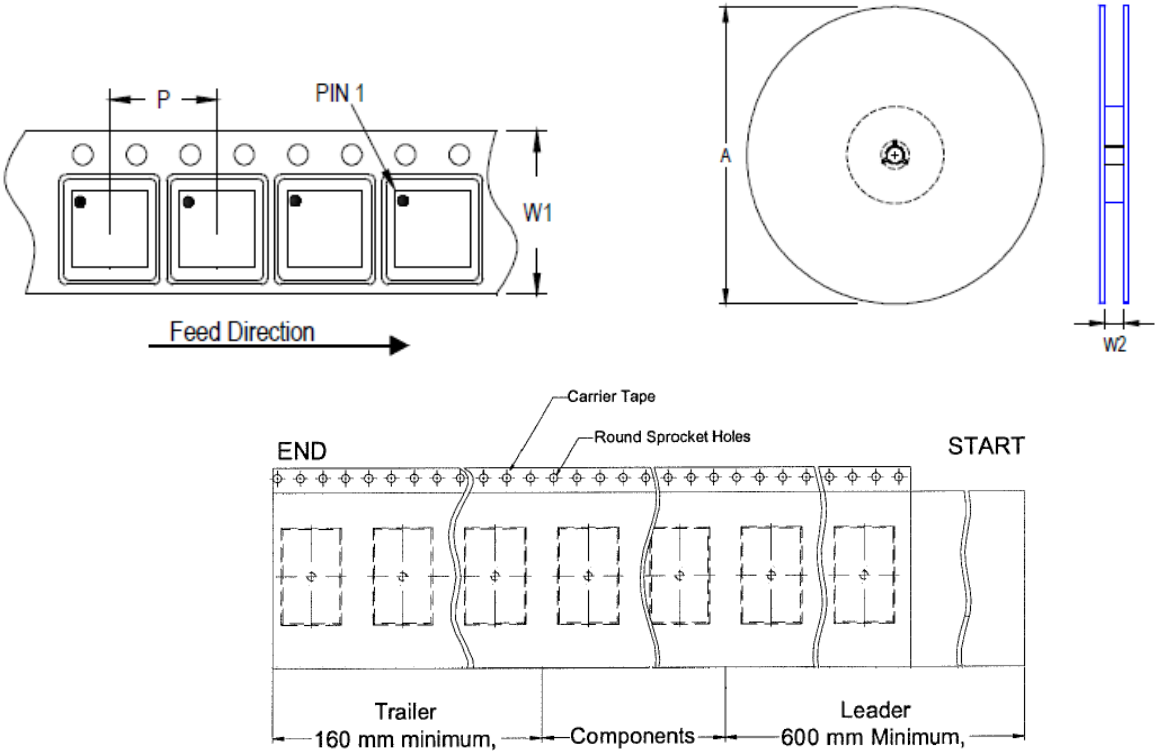
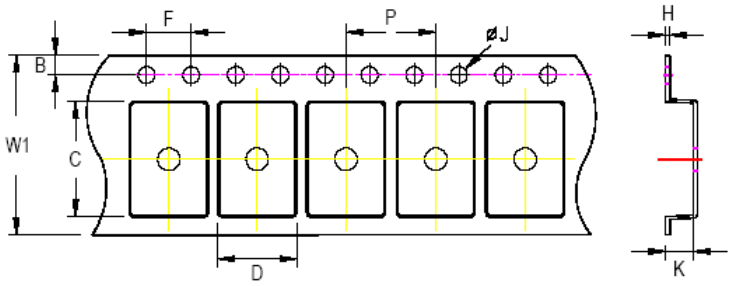
# 20 Packing Information

## 20.1 Tape and Reel Data




| Package Type | Tape Size (W1) (mm) | Pocket Pitch (P) (mm) | Reel Size (A) | | Units per Reel | Trailer (mm) | Leader (mm) | Reel Width (W2) Min./Max. (mm) |
|---|---|---|---|---|---|---|---|---|
| | | | (mm) | (in) | | | | |
| QFN/DFN 3x3 | 8 | 4 | 180 | 7 | 3,000 | 160 | 600 | 8.4/9.9 |




**C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:**

**- For 8mm carrier tape: 0.5mm max.**

| Tape Size | W1 | P | | B | | F | | ØJ | | H |
|---|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Max. |
| 12mm | 12.3mm | 7.9mm | 8.1mm | 1.65mm | 1.85mm | 3.9mm | 4.1mm | 1.5mm | 1.6mm | 0.6mm |

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### 20.2 Tape and Reel Packing

| Step | Photo/Description | Step | Photo/Description |
|---|---|---|---|
| 1 |  Reel 7” | 4 |  3 reels per inner box **Box A** |
| 2 |  HIC & Desiccant (1 Unit) inside | 5 |  12 inner boxes per outer box |
| 3 |  Caution label is on backside of Al bag | 6 |  Outer box **Carton A** |

| Container / Package | Reel | | Box | | | Carton | | |
|---|---|---|---|---|---|---|---|---|
| | Size | Units | Item | Reels | Units | Item | Boxes | Unit |
| QFN & DFN 3x3 | 7” | 1,500 | Box A | 3 | 9,000 | Carton A | 12 | 108,000 |
| | | | Box E | 1 | 3,000 | For Combined or Partial Reel. | | |

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### 20.3 Packing Material Anti-ESD Property

| Surface Resistance | Aluminum Bag | Reel | Cover tape | Carrier tape | Tube | Protection Band |
|---|---|---|---|---|---|---|
| Ω/cm$^2$ | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** | **$10^4$ to $10^{11}$** |

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## 21 Datasheet Revision History

| Version | Date | Description | Item |
|---|---|---|---|
| 01 | 2023/5/22 | Modify | RT7220D Version Table on P2<br>Absolute Maximum Ratings on P6<br>Recommended Operating Conditions on P6<br>Electrical Characteristics on P7<br>Application Information on P24 |
| 02 | 2024/7/5 | Modify<br>(Added RT7220DN-LMA) | General Description on P1<br>Features on P1<br>Ordering Information on P1<br>Marking Information on P2<br>RT7220D Version Table on P5<br>Note 4 on P8<br>Electrical Characteristics on P11, 12, 13<br>Typical Application Circuit on P14, 15<br>Typical Operating Characteristics on P20, 21, 22<br>Operation on P24<br>Application Information on P31<br>Packing Information on P35 |

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