Synchronous Rectifier Controller with Wide Output Voltage Operating Range

General Description

The RT7220A is a high performance Synchronous Rectifier (SR) controller for flyback converters operating in Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM) and Quasi-Resonant (QR) mode. This SR controller senses the drain voltage of MOSFET to determine SR gate on/off so as to minimize turn-off dead-time and enhance efficiency.

The RT7220A is designed to support a wide output voltage range of 3V to 22V, and an HV LDO is especially built-in for the MOSFET gate driver to operate at low output voltage.

Furthermore, the RT7220A offers a Green Mode operation, in light load condition, in which the RT7220A counts the gate pulse of MOSFET to determine the timing for entering green mode and to reduce operation current under 160μA.

The recommended junction temperature range is −40°C to 125°C, and the ambient temperature range is −40°C to 105°C.

Ordering Information

RT7220A□□□□

- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Richtek Green Policy Compliant
- RT7220A Version
  (Refer to Version Table)

Note:

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

Features

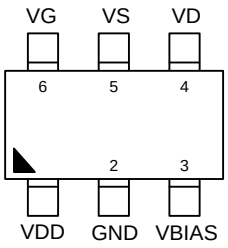
- **Suitable for High/Low-Side SR Control of Flyback in CCM, DCM and Quasi-Resonant Mode**
- **Suitable for 3V to 22V V_{OUT} Range**
- **<1.2mA Operating Current in Normal Mode (Without SR Driver)**
- **<160μA Operating Current in Green Mode**
- **Built-in HV LDO to Supply SR Driver when V_{OUT} Lower than 5V**
- **Automatic Tracking Control to Optimize Efficiency**
- **300kHz Maximum Operation Frequency**
- **Protection**
  - **SR Gate Driver with 6V Clamp**
  - **SR Gate Initial Output Low Clamping Voltage before Start-Up**
  - **Optional Minimum Period Protection**
  - **Optional SR Minimum Off-Time**
  - **VG Fast Turn-Off (The Total Delay is Less than 35ns)**

Applications

- Travel Adapters with Fast Charge Protocols (e.g., FCP, SCP, AFC and QC2.0/QC3.0)
- Travel Adapters with USB PD Type-C Control
- Netcom Adapters

Pin Configuration

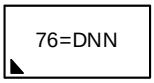
(TOP VIEW)



SOT-23-6

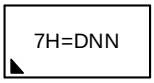
Marking Information

RT7220AMDGE



76= : Product Code
DNN : Date Code

RT7220AHDGE



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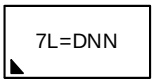
RT7220AHCGE



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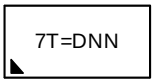
RT7220AHFGE



7T= : Product Code
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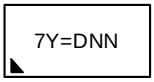
RT7220AHJGE

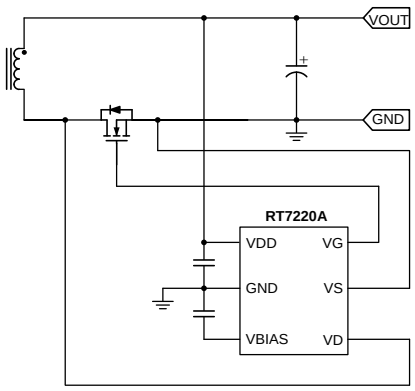


7Y= : Product Code
DNN : Date Code

RT7220A Version Table

Version		RT7220AMD	RT7220AHD	RT7220AHC	RT7220AHF	RT7220AHJ
VD Voltage Supported		120V	120V	120V	120V	120V
Output Voltage Supported		3V to 22V	3V to 22V	3V to 22V	3V to 22V	3V to 22V
Maximum Operation Frequency		100kHz	150kHz	150kHz	150kHz	150kHz
Minimum Period		Disable	Disable	Disable	Disable	Disable
HV LDO		120V / 60mA	120V / 60mA	120V / 60mA	120V / 60mA	120V / 60mA
VG Minimum On Time		1500ns	890ns	500ns	890ns	500ns
VG Minimum Off Time	Initial	0.45μs	0.45μs	0.3μs	0.45μs	0.45μs
	VIN Low	1.95μs	1.95μs	1.05μs	1.95μs	1.95μs
VD Falling Time Threshold for VG Trigger		150ns			200ns	150ns
VG Fast Turn-Off Initial Threshold		−10mV				−25mV

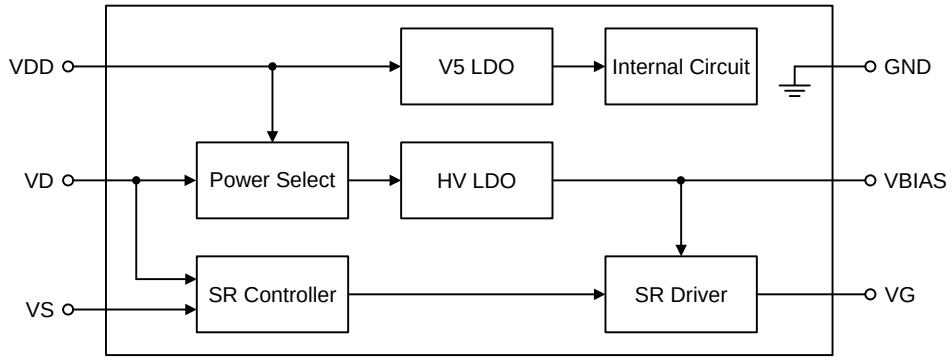
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	VDD	PWR	Supply input voltage.
2	GND	GND	Ground.
3	VBIAS	PWR	Regulated DC bias.
4	VD	AI	Drain voltage sense node for the SR MOSFET.
5	VS	AI	Source voltage sense node for the SR MOSFET.
6	VG	AO	Gate driver output for the SR MOSFET.

Functional Block Diagram



Operation

The RT7220A SR controller is a secondary-side synchronous rectification controller for flyback converters operating in CCM mode, DCM mode and QR mode. The RT7220A senses the MOSFET drain voltage to determine VG turn-on/off, and modulates VG pulse width cycle-by-cycle to minimize turn-off dead time and therefore enhances the efficiency.

Power Structure

The VDD pin supplies power for the IC, and can be directly connected to the power supply output capacitor, of which the VDD pin supports a wide operating range from 3V to 22V, and the VBIAS is regulated from LDO to supply the gate driver when output voltage is under 4.7V.

Ground

In order to accurately detect VDS, the PCB layout of VS and GND must be connected to the Source of the SR MOSFET and system ground independently.

Drain Voltage Sense

The VD pin connects the MOSFET drain pin to detect VD signal as VG turn-on/off criterion. The DC voltage is supplied from VD to VBIAS via a built-in HV LDO.

Gate Driver

The VG pin is a synchronous rectifier MOSFET driver, where the VG's power is supplied by selected either from VDD or VBIAS so as to ensure MOSFET is fully turned-on, and to provide the gate fast turn-off function under a reliable operation.

Source Voltage Sense

The source pin of MOSFET is connected to the input of the source voltage sensing VS pin. To ensure correct drain-sense voltage sensing, it is strongly recommended that the sense node should be directly connected to the source of MOSFET.

Absolute Maximum Ratings (Note 1)

- VD to GND (Pulse Width 500ns) ---------- –1V to 130V
- VD to GND (DC Continue) ---------- –1V to 120V
- VDD to GND ---------- –0.3V to 25V
- VG to GND ---------- –0.3V to 10V
- VBIAS to GND ---------- –0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 260.7°C/W
  SOT-23-6, θ_{JC} ---------- 135°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model)
  Except VD Pin ---------- 2kV
  VD to GND ---------- 1kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VD ---------- ---------- –1V to 120V
- Supply Input Voltage, VDD ---------- 3V to 22V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold Voltage	V_{VDD_ON}		3.05	3.25	3.45	V
VDD Turn-Off Threshold Voltage	V_{VDD_OFF}		2.7	2.8	2.9	V
Hysteresis Voltage for VDD Turn-On/VDD Turn-Off Threshold	V_{VDD_HYST}		0.35	0.45	0.55	V
VDD Turn-On Deglitch Time	$t_{D\_VDD\_ON}$		--	50	--	µs
VDD Turn-Off Deglitch Time	$t_{D\_VDD\_OFF}$		--	5	--	µs
VDD Start-Up Current	I_{DD_START}		--	--	150	µA
VDD Operating Current	I_{DD_OP}	SR driver is disabled.	--	1	1.2	mA
VDD Green-Mode Current	I_{DD_GREEN}	In green mode.	--	120	160	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBIAS Section						
VBIAS Output Voltage	V_{BIAS}	I_{LOAD} = 15mA, V_{DD} > 6V	5.5	6	6.5	V
		I_{LOAD} = 5mA, 4.7V < V_{DD} < 6V	V_{DD} - 0.15	--	V_{DD}	
		I_{LOAD} = 5mA, V_{DD} < 4.7V, 9V < V_D < 130V, V_D duty > 20% at 200kHz. The power path for the SR driver is from the VD and cycle by cycle to detect VDD to change power source.	4.5	4.7	4.9	
VBIAS Load Regulation		1mA < I_{VBIAS} < 15mA (Continuance)	--	--	200	mV
VBIAS Output Short Circuit Current	I_{VBIAS_SC}		50	65	80	mA
SR Driver Section						
Output High Voltage	V_{OH_VG}	I_{SOURCE} = 20mA	V_{BIAS} - 0.3	--	V_{BIAS}	V
Output Low Voltage	V_{OL_VG}		--	--	0.5	V
Rise Time	t_{R_VG}	C_L = 4nF, V_G is from 1V to 4V	--	50	100	ns
Turn-On Propagation Time	t_{P_ON}	From trigger VTR falling edge to V_G = 0.1V	--	50	--	ns
Fall Time	t_{F_VG}	C_L = 4nF, from 80% x V_{OH_VG} to 1V	--	--	15	ns
Turn-Off Propagation Time	t_{P_OFF}		--	--	30	ns
Initial Output Low Clamping Voltage before Start-up	$V_{OL\_VG\_INI}$	C_{DG} = 330pF, C_{GS} = 27pF, VD is from 0V to 40V, t_R = 50ns, pulse width = 1μs (Note 5)	--	--	1.5	V
Internal Pull-Low Resistor	R_{GS_LOW}		70	100	130	kΩ
VD Section						
VD Resistor	R_{VD}		175	250	325	kΩ
VD Scaling Resistor	K_{VD}		49	50	51	--
VTR Sample and Hold Error	E_{SH_VTR}	(|V_{VTR_HIGH} - V_{VTR_SH}| / V_{VTR_HIGH}) x 100	--	--	5	%
VTR Sample and Hold Threshold	V_{VTR_SH}	V_{TH_SH} = K_{VTR_SH} x $V_{V\_TR\_HIGH}$[n-1]	0.665	0.7	0.735	--
Mask Time	t_{MASK}	V_{VTR} > V_{TH_SH}	200	300	400	ns
Initial VTR Blanking Time	$t_{BLANK\_VTR\_INI}$		0.35	0.45	0.55	μs
V_{IN} Low VTR Blanking Time	$t_{BLANK\_VTR\_VINL}$		1.04	1.2	1.36	μs
Low Level Threshold for Input Voltage	K_{VIN_LOW}	When V_{DS} < K_{VIN_LOW} x V_{DD}, VTR blanking time will be changed to V_{IN} low blanking time and minimum off time.	2	2.2	2.4	--
Low Level Threshold for VD Falling Edge Detection	$V_{LOW\_FALLING}$		–0.4	–0.3	–0.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Dead Time Comparison High Threshold	V_{TH_DT}		0.4	0.5	0.6	V
VG Fast Turn-Off Initial Threshold	$V_{TH\_VGOFF\_INI}$	For RT7220AMD, RT7220AHD, RT7220AHC and RT7220AHF (Note 5)	−13	−10	−7	mV
		For RT7220AHJ (Note 5)	−28	−25	−22	
Maximum VG Fast Turn-Off Limit for Tracking Up/Down	V_{VGOFF_MAX}	With 8-bit tracking control	18	20	22	mV
VG Fast Turn-Off Step Limit for Tracking Up/Down	ΔV_{VGOFF}	$V_{TH\_VGOFF}[n] = V_{TH\_VGOFF}[n-1] \pm \Delta V_{VGOFF}$	0.062	0.078	0.094	mV
Dead Time Comparator Delay		(Note 5)	--	--	40	ns
VD Falling Time Threshold for VG Trigger	$t_{VD\_FALLING}$	VD falling edge is from V_{VTR} = 0.7 x V_{VTR_SH} to V_D = $V_{LOW\_FALLING}$. If V_D falling time < $t_{VD\_FALLING}$ and disable VTR falling edge debouce time, VG is triggered when VD < $V_{LOW\_FALLING}$. For RT7220AMD, RT7220AHD, RT7220AHC and RT7720AHJ (Note 5)	100	150	200	ns
		For RT7220AHF (Note 5)	170	200	230	ns
VD Edge Threshold for Exit Green Mode Detection	V_{VD_EDGE}		−0.4	−0.3	−0.2	V
Debounce Time for Exit/Enter Green Mode Detection	t_{VD_EDGE}		9	10	11	ms
VD Cycle Number for Enter Green Mode	N_{ENGR}	If the number of VG pulses in t_{VD_EDGE} is less than N_{ENGR}.	--	32	--	--
VD Cycle Number for Exit Green Mode	N_{EXGR}	If the number of VD pulses in t_{VD_EDGE} is more than N_{EXGR}.	--	64	--	--
VD UVP Trigger Voltage	VD_UVP	For RT7220AHC (Note 5)	--	--	V_{DD} + 3.5	V
		For RT7220AMD, RT7220AHD, RT7220AHF and RT7720AHJ (Note 5)	--	--	V_{DD} + 7	
SR Control Section						
VG Minimum On Time	t_{MINON_VG}	From VG rising edge to VG falling edge. For RT7220AMD (Note 5)	1200	1500	1800	ns
		From VG rising edge to VG falling edge. For RT7220AHD and RT7220AHF (Note 5)	710	890	1070	
		From VG rising edge to VG falling edge. For RT7220AHC and RT7720AHJ (Note 5)	400	500	600	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Disable VG Minimum ON Time Threshold	V_{MINON_DIS}	When $V_D > V_{MINON\_DIS}$ during t_{MINON_VG}, VG will be disabled immediately.	0.4	0.5	0.6	V
Initial VG Minimum OFF Time	$t_{MINOFF\_VG\_INI}$	From VG falling edge to next VG rising edge. For RT7220AMD, RT7220AHD, RT7220AHF and RT7720AHJ (Note 5)	0.39	0.45	0.51	µs
		From VG falling edge to next VG rising edge. For RT7220AHC (Note 5)	0.25	0.3	0.35	
V_{IN} Low VG Minimum OFF Time	$t_{MINOFF\_VG\_VINL}$	From VG falling edge to next VG rising edge. For RT7220AMD, RT7220AHD, RT7220AHF and RT7720AHJ (Note 5)	1.68	1.95	2.22	µs
		From VG falling edge to next VG rising edge. For RT7220AHC (Note 5)	0.9	1.05	1.2	
Automatic Tracking Section						
Auto-Tracking Dead Time	t_{DEAD_TRACK}	From VG falling edge to VD = $V_{TH\_HIGH\_DT}$	90	100	110	ns

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

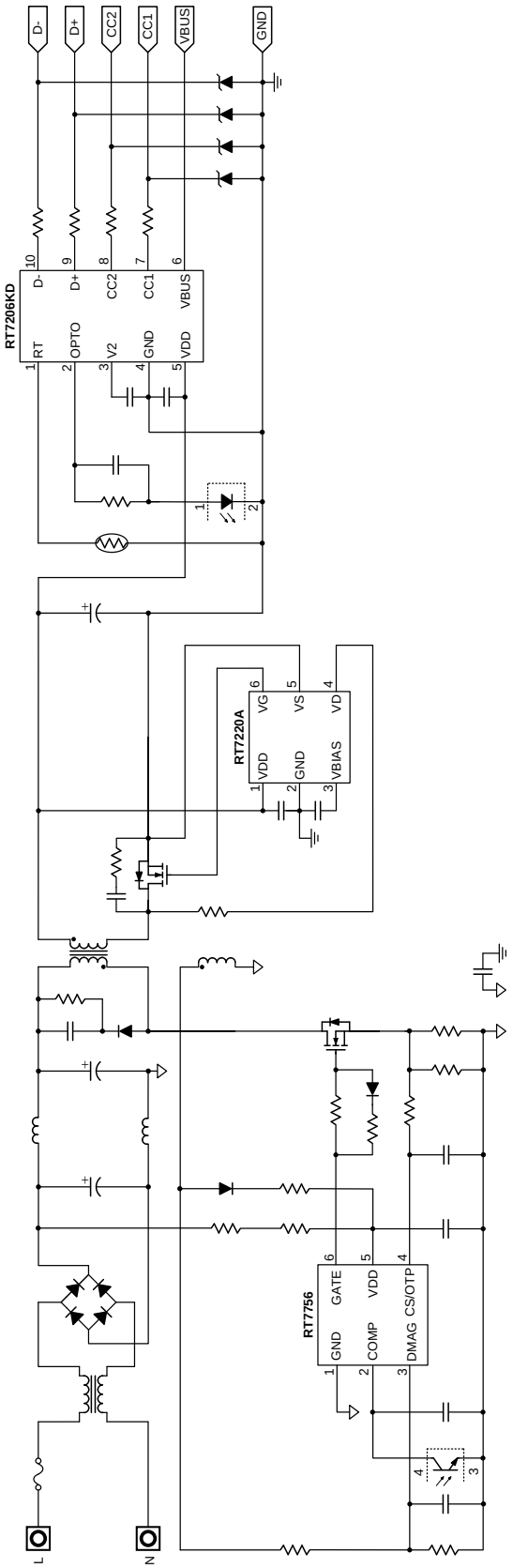
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

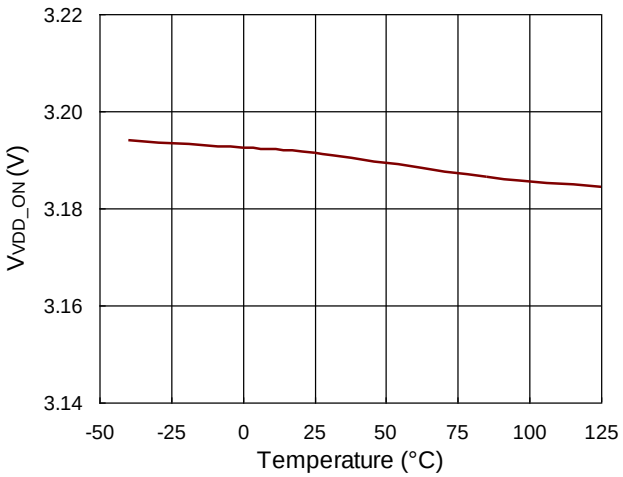
Note 5. Guaranteed by design.

Typical Application Circuit

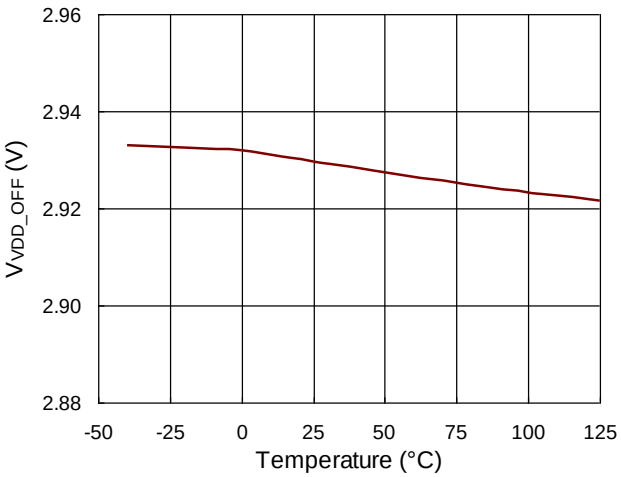


Typical Operating Characteristics

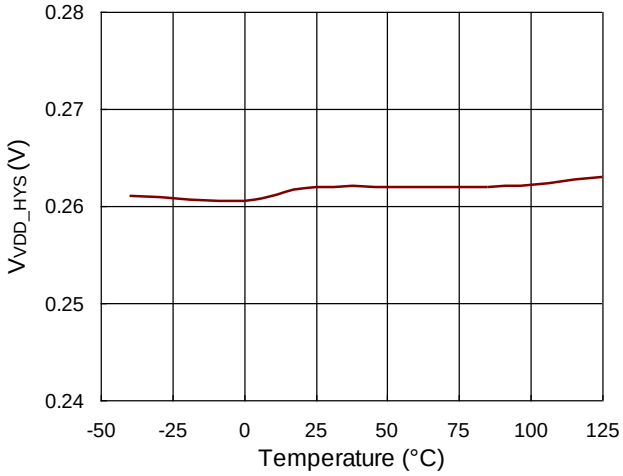
V_{VDD_ON} vs. Temperature



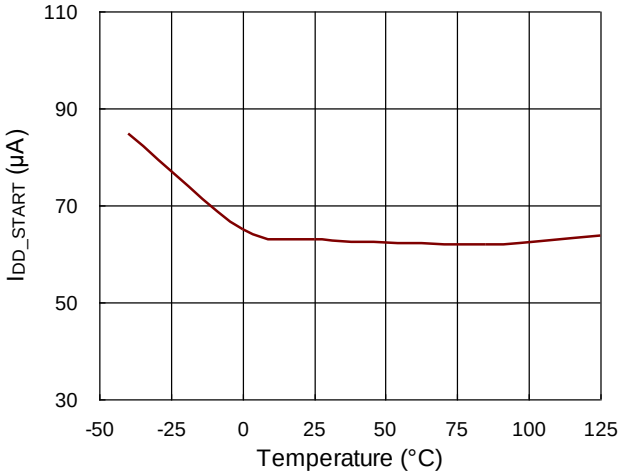
V_{VDD_OFF} vs. Temperature



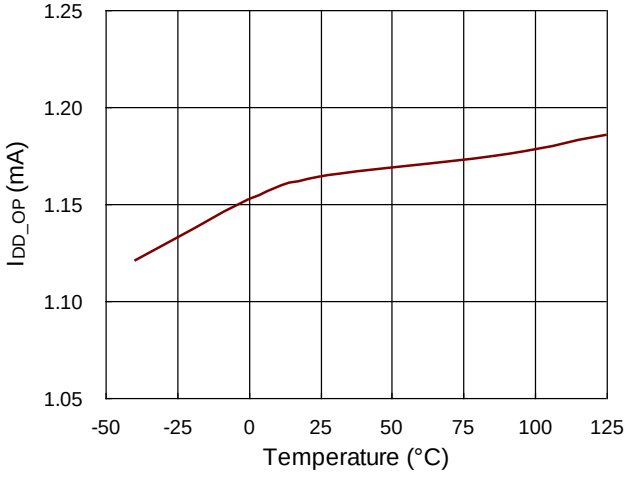
V_{VDD_HYS} vs. Temperature



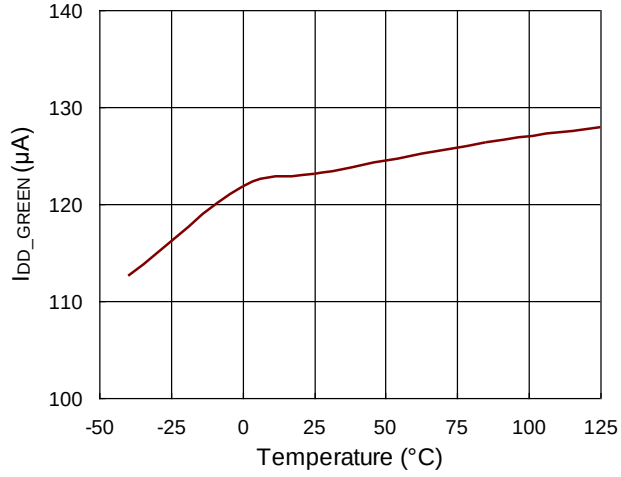
I_{DD_START} vs. Temperature



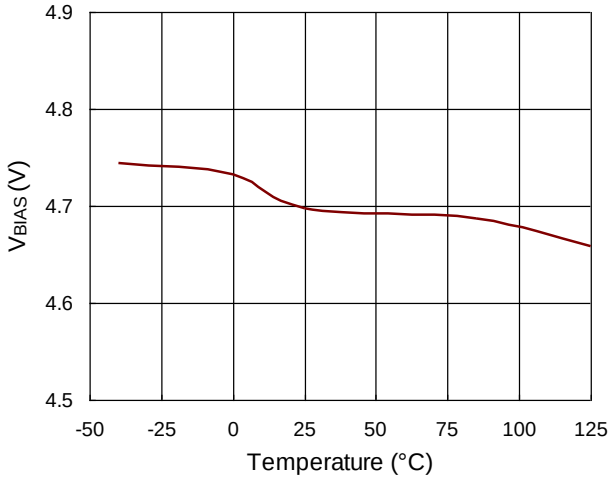
I_{DD_OP} vs. Temperature



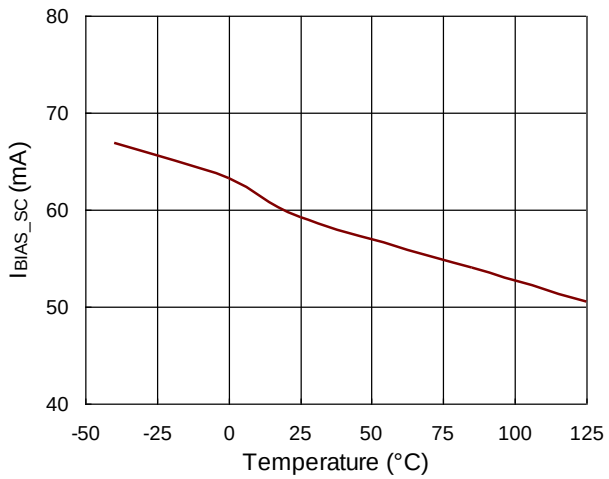
I_{DD_GREEN} vs. Temperature



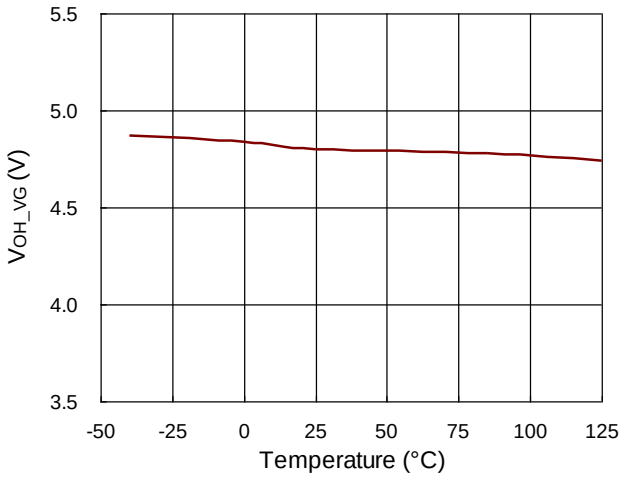
V_{BIAS} vs. Temperature



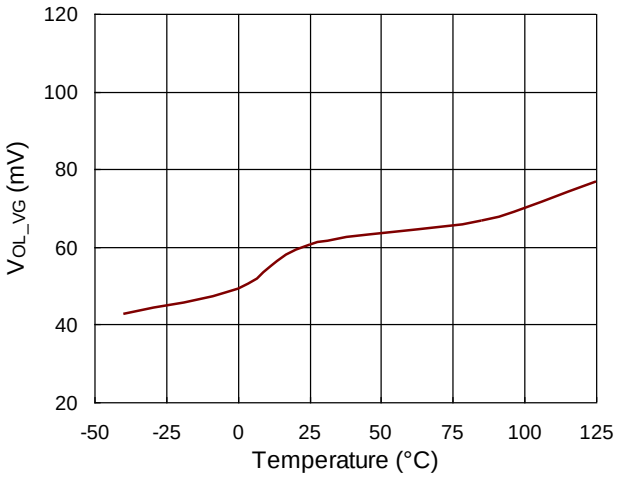
I_{BIAS_SC} vs. Temperature



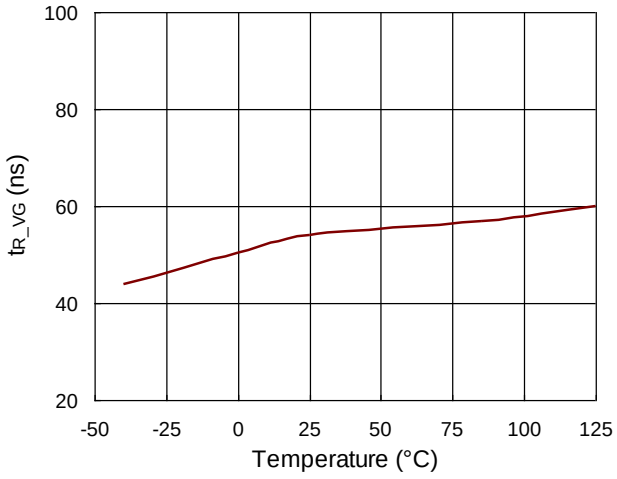
V_{OH_VG} vs. Temperature



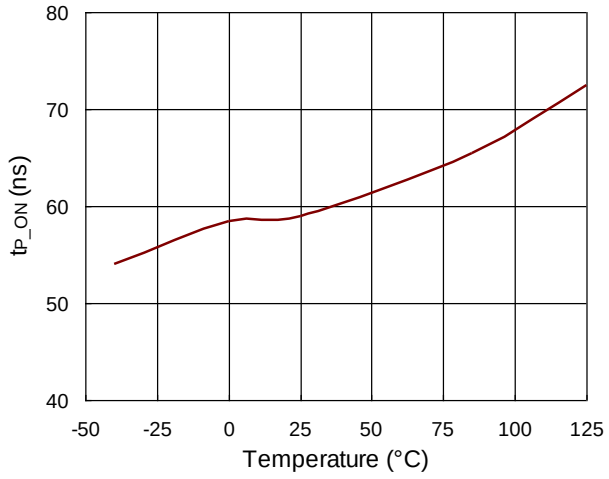
V_{OL_VG} vs. Temperature

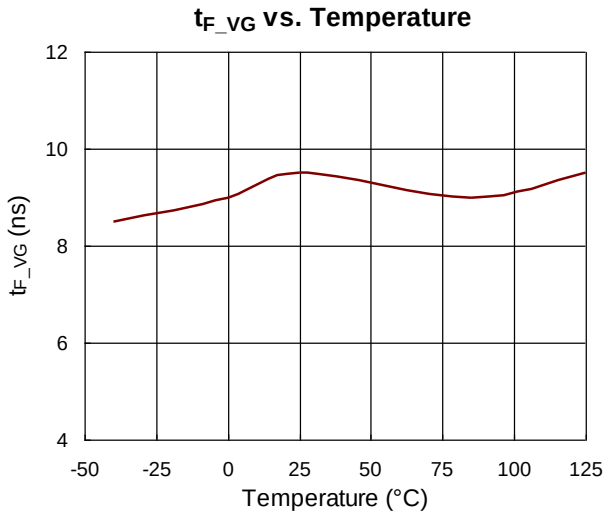


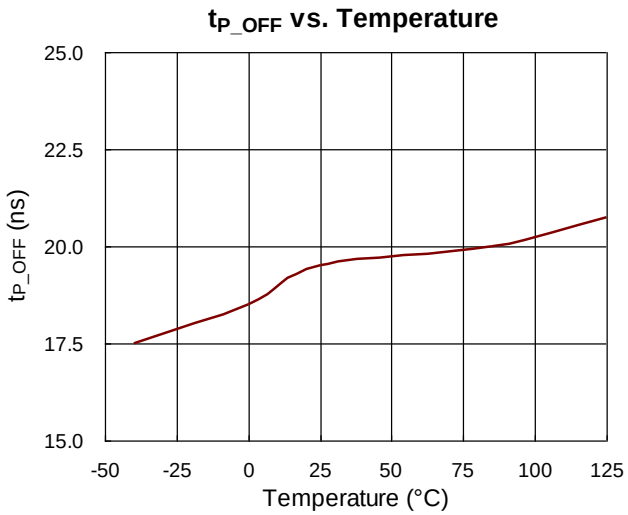
t_{R_VG} vs. Temperature

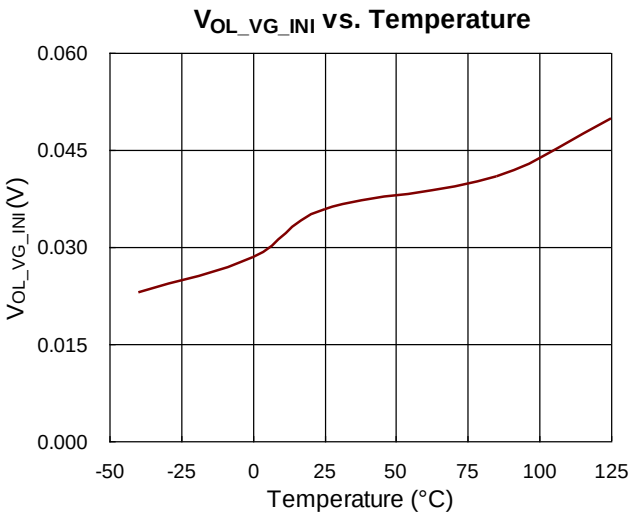


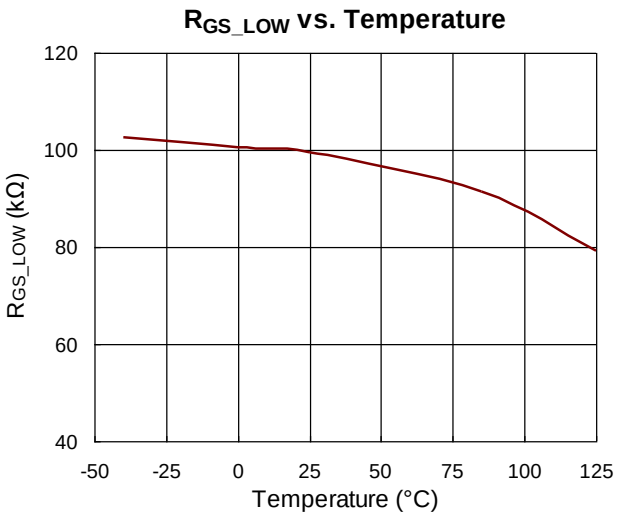
t_{P_ON} vs. Temperature

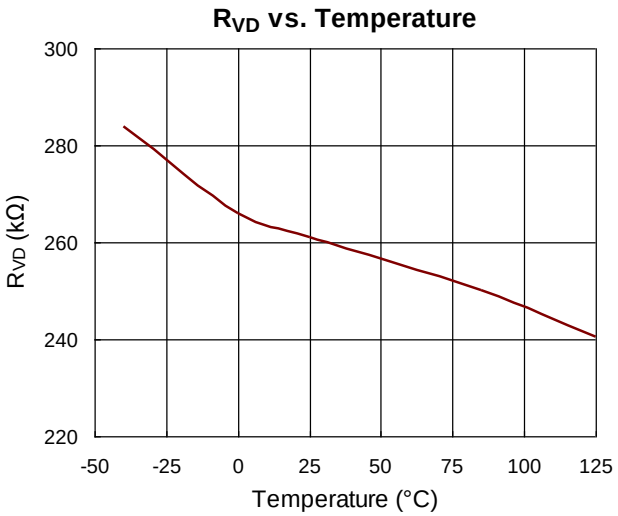


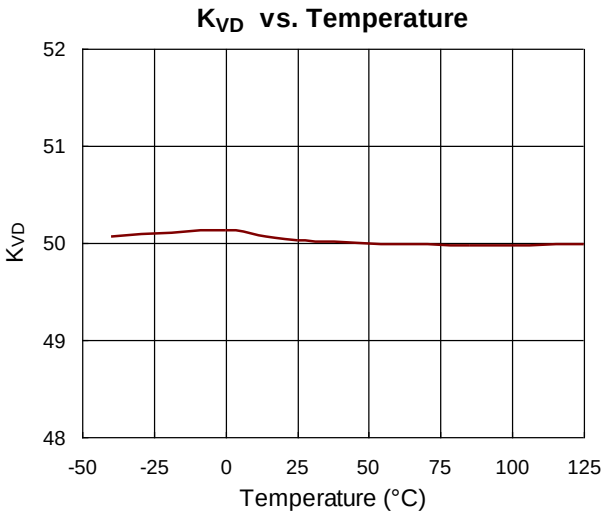




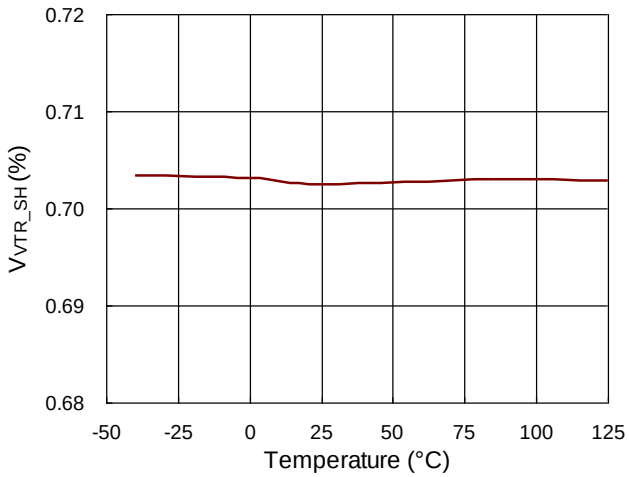




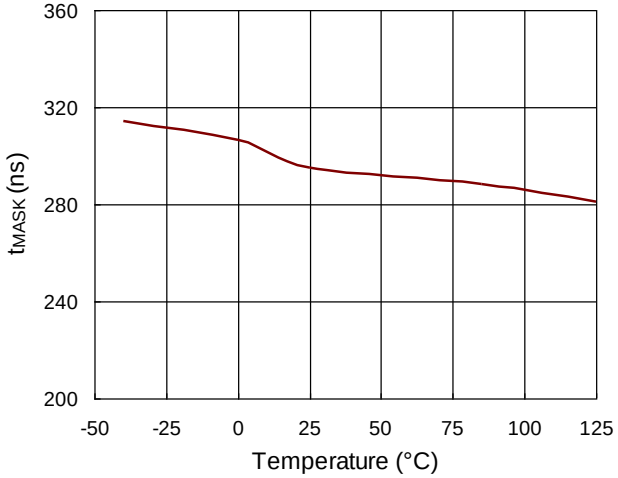




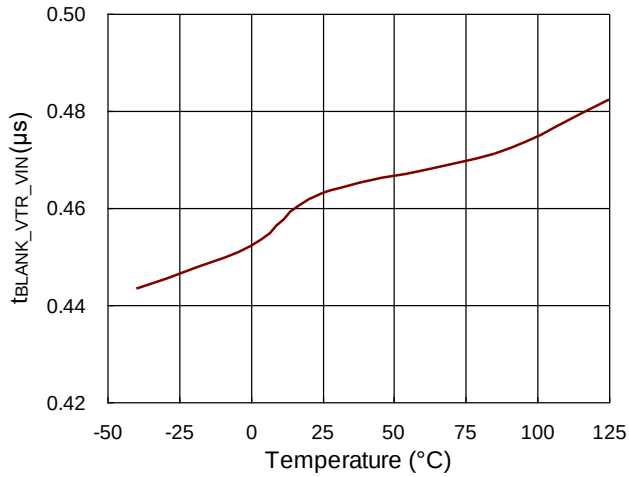
V_{VTR_SH} vs. Temperature



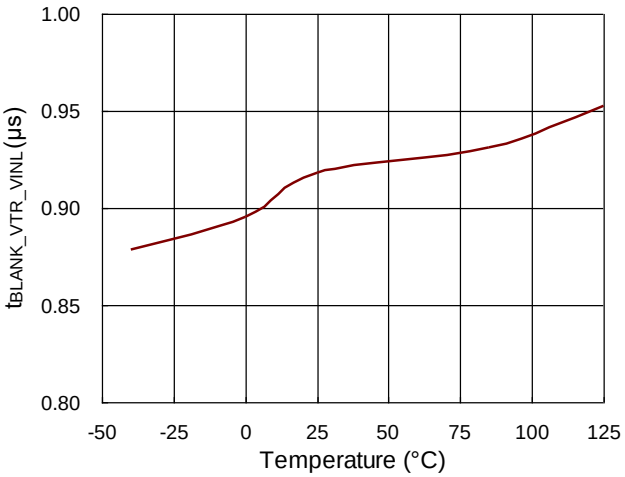
t_{MASK} vs. Temperature



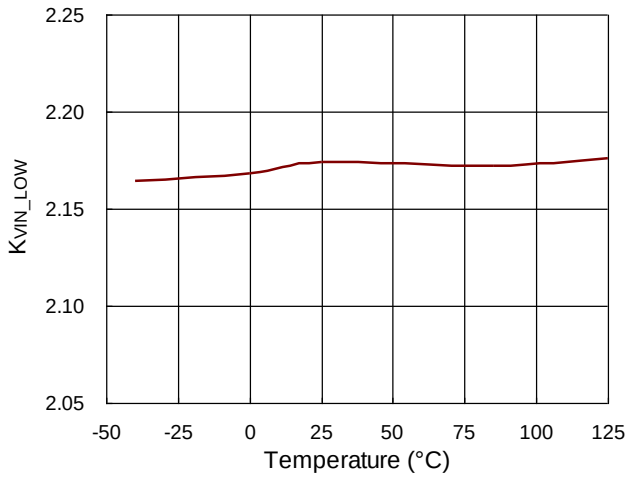
$t_{BLANK\_VTR\_VIN}$ vs. Temperature



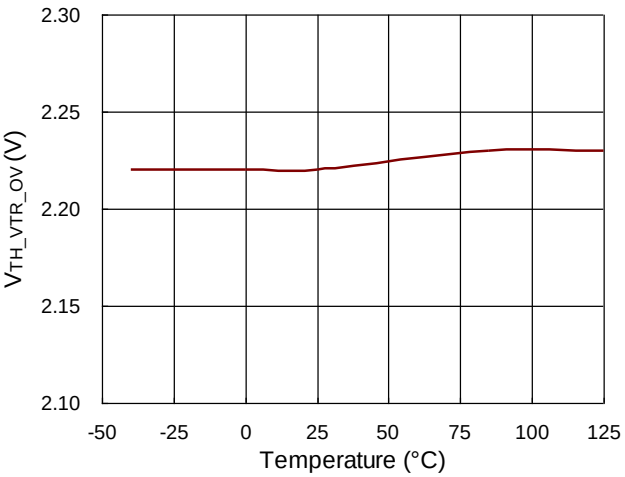
$t_{BLANK\_VTR\_VINL}$ vs. Temperature



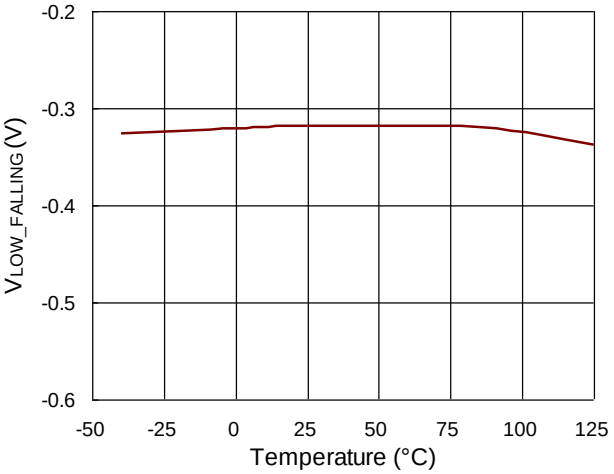
K_{VIN_LOW} vs. Temperature



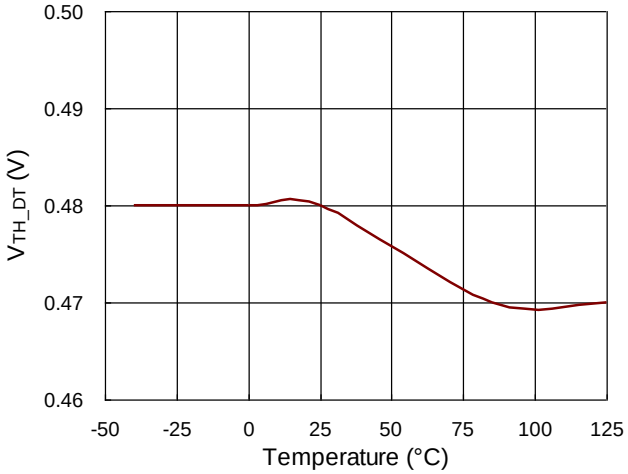
$V_{TH\_VTR\_OV}$ vs. Temperature



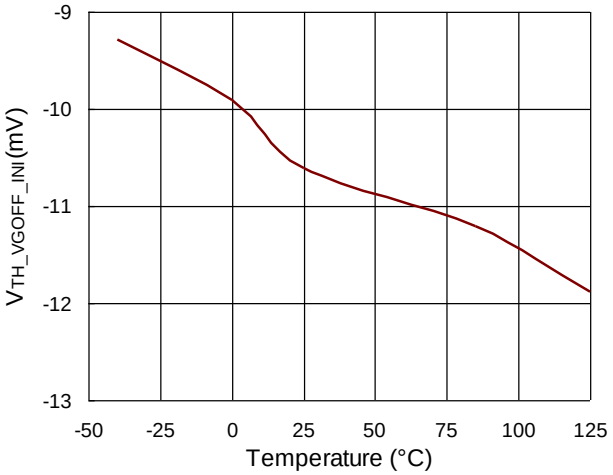
$V_{LOW\_FALLING}$ vs. Temperature



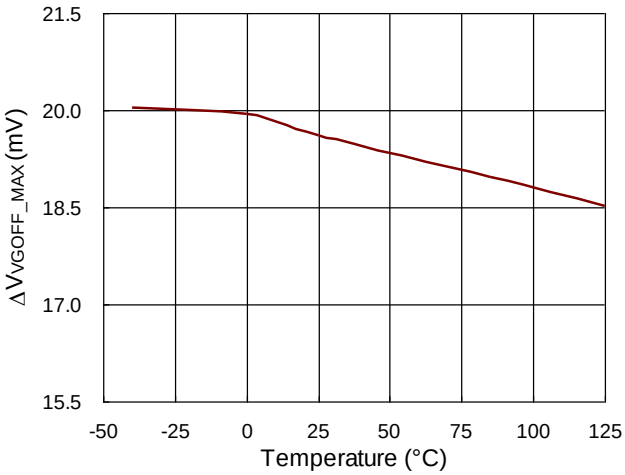
V_{TH_DT} vs. Temperature



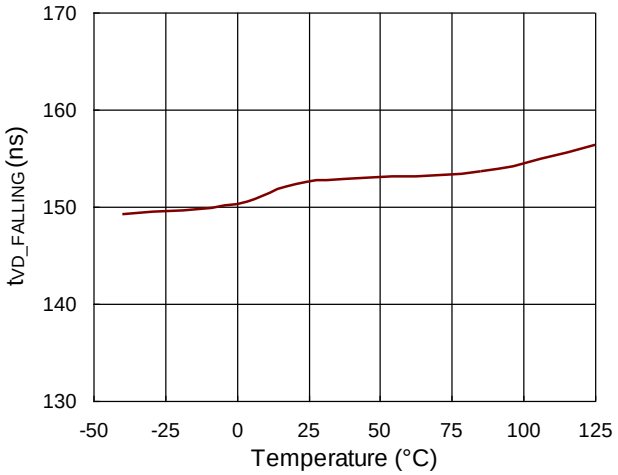
$V_{TH\_VGOFF\_INI}$ vs. Temperature



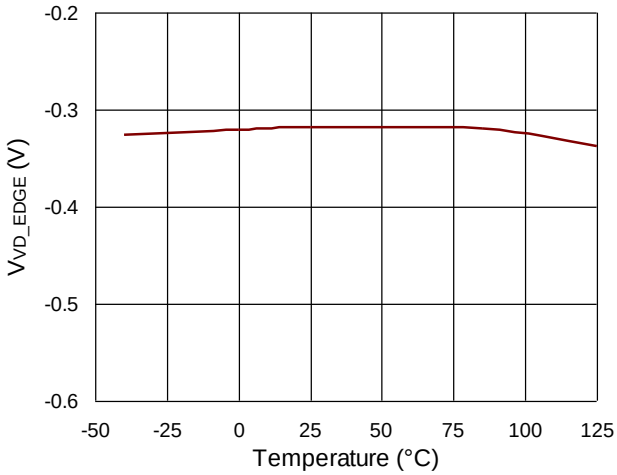
ΔV_{VGOFF_MAX} vs. Temperature



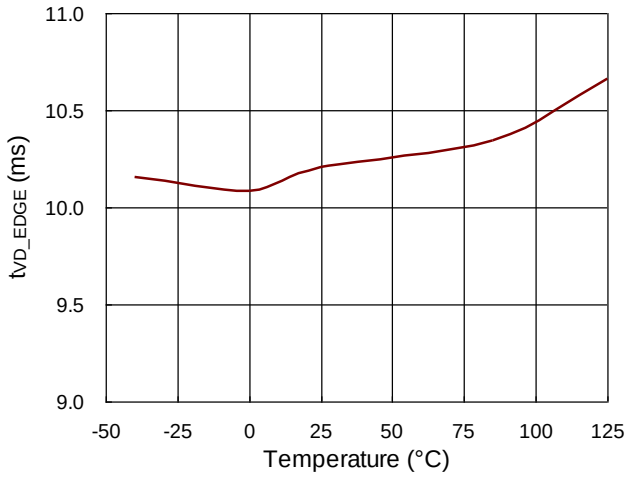
$t_{VD\_FALLING}$ vs. Temperature



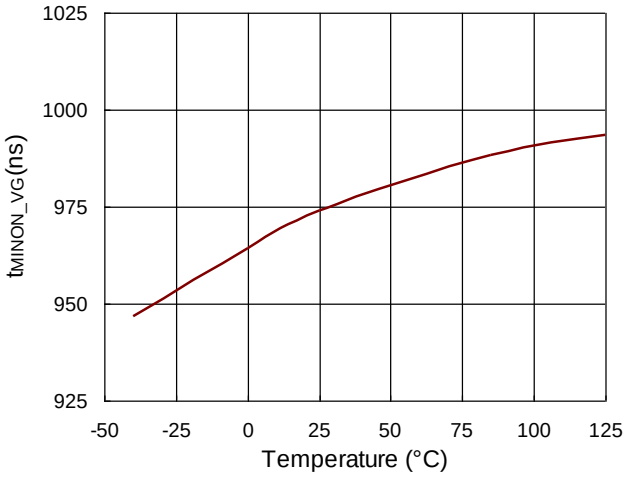
V_{VD_EDGE} vs. Temperature



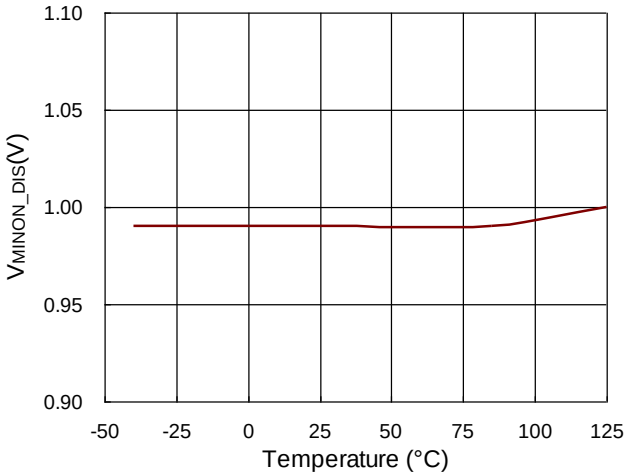
t_{VD_EDGE} vs. Temperature



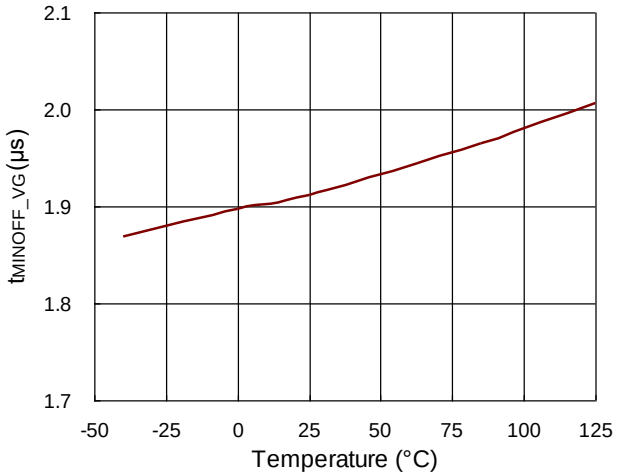
t_{MINON_VG} vs. Temperature



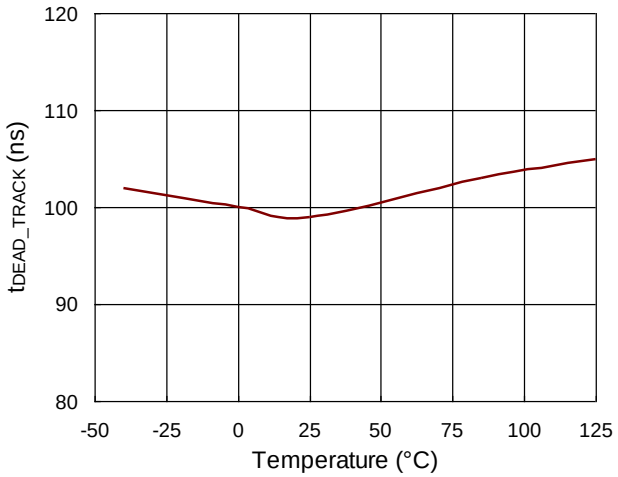
V_{MINON_DIS} vs. Temperature



t_{MINOFF_VG} vs. Temperature



t_{DEAD_TRACK} vs. Temperature



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

Power Selection

The RT7220A provides a wide output voltage range of 3V to 22V, of which a VDD pin can be directly connected to the power output of a converter. In addition, a HV LDO is built-in to supply the gate drive VG for the MOSFET. It is designed in a way that when the VDD is lower than 4.7V, the VG voltage powered by the VBIAS will be clamped to 4.7V at lower output voltage, as shown in Figure1. When the VDD is higher than 4.7V, the VG voltage which is then powered by the VDD will increase as VDD voltage increases. Once VDD is higher than 6V, the VG voltage will be clamped at 6V to prevent the slower turn-off time.

Moreover, the RT7220A provides the initial clamp function to avoid SR MOSFET gate being falsely turned-on by the parasitic capacitance during start-up.

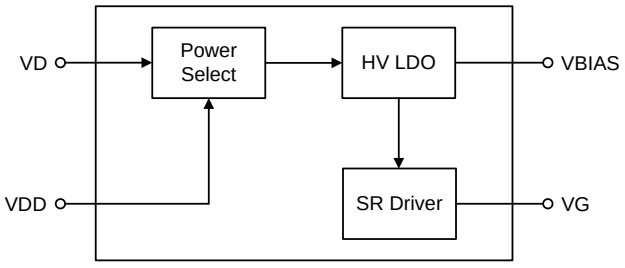


Figure 1. Power Selection Circuit

VG Turn-On

VG is turned-on under the condition when VD voltage is falling during the period (<$t_{VD\_FALLING}$).

Simultaneously, at the same time a current flows through the body diode of the MOSFET, and a negative voltage ($V_{LOW\_FALLING}$) of V_{DS} as shown in Figure 2.

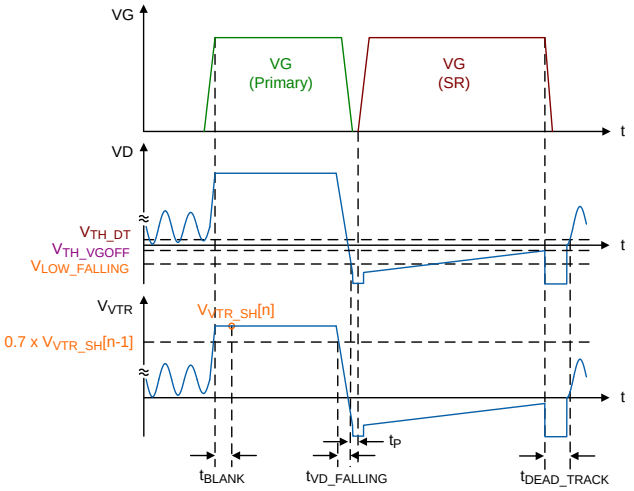


Figure 2. SR Turn-On/Off

VG Turn-Off

The turn-off of VG is triggered when the VDS voltage rises to reach the turn-off threshold (V_{TH_VGOFF}) after a short delay shown in Figure 3. Furthermore, the RT7220A provides the reliable operation and high efficiency in CCM control by minimizing the turn-off dead-time, which is accomplished by modulating the turn-off threshold cycle-by-cycle so as to close to tacking dead-time. However, considering the MOSFET parasitic capacitor variation, and resister (or inductance) delay from gate driver circuit (t_{VGOFF_delay}), which is shown as Figure 4, should be smaller than minimum tracking dead-time 50%.

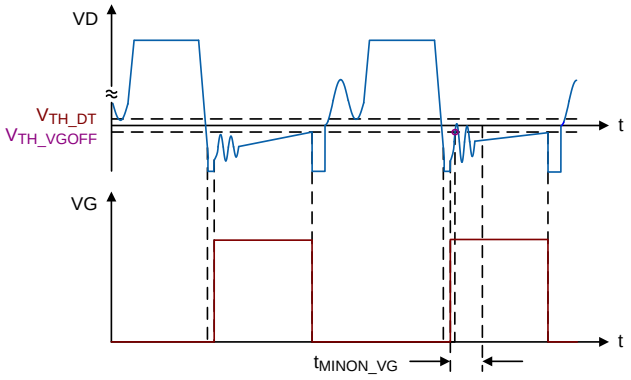


Figure 3. VG Minimum On-Time

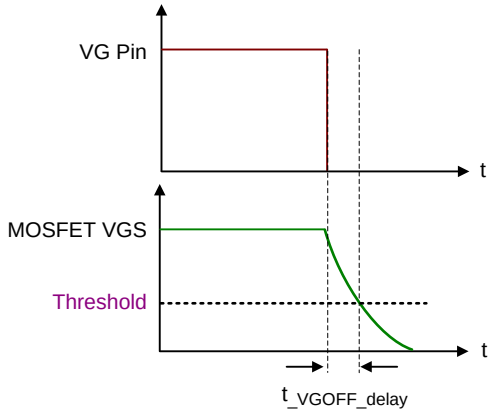


Figure 4. VG Turned Off Delay Time

VG Minimum On-Time

The RT7220A provides a function to prevent an accidental turn-off due to ringing, during this period when the turn-off threshold is blanked, as shown in Figure 3. In normal case, the minimum turn-on time (t_{MINON_VG}) 1μs is suggested.

VG Minimum Off-Time

During the falling edge of VG, the minimum off-time timer is initiated and the turn-on of the SR is avoided until minimum off-time (t_{MINOFF_VG}) expires. This eliminates false turn-on of VG, caused by the DCM ringing, as shown in Figure 5.

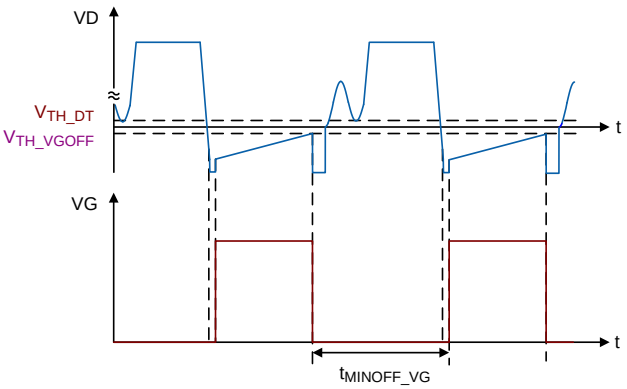


Figure 5. VG Minimum Off-Time

Green Mode Operation

For improving the efficiency in light load conditions, the RT7220A features a green mode operation that disables the SR MOSFET and reduces the device operation current. This operation mode is determined by detecting the numbers of VD and VG pulse respectively.

If VG pulse is less than 32 cycles in t_{VD_EDGE}, the device disables the VG output and enters green mode, as shown in Figure 6.

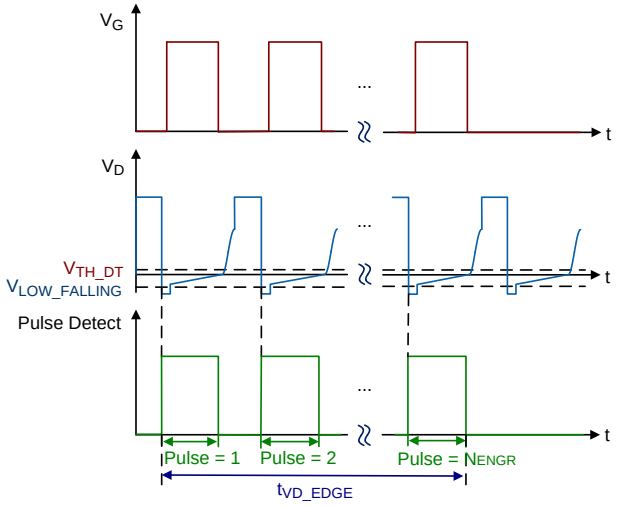


Figure 6. Entry Green Mode

Once VD pulse is more than 64 cycles in the period of t_{VD_EDGE}, the RT7220A exits from green mode and resumes normal operation immediately, as shown in Figure 7.

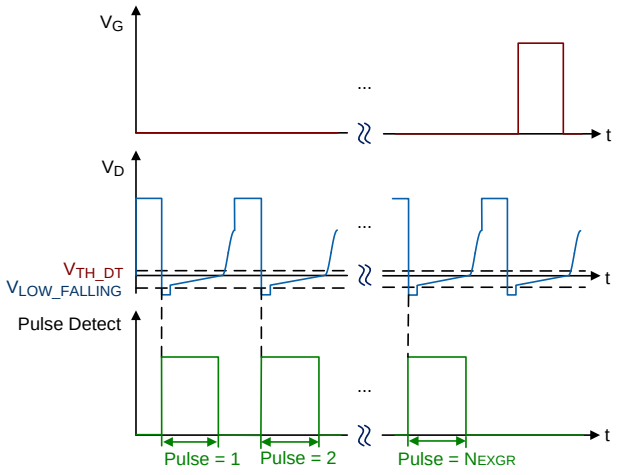


Figure 7. Exit Green Mode

VD UVP

The VD signal is related to Vin by transformer turn ratio and VDD. However, if VD is lower than VD_UVP, the VG signal will not be triggered as shown in Figure 8.

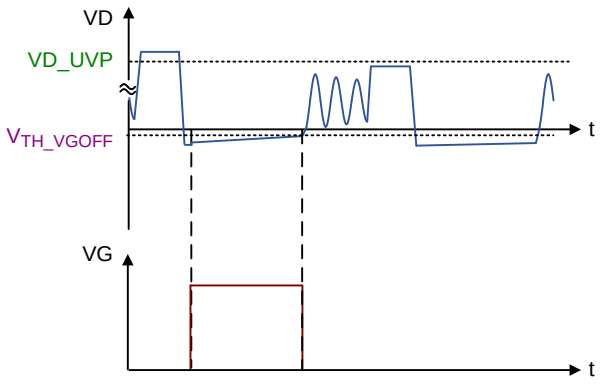


Figure 8. VD UVP

System VD Falling Time Design Note

VD falling time is determined by parasitic capacitor from primary and secondary side, and also influenced by magnetizing current. Figure 9 shows the measurement waveform; the worst VD falling time happens with minimum I_{peak} condition. For RT7220A to precisely trigger VG signal, and considering internal comparator delay time, it is strongly suggested that system VD falling time, $t_{SYS\_VD\_FALLING}$, should be at least 30ns smaller than $t_{VD\_FALLING}$ (typ.).

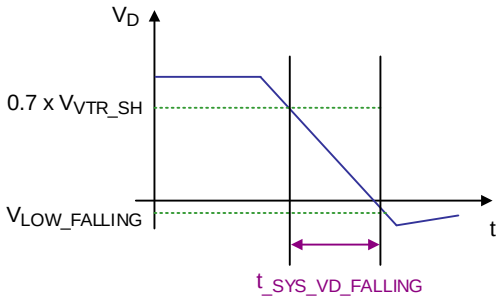


Figure 9. VD Falling Time Measurement Waveform

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is normally 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOT-23-6 package, the thermal resistance, θ_{JA}, is 260.7°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (260.7°C/W) = 0.38W for a SOT-23-6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 10 allows the designer to inspect the effect of rising ambient temperature on the maximum power dissipation.

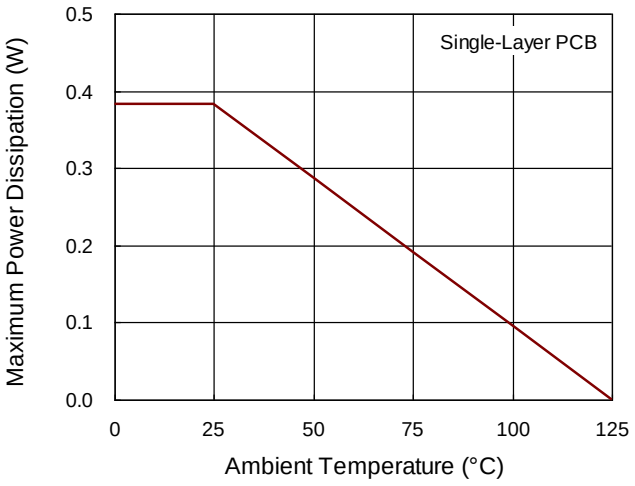
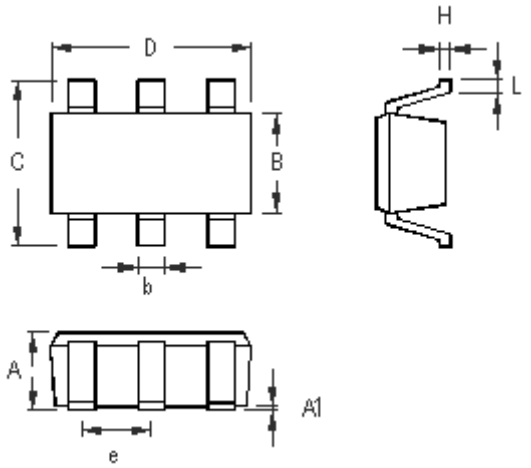


Figure 10. Derating Curve of Maximum Power Dissipation

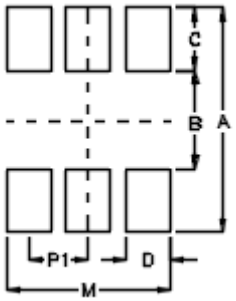
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

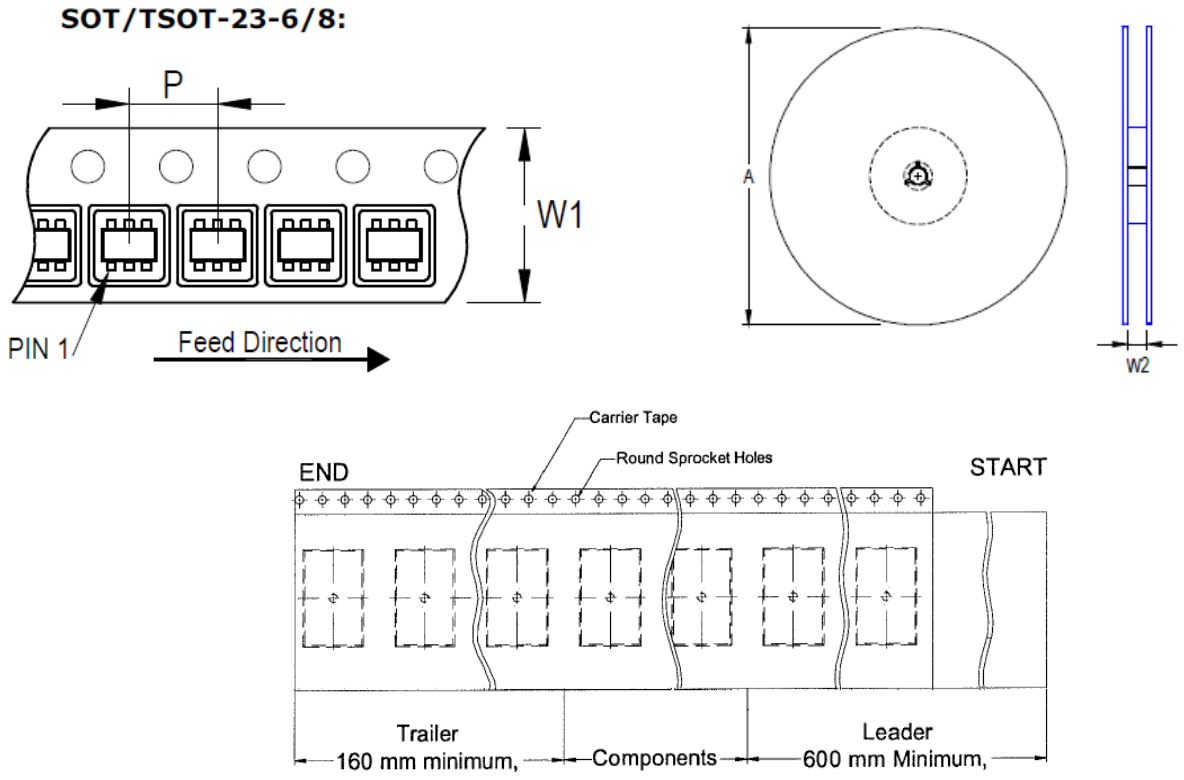
Footprint Information



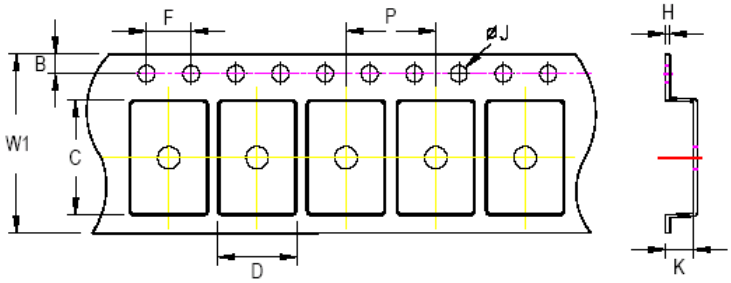
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-26/TSOT-26(FC)/SOT-26	6	0.95	3.60	1.60	1.00	0.70	2.60	±0.10

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOT/TSOT-23-6	8	4	180	7	3,000	160	600	8.4/9.9



C, D and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
SOT/TSOT-23-6	7”	3,000	Box A	18.3*18.3*8.0	3	9,000	Carton A	38.3*27.2*38.3	12	108,000
			Box E	18.6*18.6*3.5	1	3,000	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
05	2023/4/27	Modify	Electrical Characteristics on P6 Application Information on P15
06	2023/7/27	Modify (Added RT7220AHF)	Ordering Information on P1 Marking Information on P2 RT7220A Version Table on P2 Electrical Characteristics on P6, 7 Application Information on P15, 17 Packing Information on P20, 21, 22
07	2023/10/20	Modify (Added RT7220AHJ)	General Description on P1 Marking Information on P2 RT7220A Version Table on P2 Electrical Characteristics on P6, 7