RICHTEK®

RT7209

Programmable USB PD Controller for Extended Power Range

1 General Description

The RT7209 is a highly integrated programmable controller, featuring internal feedback compensation and a V5 (regulated voltage for internal MCU).

Its wide operation voltage range, from 3.3V to 53V, supports USB PD3.1 SPR and EPR 48V specifications.

An internal MCU is designed to meet standard USB PD protocols, Universal Fast Charging Specification (UFCS) and proprietary protocols. This controller is a specifically designed for off-line AC-DC converters to achieve high power density in fast charge systems. The built-in feedback compensation not only reduces the need for external components but also enhances the transient response. For safety considerations, the RT7209 provides comprehensive protections.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

2 Ordering Information

RT7209□□□-□

- **Programmed Firmware Code AABBX**
  AA: Application Code
  BB: Model Code
  X: Customer Approved Version Code
- **Package Type**(1)
  QW: WQFN-28L 4x5 (W-Type)
  (Exposed Pad: Option 1)
- **Lead Plating System**
  G: Richtek Green Policy Compliant(2)
- **Application Code**
  (Refer to Version Table)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **Protocol Support**
  - **USB PD3.1 SPR, PPS, EPR and AVS**
  - **Universal Fast Charging Specification (UFCS)**
  - **Proprietary Protocols**
- **Suited for 3.3V to 53V V_{VDD} Range**
- **Embedded MCU with an OTP-ROM of 16kB, and an SRAM of 2kB**
- **Built-In Shunt Regulators for Constant Voltage and Constant Current Control**
- **Built-In Feedback Compensation**
- **Built-In V_{CONN} Power (100mW)**
- **The BLD Pin for Quick Discharge of Output Capacitor**
- **Support Programmable Cable Compensation**
- **Support VIN (Vbulk) Detection**
- **The USBP Pin for Direct Drive of External Blocking N-MOSFET**
- **Power-Saving Mode in Standby Mode**
- **Protection**
  - **Adaptive Output Overvoltage Protection**
  - **Adaptive Output Undervoltage Protection**
  - **CC1/CC2/D+/D- Overvoltage Protection**
  - **Programmable Overcurrent Protection**
  - **Programmable Constant Current Protection**
  - **Programmable Over-Temperature Protection**
  - **Internal Over-Temperature Protection**

4 Applications

- USB Type-C PD Controller in Source Application for Chargers/Adapters of Smartphone, Tablet, Notebook, and Other Electronics

5 Marking Information

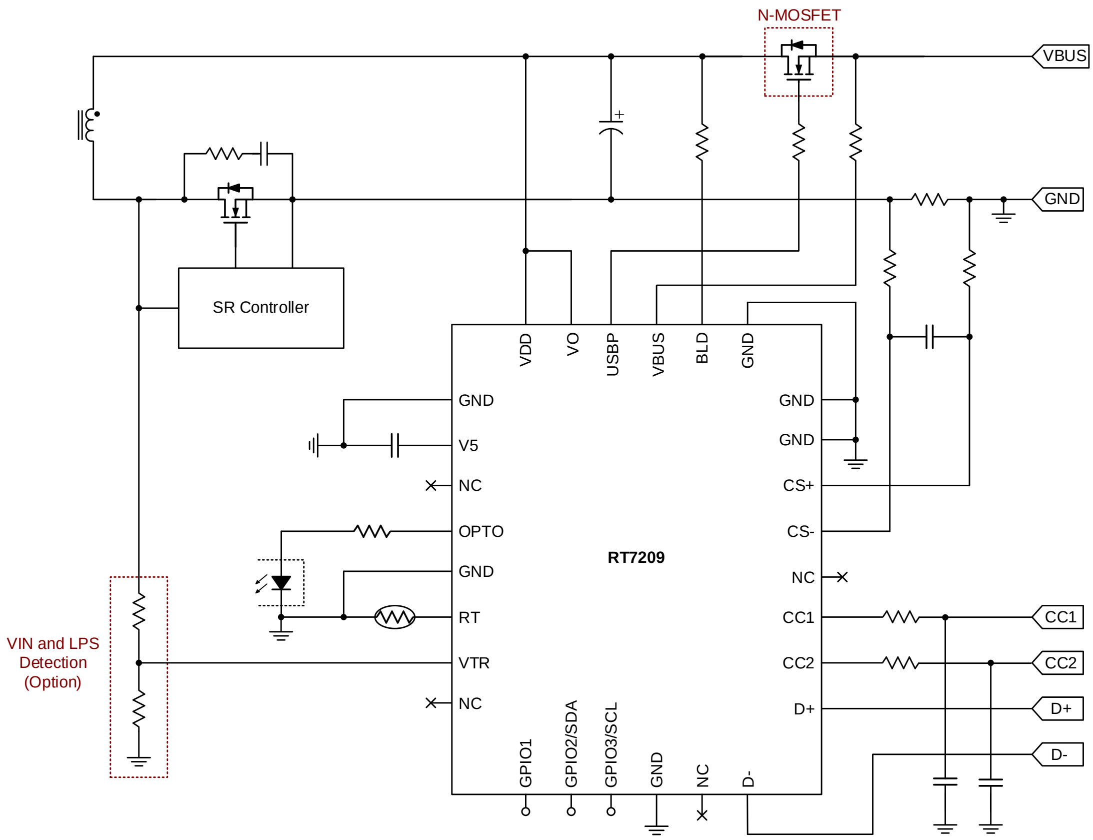
For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 RT7209 Version Table

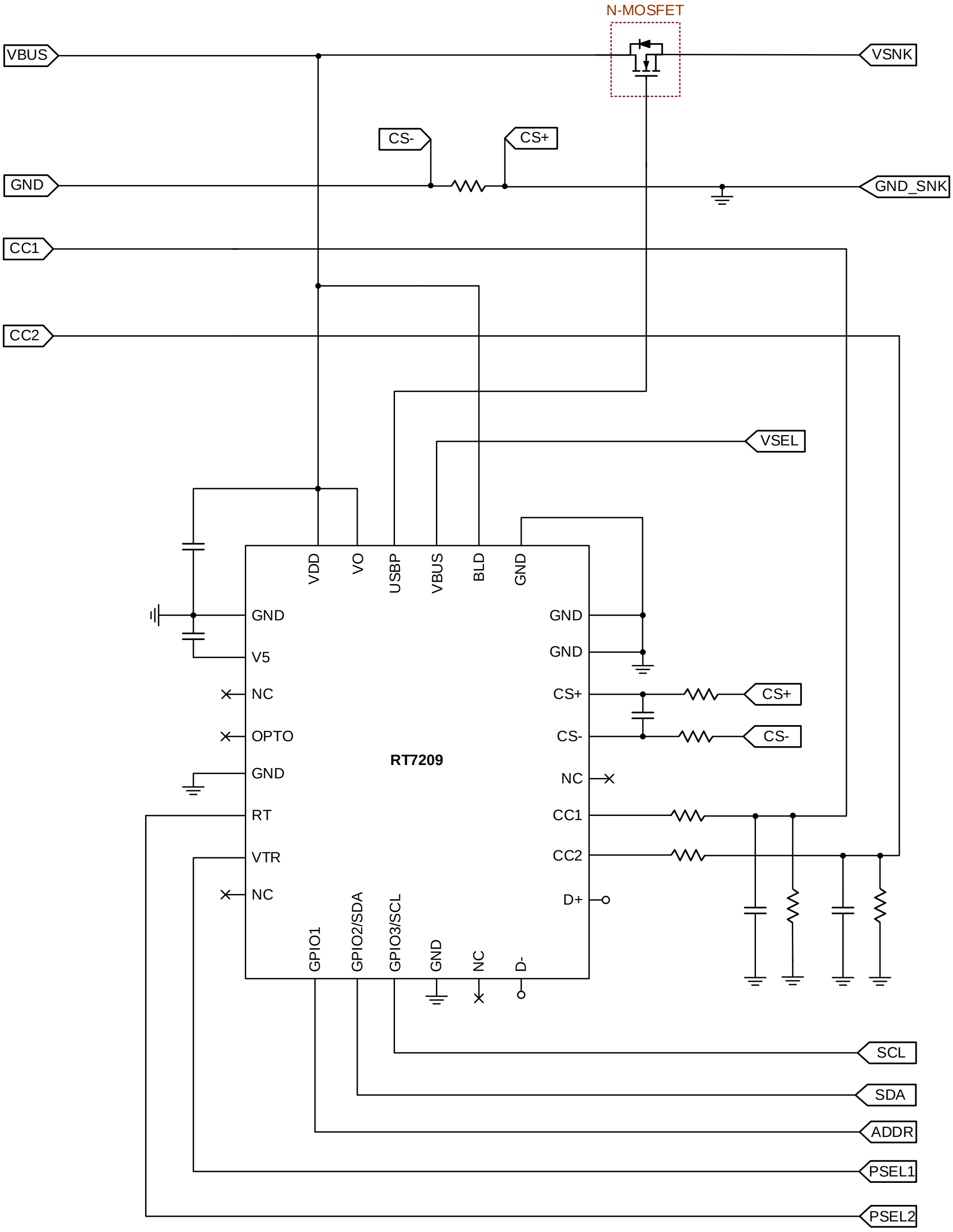
Part Number	RT7209GQW		RT7209BGQW	
VBUS Drop	Yes		No	
USBP Clamp	Yes		No	
USBP Pull-Low Resistance when USBP is Turned Off	6.8kΩ		5kΩ	
USBP Pull-Low Resistance during VDD UVLO	6.8kΩ		5kΩ	
RT/GPIO23 Register-Programmable Internal Bias Current	00	100μA	00	Open
	01	20μA	01	5μA
	10	5μA	10	20μA
	11	Open	11	100μA
Output Voltage Supported	3.3V to 53V			
V_{OUT} Scaling Factor (R_{FB1} + R_{FB2}) / R_{FB2}	10 (For SPR)			
	25 (For EPR)			
Built-In FB Resistors	Yes			
Blocking MOSFET Driver	N-MOSFET			
Package	WQFN-28L 4x5			

7 Simplified Application Circuit

7.1 Simplified Circuit in Source Application



7.2 Simplified Circuit in Sink Application



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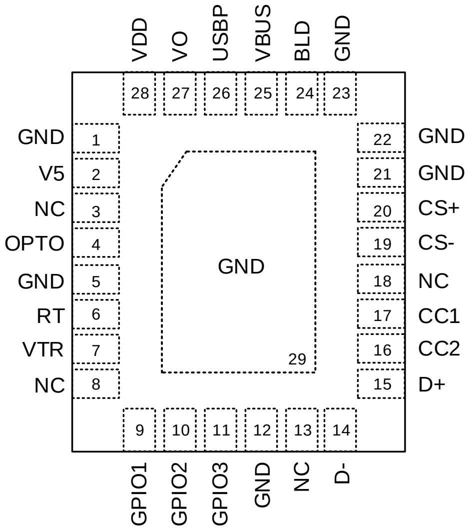
8 Pin Configuration

(TOP VIEW)



WQFN-28L 4x5

9 Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1, 5, 12, 21, 22, 23	GND	GND	Ground.
2	V5	PWR	Regulated DC bias supply for internal circuitry.
3, 8, 13, 18	NC	NC	No internal connection.
4	OPTO	AO	Current source output for optocoupler connection. Can be configured as an ADC input.
6	RT	A/D IO	Remote thermal sensor connection node for over-temperature protection. Can be configured as a sourcing current output and an ADC input.
7	VTR	AI	Transformer voltage sense node for VIN (bulk voltage) detection. Can be configured as a sourcing current output and an ADC input.
9	GPIO1	A/D IO	General purpose input/output. Can be configured as an open-drain output, a sourcing current output, and an ADC input.
10	GPIO2	A/D IO	General purpose input/output. Can be configured as I^2C-SDA, UART_TX/UART_RX, an open-drain output, a sourcing current output, and an ADC input. (Note 2)
11	GPIO3	A/D IO	General purpose input/output. Can be configured as I^2C-SCL, UART_TX/UART_RX, an open-drain output, a sourcing current output, and an ADC input. (Note 2)
14	D-	A/D IO	USB D- channel, for BC1.2 and proprietary protocols. Can be configured as I^2C-SDA, UART_TX/UART_RX, and an ADC input. (Note 2)
15	D+	A/D IO	USB D+ channel, for BC1.2 and proprietary protocols. Can be configured as I^2C-SCL, UART_TX/UART_RX, and an ADC input. (Note 2)

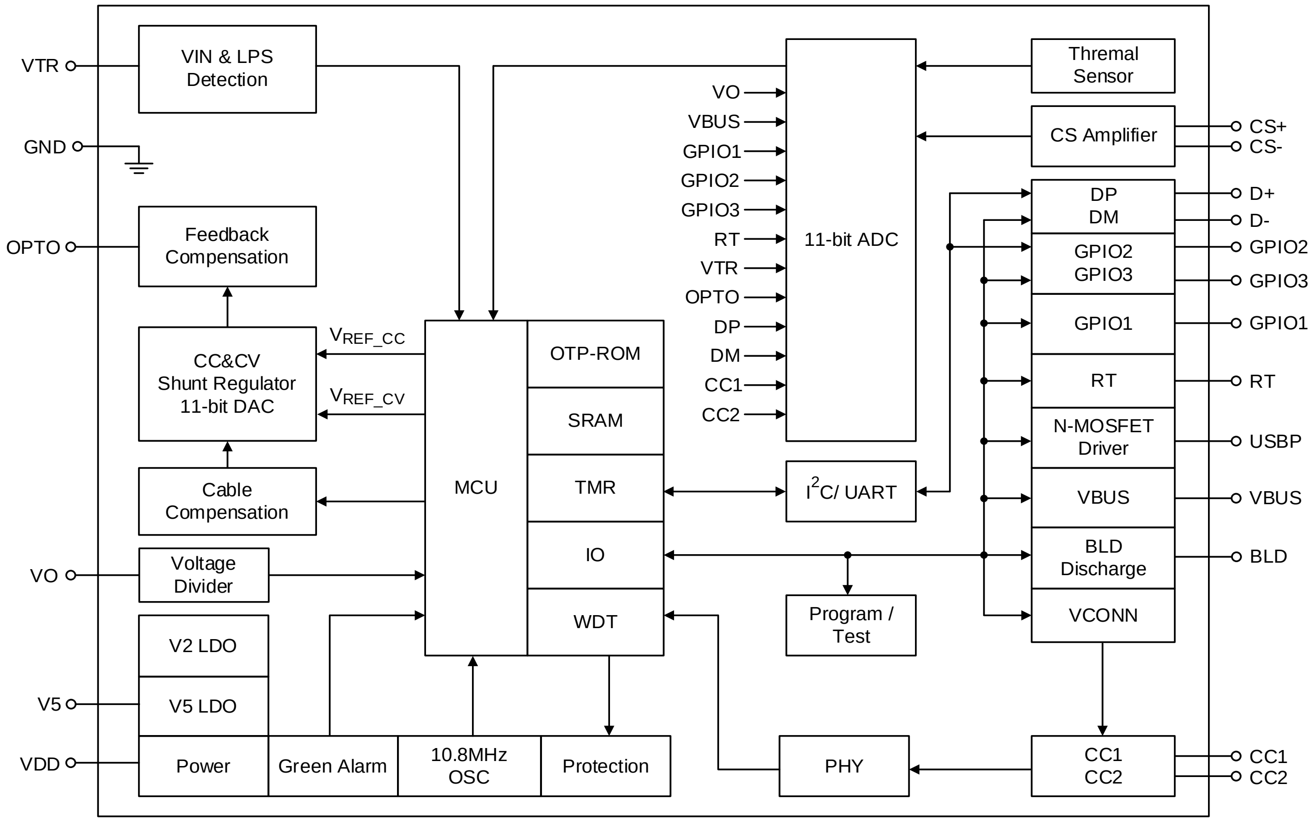
Pin No.	Pin Name	Type	Pin Function
16	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation. Can be configured as an ADC input.
17	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation. Can be configured as an ADC input.
19	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
20	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
24	BLD	AO	Bleeder connection node to provide the path to discharge the output capacitor.
25	VBUS	A IO	VBUS sensing and bleeder connection node to provide the path to discharge the VBUS capacitor. Can be configured as an ADC input.
26	USBP	D IO	Control signal of the blocking N-MOSFET.
27	VO	AI	VOUT connection node. Can be configured as an ADC input.
28	VDD	PWR	Supply input voltage.
29 (Exposed Pad)	GND	GND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

Note 2. The RT7209 has one set of UART and I^2C. The MUX can be configured through the MCU to select the connection to either GPIO2/GPIO3 or DP/DM. For example, DP/DM can be configured as UART and GPIO2/GPIO3 as I^2C, or DP/DM as I^2C and GPIO2/GPIO3 as UART.

9.1 IO Type Definition

- PWR: Power Pin
- GND: Ground Pin
- AI: Analog Input Pin
- AO: Analog Output Pin
- A IO: Analog Input/Output Pin
- D IO: Digital Input/Output Pin
- A/D IO: Analog/Digital Input/Output Pin
- NC: No Connection

10 Functional Block Diagram



11 Absolute Maximum Ratings

(Note 3)

- USBP to GND -- –0.3V to 72V
- VDD, VBUS, VO, BLD to GND -- –0.3V to 65V
- OPTO, VTR, GPIO1, GPIO2, GPIO3, CC1, CC2, D+, D-, RT, V5 to GND----------------------------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-28L 4x5--- 1.42W
- Package Thermal Resistance (Note 4)

  WQFN-28L 4x5, θ_{JA} -- 70.65°C/W

  WQFN-28L 4x5, θ_{JC} -- 4.72°C/W
- Junction Temperature --- 150°C
- Lead Temperature (Soldering, 10 sec.)-- 260°C
- Storage Temperature Range --- –65°C to 150°C
- ESD Susceptibility (Note 5)

  HBM (Human Body Model) ---2kV

Note 3. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 4. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 6)

- Supply Input Voltage, VDD --- 3.3V to 53V
- Junction Temperature Range--- –40°C to 125°C
- Ambient Temperature Range--- –40°C to 105°C

Note 6. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.8	2.85	2.9	V
VDD Turn-On/Off Hysteresis	V_{VDD_HYS}		0.1	0.2	0.3	V
VDD Start-Up Current	I_{VDD_START}	V_{VDD} = 2.8V	--	200	300	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Current	I_{OP}	1. V_{VDD} and V_{VO} = 5V 2. Measure I_{VDD} + I_{VO} 3. Disable VTR function 4. Does not include sourcing current of each pin.		--	--	7	mA
Sleep-Mode Current	I_{SLEEP}	1. V_{VDD} and V_{VO} = 5V 2. Measure I_{VDD} + I_{VO} 3. Disable VTR function 4. Does not include sourcing current of each pin.		--	--	2.2	mA
Green-Mode Current	I_{GREEN}	1. V_{VDD} and V_{VO} = 5V 2. Measure I_{VDD} + I_{VO} 3. Disable VTR function 4. Does not include sourcing current of each pin.		--	--	900	μA
MCU Operating Frequency	f_{OSC_MCU}	V_{VDD} > 2.8V		10.26	10.8	11.34	MHz
VO Section							
Maximum VO Overvoltage Protection Threshold	$V_{MAX\_VO\_OVP}$	EPR_EN = 0 and MOVP_OPT= 0		23	24	25	V
		EPR_EN = 1 or MOVP_OPT = 1		58	60	62	V
Maximum VO Overvoltage Protection Deglitch Time	$t_{DEGLITCH\_MAX\_VO\_OVP}$	(Note 7)		25	30	35	μs
Register-Programmable VO Undervoltage Wake-Up Threshold	$V_{VO\_UV\_WK}$	With respect to V_{REF_CV}. It can be disabled by register.	0	85.5	90	94.5	%
			1	80.75	85	89.25	%
VO Undervoltage Deglitch Time	$t_{DEGLITCH\_VO\_UV}$	(Note 7)		25	30	35	μs
Register-Programmable Overvoltage Protection Threshold	V_{VO_OVP}	With respect to V_{REF_CV}.	00	106.7	110	113.3	%
			01	109.3	115	120.8	%
			10	115	120	125	%
		EPR_EN = 0	11	126.3	133	139.6	%
		EPR_EN = 1	11	124.4	131	137.5	%
VO Overvoltage Protection Deglitch Time	$t_{DEGLITCH\_VO\_OVP}$	(Note 7)		25	30	35	μs
Regulator Section							
VO Divider Resistor	R_{FB}	R_{FB} = R_{FB1} + R_{FB2} R_{FB1}: VO to VFB R_{FB2}: VFB to GND (Note 7)		294	420	546	kΩ

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VO Scaling Factor	K_{FB}	$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2}$ EPR_EN = 0 (Note 7)		9.9	10	10.1	--
		$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2}$ EPR_EN = 1 (Note 7)		24.75	25	25.25	
Reference Voltage for Standby CV Regulators	$V_{ST\_REF\_CV}$			0.485	0.5	0.515	V
Minimum DAC Output Voltage for CV Regulators	$V_{DAC\_MIN\_CV}$	With 11-bit digital to analog converter		0.122	0.152	0.172	V
Maximum DAC Output Voltage for CV Regulators	$V_{DAC\_MAX\_CV}$			2.178	2.2	2.222	V
Minimum DAC Output Voltage for CC Regulators	$V_{DAC\_MIN\_CC}$	With 11-bit digital to analog converter		--	0	--	V
Maximum DAC Output Voltage for CC Regulators	$V_{DAC\_MAX\_CC}$			1.98	2	2.02	
Maximum ADC Sense Voltage	V_{ADC_MAX}	With 11-bit analog to digital converter		2.178	2.2	2.222	V
ADC Error	E_{ADC}			–6	--	6	LSB
Maximum OPTO Output Voltage	V_{OPTO_MAX}	V_{VDD} = 2.8V to 53V, I_{SRC_OPTO} = 1mA		1.8	--	--	V
Maximum OPTO Output Clamping Voltage	$V_{OPTO\_MAX\_CLAMP}$	V_{VDD} = 5V, I_{SRC_OPTO} = 1mA		2.1	2.4	2.7	V
Maximum OPTO Sourcing Current	I_{OPTO_MAX}	100Ω resistor connected in series		2	--	40	mA
Internal Resistor between OPTO and GND	R_{OPTO_GND}			42	60	78	kΩ
OPTO Pull-Low Impedance for CV Open Loop	R_{L_OPTO}	OPTO shorted to GND by register setting		--	--	200	Ω
Internal Bias Section							
V5 Bias	V_{BIAS_V5}	6V < V_{VDD} < 53V	00	4.61	4.75	4.89	V
			01	4.26	4.4	4.54	V
			10	3.8	4	4.2	V
V5 Load Regulation	$V_{V5\_LOAD\_REG}$	1mA < I_{BIAS_V5} < 30mA		--	--	200	mV
V5 Output Short-Circuit Current	I_{V5_SC}			45	70	95	mA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
BLD Section							
Register-Programmable BLD Discharge Current	I_{DISCHG_BLD}	V_{VDD} > 3V. It is necessary to gradually reduce the discharge current before closing I_{DISCHG_BLD}.	00	105	150	195	mA
			01	84	120	156	
			10	63	90	117	
			11	42	60	78	
BLD Discharge Current Step Change Delay Time	$t_{DLY\_STEP\_BLD}$	When BLD is disabled.		80	100	120	μs
Maximum BLD Sinking Current	I_{BLD_MAX}	V_{BLD} = 48V, in 700ms (Note 7)		0.2	--	0.5	A
Pull-Low Impedance	R_{L_BLD}	I_{BLD} = 50mA		--	--	30	Ω
Current Sense Section							
Register-Programmable Current-Sense Voltage Gain	K_{CS}			19.8	20	20.2	V/V
				39.6	40	40.4	
Current-Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}			0.35	0.4	0.45	V
Register-Programmable Exit Green Mode Threshold	V_{GREEN_ED}	$(V_{CS+} - V_{CS-})$ x K_{CS} + V_{OFFSET_CS}	0	0.41	0.45	0.49	V
			1	0.51	0.55	0.59	
Register-Programmable Transconductance Amplifier of Cable Compensation	gm_{COMP}	R_{CS} x K_{CS} = 100m	00	--	1.323	--	μA/V
		R_{CS} x K_{CS} = 120m	01	--	1.102	--	
		R_{CS} x K_{CS} = 200m	10	--	0.661	--	
		R_{CS} x K_{CS} = 400m	11	--	0.331	--	
Register-Programmable Cable Compensation Gain	K_{CC}	Disable cable compensation	000	Disable			V/V
		R_{CABLE} = 50mΩ	001	--	1	--	
		R_{CABLE} = 75mΩ	010	--	1.5	--	
		R_{CABLE} = 100mΩ	011	--	2	--	
		R_{CABLE} = 125mΩ	100	--	2.5	--	
		R_{CABLE} = 150mΩ	101	--	3	--	
		R_{CABLE} = 175mΩ	110	--	3.5	--	
		R_{CABLE} = 200mΩ	111	--	4	--	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Internal Compensation Section							
Register-Programmable Rz for Zero Point	R_Z	(Note 7)	000	6.5	10	13.5	kΩ
			001	19.5	30	40.5	
			010	32.5	50	67.5	
			011	52	80	108	
			100	65	100	135	
			101	104	160	216	
			110	149.5	230	310.5	
			111	201.5	310	418.5	
Register-Programmable Cz for Zero Point	C_Z	It can be programmed by register. (Note 7)		4.16	--	4256	nF
Register-Programmable Zero Point	f_{ZERO}	It can be programmed by register. (Note 7)		0.12	--	3832	Hz
Register-Programmable Middle Gain		It can be programmed by register. (Note 7)		–20	--	27.89	dB
Overshoot Clamping Threshold	V_{VO_OVC}	Ratio of V_{REF_CV}		104.5	110	115.5	%
Register-Programmable Undershoot Clamping Triggered Threshold	$V_{VO\_UVC\_Triggered}$	1. Ratio of V_{REF_CV} 2. Default is disabled 3. Disable at CC mode	0	85.5	90	94.5	%
			1	87.8	92.5	97.2	
Register-Programmable Undershoot Clamping Released Threshold	$V_{VO\_UVC\_Released}$	1. Ratio of V_{REF_CV} 2. Default is disabled 3. Disable at CC mode	0	90.3	95	99.8	%
			1	92.6	97.5	102.4	
Register-Programmable Debounce Time of Overshoot and Undershoot Clamping	$t_{DEBOUNCE\_OVUV\_CLAMP}$	(Note 7)	0	5	10	15	μs
			1	15	20	25	
Register-Programmable Debounce Time of Disable Undershoot Clamping at CC Mode	$t_{DEBOUNCE\_UVCC\_CLAMP}$	(Note 7)	0	5	10	15	μs
			1	15	20	25	
RT Section							
Open Loop Voltage	V_{RT_OP}	V_{VDD} = 5V, I_{BIAS_RT} = 0μA		3.6	V5 – 0.4	V5	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Internal Bias Current	I_{BIAS_RT}	V_{VDD} > 3V (For RT7209GQW)	00	95	100	105	μA
			01	18	20	22	
			10	4.5	5	5.5	
			11	Open			
		V_{VDD} > 3V (For RT7209BGQW)	00	Open			
			01	4.5	5	5.5	
			10	18	20	22	
			11	95	100	105	
RT Overvoltage Protection Threshold	V_{RT_OVP}	1. Turn-off the blocking MOSFET by register setting 2. Send a flag to MCU. 3. V_{VDD} > 5.5V		V5 + 0.2	V5 + 0.4	V5 + 0.6	V
Register-Programmable RT Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_RT\_OVP}$	(Note 7)	00	0.029	0.031	0.032	ms
			01	0.095	0.1	0.105	
			10	0.95	1	1.05	
			11	4.75	5	5.25	
GPIO1 Section							
Open-Loop Voltage	V_{GP1_OP}	V_{VDD} = 5V, I_{BIAS_GP} = 0μA		3.6	V5 – 0.4	V5	V
Register-Programmable Internal Bias Current	I_{BIAS_GP1}	V_{VDD} > 3V	00	900	1150	1400	μA
			01	95	100	105	
			10	18	20	22	
			11	Open			
GPIO1 Overvoltage Protection Threshold	V_{GP1_OVP}	1. Send a flag to MCU 2. V_{VDD} > 5.5V		V5 + 0.2	V5 + 0.4	V5 + 0.6	V
GPIO1 Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_GP1\_OVP}$	(Note 7)		30	50	70	μs
GPIO2 and GPIO3 Section							
Open-Loop Voltage	V_{GP_OP}	V_{VDD} = 5V, I_{BIAS_GP} = 0μA		3.6	V5 – 0.4	V5	V
Register-Programmable Internal Bias Current	I_{BIAS_GP}	V_{VDD} > 3V (For RT7209GQW)	00	95	100	105	μA
			01	18	20	22	
			10	4.5	5	5.5	
			11	Open			
		V_{VDD} > 3V (For RT7209BGQW)	00	Open			
			01	4.5	5	5.5	
			10	18	20	22	
			11	95	100	105	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
GPIO2/GPIO3 Overvoltage Protection Threshold	V_{GP_OVP}	1. Send a flag to MCU 2. V_{VDD} > 5.5V		V5 + 0.2	V5 + 0.4	V5 + 0.6	V
GPIO2/GPIO3 Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_GP\_OVP}$	(Note 7)		30	50	70	μs
VBUS Section							
Maximum VBUS Pulsed Discharge Current	I_{DISCHG_VBUS}			2	--	40	mA
Pull-Low Impedance	R_{L_VBUS}	I_{VBUS_MAX} = 40mA		100	150	250	Ω
VBUS Divider Resistor for ADC Sensing	R_{VBUS}	R_{VBUS} = R_{VBUS1} + R_{VBUS2}		294	420	546	kΩ
Trim-Programmable VBUS Scaling Factor for ADC Sensing	K_{VBUS}	K_{VBUS} = (R_{VBUS1} + R_{VBUS2}) / R_{VBUS2}, EPR_EN = 0		9.9	10	10.1	--
		K_{VBUS} = (R_{VBUS1} + R_{VBUS2}) / R_{VBUS2}, EPR_EN = 1		24.75	25	25.25	
Register-Programmable VBUS Drop Threshold for Output Short Protection	V_{DROP_VBUS}	V_{VDD} > 3.3V If V_{VO} - V_{BUS} > V_{DROP_VBUS}	0	0.1	0.2	0.3	V
			1	0.2	0.3	0.4	
Register-Programmable VBUS Drop Debounce Time for Output Short Protection	$t_{DEBOUNCE\_DROP\_VBUS}$	V_{VDD} > 5V (Note 7)	0	8	10	12	μs
			1	16	20	24	
D+ and D- Section							
Register-Programmable Pull-High Resistance	R_{H_DPDM}		0	Open			kΩ
			1	10	12.5	15	
Register-Programmable Pull-Low Resistance	R_{L_DPDM}		0	Open			kΩ
			1	16	20	24	
Register-Programmable Output Voltage Logic-High	V_{OH_OP}		00	Open Drain			V
	$V_{OH\_3.3V}$	V_{VDD} = 5V, R_L = 15kΩ	01	2.97	3.3	3.63	
	$V_{OH\_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH\_4.6V}$		11	4.1	4.6	5.1	
Output Voltage Logic-Low	V_{OL_OP} $V_{OL\_3.3V}$ $V_{OL\_1.8V}$ $V_{OL\_4.6V}$	R_L = 15kΩ		--	--	0.2	V
Register-Programmable DP and DM Input Level	V_{IN_LEV}		0	--	0	--	V
			1	0.3	0.4	0.5	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Input Voltage Logic-High	V_{IH_DPDM}		00	0.7 + V_{IN_LEV}	0.8 + V_{IN_LEV}	0.9 + V_{IN_LEV}	V
			01	1.2 + V_{IN_LEV}	1.3 + V_{IN_LEV}	1.4 + V_{IN_LEV}	
			10	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2 + V_{IN_LEV}	
			11	2 + V_{IN_LEV}	2.1 + V_{IN_LEV}	2.2 + V_{IN_LEV}	
Register-Programmable Input Voltage Logic-Low	V_{IL_DPDM}		00	0.5 + V_{IN_LEV}	0.6 + V_{IN_LEV}	0.7 + V_{IN_LEV}	V
			01	1.0 + V_{IN_LEV}	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	
			10	1.7 + V_{IN_LEV}	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	
			11	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2.0 + V_{IN_LEV}	
DPDM Switch On-Resistance	R_{ON_DPDM}			--	--	40	Ω
DP Comparison Threshold for Cable Detection	$V_{TH\_DP\_CD}$	Send an interrupt to MCU when cable detached. Disable/enable cable detection by register.		0.2	0.3	0.4	V
Register-Programmable Cable Detection Debounce Time	$t_{DEBOUNCE\_DP\_CD}$	Disable/Enable by register. (Note 7)	00	0.4	0.65	0.9	ms
			01	0.9	1.15	1.4	
			10	1.85	2.1	2.35	
			11	3.85	4.1	4.35	
Register-Programmable Input Debounce Time	$t_{DEBOUNCE\_DPDMIN}$	Debounce time = $t_{DEBOUNCE\_DPDMIN}$ x $K_{tDEBOUNCE\_DPDMIN}$ (Note 7)	00	0.95	1	1.05	μs
			01	1.9	2	2.1	
			10	3.8	4	4.2	
			11	7.6	8	8.4	
Register-Programmable Input Debounce Time Scale	$K_{tDEBOUNCE\_DPDMIN}$	(Note 7)	00	--	1	--	--
			01	--	8	--	
			10	--	64	--	
			11	--	512	--	
Register-Programmable DP/DM Overvoltage Protection Threshold	V_{DPDM_OVP}	1. Turn-off the blocking MOSFET by register setting 2. Send a flag to MCU 3. V_{VDD} > 5.5V	0	V5 - 0.1	V5	V5 + 0.1	V
			1	V5 - 0.5	V5 - 0.4	V5 - 0.3	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable DP/DM Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_DPDM\_OVP}$	(Note 7)	00	0.024	0.025	0.026	ms
			01	0.095	0.1	0.105	
			10	0.95	1	1.05	
			11	4.75	5	5.25	
Sourcing Current for Rust Protection	I_{DM_RUST}	1. V_{VDD} > 3.65V 2. Only for the DM pin 3. Disable/Enable by register		2.4	3	3.6	mA
Pull-High Resistance for Apple Mode	$R_{H\_DPDM\_AM}$			24	30	36	kΩ
Register-Programmable Output Voltage Logic-High for Apple Mode	$V_{OH\_2.7V\_AM}$	V_{VDD} > 4V	0	2.565	2.7	2.835	V
	$V_{OH\_2V\_AM}$		1	1.88	2	2.12	
CC1 and CC2 Section							
Output Voltage Logic-High	V_{OH_CC}			1.05	1.125	1.2	V
Output Voltage Logic-Low	V_{OL_CC}			0	0.0375	0.075	V
Register-Programmable Input Voltage Logic-High	V_{IH_CC}		00	0.8	0.9	1	V
			01	0.7	0.8	0.9	
			10	0.6	0.7	0.8	
			11	0.5	0.6	0.7	
Register-Programmable Input Voltage Logic-Low	V_{IL_CC}		00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
Open Loop Voltage for CC1/CC2 Sourcing Current	V_{CC_OP}	V_{VDD} > 5V		2.9	3.25	3.6	V
Register-Programmable Sourcing Current	I_{CC_SRC}	V_{VDD} > 3V	00	High Impedance			μA
			01	76	80	84	
			10	171	180	189	
			11	304	330	356	
CC1/CC2 Comparison Threshold for Cable Detection	V_{CC_CD}	1. V_{VDD} > 3V 2. Disable/Enable by register 3. Send a flag to MCU		2.5	2.6	2.7	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable CC1/CC2 Overvoltage Protection Threshold	V_{CC_OVP}	1. Turn-off the blocking MOSFET by register setting 2. Send a flag to MCU 3. V_{VDD} > 5.5V 4. CC_OVP_SEL = 0	0	V5 – 0.1	V5	V5 + 0.1	V
			1	V5 – 0.5	V5 - 0.4	V5 - 0.3	
		1. to 4. as noted above 5. CC_OVP_SEL = 1		V5 + 0.5	V5 + 0.75	V5 + 1	
		1. to 4. as noted above 5. VCONN_EN = 1	00	4.475	4.575	4.675	
			01	4.6	4.675	4.75	
			10	4.625	4.725	4.825	
			11	5.3	5.4	5.5	
Register-Programmable CC1/CC2 Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_CC\_OVP}$	(Note 7)	00	0.024	0.025	0.026	ms
			01	0.095	0.1	0.105	
			10	0.95	1	1.05	
			11	4.75	5	5.25	
V_{CONN} Voltage	V_{VCONN}	V_{VDD} = 5V, I_{VCONN} = 0mA		--	--	V5	V
		V_{VDD} = 5V, I_{VCONN} = 30mA		3.3	--	--	
V_{CONN} Short-Circuit Current	I_{VCONN_SC}			45	70	95	mA
USBP Section							
USBP Output Voltage Logic-High	V_{OH_USBP}	R_L = 10MΩ		V_{VO} + 8.5	V_{VO} + 10	V_{VO} + 12	V
USBP Undervoltage Protection Threshold Voltage	V_{USBP_UVP}	1. Disable/Enable by register 2. Send a flag to MCU		V_{VO} + 5	--	--	V
USBP Undervoltage Deglitch Time	$t_{DEGLITCH\_USBP\_UV}$	(Note 7)		30	50	70	μs
Register-Programmable Pull-Low Resistance for VBUS Drop Protection	$R_{PL\_VBUSDR\_USBP}$	If VBUS drop protection is triggered and USBP_PE = 1, then R_{USBP} = $R_{PL\_VBUSDR\_USBP}$	0	7	10	13	kΩ
			1	14	20	26	

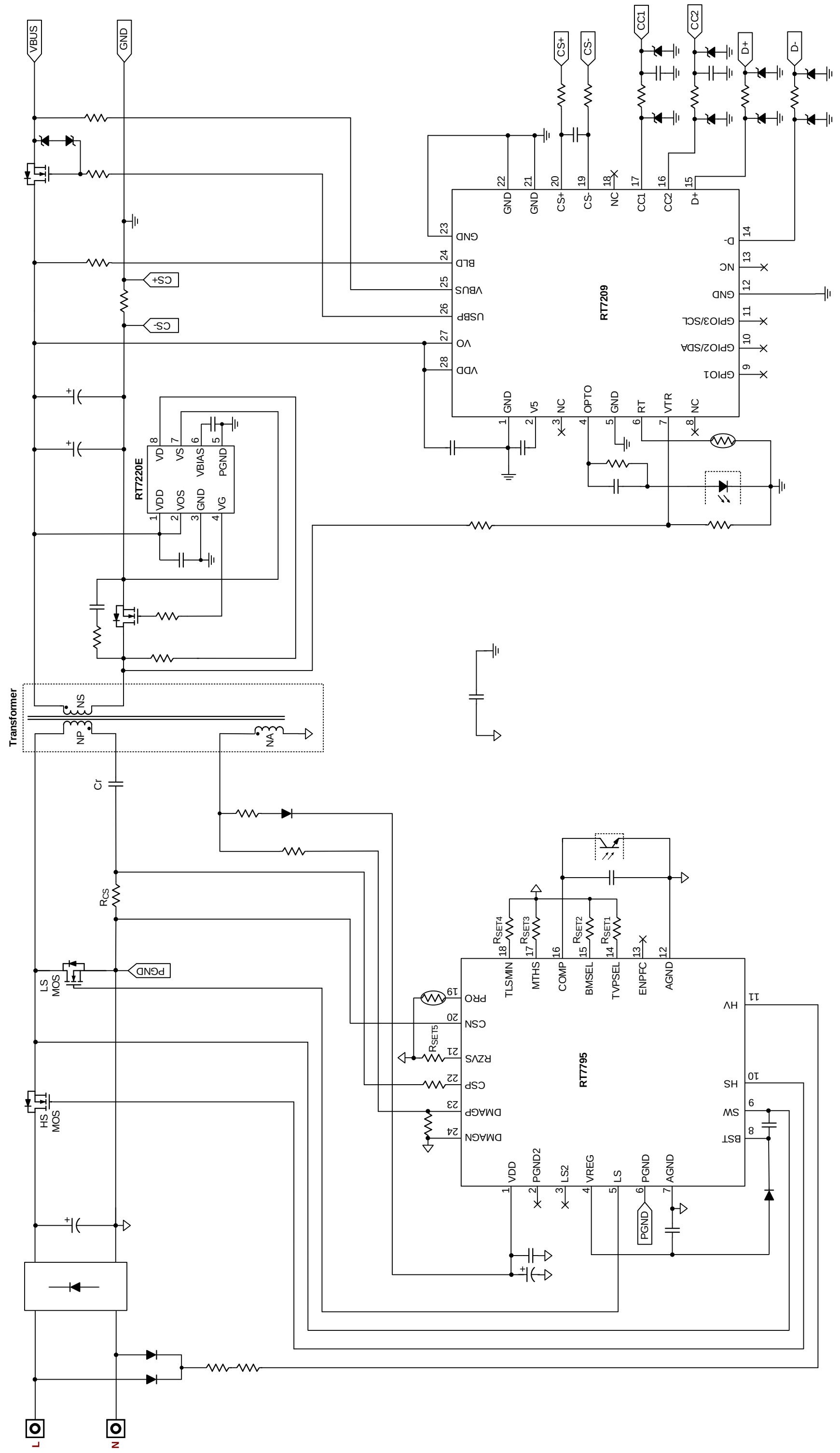
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Pull-Low Resistance when USBP is Turned Off	$R_{PL\_USBPOFF}$	For $V_{VDD} > V_{VDD\_ON}$, if USBP_PE = 0, then $R_{USBP} = R_{PL\_USBPOFF}$ (RT7209GQW)		5.44	6.8	8.16	kΩ
		For $V_{VDD} > V_{VDD\_ON}$, if USBP_PE = 0, then $R_{USBP} = R_{PL\_USBPOFF}$ (RT7209BGQW)		3.5	5	6.5	kΩ
Pull-Low Resistance during VDD UVLO	$R_{PL\_UVLO\_USBP}$	For $V_{VDD} < V_{VDD\_ON}$, then $R_{USBP} = R_{PL\_UVLO\_USBP}$ (RT7209GQW)		5.44	6.8	8.16	kΩ
		For $V_{VDD} < V_{VDD\_ON}$, then $R_{USBP} = R_{PL\_UVLO\_USBP}$ (RT7209BGQW)		3.5	5	6.5	kΩ
USBP Divider Resistor for Capacitive Loads	R_{USBP}	Capacitive load function can be disabled/enabled by register.		650	800	950	kΩ
USBP Scaling Factor for Capacitive Loads	K_{USBP}			4.85	5	5.15	--
Maximum DAC Output Voltage for Capacitive Loads	$V_{DAC\_MAX\_CL}$	With 8-bit digital to analog converter		2.134	2.2	2.266	V
Minimum DAC Output Voltage for Capacitive Loads	$V_{DAC\_MIN\_CL}$	With 8-bit digital to analog converter		--	0	--	V
Register-Programmable USBP Soft-Start Time	t_{SS_USBP}	MCU can disable/enable soft-start function	000	0.9	1	1.1	ms
			001	1.8	2	2.2	
			010	3.6	4	4.4	
			011	7.2	8	8.8	
			100	14.4	16	17.6	
			101	28.8	32	35.2	
			110	57.6	64	70.4	
			111	115.2	128	140.8	
VTR Section							
VTR Sample and Hold Threshold	K_{VTR_SH}	$V_{TH\_SH} = K_{VTR\_SH} \times V_{VTR\_HIGH[n-1]}$		0.831	0.875	0.919	--
Register-Programmable Mask Time	t_{MASK}	$V_{VTR} > V_{TH\_SH}$ (Note 7)	0	170	320	470	ns
			1	60	160	260	
Register-Programmable VTR Blanking Time	t_{BLANK_VTR}	$V_{VTR} > V_{TH\_SH}$ VTR blanking time change limit is ±185ns per cycle. (Note 7)	00	0.2	0.285	0.37	μs
			01	0.32	0.47	0.62	
			10	0.85	1.03	1.21	
			11	1.38	1.58	1.78	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Trim-Programmable VTR Falling Time Threshold	$t_{VTR\_FALLING}$	VTR falling edge is from V_{VTR} = 0.875 x V_{VTR_SH} to VTR = V_{VTR_RST} (Note 7)	00	500	550	600	ns
			01	300	350	400	
			10	150	200	250	
			11	50	100	150	
VTR Overvoltage Threshold	$V_{TH\_VTR\_OV}$	1. Send a flag to MCU 2. V_{VDD} > 5.5V		2.6	2.7	2.8	V
VTR Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_VTR\_OVP}$	(Note 7)		30	50	70	μs
VTR Rising Edge Threshold for AC OFF Detection	V_{EDGE_VTR}			30	70	110	mV
VTR Edge Debounce Time for AC OFF Detection	$t_{DEBOUNCE\_EDGE\_VTR}$	If V_{VTR} in $t_{DEBOUNCE\_EDGE\_VTR}$ is lower than V_{EDGE_VTR}, it will send an AC OFF flag to MCU. (Note 7)		90	100	110	ms
Reset Voltage for VTR Sample and Hold	V_{RST_VTR}	V_{VDD} = 5V		30	70	110	mV
VTR Section (For RT Application)							
Open-Loop Voltage	V_{VTR_OP}	V_{VDD} = 5V, I_{VTR} = 0μA		3.6	V5 – 0.4	V5	V
Register-Programmable Internal Bias Current	I_{BIAS_VTR}	V_{VDD} > 3V	00	95	100	105	μA
			01	18	20	22	
			10	4.5	5	5.5	
			11		Open		
VTR Overvoltage Threshold	$V_{TH\_VTR\_OV}$	V_{VDD} > 5.5V		V5 + 0.2	V5 + 0.4	V5 + 0.6	V
VTR Overvoltage Protection Debounce Time	$t_{DEBOUNCE\_VTR\_OVP}$	(Note 7)		30	50	70	μs
Thermal Sensor Section							
Thermal Sensor Error		25°C to 105°C (single point)		–7	--	7	°C

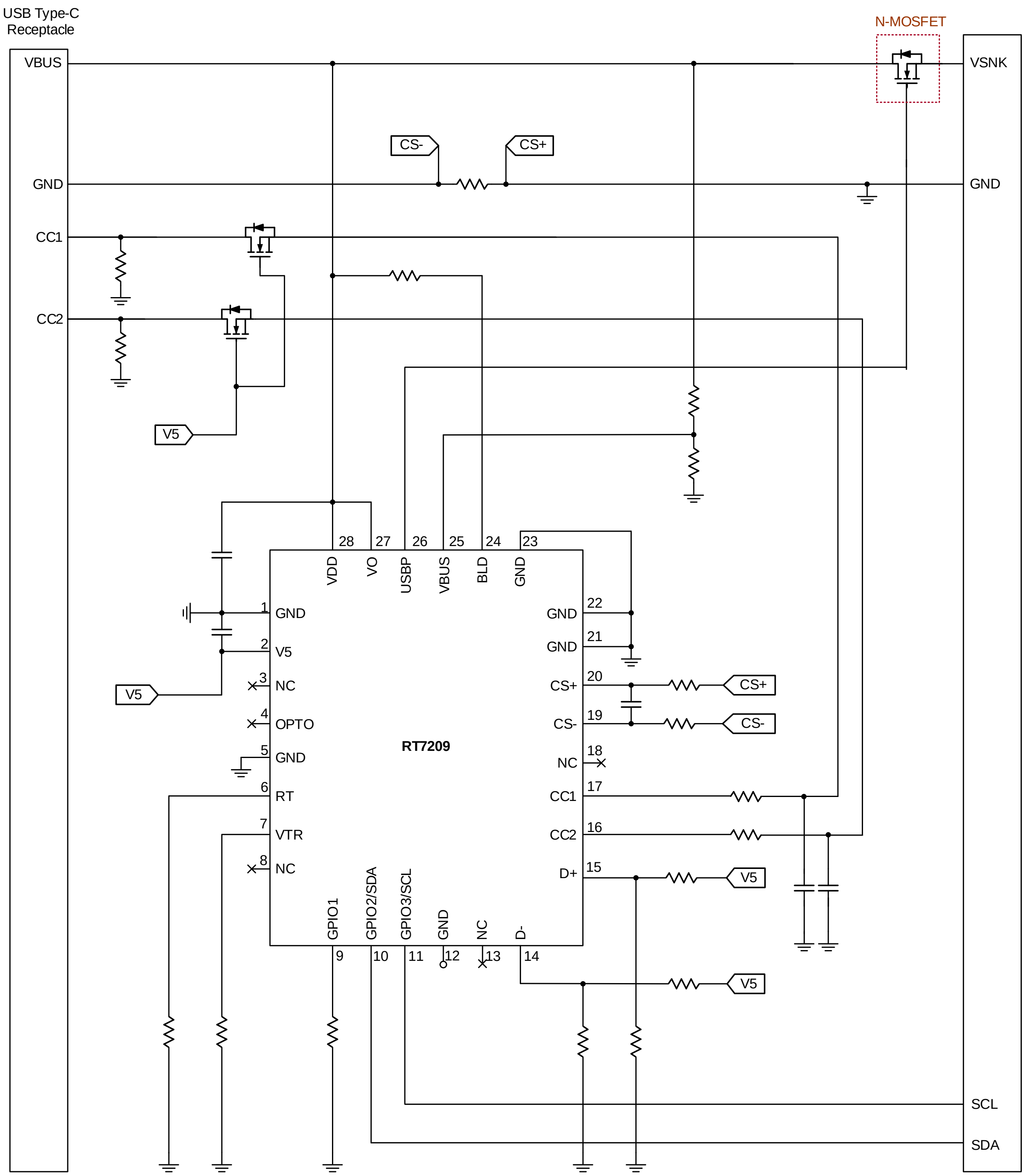
Note 7. Guaranteed by design.

14 Typical Application Circuit

14.1 The RT7209 in Source Application (Only for Low-Side)

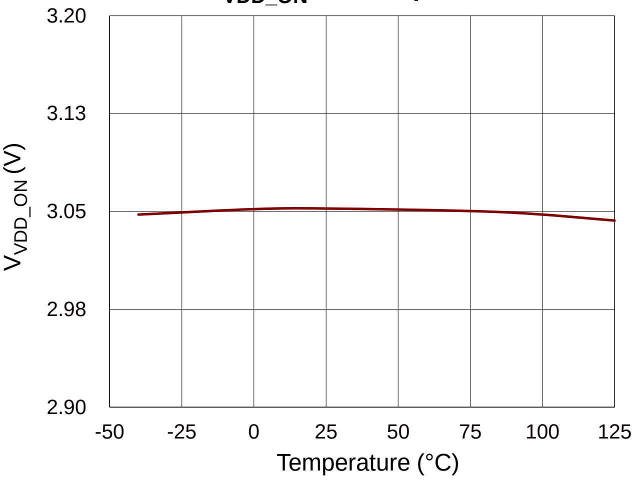


14.2 The RT7209 in Sink Application

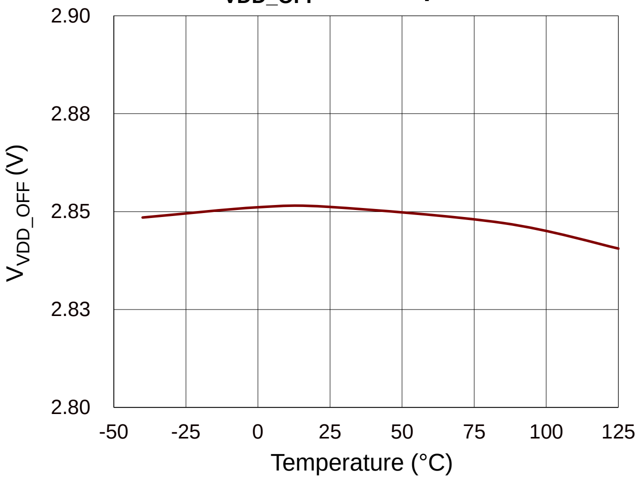


15 Typical Operating Characteristics

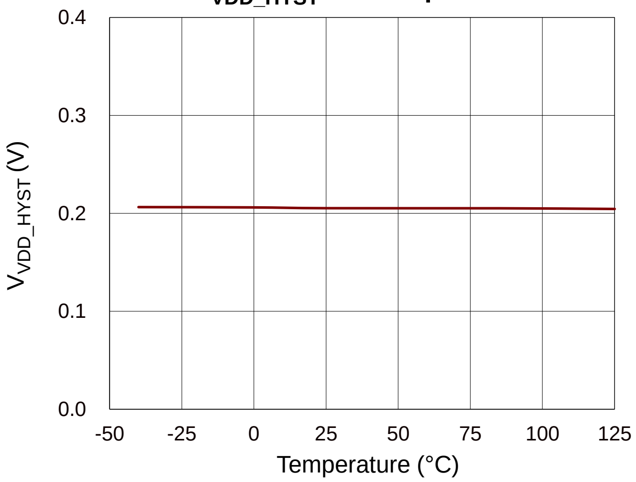
V_{VDD_ON} vs. Temperature



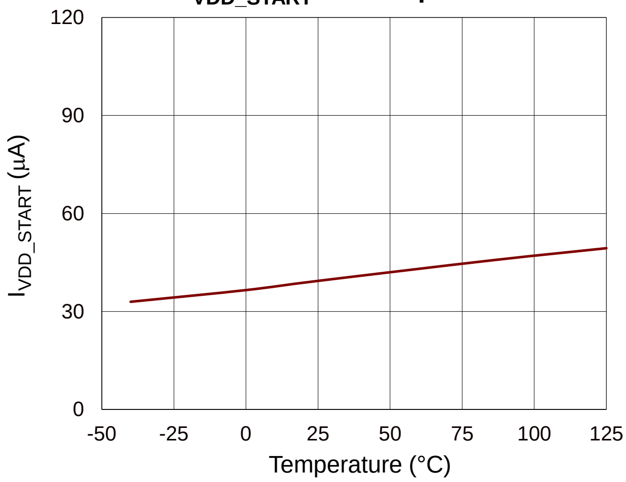
V_{VDD_OFF} vs. Temperature



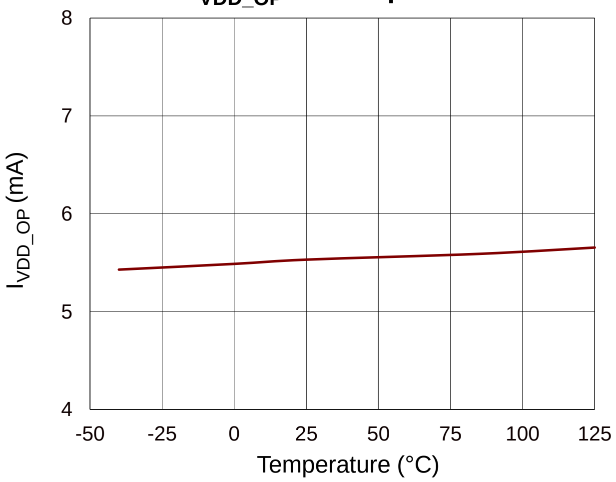
V_{VDD_HYST} vs. Temperature



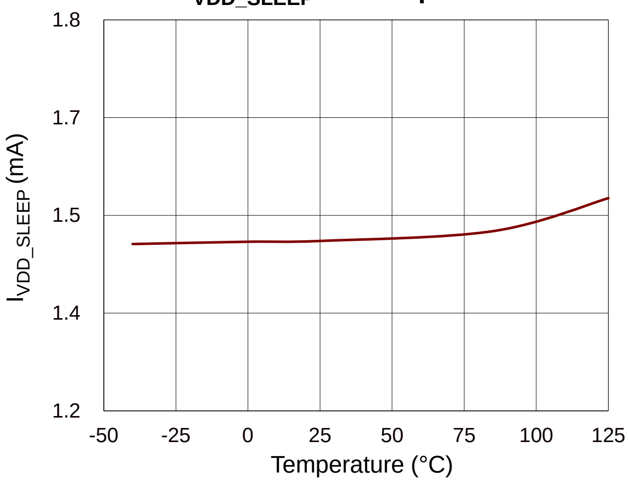
I_{VDD_START} vs. Temperature

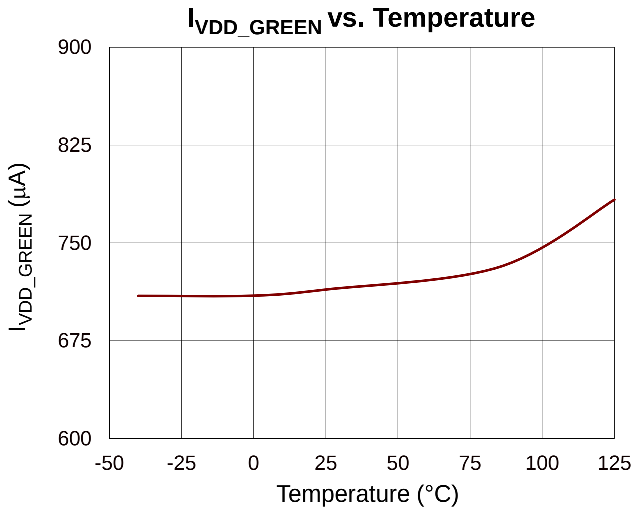


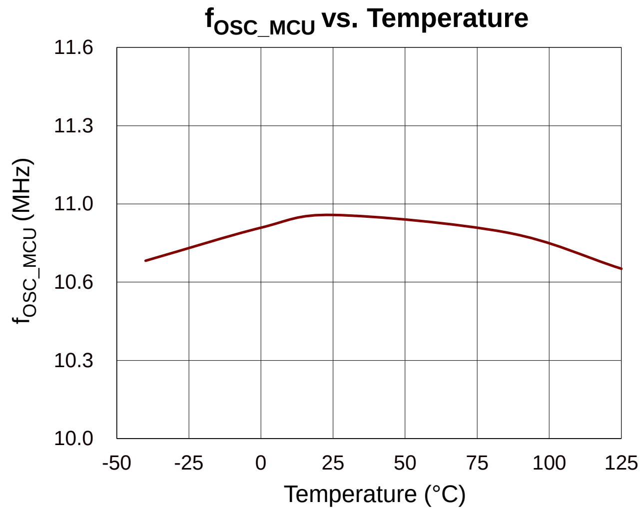
I_{VDD_OP} vs. Temperature

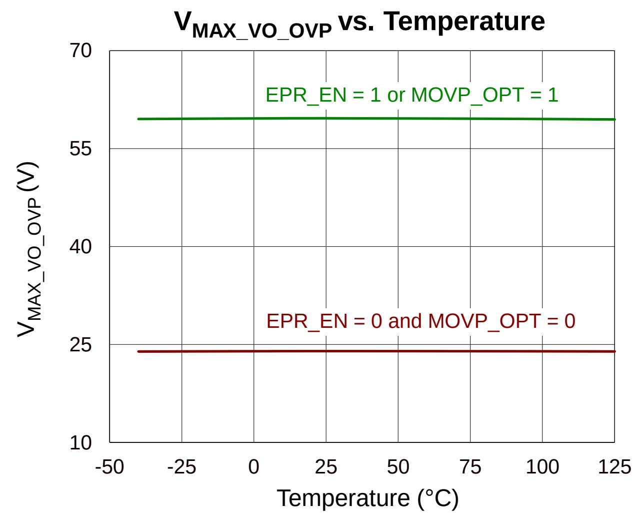


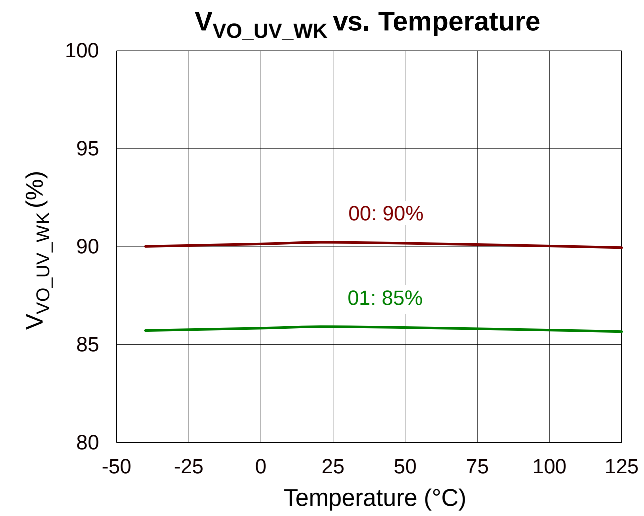
I_{VDD_SLEEP} vs. Temperature

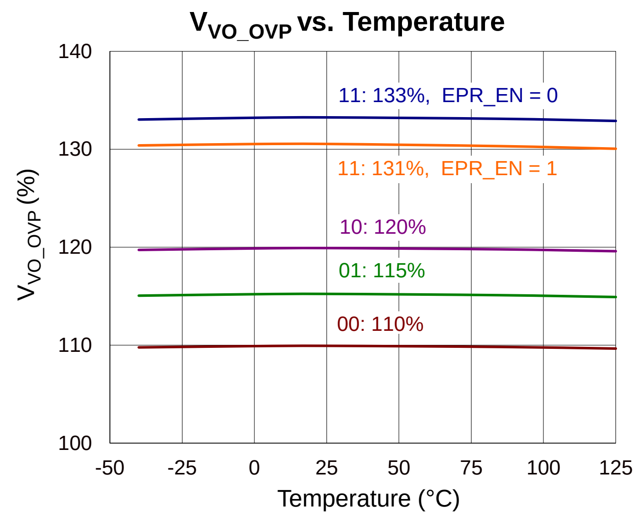


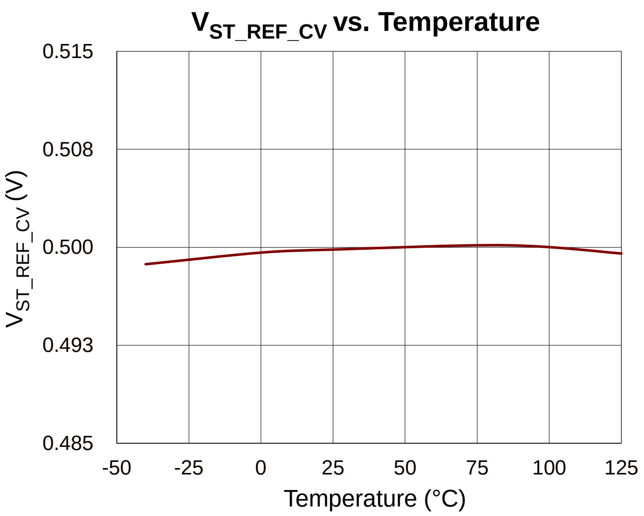

IVDD_GREEN vs. Temperature
IVDD_GREEN (μA)
900
825
750
675
600
-50 -25 0 25 50 75 100 125
Temperature (°C)


fOSC_MCU vs. Temperature
fOSC_MCU (MHz)
11.6
11.3
11.0
10.6
10.3
10.0
-50 -25 0 25 50 75 100 125
Temperature (°C)

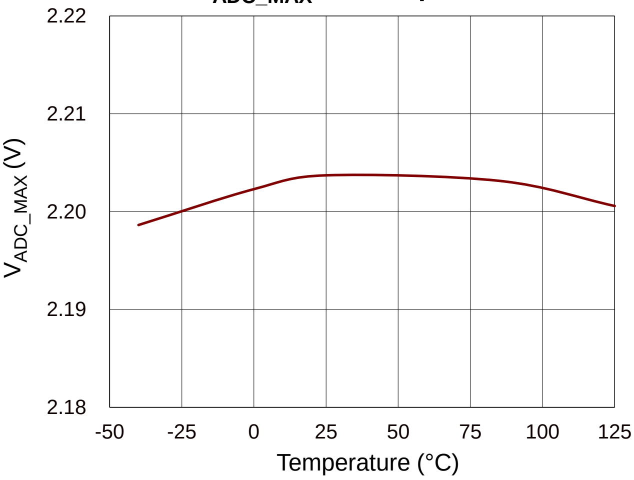

VMAX_VO_OVP vs. Temperature
VMAX_VO_OVP (V)
70
55
40
25
10
EPR_EN = 1 or MOVP_OPT = 1
EPR_EN = 0 and MOVP_OPT = 0
-50 -25 0 25 50 75 100 125
Temperature (°C)


VVO_UV_WK vs. Temperature
VVO_UV_WK (%)
100
95
90
85
80
00: 90%
01: 85%
-50 -25 0 25 50 75 100 125
Temperature (°C)

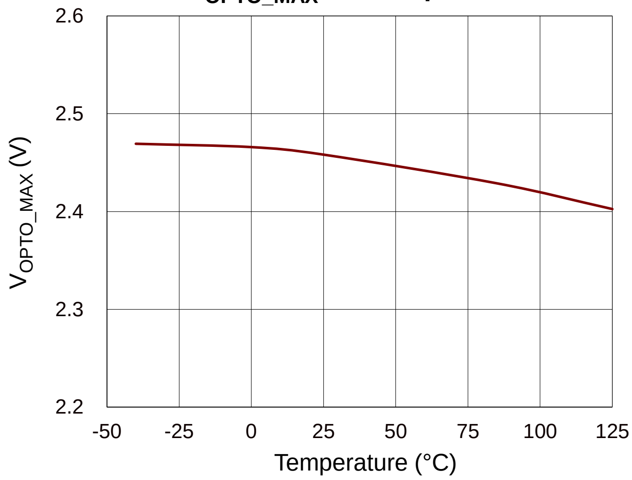

VVO_OVP vs. Temperature
VVO_OVP (%)
140
130
120
110
100
11: 133%, EPR_EN = 0
11: 131%, EPR_EN = 1
10: 120%
01: 115%
00: 110%
-50 -25 0 25 50 75 100 125
Temperature (°C)


VST_REF_CV vs. Temperature
VST_REF_CV (V)
0.515
0.508
0.500
0.493
0.485
-50 -25 0 25 50 75 100 125
Temperature (°C)

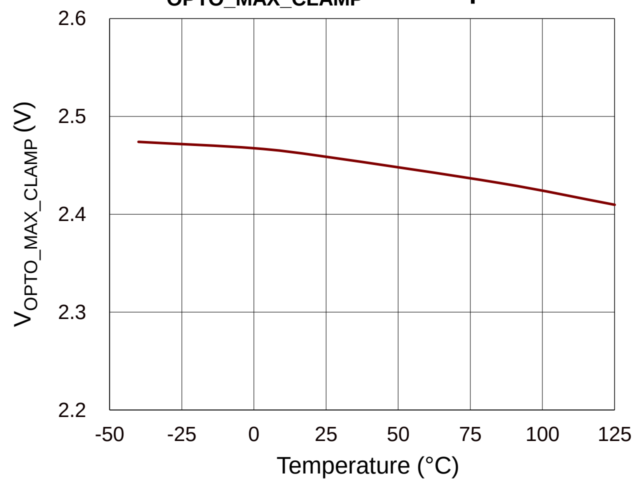
V_{ADC_MAX} vs. Temperature



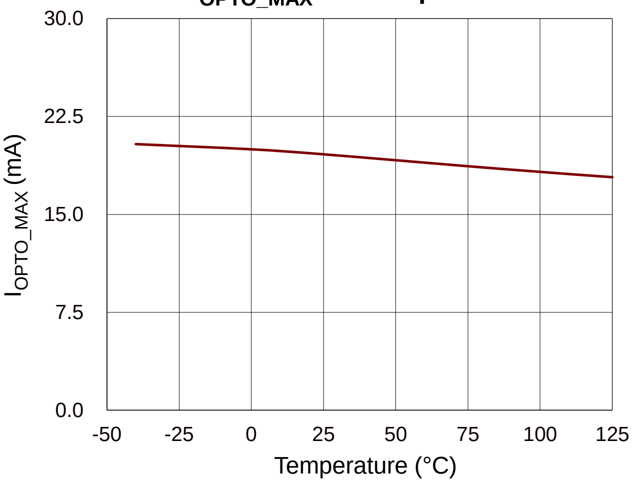
V_{OPTO_MAX} vs. Temperature



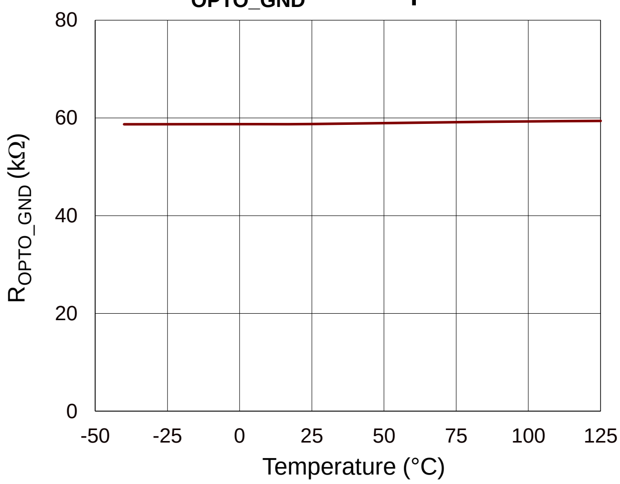
$V_{OPTO\_MAX\_CLAMP}$ vs. Temperature



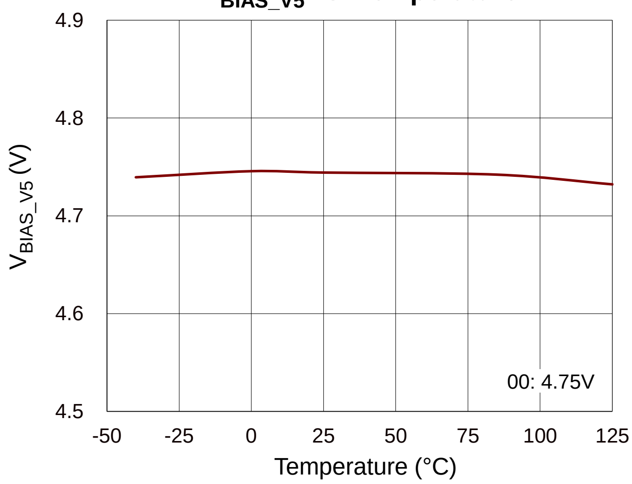
I_{OPTO_MAX} vs. Temperature

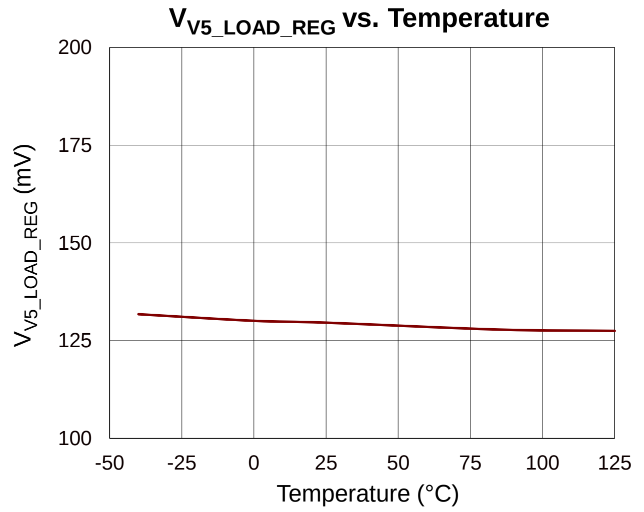


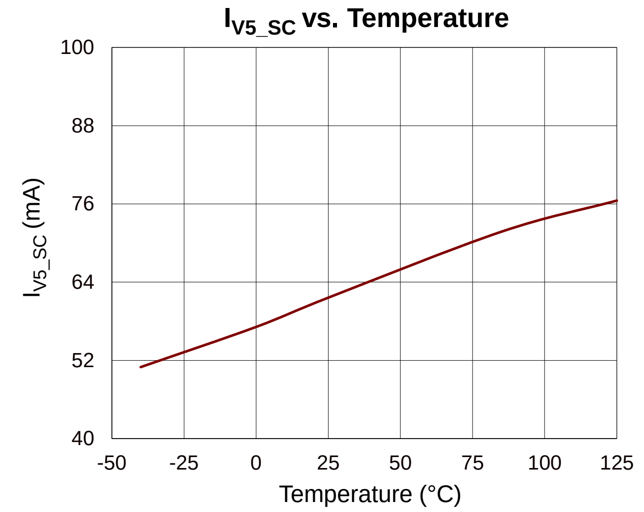
R_{OPTO_GND} vs. Temperature

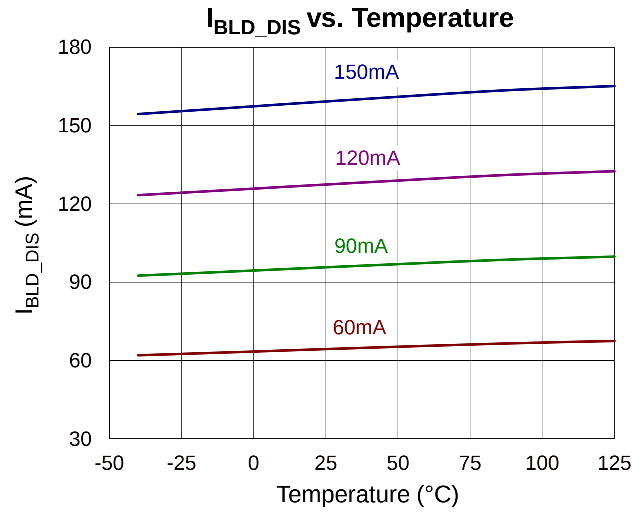


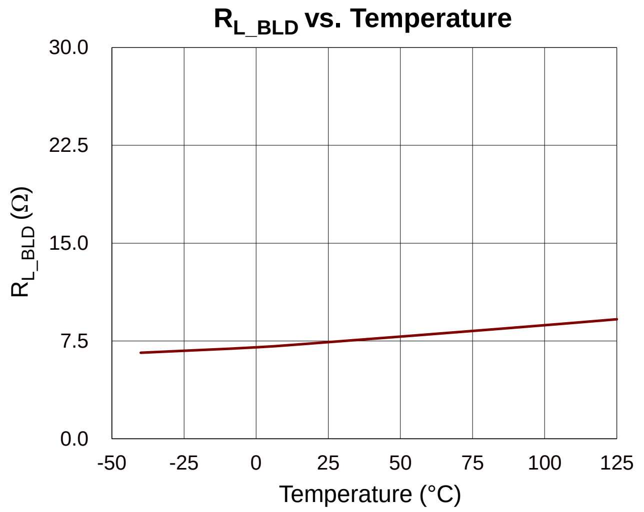
V_{BIAS_V5} vs. Temperature

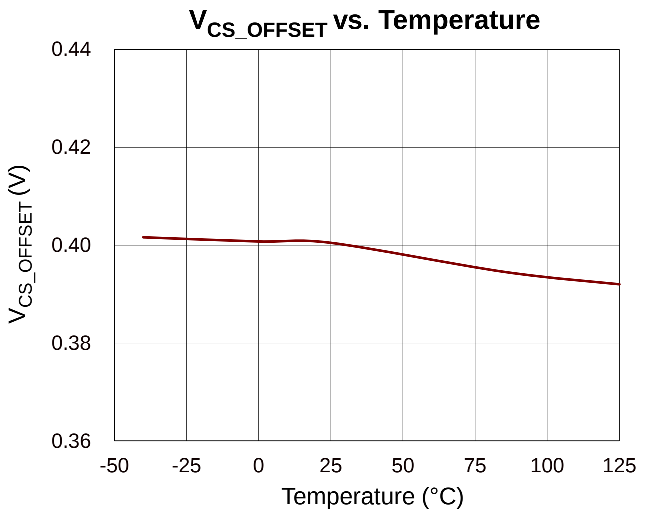


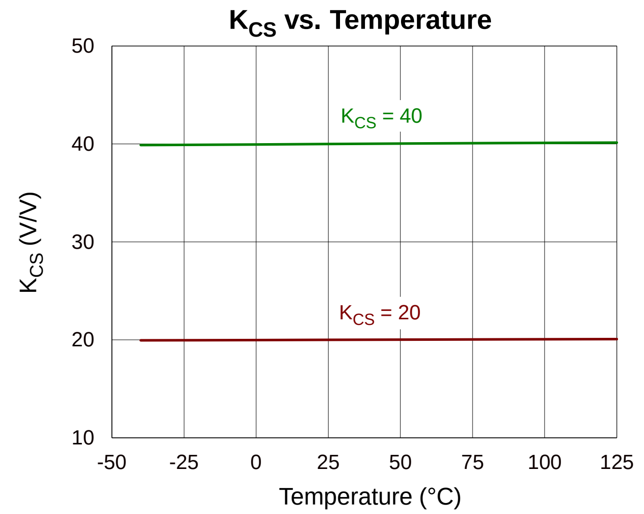

$V_{V5\_LOAD\_REG}$ vs. Temperature
200
175
150
125
100
$V_{V5\_LOAD\_REG}$ (mV)
-50 -25 0 25 50 75 100 125
Temperature (°C)


I_{V5_SC} vs. Temperature
100
88
76
64
52
40
I_{V5_SC} (mA)
-50 -25 0 25 50 75 100 125
Temperature (°C)

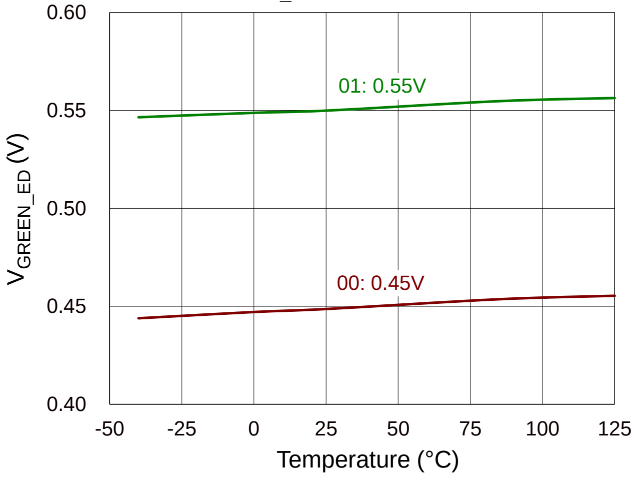

I_{BLD_DIS} vs. Temperature
180
150
120
90
60
30
I_{BLD_DIS} (mA)
150mA
120mA
90mA
60mA
-50 -25 0 25 50 75 100 125
Temperature (°C)


R_{L_BLD} vs. Temperature
30.0
22.5
15.0
7.5
0.0
R_{L_BLD} (Ω)
-50 -25 0 25 50 75 100 125
Temperature (°C)

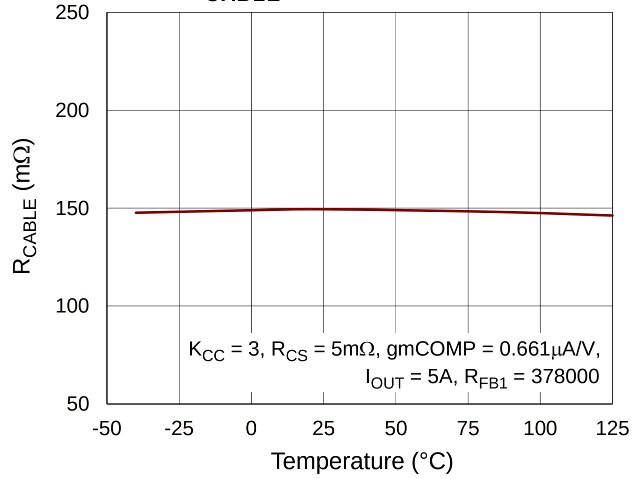

V_{CS_OFFSET} vs. Temperature
0.44
0.42
0.40
0.38
0.36
V_{CS_OFFSET} (V)
-50 -25 0 25 50 75 100 125
Temperature (°C)


K_{CS} vs. Temperature
50
40
30
20
10
K_{CS} (V/V)
K_{CS} = 40
K_{CS} = 20
-50 -25 0 25 50 75 100 125
Temperature (°C)

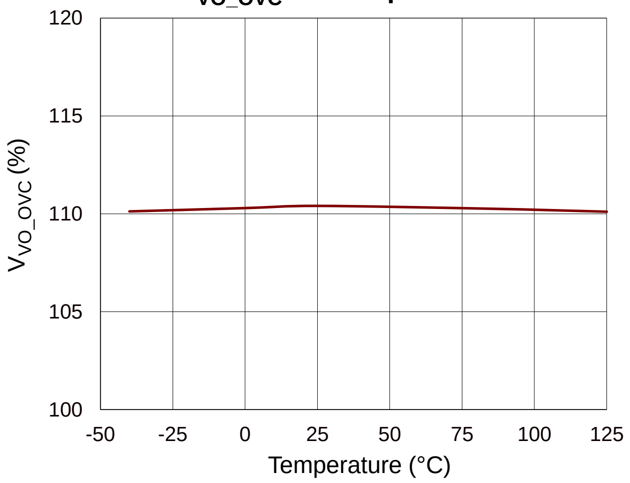
V_{GREEN_ED} vs. Temperature



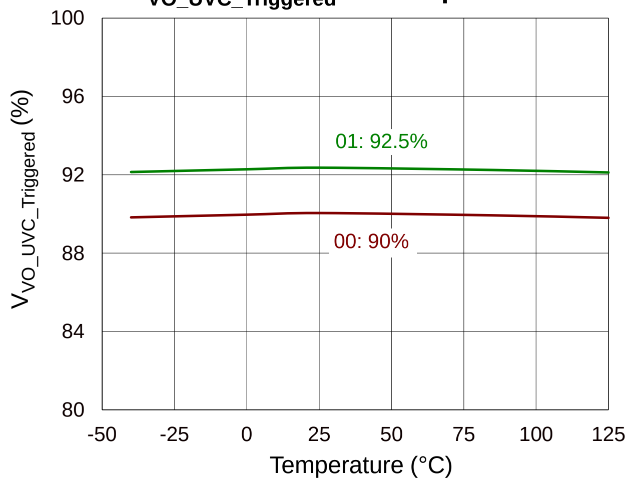
R_{CABLE} vs. Temperature



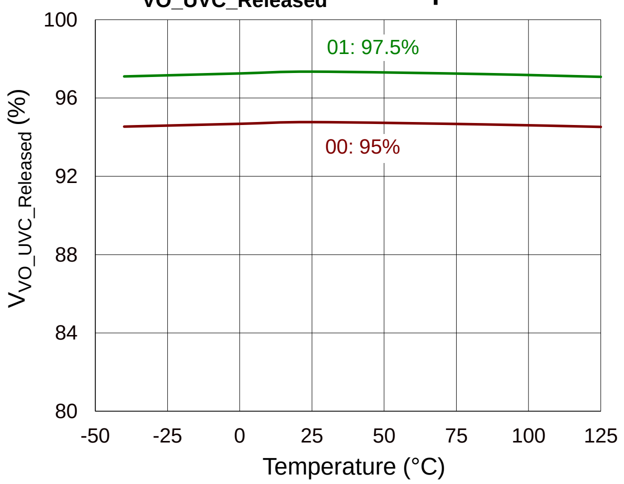
V_{VO_OVC} vs. Temperature



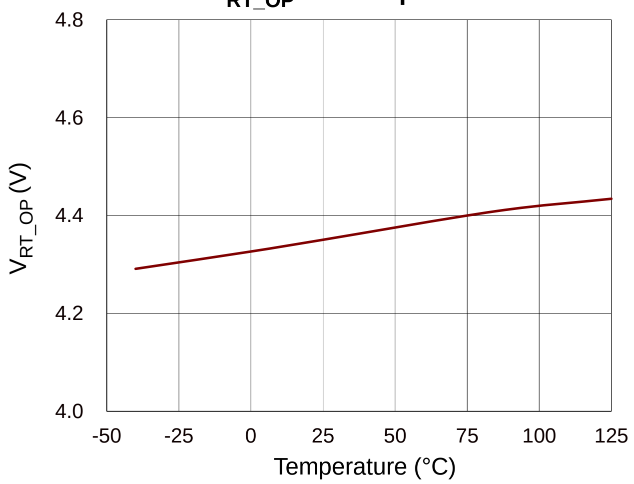
$V_{VO\_UVC\_Triggered}$ vs. Temperature

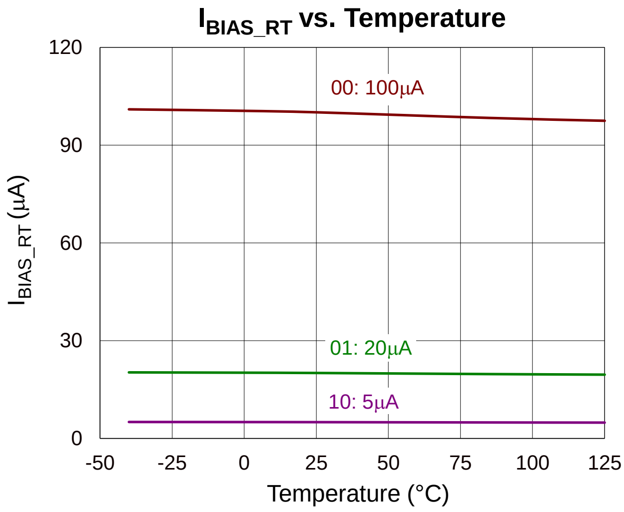


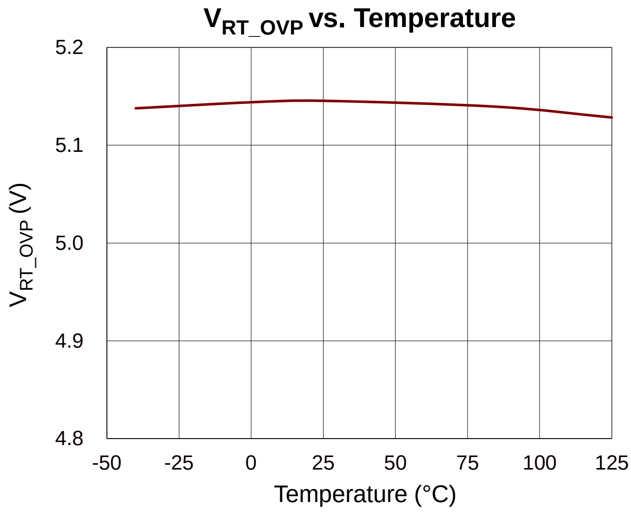
$V_{VO\_UVC\_Released}$ vs. Temperature

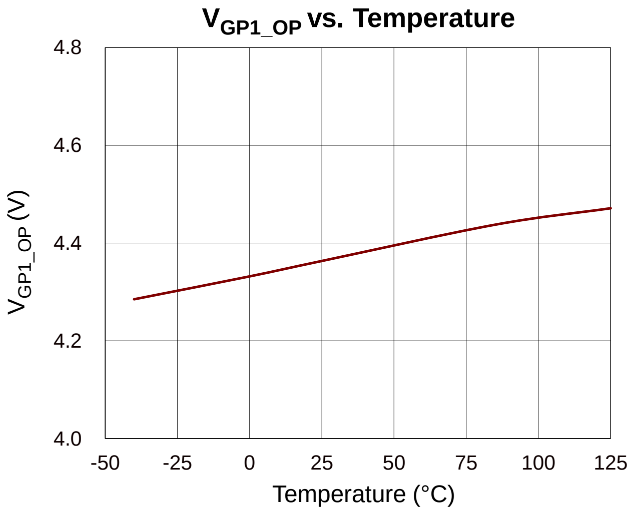


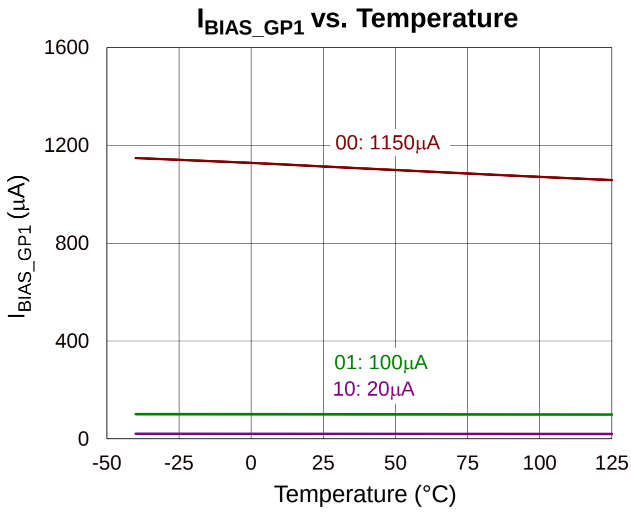
V_{RT_OP} vs. Temperature

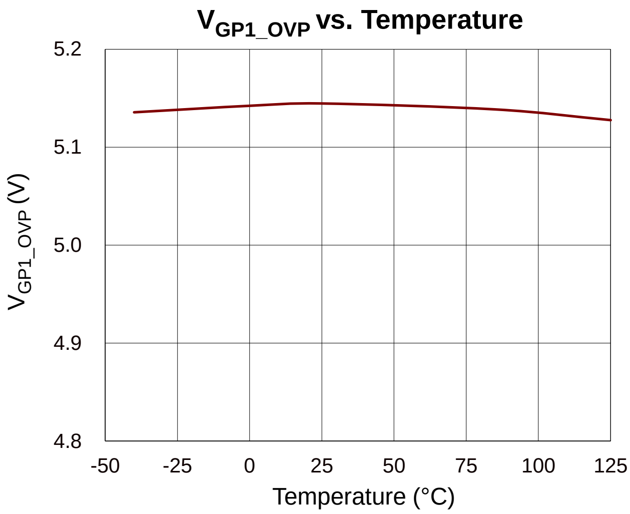


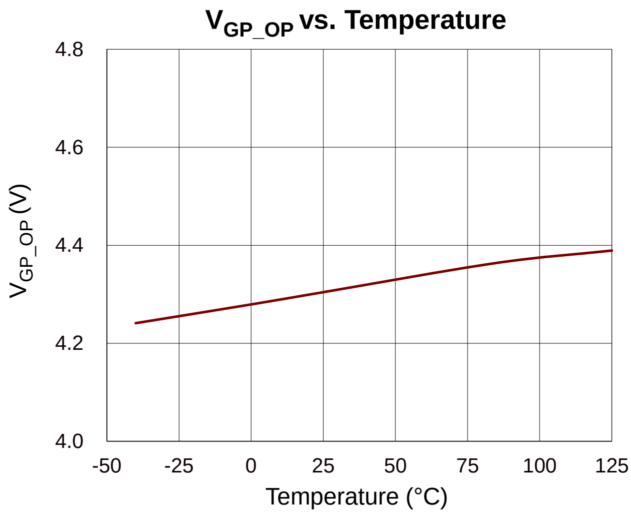

I_BIAS_RT vs. Temperature
I_BIAS_RT (µA)
Temperature (°C)
00: 100µA
01: 20µA
10: 5µA
120
90
60
30
0
-50 -25 0 25 50 75 100 125


V_RT_OVP vs. Temperature
V_RT_OVP (V)
Temperature (°C)
5.2
5.1
5.0
4.9
4.8
-50 -25 0 25 50 75 100 125

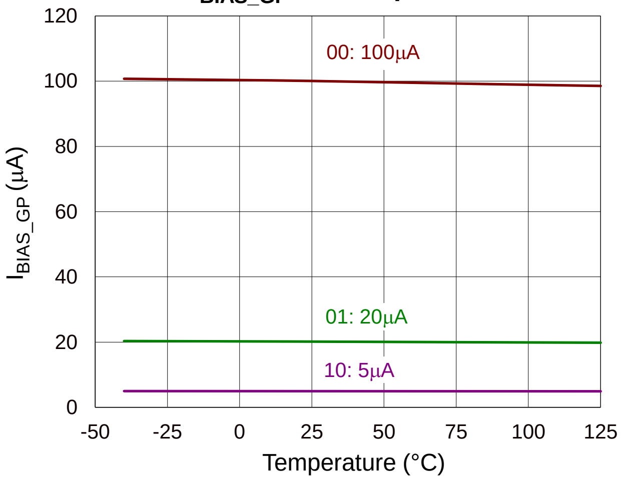

V_GP1_OP vs. Temperature
V_GP1_OP (V)
Temperature (°C)
4.8
4.6
4.4
4.2
4.0
-50 -25 0 25 50 75 100 125


I_BIAS_GP1 vs. Temperature
I_BIAS_GP1 (µA)
Temperature (°C)
00: 1150µA
01: 100µA
10: 20µA
1600
1200
800
400
0
-50 -25 0 25 50 75 100 125

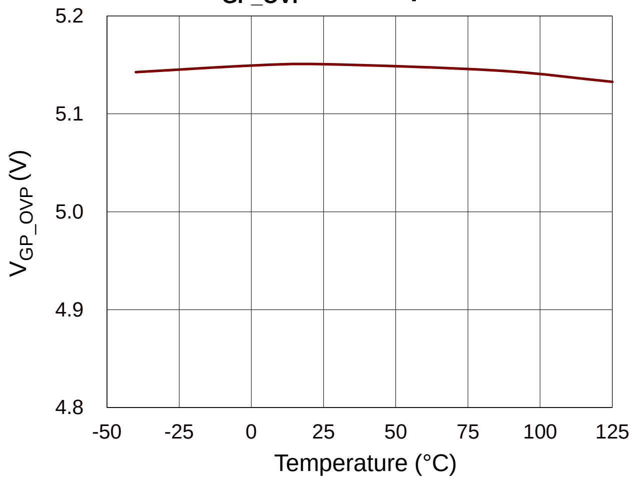

V_GP1_OVP vs. Temperature
V_GP1_OVP (V)
Temperature (°C)
5.2
5.1
5.0
4.9
4.8
-50 -25 0 25 50 75 100 125


V_GP_OP vs. Temperature
V_GP_OP (V)
Temperature (°C)
4.8
4.6
4.4
4.2
4.0
-50 -25 0 25 50 75 100 125

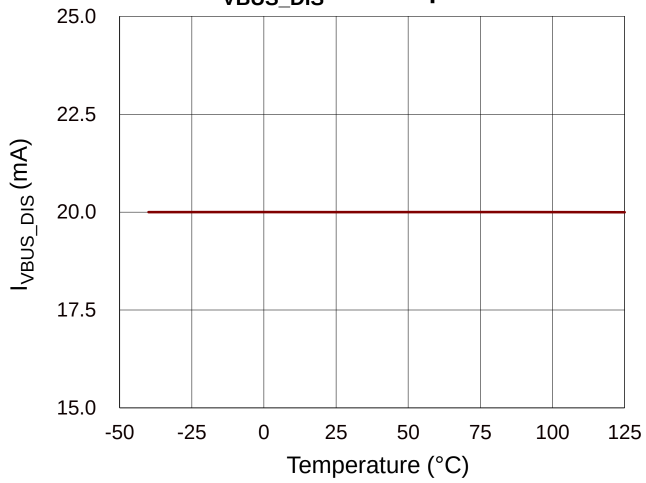
I_{BIAS_GP} vs. Temperature



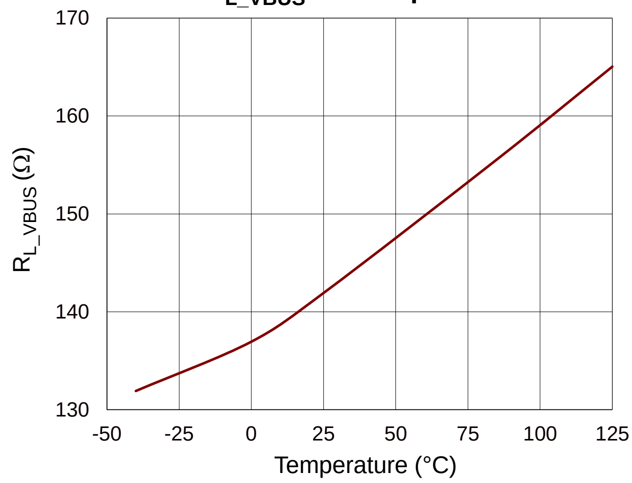
V_{GP_OVP} vs. Temperature



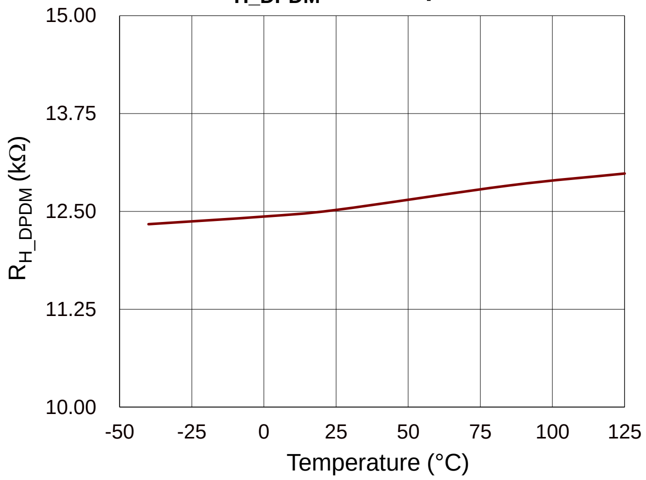
I_{VBUS_DIS} vs. Temperature



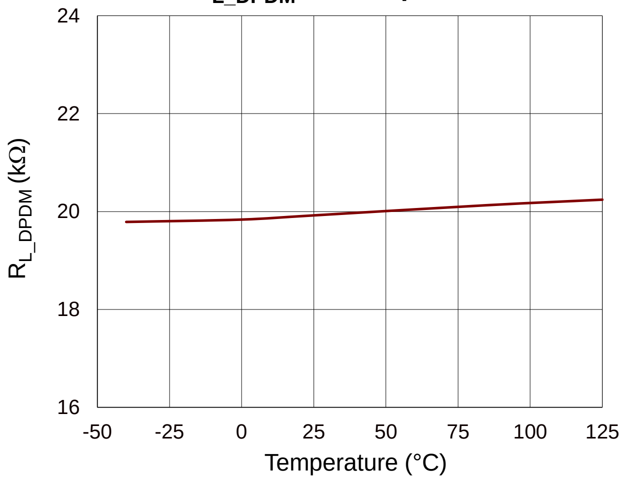
R_{L_VBUS} vs. Temperature

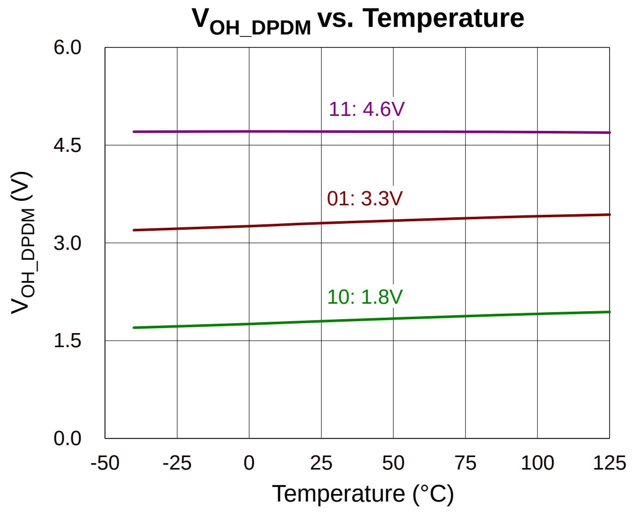


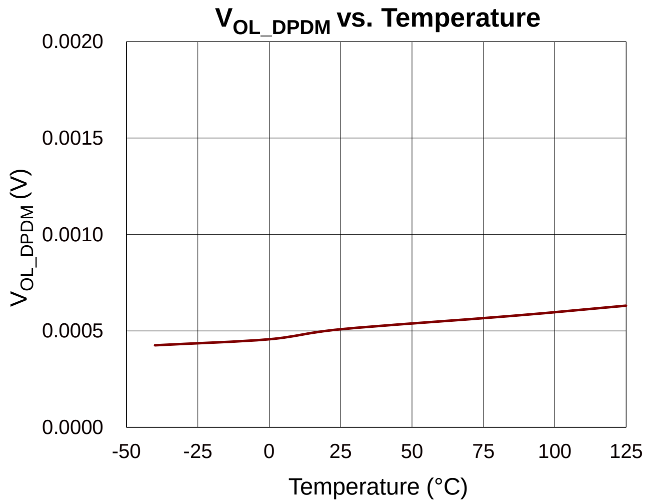
R_{H_DPDM} vs. Temperature

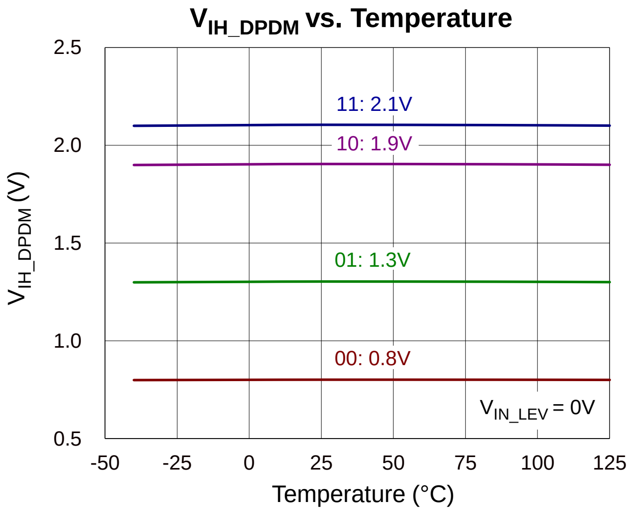


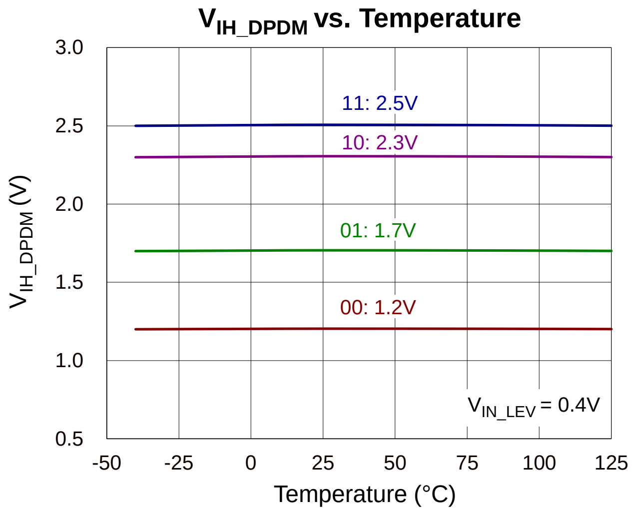
R_{L_DPDM} vs. Temperature

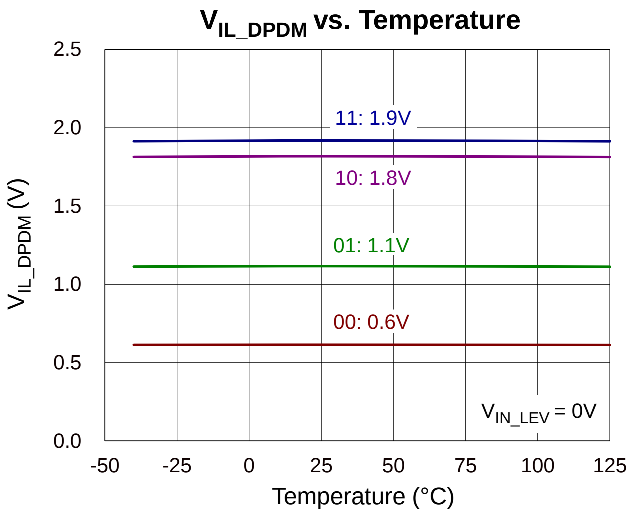


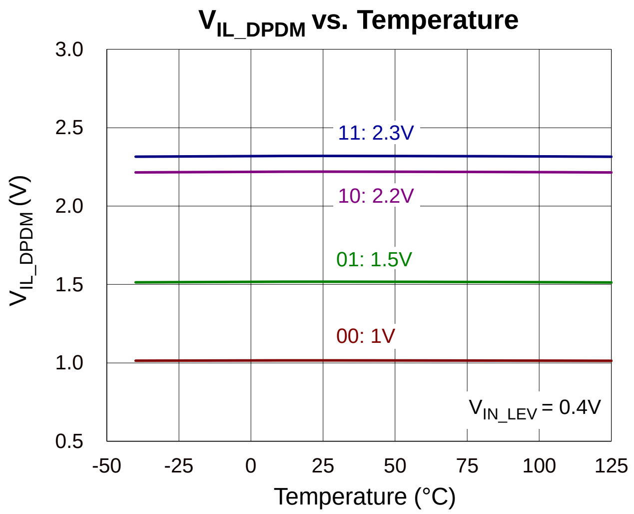

VOH_DPDM vs. Temperature
11: 4.6V
01: 3.3V
10: 1.8V
VOH_DPDM (V)
Temperature (°C)

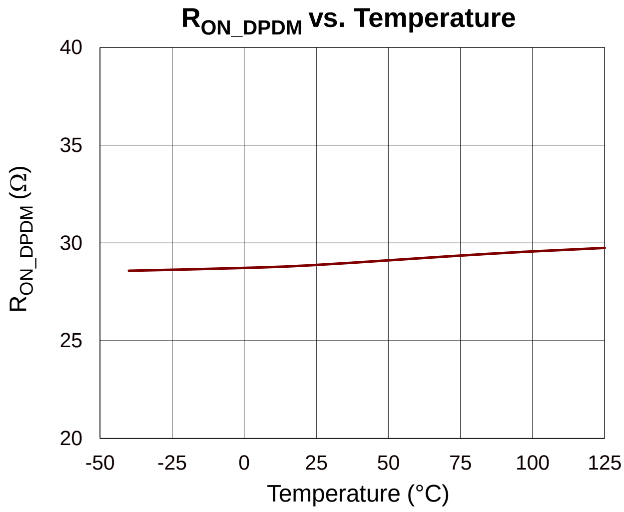

VOL_DPDM vs. Temperature
VOL_DPDM (V)
Temperature (°C)

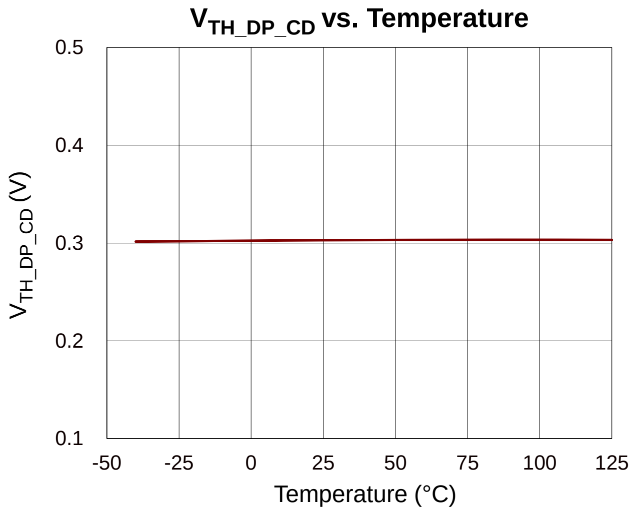

VIH_DPDM vs. Temperature
11: 2.1V
10: 1.9V
01: 1.3V
00: 0.8V
VIN_LEV = 0V
VIH_DPDM (V)
Temperature (°C)

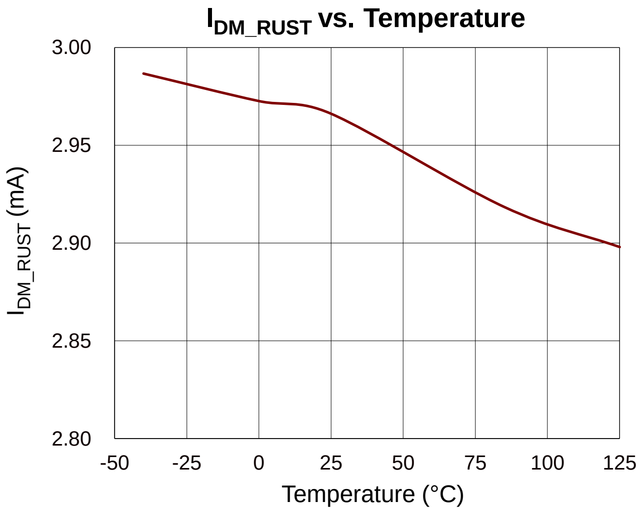

VIH_DPDM vs. Temperature
11: 2.5V
10: 2.3V
01: 1.7V
00: 1.2V
VIN_LEV = 0.4V
VIH_DPDM (V)
Temperature (°C)

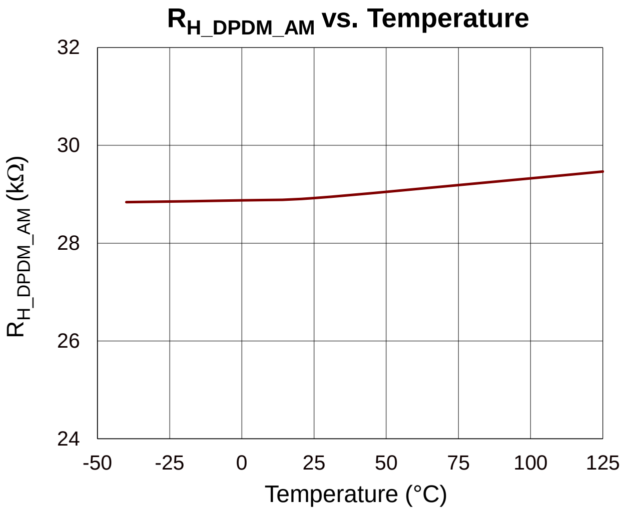

VIL_DPDM vs. Temperature
11: 1.9V
10: 1.8V
01: 1.1V
00: 0.6V
VIN_LEV = 0V
VIL_DPDM (V)
Temperature (°C)

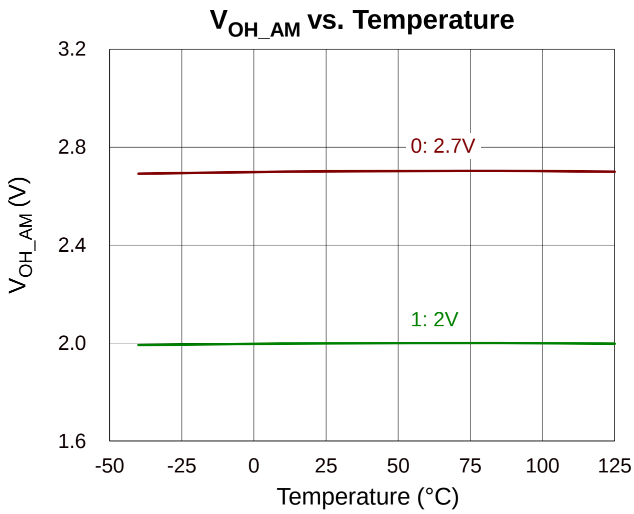

VIL_DPDM vs. Temperature
11: 2.3V
10: 2.2V
01: 1.5V
00: 1V
VIN_LEV = 0.4V
VIL_DPDM (V)
Temperature (°C)

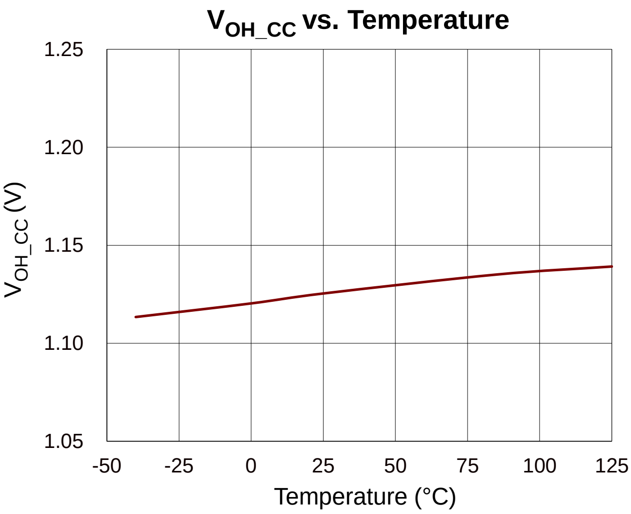

R_ON_DPDM vs. Temperature
40
35
30
25
20
R_ON_DPDM (Ω)
-50
-25
0
25
50
75
100
125
Temperature (°C)

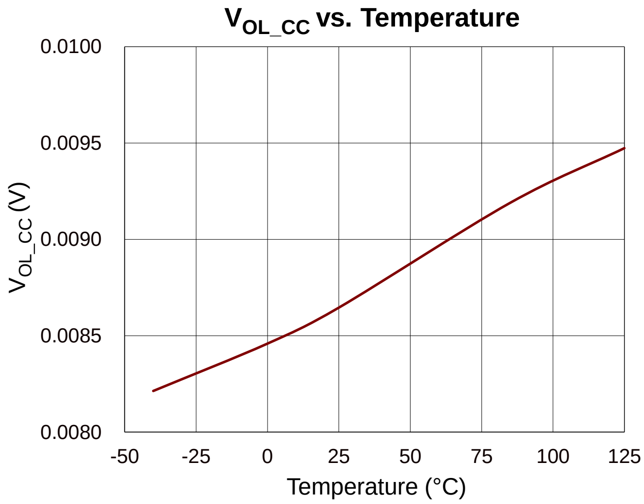

V_TH_DP_CD vs. Temperature
0.5
0.4
0.3
0.2
0.1
V_TH_DP_CD (V)
-50
-25
0
25
50
75
100
125
Temperature (°C)

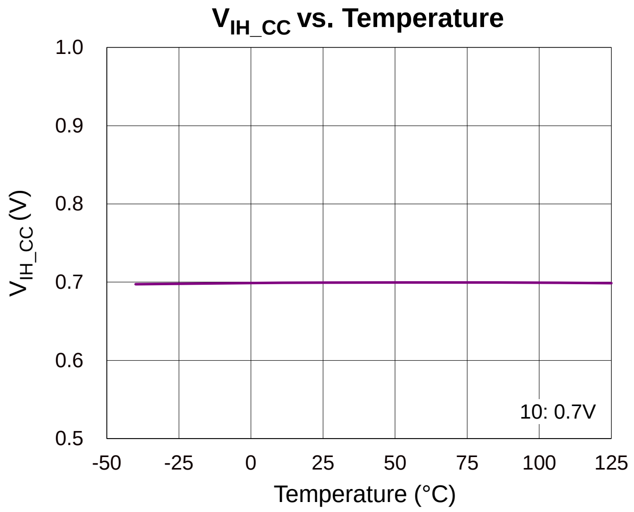

I_DM_RUST vs. Temperature
3.00
2.95
2.90
2.85
2.80
I_DM_RUST (mA)
-50
-25
0
25
50
75
100
125
Temperature (°C)

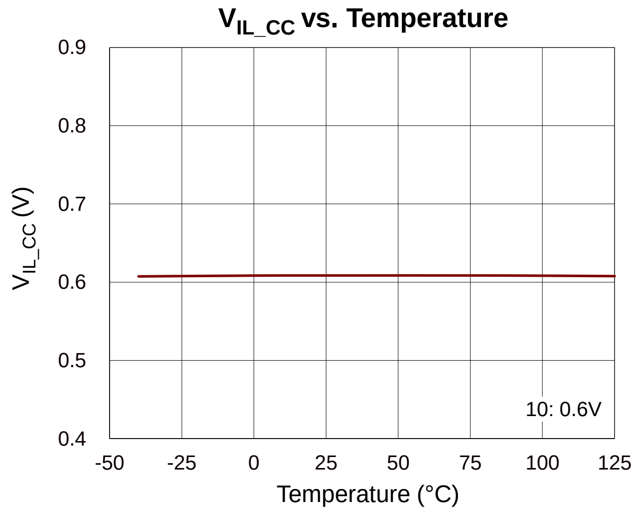

R_H_DPDM_AM vs. Temperature
32
30
28
26
24
R_H_DPDM_AM (kΩ)
-50
-25
0
25
50
75
100
125
Temperature (°C)

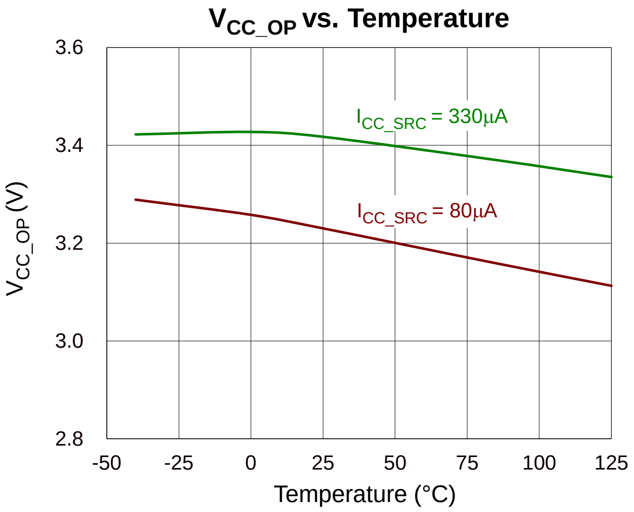

V_OH_AM vs. Temperature
3.2
2.8
2.4
2.0
1.6
V_OH_AM (V)
0: 2.7V
1: 2V
-50
-25
0
25
50
75
100
125
Temperature (°C)

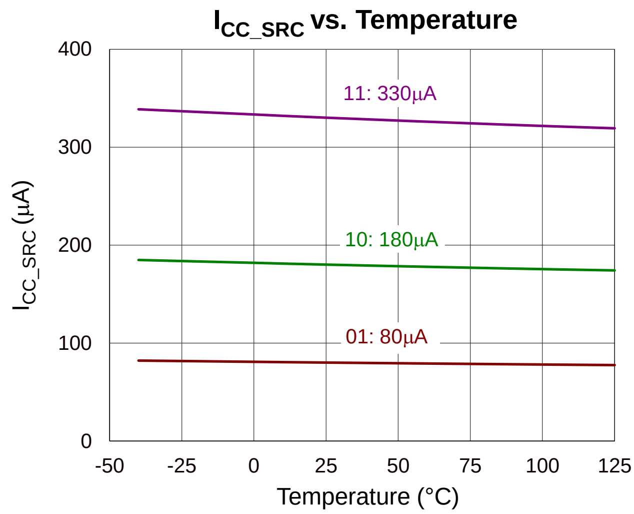

V_OH_CC vs. Temperature
1.25
1.20
1.15
1.10
1.05
V_OH_CC (V)
-50
-25
0
25
50
75
100
125
Temperature (°C)

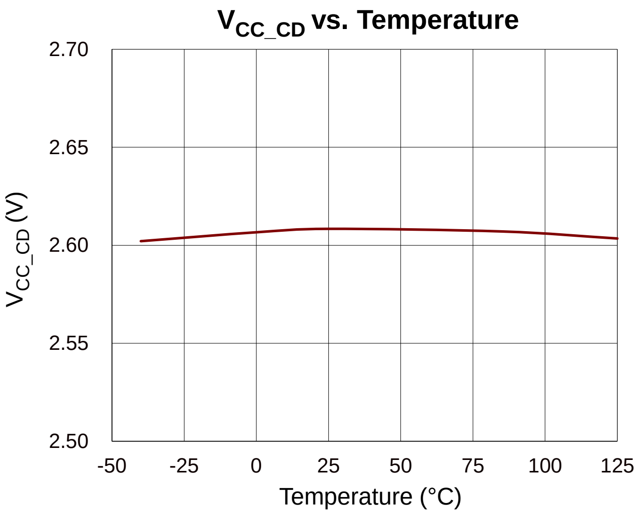

V_{OL_CC} vs. Temperature
0.0100
0.0095
0.0090
0.0085
0.0080
V_{OL_CC} (V)
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{IH_CC} vs. Temperature
1.0
0.9
0.8
0.7
0.6
0.5
V_{IH_CC} (V)
10: 0.7V
-50 -25 0 25 50 75 100 125
Temperature (°C)

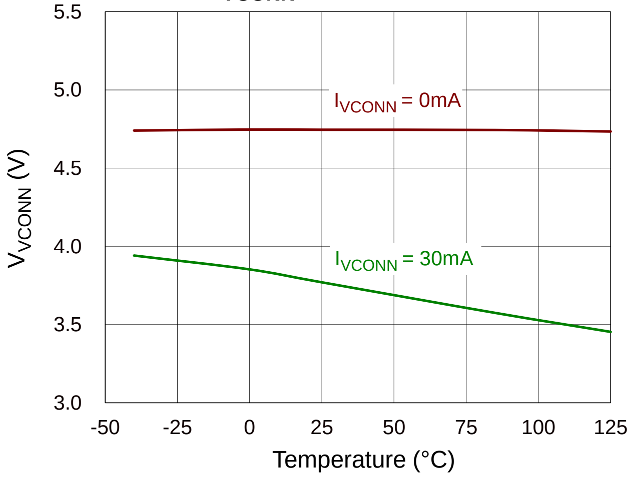

V_{IL_CC} vs. Temperature
0.9
0.8
0.7
0.6
0.5
0.4
V_{IL_CC} (V)
10: 0.6V
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{CC_OP} vs. Temperature
3.6
3.4
3.2
3.0
2.8
V_{CC_OP} (V)
I_{CC_SRC} = 330μA
I_{CC_SRC} = 80μA
-50 -25 0 25 50 75 100 125
Temperature (°C)

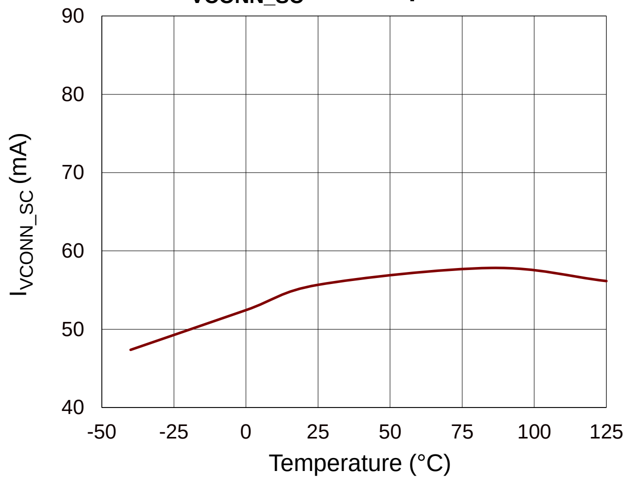

I_{CC_SRC} vs. Temperature
400
300
200
100
0
I_{CC_SRC} (μA)
11: 330μA
10: 180μA
01: 80μA
-50 -25 0 25 50 75 100 125
Temperature (°C)


V_{CC_CD} vs. Temperature
2.70
2.65
2.60
2.55
2.50
V_{CC_CD} (V)
-50 -25 0 25 50 75 100 125
Temperature (°C)

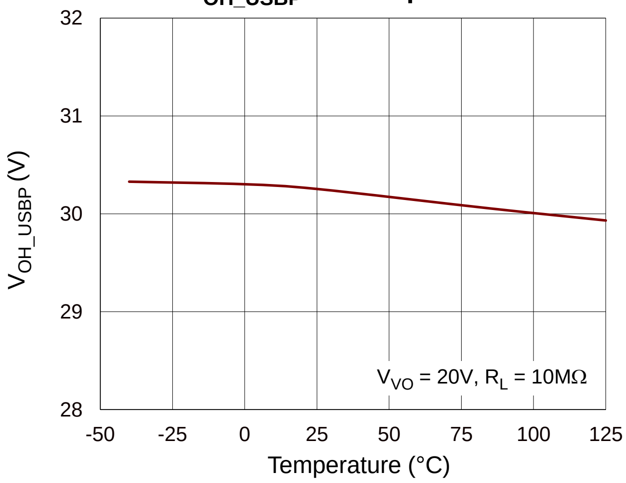
V_{VCONN} vs. Temperature



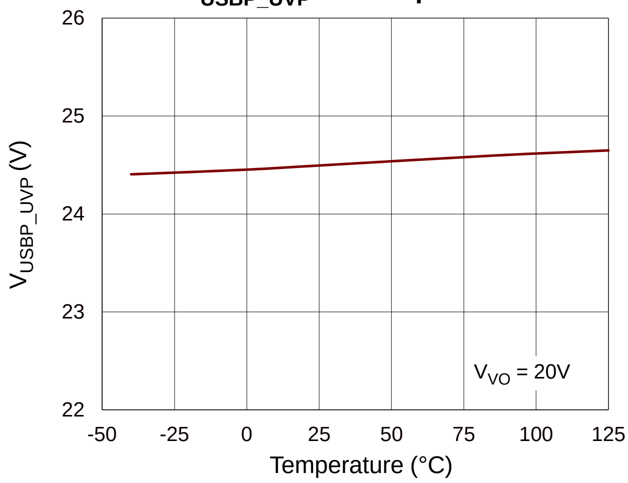
I_{VCONN_SC} vs. Temperature



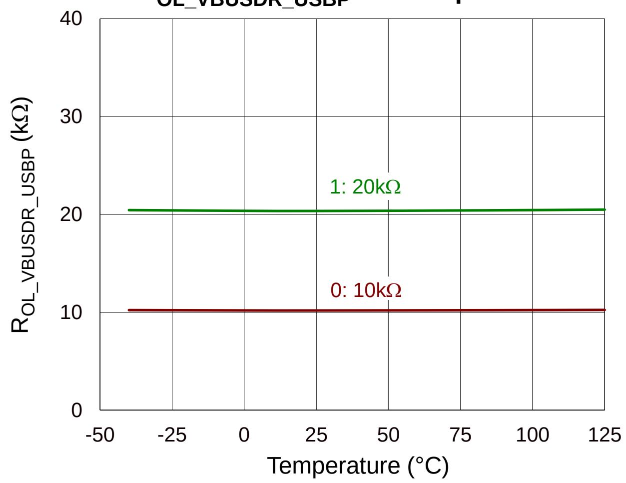
V_{OH_USBP} vs. Temperature



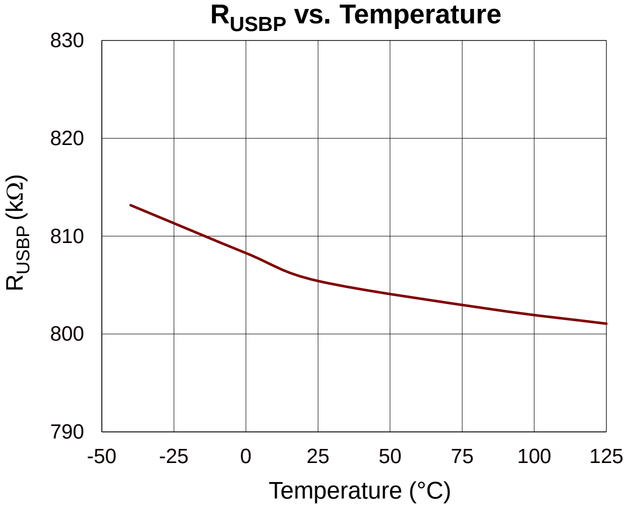
V_{USBP_UVP} vs. Temperature



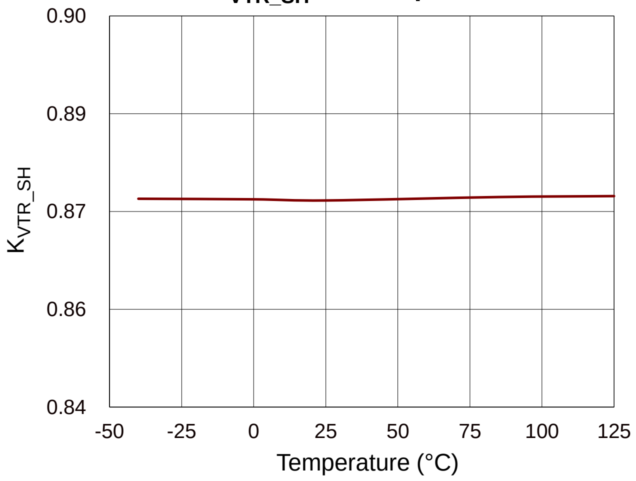
$R_{OL\_VBUSDR\_USBP}$ vs. Temperature



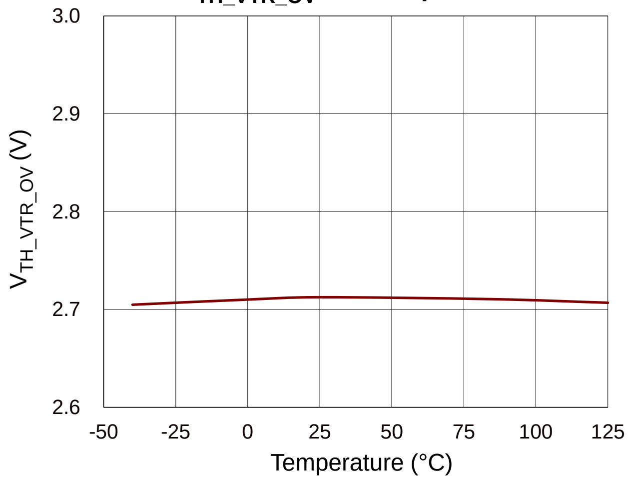
R_{USBP} vs. Temperature



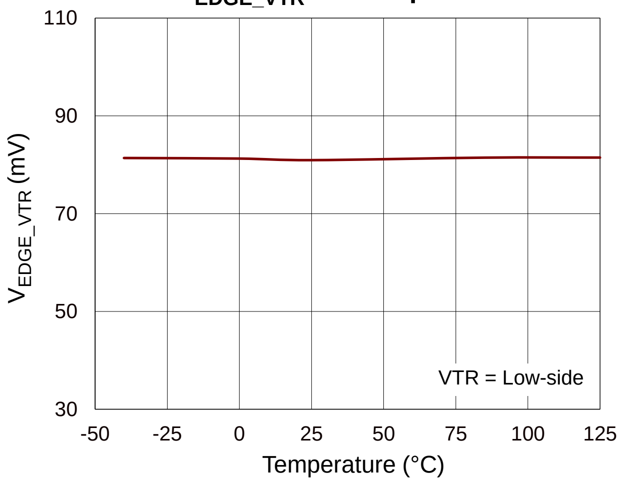
K_{VTR_SH} vs. Temperature



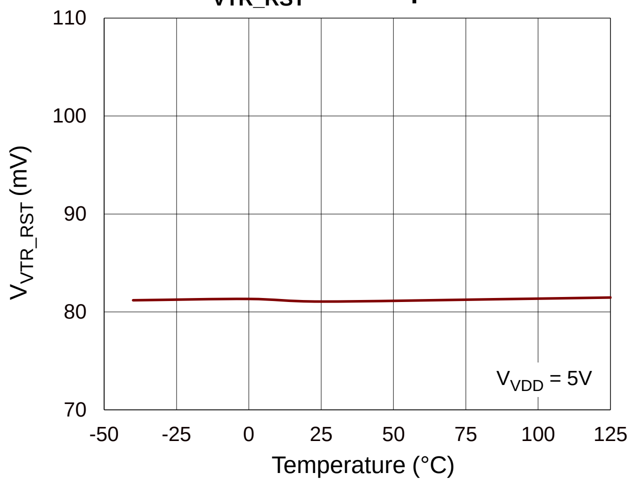
$V_{TH\_VTR\_OV}$ vs. Temperature



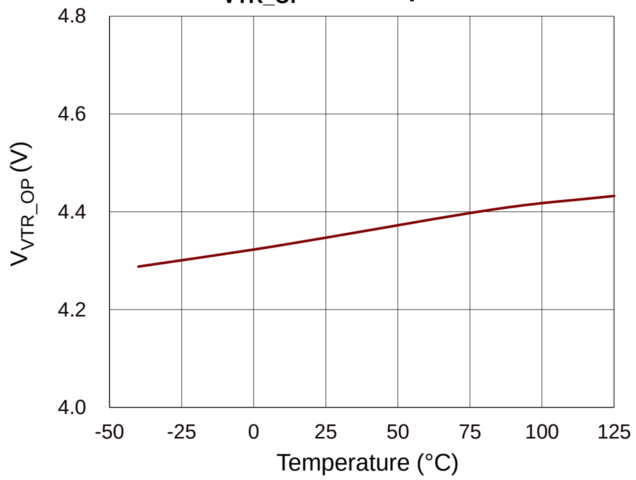
V_{EDGE_VTR} vs. Temperature



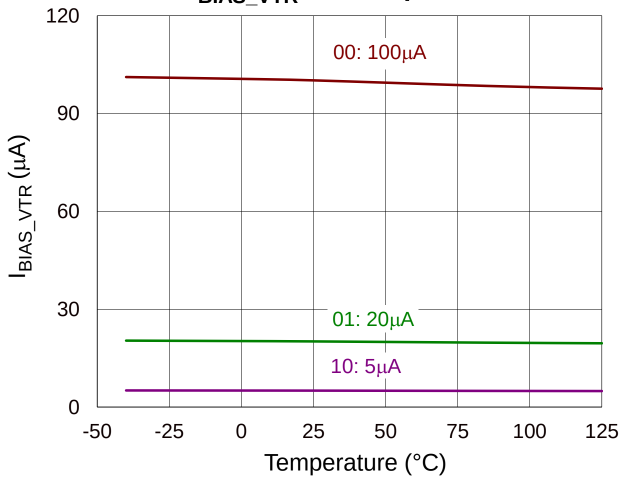
V_{VTR_RST} vs. Temperature

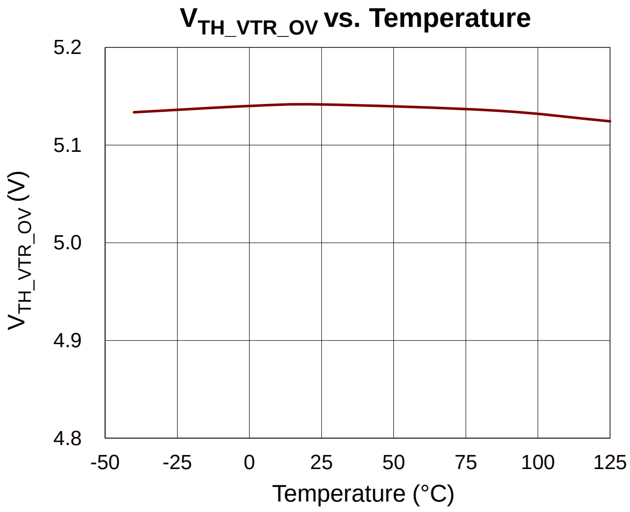


V_{VTR_OP} vs. Temperature



I_{BIAS_VTR} vs. Temperature





$V_{TH\_VTR\_OV}$ vs. Temperature
5.2
5.1
5.0
4.9
4.8
$V_{TH\_VTR\_OV}$ (V)
-50
-25
0
25
50
75
100
125
Temperature (°C)

16 Operation

The RT7209 is a highly integrated programmable secondary side PD controller, providing various functions and comprehensive protections for off-line AC-DC converters.

16.1 Power Structure

The internal V5 and V2 regulated voltages, biased by the VDD of the RT7209, are used to supply the internal circuit and the internal microprocessor (MCU), respectively.

16.2 Constant Voltage and Constant Current (CV/CC) Regulators

The RT7209 has two transconductance amplifiers connected in parallel to the feedback compensator. The feedback compensator sources a current at the OPTO pin to regulate the output voltage and the output current. Note that the operation of each feedback loop is opposite to that of the traditional TL431 shunt regulator.

The OPTO pin is in high impedance state if the VDD voltage is still below the VDD turn-on threshold (V_{VDD_ON}), which ensures a smooth power-on sequence. The reference voltages, V_{REF_CV} and V_{REF_CC}, of the voltage feedback loop and the current feedback loop are programmable analog output voltages of 11-bit DAC. For the V_{OUT} scaling factor K_{FB} of 10, the resolution of DAC output voltage for CV is 10mV; for the K_{FB} of 25, the resolution of DAC output voltage for CV is 25mV, which can achieve high precision CV regulation.

16.3 Current Sense Amplifier

To minimize the power loss of the current sense resistor, a low input offset amplifier with voltage gain of 20 or 40 is used. When the 5mΩ (typical) RCS is used with the voltage gain of 40, the resolution of the output current is around 5mA. The operation of the CV and CC loops is shown in Figure 1.

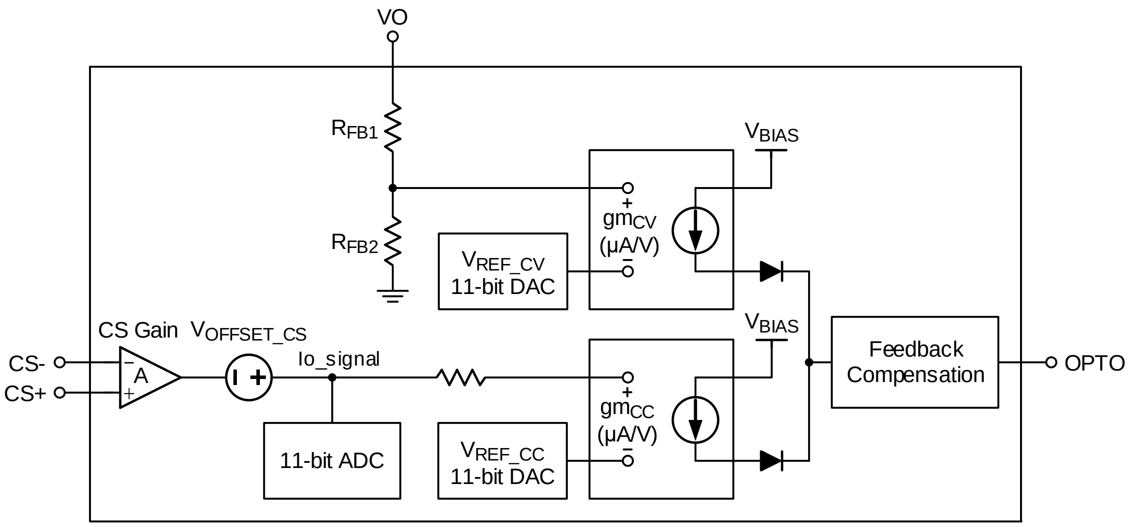


Figure 1. CV and CC Loops

16.4 External Temperature Sensing

As shown in Figure 2, the RT7209 provides the RT pin as a programmable current source to bias a remote thermal sensor, such as a thermistor (NTC). If the RT voltage is below the over-temperature protection (OTP) threshold and the condition sustains for a programmed delay time, the OTP will be triggered.

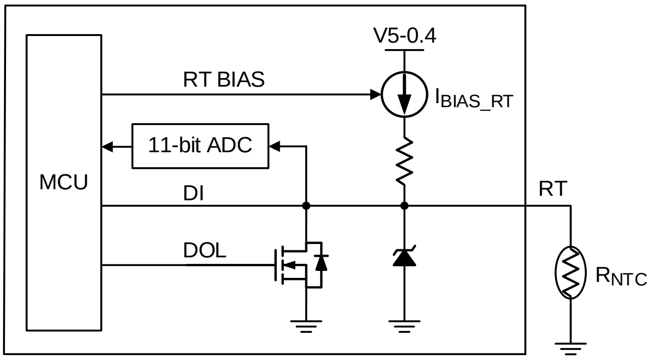


Figure 2. External Temperature Sensing

16.5 Interface of D+ and D-

The D+ and D- pins are used for BC1.2 compliance or for communication with other proprietary protocols. The D+ and D- pins, connected to the MCU by an ADC, can be re-programmed for other purposes since they can be used as analog/digital inputs or outputs, as shown in Figure 3.

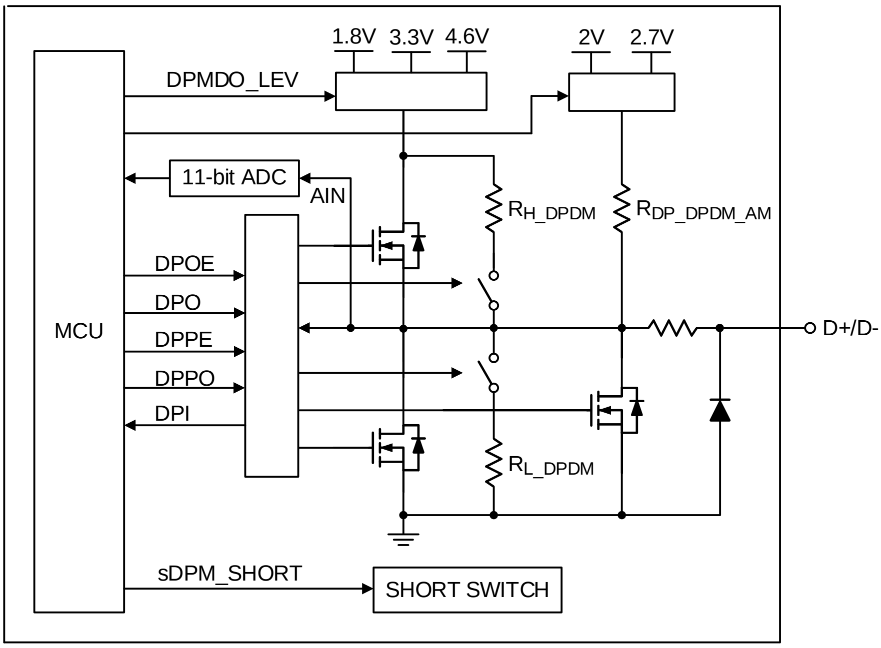


Figure 3. Interface of D+ and D-

16.6 Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with the USB Type-C specification. When configured as a source port, three current capabilities of 80μA, 180μA, and 330μA, provided by each of the CC pin, will be advertised to a device as the default USB current, 1.5A, and 3.0A, respectively. The interface of CC1 and CC2 is shown in Figure 4.

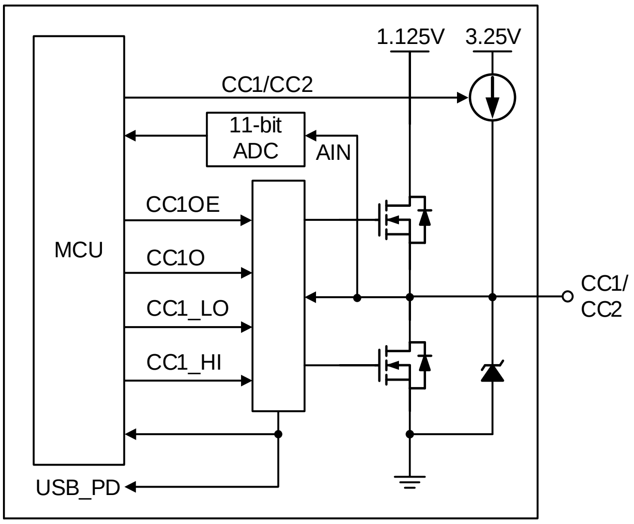


Figure 4. Interface of CC1 and CC2

16.7 Open-Drain Driver of The VBUS Pin

Figure 5 shows the VBUS pin with open-drain drivers. The internal bleeder circuit at the VBUS pin is used to discharge the VBUS capacitor when the cable is detached from a device or when protection is triggered.

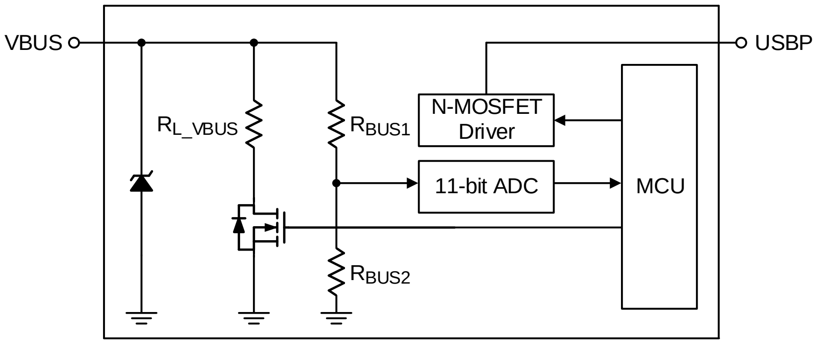


Figure 5. Open Drain Driver of the VBUS Pin

16.8 USBP Clamp

To prevent the blocking MOSFET from causing a negative VGS voltage that exceeds specifications during turn-off, a clamp circuit is needed as shown in Figure 6.

The RT7209GQW features an internal USBP clamp circuit to minimize the number of external components. This function necessitates that the VBUS ADC senses a voltage less than 20V before the firmware enables VBUS to pull low. Additionally, the external resistor of the VBUS pin must be equal to 0.5kΩ.

The RT7209BGQW does not have an internal USBP clamp feature; therefore, an external diode is required to solve the negative voltage issue. The external resistor of the VBUS pin is set to 1.5kΩ by default

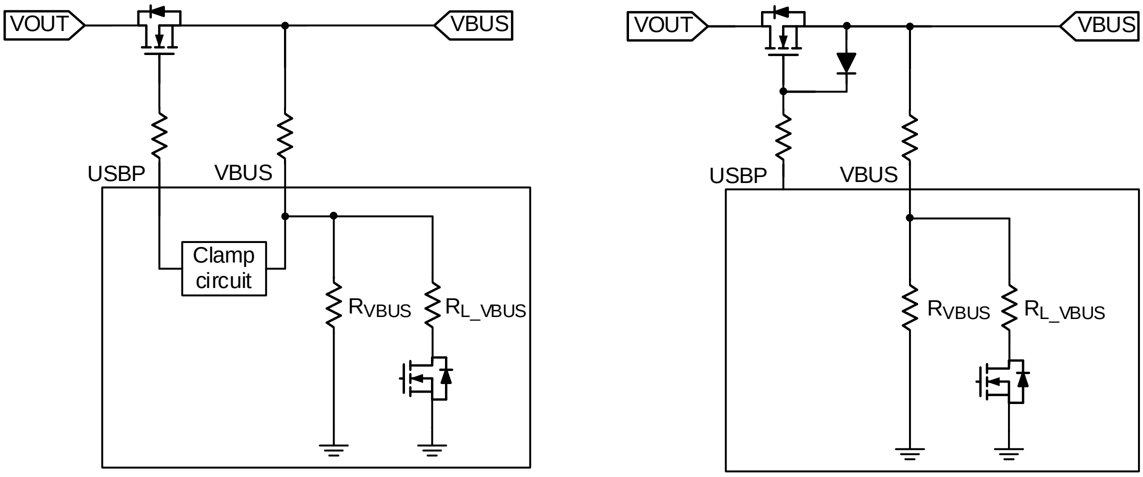


Figure 6. USBP Clamp Circuit

16.9 I²C Communication

The RT7209 can share the output power through Master/Slave I²C communication by connecting GPIO2/D- (SDA) and GPIO3/D+ (SCL) to the other IO pins of the RT7209, respectively. The interface for I²C communication is shown in Figure 7. (Note 2)

16.10 Capability Selector in Sink Application

When the RT7209 is utilized in a sink port, two methods are implemented to set the corresponding capabilities. The embedded ADCs in VBUS, RT, VTR, GPIO1, D+ and D- measure the related voltages, V_{BUS}, V_{RT}, V_{VTR}, V_{GPIO1}, V_{D+} and V_{D-} as the analog inputs for setting the voltage and power capabilities. In addition, if the I²C communication is connected to a host controller by GPIO2/D- and GPIO3/D+, the capabilities can be set directly by the host controller.

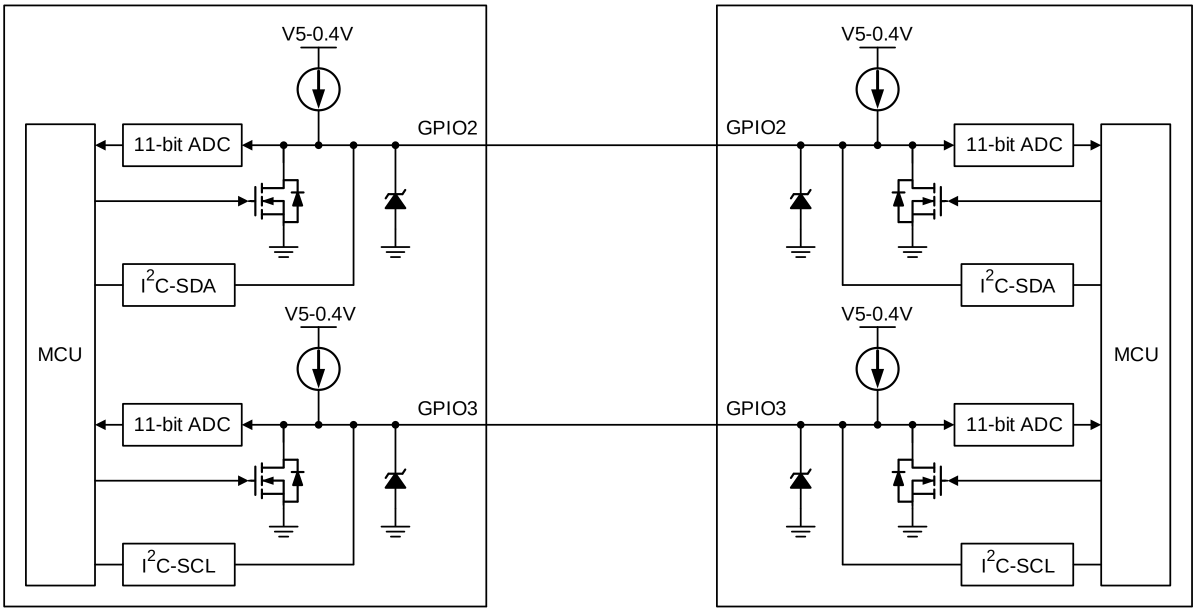


Figure 7. Interface for I²C Communication

17 Application Information

(Note 8)

17.1 Constant Voltage (CV) Loop

As shown in Figure 8, the RT7209 integrates two transconductance amplifiers, which are connected to the feedback compensation to regulate the output voltage and current, respectively. The output voltage is determined as:

$V_{OUT} = K_{FB} \times V_{REF\_CV}$

where $K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2} = 10, 25$

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, which is controlled by the MCU.

17.2 Constant Current (CC) Loop

As shown in Figure 8, the RT7209 integrates a virtually zero input offset current-sense amplifier with differential mode inputs to minimize noise interference. The voltage gain of 20 or 40 can be set by the internal register. The sensed signal, I_{O_signal}, is fed into an 11-bit ADC to be monitored and processed by the MCU. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed by the requirements of charger.

The constant voltage and the constant current compensation loops are both connected to the feedback compensation. The OPTO driver sources current through an external resistor R_{OPTO} and an optocoupler that isolates the secondary side from the primary side and then feeds back the compensation signal to the primary side. Note that for better linearity of the loop compensation range, R_{OPTO} should be designed to cover the operation at the minimum output voltage.

$$\frac{(V_{OPTO\_MAX} - V_F)}{R_{OPTO}} \times CTR \geq I_{COMP\_MAX}$$

where

CTR: Current transfer ratio of the optocoupler;

V_F: Forward voltage of the optocoupler;

V_{OPTO_MAX}: The maximum OPTO voltage for the OPTO driver to source 1mA;

I_{COMP_MAX}: The maximum COMP sourcing current of a traditional PWM controller on the primary side. It is a current sourced from an internal bias through a built-in pull-high resistor connected to the COMP pin in the PWM controller.

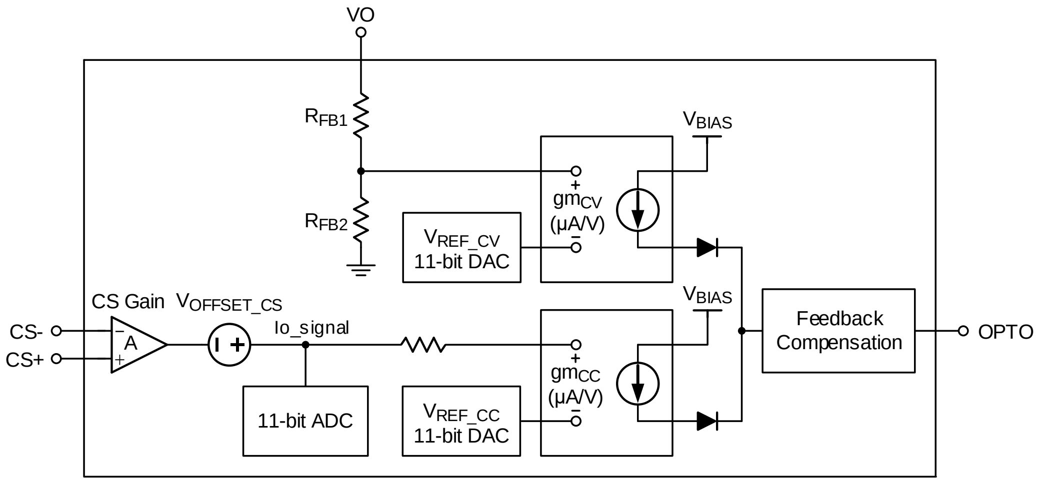


Figure 8. CV and CC Loops

17.3 Internal Feedback Compensation

The RT7209 has a built-in feedback compensator that optimizes system stability and response for different applications and furthermore reduces the external component counts. The feedback compensation design is based on the system operation mode and component parameters. In general, converters mostly use a Type-II compensator to compensate for the feedback loop. It has a zero frequency pole, a low frequency zero and a high frequency pole. The feedback compensation design is to make the low frequency zero point of the compensator compensate for the low frequency pole point of the system and make the high frequency pole point compensate for the ESR zero point of the output capacitor. With proper compensation, the system can achieve a better phase margin. In addition, a proper middle gain of the compensator is chosen to get a better transient response and improve system stability.

The RT7209 provides a simple and flexible design for feedback compensation. The R_Z, C_Z and middle gain of the compensator can be programmed according to different output conditions. With this feature, one can easily achieve a stable system by using this flexible design for compensation.

17.4 Power-Up Sequence

Figure 9 shows the timing diagram for the power-up sequence. When start-up, the default output voltage is set at 5V. Once a Type-C cable is attached, the UFP will deliver voltage and current settings to the RT7209 for the MCU to decode and to program reference voltages, V_{REF_CV} and V_{REF_CC}, for the CV and CC loops, which are the analog outputs converted by the DAC. If the Type-C cable is detached, or the output current is lower than the power-saving mode threshold, which is typically programmed as 200mA, the RT7209 will enter the power-saving mode, under which the RT7209 operates at ultra-low operating current and thus the total input power can be tremendously saved. Meanwhile, if the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, the RT7209 will exit from the power-saving mode.

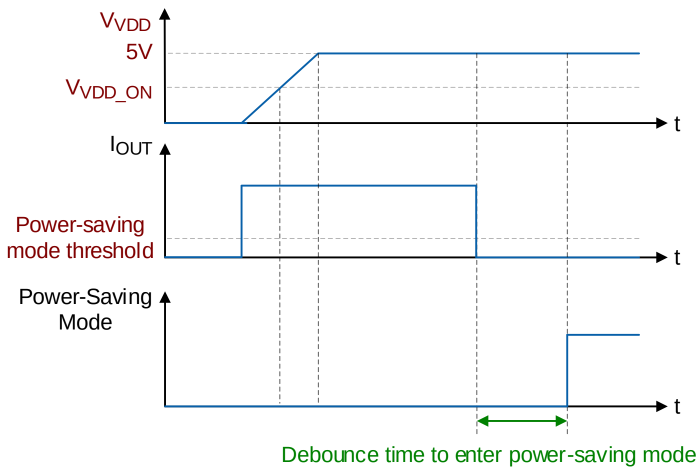
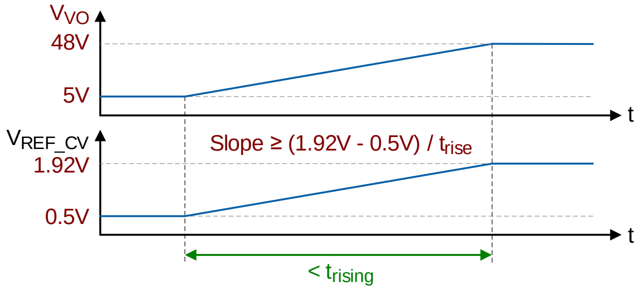


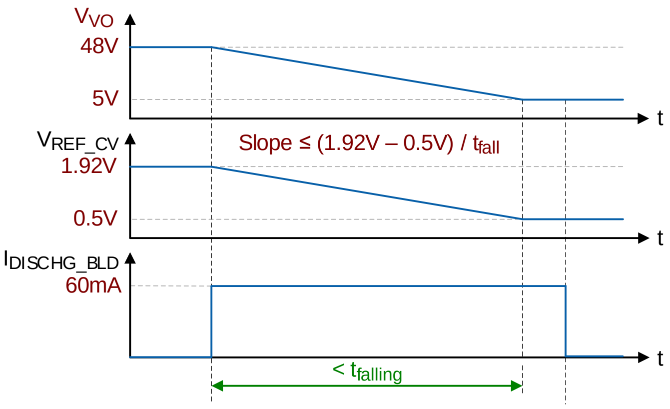
Figure 9. The Bias Voltages Sequence during Start-Up

17.5 Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of the UFP. Both the rise time and fall time of output voltages should be less than the defined specification, as shown in Figure 10.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 10. Output Voltage Transient Waveforms

The RT7209 provides control for the discharge constant current or fully-on from the BLD pin. This function utilizes a bleeder to help discharge the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as VOUT from 48V to 5V. The discharge current can be programmed by the internal register according to VDD voltage level, as shown in Figure 11.

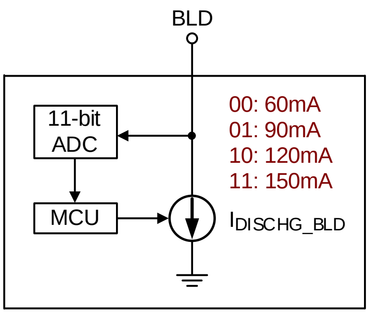


Figure 11. Discharge Current Control from the BLD Pin

17.6 Linear Cable Compensation

The RT7209 adjusts the feedback control voltage (V_{FB}) based on the output current to implement a linear cable compensation, as shown in Figure 12. The transconductance amplifier gain (gm_{COMP}) and the cable compensation gain (K_{CC}) can be set by the internal register.

$$V_{CABLE\_COMP} = I_{OUT} \times K_{CS} \times K_{CC} \times gm_{COMP} \times R_{FB1}$$

where

K_{CS}: Current sense gain

K_{CC}: Cable Compensation Gain

gm_{COMP}: Transconductance amplifier gain

R_{FB1}: V_{VO} upper divider resistor

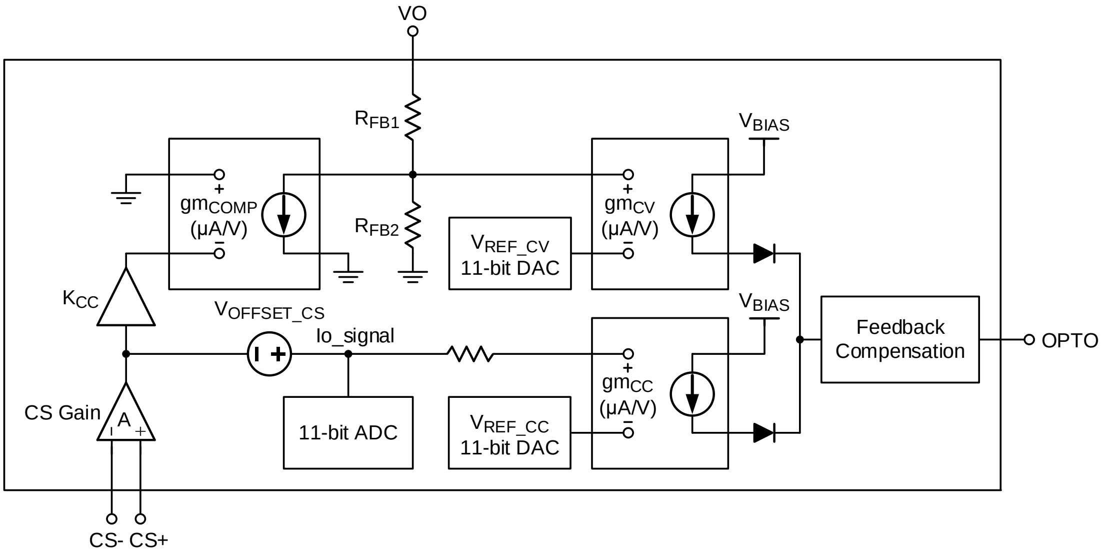


Figure 12. Linear Cable Compensation

17.7 Output Overvoltage Protection

As shown in Figure 13 and Figure 14, the RT7209 provides a fast turn-off blocking N-MOSFET as a backup VOUT overvoltage protection, in case the optocoupler of the feedback loop malfunctions due to aging. If the internal voltage related to VO is higher than the programmable threshold V_{VO_OVP}, the blocking N-MOSFET will be turned off. The OPTO pin voltage will be latched high until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

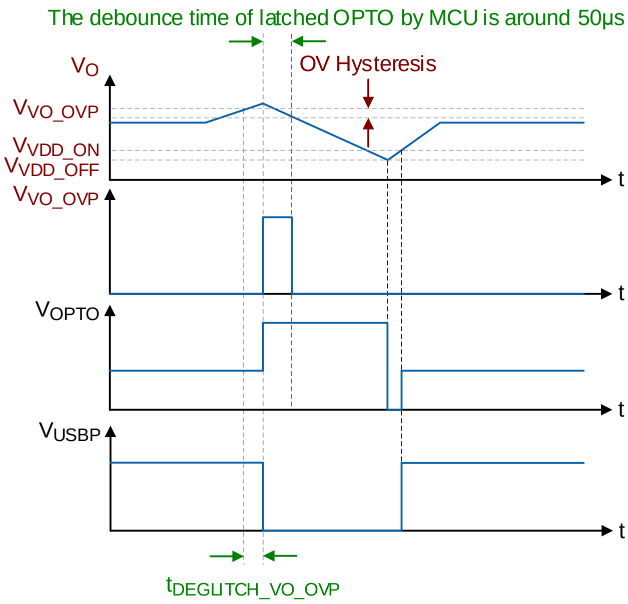


Figure 13. Timing Sequence of the OVP Function

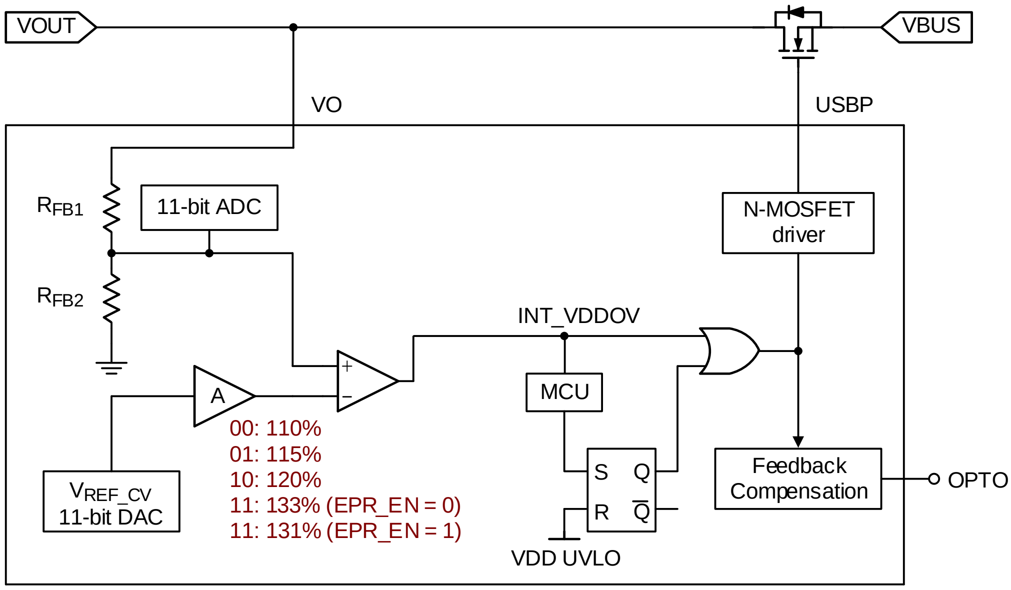


Figure 14. OVP Functional Diagram

17.8 Blocking N-MOSFET Control

The RT7209 provides a charge-pump driver for controlling an external blocking N-MOSFET, as shown in Figure 15. The blocking N-MOSFET can be quickly turned off in any fault condition. Once the communication is set up with a UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector is detected, the N-MOSFET will be turned on. If a VOUT overvoltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged. When VOUT is shorted to GND, the N-MOSFET will be turned off automatically and the output power will be limited.

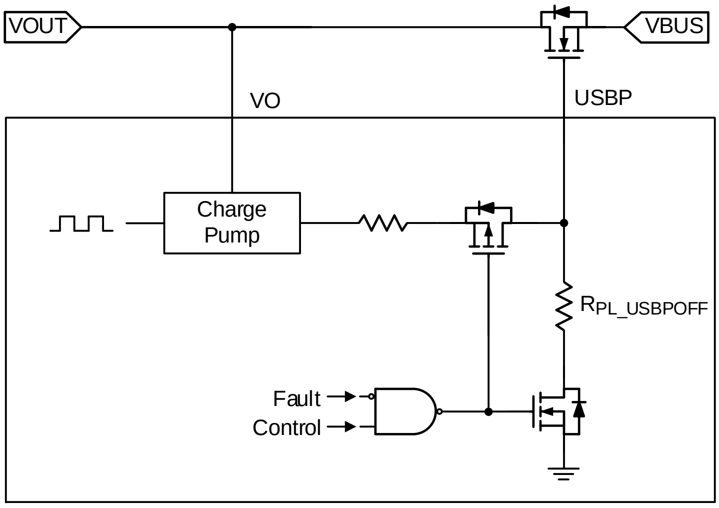


Figure 15. Blocking N-MOSFET Control

17.9 VBUS Drop Protection

VBUS drop protection provides another mechanism to protect against output short circuit, as shown in Figure 16. It is used to detect the voltage difference between the VBUS pin and the VO pin. When the voltage difference exceeds the VBUS drop threshold, the blocking N-MOSFET will be clamped off immediately. The external resistance of VBUS also creates a voltage difference with the internal R_{VBUS}. To avoid triggering VBUS drop protection erroneously, it is recommended that the external resistance be smaller than 1.5kΩ when VBUS drop function is enabled and pay attention to not exceed the current I_{VBUS_DIS} during VBUS discharge.

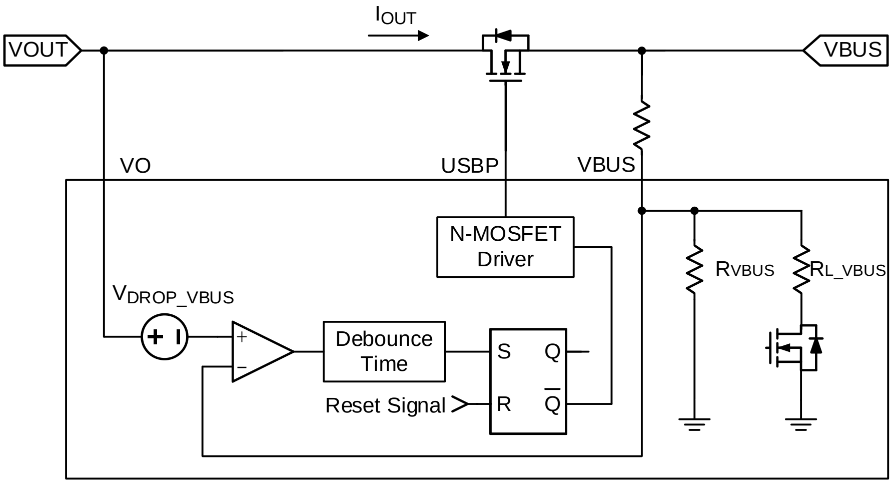


Figure 16. VBUS Drop Protection

17.10 Temperature Sensing and Thermal Protection

The RT7209 provides the RT pin for over-temperature protection or thermal monitoring. The RT pin sources a constant bias current for a remote thermal sensor, such as an NTC thermistor, connected from the RT pin to GND, for temperature sensing. If the RT voltage is below a programmable threshold voltage and the condition sustains for a programmable deglitch time, the over-temperature protection is triggered.

The bias current through the RT pin can be programmed as 100μA, 20μA, or 5μA. With the appropriate bias current setting, the linearity of temperature sensing over the range from 25°C to 100°C can be enhanced. The RT7209 can deliver the sensed RT voltage signal to the device via the protocol, if necessary. Figure 17 shows the RT voltages varying with temperature at three different bias currents with an NTC thermistor TTC104 as an example.

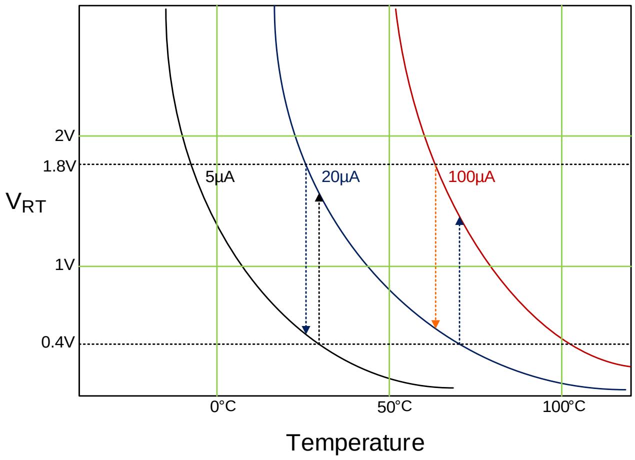


Figure 17. The RT Voltages vs. Temperature at Three Bias Currents

17.11 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-28L 4x5 package, the thermal resistance, θ_{JA}, is 70.65°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (70.65°C/W) = 1.42W for a WQFN-28L 4x5 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 18 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

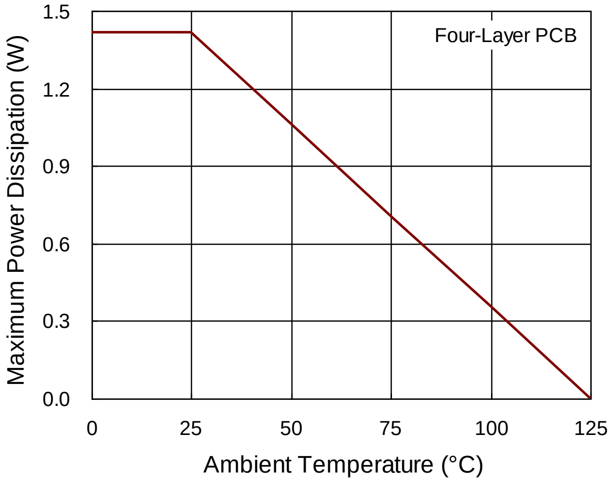
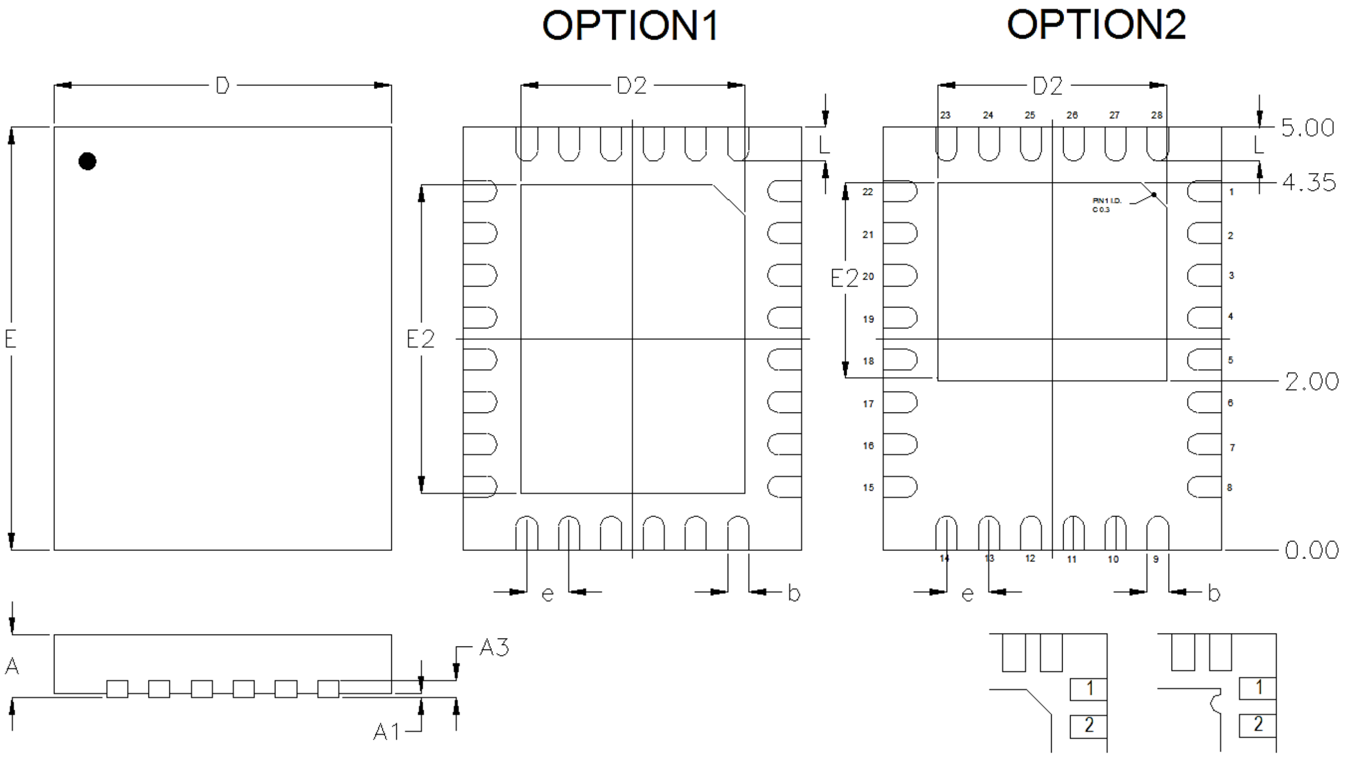


Figure 18. Derating Curve of Maximum Power Dissipation

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

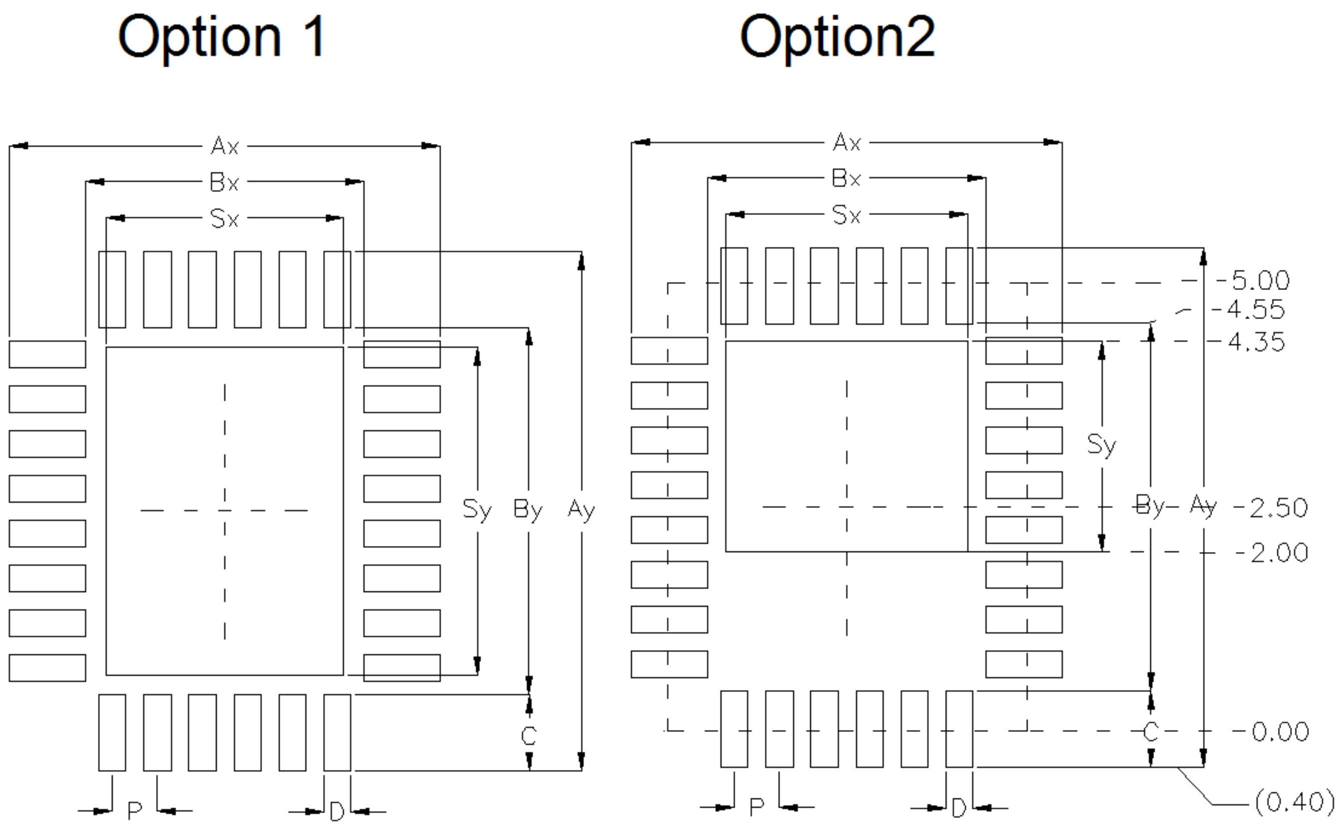
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.900	4.100	0.154	0.161
D2	Option1	2.600	2.700	0.102	0.106
	Option2	2.650	2.750	0.104	0.108
E		4.900	5.100	0.193	0.201
E2	Option1	3.600	3.700	0.142	0.146
	Option2	2.300	2.400	0.091	0.094
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 28L QFN 4x5 Package

Note 9. The package of the RT7209 uses Option 1.

19 Footprint Information

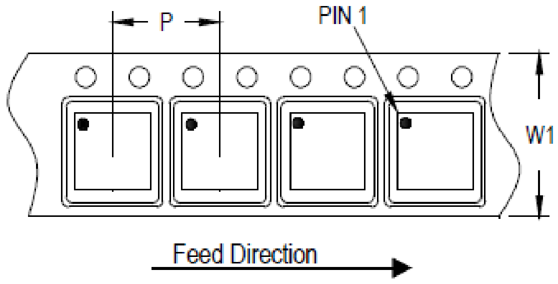


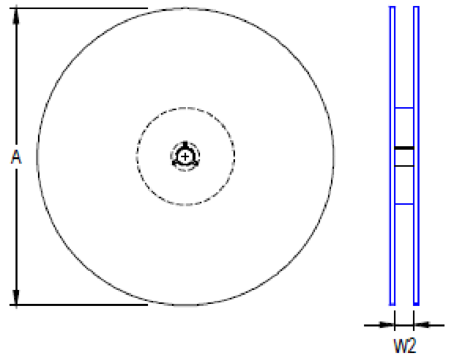
Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4x5-28	Option1	28	0.50	4.80	5.80	3.10	4.10	0.85	0.30	2.65	3.65	±0.05
	Option2									2.70	2.35	

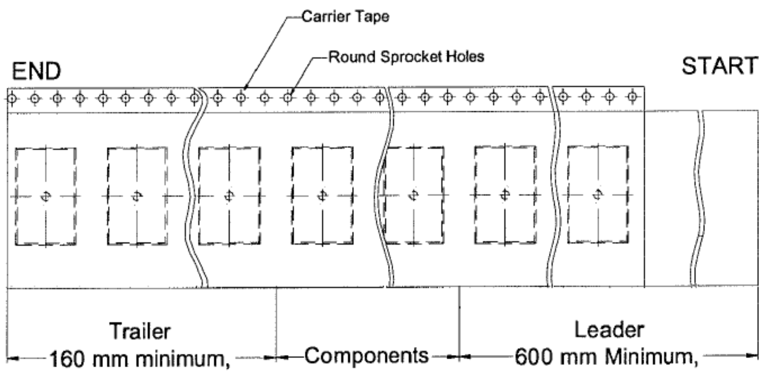
Note 10. The package of the RT7209 uses Option 1.

20 Packing Information

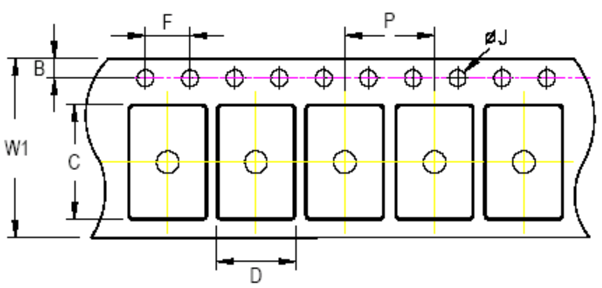
20.1 Tape and Reel Data

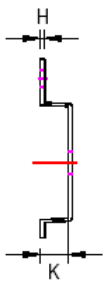






Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x5	12	8	180	7	1,500	160	600	12.4/14.4





C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 4x5	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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21 Datasheet Revision History

Version	Date	Description	Item
00	2024/11/7	Final	*General Description on page 1* - Modified operation voltage range *Ordering Information on page 1* - Added Application code and note *Features on page 1* - Modified operation voltage range *RT7209 Version Table on page 2* - Added version table *RT7209 Functional Table on page 2* - Modified output voltage supported range *Simplified Circuit in Sink Application on page 3* - Added pull low resistor to CC1/CC2 *Note 4 on page 8* - Modified description *Functional Pin Description on page 5, 6* - Modified description *Functional Block Diagram on page 7* - Modified Block diagram about I^2C and UART *Absolute Maximum Ratings on page 8* - Added VDD, VBUS, VO, BLD to GND voltage unit - Added V5 spec *Recommended Operating Conditions on page 8* - Modified the range of VDD *Electrical Characteristics on page 8 to 18* - Added spec of I_{BIAS_RT} for the RT7209BQGW - Added spec of I_{BIAS_GP} for the RT7209BQGW - Modified description of I_{VBUS_DIS} - Modified test conditions of R_{L_VBUS} - Modified parameter of V_{OH_USBP} - Modified description of V_{DAC_SLOP} - Added spec of $R_{OL\_USBPOFF}$ for the RT7209BQGW - Added spec of $R_{OL\_UVLO\_USBP}$ for the RT7209BQGW *Typical Application Circuit on page 19* - Modified connection to VTR of typical application circuit in source application *Typical Operating Characteristics on page 21 to 34* - Added typical operating characteristics *Application Information on page 37, 38, 39, 40, 41, 42, 43, 45* - Modified the description of Open-Drain Driver of the VBUS Pin - Added USBP Clamp Section - Modified the description of Internal Feedback Compensation and VBUS Drop Protection - Modified Figure 8, 9, 15, 16, - Modified declaration *Packing Information on page 48, 49* - Updated packing information