RICHTEK®

RT7204E

High-Integration USB Multi-Protocol Controller with Rectification Detection

1 General Description

The RT7204E is a highly integrated, programmable controller that offers multi-protocol support and features high-precision shunt regulators for constant voltage (CV) and constant current (CC) regulation. An embedded MCU is designed to handle customized functions with flexibility, ensuring compatibility with USB PD protocol, Universal Fast Charging Specification (UFCS), and proprietary protocols via the CC1, CC2, D+, and D- interface.

This controller is specifically designed for off-line AC-DC converters to achieve the high power density of a fast charging system. The RT7204E is equipped with rectification detection to sense the AC input voltage and adaptively configure the power rating. Additionally, it monitors the PWM switching state to detect AC OFF conditions. For safety considerations, the RT7204E provides comprehensive protections, including Limited Power Source (LPS) protection and precise internal Over-Temperature Protection (OTP). Furthermore, the RT7204E can also share the output power through I^2C communication for multi-port applications.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

2 Applications

- USB Type-C Controller in Source Applications for Single-Port or Multi-Port Charger / Adapters of Smartphone, Tablet, Notebook, and Other Electronics

3 Features

- **Protocol Support**
  - **USB PD 3.1 and PPS**
  - **Universal Fast Charging Specification (UFCS)**
  - **Proprietary Protocols**
- **Highly Integrated**
  - **Suited for 3V to 21V VDD Range**
  - **Built-In Shunt Regulators for Constant Voltage and Constant Current Control**
  - **Built-In 11-bit Analog-to-Digital Converter (ADC)**
  - **Built-In Linear Regulator**
  - **Built-In Blocking N-MOSFET Driver with Soft-Start for Capacitive Load**
  - **VDD Quick Discharge for Output Capacitor**
  - **Built-In Output Bleeder for Quick VBUS Discharge**
  - **Support High-Side Current Sensing**
  - **Support Programmable Cable Compensation**
  - **Support Input Voltage (V_{IN}) Detection**
  - **Support Slave I^2C Communication**
  - **Built-In V_{CONN} Power and Switches**
  - **<5mA Operating Current in Normal Mode**
  - **<2mA Operating Current in Idle Mode**
  - **<1mA Operating Current in Green Mode**
- **Protection**
  - **VDD Adaptive Output Overvoltage Protection**
  - **VDD Adaptive Undervoltage Protection**
  - **USBP Undervoltage Protection**
  - **CC1/CC2/D+/D-/RT/VTR/GPIO Overvoltage Protection**
  - **Short-Circuit Protection**
  - **Overcurrent Protection**
  - **Constant Current Protection**
  - **Over-Temperature Protection**
  - **Limited Power Source (LPS) Protection**
  - **Internal Over-Temperature Protection**

4 Ordering Information

RT7204E□-□□

- Packing
  - A: Standard
- Programmed Firmware Code AABBX
  - AA: Application Code
  - BB: Model Code
  - X: Customer Approved Version Code
- Package Type(1)
  - N: WQFN-24L 4x4 (W-Type) (Exposed Pad-Option 2)

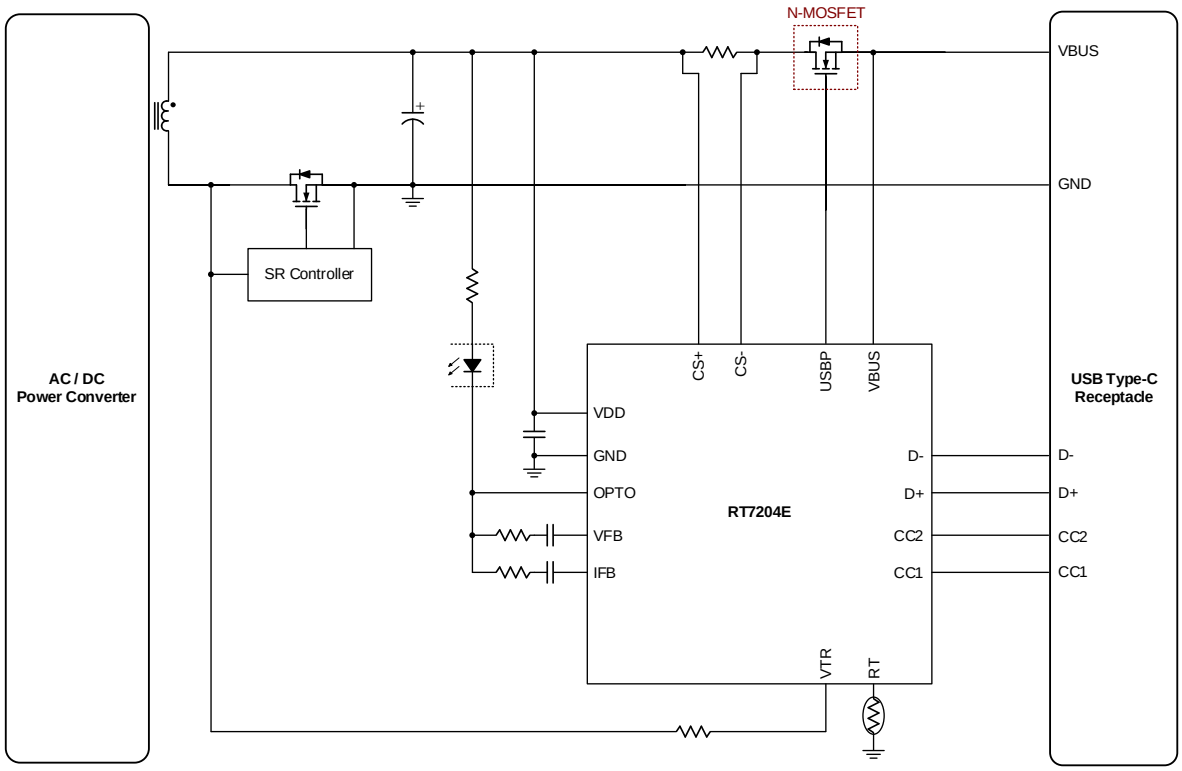
Note 1.

Richtek products are Richtek Green Policy compliant and marked with (1) indicates compatible with the current requirements of IPC/JEDEC J-STD-020.

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit



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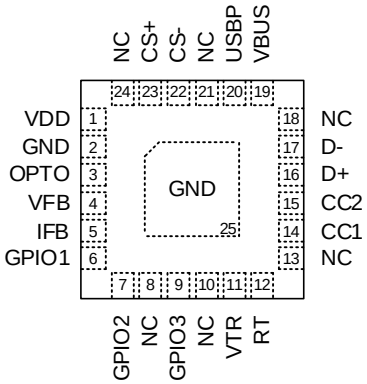
7 Pin Configuration

(TOP VIEW)



WQFN-24L 4x4

8 Functional Pin Description

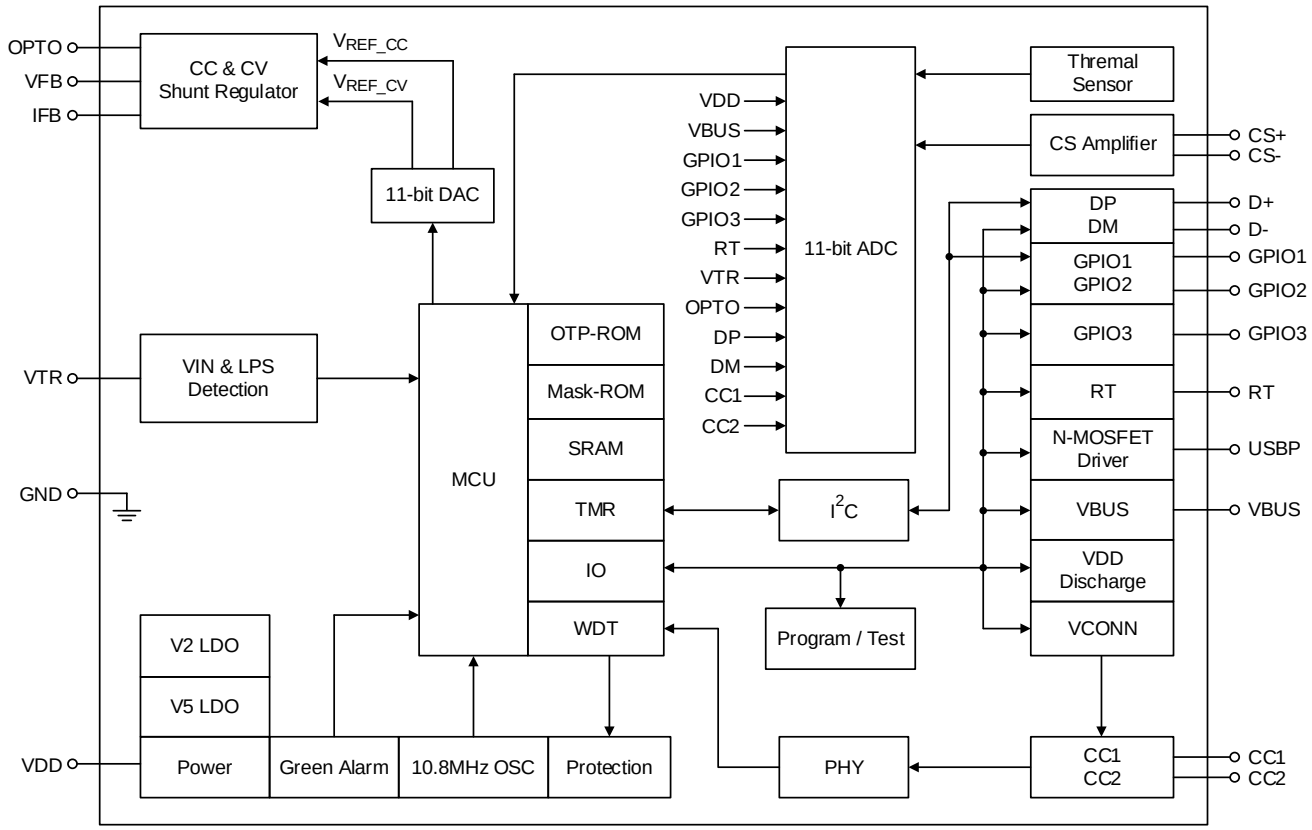
Pin No.	Pin Name	Type	Pin Function
1	VDD	PWR	Supply input voltage.
2	GND	GND	Ground.
3	OPTO	AO	Current sink output for optocoupler connection. Can be configured as open-drain output and ADC input.
4	VFB	AI	Feedback input for constant-voltage loop.
5	IFB	AI	Feedback input for constant-current loop.
6	GPIO1	A/D IO	General purpose input/output. Can be configured as I^2C-SDA, UART_TX/UART_RX, open-drain output, sourcing current, and ADC input.
7	GPIO2	A/D IO	General purpose input/output. Can be configured as I^2C-SCL, UART_TX/UART_RX, open-drain output, sourcing current, and ADC input.
8, 10, 13, 18, 21, 24	NC	NC	No internal connection.
9	GPIO3	A/D IO	General purpose input/output. Can be configured as open-drain output, sourcing current, and ADC input.
11	VTR	AI	Transformer voltage sense node for input voltage detection. Can be configured as open-drain output and ADC input.
12	RT	A/D IO	Remote thermal sensor connection node for over-temperature protection. Can be configured as open-drain output, sourcing current, and ADC input.
14	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
15	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.

Pin No.	Pin Name	Type	Pin Function
16	D+	A/D IO	USB D+ channel for BC1.2 and proprietary protocols. Can be configured as I^2C-SCL, UART_TX/UART_RX, and ADC input.
17	D-	A/D IO	USB D- channel for BC1.2 and proprietary protocols. Can be configured as I^2C-SDA, UART_TX/UART_RX, and ADC input.
19	VBUS	A IO	VBUS sensing and bleeder connection node to provide another path to discharge the VBUS capacitor. Can be configured as ADC input.
20	USBP	D IO	Control signal of the blocking N-MOSFET.
22	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
23	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
25 (Exposed Pad)	GND	GND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

8.1 IO Type Definition

- PWR: Power Pin
- GND: Ground Pin
- AO: Analog Output Pin
- AI: Analog Input Pin
- A IO: Analog Input/Output Pin
- D IO: Digital Input/Output Pin
- A/D IO: Analog/Digital Input/Output Pin
- NC: No Connection Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- USBP to GND ---------- –0.3V to 32V
- VDD, VBUS, OPTO, CS+, CS- to GND ---------- –0.3V to 28V
- VFB, IFB, VTR, RT, GPIO1, GPIO2, GPIO3, CC1, CC2, D+, D- to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-24L 4x4 ---------- 2.52W
- Package Thermal Resistance (Note 3)

  WQFN-24L 4x4, θ_{JA} ---------- 39.6°C/W

  WQFN-24L 4x4, θ_{JC} ---------- 7.1°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD ---------- 3V to 21V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.8	2.85	2.9	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.8V	--	200	300	μA
VDD Operating Current	I_{DD_OP}	V_{DD} = 5V	--	3.5	5	mA
VDD Idle-Mode Current	I_{DD_IDLE}	V_{DD} = 5V	--	1.5	2	mA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDD Green-Mode Current	I_{DD_GREEN}	V_{DD} = 5V		--	750	1000	μA
VDD Threshold of Enable IO Pins Overvoltage Protection	$V_{VDD\_IOOVP\_EN}$			5.2	5.5	5.8	V
VDD Hysteresis of Enable/Disable IO Pins Overvoltage Protection	$V_{VDD\_IOOVP\_HYS}$			0.2	0.3	0.4	V
Maximum VDD Overvoltage Protection Threshold	$V_{VDD\_MAX\_OVP}$			23	24	25	V
Register-Programmable Overvoltage Protection Threshold	V_{VDD_OVP}	With respect to V_{REF_CV} (Disable/enable by register)	00	105	110	115	%
			01	109.3	115	120.8	
			10	114	120	126	
VDD Overvoltage Protection Deglitch Time	t_{VDD_OVP}	(Note 6)		25	30	35	μs
Register-Programmable VDD Undervoltage Protection Threshold	V_{VDD_UVP}	With respect to V_{REF_CV} (Disable/enable by register)	0	85	90	95	%
			1	80	85	90	
VDD Undervoltage Protection Deglitch Time	t_{VDD_UVP}	(Note 6)		25	30	35	μs
Register-Programmable VDD Discharge Current	I_{DD_DIS}	V_{DD} > 3V	00	42	60	78	mA
			01	63	90	117	
			10	84	120	156	
			11	126	180	234	
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} > 2.8V		10.26	10.8	11.34	MHz
Regulator Section							
V_{DD} Divider Resistor for Feedback Loop	R_{FB}	R_{FB} = R_{FB1} + R_{FB2} R_{FB1}: VDD to VFB R_{FB2}: VFB to GND (Note 6)		140	200	260	kΩ
V_{DD} Scaling Factor	K_{FB}	K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2}		9.9	10	10.1	--
Reference Voltage for Standby CV Regulator	$V_{REF\_CV\_STBY}$			0.485	0.5	0.515	V
Minimum Reference Voltage for CV Regulator	$V_{REF\_CV\_MIN}$	With 11-bit digital to analog converter		--	0.15	--	V
Maximum Reference Voltage for CV Regulator	$V_{REF\_CV\_MAX}$			2.156	2.2	2.244	V
Minimum Reference Voltage for CC Regulator	$V_{REF\_CC\_MIN}$	VDD > 3.3V With 11-bit digital to analog converter		--	0	--	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Maximum Reference Voltage for CC Regulator	$V_{REF\_CC\_MAX}$			1.862	1.9	1.938	
Maximum ADC Sense Voltage	V_{ADC_MAX}	With 11-bit analog to digital converter		2.178	2.2	2.222	V
OPTO Turn-On Sinking Current Capability	I_{OPTO_ON}	V_{DD} = 5V, V_{OPTO} = 3V, V_{REF_CV} = 0.15V (Note 6)		2	60	120	mA
OPTO Resistor Connected to VDD	R_{OPTO_VDD}			35.7	51	66.3	kΩ
OPTO Resistor Connected to GND	R_{OPTO_SINK}	V_{DD} = V_{OPTO} = 2.5V		42	60	78	kΩ
OPTO Sinking Current Source	I_{OPTO_SINK}			20	25	30	μA
OPTO Pull-Low Impedance	R_{OPTO_OL}	OPTO shorted to GND (Disable/enable by register)		--	--	200	Ω
Current Sense Section							
Current-Sense Voltage Gain	K_{CS}			30.4	32	33.6	V/V
Current-Sense Amplifier Output Offset Voltage	V_{CS_OFFSET}			0.36	0.4	0.44	V
Register-Programmable Exit Green Mode Threshold	V_{GREEN_EX}	(V_{CS+} - V_{CS-}) x K_{CS} + V_{CS_OFFSET}	0	0.41	0.45	0.49	V
			1	0.51	0.55	0.59	
RT Section							
RT Open Loop Voltage	V_{RT_OP}	V_{DD} = 5V, I_{RT_BIAS} = 95μA		3.6	4	4.4	V
Register-Programmable RT Internal Bias Current	I_{RT_BIAS}	V_{DD} > 3V	0	95	100	105	μA
			1	18	20	22	
RT Overvoltage Protection Threshold	V_{RT_OVP}	1. The blocking MOSFET can be turned off or left on based on the register setting 2. Send a flag to MCU 3. V_{DD} > $V_{VDD\_IOOVP\_EN}$ 4. Disable/enable by register		4.6	4.85	5.1	V
Register-Programmable RT Overvoltage Protection Deglitch Time	t_{RT_OVP}	(Note 6)	0	0.09	0.1	0.11	ms
			1	0.9	1	1.1	
GPIO1 (SDA), GPIO2 (SCL), and GPIO3 Section							
GPIO1 Open-Loop Voltage	V_{GP1_OP}	V_{DD} = 5V, I_{GP1_BIAS} = 900μA		3.2	3.6	4	V
GPIO2/GPIO3 Open-Loop Voltage	V_{GP_OP}	V_{DD} = 5V, I_{GP_BIAS} = 95μA		3.6	4	4.4	V
Register-Programmable GPIO1 Internal Bias Current	I_{GP1_BIAS}	V_{DD} > 3V		900	1300	1700	μA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable GPIO2 Internal Bias Current	I_{GP2_BIAS}	V_{DD} > 3V	0	95	100	105	μA
			1	18	20	22	
Register-Programmable GPIO3 Internal Bias Current	I_{GP3_BIAS}	V_{DD} > 3V		90	100	110	μA
GPIO1/GPIO2/GPIO3 Overvoltage Protection Threshold	V_{GP_OVP}	1. The blocking MOSFET can be turned off or left on based on the register setting 2. Send a flag to MCU 3. V_{DD} > $V_{VDD\_IOOVP\_EN}$ 4. Disable/enable by register		4.6	4.85	5.1	V
GPIO1/GPIO2/GPIO3 Overvoltage Protection Deglitch Time	t_{GP_OVP}	(Note 6)	0	0.09	0.1	0.11	ms
			1	0.9	1	1.1	
I^2C High-Level Input Threshold Voltage	V_{IH_I2C}			1.3	--	--	V
I^2C Low-Level Input Threshold Voltage	V_{IL_I2C}			--	--	0.4	V
D+ and D- Section							
Register-Programmable DP/DM Pull-Low Resistance	R_{DPDM_L}			16	20	24	kΩ
Register-Programmable DP/DM Leakage Resistance	R_{DPDM_LKG}			300	900	1500	kΩ
Register-Programmable DP/DM Output High Voltage	V_{DPDM_OH}	V_{DD} = 5V, R_L = 15kΩ		2.97	3.3	3.63	V
DP/DM Output Low Voltage	V_{DPDM_OL}	R_L = 15kΩ		--	--	0.2	V
Register-Programmable DP/DM Input High Threshold Voltage	V_{DPDM_IH}		00	1.1	1.2	1.3	V
			01	1.2	1.3	1.4	
			10	2	2.1	2.2	
Register-Programmable DP/DM Input Low Threshold Voltage	V_{DPDM_IL}		00	0.9	1	1.1	V
			01	1.0	1.1	1.2	
			10	1.8	1.9	2.0	
Register-Programmable DP/DM Input Deglitch Time	t_{DPDM_IN}	(Note 6)	00	0.95	1	1.05	μs
			01	142.5	150	157.5	
			10	475	500	525	
			11	950	1000	1050	
DP/DM Short Switch On-Resistance	R_{DPDM_ON}			--	--	40	Ω
DP Comparison Threshold for Cable Detachment	V_{DP_CD}	Disable/enable cable detection by register		0.2	0.3	0.4	V

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DP Comparison Threshold for Cable Attachment	V_{DP_CA}			0.3	0.4	0.5	V
Register-Programmable DP Cable Detection Deglitch Time	t_{DP_CD}	(Note 6)	00	0.25	0.5	0.75	ms
			01	0.75	1	1.25	
			10	1.75	2	2.25	
			11	3.75	4	4.25	
DP/DM Overvoltage Protection Threshold	V_{DPDM_OVP}	1. The blocking MOSFET can be turned off or left on based on the register setting 2. Send a flag to MCU 3. $V_{DD} > V_{VDD\_IOOVP\_EN}$ 4. Disable/enable by register		4.6	4.85	5.1	V
Register-Programmable DP/DM Overvoltage Protection Deglitch Time	t_{DPDM_OVP}	(Note 6)	0	0.09	0.1	0.11	ms
			1	0.9	1	1.1	
CC1 and CC2 Section							
CC1/CC2 Output High Voltage	V_{CC_OH}			1.05	1.125	1.2	V
CC1/CC2 Output Low Voltage	V_{CC_OL}			0	0.0375	0.075	V
CC1/CC2 Input High Threshold Voltage	V_{CC_IH}			0.7	0.8	0.9	V
CC1/CC2 Input Low Threshold Voltage	V_{CC_IL}			0.5	0.6	0.7	V
Open Loop Voltage for CC1/CC2 Sourcing Current	V_{CC_OP}	$V_{DD} > 5V$		2.9	3.25	3.6	V
Register-Programmable CC1/CC2 Sourcing Current	I_{CC_SRC}	$V_{DD} > 3V$	01	72	80	88	µA
			10	169	180	191	
			11	304	330	356	
CC1/CC2 Sourcing Current for Rust Protection	I_{CC_RUST}	Disable/Enable by register		0.5	1	1.5	µA
CC1/CC2 Comparison Threshold for Cable Detection	V_{CC_CD}	1. $V_{DD} > 3V$ 2. Send a flag to MCU 3. Disable/Enable by register		2.5	2.6	2.7	V
CC1/CC2 Overvoltage Protection Threshold	V_{CC_OVP}	1. The blocking MOSFET can be turned off or left on based on the register setting 2. Send a flag to MCU 3. $V_{DD} > V_{VDD\_IOOVP\_EN}$ 4. Disable/enable by register		4.6	4.85	5.1	V
Register-Programmable CC1/CC2 Overvoltage Protection Deglitch Time	t_{CC_OVP}	(Note 6)	0	0.09	0.1	0.11	ms
			1	0.9	1	1.1	

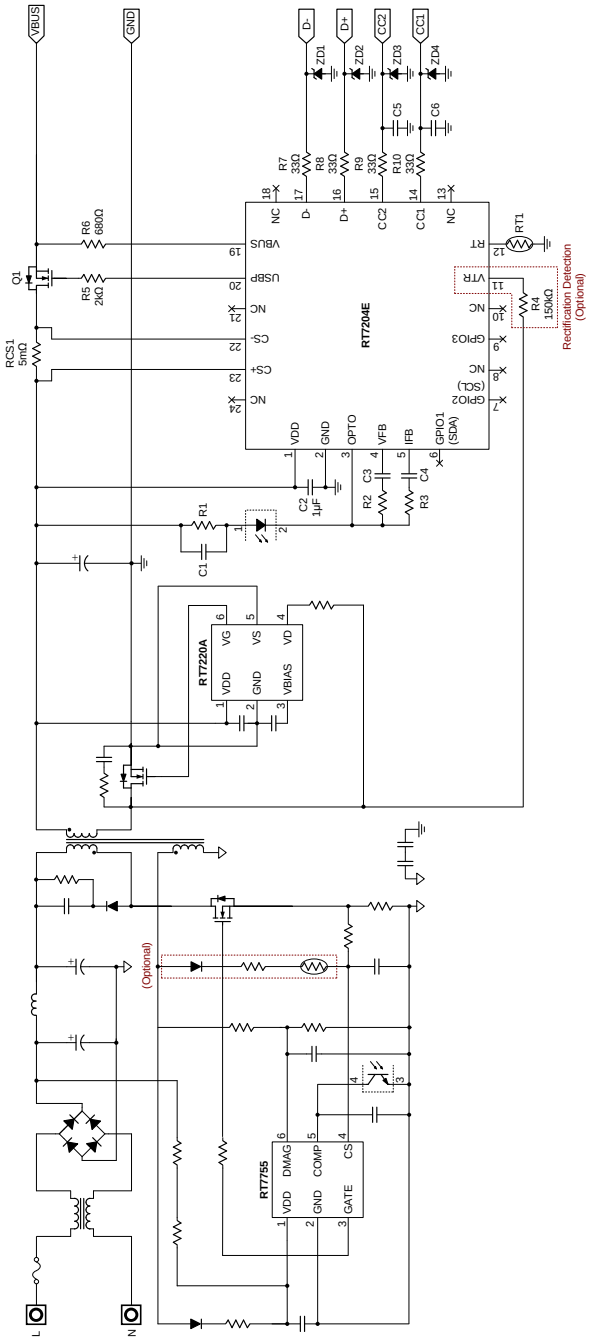
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable V_{CONN} Voltage	V_{VCONN}	V_{DD} = 5V, I_{VCONN} = 0mA		4	4.2	4.4	V
		V_{DD} = 5V, I_{VCONN} = 30mA		3.3	--	--	
V_{CONN} Short-Circuit Current	I_{VCONN_SC}	(Note 6)		45	70	95	mA
VBUS Section							
Maximum VBUS Discharge Current	I_{VBUS_DIS}	V_{DD} = 3V to 21V		2	--	30	mA
VBUS Pull-Low Impedance	R_{VBUS_L}	I_{VBUS} = 2mA		0.7	1	1.3	kΩ
VBUS Divider Resistor for ADC Sensing	R_{VBUS_ADC}	R_{VBUS_ADC} = R_{VBUS1} + R_{VBUS2}		294	420	546	kΩ
VBUS Scaling Factor for ADC Sensing	K_{VBUS_ADC}	K_{VBUS_ADC} = (R_{VBUS1} + R_{VBUS2}) / R_{VBUS2} (Note 6)		9.7	10	10.3	--
Register-Programmable VBUS Drop Threshold for Output Short Protection	V_{VBUS_DROP}	V_{DD} > 3.3V If V_{DD} - V_{BUS} > V_{VBUS_DROP}, 1. The blocking MOSFET can be turned off or left on based on the register setting 2. Send a flag to MCU 3. Disable/enable by register (Note 6)	0	0.2	0.3	0.4	V
			1	0.3	0.4	0.5	
Register-Programmable VBUS Drop Deglitch Time for Output Short Protection	t_{VBUS_DROP}	V_{DD} > 5V (Note 6)	0	16	20	24	µs
			1	24	30	36	
USBP Section							
USBP Output High Voltage	V_{USBP_OH}			VDD + 7	VDD + 8.5	VDD + 10	V
USBP Undervoltage Protection Threshold	V_{USBP_UVP}	1. Disable/Enable by register 2. Send a flag to MCU 3. The blocking MOSFET can be turned off or left on based on the register setting 4. Disable/enable by register		VDD + 4	VDD + 4.5	VDD + 5	V
USBP Undervoltage Deglitch Time	t_{USBP_UVP}	(Note 6)		30	50	70	µs
Register-Programmable Pull-Low Resistance when USBP Turn-Off	$R_{USBPOFF\_OL}$	1. For V_{DD} > V_{VDD_ON} 2. If USBP is turned Off		14	20	26	kΩ

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable USBP Soft-Start Time	t_{USBP_SS}	Default is disabled (Note 6)	000	0.9	1	1.1	ms
			001	1.8	2	2.2	
			010	3.6	4	4.4	
			011	7.2	8	8.8	
			100	14.4	16	17.6	
			101	28.8	32	35.2	
			110	57.6	64	70.4	
			111	115.2	128	140.8	
VTR Section							
VTR Divider Resistance for Rectification Detection	R_{VTR_L}	1. R_{VTR_H} / R_{VTR_L} = 29, R_{VTR_H} is the divider resistor from SR MOSFET drain to the VTR pin 2. Disable/enable by register		4.91	5.17	5.43	kΩ
VTR Falling Edge Threshold for Rectification Detection	V_{VTR_EDGE}			25	60	95	mV
Register-Programmable VTR Low Blanking Time	$t_{VTR\_L\_BLK}$	$V_{VTR} < V_{VTR\_EDGE}$ (Note 6)	000	0.4	0.5	0.6	µs
			001	0.6	0.7	0.8	
			010	0.8	0.9	1	
			011	1	1.1	1.2	
			100	1.6	1.7	1.8	
			101	1.8	1.9	2	
			110	2	2.1	2.2	
			111	2.2	2.3	2.4	
VTR Overvoltage Protection Threshold	V_{VTR_OVP}	1. The blocking MOSFET can be turned off or left on based on the register setting 2. Send a flag to MCU 3. $V_{DD} > V_{VDD\_IOOVP\_EN}$ 4. Disable/enable by register		4.6	4.85	5.1	V
Register-Programmable VTR Overvoltage Protection Deglitch Time	t_{VTR_OVP}	(Note 6)	0	0.09	0.1	0.11	ms
			1	0.9	1	1.1	
Thermal Sensor Section							
Thermal Sensor Error		25°C to 105°C (Note 6)		–7	--	7	°C

Note 6. Guaranteed by design.

13 Typical Application Circuit

(Note 7)



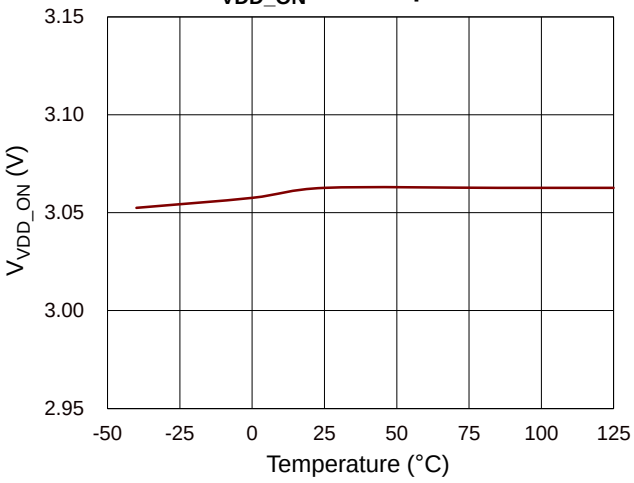
Note 7.

1. The selection of resistors R1, R2, R3, and capacitors C1, C3, and C4 should be based on the feedback compensation design requirements of the closed-loop power stage.
2. The R4 is an optional component for V_{IN} detection. If used, it is recommended to select a resistor with a tolerance of ±1%.
3. The value of resistor R5 is determined by the desired turn-on and turn-off speed for power path.

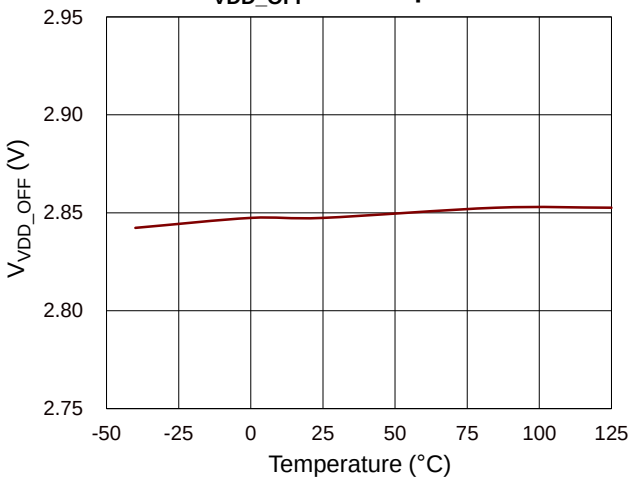
4. It is suggested to use 24V zener diodes for ZD1, ZD2, ZD3, and ZD4, specifically the BZX585-B24 model.
5. The values for capacitors C5 and C6 should be chosen in accordance with the USB PD specification: 200pF ≤ cReceiver ≤ 600pF.

14 Typical Operating Characteristics

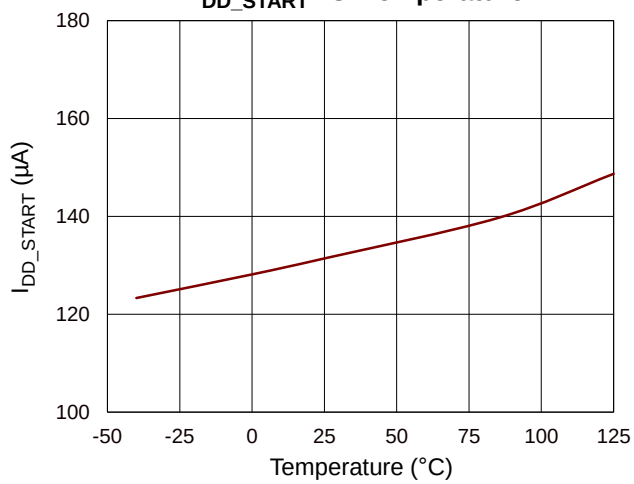
V_{VDD_ON} vs. Temperature



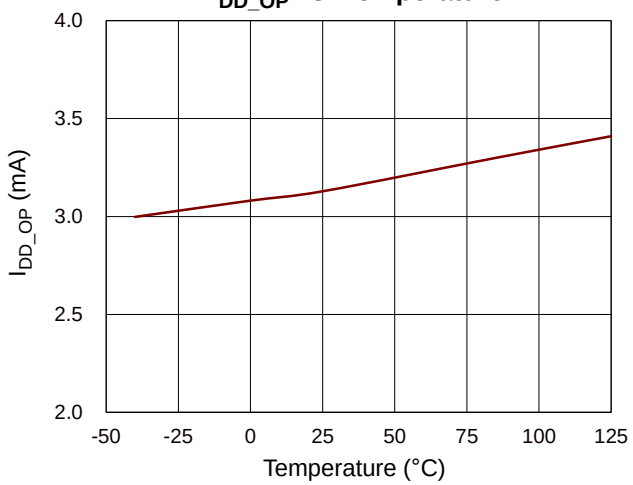
V_{VDD_OFF} vs. Temperature



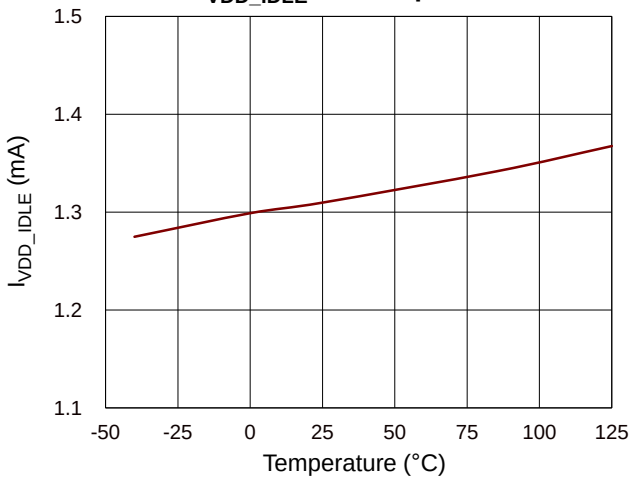
I_{DD_START} vs. Temperature



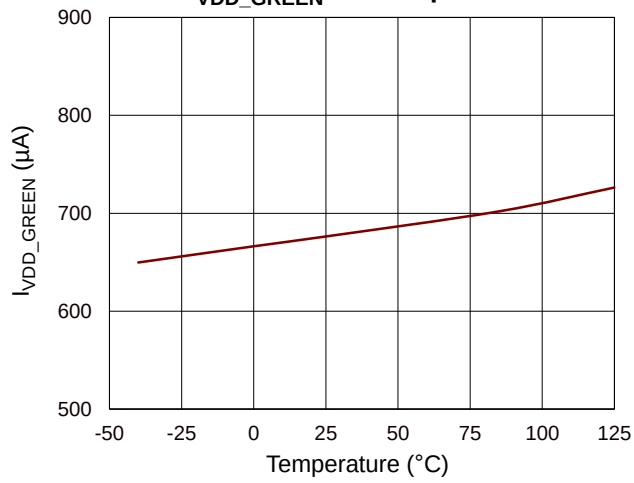
I_{DD_OP} vs. Temperature

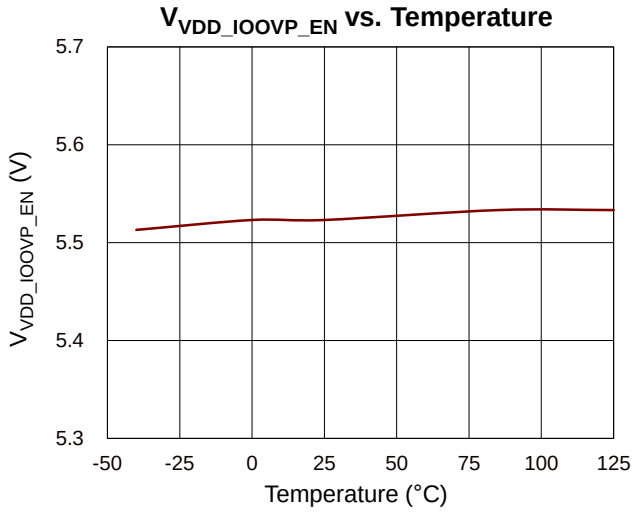


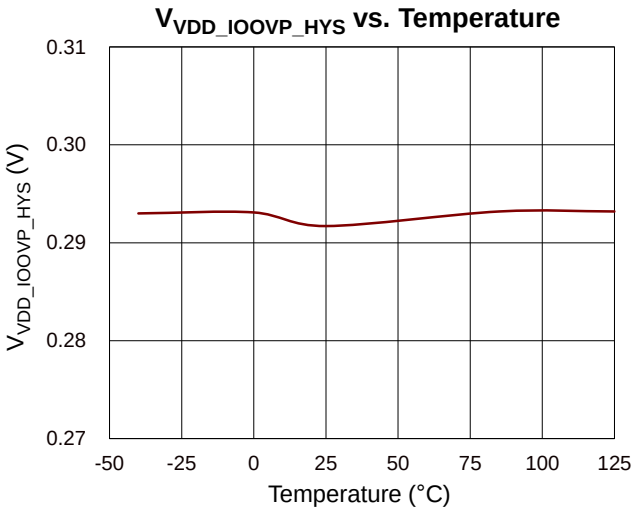
I_{VDD_IDLE} vs. Temperature

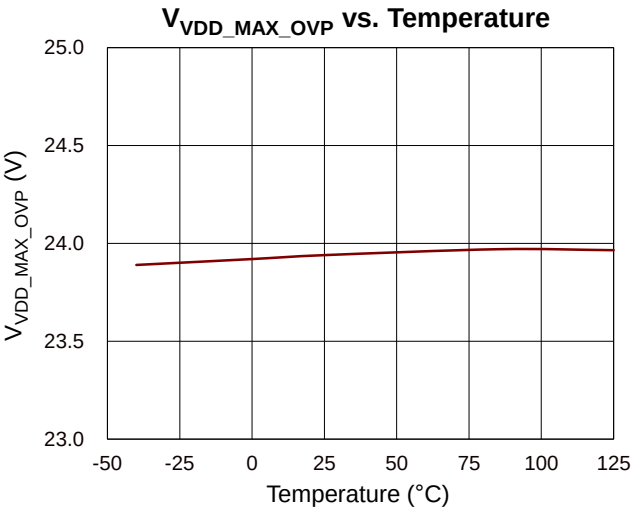


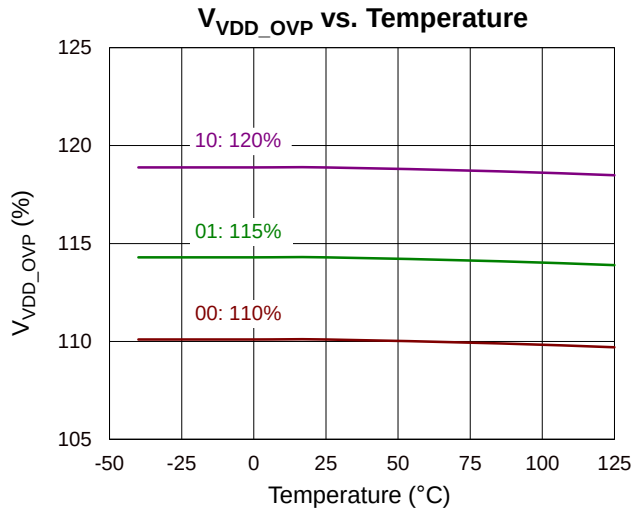
I_{VDD_GREEN} vs. Temperature

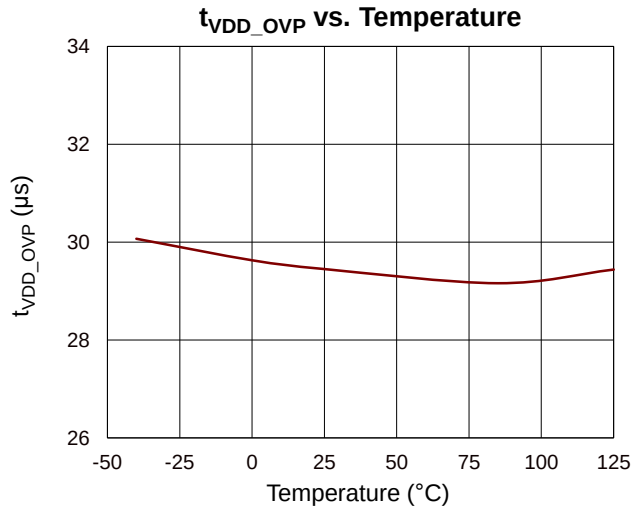


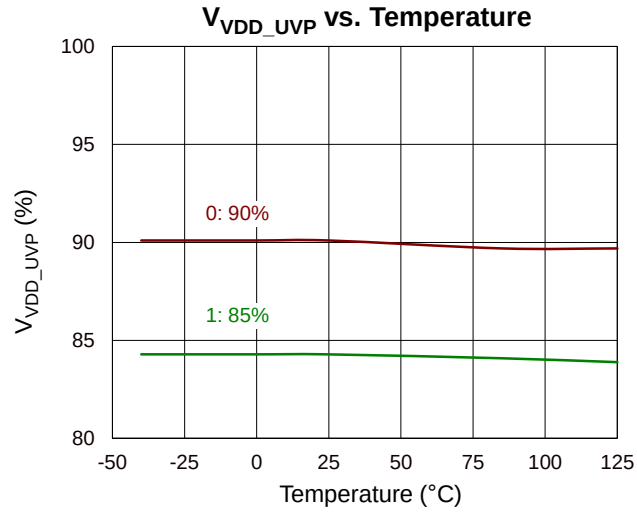


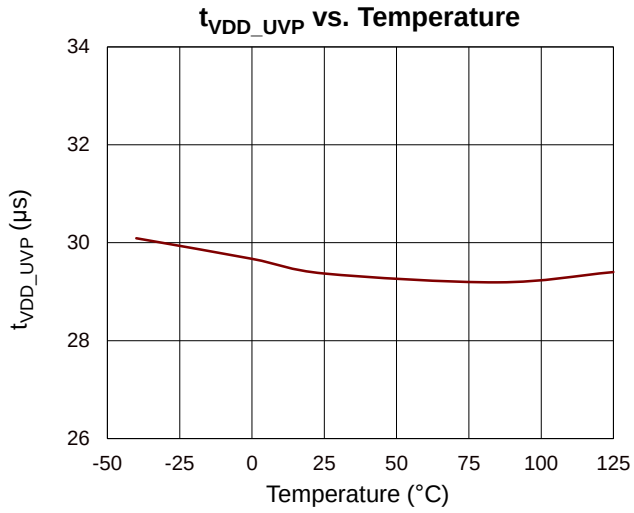


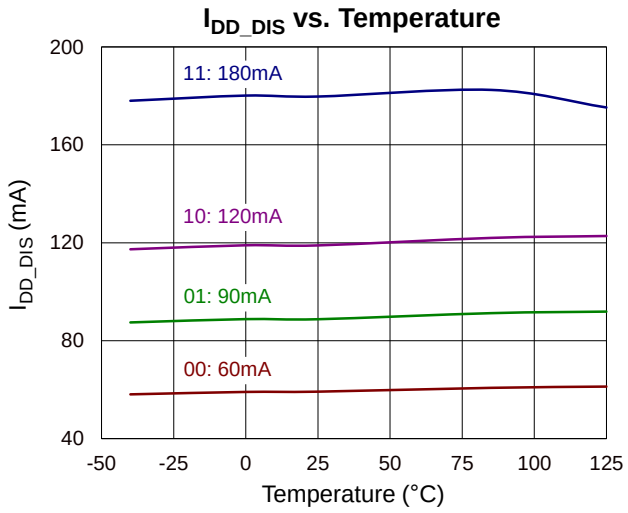


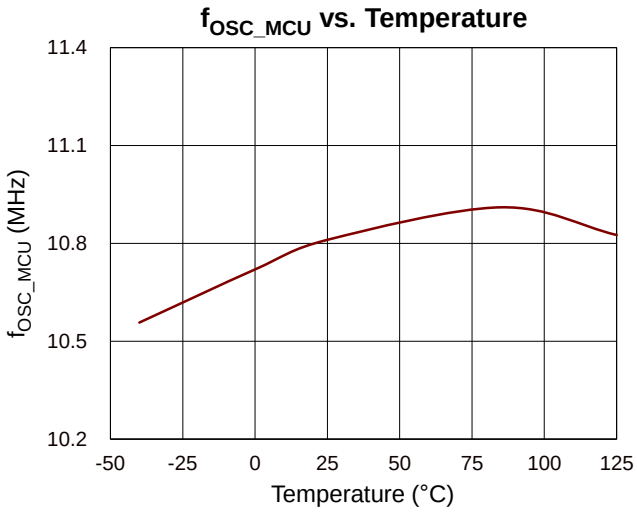


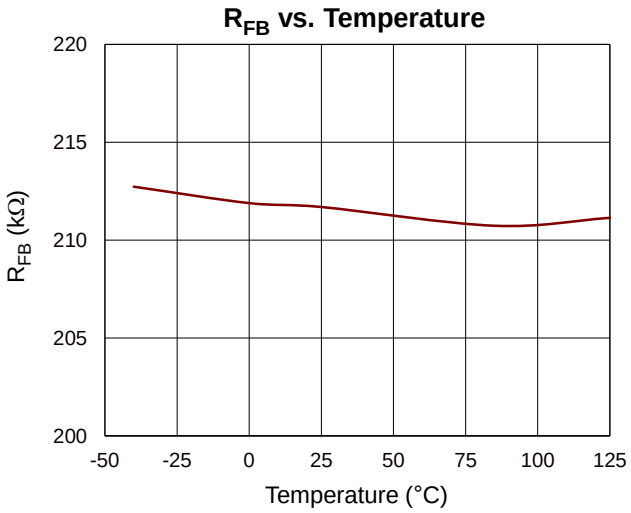


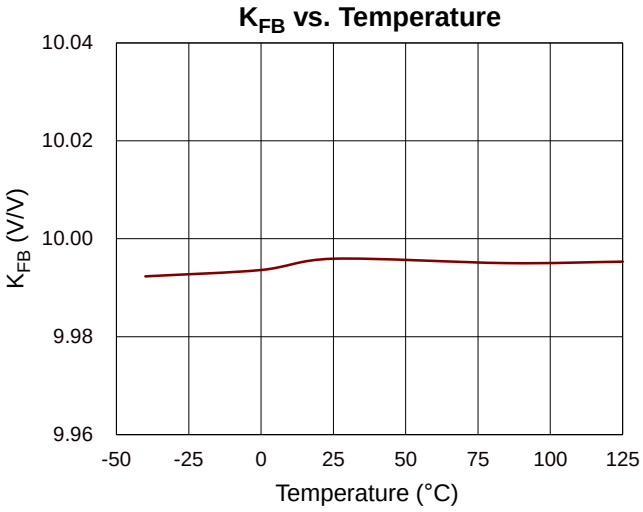


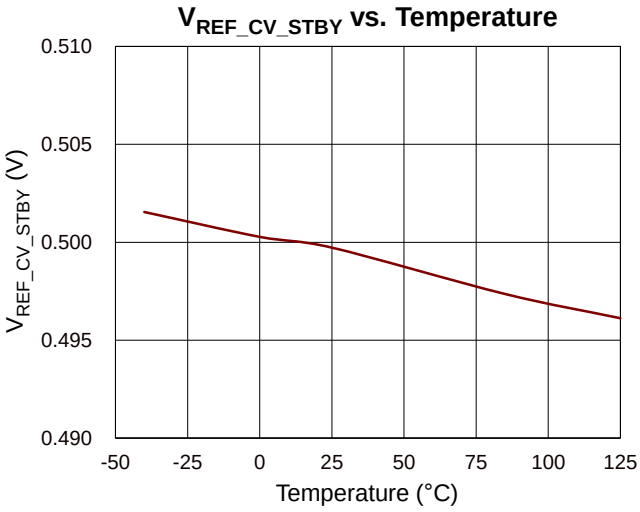


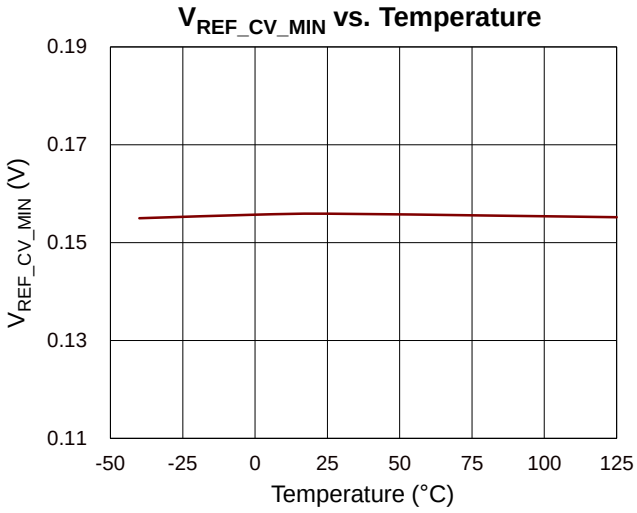


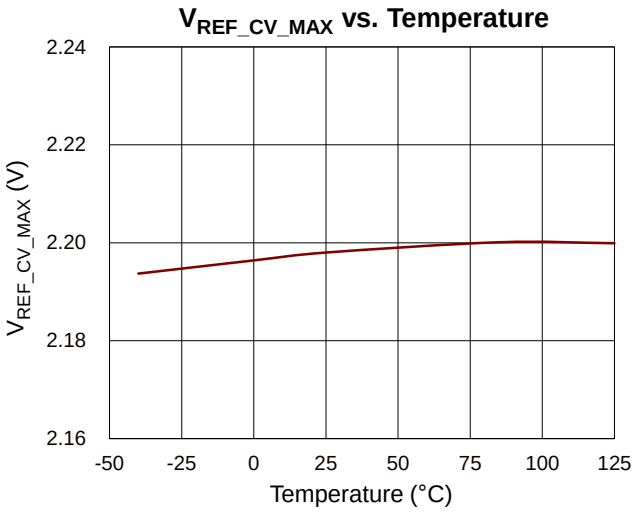


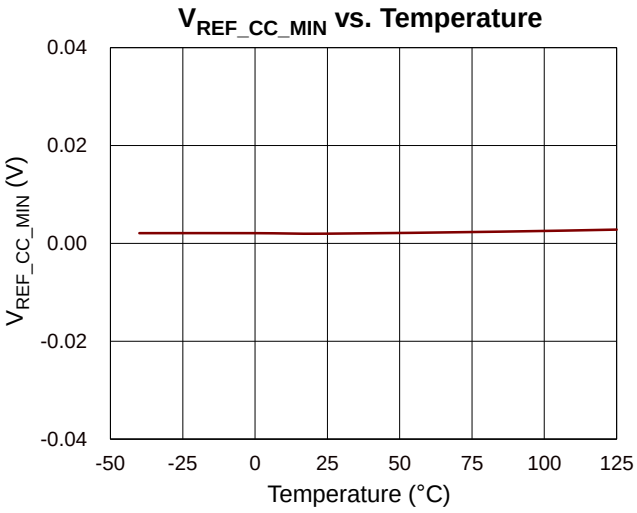


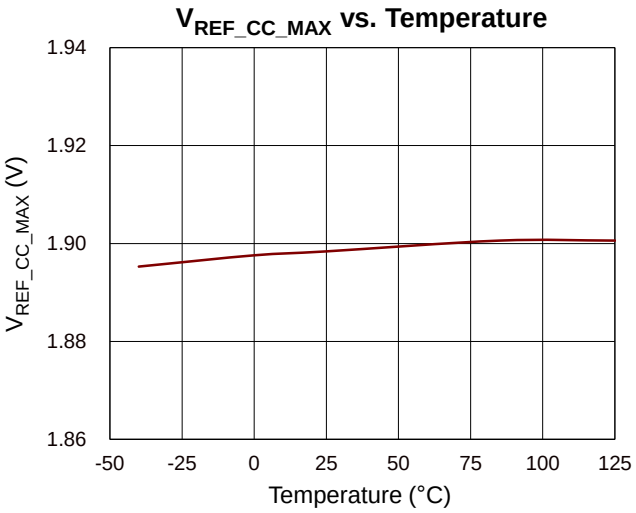


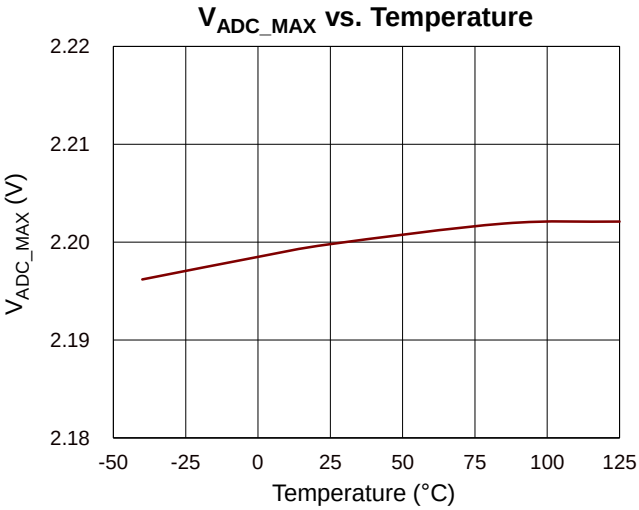


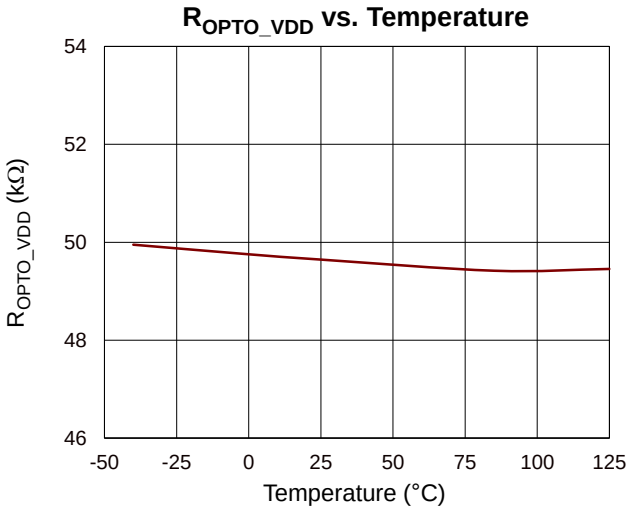


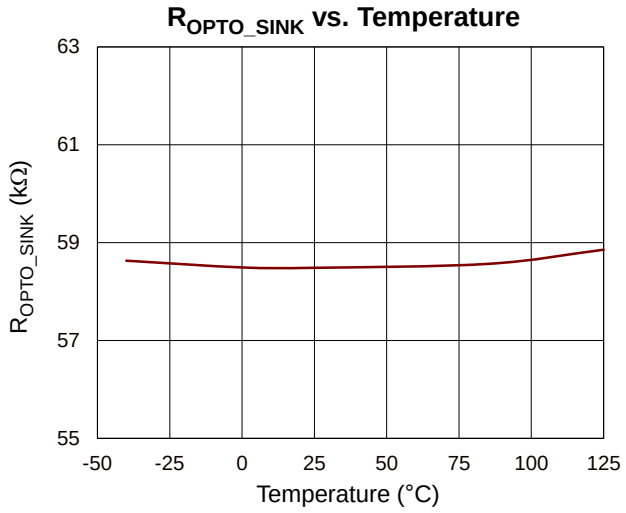


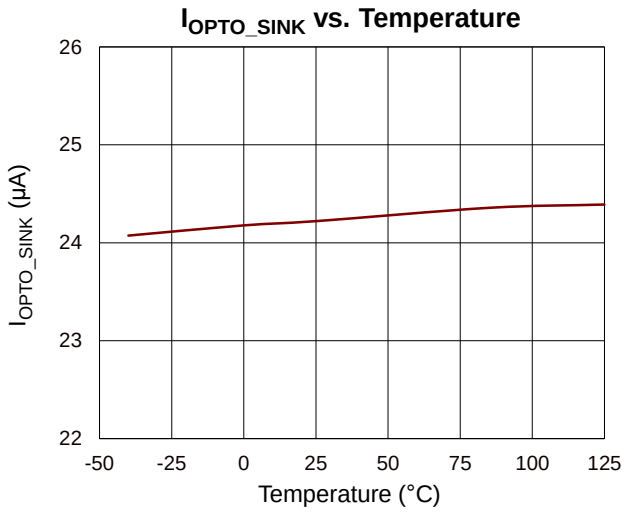


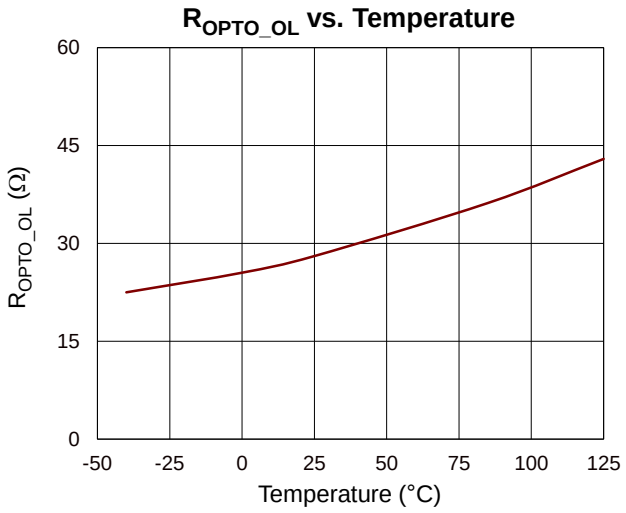


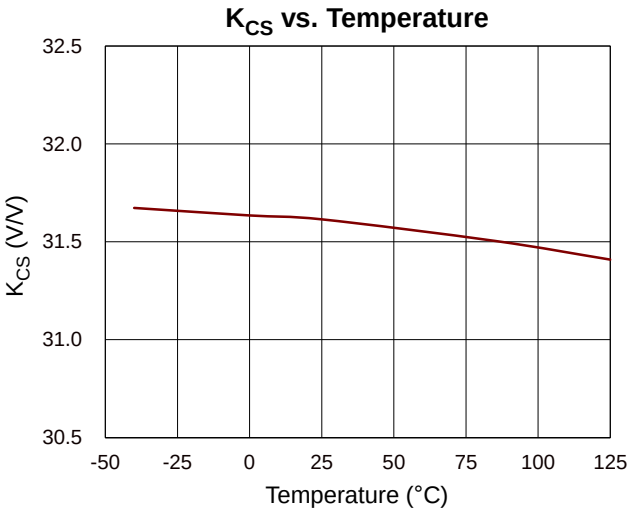


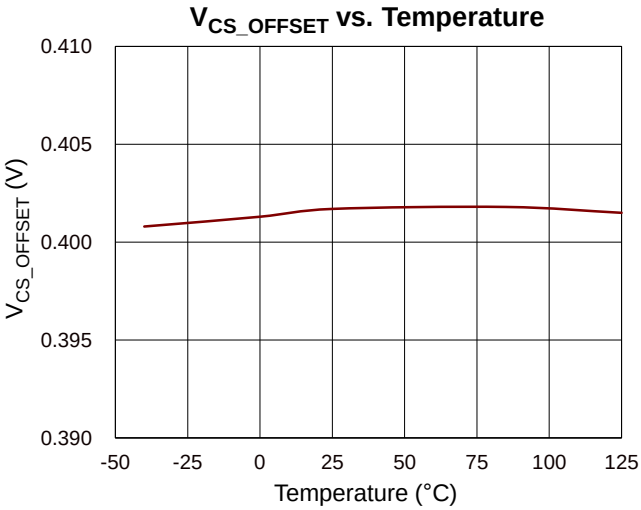


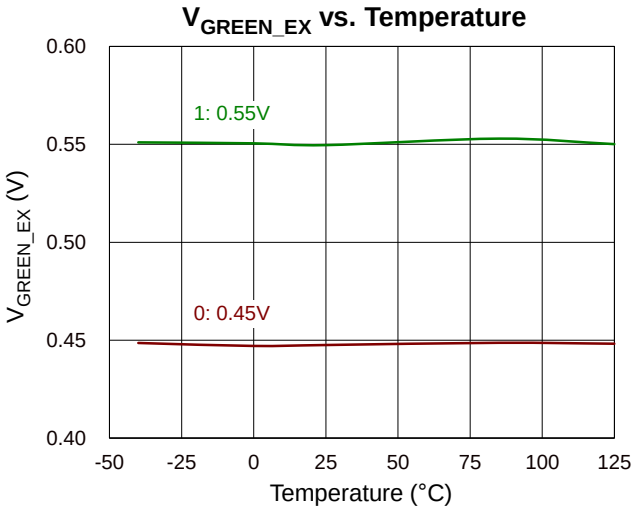


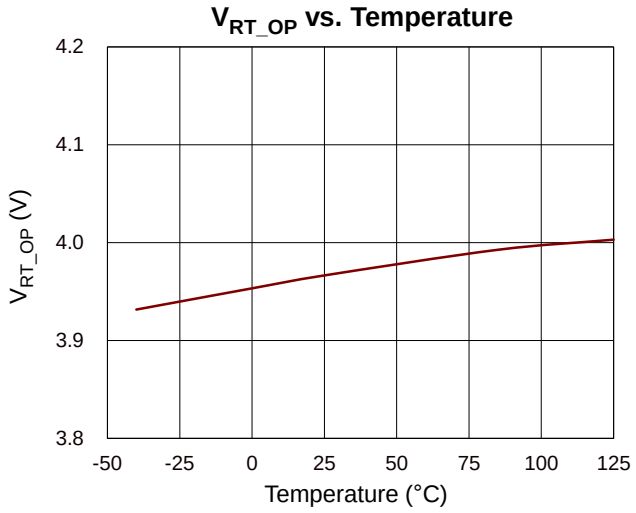


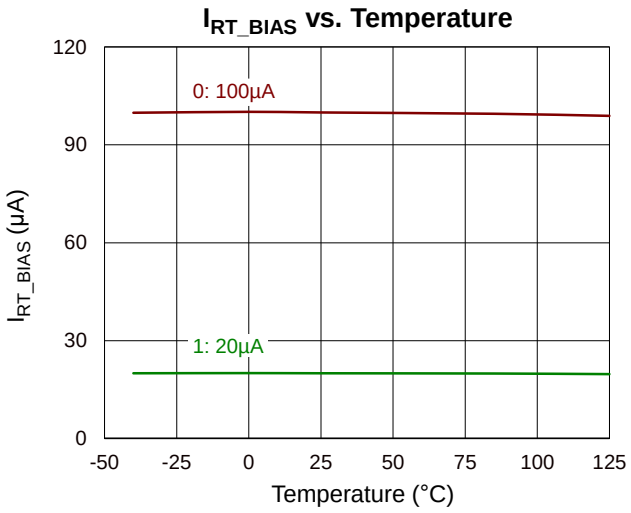


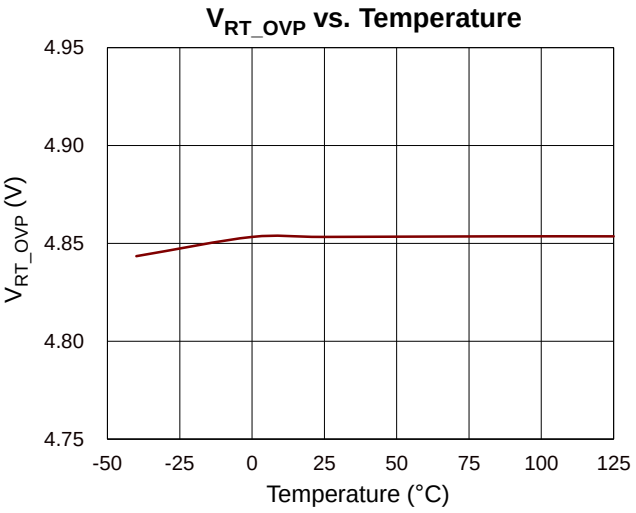


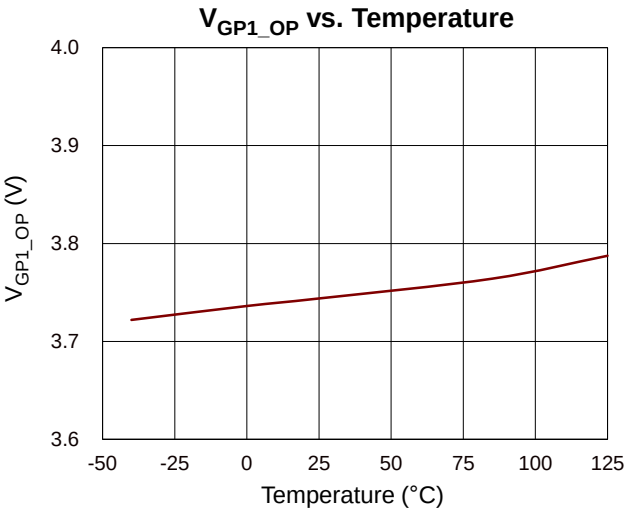


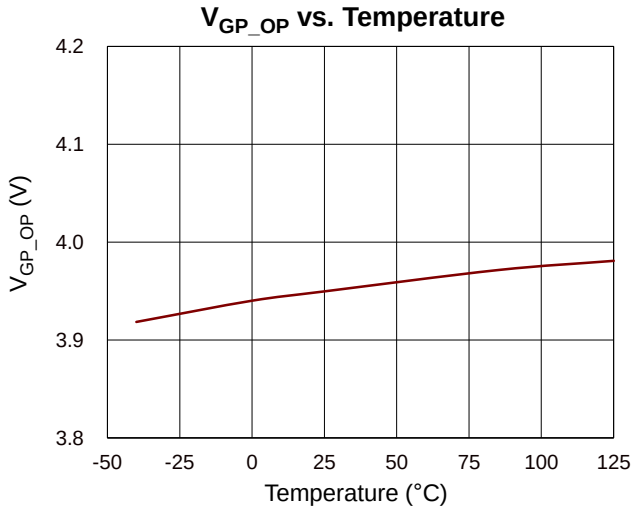


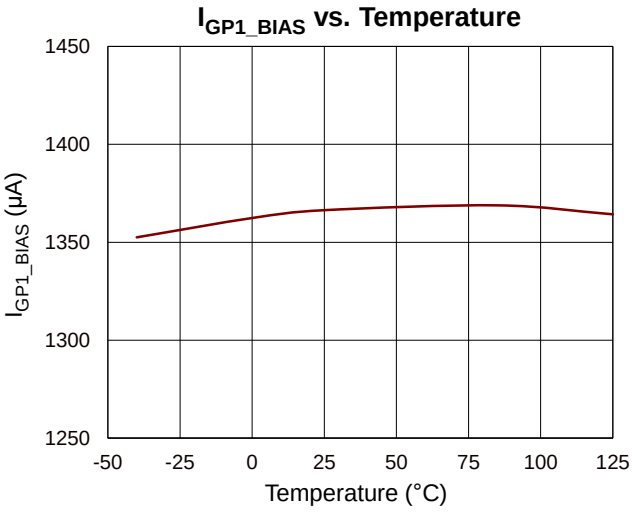


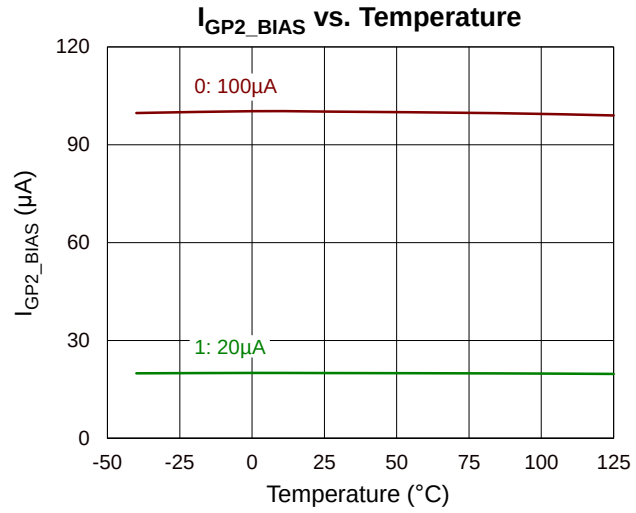


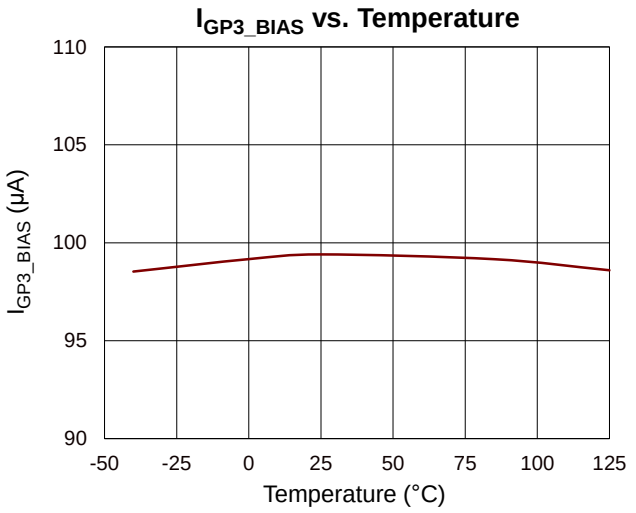


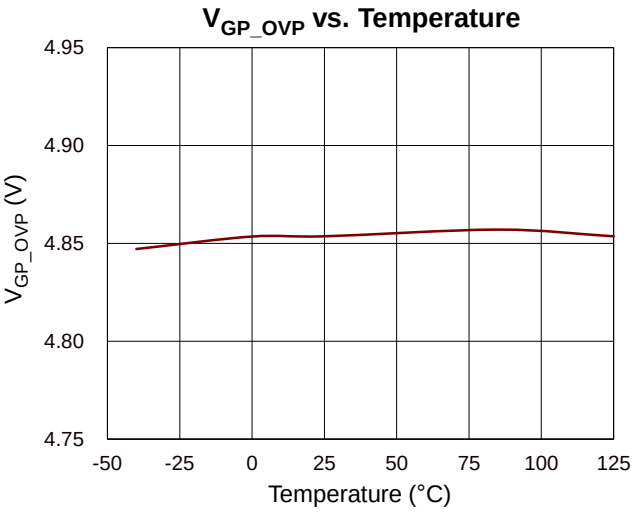


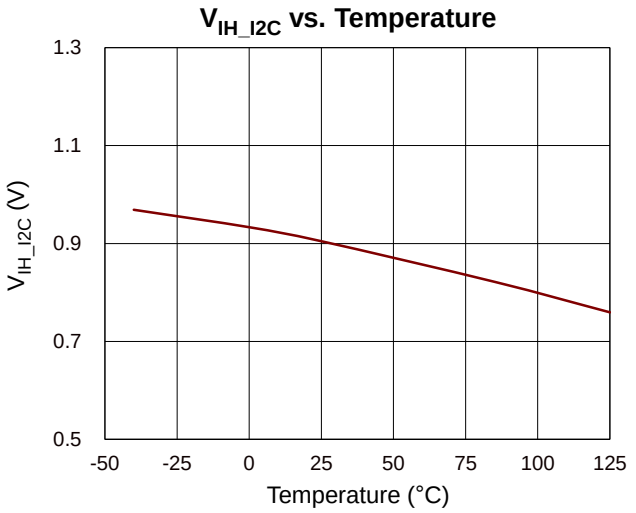


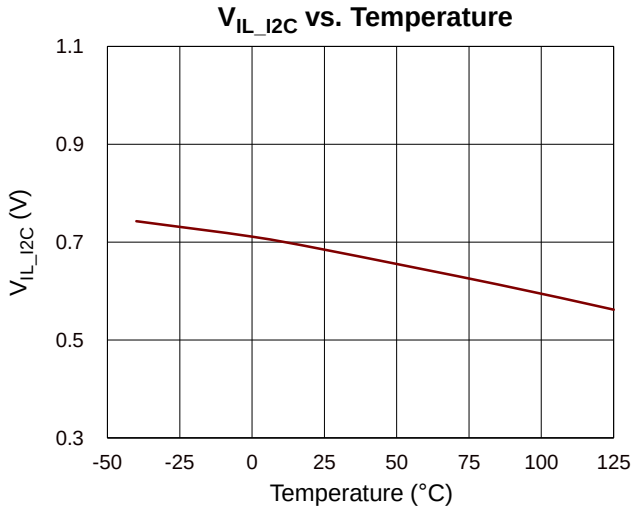


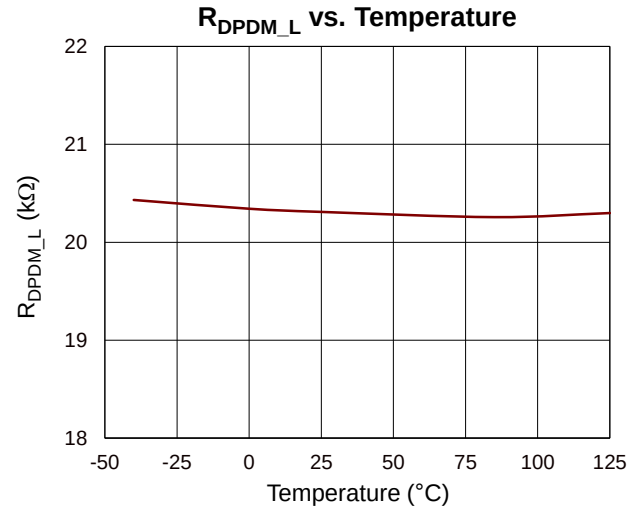


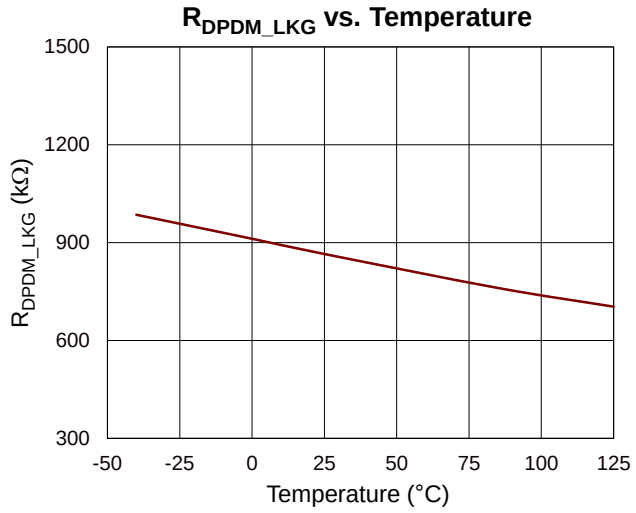


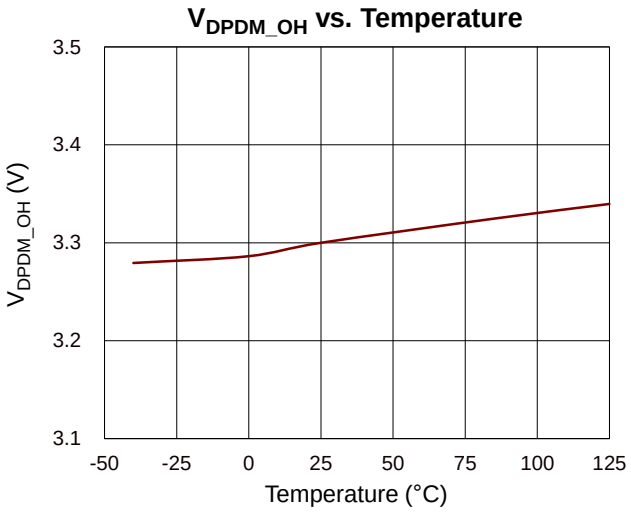


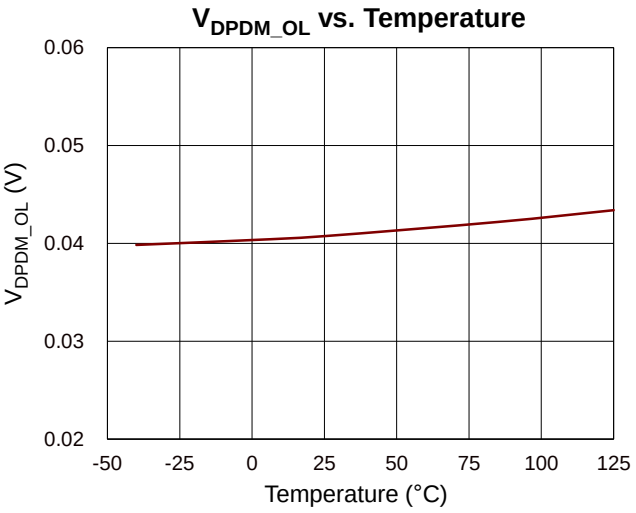


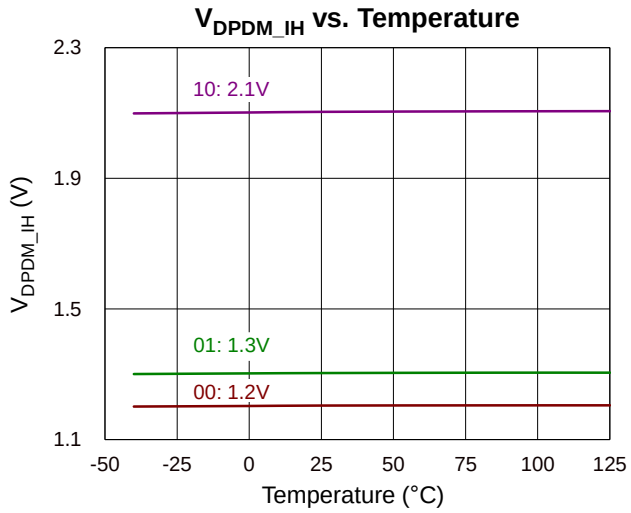


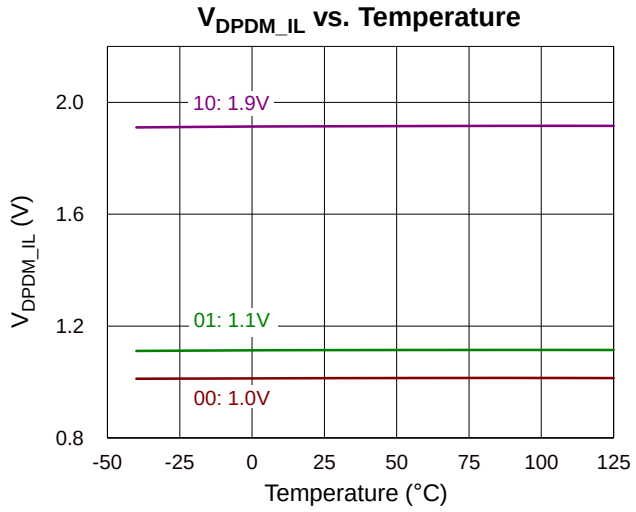


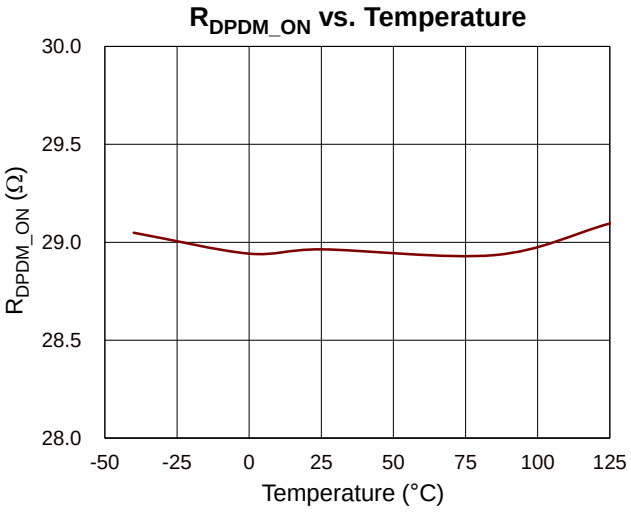


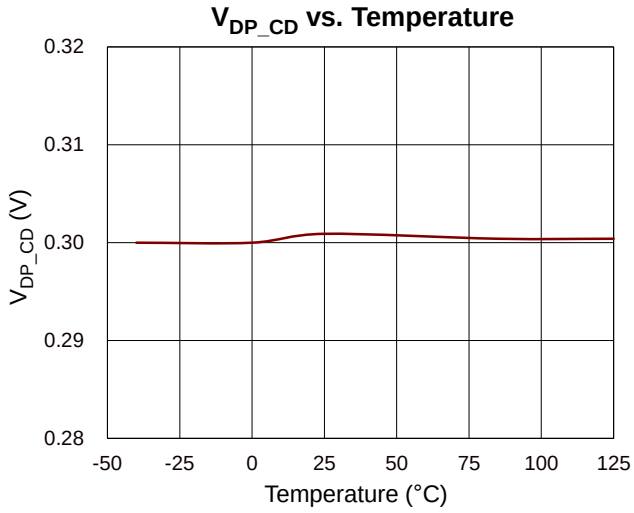


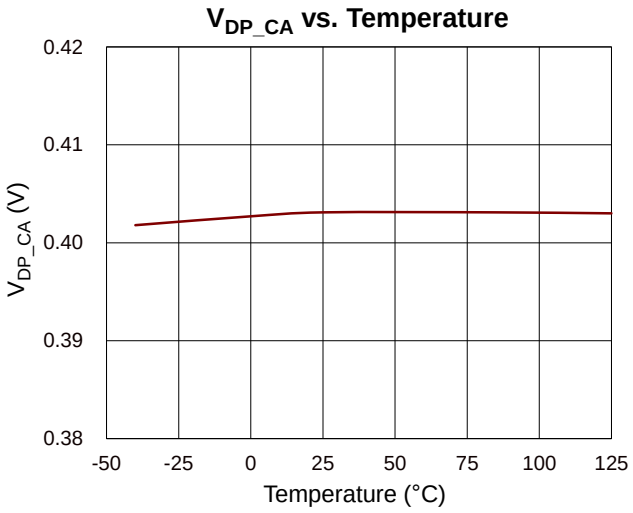


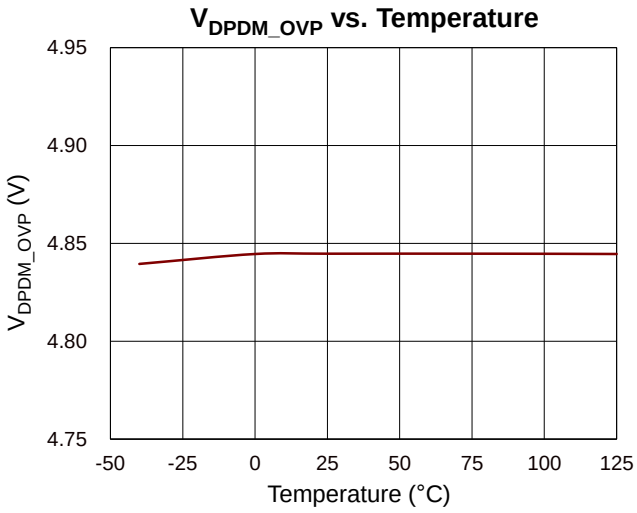


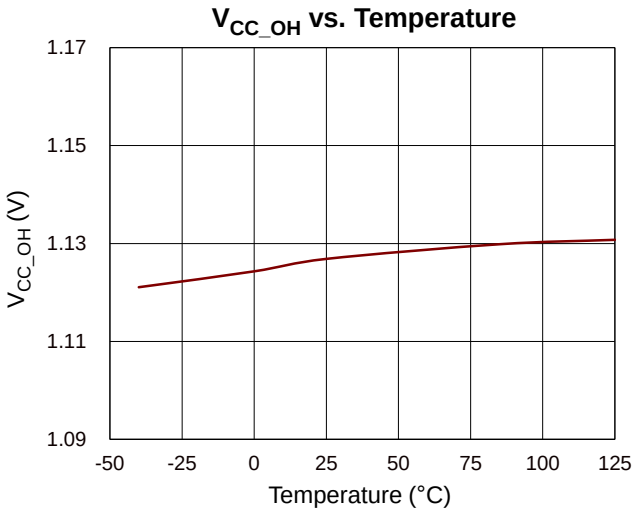


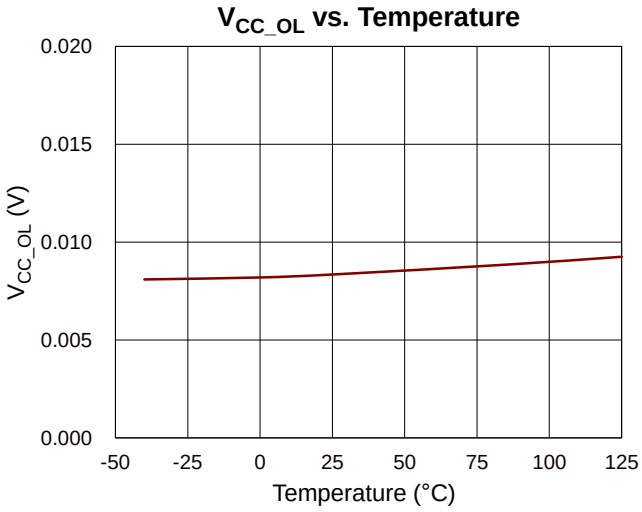


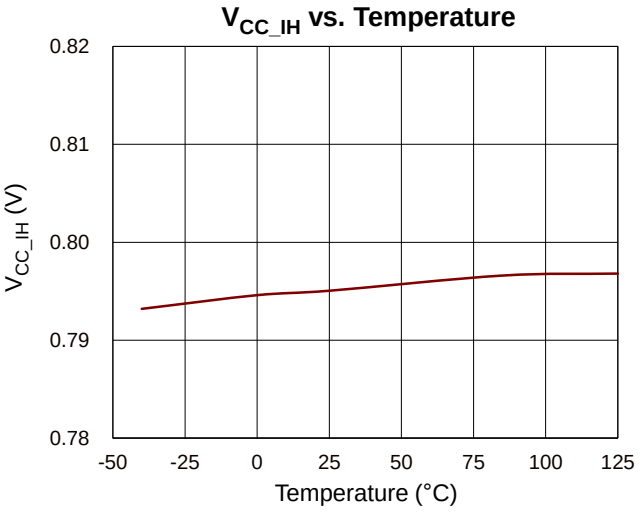


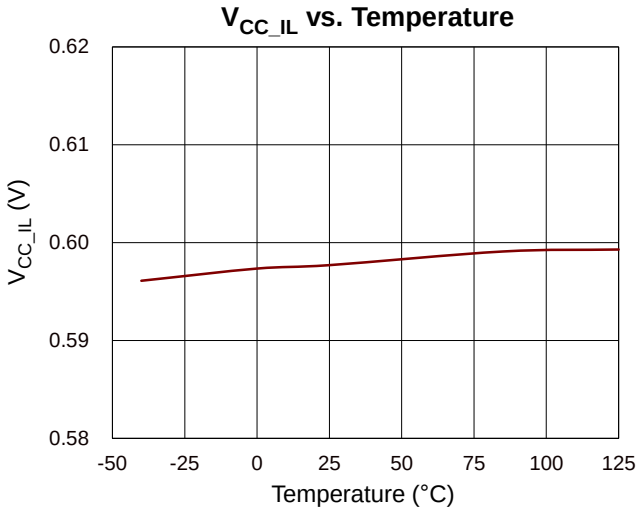


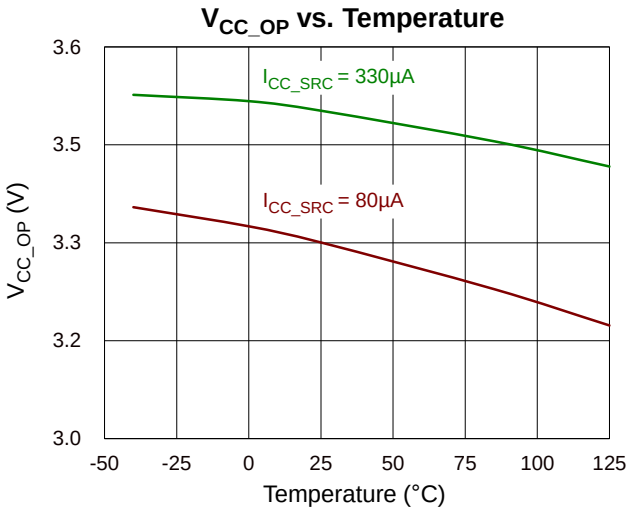


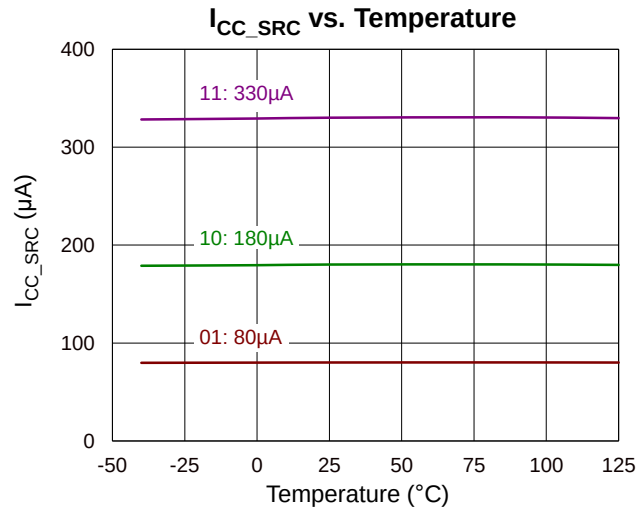


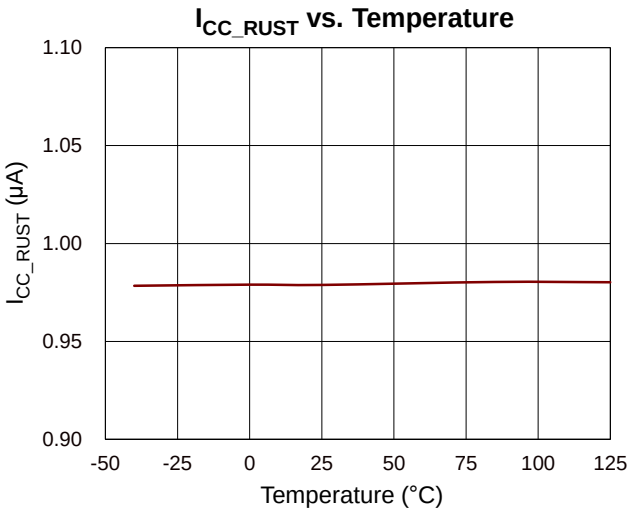


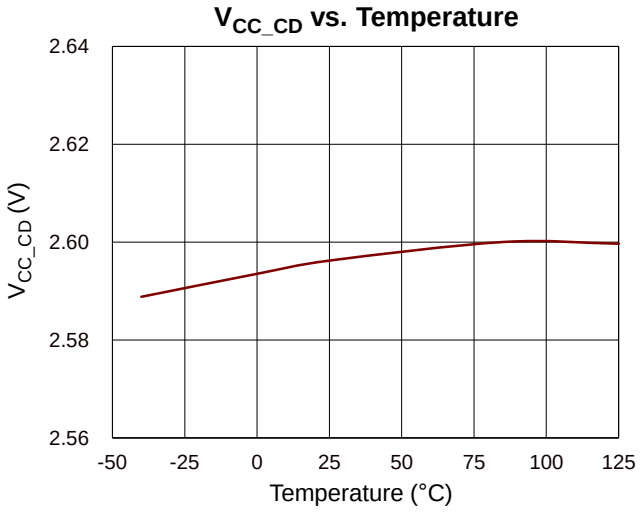


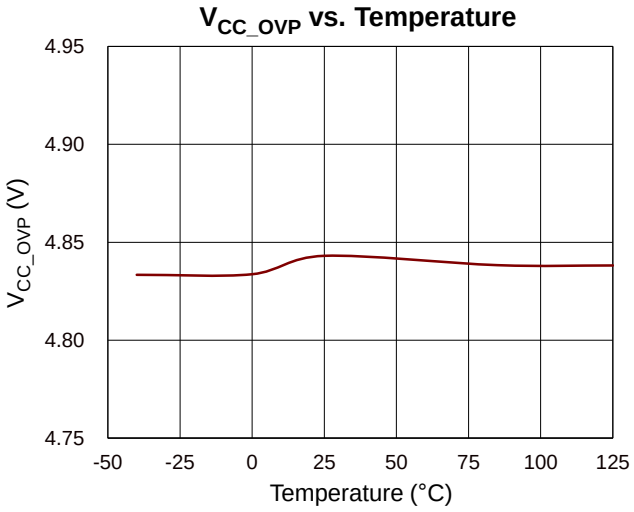


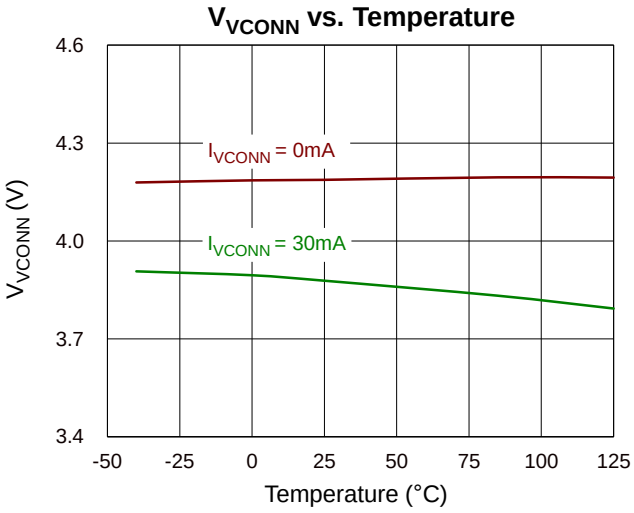


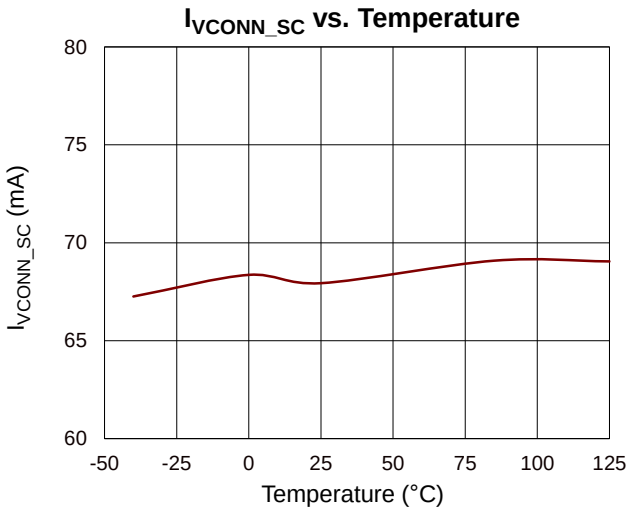


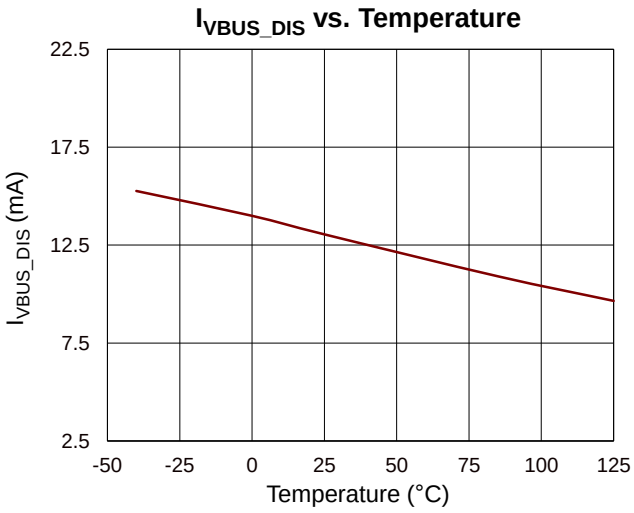


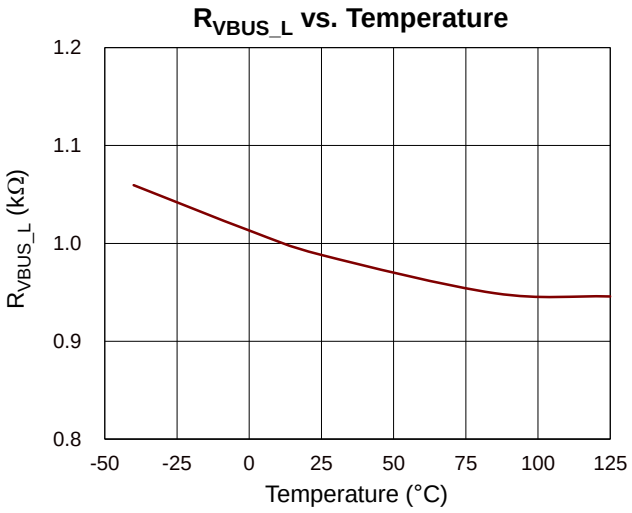


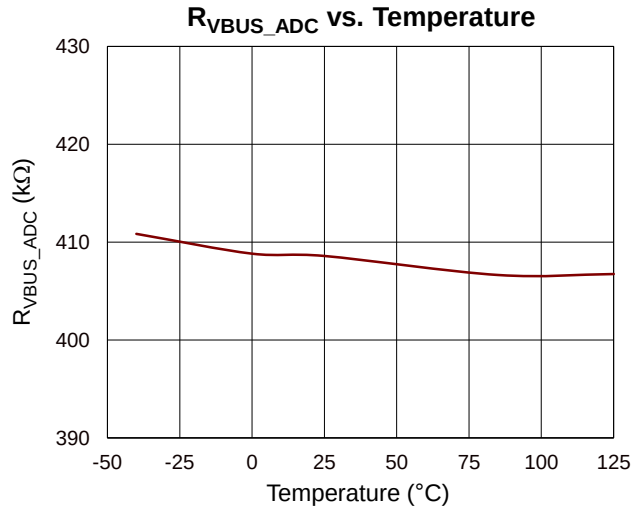


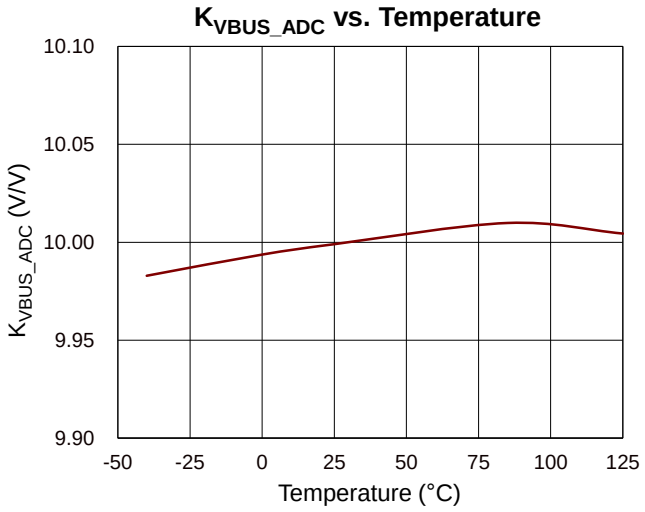


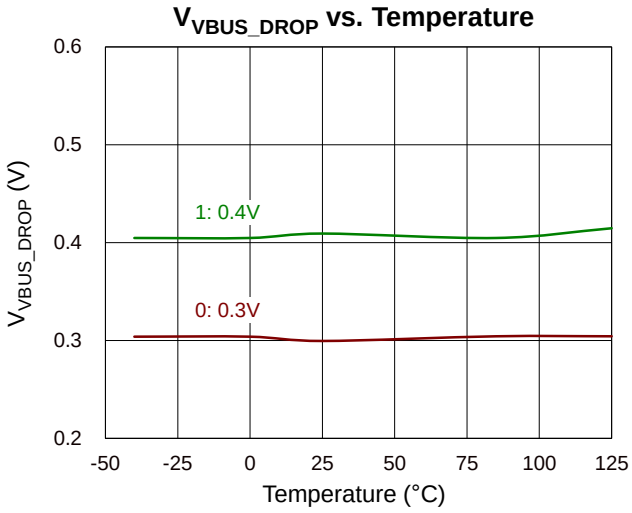


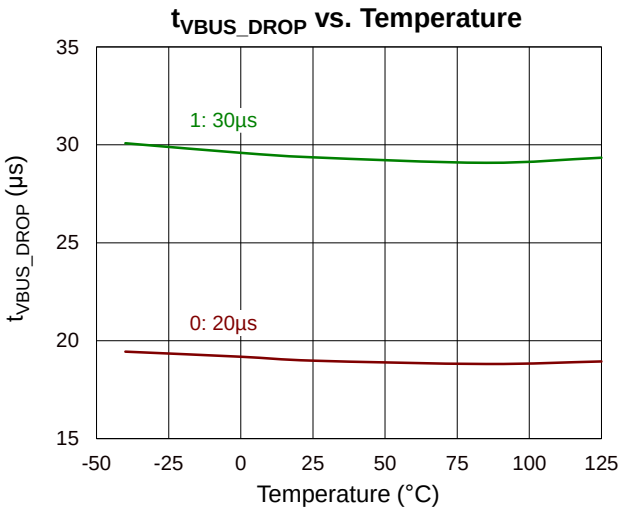


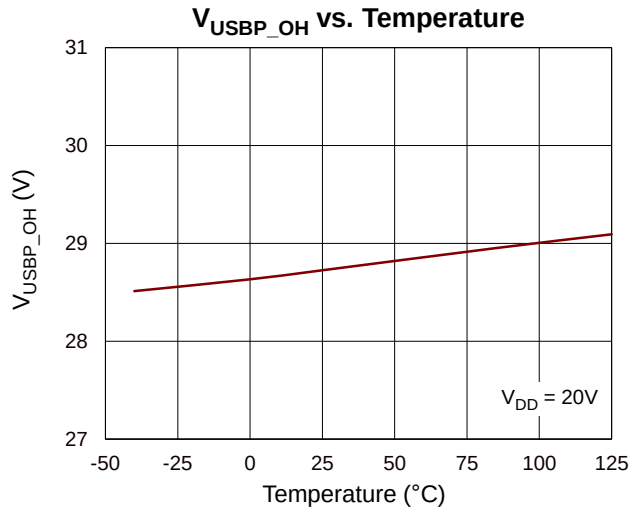


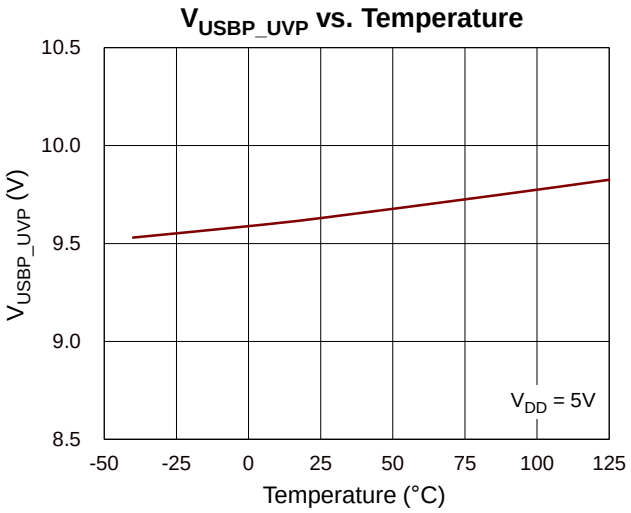


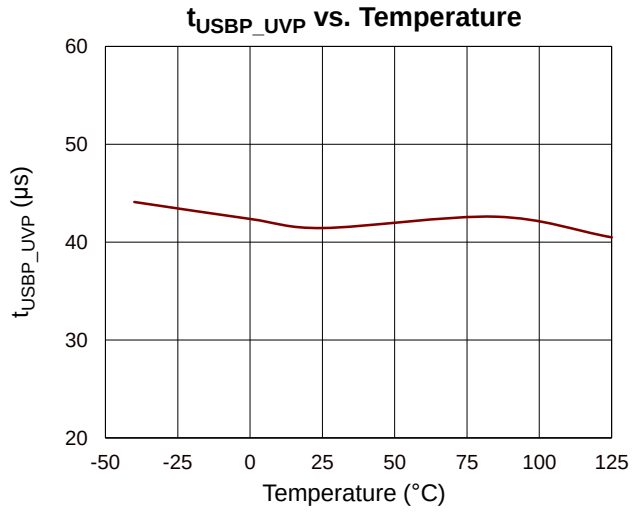


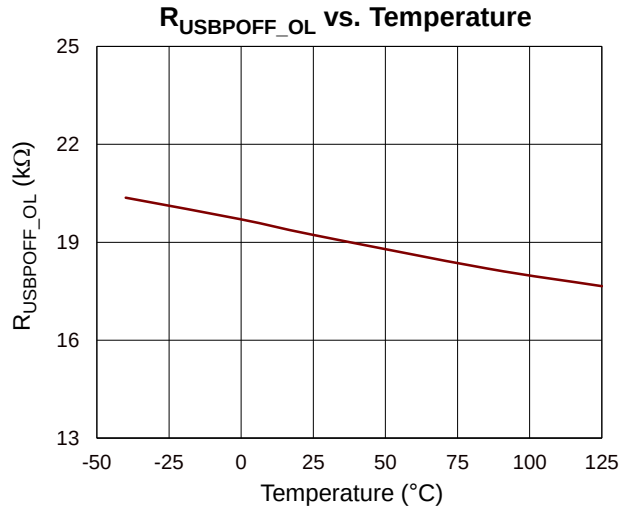


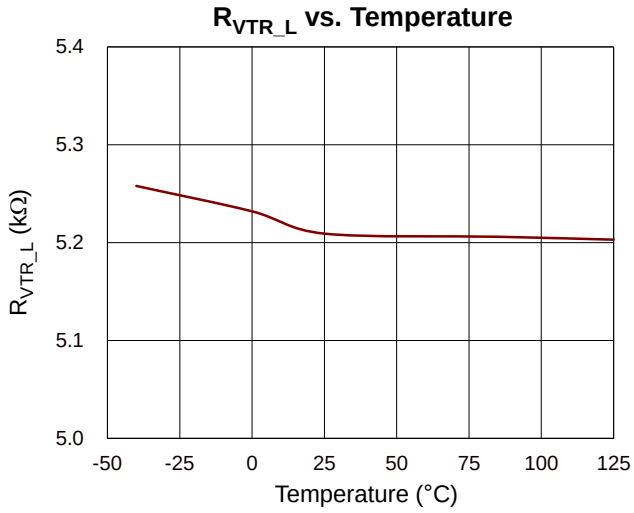


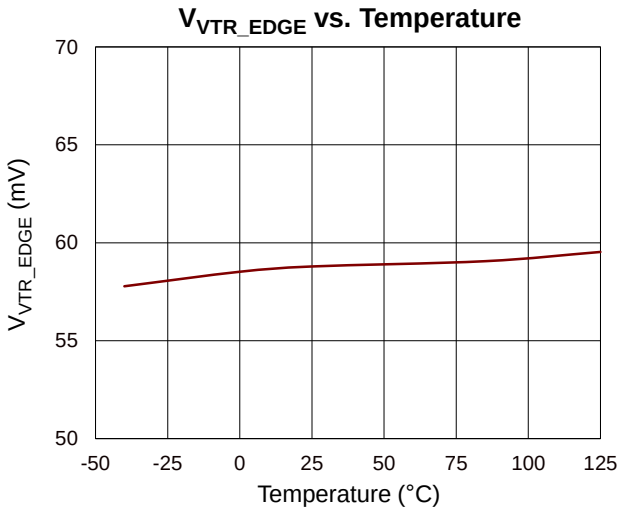


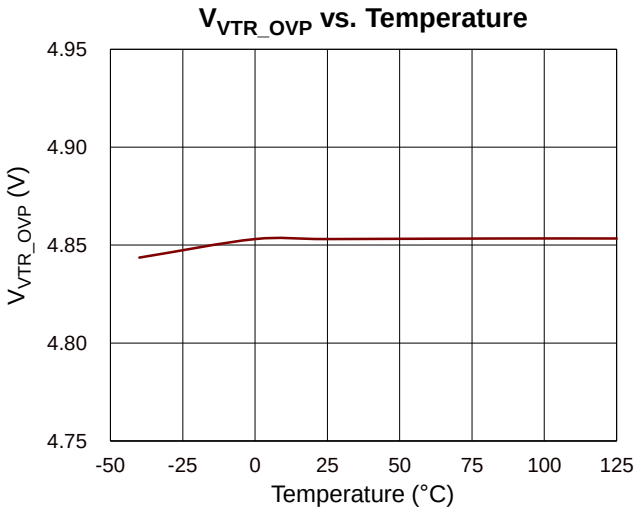












15 Operation

The RT7204E is a highly integrated secondary-side programmable controller, providing various functions and comprehensive protections for off-line AC-DC converters.

15.1 Power Structure

The RT7204E features internal regulated voltages, V5 and V2, which are derived from VDD supply. These voltages are utilized to power the internal circuit and the internal microprocessor (MCU), respectively.

15.2 Constant Voltage and Constant Current (CV/CC) Regulators

Two regulators are paralleled and connected to the OPTO pin, an open-drain output. Each feedback loop operates similarly to the traditional TL431 shunt regulator. However, the V_{OPTO} operating voltage range is broader, extending from 0.3V to 25V.This extended range facilitates the design of converters with a wider output voltage range. When the VDD voltage is below the turn-on threshold V_{VDD_ON}, the OPTO pin remains in a high-impedance state. This feature is critical for ensuring a smooth power-on sequence. The reference voltages, V_{REF_CV} and V_{REF_CC}, for the voltage and current feedback loops are provided by the analog output voltages of an 11-bit DAC. With a resolution of 10mV for the DAC's CV output voltage, the system is capable of achieving high-precision CV and CC regulation.

15.3 Current Sense Amplifier

To minimize power loss of the current sense resistor, a low input offset amplifier with voltage gain of 32 is applied. When the 5mΩ (typical) R_{CS} goes with the voltage gain of 32, the resolution of the output current is approximately 6mA. The operation of the CV and CC loops is shown in Figure 1. The sensed output current is amplified by the current-sense amplifier as "I_{o_signal}", which is then sent to the current-loop regulator for constant-current regulation and also sent to the MCU, by way of an 11-bit ADC for analog-to-digital conversion, to update the output current status for the MCU.

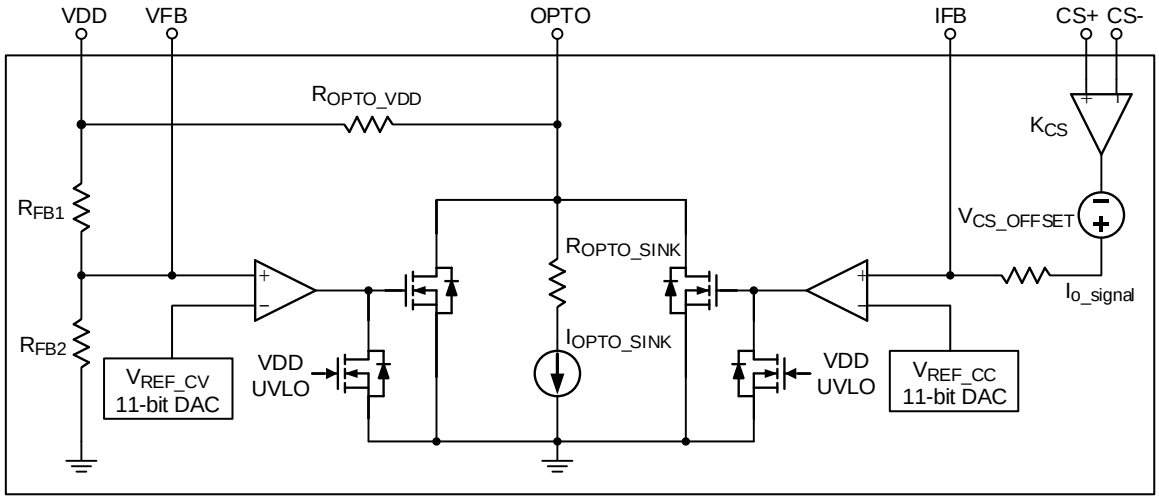


Figure 1. CV and CC Loops

15.4 External Temperature Sensing

As shown in Figure 2, the RT7204E provides the RT pin as a register-programmable current source to bias a remote thermal sensor, such as a thermistor (NTC). If the RT voltage falls below the over-temperature protection (OTP) threshold and the condition sustains for a programmed delay time, the OTP will be triggered.

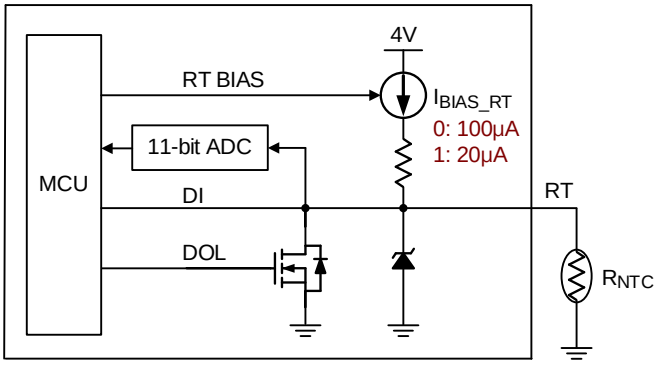


Figure 2. External Temperature Sensing

15.5 Interface of D+ and D-

The D+ and D- pins are used for BC1.2 compliance or for communication with other proprietary protocols. The D+ and D- pins, connected to the MCU via an ADC, can be reprogrammed for other purposes, including acting as analog or digital inputs or outputs, as shown in Figure 3.

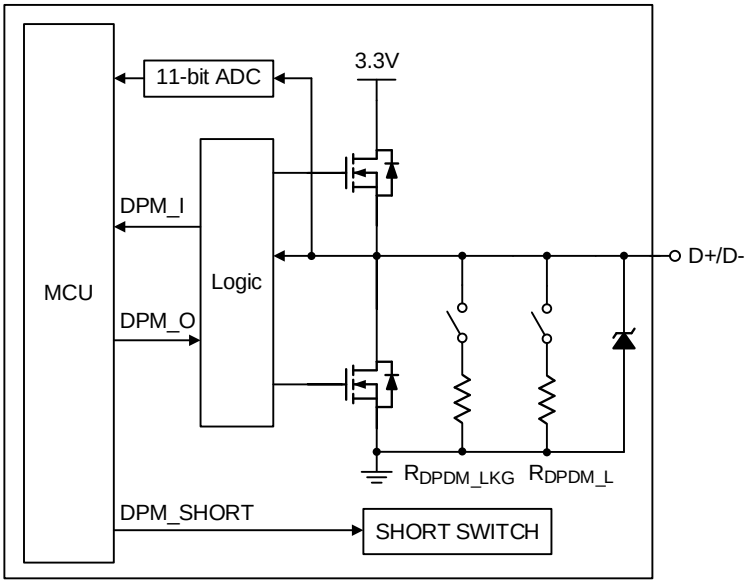


Figure 3. Interface of D+ and D-

15.6 Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with the USB Type-C specification. When configured as a Downstream Facing Port (DFP), three current capabilities of 80μA, 180μA, and 330μA, provided by each of the CC pin, will be advertised to an Upstream Facing Port (UFP) as the default USB current, 1.5A, and 3.0A, respectively. If the resistor Ra on the powered cable termination is detected, the VCONN power and switches can be controlled by MCU with 100mW output capability during the identification of E-marked cable. The interface of CC1 and CC2 is shown in Figure 4.

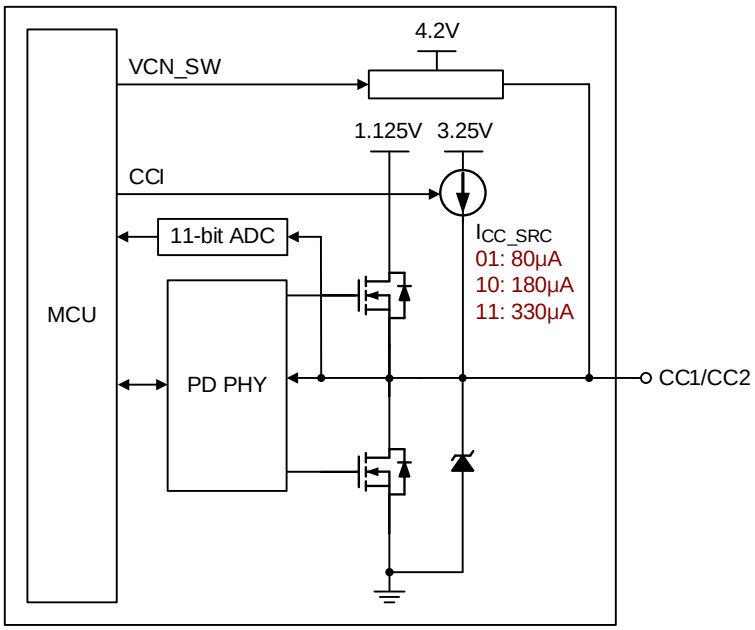


Figure 4. Interface of CC1 and CC2

15.7 Open-Drain Driver of The VBUS Pin

Figure 5 shows the VBUS pin with the open-drain drivers. The internal bleeder circuit at the VBUS pin is used to discharge the VBUS capacitor to Vsafe0V upon the detachment of a connected device. The VBUS pin voltage provides real-time VBUS voltage detection by ADC, and the voltage between VDD and VBUS can be compared to achieve VBUS drop protection.

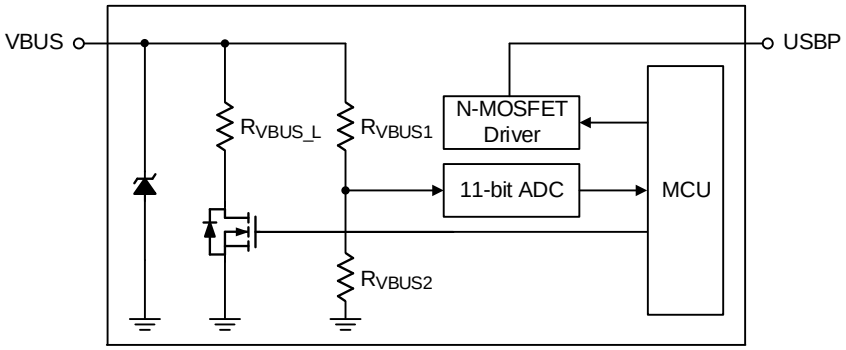


Figure 5. Open-Drain Driver of the VBUS Pin

15.8 I²C Communication

In multi-port applications, the RT7204E can share the output power through I²C communication by connecting GPIO1 (SDA) and GPIO2 (SCL) to the other master controller, respectively.

15.9 Rectification Detection

The RT7204E provides the VTR pin to sense the transformer voltage, which is the drain voltage of the SR MOSFET, as shown in Figure 6. By connecting the drain of SR MOSFET to the VTR pin through a divider resistor, the RT7204E can keep the divided voltage of SR V_{DS} plateau and read the internal peak holding voltage, V_{VTR_PH}, by ADC for V_{IN} detection. With a proper setting of VTR blanking time, the RT7204E can distinguish between the PWM switching and the DCM ringing to prevent false detection of the PWM switching state, which is used to achieve LPS protection.

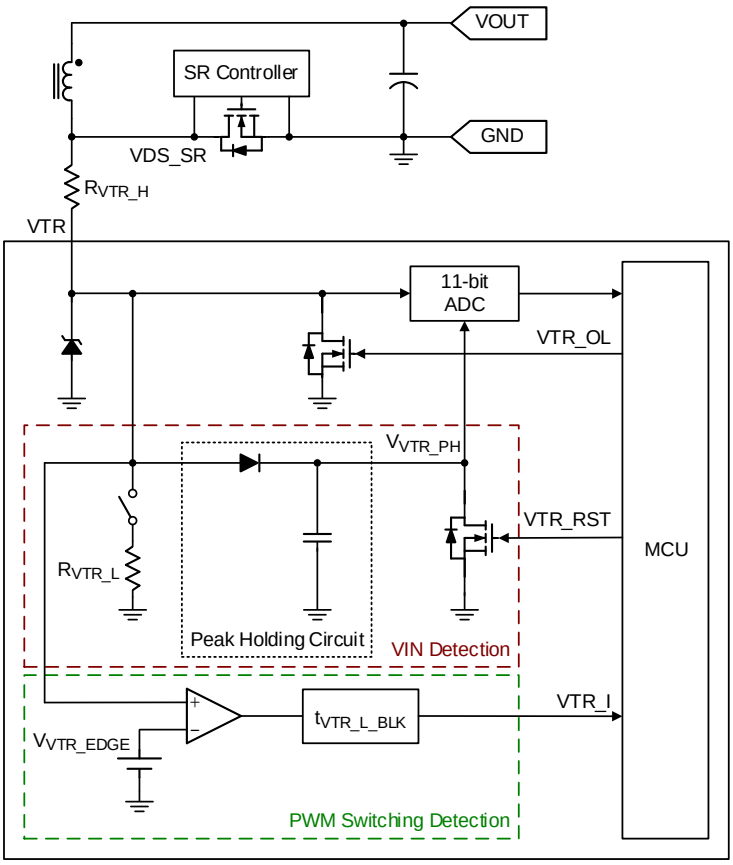


Figure 6. Rectification Detection

16 Application Information

(Note 8)

16.1 Constant Voltage (CV) Loop

As shown in Figure 7, the RT7204E integrates two error amplifiers (EA), which are connected with the feedback compensators to regulate the output voltage and current, respectively. The output voltage is determined by the following equation:

$V_{OUT} = K_{FB} \times V_{REF\_CV}$

where

$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2} = 10$

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, which is controlled by MCU.

16.2 Constant Current (CC) Loop

As shown in Figure 7, the RT7204E integrates a virtually zero input offset high-side current-sense amplifier with differential mode inputs to minimize noise interference. The sensed signal, I_{o_signal}, is fed into an 11-bit ADC for monitoring and processing by the MCU. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed according to the requirements of charger.

Both the constant voltage and the constant current compensation loops are connected to the OPTO pin. The OPTO driver sinks current through an external resistor R_D and an optocoupler that isolates the secondary side from the primary side, and then feedbacks the compensation signal to the primary side. Note that for better linearity of the loop compensation range, R_D should be designed to cover the operation at the minimum output voltage.

$$\frac{(V_{OUT\_MIN} - V_F - 0.3V)}{R_D} \times CTR \geq I_{COMP\_MAX}$$

where

CTR: Current transfer ratio of the optocoupler

V_F: Forward voltage of the optocoupler

0.3V: The minimum OPTO voltage for the OPTO driver to sink the minimum OPTO sink current

I_{COMP_MAX}: The maximum COMP sourcing current of a traditional PWM controller in the primary side. It is a current sourced from an internal bias through a built-in pull-up resistor connected to the COMP pin in the PWM controller.

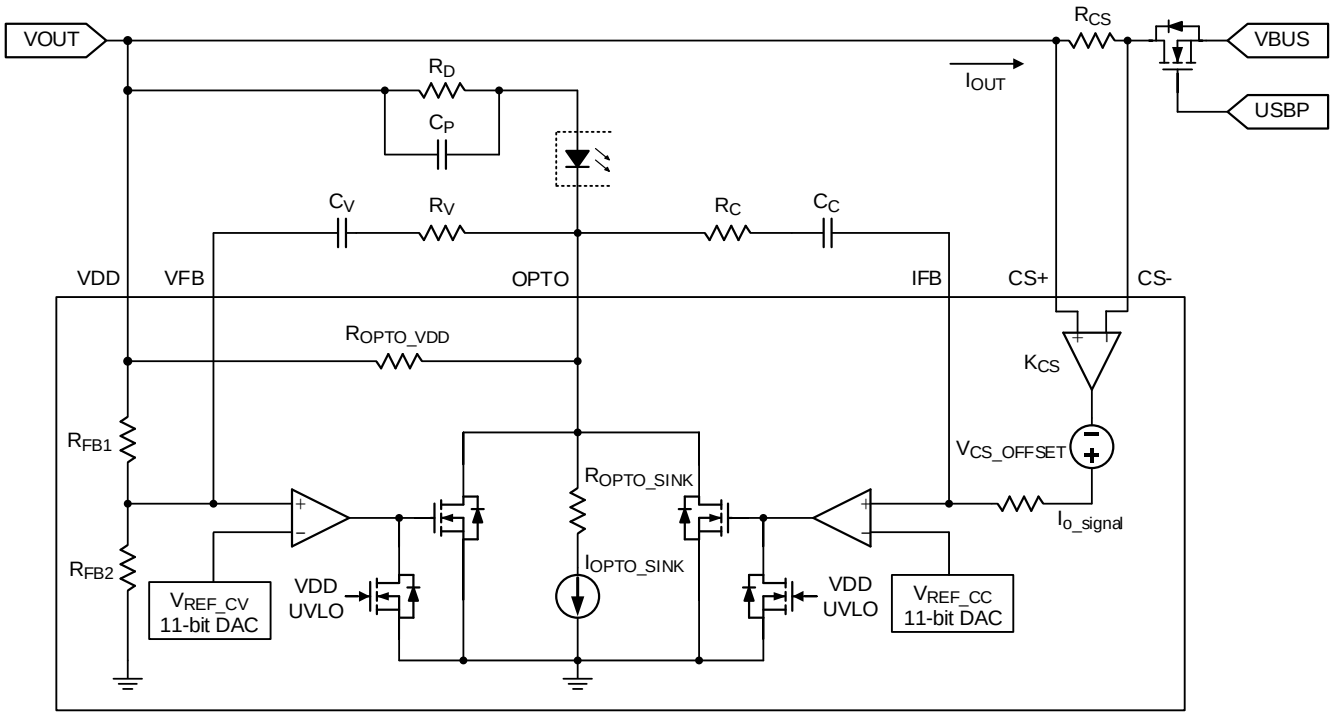


Figure 7. CV and CC Loops

16.3 Power-Up Sequence

Figure 8 shows the timing diagram for the power-up sequence. When start-up, the default output voltage is set to 5V. Once a Type-C cable is connected, the UFP delivers voltage and current settings to the RT7204E, enabling the MCU to decode these settings and program reference voltages, V_{REF_CV} and V_{REF_CC}, for the CV and CC loops. These loops are the analog outputs converted by the DAC.

The RT7204E directly drives an external blocking N-MOSFET on the USBP pin, which features a programmable soft-start function to ensure a smooth VBUS turn-on under capacitive load conditions. If the Type-C cable is disconnected, or if the output current falls below the power-saving mode threshold, typically set at 200mA, the RT7204E will enter power-saving mode. In this mode, it operates with ultra-low current, significantly reducing total input power. Conversely, if the output current increases and exceeds the power-saving mode threshold, or if any input/output signal is toggled, the RT7204E will exit power-saving mode.

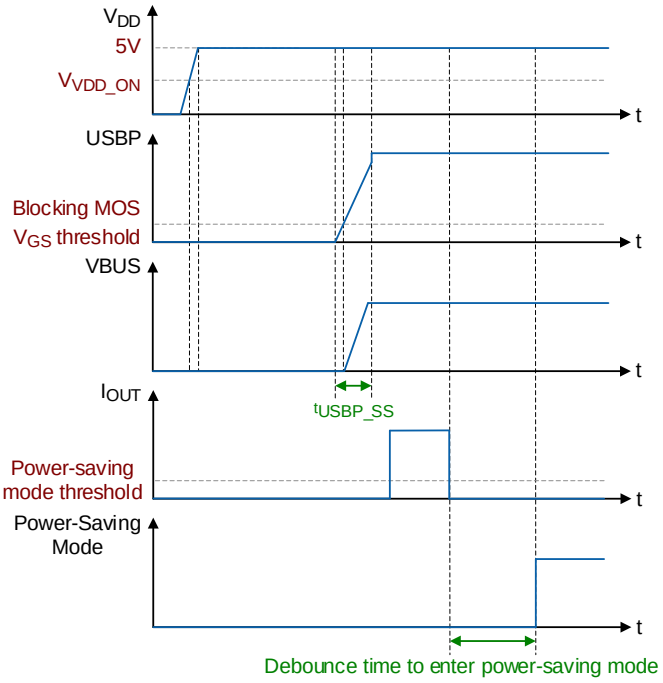
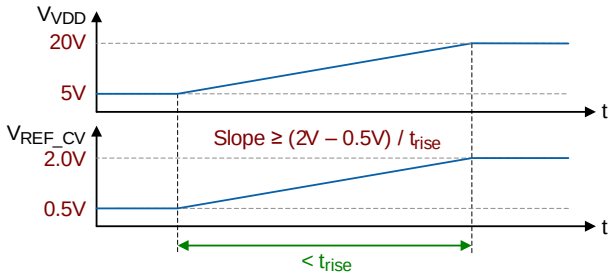


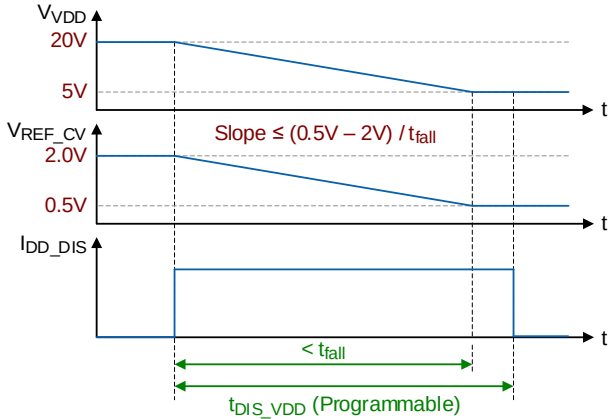
Figure 8. The Output Sequence during Start-Up

16.4 Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of UFP. Both the rise time and fall time of output voltages should be less than the defined specification, as shown in Figure 9.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 9. Output Voltage Transient Waveforms

The RT7204E provides a control for the discharge current from the VDD pin. This function serves as a bleeder to facilitate the discharge of the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as VOUT from 20V to 5V. During the falling interval, the capability of I_{DIS_VDD} must take the operating voltage and the output capacitors of the system into consideration. The discharge current can be programmed by the internal register according to VDD voltage level, as shown in Figure 10.

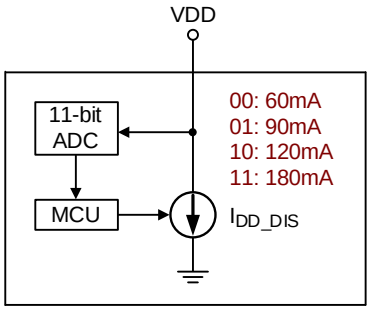


Figure 10. Discharge Current Control from The VDD Pin

16.5 Output Overvoltage Protection

As shown in the Figure 11, the RT7204E provides a fast turn-off blocking N-MOSFET as a backup VOUT overvoltage protection mechanism, in the event of malfunction due to aging of the optocoupler in the feedback loop. If the internal voltage related to VDD exceeds the programmable threshold V_{VDD_OVP}, the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will be sent to the embedded MCU to enable customized protection behavior.

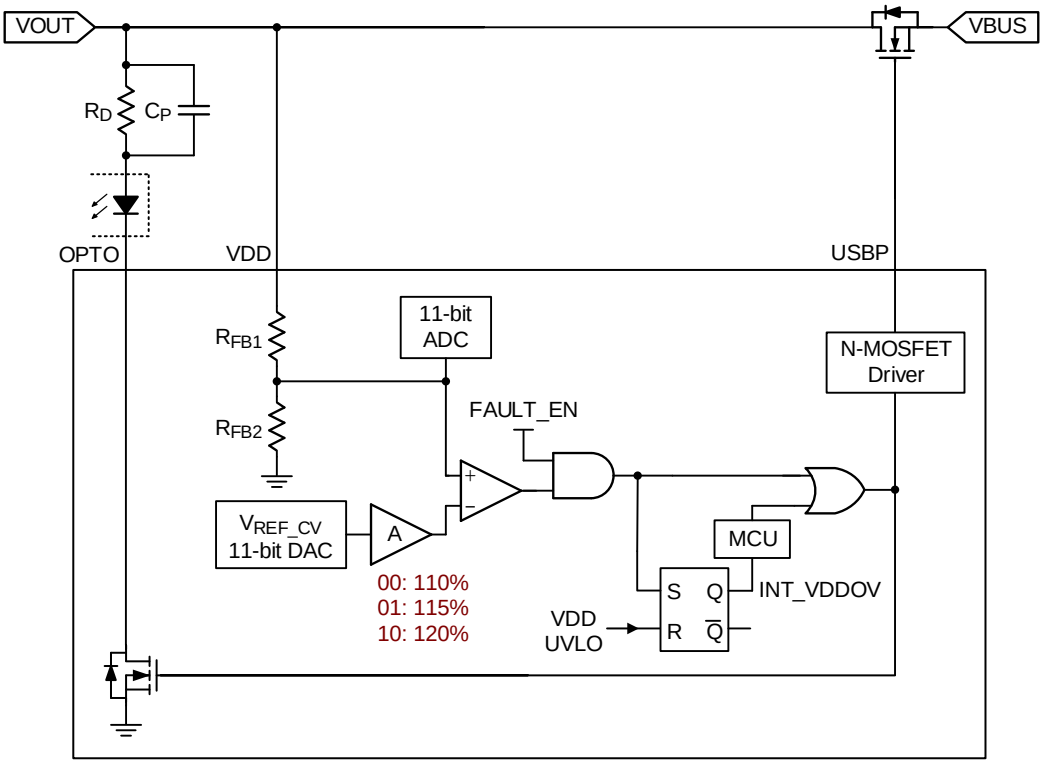


Figure 11. OVP Functional Diagram

For the typical protection behavior of shutdown with auto-recovery, the OPTO pin voltage will be latched low to limit the output power until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}, as shown in Figure 12. After V_{DD} is turned off, V_{OPTO} is released and V_{DD} will be automatically powered up again.

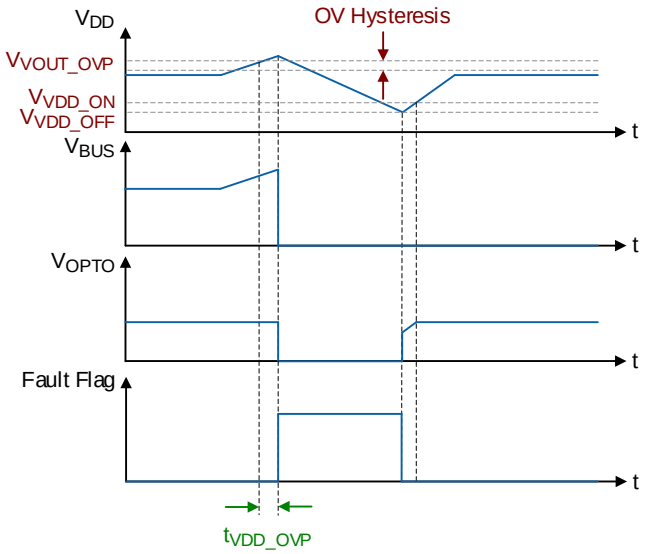


Figure 12. Timing Sequence of the OVP Function

16.6 Blocking N-MOSFET Control

The RT7204E provides a charge-pump driver for controlling an external blocking N-MOSFET, which is shown in Figure 13. The N-MOSFET is activated once the communication is set up with an UFP, or a sink termination resistor R_d at the CC1/CC2 pin of a USB Type-C connector is detected. The blocking N-MOSFET can be quickly turned off in the event of any fault condition. In the case of a VOUT overvoltage condition, the blocking N-MOSFET will be turned off to protect the UFP from potential damage. When VOUT is shorted to GND, the N-MOSFET will automatically turn off, and the output power will be limited. Additionally, to prevent the IO pins from damaging due to abnormal contact with VBUS at the USB Type-C receptacle, a quick-interruption feature is designed to turn off the blocking N-MOSFET.

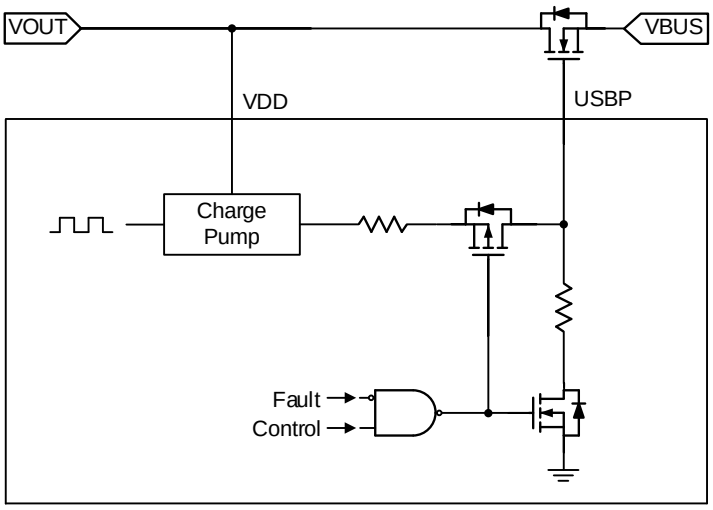


Figure 13. Blocking N-MOSFET Control

16.7 VBUS Drop Protection

The VBUS drop protection provides an additional mechanism to protect the output short circuit, as shown in Figure 14. It is designed to detect the voltage difference between VDD and VBUS, which includes current-sense resistor and blocking N-MOSFET drain-to-source. When the voltage difference exceeds the VBUS drop threshold, the blocking N-MOSFET will be clamped-off immediately.

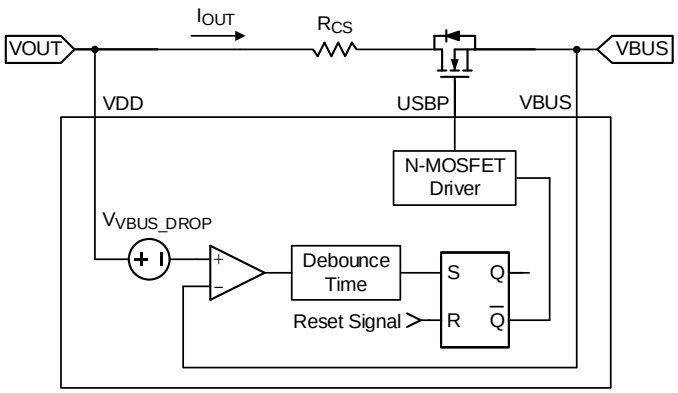


Figure 14. VBUS Drop Protection

16.8 Temperature Sensing and Thermal Protection

The RT7204E provides the RT pin for over-temperature protection or thermal monitoring. As shown in Figure 2, the RT pin sources a constant bias current for a remote thermal sensor of an NTC thermistor, connected from the RT pin to GND, for temperature sensing. If the RT voltage falls below a programmable threshold voltage and the condition sustains for a programmable deglitch time, the over-temperature protection will be triggered.

The bias current passing through the RT pin can be programmed to either 100μA or 20μA via a register setting. Selecting the appropriate bias current enhances the linearity of the temperature sensing function across a temperature range of 25°C to 100°C. Additionally, The RT7204E can transmit the sensed RT voltage signal to the UFP via the protocol (Vendor Defined Message), if necessary. Figure 15 shows the RT voltages vary with temperature at two different bias currents using an NTC thermistor TTC104 as an example.

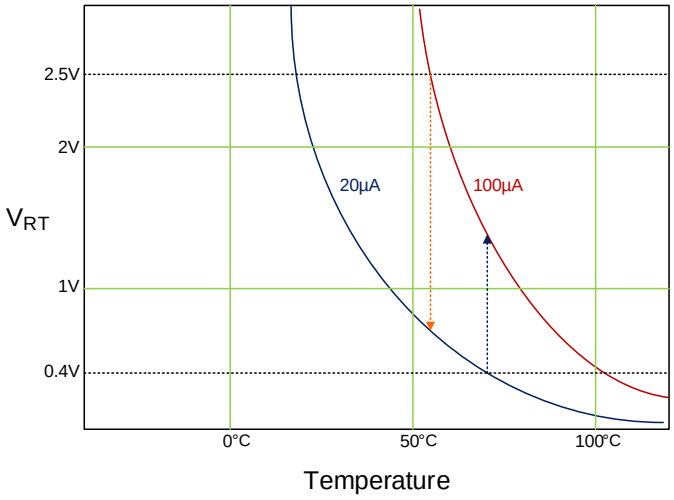


Figure 15. The RT Voltages vs. Temperature

16.9 V_{IN} Detection and LPS Protection

The RT7204E can detect the input voltage and implement LPS protection by sensing the drain voltage of the low-side SR MOSFET, as shown in Figure 6. The recommended divider resistance, R_{VTR_H}, between the SR MOSFET drain terminal and the VTR pin is 150kΩ. Due to varying component stress and thermal considerations under AC high/low line conditions, the power rating and OTP threshold can be adaptively customized through input voltage detection for a more compact design. The VTR pin also provides AC OFF detection to prevent the RT7204E from being reverse biased through the body diode of a blocking N-MOSFET. If there is no switching signal on the VTR within the programmable delay time, a flag will be sent to the MCU to fulfill power saving requirements.

16.10 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 4x4 package, the thermal resistance, θ_{JA}, is 39.6°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (39.6°C/W) = 2.52W for a WQFN-24L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 16 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

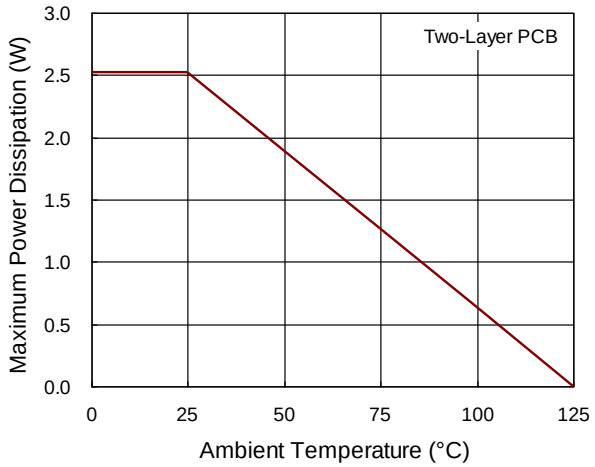
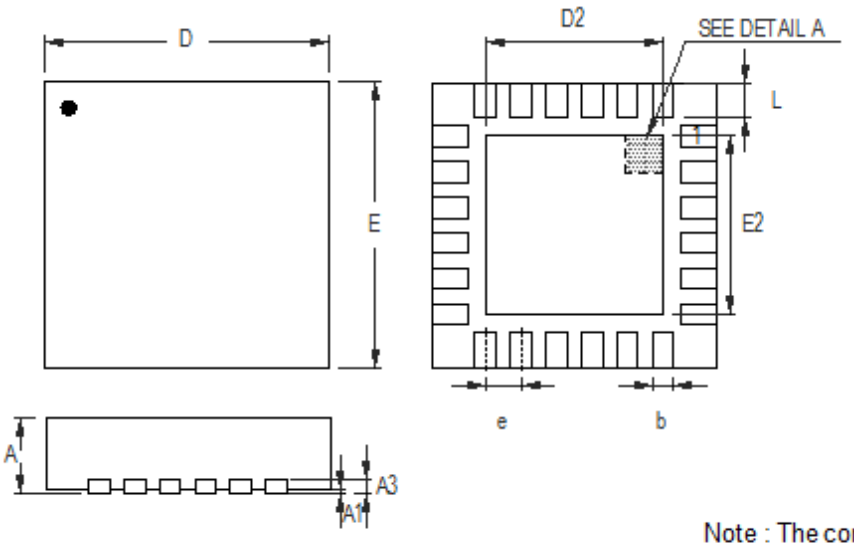
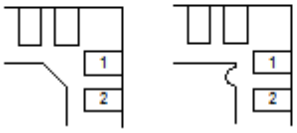


Figure 16. Derating Curve of Maximum Power Dissipation

Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

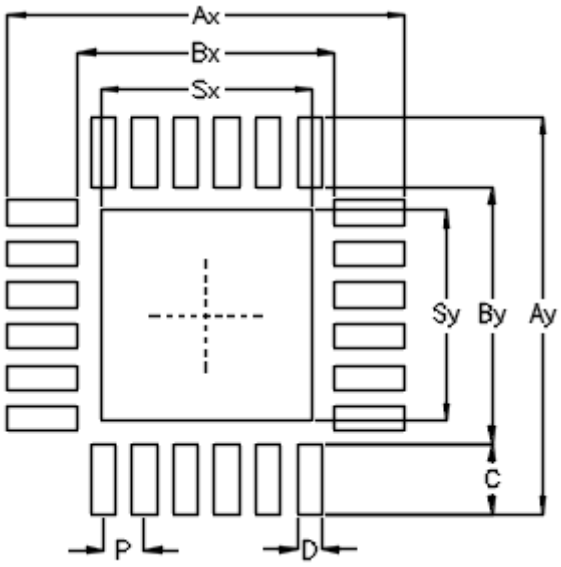
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

Note 9. The package of the RT7204E uses Option 2.

18 Footprint Information

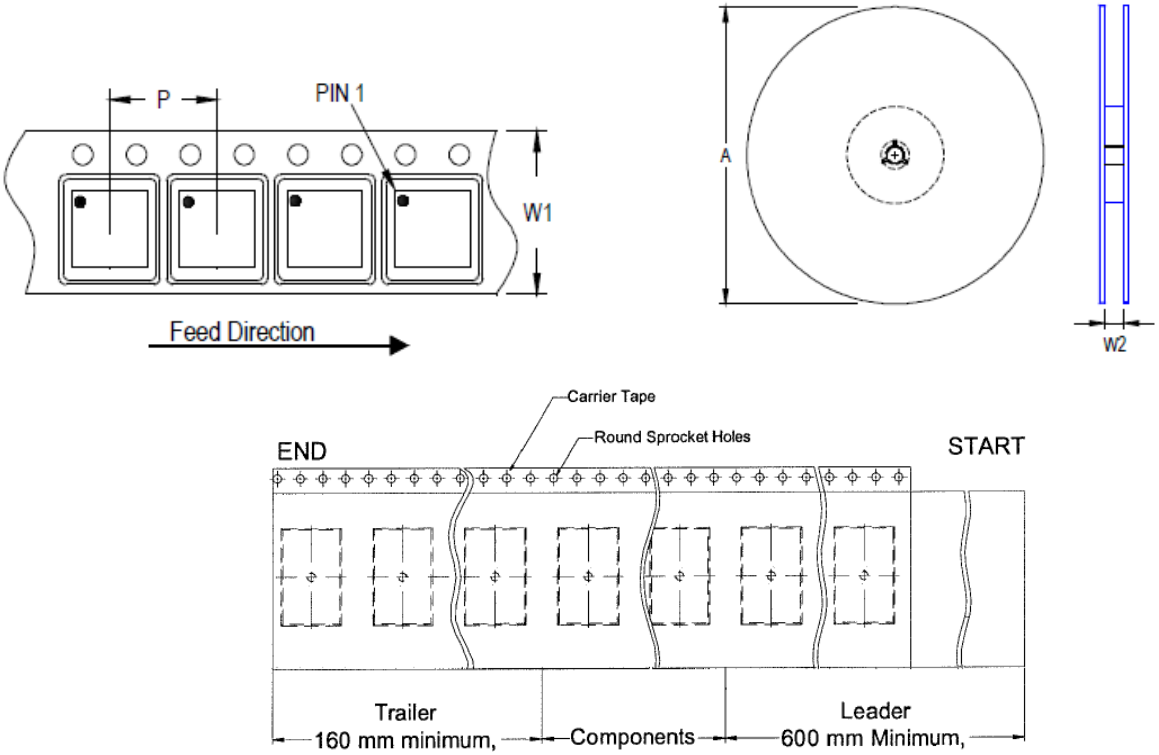


Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24	Option1	24	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.55	2.55	±0.05
	Option2									2.60	2.60	

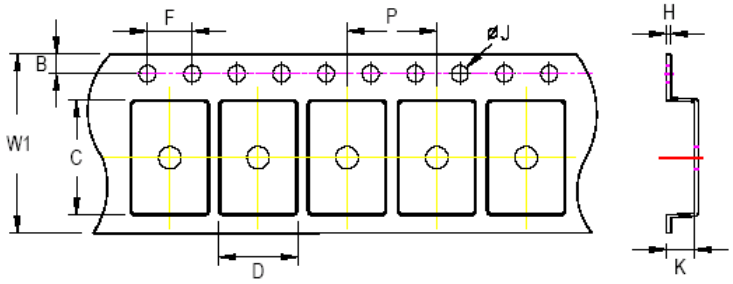
Note 10. The package of the RT7204E uses Option 2.

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size.

The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
00	2024/5/23	Final	Ordering Information on P2 Application Information on P39