High-Integration VOOC (Voltage Open Loop Multi-Step Constant-Current Charging) Protocol Controller with Internal Feedback Compensation

General Description

The RT7203V is a programmable controller with integration of VOOC protocol, and the built-in feedback compensation. An internal MCU is designed in to handle various proprietary protocols via the D+/D- interface.

This controller is a specific design with high integration for off-line AC-DC converters possessing high power density. The RT7203V integrates a constant voltage loop, a constant current loop and the built-in compensation in feedback control to better regulate the design, this IC not only possesses a feature of component saving via its feedback compensation, but also provides an enhanced transient response and safety protections via the integration of diverse functions.

In applications of high precision control, dual operational amplifiers are adopted in the Digital-to-Analog Converter (DAC) to provide reference voltages used for regulation of voltage loop and current loop in programming the constant voltage (CV) and the constant current (CC), respectively.

Ordering Information

RT7203V □□-□

- Programmed Firmware Code AABBX
  - AA : Application Code
  - BB : Model Code
  - X : Customer Approved Version Code
- Package Type
  - S : SOP-8
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- RT7203V Version
  - (Refer to Functional Table)

Note :

The products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

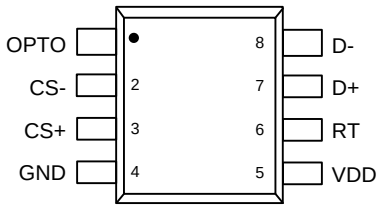
- **Protocol Support**
  - **Proprietary Protocols**
- **Highly Integrated**
  - **Suited for 3.3V to 13V VDD Range**
  - **Embedded MCU with an Mask ROM of 20kB, an OTP-ROM of 4kB, and an SRAM of 0.75kB**
  - **Built-in Shunt Regulators for Constant Voltage and Constant Current Control**
  - **Built-in Feedback Compensation**
  - **Built-in Temperature Sensing**
  - **Built-in 10-bit Analog-to-Digital Converter**
  - **VDD Pin for Quick Discharge of Output Capacitor**
  - **< 3mA Operating Current in Normal Mode**
  - **< 1.5mA Operating Current in Sleep Mode**
  - **< 900μA Operating Current in Green Mode**
- **Protection**
  - **Adaptive Output Over-Voltage Protection**
  - **Adaptive Under-Voltage Protection**
  - **D+/D- Over-Voltage Protection**
  - **Firmware-Programmable Contant Current Protection**
  - **Firmware-Programmable Over-Current Protection**
  - **Firmware-Programmable Over-Temperature Protection**

Applications

- Travel Adapters with VOOC Protocol

Pin Configuration

(TOP VIEW)



SOP-8

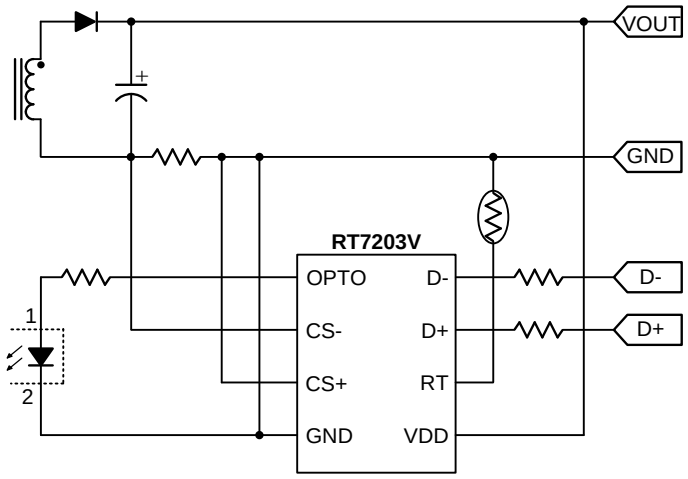
Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

RT7203V Functional Table

Version	RT7203V
Output Voltage Supported	3.3V to 13V
V_{OUT} Scaling Factor R_{FB2} / (R_{FB1} + R_{FB2})	1/6
Built-in FB Resistor	O
Application	Proprietary Protocols

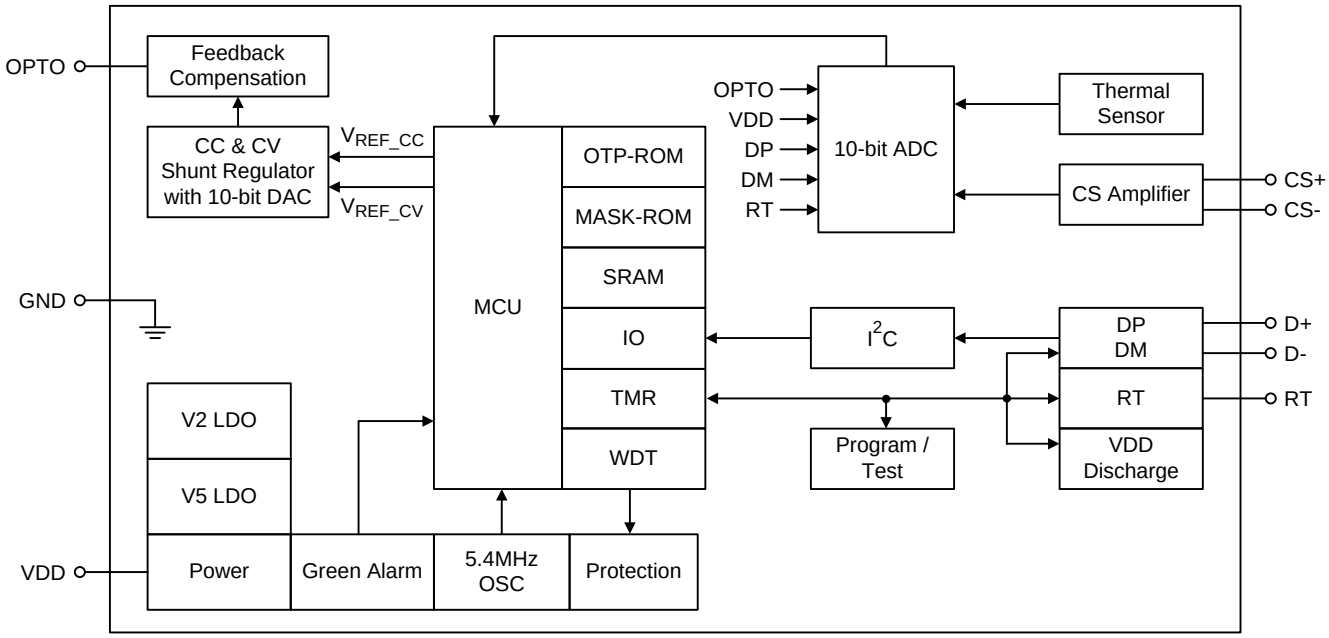
Simplified Application Circuit



Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	OPTO	AO	Current source output for optocoupler connection.
2	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
3	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
4	GND	GND	Ground.
5	VDD	PWR	Supply input voltage.
6	RT	A/D IO	Remote thermal sensor connection node for over-temperature protection.
7	D+	A/D IO	USB D+ channel.
8	D-	A/D IO	USB D- channel.

Functional Block Diagram



Operation

The RT7203V is a highly integrated programmable secondary-side controller for VOOC protocol featured with innovative functions and protections for off-line AC-DC converters.

Power Structure

Biased by the VDD pin, the RT7203V has two regulated DC output voltages, V_5 and V_2, to supply the internal circuit and the internal microprocessor (MCU). A bypass capacitor at the VDD is required to improve stability of the internal LDO and to minimize regulated ripple voltages.

Constant Voltage and Constant Current (CV/CC) Regulators

The RT7203V has two transconductance amplifiers parallel connected to the feedback compensator. The feedback compensator sends signal to the OPTO pin to regulate the output voltage and the output current. The operation of each feedback loop is opposite to that of a traditional TL431 shunt regulator. The OPTO pin is in high impedance state, if the VDD voltage is still below a UVLO threshold V_{VDD_ON}, which ensures a smooth power-on sequence. The reference voltages of the voltage feedback loop and the current feedback loop (V_{REF_CV} and V_{REF_CC}, respectively) are analog output voltages from a 10-bit DAC. In this loop, the analog output voltage of the 10-bit DAC ranges from V_{DAC_MIN} = 0.523V to V_{DAC_MAX} (typical 2.3V), which makes output voltage resolution as small as 10mV scale to achieve high-precision CV regulation.

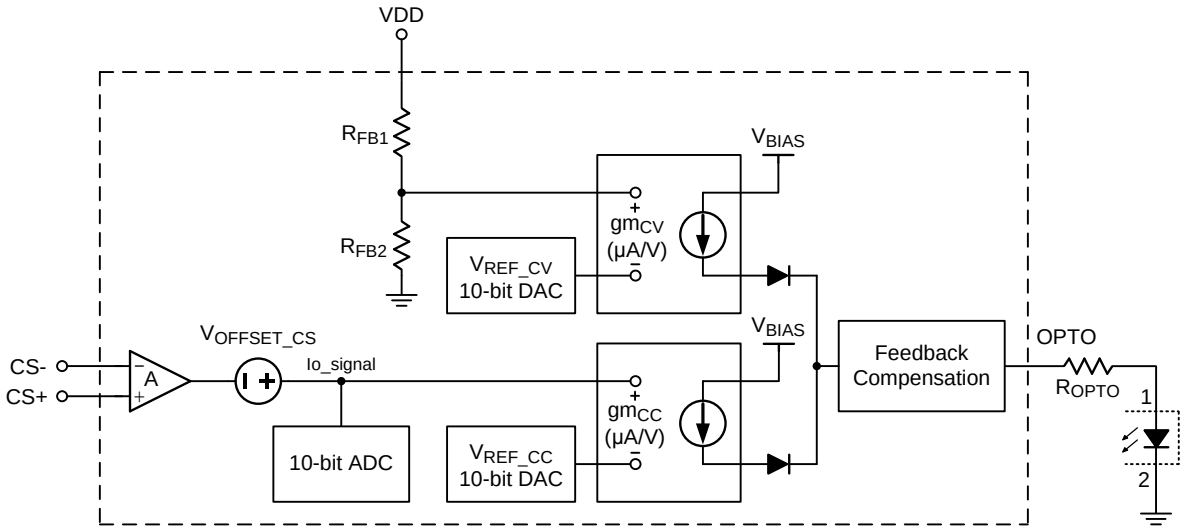


Figure 1. CV/CC Loops and Current Sense

Current Sense

To minimize power loss of the current sense resistor in the converter, the RT7203V employs an amplifier with virtually zero input offset voltage a voltage gain of 20 or 40. The sensed output current is amplified by the current-sense amplifier, shown as the “Io_signal” in Figure 1, which is then sent to the current-loop regulator for constant-current regulation and also sent to the MCU, via a 10-bit ADC for analog-to-digital conversion, to update the output current status for the MCU.

External Temperature Sensing

The RT7203V equips the RT pin, as a register-programmable current source to bias a remote thermal sensor, such as a thermistor (NTC) shown in Figure 2. If the RT voltage is lower than the over-temperature protection (OTP) threshold, and this condition sustains for a period of the programmed time delay, the OTP is then activated and triggered.

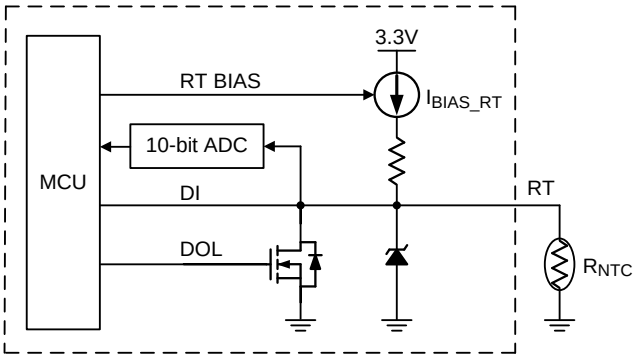


Figure 2. External Temperature Sensing

Interface of D+ and D-

The D+ and D- pins are used for BC1.2 compliance or for communication with other proprietary protocols. The D+ and D- pins, connected to the MCU via an ADC, can be reprogrammed for other purposes. These two pins can also be used as an analog/digital input or output, as shown in Figure 3.

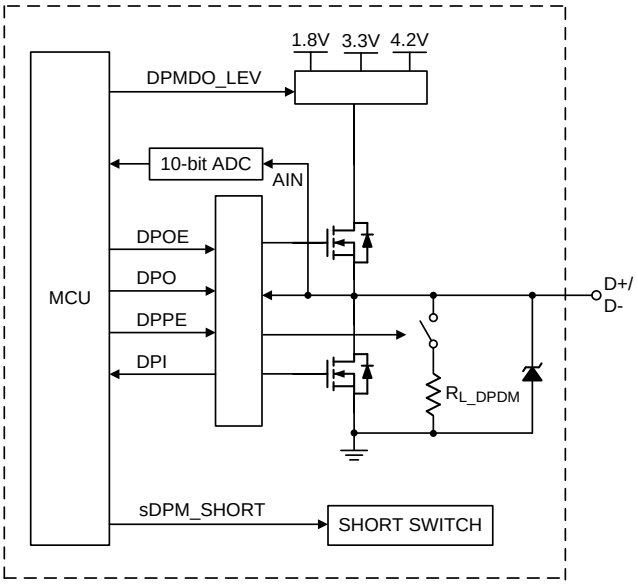


Figure 3. Interface of D+ and D-

Absolute Maximum Ratings (Note 1)

- VDD to GND ---------- –0.3V to 17V
- OPTO, CS-, CS+, RT, D+, D- to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.38W
- Package Thermal Resistance (Note 2)
  SOP-8, θ_{JA} ---------- 261.1°C/W
  SOP-8, θ_{JC} ---------- 47°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VDD ---------- 3.3V to 13V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDD Section							
VDD Turn-On Threshold	V_{VDD_ON}			3.4	3.5	3.6	V
VDD Turn-Off Threshold	V_{VDD_OFF}			2.85	2.95	3.05	V
VDD Turn-On/Off Hysteresis	V_{VDD_HYS}			--	0.55	--	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 3.2V		--	200	300	μA
VDD Operating Current	I_{DD_OP}	V_{DD} = 5V		--	--	4.5	mA
VDD Green-Mode Current	I_{DD_GREEN}	V_{DD} = 5V		--	700	900	μA
Maximum VDD Over-Voltage Protection Threshold	$V_{MAX\_VDD\_OVP}$			14.5	15.5	16.5	V
Register-Programmable Over-Voltage Protection Threshold	V_{VOUT_OVP}	With respect to V_{REF_CV}	00	104.5	110	115.5	%
			01	109.2	115	120.8	
			10	114	120	126	
			11	Disable			
VDD Over-Voltage Protection Deglitch Time	t_{D_VDDOVP}	(Note 5)		25	30	35	μs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable VDD Under-Voltage Wake-Up Threshold	$V_{DD\_UV\_WK}$	With respect to V_{REF_CV}. It can be disabled by firmware.	0	85.5	90	94.5	%
			1	80.75	85	89.25	
VDD Under-Voltage Deglitch Time	$t_{D\_VDD\_UV}$			--	50	--	μs
Register-Programmable VDD Discharge Current	I_{DD_DIS}	It is necessary to gradually reduce the discharge current before closing I_{DD_DIS}.	00	15	30	45	mA
			01	42	60	78	
			10	63	90	117	
			11	84	120	156	
VDD Discharge Current Step Change Delay Time	t_{STEP_BLD}	When BLD is disabled. (Note 5)		80	100	120	μs
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} > 3V		5.13	5.4	5.67	MHz
Regulator Section							
V_{DD} Divider Resistor	R_{FB}	$R_{FB} = R_{FB1} + R_{FB2}$ R_{FB1} : VDD to VFB R_{FB2} : VFB to GND (Note 5)		336	420	504	kΩ
V_{OUT} Scaling Factor	K_{FB}	$(R_{FB1} + R_{FB2}) / R_{FB2}$ (Note 5)		5.94	6	6.06	--
Reference Voltage for Standby CV Regulators	$V_{ST\_REF\_CV}$			0.808	0.833	0.858	V
Minimum DAC Output Voltage for CV Regulators	$V_{DAC\_MIN\_CV}$	With 10-bit digital to analog converter.		--	0.523	--	V
Maximum DAC Output Voltage for CV Regulators	$V_{DAC\_MAX\_CV}$			2.277	2.3	2.323	V
Minimum DAC Output Voltage for CC Regulators	$V_{DAC\_MIIN\_CC}$	With 10-bit digital to analog converter.		--	0	--	V
Maximum DAC Output Voltage for CC Regulators	$V_{DAC\_MAX\_CC}$			1.863	1.882	1.901	
Maximum ADC Sense Voltage	V_{ADC_MAX}	With 10-bit analog to digital converter		2.277	2.3	2.323	V
Maximum OPTO Output Voltage	V_{OPTO_MAX}	V_{DD} = 3.2V to 13V, I_{SRC_OPTO} = 1mA		1.8	--	--	V
Maximum OPTO Output Clamping Voltage	$V_{OPTO\_MAX\_CLAMP}$	V_{DD} = 5V, I_{SRC_OPTO} = 1mA		2.1	2.4	2.7	V
Maximum OPTO Sourcing Current	I_{OPTO_MAX}			2	--	40	mA
Internal Resistor between OPTO and GND	R_{OPTO_GND}			48	60	72	kΩ

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Current Sense Amplifier							
Current Sense Voltage Gain	K_{CS}		0	--	20	--	V/V
			1	--	40	--	
Unit Gain Bandwidth		(Note 5)		1000	--	--	kHz
Current Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}			--	0.523	--	V
Internal Compensation Section							
Register-Programmable R_Z for Zero Point	R_Z	(Note 5)	000	8	10	12	kΩ
			001	24	30	36	
			010	40	50	60	
			011	64	80	96	
			100	96	120	144	
			101	136	170	204	
			110	184	230	276	
			111	248	310	372	
Register-Programmable C_Z for Zero Point	C_Z	It can be programmed by firmware. (Note 5)		4.16	--	4770	nF
Register-Programmable Zero Point	f_{ZERO}	It can be programmed by firmware. (Note 5)		0.10	--	3830	Hz
Register-Programmable Middle Gain		It can be programmed by firmware. (Note 5)		−20	--	27.89	dB
Overshoot Clamping Comparator		Ratio of V_{REF_CV}		104.5	110	115.5	%
Debounce Time of Overshoot Clamping	t_{OVC}			25	30	35	μs
D+, D- Section							
Pull-Low Resistance	R_{L_DPDM}	Disable/enable by firmware.		16	20	24	kΩ
Leakage Current	I_{LKG_DPDM}	Disable/enable by firmware.		0.5	1	1.5	μA
Register-Programmable Output High Voltage	V_{OH_OP}		00	Open Drain			V
	$V_{OH\_3.3V}$	V_{DD} = 5V, R_L = 15kΩ	01	2.97	3.3	3.63	
	$V_{OH\_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH\_4.2V}$		11	3.78	4.2	4.62	
Output Low Voltage	V_{OL_OP}	R_L = 15kΩ		--	--	0.2	V
	$V_{OL\_3.3V}$						
	$V_{OL\_1.8V}$						
	$V_{OL\_4.2V}$						
Register-Programmable DP and DM Input Level	V_{IN_LEV}		0	--	0	--	V
			1	--	0.4	--	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Register-Programmable Input High Trip Voltage	V_{IH_DPDM}		00	0.7 + V_{IN_LEV}	0.8 + V_{IN_LEV}	0.9 + V_{IN_LEV}	V
			01	1.3 + V_{IN_LEV}	1.4 + V_{IN_LEV}	1.5 + V_{IN_LEV}	
			10	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2 + V_{IN_LEV}	
			11	2 + V_{IN_LEV}	2.1 + V_{IN_LEV}	2.2 + V_{IN_LEV}	
Register-Programmable Input Low Trip Voltage	V_{IL_DPDM}		00	0.5 + V_{IN_LEV}	0.6 + V_{IN_LEV}	0.7 + V_{IN_LEV}	V
			01	1.0 + V_{IN_LEV}	1.1 + V_{IN_LEV}	1.2 + V_{IN_LEV}	
			10	1.7 + V_{IN_LEV}	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	
			11	1.8 + V_{IN_LEV}	1.9 + V_{IN_LEV}	2.0 + V_{IN_LEV}	
DPDM Switch On-Resistance	R_{ON_DPDM}			--	--	40	Ω
DP Comparison Threshold for Cable Detection	$V_{VTH\_DP\_CD}$	Send an interrupt to MCU when cable detached. Disable/enable cable detection by register.		0.2	0.3	0.4	V
Register-Programmable Cable Detection Debounce Time	t_{DP_CD}	(Note 5)	00	0.475	0.5	0.525	ms
			01	0.95	1	1.05	
			10	1.9	2	2.1	
			11	3.8	4	4.2	
Register-Programmable Input Debounce Time	t_{D_DPDMIN}	Debounce time = t_{D_DPDMIN} x K_{tD_DPDMIN} (Note 5)	0	Disable			µs
			1	142.5	150	157.5	
DP/DM Over-Voltage Protection Threshold	V_{DPDM_OVP}	Send a flag to MCU.		4.5	4.75	5	V
Register-Programmable DP/DM Over-Voltage Protection Debounce Time	t_{DPDM_OVP}	(Note 5)	00	0.095	0.1	0.105	ms
			01	0.95	1	1.05	
			10	4.75	5	5.25	
			11	14.25	15	15.75	
RT Section							
Open Loop Voltage	V_{RT_OP}	V_{DD} = 5V		2.6	3	3.4	V
Register-Programmable Internal Bias Current	I_{BIAS_RT}		00	95	100	105	µA
			01	18	20	22	
			10	4.5	5	5.5	
			11	Open			
RT Over-Voltage Protection Threshold	V_{RT_OVP}	1. Turn-off blocking MOSFET or not by register setting. 2. Send a flag to MCU.		4.5	4.75	5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Register-Programmable RT Over-Voltage Protection Debounce Time	t_{RT_OVP}	(Note 5)	30	50	70	μs
Thermal Sensor Section						
Thermal Sensor Error		25°C to 105°C	−10	--	10	°C

Note1. Stresses beyond those listed under ”Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

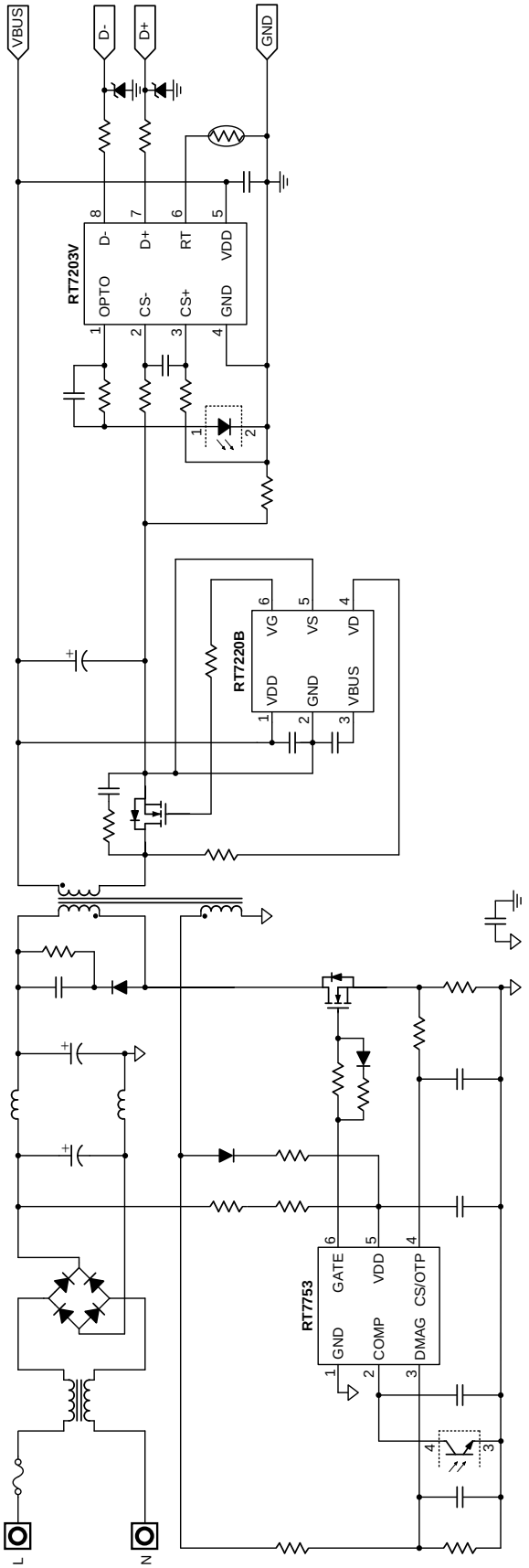
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

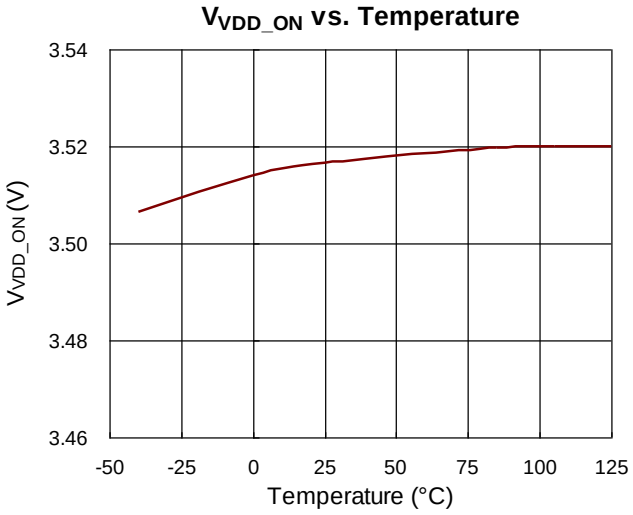
Note 4. The device is not guaranteed to function outside its operating conditions.

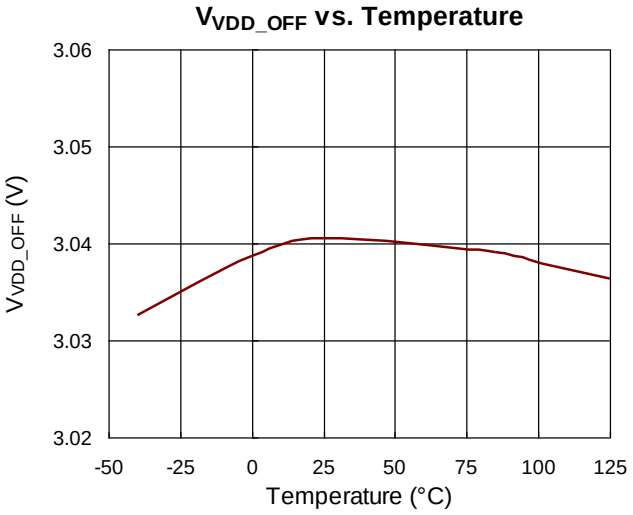
Note 5. Guaranteed by design.

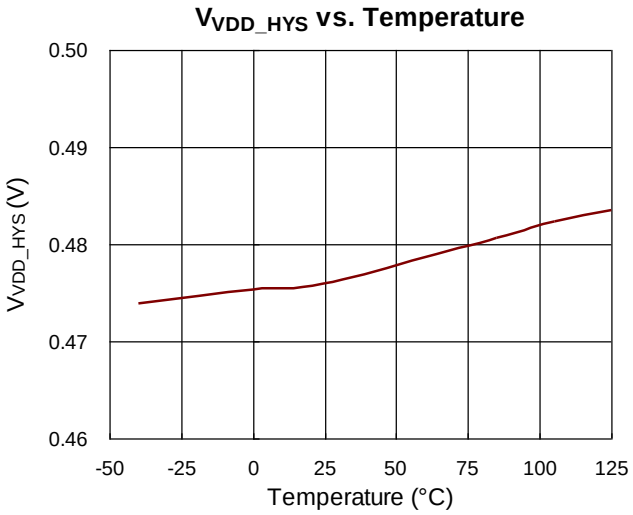
Typical Application Circuit

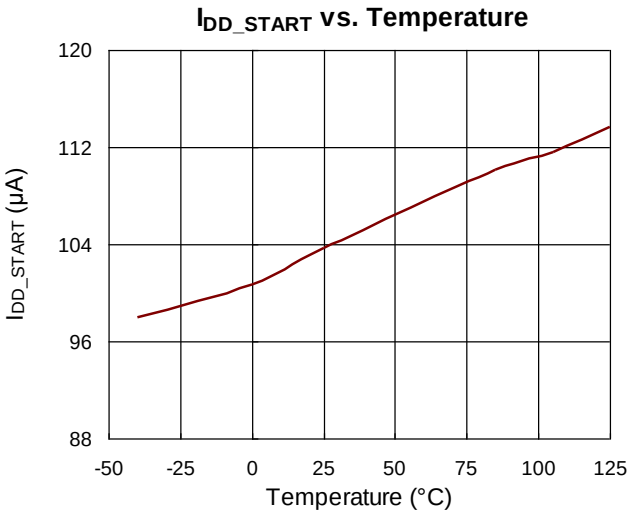


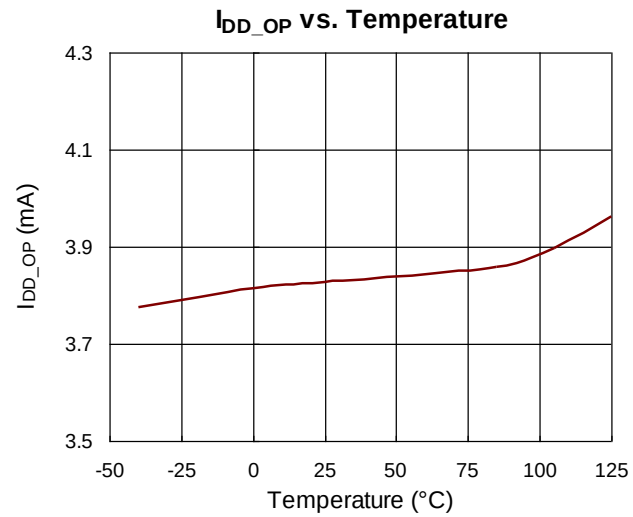
Typical Operating Characteristics

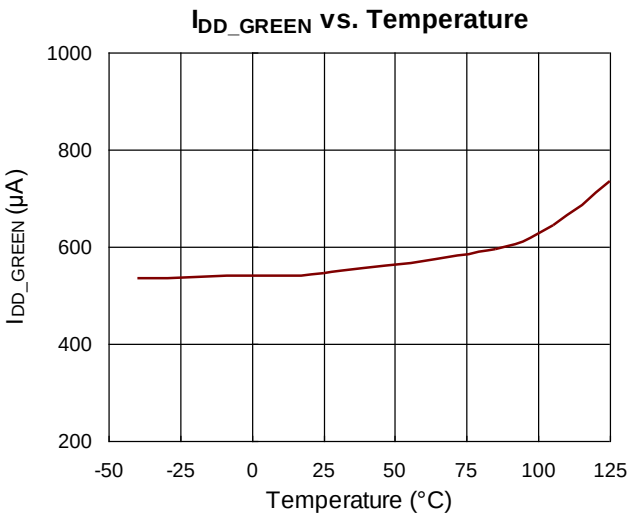




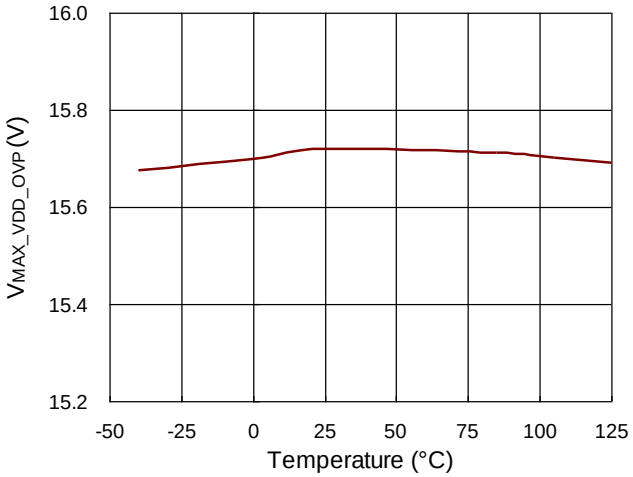




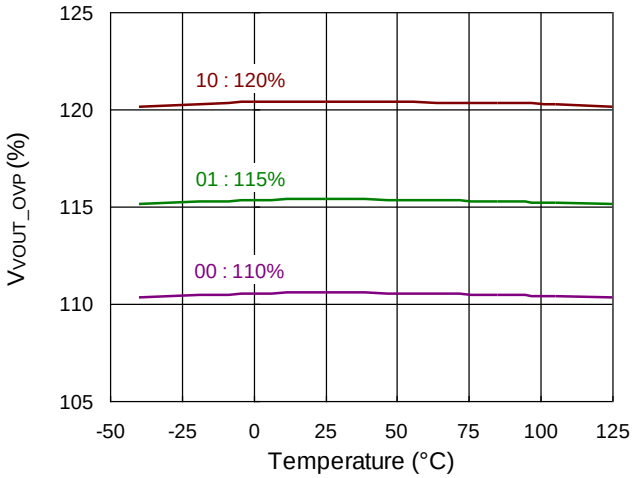




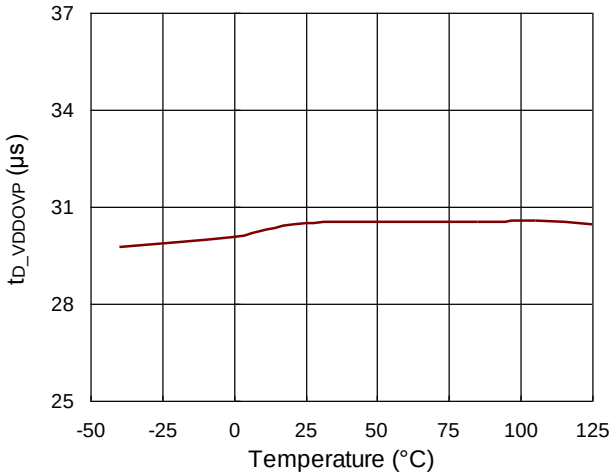
$V_{MAX\_VDD\_OVP}$ vs. Temperature



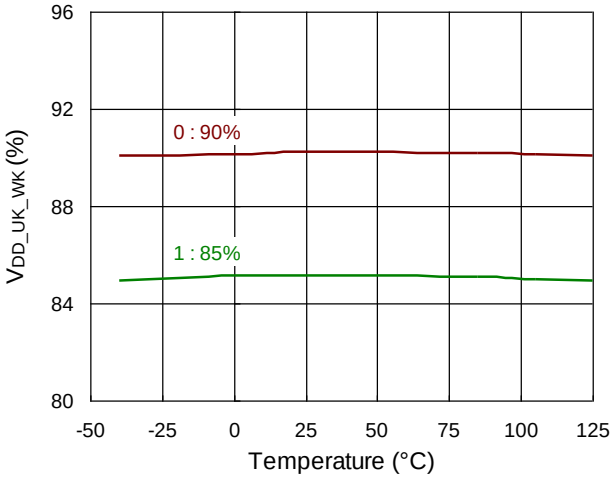
V_{VOUT_OVP} vs. Temperature



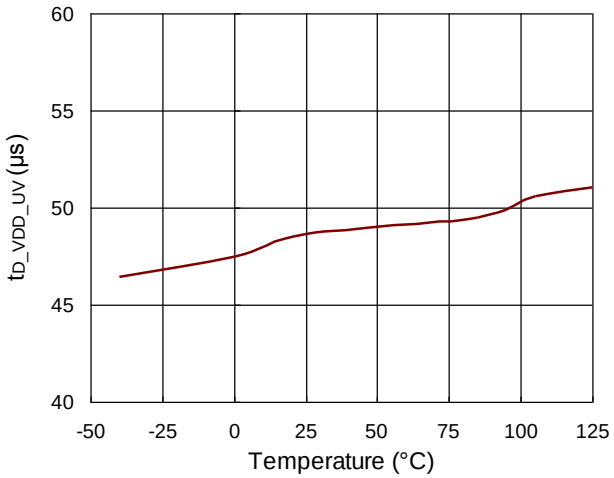
t_{D_VDDOVP} vs. Temperature



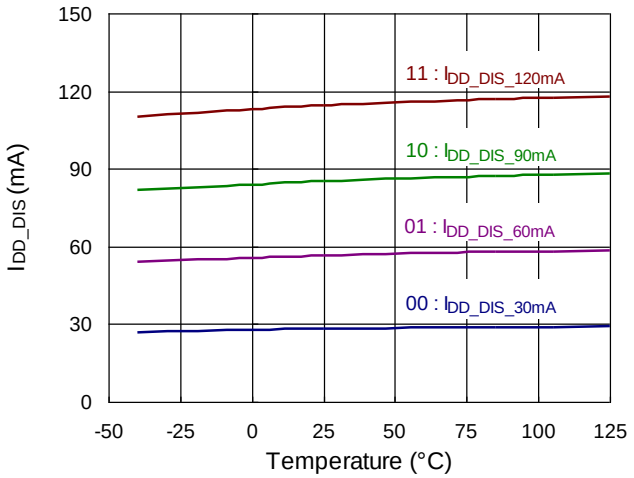
$V_{DD\_UV\_WK}$ vs. Temperature



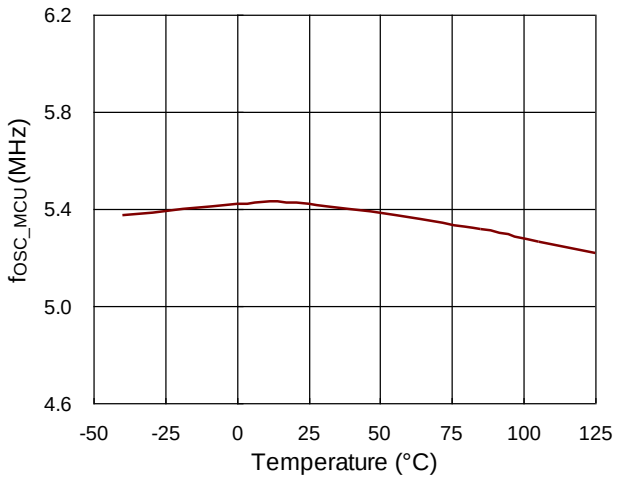
$t_{D\_VDD\_UV}$ vs. Temperature



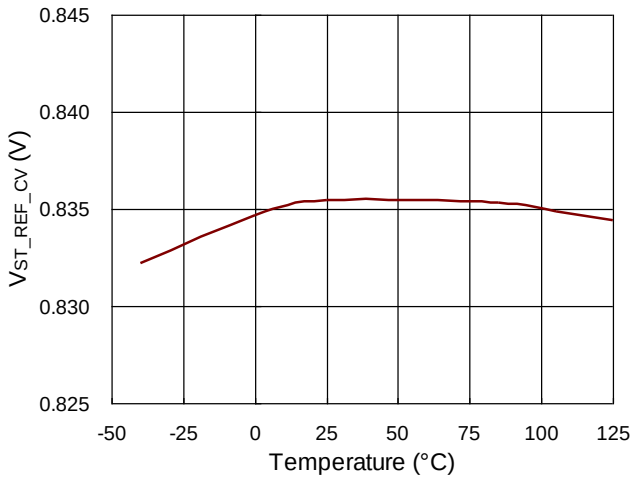
I_{DD_DIS} vs. Temperature



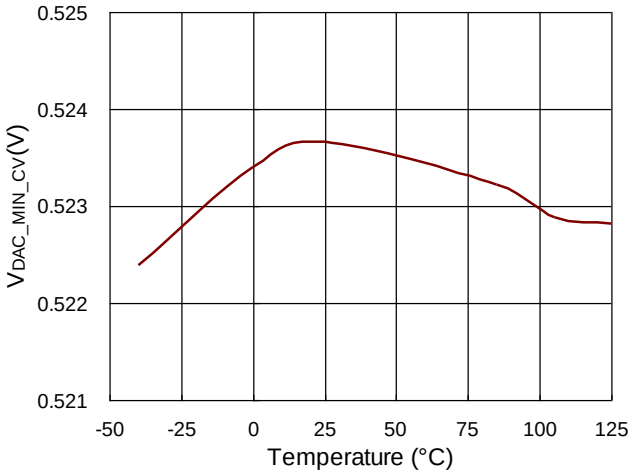
f_{OSC_MCU} vs. Temperature



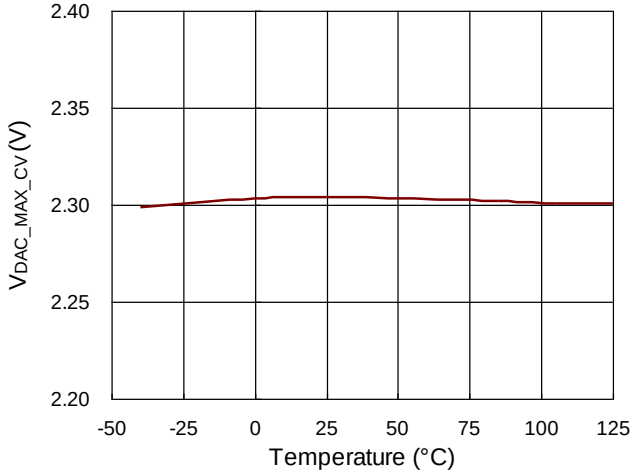
$V_{ST\_REF\_CV}$ vs. Temperature



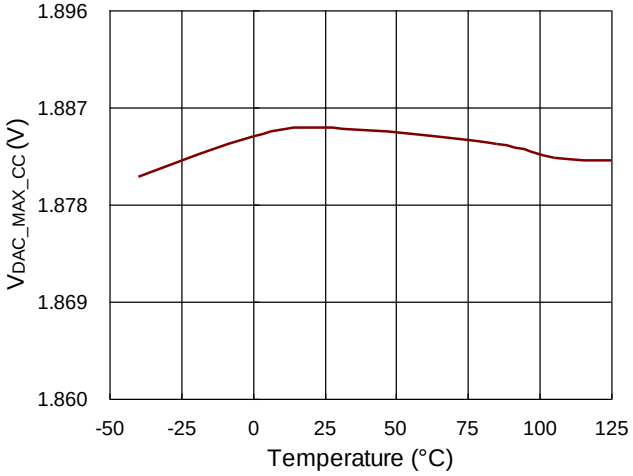
$V_{DAC\_MIN\_CV}$ vs. Temperature



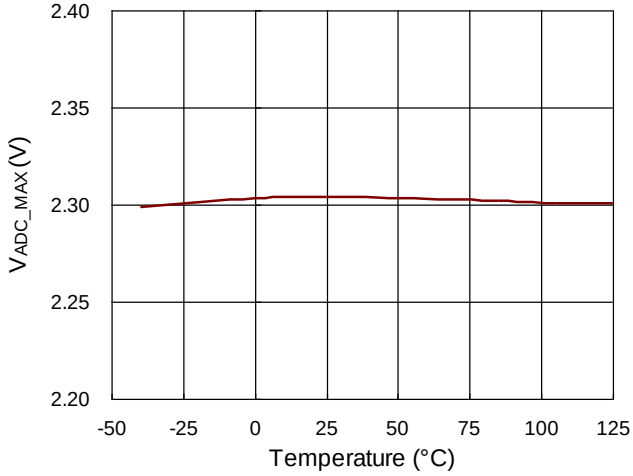
$V_{DAC\_MAX\_CV}$ vs. Temperature

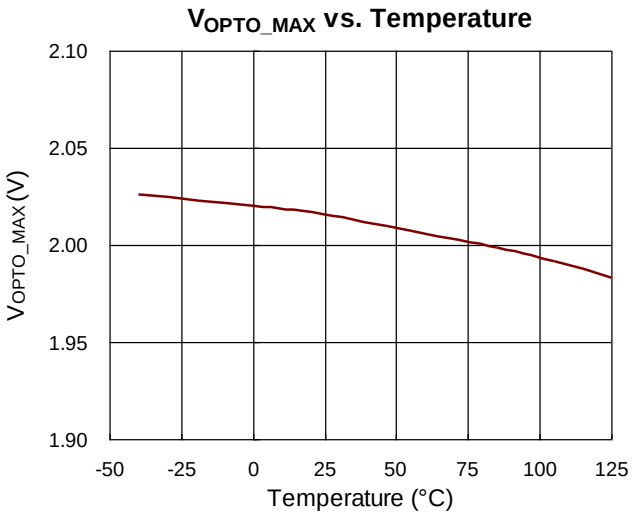


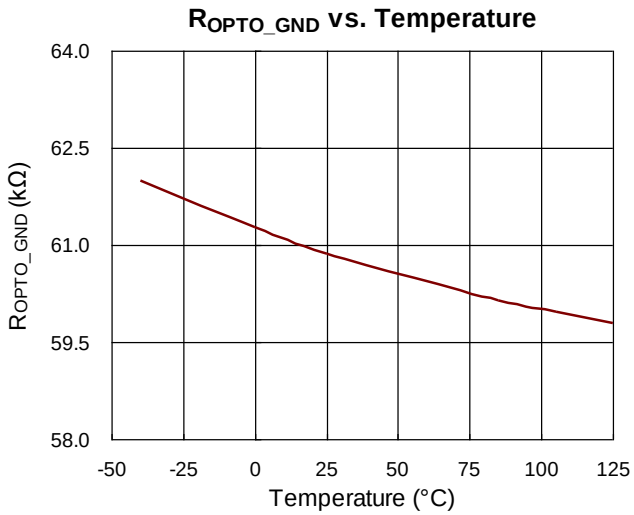
$V_{DAC\_MAX\_CC}$ vs. Temperature

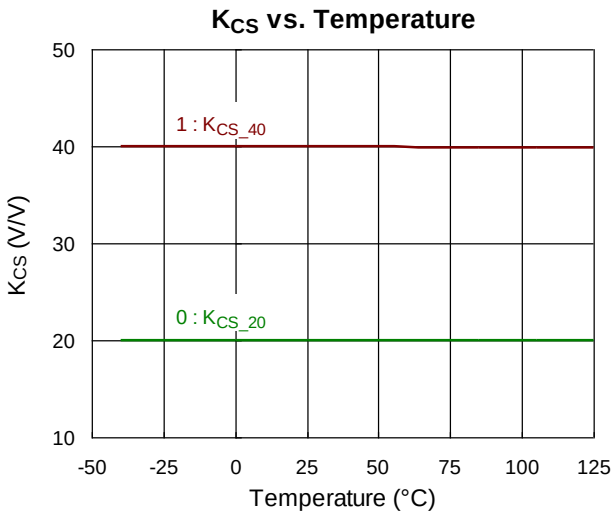


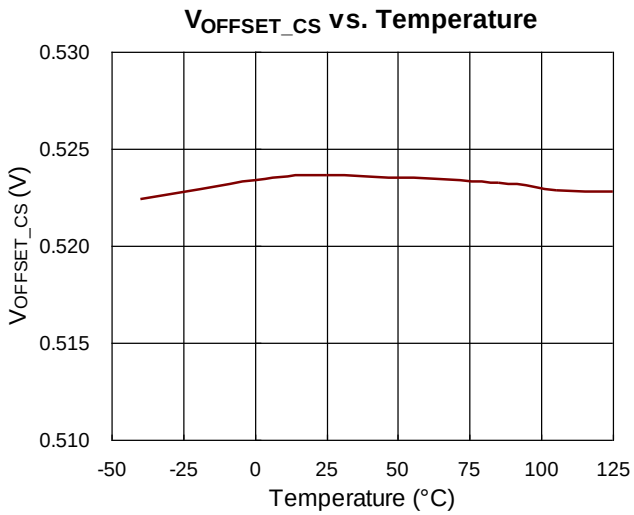
V_{ADC_MAX} vs. Temperature

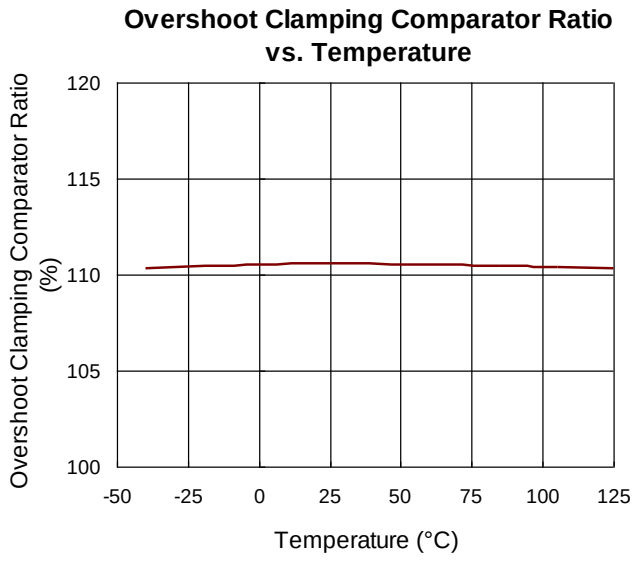


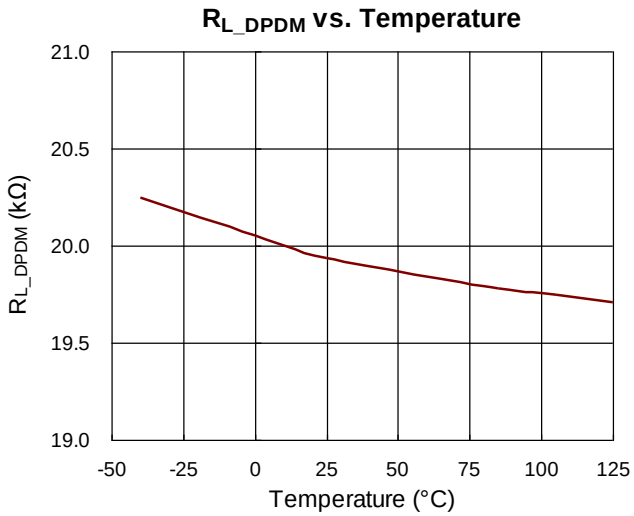




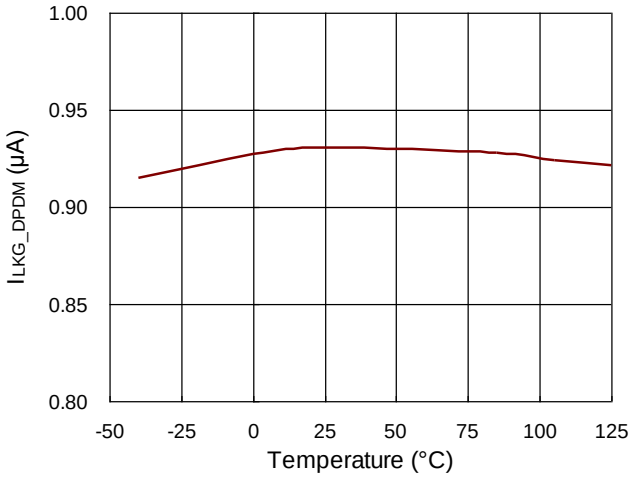




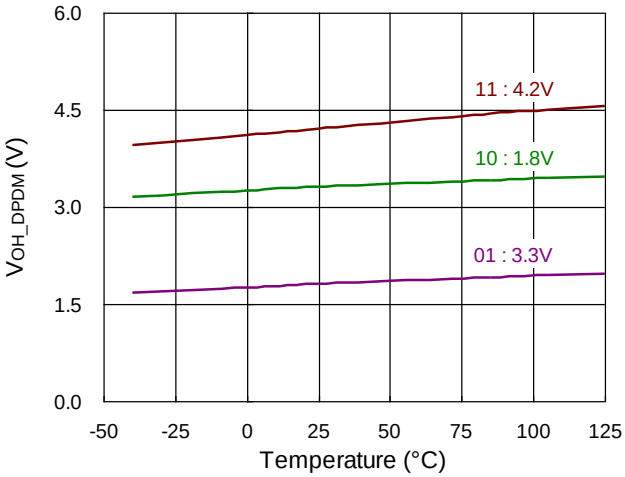




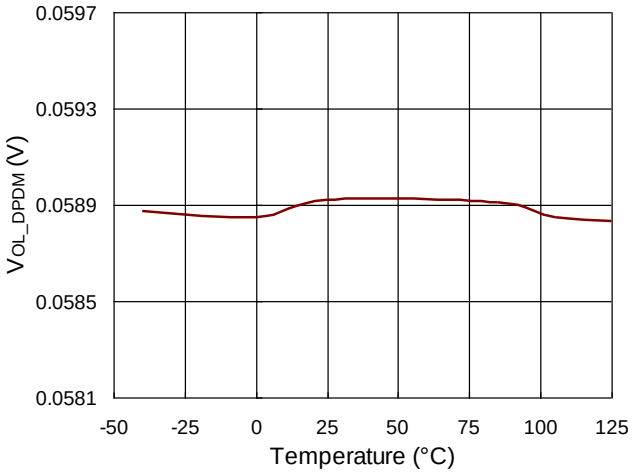
I_{LKG_DPDM} vs. Temperature



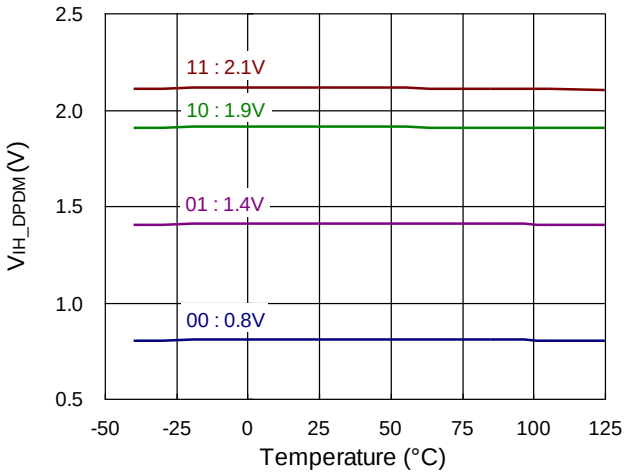
V_{OH_DPDM} vs. Temperature



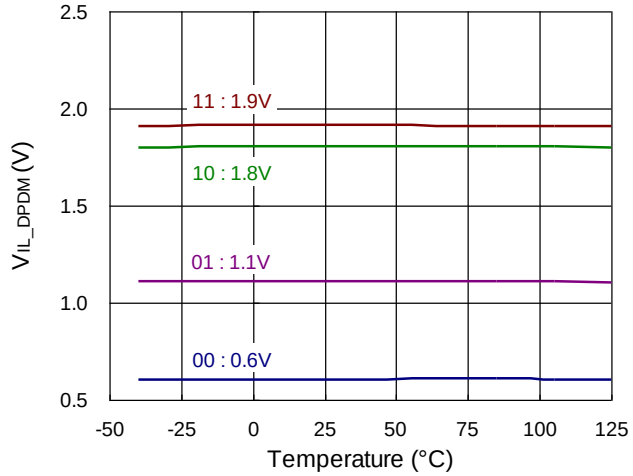
V_{OL_DPDM} vs. Temperature



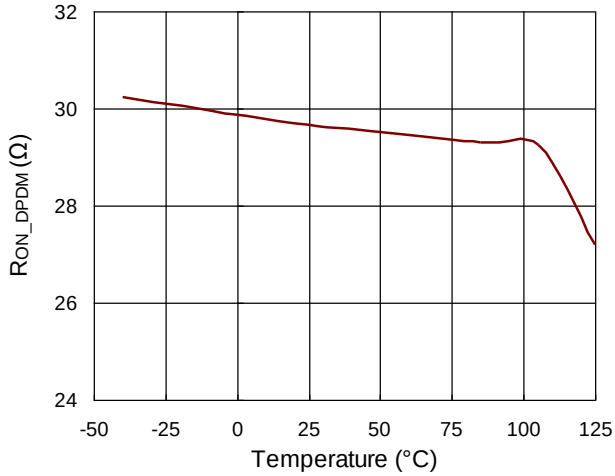
V_{IH_DPDM} vs. Temperature

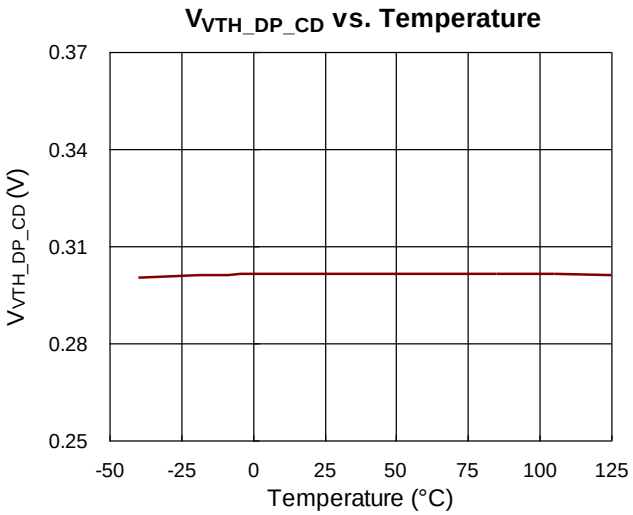


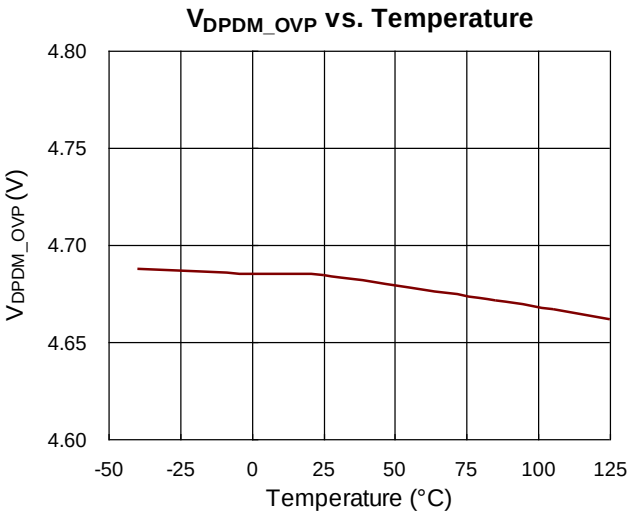
V_{IL_DPDM} vs. Temperature

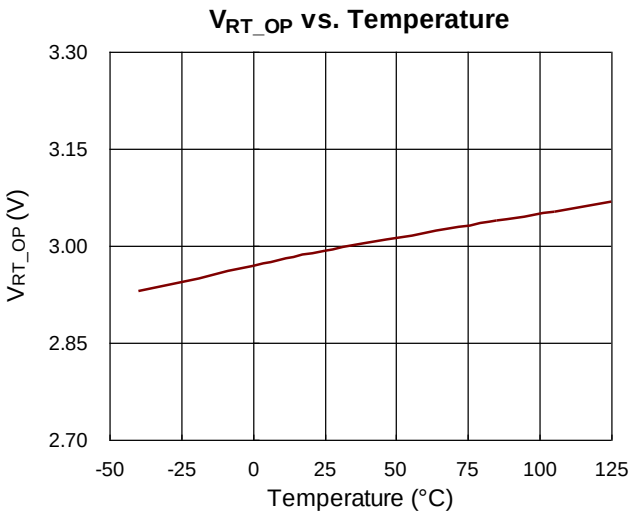


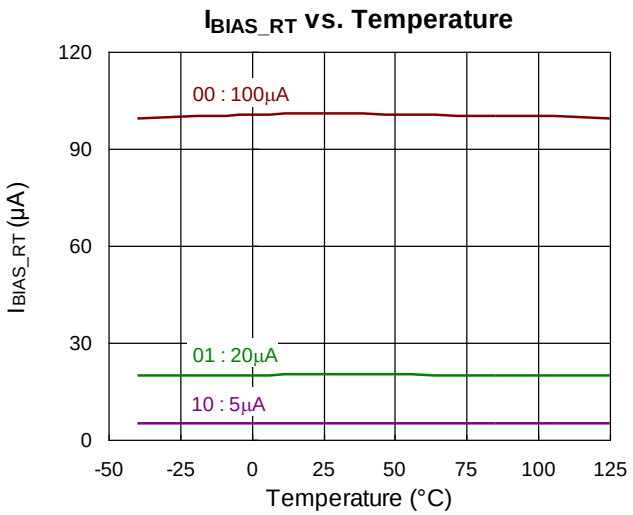
R_{ON_DPDM} vs. Temperature

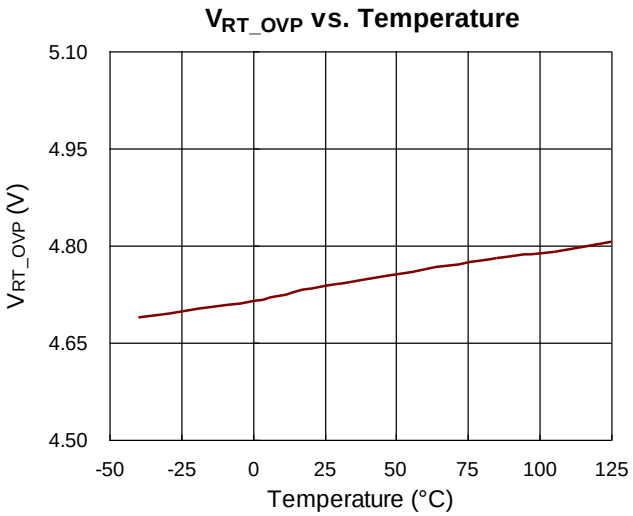


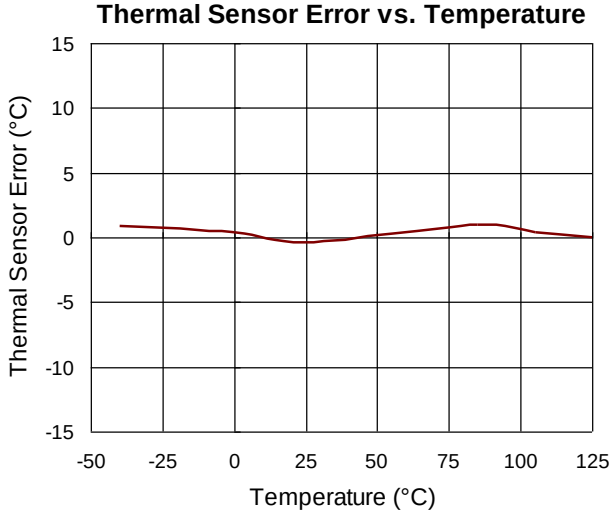












Application Information

Constant Voltage (CV) Loop

As shown in Figure 4, the RT7203V incorporates two transconductance amplifiers which are connected to feedback compensation to regulate output voltage and current, respectively. The output voltage is determined as :

$V_{OUT} = K_{FB} \times V_{REF\_CV}$

Where

$K_{FB} = (R_{FB1} + R_{FB2}) / R_{FB2} = 6$

Therefore, the V_{OUT} is determined by V_{REF_CV}, the analog output from the DAC, and its digital counterpart, which is controlled by the MCU, as shown in the Functional Block Diagram.

Constant Current (CC) Loop and Current Sense

Both the constant voltage and constant current compensation loops are connected to feedback compensation. The OPTO driver is sourced the current through an external resistor R_{OPTO} and an optocoupler, which isolates the secondary side from the primary side and then feedbacks the compensation signal to the primary side. Note that for better linearity of the loop compensation range, R_{OPTO} should be designed to cover the operation at the minimum output voltage.

$$\frac{(V_{OPTO\_MAX} - V_F)}{R_{OPTO}} \times CTR \geq I_{COMP\_MAX}$$

CTR : Current transfer ratio of the optocoupler

V_F : Forward voltage of the optocoupler

V_{OPTO_MAX} : The maximum OPTO voltage for the OPTO driver at sourcing 1mA.

I_{COMP_MAX} : The maximum COMP sourcing current of a traditional PWM controller in the primary side. It is a current sourced from an internal bias through a built-in pull-high resistor connected the COMP pin in the PWM controller.

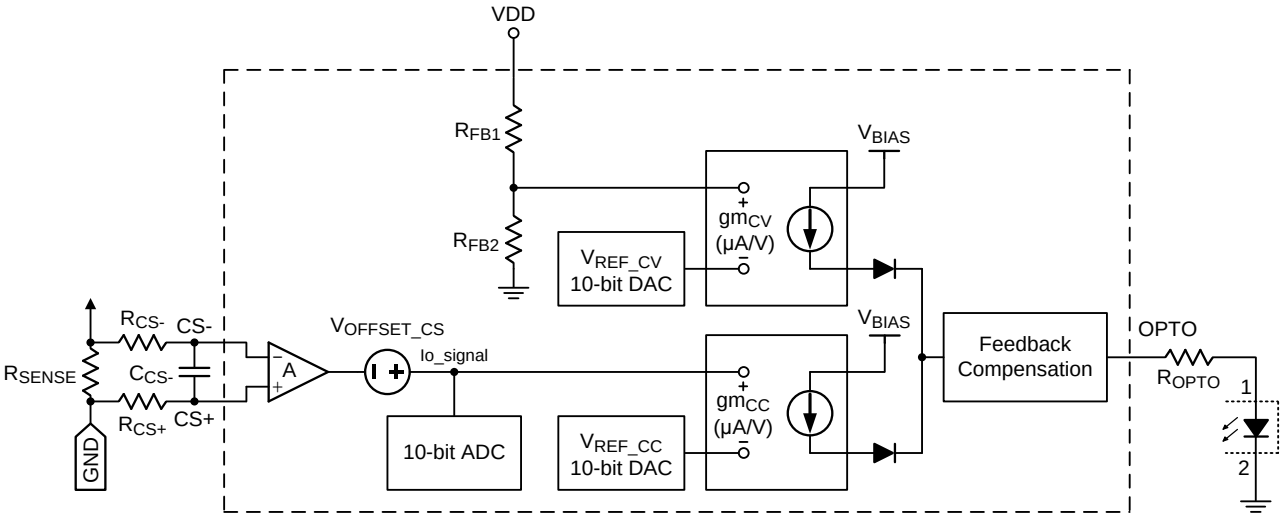


Figure 4. CV and CC Loops

Internal Feedback Compensation

The RT7203V has a built-in feedback compensator that optimizes system stability and response for different applications, and furthermore can reduce external components.

The feedback compensation design is based on the system operation mode and component parameters. An off-line flyback converter mostly uses a Type-II compensator to compensate for the feedback loop. It has a zero frequency pole, a low frequency zero and a high frequency pole. The feedback compensation design is to make the low frequency zero point of compensator to compensate the low frequency pole point of system and make the high frequency pole point to compensate the ESR zero point of output capacitor, by doing this the system can possess a better phase margin. In addition to phase margin, a proper middle gain of compensator is chosen to get the better transient response, and improve the system stability.

The RT7203V provides a simple and flexible design for the feedback compensation. The R_Z, C_Z and the middle gain of the compensator can be programmed according to different output conditions. With this feature, one can easily achieve a stable system by using this flexible design for compensation.

Power-Up Sequence

Figure 5 shows the timing diagram for the power-up sequence. When start-up, the default output voltage is set at 5V. Once a device via the proprietary protocol is attached, the UFP will deliver voltage and current settings to the RT7203V for the MCU to decode. The controller simultaneously programs reference voltages, V_{REF_CV} and V_{REF_CC}, for the CV and CC loops, respectively. Those voltages are the analog outputs converted by the DAC. If the devise via the proprietary protocol is detached and the output current is lower than the power-saving mode threshold, which is typically programmed as 200mA, the RT7203V will enter the power-saving mode, under which the RT7203V operates at an ultra-low operating current and thus the total input power can be saved. Meanwhile, if the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, or a proprietary protocol device is attached, the RT7203V will exit from the power-saving mode.

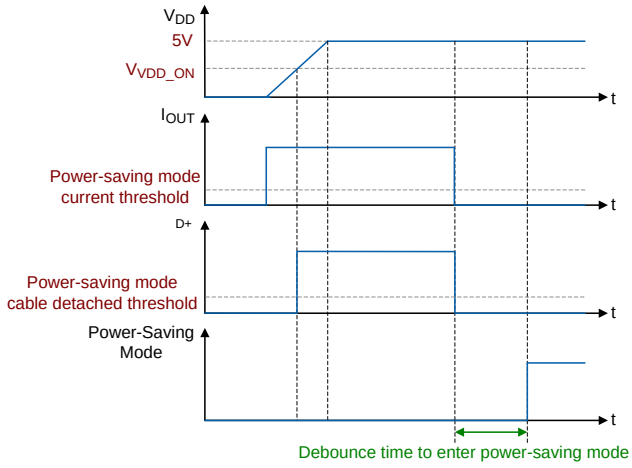
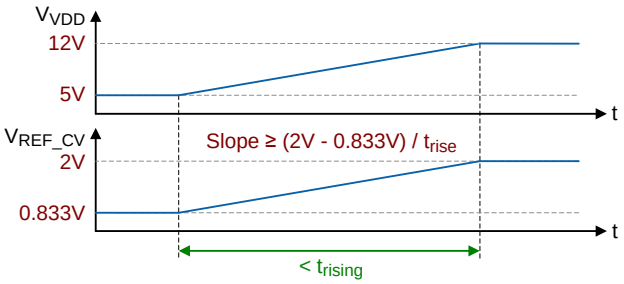


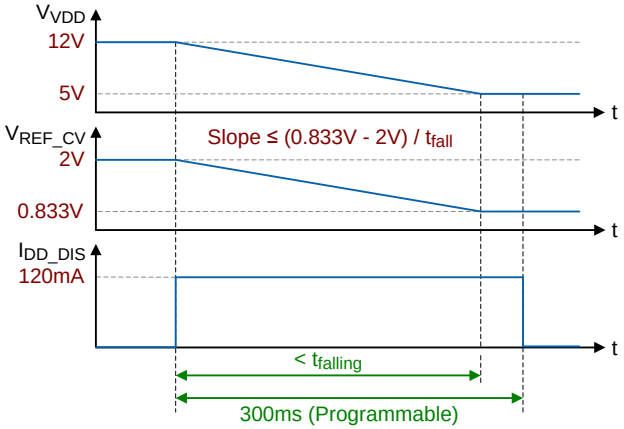
Figure 5. The Bias Voltages Sequence during Start-Up

Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of the UFP. Both the rise time and fall time of output voltages should be less than the spec. given in Figure 6.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 6. Output Voltage Transient Waveforms

The RT7203V provides a control for the discharge current from the VDD pin. This function utilizes a bleeder to help discharge of the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as VOUT from 12V to 5V. The discharge current can be programmed by the internal register according to the VDD voltage level, as shown in Figure 7.

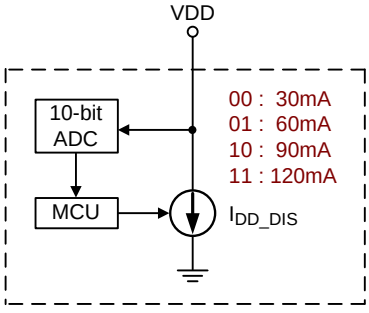


Figure 7. Discharge Current Control from VDD Pin

Output Over-Voltage Protection

As shown in the Figure 8 and Figure 9, in case the optocoupler of the feedback loop is in malfunction due to aging. If the internal voltage related to VDD is higher than the programmable threshold V_{VOUT_OVP}. The OPTO pin voltage will be latched high and the VDD discharge current function will be enabled by a period until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

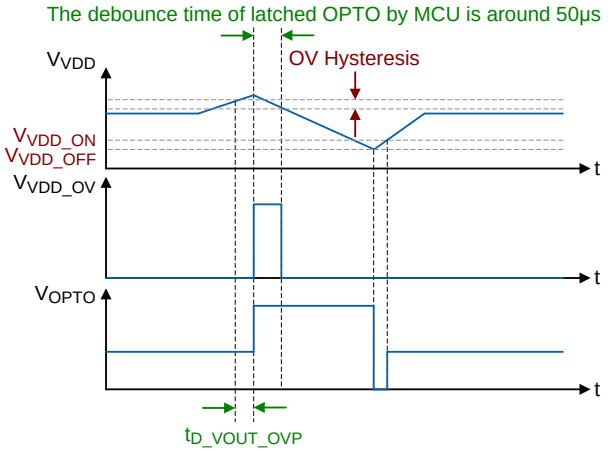


Figure 8. Timing Sequence of the OVP Function

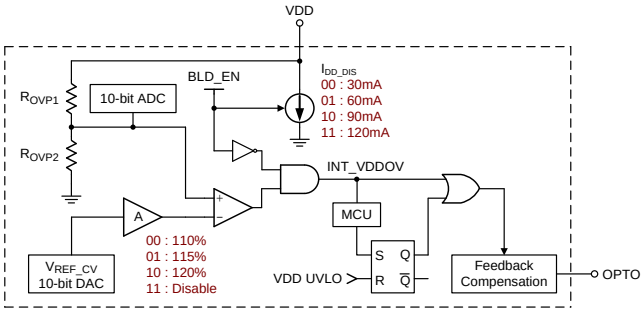


Figure 9. OVP Functional Diagram

Temperature Sensing and Thermal Protection

The RT7203V provides the RT pin for over-temperature protection or thermal monitoring. As shown in Figure 2, the RT pin sources a constant bias current for the remote thermal sensor of a NTC thermistor, connected from the RT pin to GND for temperature sensing. If the RT voltage is lower than the programmable threshold voltage and the condition sustains for a programmable deglitch time, the over-temperature protection can then be activated and triggered.

The bias current through the RT pin can be programmed as 100μA, 20μA, or 5μA by setting the internal register. With an appropriate bias current setting, linearity of temperature sensing over the temperature range of 25°C to 100°C can be significantly improved. In addition, the RT7203V can deliver the sensed RT voltage data back to the UFP via the protocol (Vendor Defined Message), if necessary. Figure 10 shows the RT voltages vary with temperature at three different bias currents, using the NTC thermistor TTC104 as an example.

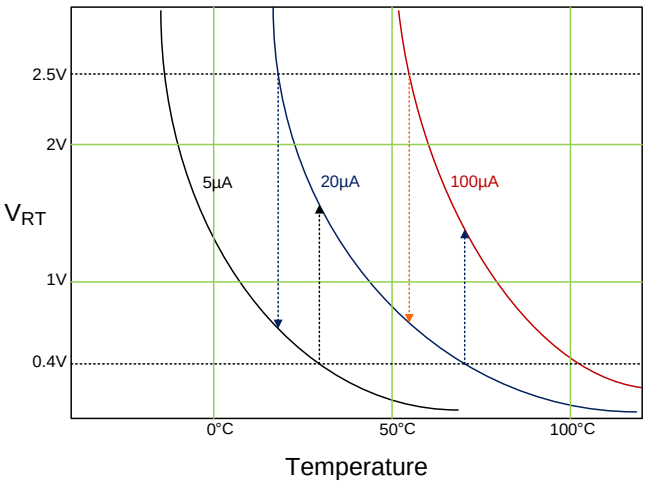


Figure 10. The RT Voltages vs. Temperature at Three Bias Currents

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction to ambient thermal resistance, θ_{JA}, is highly package dependent.

For a SOP-8 package, the thermal resistance, θ_{JA}, is 261.1°C/W on a standard JEDEC 51-3 low effective thermal conductivity single layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C - 25°C) / (261.1°C/W) = 0.38W for a SOP-8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 11 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

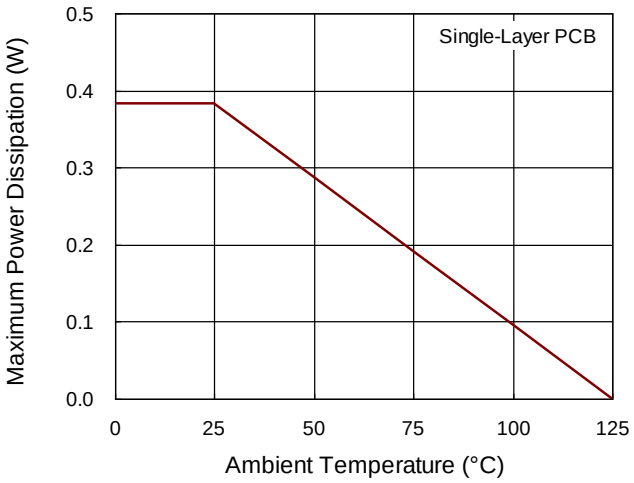
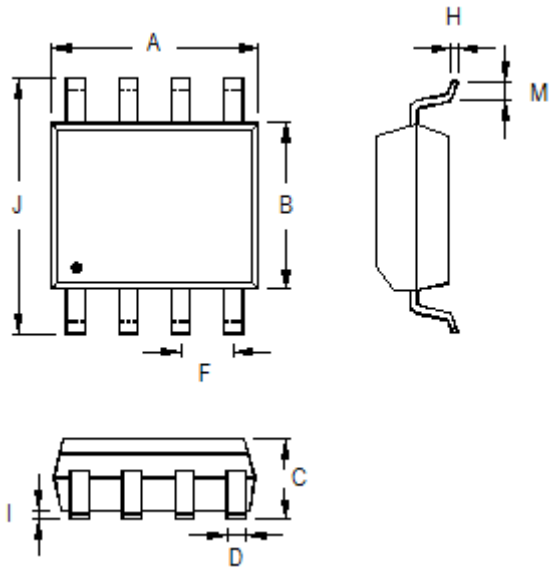


Figure 11. Derating Curve of Maximum Power Dissipation

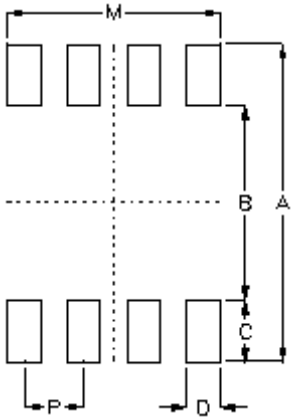
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-8/SOP-8(FC)	8	1.27	6.80	4.20	1.30	0.70	4.51	±0.10

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789