RICHTEK®

RT7202KNL

Highly-Integrated USB Type-C Power Delivery Controller with Built-In N-MOSFET Driver

1 General Description

The RT7202KNL is a USB Type-C Power Delivery (PD) controller, that mainly utilized in the secondary side for off-line AC-DC power converters. Through the high integration of control regulators and built-in N-MOSFET driver, more compact designs are easily implemented. The embedded MCU solution and Bi-phase Mark Coding (BMC) Transmitter are incorporated to handle PD protocol. Furthermore, the digital-to-analog (DAC) and analog-to-digital (ADC) converters are introduced to achieve high-precision control in various applications.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

2 Ordering Information

RT7202KNL□□-□

- Programmed Firmware Code AABBX
  - AA: Application Code
  - BB: Model Code
  - X: Customer Approved Version Code
- Package Type(1)
  - S: SOP-10
- Lead Plating System(2)
  - G: Richtek Green Policy Compliant

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **Protocol Support**
  - **USB PD3.0 and PPS**
- **High Integration**
  - **Wide Operating Range from 3.3V to 21V**
  - **Built-In Shunt Regulator for Constant-Voltage and Constant-Current Regulations**
  - **Built-In N-MOSFET Driver**
  - **Built-In Quick Discharge in VDD and USBP**
  - **Built-In VCONN Power and Switch**
  - **Linear Cable Compensation**
  - **Power Saving Mode Supported**
  - **Embedded MCU with 16kB OTP-ROM**
  - **Embedded BMC Transmitter**
- **Protection**
  - **VDD Adaptive Overvoltage Protection (OVP)**
  - **VDD Adaptive Undervoltage Protection (UVP)**
  - **USBP Undervoltage Protection (USBP UVP)**
  - **CC1/CC2 Overvoltage Protection (IO OVP)**
  - **Overcurrent Protection (OCP)**
  - **Over-Temperature Protection (OTP)**

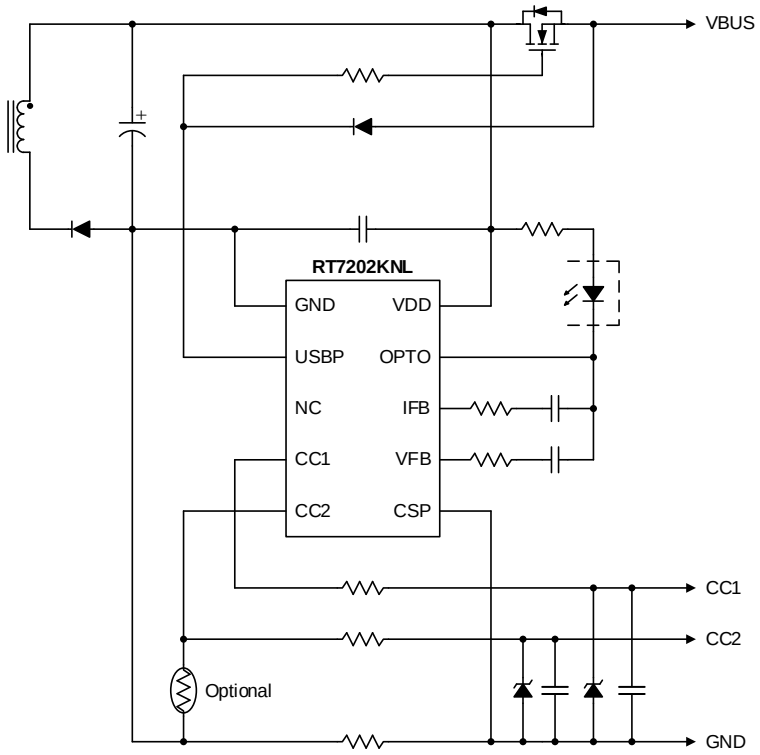
4 Applications

- USB Type-C PD Controller in Source Application for Chargers/Adapters of Smartphone, Tablet, Notebook, and Other Electronics

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit



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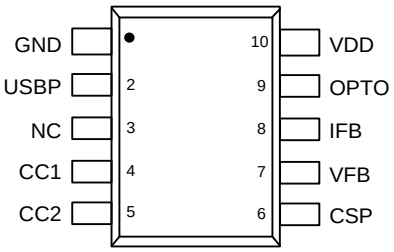
7 Pin Configuration

(TOP VIEW)



SOP-10

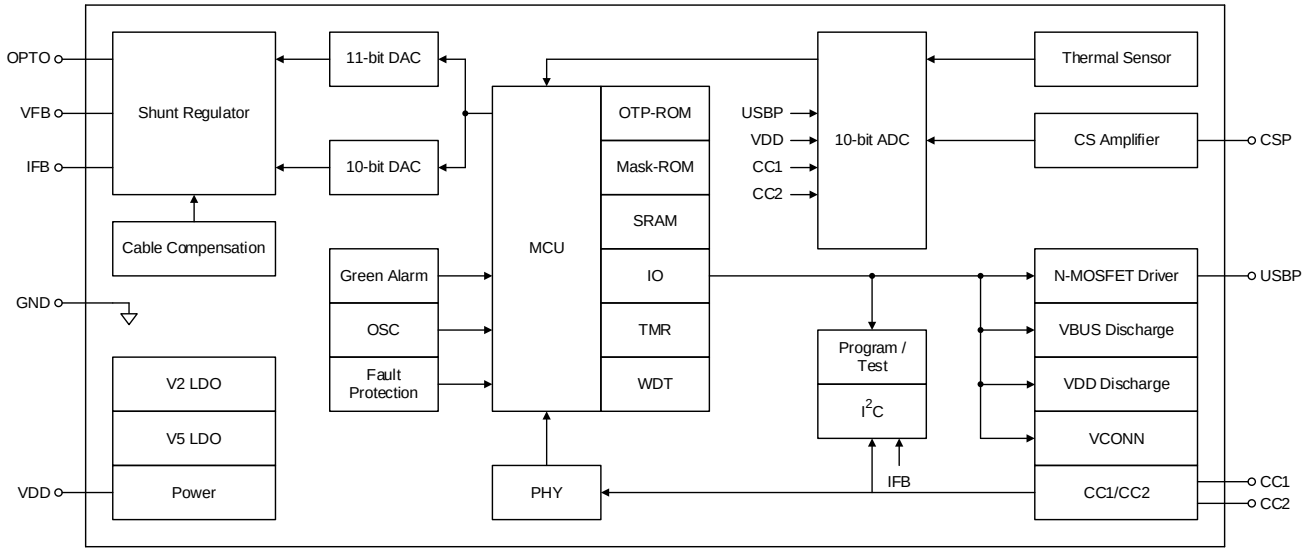
8 Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	GND	GND	Ground.
2	USBP	A/D IO	Control signal for Gate terminal of blocking N-MOSFET.
3	NC	--	No internal connection.
4	CC1	A/D IO	Type-C connector Configuration Channel 1, used to detect cable-plug event, determine the cable orientation, and supply VCONN power. Can be configured as ADC input.
5	CC2	A/D IO	Type-C connector Configuration Channel 2, used to detect cable-plug event, determine the cable orientation, and supply VCONN power. Can be configured as ADC input.
6	CSP	AI	Positive input of current-sense amplifier for sensing output current.
7	VFB	AI	Feedback input for constant-voltage loop.
8	IFB	AI	Feedback input for constant-current loop.
9	OPTO	A/D IO	Current-sink output connected to optocoupler. Can be configured as open-drain output.
10	VDD	PWR	Supply input voltage

8.1 IO Type Definition

- PWR: Power Pin
- GND: Ground Pin
- AI: Analog Input Pin
- A/D IO: Analog/Digital Input/Output Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VDD, OPTO to GND ---------- –0.3V to 28V
- USBP to GND ---------- –0.3V to 32V
- VFB, IFB, CC1, CC2, CSP to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  SOP-10 ---------- 0.51W
- Package Thermal Resistance (Note 3)

  SOP-10, θ_{JA} ---------- 194.2°C/W

  SOP-10, θ_{JC} ---------- 36.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the bottom of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD ---------- 3.3V to 21V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.8	2.85	2.9	V
VDD Start-Up Current	I_{VDD_START}	V_{DD} = 2.8V	50	100	150	μA
VDD Nominal Current	I_{VDD_NOM}	V_{DD} = 5V	2.81	3.81	4.81	mA
VDD Idle-Mode Current	I_{VDD_IDLE}	V_{DD} = 5V	0.81	1.31	1.81	mA
VDD Green-Mode Current	I_{VDD_GREEN}	V_{DD} = 5V	310	460	610	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Maximum Overvoltage Protection Threshold	V_{VDD_MAXOVP}		23	24	25	V
VDD Adaptive Overvoltage Protection Threshold	V_{VDD_OVP}	(Enable/Disable) (Note 6)	105	110	115	%
			110	115	120	
			115	120	125	
VDD Overvoltage Protection Deglitch	t_{VDD_OVP}	(Note 7)	25	30	35	µs
VDD Adaptive Undervoltage Protection Threshold	V_{VDD_UVP}	(Enable/Disable) (Note 6)	80	85	90	%
			85	90	95	
VDD Undervoltage Protection Deglitch	t_{VDD_UVP}	(Note 7)	30	50	70	µs
VDD Threshold for CC1/CC2 Overvoltage Protection	V_{VDD_IOOVP}		5.75	6	6.25	V
VDD Constant-Discharge Current	I_{DIS_VDD}	V_{DD} > 3.3V (Note 6)	63	90	117	mA
			84	120	156	
			120	150	180	
			150	180	210	
VFB/IFB/OPTO Regulator Section						
VFB Resistor Divider for Voltage Feedback	R_{VFB}	R_{VFB} = R_{VFB1} + R_{VFB2} R_{VFB1}: VDD to VFB R_{VFB2}: VFB to GND	294	420	546	kΩ
VFB Resistor Divider Scaling Factor for Voltage Feedback	K_{VFB}		9.9	10	10.1	--
Standby Reference Voltage for CV Regulator	$V_{REF\_CV\_ST}$		0.485	0.5	0.515	V
Typical Reference Voltage from DAC for CV Regulator	V_{REF_CV}		0.152	--	2.2	V
Typical Reference Voltage from DAC for CC Regulator	V_{REF_CC}	V_{DD} > 3.3V	0	--	1.5	V
Ratio of Change in Reference Voltage to Change in OPTO Voltage	$\Delta V_{REF}/\Delta V_{OPTO}$	V_{OPTO} = 25V to V_{REF} (Note 7)	–2.4	–1.2	–0.1	mV/V
OPTO Dynamic Impedance	$\lvert Z_{OPTO} \rvert$	V_{OPTO} = V_{REF}, I_{OPTO} = 1mA, f < 1kHz (Note 7)	0.1	0.22	0.5	Ω
OPTO Turn-On Sinking Current Capability	I_{OPTO_ON}	V_{DD} = 5V, V_{OPTO} = 3V (Note 7)	0	--	120	mA
OPTO Turn-On Impedance	R_{OPTO_ON}	I_{OPTO} = 20mA	1	--	200	Ω
OPTO Pull-Up Impedance	R_{p_OPTO}	OPTO shorted to VDD (Enable/Disable)	1	--	200	Ω
OPTO Pull-Down Impedance	R_{d_OPTO}	OPTO shorted to GND (Enable/Disable)	1	--	200	Ω

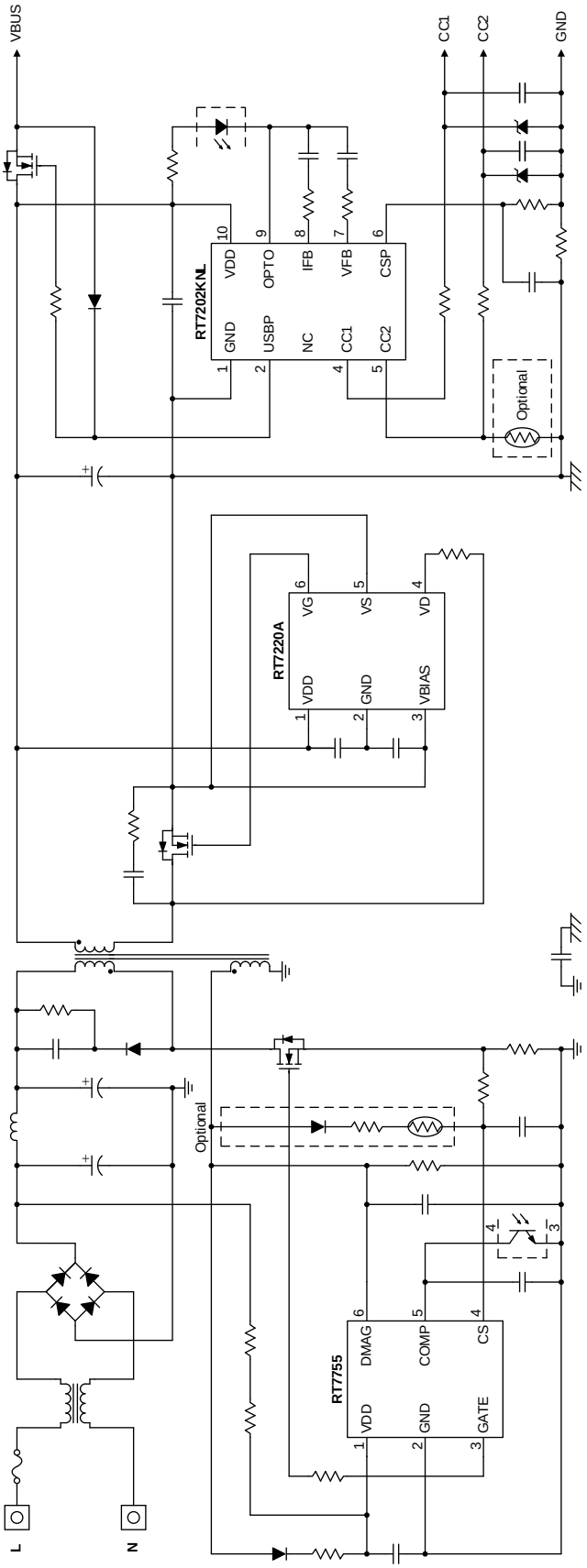
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CSP Section						
Current-Sense Amplifier Gain	K_{CS}	(Note 6)	19.8	20	20.2	V/V
			29.7	30	30.3	
Current-Sense Amplifier Output Offset Voltage	V_{CS_OFFSET}		0.36	0.4	0.44	V
Current-Sense Amplifier Unit Gain Bandwidth		(Note 7)	1000	--	5000	kHz
Current-Sense Amplifier Output Threshold for Exit Power-Saving Mode	$V_{CS\_PSM\_EX}$	$V_{CS\_PSM\_EX} = V_{CSP} \times K_{CS} + V_{CS\_OFFSET}$ (Enable/Disable) (Note 6)	0.41	0.45	0.49	V
			0.51	0.55	0.59	
Cable-Compensation Resistance	R_{CABLE_COMP}	(Enable/Disable) (Note 6)	40	50	60	mΩ
			65	75	85	
			90	100	110	
			105	125	145	
			130	150	170	
			180	200	220	
			230	250	270	
Cable-Compensation Transconductance Amplifier Bandwidth		(Note 7)	20	--	65	kHz
CC1/CC2 Section						
CC1/CC2 Open-Circuit Voltage	V_{CC_OC}	V_{DD} > 5V	2.9	3.25	3.6	V
CC1/CC2 Leakage Current	I_{CC_LK}	V_{DD} = 0V, V_{CC} = 5V	0	--	0.2	μA
CC1/CC2 Cable-Detached Threshold	V_{CC_CD}		2.5	2.6	2.7	V
CC1/CC2 Overvoltage Protection Threshold	V_{CC_OVP}	(Note 6)	4.2	4.35	4.5	V
			3.85	4	4.15	
CC1/CC2 Overvoltage Protection Debounce	t_{CC_OVP}	(Note 6) (Note 7)	0.095	0.1	0.105	ms
			0.95	1	1.05	
CC1/CC2 Sourcing Current Source	I_{SRC_CC}	V_{DD} > V_{DD_ON} (Enable/Disable) (Note 6)	76	80	84	μA
			171	180	189	
			304	330	356	
CC1/CC2 BMC Transmitter Tx Output-High Voltage	V_{OH_CC}		1.05	1.125	1.2	V
CC1/CC2 BMC Transmitter Tx Output-Low Voltage	V_{OL_CC}		0	0.0375	0.075	V
CC1/CC2 BMC Transmitter Tx Rise Time	t_{RISE_CC}	C_{LOAD} < 470pF	300	--	700	ns
CC1/CC2 BMC Transmitter Tx Fall Time	t_{FALL_CC}	C_{LOAD} < 470pF	300	--	700	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CC1/CC2 BMC Transmitter Rx Input-High Voltage	V_{IH_CC}	(Note 6)	0.8	0.9	1	V
			0.7	0.8	0.9	
			0.6	0.7	0.8	
			0.5	0.6	0.7	
CC1/CC2 BMC Transmitter Rx Input-Low Voltage	V_{IL_CC}	(Note 6)	V_{IH_CC} - 0.1	V_{IH_CC} - 0.1	V_{IH_CC} - 0.1	V
CC1/CC2 VCONN Voltage	V_{CONN}	V_{DD} = 5V, I_{VCONN} = 0mA	3.8	4	4.2	V
		V_{DD} = 5V, I_{VCONN} = 30mA	3.3	--	3.5	
CC1/CC2 VCONN Short-Circuit Current	I_{VCONN_SC}		45	70	95	mA
USBP Section						
USBP Undervoltage Protection Threshold	V_{USBP_UVP}		V_{DD} + 4	V_{DD} + 4.5	V_{DD} + 5	V
USBP Undervoltage Protection Deglitch	t_{USBP_UVP}	(Note 7)	30	50	70	µs
USBP Undervoltage Protection Masking Time	$t_{USBP\_UVP\_MASK}$	Masking time for USBP UVP after N-MOSFET driver on (Note 7)	45	50	55	ms
USBP Output-High Voltage	V_{OH_USBP}	R_{LOAD} = 10MΩ	V_{DD} + 7	V_{DD} + 8.5	V_{DD} + 10	V
		R_{LOAD} = 1MΩ	V_{DD} + 5	--	V_{DD} + 10	
USBP Maximum Output-High Voltage	$V_{OH\_USBP\_MAX}$		30	31	32	V
USBP Output-Low Voltage	V_{OL_USBP}	(Note 7)	0.1	0.5	1	V
USBP Output-High Impedance	R_{OH_USBP}	(Note 7)	10	--	1000	MΩ
USBP Output-Low Impedance	R_{OL_USBP}	(Note 6)	350	500	650	Ω
		(Note 7)	1.89	2.7	3.55	kΩ
		V_{DD} < V_{VDD_OFF} (Note 7)	3.08	4.4	5.72	kΩ
Accuracy Section						
Voltage Regulation Accuracy	E_{VOUT}	V_{OUT} = 3.3V to 21V, I_{OUT} = 1A to 5A	–100	--	100	mV
Current Regulation Accuracy	E_{IOUT}	V_{OUT} = 3.3V to 21V, I_{OUT} = 1A to 5A, R_{CS} = 1% accuracy	–150	--	150	mA
Internal Thermal Sensor Accuracy	E_{TS}	T_C = –40°C to 105°C	–7	--	7	°C

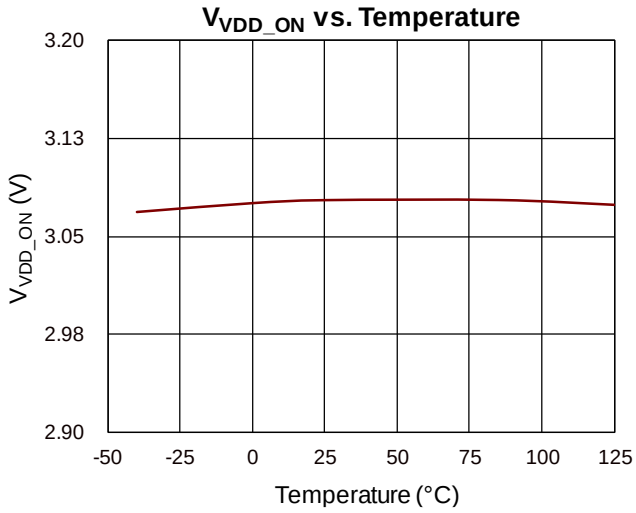
Note 6. Register option by OTP program.

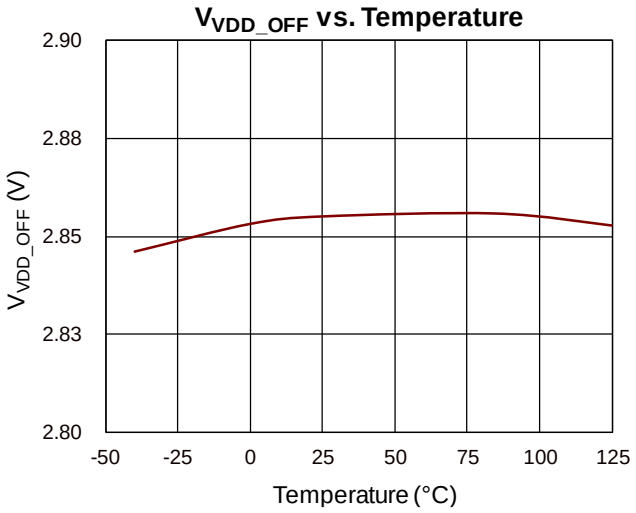
Note 7. Guaranteed by design.

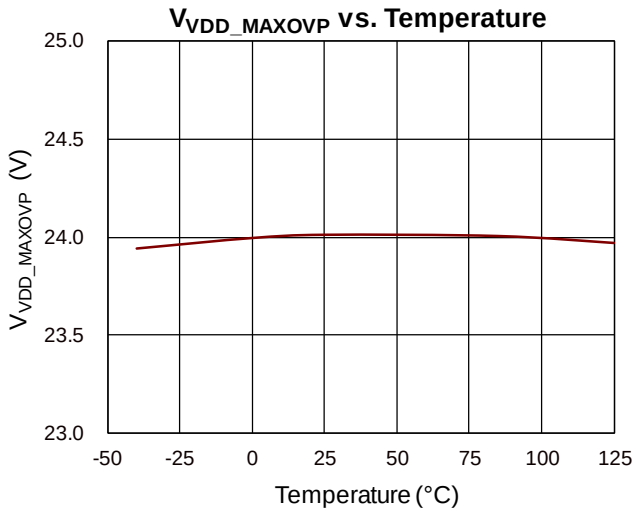
13 Typical Application Circuit

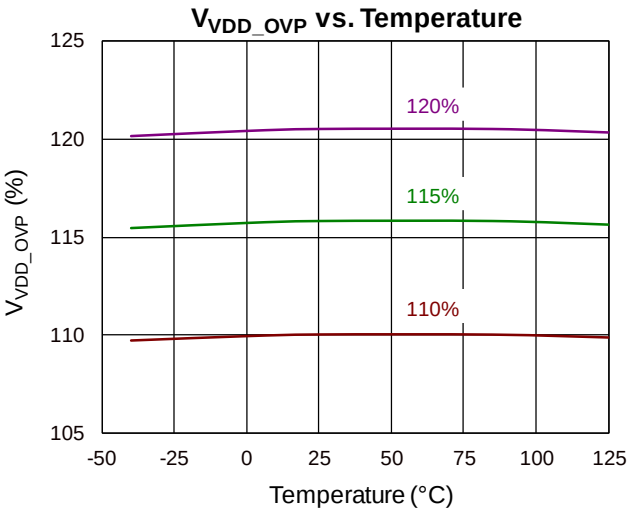


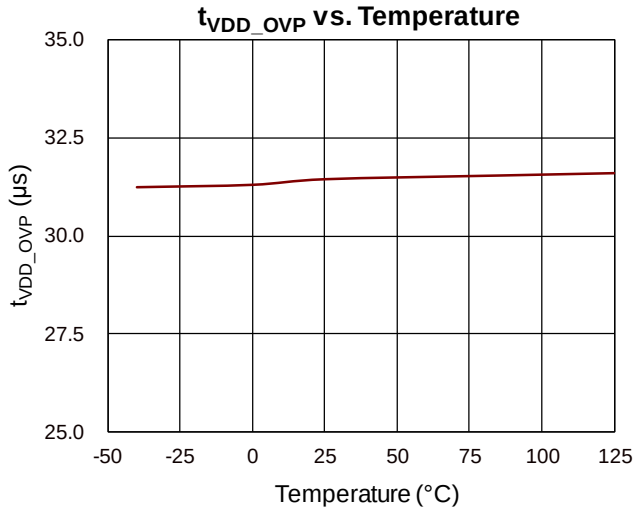
14 Typical Operating Characteristics

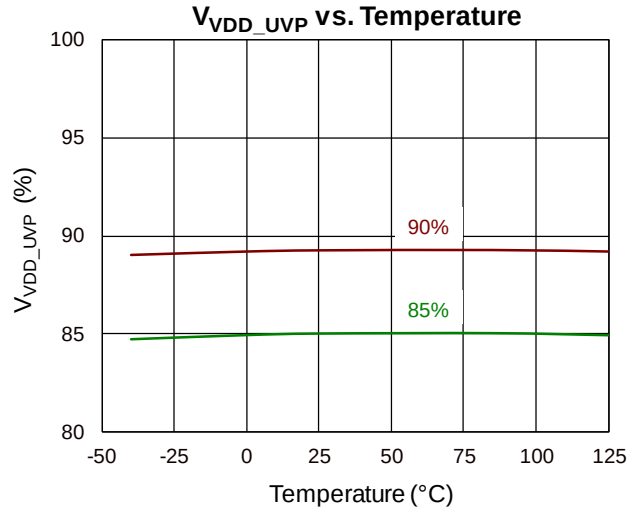


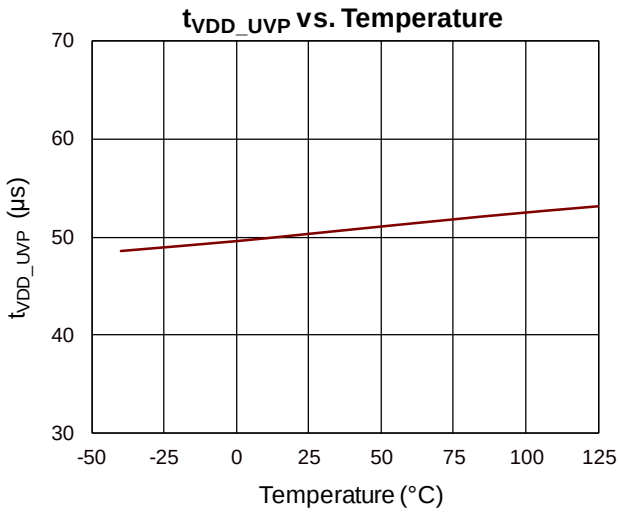


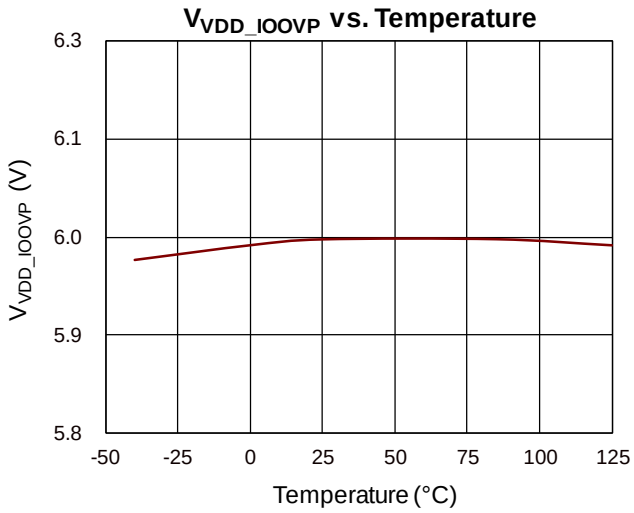


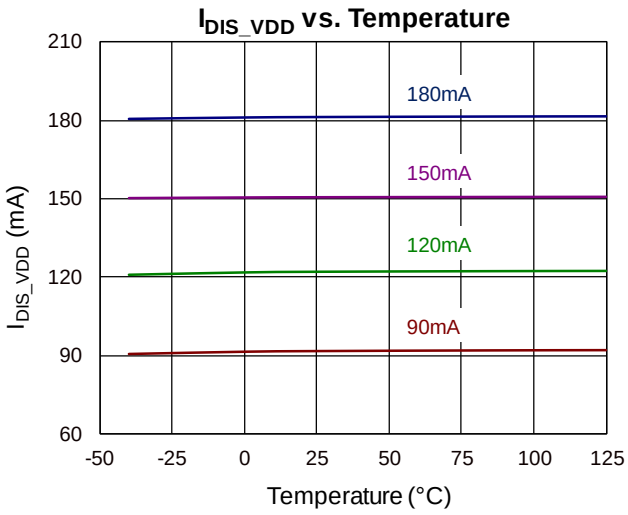


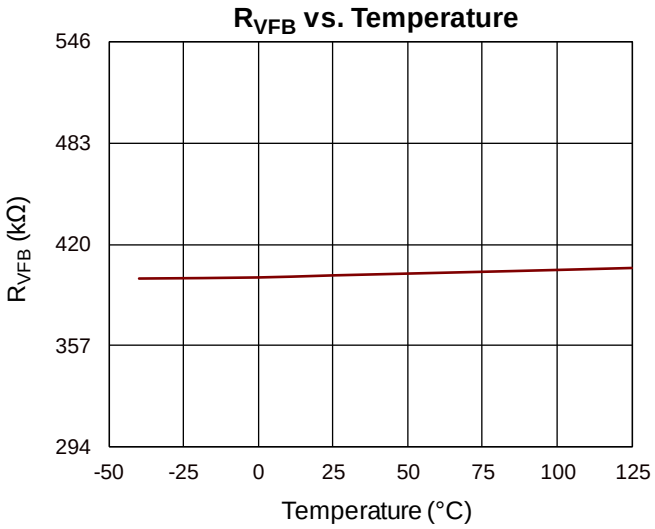


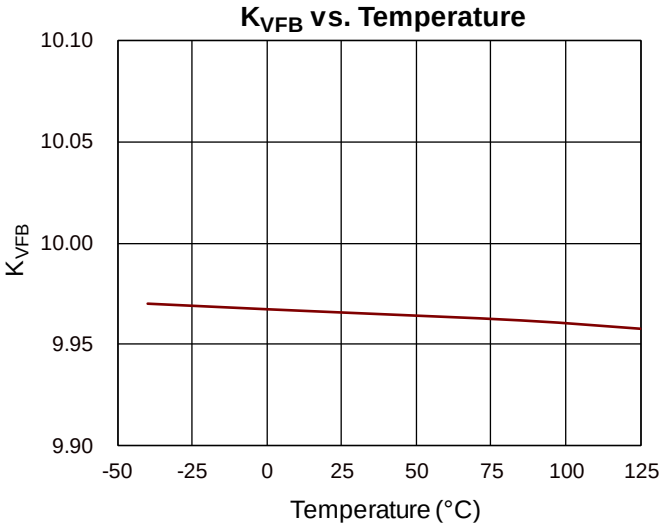


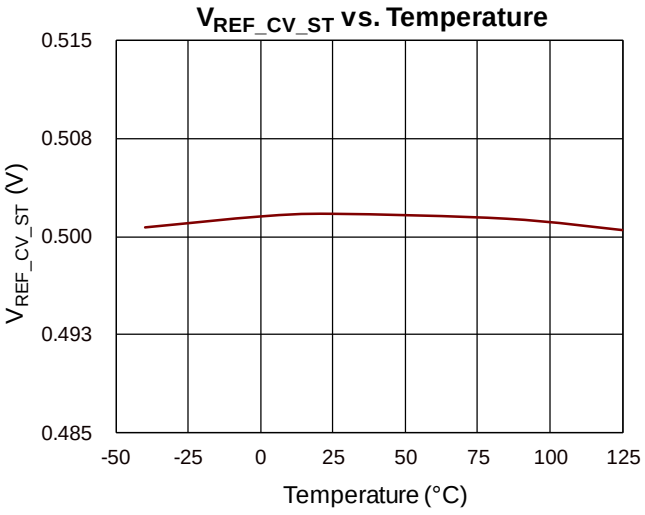


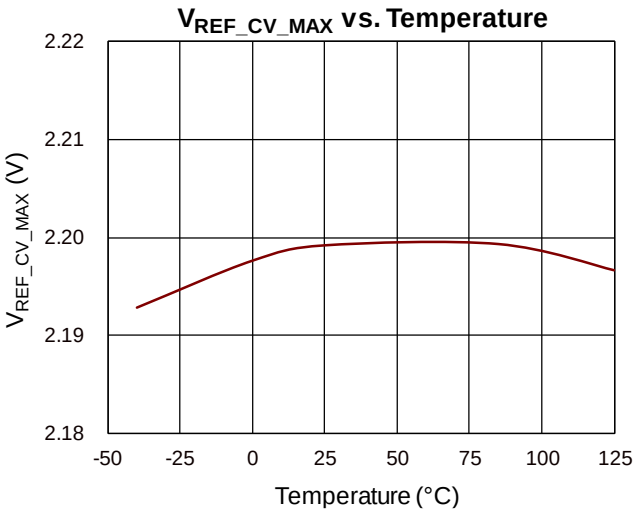


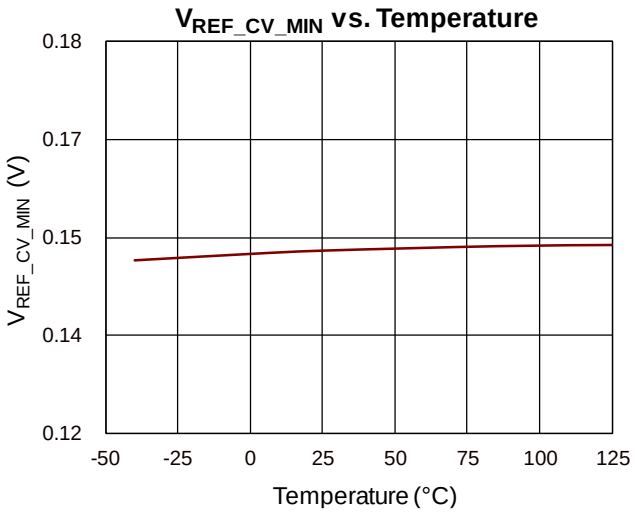


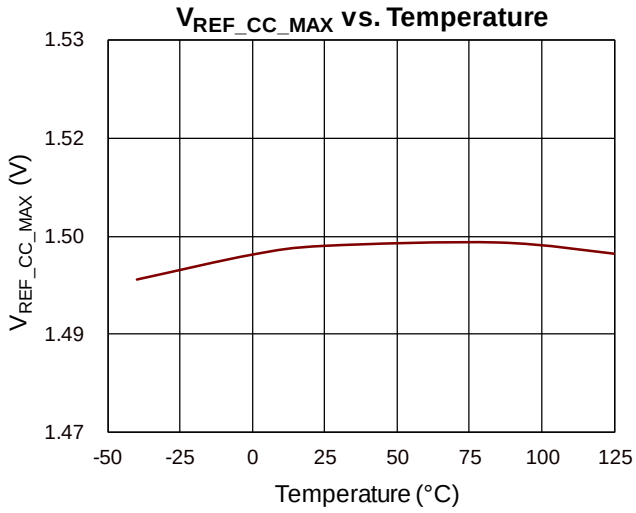


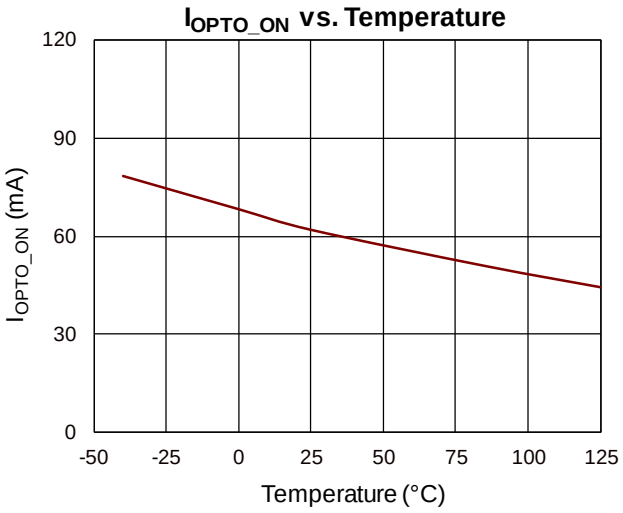


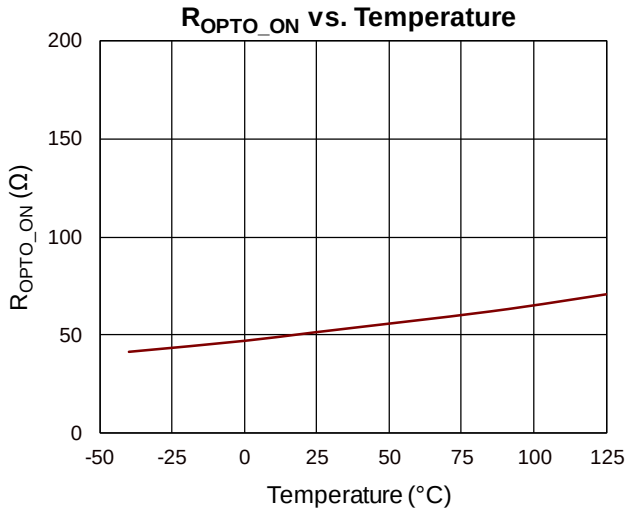


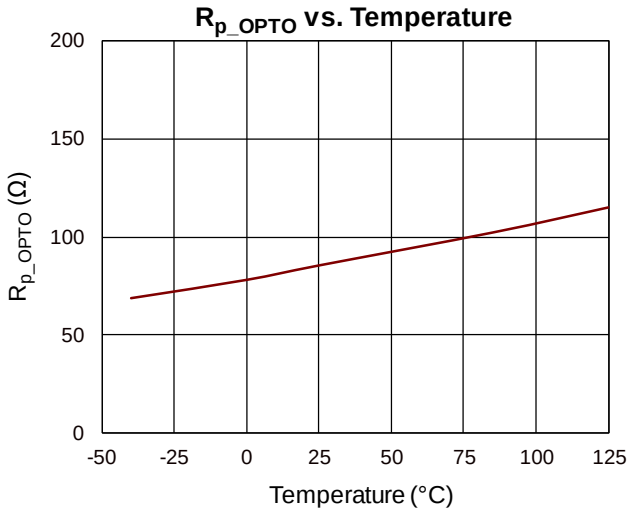


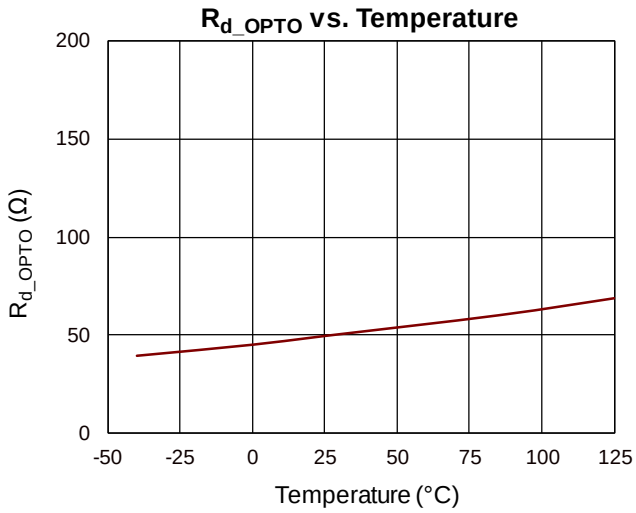


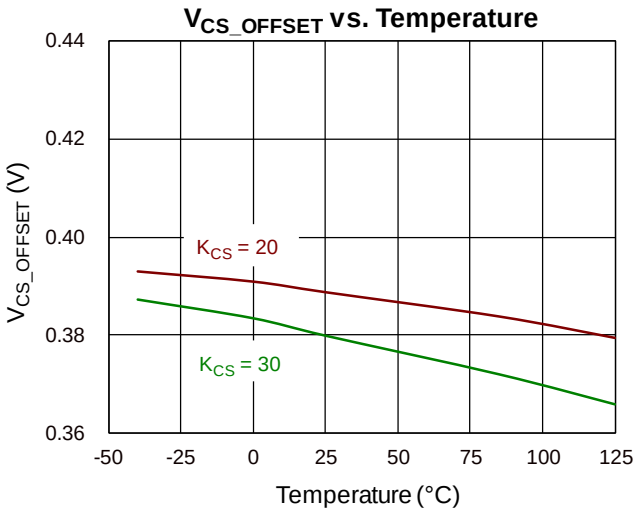


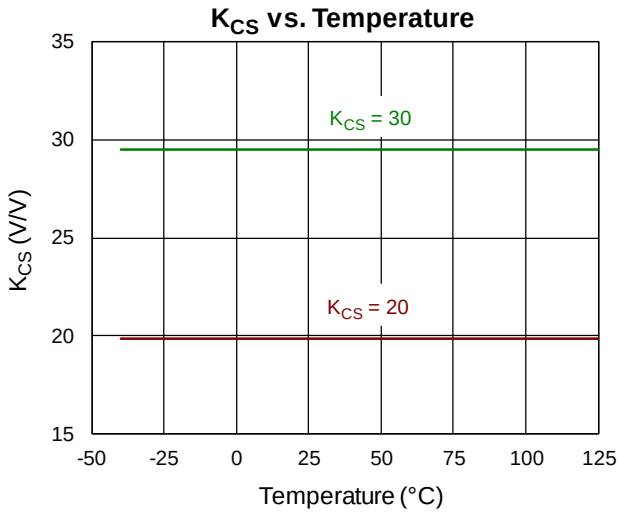


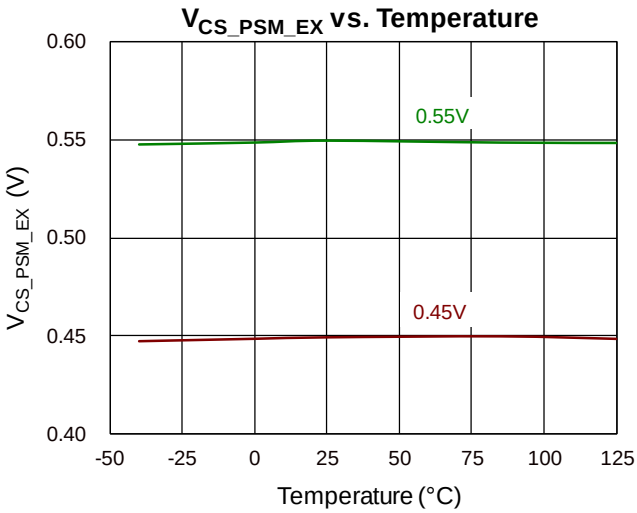


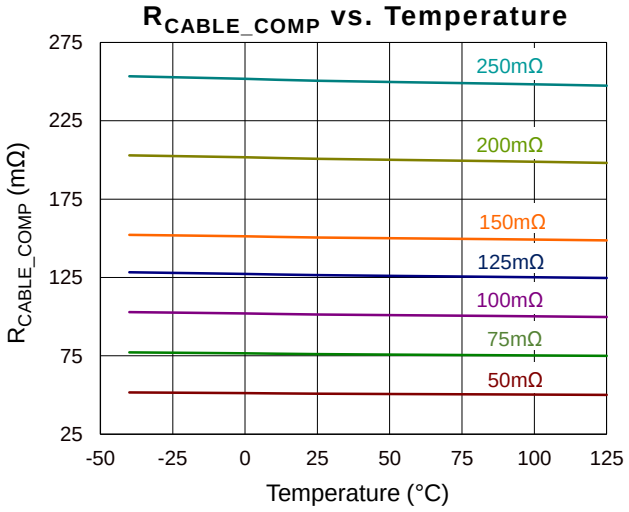


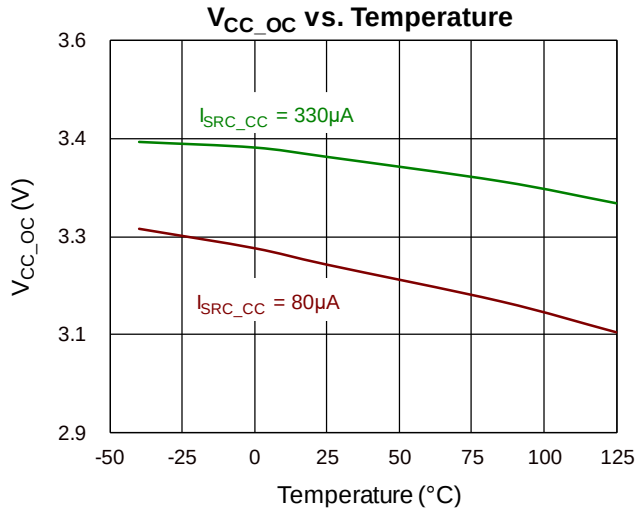


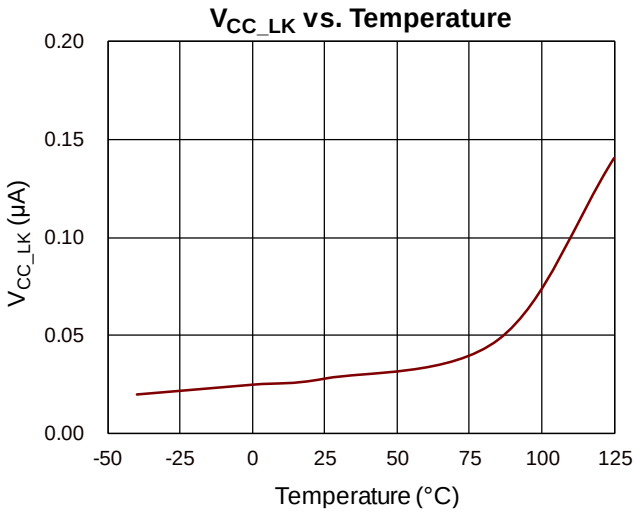


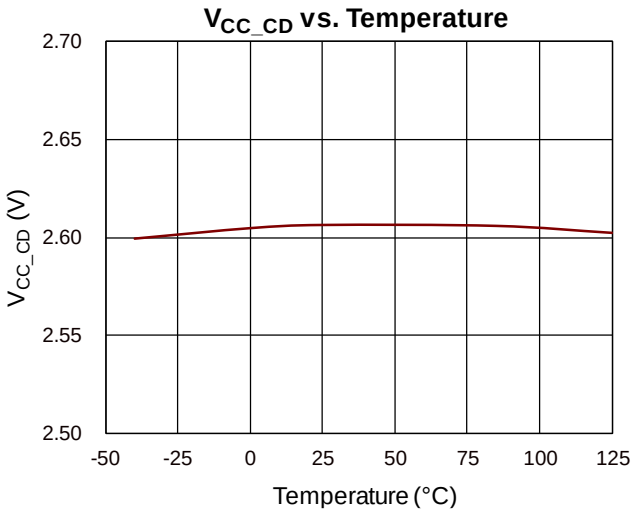


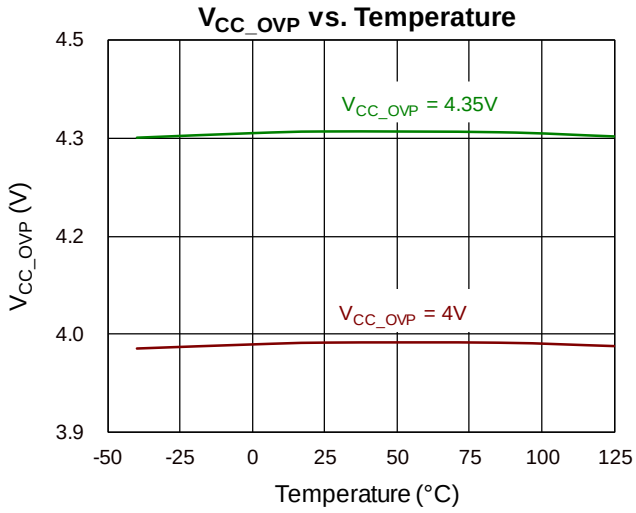


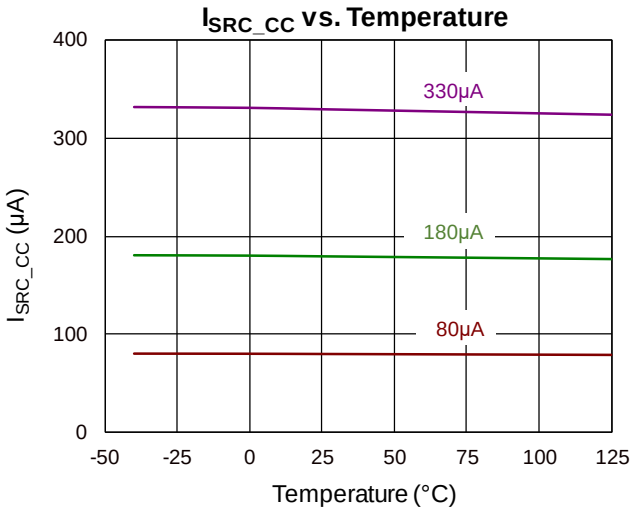


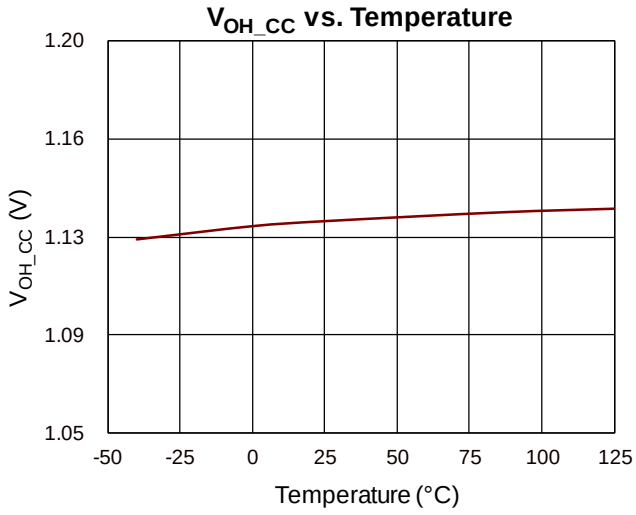


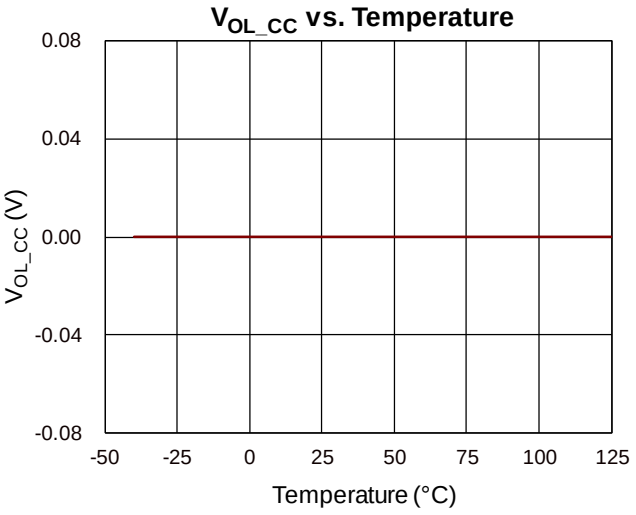


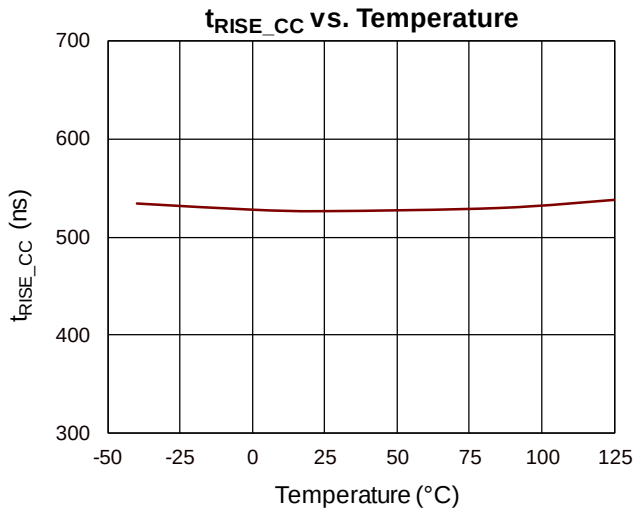


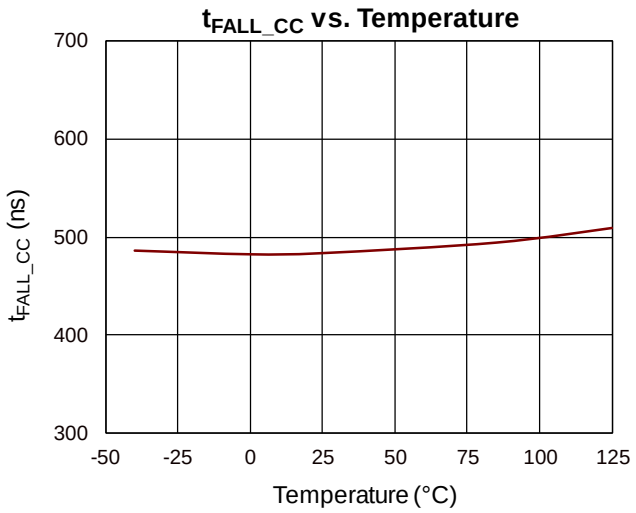


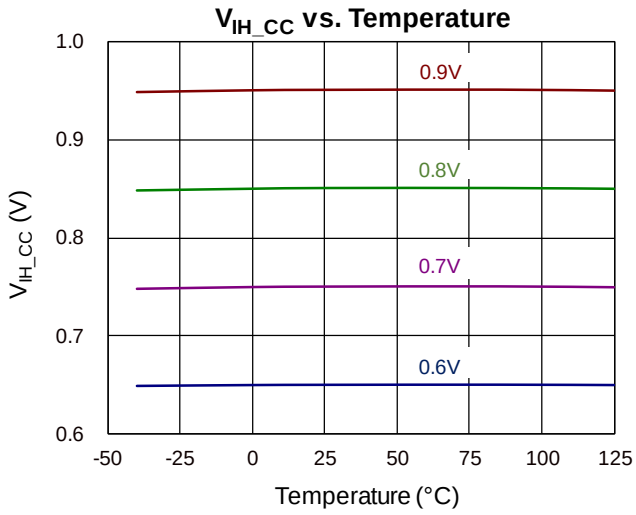


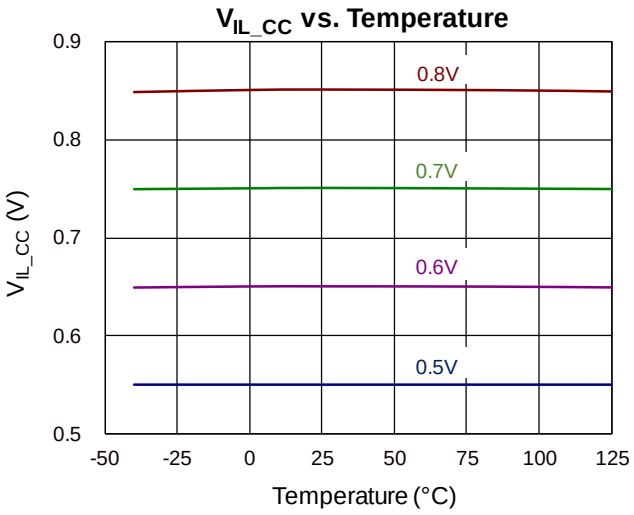


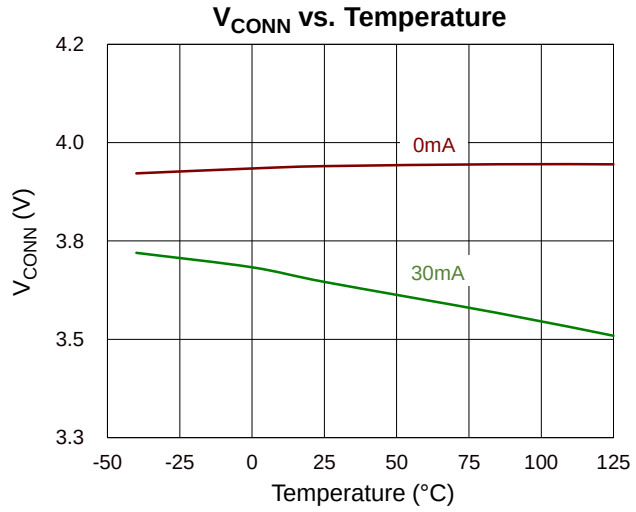


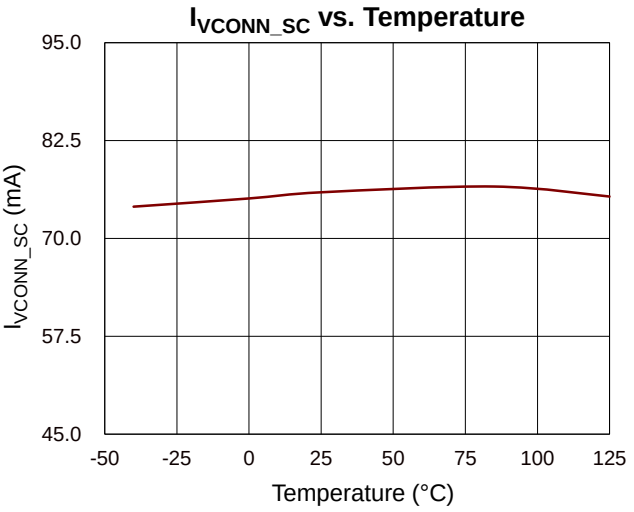


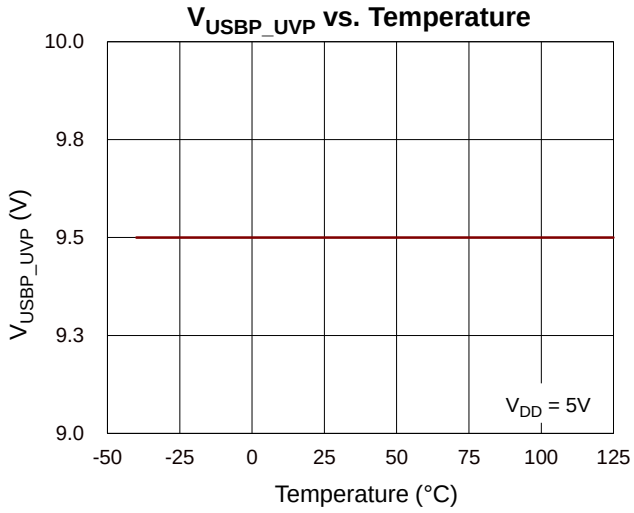


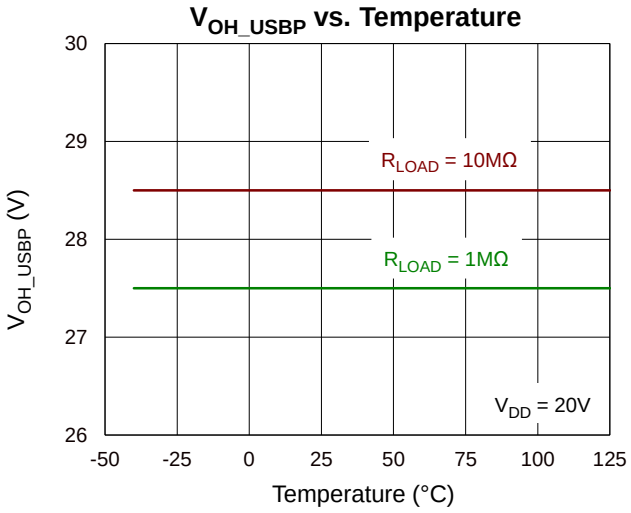


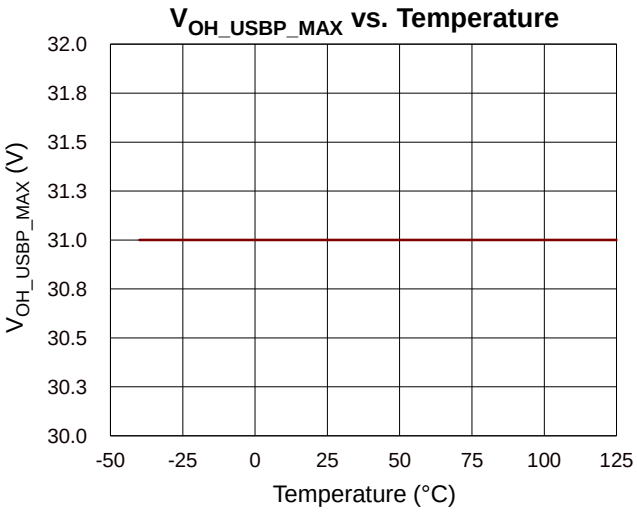












15 Operation

15.1 Constant Voltage (CV) and Constant Current (CC) Regulators in Source Application

The RT7202KNL integrates a shunt regulator for CV and CC regulations. Both outputs of CV and CC regulators are connected to OPTO in parallel as the analog output. The operation of each feedback loop is similar to that of TL431-based regulator. However, the wider operating range of OPTO, from 0.3V to 25V, improves the design of power converters with a wider output range. If the voltage related to VDD, V_{DD}, is still below the turn-on threshold, V_{VDD_ON}, OPTO will keep in high impedance to ensure a soft-start-up sequence. The reference voltages, V_{REF_CV} and V_{REF_CC}, are analog outputs from the embedded DACs which provide 10mV-resolution and 10mA-resolution for each CV and CC regulations.

15.2 Current-Sense Amplifier

The current in the power-ground bus can be sensed by an external current-sense resistor, R_{CS}. In order to minimize the power loss of R_{CS} and the noise, a differential amplifier with output gain, K_{CS}, and output offset, V_{CS_OFFSET}, is integrated.

15.3 CC1/CC2 Interface

The specific I/O pins, CC1/CC2, are integrated to handle USB Type-C compliance and PD protocol. When the RT7202KNL configured as a Source device, the optional current capabilities of 80μA, 180μA, and 330μA, provided by each of CC1 and CC2, will be advertised to a Sink device, implying the USB Type-C current of default, 1.5A, and 3.0A respectively.

16 Application Information

(Note 8)

16.1 AC-DC Source Port

16.1.1 Voltage Sense and Current Sense

The RT7202KNL integrates a resistor divider, R_{VFB}, for voltage feedback as shown in Figure 1. The voltage related to VDD, V_{DD} is determined as:

$V_{DD} = K_{VFB} \times V_{VFB}$

$K_{VFB} = (R_{VFB1} + R_{VFB2}) / R_{VFB2} = 10$

The RT7202KNL also integrates a differential amplifier so that the sensed current, I_{CS}, through the current-sense resistor, R_{CS}, is determined as:

$I_{CS} = (V_{IFB} – V_{CS\_OFFSET}) / (R_{CS} \times K_{CS})$

16.1.2 Constant-Voltage (CV) and Constant-Current (CC) Regulations

For the CV loop, V_{DD} is determined by the reference voltage of CV regulator, V_{REF_CV}. For the CC loop, I_{CS} is determined by the reference voltage of CC regulator, V_{REF_CC}. Two loops incorporate an error amplifier respectively and both of them are connected to OPTO, driving the sinking current from the external circuit with an optocoupler and a resistor, R_D, in series to V_{DD}. The optocoupler transfers the compensation signal from the secondary side to the primary side. Note that for better linearity of the compensation range, R_D is suggested to be designed for satisfying the maximum COMP current of PWM controller, I_{COMP_MAX}, at the minimum voltage related to VDD, V_{DD_MIN}.

$$\frac{(V_{DD\_MIN} - V_F - 0.3V)}{R_D} \times CTR \geq I_{COMP\_MAX}$$

CTR: Current transfer ratio of the optocoupler

V_F: Forward voltage of the optocoupler

0.3V: The threshold of OPTO voltage for driving the minimum OPTO sinking current

16.1.3 Linear Cable Compensation

A transconductance amplifier is integrated for linear cable compensation. The compensation voltage, V_{CABLE_COMP}, is determined as:

$V_{CABLE\_COMP} = I_{CS} \times R_{CABLE\_COMP}$

In addition, a programable solution is reserved by ADC-measurement as a proprietary function.

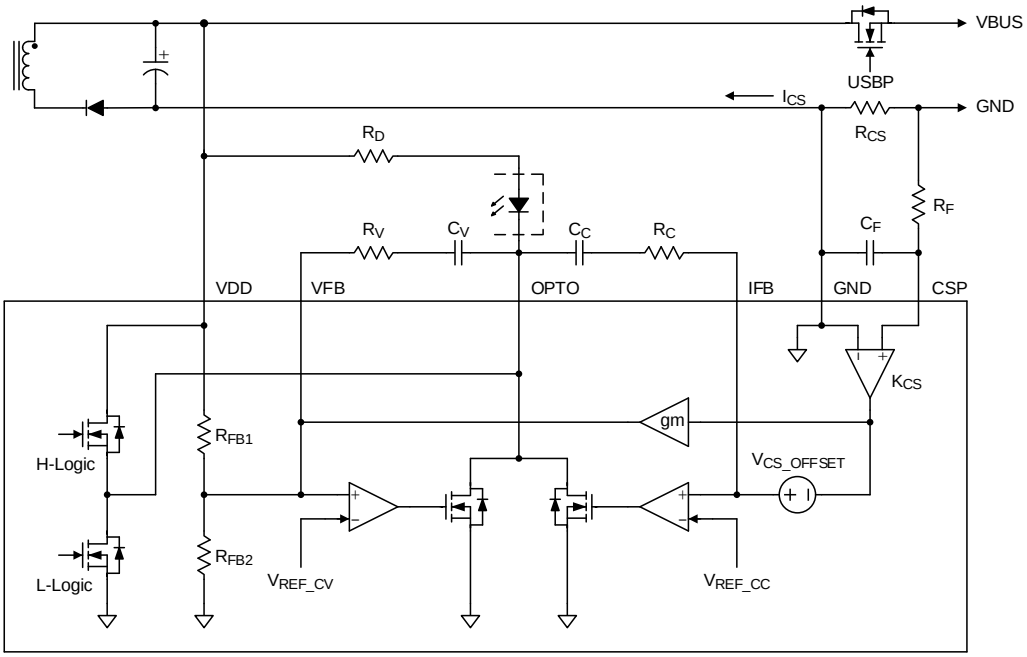


Figure 1. Application Circuit for CV and CC Regulations

16.1.4 Power Sequence

When start-up, V_{REF_CV} is set to the standby reference voltage, $V_{REF\_CV\_ST}$, and then V_{DD} is regulated to 5V. Once a Type-C cable attached, the Sink port will deliver power request back to the embedded MCU, changing V_{REF_CV} and regulating V_{DD} to the correspond voltage level. In contrary, once the Type-C cable detached, the embedded MCU will enter power-saving mode and back to 5V.

16.1.5 Rising and Falling Regulation

As shown in Figure 2, when PD protocol established, V_{REF_CV} can be set by the request of the Sink port. Both rise and fall time of V_{DD} must meet PD compliance, defined as 275ms. The slope of V_{REF_CV} during rising interval, S_{RISE}, can be determined as:

$$S_{RISE} \geq \frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms}$$

V_{DD_MAX}: Maximum voltage request

V_{DD_MIN}: Minimum voltage request

275ms: Rise and fall time of PD compliance

25ms: Time margin from transient response of system

During the falling interval, the constant-discharge current, I_{DIS_VDD}, is enabled. The capability of I_{DIS_VDD} must take the output capacitors of system, C_{OUT}, in consideration. I_{DIS_VDD} can be determined as:

$$I_{DIS\_VDD} \geq C_{OUT} \times \frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms}$$

The slope of V_{REF_CV} during falling interval, S_{FALL}, can be determined as:

$$\frac{V_{DD\_MAX} - V_{DD\_MIN}}{275ms - 25ms} \leq S_{FALL} \leq \frac{I_{DIS\_VDD}}{C_{OUT}}$$

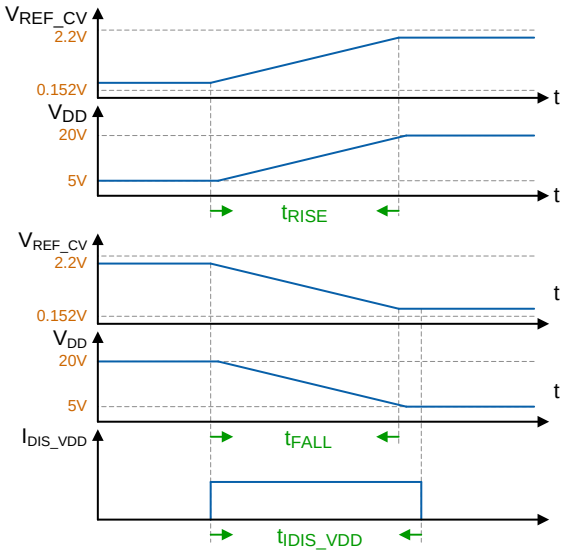


Figure 2. Rising and Falling Regulation

16.1.6 Programmable Shutdown Flow from Protections

The RT7202KNL can achieve multiple behaviors for any abnormal condition occurs.

- Auto-Recovery

  Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously V_{DD} is forced down to V_{VDD_OFF} by pulling V_{OPTO} down. After V_{DD} turned-off, V_{OPTO} is released and V_{DD} is powered up again.

- Output-Latch

  Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously V_{DD} is set back to 5V. To recover the system, the output cable must be removed and then attached again.

- Power-Latch

  Once the embedded MCU receives the fault flags from the algorithm or peripheral circuits designed for protection, the blocking N-MOSFET will be immediately turned off and simultaneously V_{DD} is set back to 5V. After that, V_{OPTO} is pulled high to trigger the protection from the primary-side PWM controller, which is supposed to be a latch behavior. To recover the system, the AC cable must be removed and then attached again.

16.1.7 Over/Undervoltage Protection (OVP/UVP)

As shown in Figure 3 and Figure 4, the RT7202KNL provides a quick-interruption solution to turn off the blocking N-MOSFET when either overvoltage or undervoltage condition occurs in VDD, such as the malfunction of feedback loop due to aging of the optocoupler. Once V_{DD} is higher than the overvoltage protection threshold, V_{VDD_OVP}, over the deglitch time, t_{VDD_OVP}, or V_{DD} is lower than the undervoltage protection threshold, V_{VDD_UVP}, over the deglitch time, t_{VDD_UVP}, the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU. Besides, a programable solution is reserved by ADC-measurement as a proprietary function.

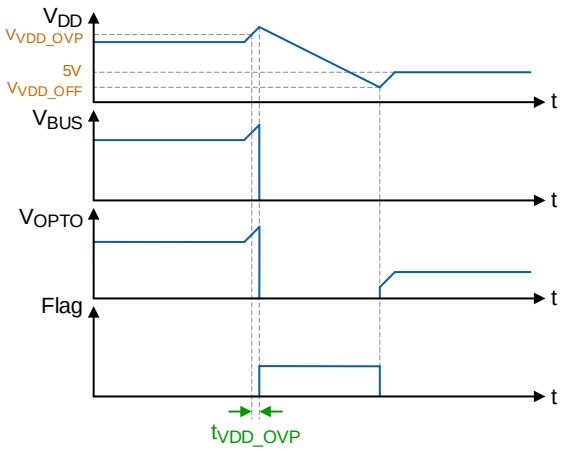


Figure 3. Timing Sequence of OVP with Auto-Recovery

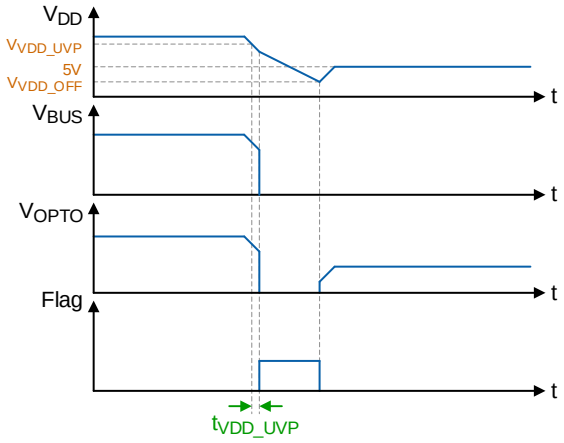


Figure 4. Timing Sequence of UVP with Auto-Recovery

16.1.8 CC1/CC2 Overvoltage Protection (IO OVP)

In order to prevent the damage of CC1/CC2 from the abnormal contact to VBUS at the USB Type-C receptacle, a quick-interruption solution is designed to turn off the blocking N-MOSFET as shown in Figure 5. Once V_{DD} is higher than the threshold for CC1/CC2 overvoltage protection, V_{VDD_IOOVP}, and the voltage related to CC1/CC2, V_{CC} is higher than the CC1/CC2 overvoltage protection threshold, V_{CC_OVP}, over the debounce time, t_{CC_OVP}, the blocking N-MOSFET will be turned off immediately. Meanwhile, a fault flag will deliver to the embedded MCU.

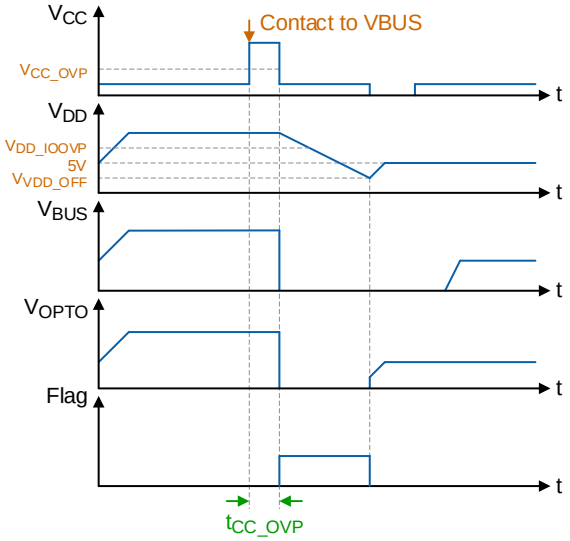


Figure 5. Timing Sequence of CC1/CC2 OVP with Auto-Recovery

16.1.9 Overcurrent Protection (OCP)

The RT7202KNL provides a programmable solution by ADC-measurement to achieve overcurrent protection as shown in Figure 6. Once I_{CS} is higher than the programming threshold, I_{OCP_ADC}, over a debounce time, t_{OCP_ADC}, the programmable shutdown flow will be triggered.

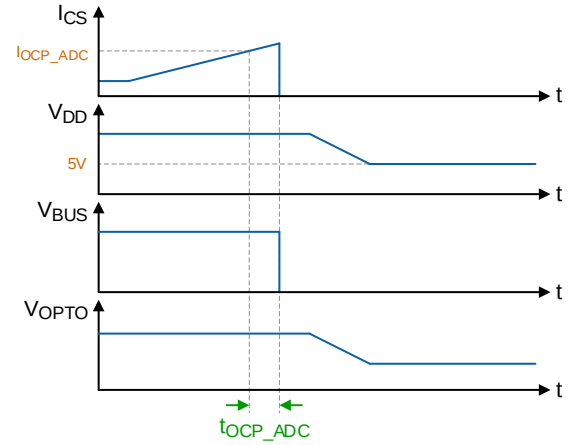


Figure 6. Timing Sequence of OCP with Output-Latch

16.1.10 Over-Temperature Protection (OTP)

A programmable solution by ADC-measurement to achieve over-temperature protection is designed as shown in Figure 7. If any of specific I/O pins, CC1/CC2, can be defined as general purpose I/O, the internal sourcing current source, I_{SRC_CC}, will be set to 80μA. By using an NTC/PTC connected between CC1/CC2 and GND, the ambient in the specific region can be monitored. Once the voltage related to CC1/CC2, V_{CC}, is lower than the over-temperature threshold, V_{OTP_ADC}, over a debounce time, t_{OTP_ADC}, the programmable shutdown flow will be triggered.

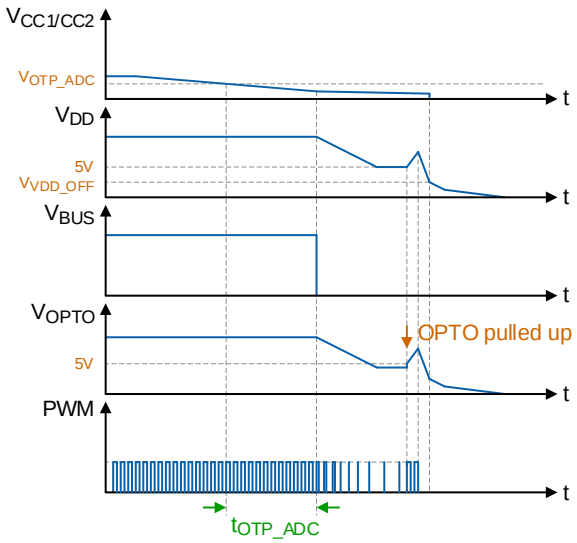


Figure 7. Timing Sequence of OTP with Power-Latch

16.2 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to -ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-10 package, the thermal resistance, θ_{JA}, is 194.2°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (194.2°C/W) = 0.51W for a SOP-10 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

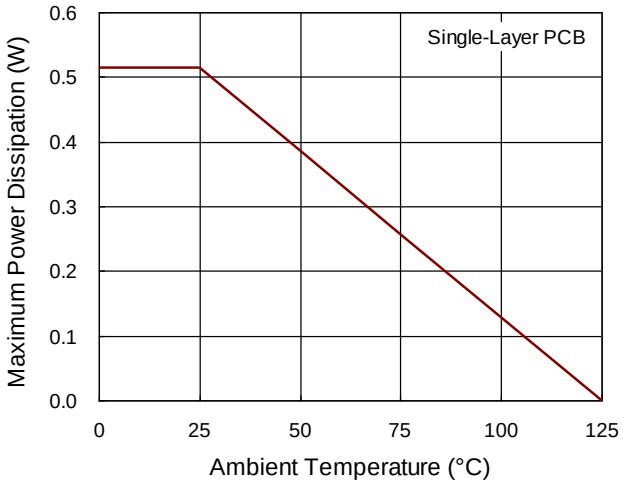
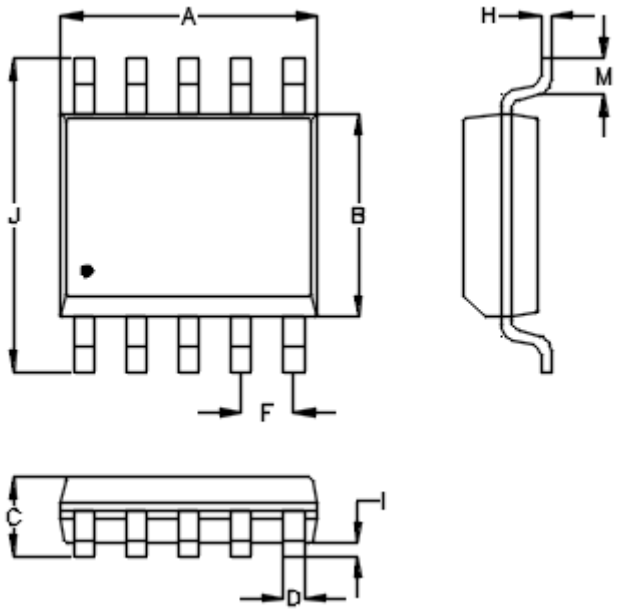


Figure 8. Derating Curve of Maximum Power Dissipation

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

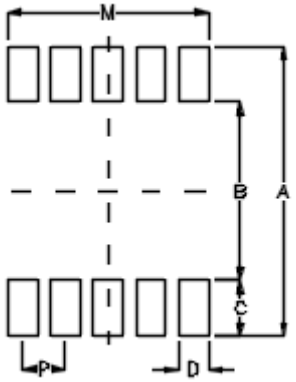
17 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.800	5.000	0.189	0.197
B	3.800	4.000	0.150	0.157
C	1.300	1.750	0.051	0.069
D	0.300	0.500	0.012	0.020
F	1.000		0.039	
H	0.100	0.250	0.004	0.010
I	0.050	0.250	0.002	0.010
J	5.800	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

10-Lead SOP Plastic Package

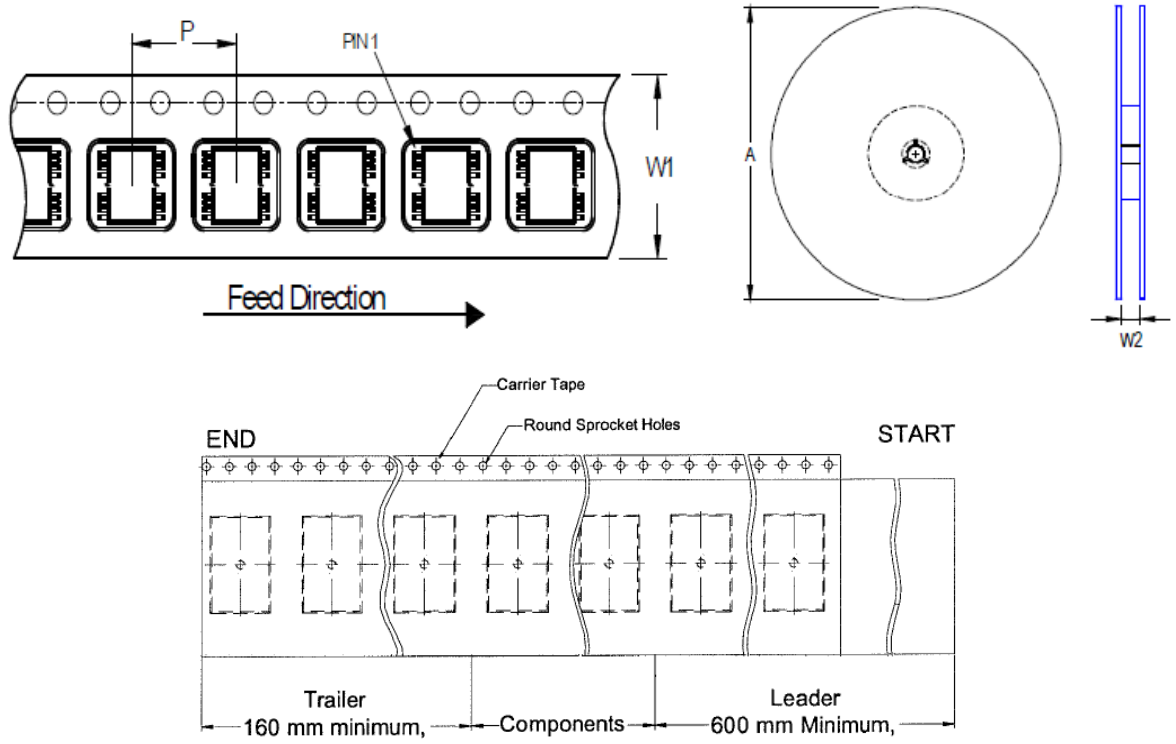
18 Footprint Information



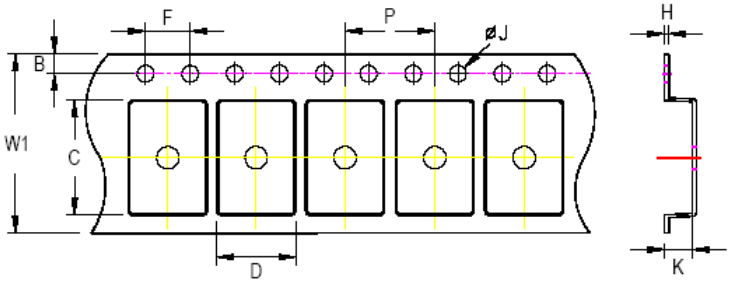
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-10	10	1.00	6.80	4.20	1.30	0.70	4.70	±0.10

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOP-10	12	8	330	13	3,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Package \ Container	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
SOP-10	13”	3,500	Box G	1	3,500	Carton A	6	21,000

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
00	2024/6/4	Final	Ordering Information on P1 Functional Pin Description on P4 Application Information on P19