RICHTEK®

RT7202KLC

Programmable USB PD Sink Controller

1 General Description

The RT7202KLC is a USB Power Delivery (PD) controller with an embedded MCU solution that is utilized on the consumer side. It supports the attaching and orientation detection of the USB Type-C. The physical layer of USB PD and BMC transceiver are also integrated. In addition, the RT7202KLC provides several monitoring and programmable solutions for the occurrence of abnormal conditions.

The recommended junction temperature range is –40°C to 125°C, while the ambient temperature range is –40°C to 105°C.

2 Ordering Information

RT7202KLC□□-□

Programmed Firmware Code AABBX(1)
AA: Application Code
BB: Model Code
X: Customer Approved Version Code

Package Type(2)
QW: WQFN-24L 4x4 (W-Type)
(Exposed Pad: Option 2)

Lead Plating System
G: Richtek Green Policy Compliant(3)

Note 1.

- Marked with (1) indicated: AABBX is optional, for firmware inside IC only.
- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **Support USB PD2.0/PD3.0 and PPS**
- **Suited for 3V to 22V VDD Range**
- **Embedded MCU with a Mask ROM of 32kB, an OTP-ROM of 16kB, and an SRAM of 2kB**
- **High-Side Current Sensing**
- **N-MOSFET Driver**
- **Slave I²C Interface**
- **Protection**
  - **Programmable Overvoltage Protection**
  - **Programmable Undervoltage Protection**
  - **Programmable Overcurrent Protection**
  - **Programmable Over-Temperature Protection**

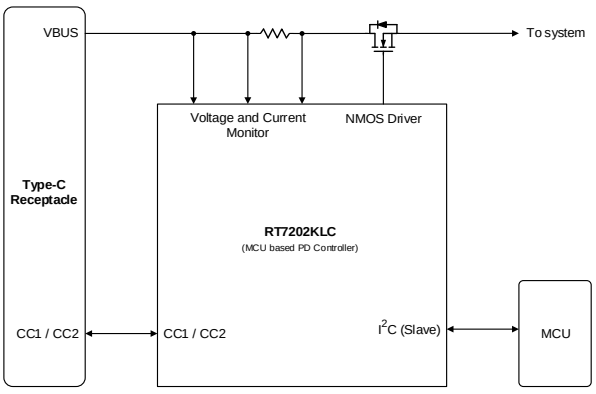
4 Applications

- USB Type-C Controller in Sink Application for IoT Devices of Power over Ethernet, Smart Speaker, Projector, and Other Electronics

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

6 Simplified Application Circuit



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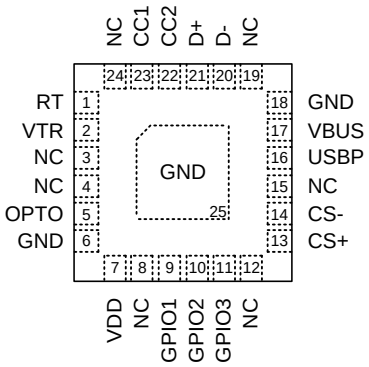
7 Pin Configuration

(TOP VIEW)



WQFN-24L 4x4

8 Functional Pin Description

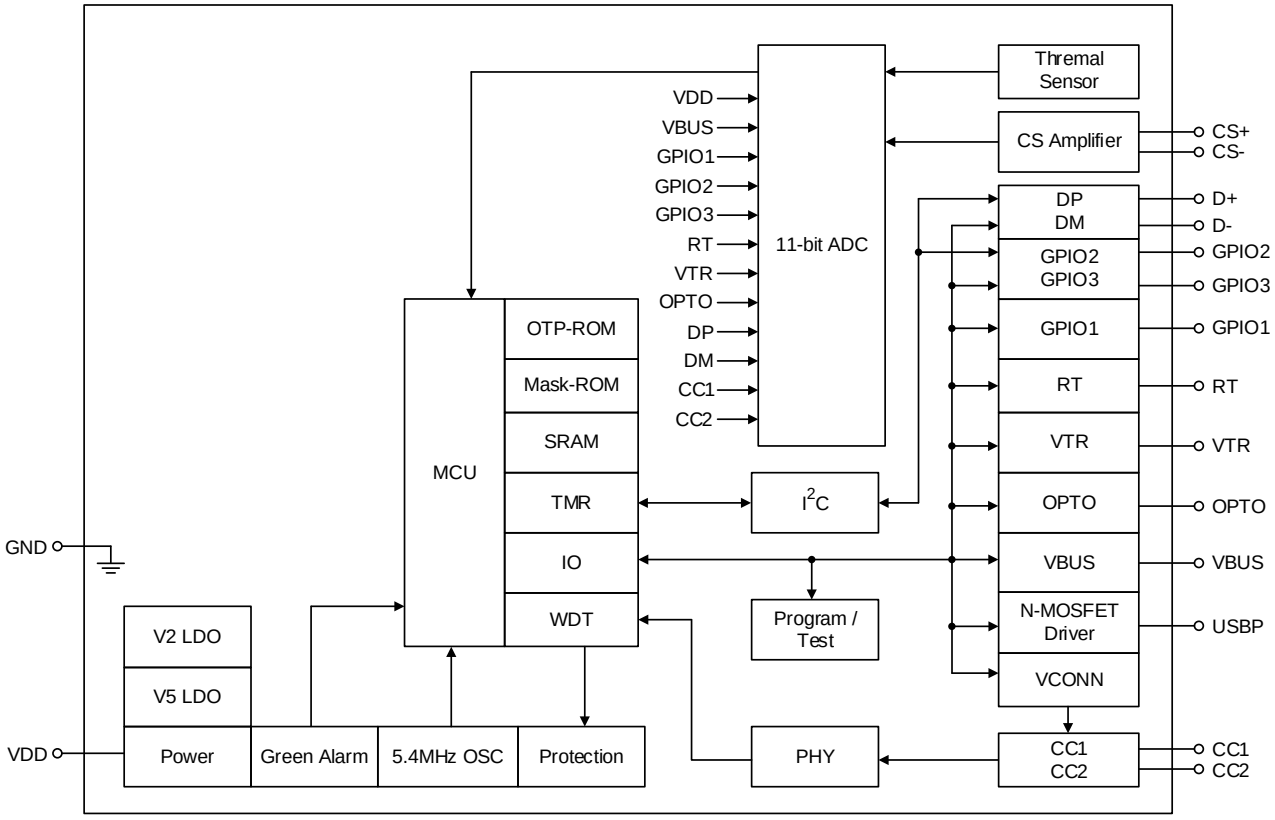
Pin No.	Pin Name	Type	Pin Function
1	RT	A/D IO	Remote thermal sensor connection node for over-temperature protection. Can be configured as sourcing current and ADC input.
2	VTR	AI	Transformer voltage sense node. Can be configured as sourcing current and ADC input.
3, 4, 8, 12, 15, 19, 24	NC	NC	No internal connection.
5	OPTO	AO	Current-source output of control regulator for optocoupler connection. Can be configured as open-drain output and ADC input.
6, 18	GND	GND	Ground.
7	VDD	PWR	Supply input voltage.
9	GPIO1	A/D IO	General purpose input/output. Can be configured as open-drain output, sourcing current, and ADC input.
10	GPIO2	A/D IO	General purpose input/output. Can be configured as I^2C-SDA, open-drain output, sourcing current, and ADC input.
11	GPIO3	A/D IO	General purpose input/output. Can be configured as I^2C-SCL, open-drain output, sourcing current, and ADC input.
13	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
14	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
16	USBP	D IO	Control signal of a blocking N-MOSFET.
17	VBUS	A IO	VBUS sensing and bleeder connection node to provide another path to discharge the VBUS capacitor. Can be configured as ADC input.
20	D-	A/D IO	USB D- channel for BC1.2. Does not support USB data transmission.
21	D+	A/D IO	USB D+ channel for BC1.2. Does not support USB data transmission.
22	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.

Pin No.	Pin Name	Type	Pin Function
23	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
25 (Exposed Pad)	GND	GND	Power ground. The exposed pad must be connected to GND and well-soldered to a large PCB copper area for maximum power dissipation.

8.1 IO Type Definition

- A/D IO: Analog/Digital Input/Output Pin
- AI: Analog Input Pin
- AO: Analog Output Pin
- A IO: Analog Input/Output Pin
- D IO: Digital Input/Output Pin
- GND: Ground Pin
- PWR: Power Pin

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- USBP to GND ---------- –0.3V to 32V
- VDD, VBUS, CS+, CS- to GND ---------- –0.3V to 28V
- OPTO, VTR, GPIO1, GPIO2, GPIO3, CC1, CC2, D+, D-, RT to GND ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-24L 4x4---------- 2.52W
- Package Thermal Resistance (Note 3)

  WQFN-24L 4x4, θ_{JA} ---------- 39.6°C/W

  WQFN-24L 4x4, θ_{JC} ---------- 7.1°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard. θ_{JC} is simulated at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD---------- 3V to 22V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
VDD Turn-On Threshold	V_{VDD_ON}		2.9	3.05	3.2	V
VDD Turn-Off Threshold	V_{VDD_OFF}		2.8	2.85	2.9	V
VDD Turn-On/Off Hysteresis	V_{VDD_HYS}		0.1	0.2	0.3	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.8V	--	200	300	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Operating Current	I_{DD_OP}	1. V_{DD} = 5V 2. Disable VTR function	--	5.5	6.6	mA
VDD Sleep-Mode Current	I_{DD_SLEEP}	1. V_{DD} = 5V 2. Disable VTR function	--	1.8	2.2	mA
VDD Green-Mode Current	I_{DD_GREEN}	1. V_{DD} = 5V 2. Disable VTR function	--	950	1150	µA
Maximum VDD Overvoltage Protection Threshold	$V_{MAX\_VDD\_OVP}$		23	24	25	V
VDD Overvoltage Protection Deglitch Time	$t_{D\_VDD\_OVP}$	(Note 6)	25	30	35	µs
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} > 2.8V	5.13	5.4	5.67	MHz
Maximum ADC Sense Voltage	V_{ADC_MAX}	With 11-bit analog to digital converter	2.178	2.2	2.222	V
OPTO Section						
OPTO Pull-Low Impedance for CV Open Loop	R_{L_OPTO}	OPTO shorted to GND by register setting	--	--	200	Ω
Current Sense Section						
Register-Programmable Current-Sense Voltage Gain	K_{CS}		39.6	40	40.4	V/V
Current-Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}		0.36	0.4	0.44	V
RT Section						
Open Loop Voltage	V_{RT_OP}	V_{DD} = 5V, I_{BIAS_RT} = 95µA	3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_RT}	V_{DD} > 3V (Note 6)	95	100	105	µA
			18	20	22	
			4.5	5	5.5	
			Open			
GPIO1 Section						
Open-Loop Voltage	V_{GP1_OP}	V_{DD} = 5V, I_{BIAS_GP} = 950µA	3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_GP1}	V_{DD} > 3V (Note 6)	900	1150	1400	µA
			95	100	105	
			18	20	22	
			Open			
GPIO2 (SDA), GPIO3 (SCL) Section (I^2C)						
Open-Loop Voltage	V_{GP_OP}	V_{DD} = 5V, I_{BIAS_GP} = 95µA	3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_GP}	V_{DD} > 3V (Note 6)	95	100	105	µA
			18	20	22	
			4.5	5	5.5	
			Open			

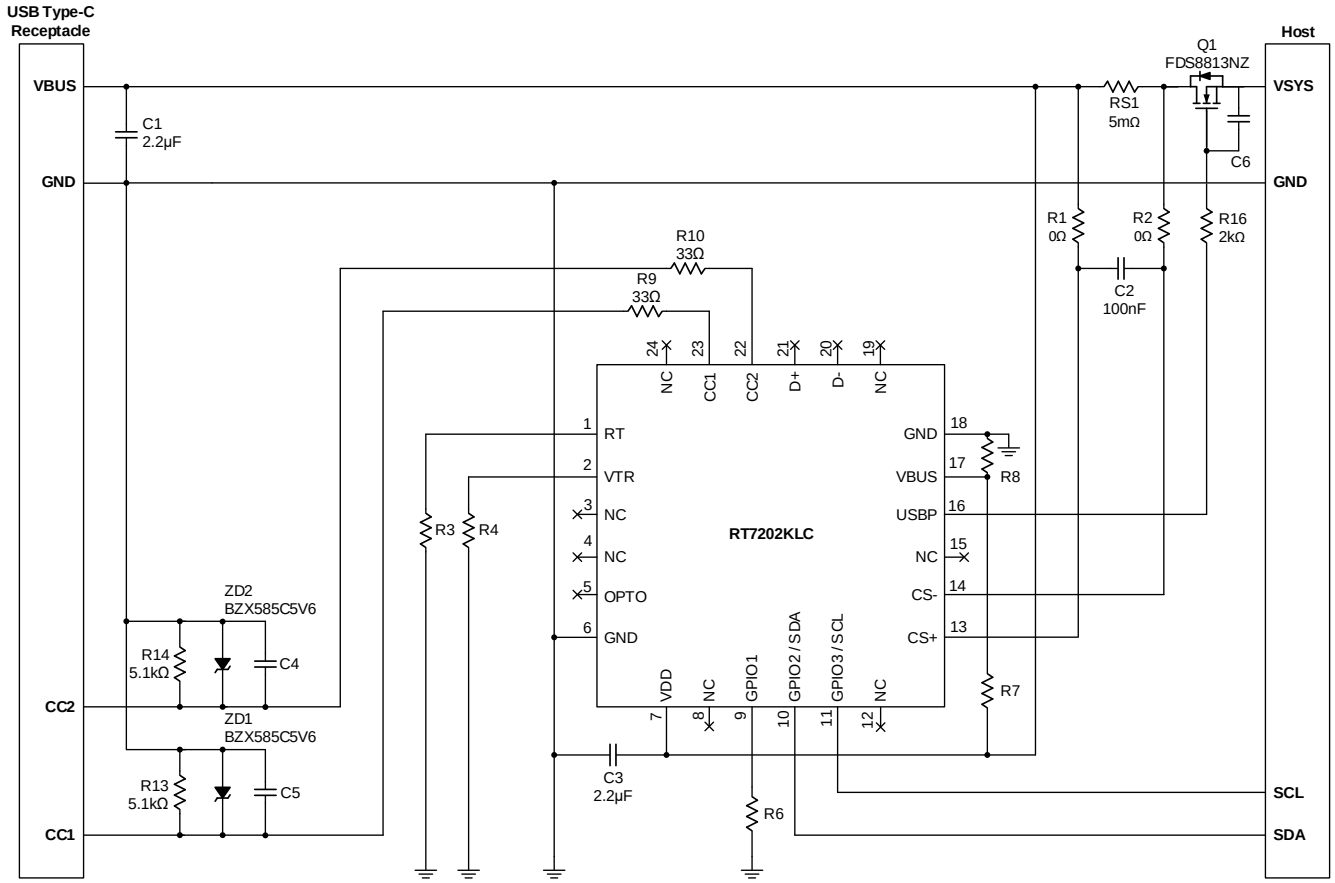
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Trip Voltage	V_{IH_I2C}		1.3	--	--	V
Input Low Trip Voltage	V_{IL_I2C}		--	--	0.4	V
VBUS Section						
Maximum VBUS Discharge Current	I_{VBUS_DIS}		2	--	30	mA
Pull-Low Impedance	R_{L_VBUS}	I_{VBUS_MAX} = 20mA	0.7	1	1.3	kΩ
D+, D- Section						
Register-Programmable Pull-High Resistance	R_{H_DPDM}	(Note 6)	Open			kΩ
			10	12.5	15	
Pull-Low Resistance	R_{L_DPDM}	(Note 6)	Open			kΩ
			16	20	24	
Register-Programmable Output High Voltage	V_{OH_OP}	V_{DD} = 5V, R_L = 15kΩ (Note 6)	Open Drain			V
	$V_{OH\_3.3V}$		2.97	3.3	3.63	
	$V_{OH\_1.8V}$		1.62	1.8	1.98	
	$V_{OH\_4.6V}$		4.1	4.6	5.1	
Output Low Voltage	V_{OL_OP}	R_L = 15kΩ	--	--	0.2	V
	$V_{OL\_3.3V}$					
	$V_{OL\_1.8V}$					
	$V_{OL\_4.6V}$					
Register-Programmable DP/DM Overvoltage Protection Threshold	V_{DPDM_OVP}	1. Turn off blocking MOSFET or not by register setting 2. Send a flag to MCU 3. V_{DD} > 5.5V	4.2	4.35	4.5	V
			3.85	4	4.15	
Register-Programmable DP/DM Overvoltage Protection Debounce Time	t_{DPDM_OVP}	(Note 6)	0.04	0.055	0.7	ms
			0.11	0.13	0.15	
			0.9	1	1.1	
			4.7	5	5.3	
CC1, CC2 Section						
Output High Voltage	V_{OH_CC}		1.05	1.125	1.2	V
Output Low Voltage	V_{OL_CC}		0	0.0375	0.075	V
Register-Programmable Input High Trip Voltage	V_{IH_CC}		0.7	0.8	0.9	V
			0.6	0.7	0.8	
			0.5	0.6	0.7	
			0.4	0.5	0.6	
Register-Programmable Input Low Trip Voltage	V_{IL_CC}		0.4	0.5	0.6	V
			0.3	0.4	0.5	
			0.2	0.3	0.4	
			0.1	0.2	0.3	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Open Loop Voltage for CC1/CC2 Sourcing Current	V_{CC_OP}		2.9	3.25	3.6	V
Register-Programmable Sourcing Current	I_{CC_SRC}		High Impedance			µA
			76	80	84	
			171	180	189	
			304	330	356	
CC1/CC2 Comparison Threshold for Cable Detection	V_{CC_CD}	1. V_{DD} > 3V 2. Disable/Enable by register 3. Send a flag to MCU	2.5	2.6	2.7	V
Register-ProgrammableCC1/CC2 Comparison Threshold for VBUS Short Detection	V_{CC_OVP}	1. Turn off blocking MOSFET or not by register setting 2. Send a flag to MCU 3. V_{DD} > 5.5V (Note 6)	4.2	4.35	4.5	V
			3.85	4	4.15	
Register-Programmable CC1/CC2 Cable Detection and Overvoltage Protection Debounce Time	t_{CC_OVP}	(Note 6)	0.04	0.055	0.7	ms
			0.11	0.13	0.15	
			0.9	1	1.1	
			4.7	5	5.3	
V_{CONN} Voltage	V_{VCONN}		4.8	--	5	V
			3.3	--	--	
V_{CONN} Short-Circuit Current	I_{VCONN_SC}		45	70	95	mA
USBP Section						
USBP Output High Voltage	V_{OH_USBP}	R_L = 10MΩ	VDD + 7	VDD + 8.5	VDD + 10	V
Maximum USBP Output High Voltage	$V_{OH\_MAX\_USBP}$		30	31	32	V
Register-Programmable Pull-Low Resistance when VBUS Drop Protection	$R_{OL\_VBUSDR\_USBP}$	If VBUS drop protection is triggered and V_{DD} > V_{USBP}, then R_{USBP} = $R_{OL\_VBUSDR\_USBP}$	7	10	13	kΩ
			14	20	26	
Pull-Low Resistance when USBP Turn-Off	$R_{OL\_USBPOFF}$	If VBUS drop protection is triggered and V_{USBP} >V_{DD}, then R_{USBP} = $R_{OL\_USBPOFF}$	1.62	2.7	3.78	kΩ
Pull-Low Resistance when VDD UVLO	$R_{OL\_UVLO\_USBP}$	If V_{DD} < V_{DD_OFF}, then R_{USBP} = $R_{OL\_UVLO\_USBP}$	3.08	4.4	5.72	kΩ
VTR Section						
Open-Loop Voltage	V_{VTR_OP}	V_{DD} = 5V, I_{VTR} = 95µA	3.6	4	4.4	V
Register-Programmable Internal Bias Current	I_{BIAS_VTR}	V_{DD} > 3V (Note 6)	95	100	105	µA
			18	20	22	
			4.5	5	5.5	
			Open			

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Sensor Section						
Thermal Sensor Error		25°C to 105°C (single point)	–7	--	7	°C

Note 6. Guaranteed by design.

13 Typical Application Circuit

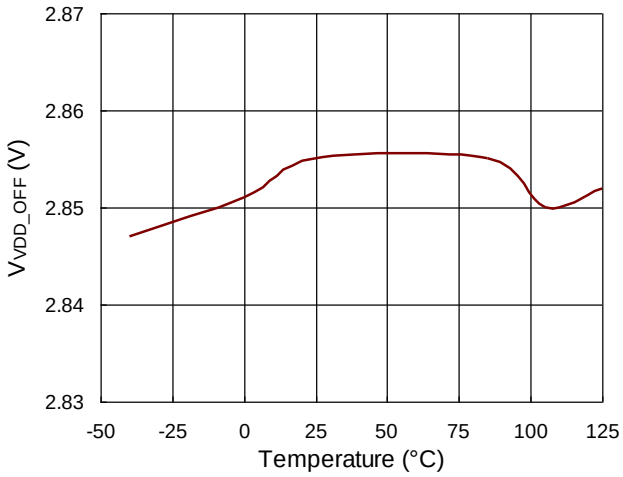


Note 7.

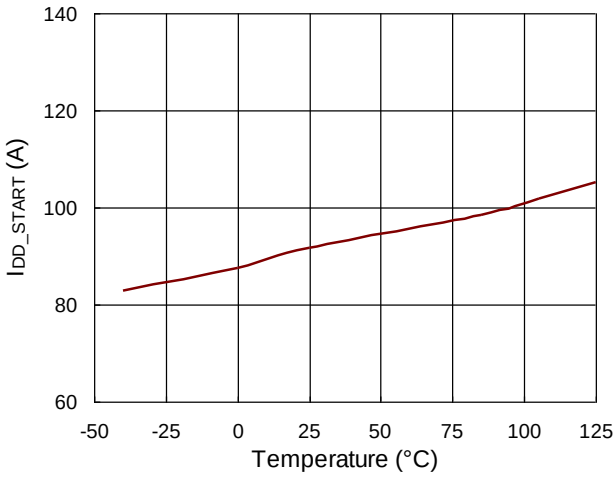
1. R3, R4, R6, R7, and R8 depend on the system design. Please use ±1% tolerance resistors for setting.
2. C4 and C5 depend on the USB PD specification: 200pF < Receiver < 600pF.
3. C6 depends on the soft-start for the power path.

14 Typical Operating Characteristics

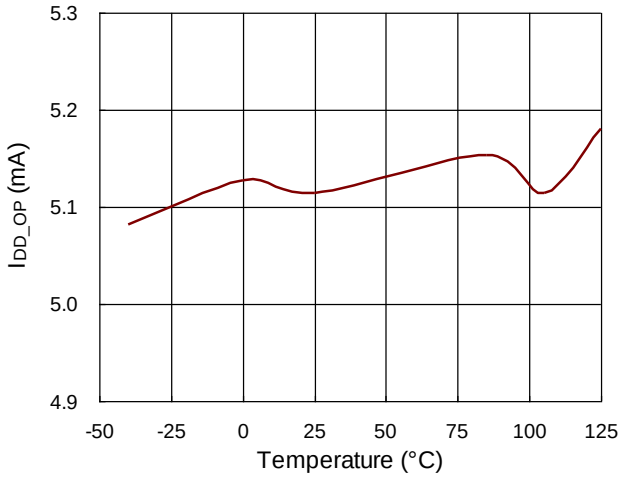
V_{VDD_OFF} vs. Temperature



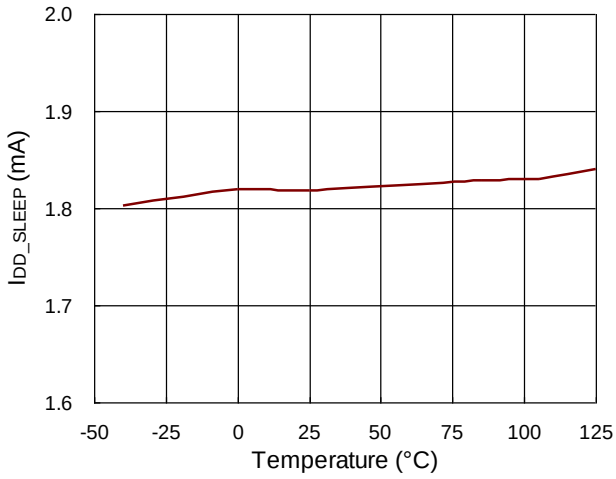
I_{DD_START} vs. Temperature



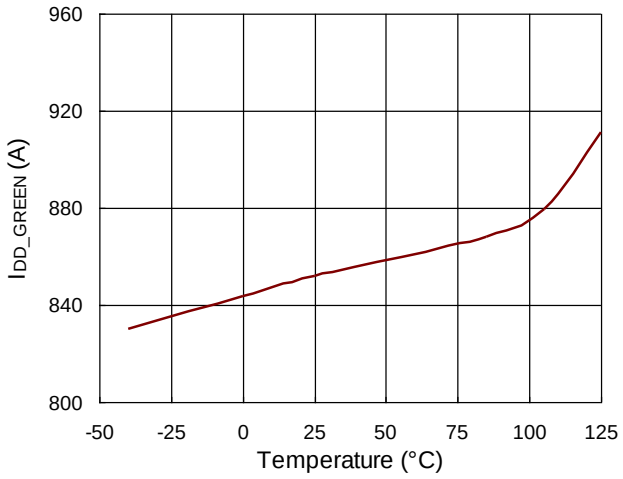
I_{DD_OP} vs. Temperature



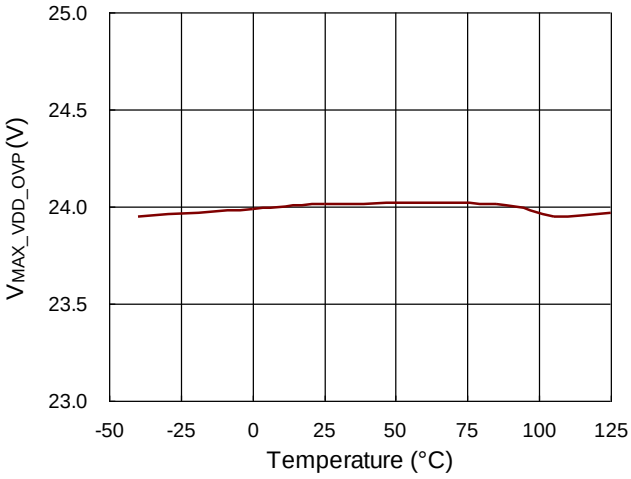
I_{DD_SLEEP} vs. Temperature

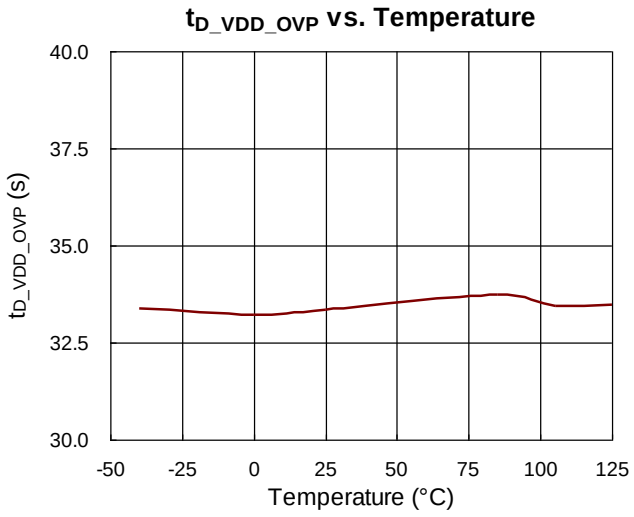


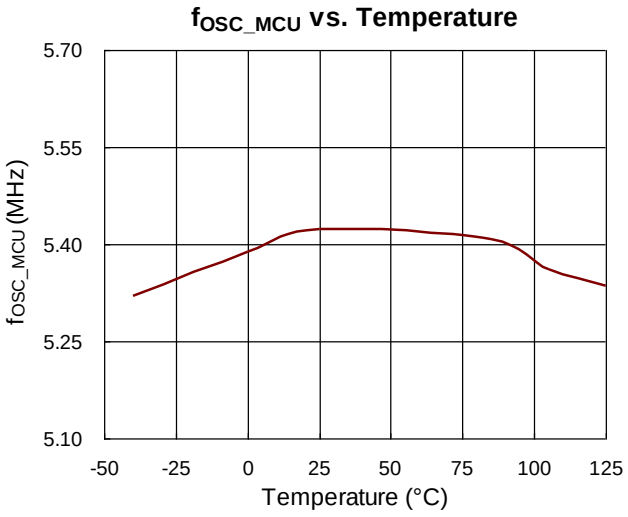
I_{DD_GREEN} vs. Temperature

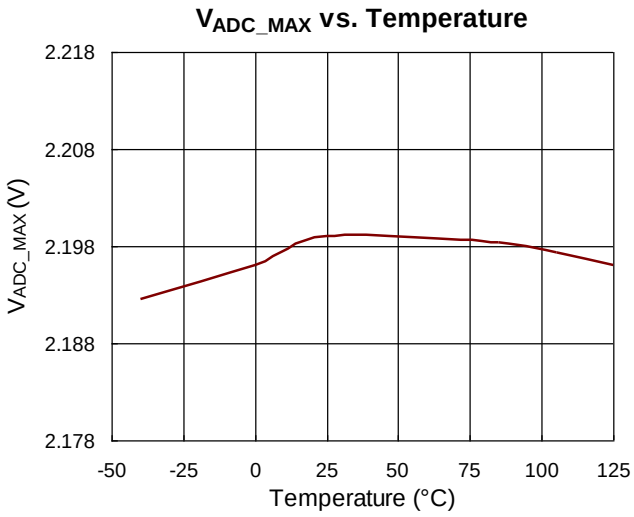


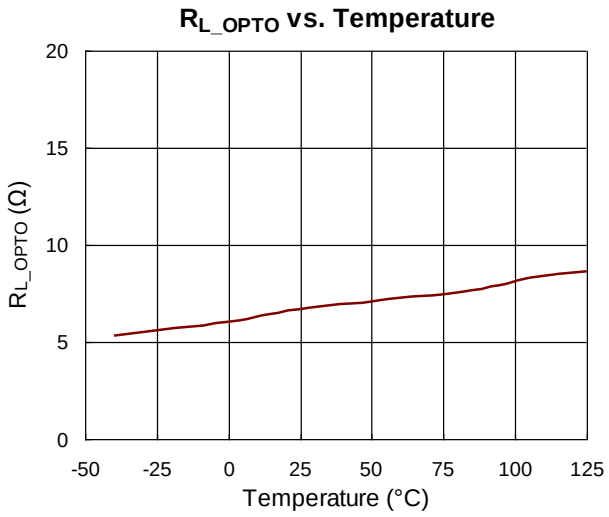
$V_{MAX\_VDD\_OVP}$ vs. Temperature

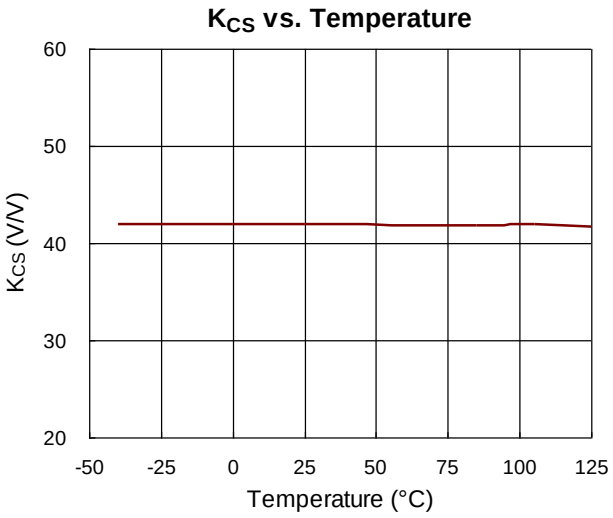


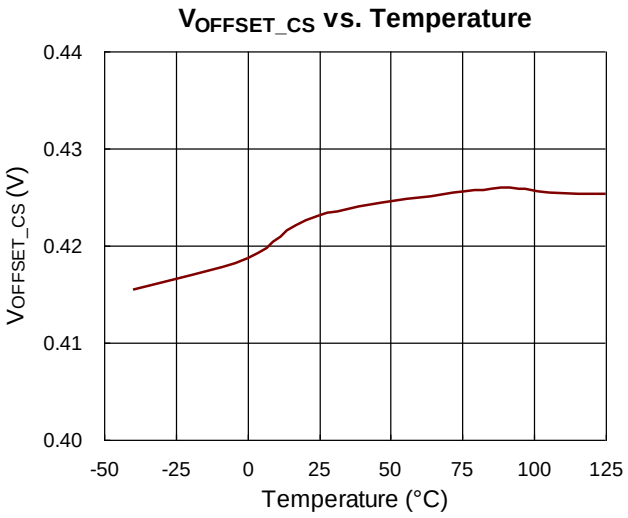


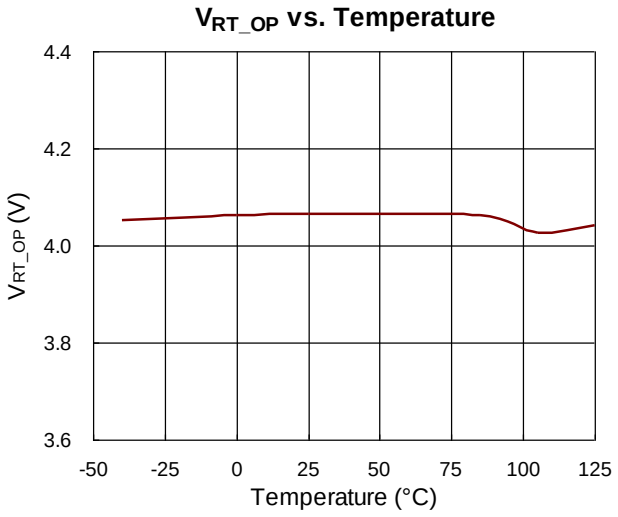


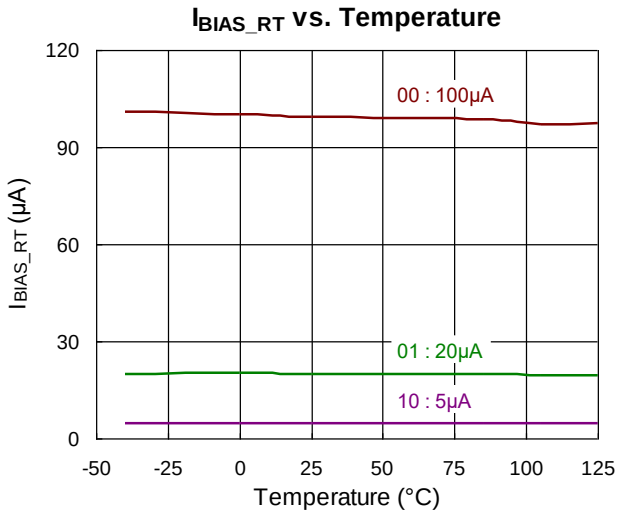


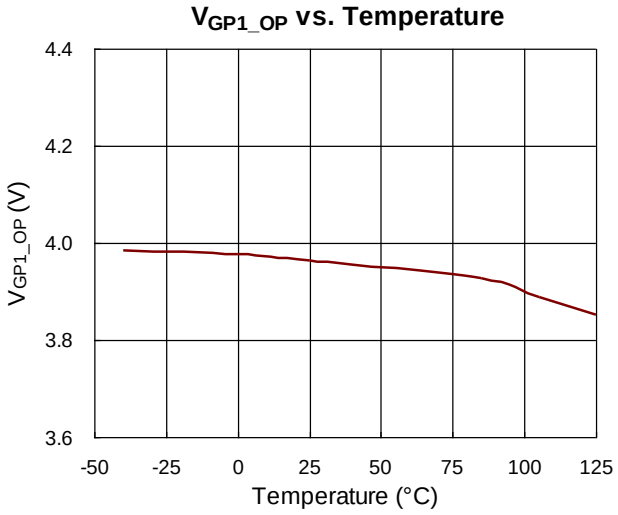


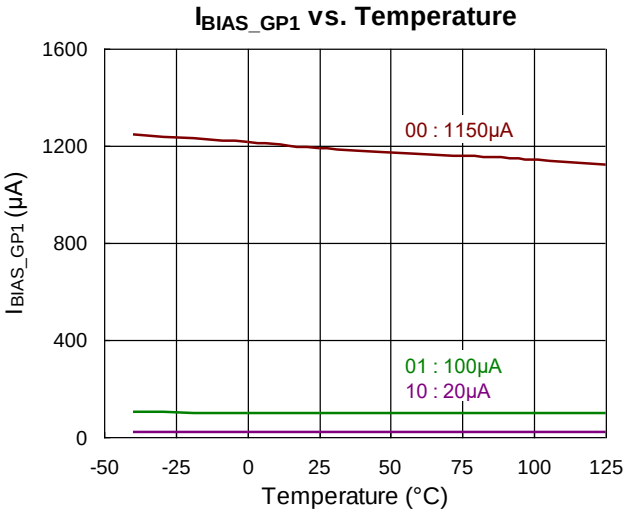


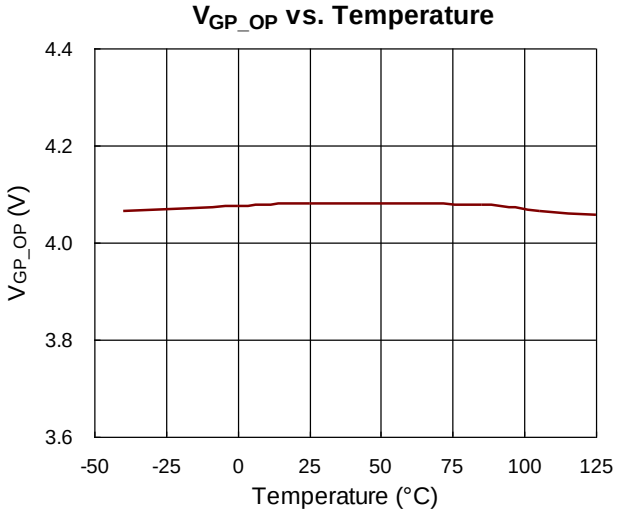


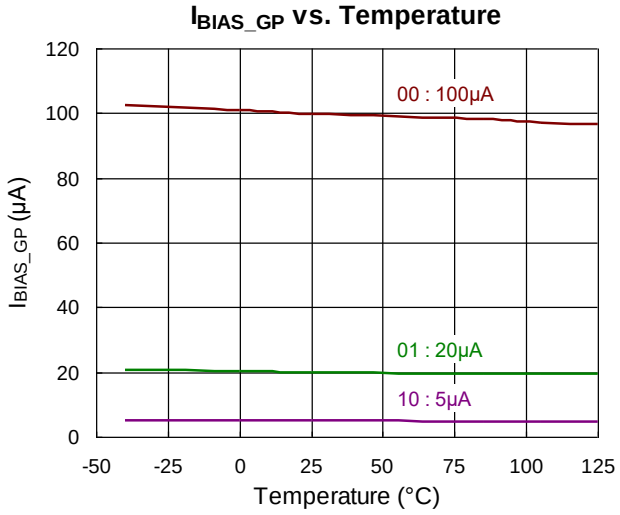




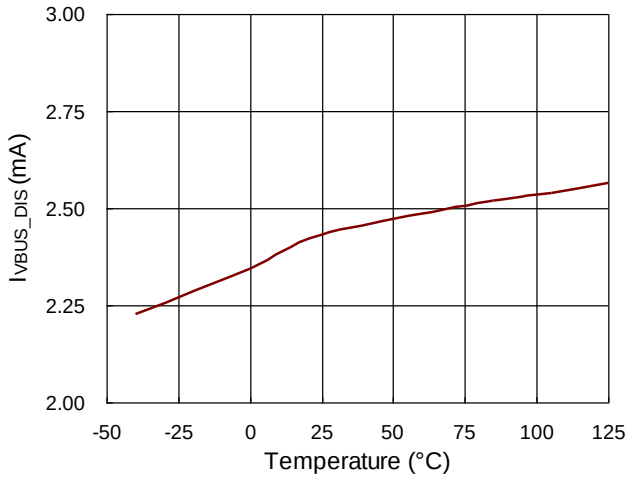




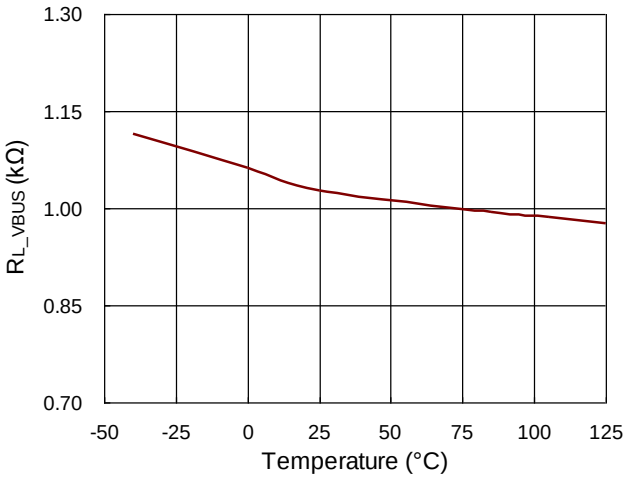




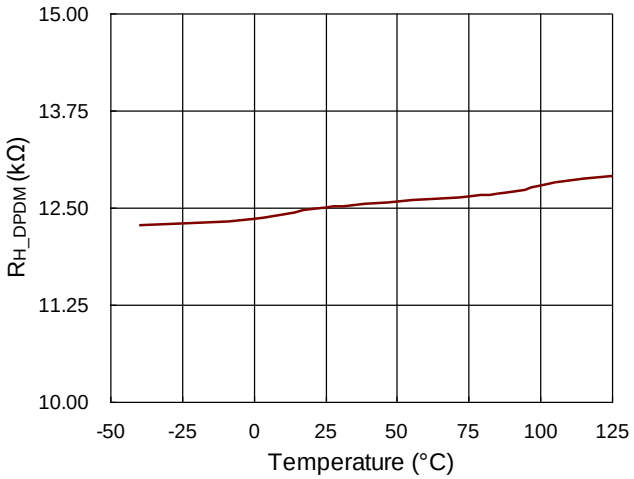
I_{VBUS_DIS} vs. Temperature



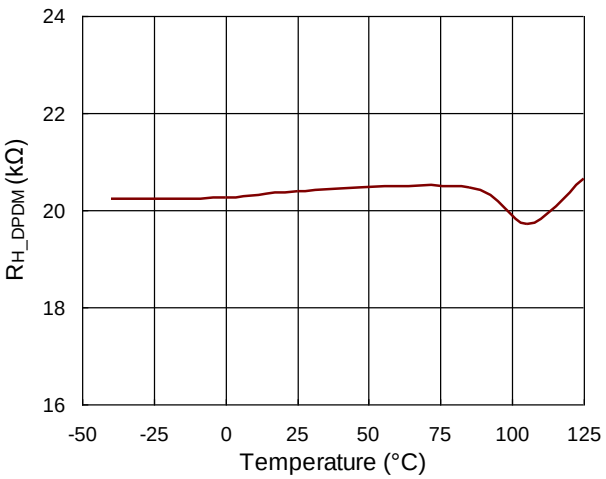
R_{L_VBUS} vs. Temperature



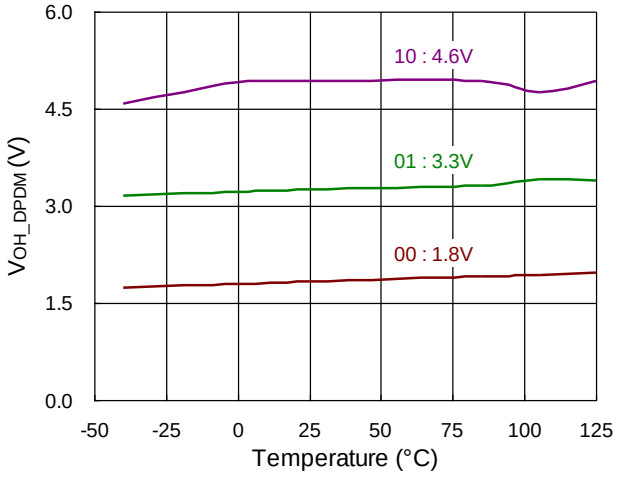
R_{H_DPDM} vs. Temperature



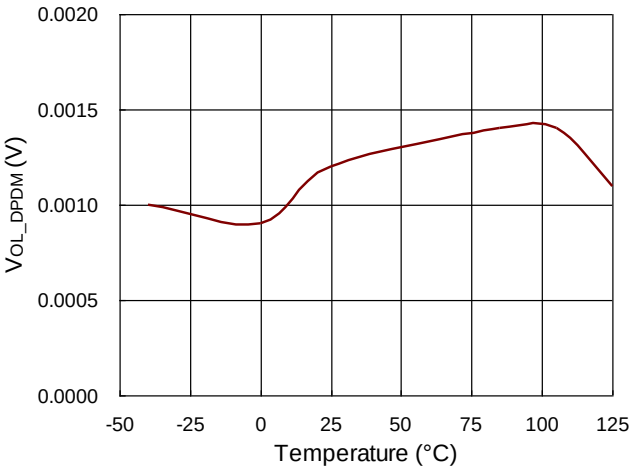
R_{H_DPDM} vs. Temperature

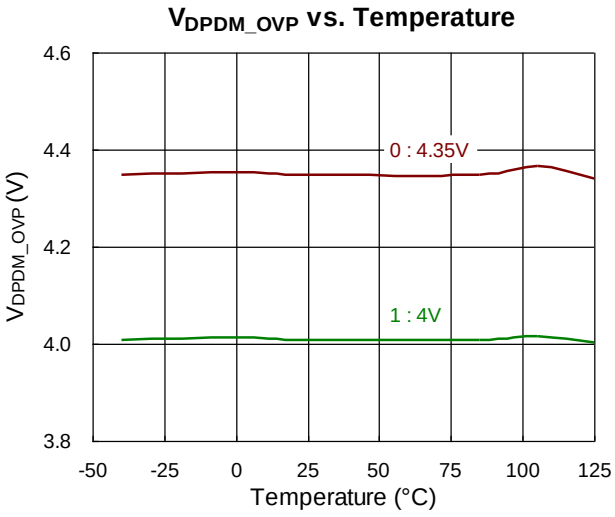


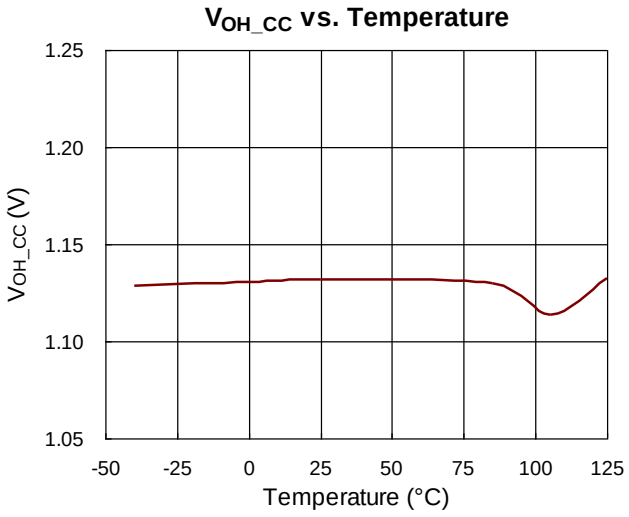
V_{OH_DPDM} vs. Temperature

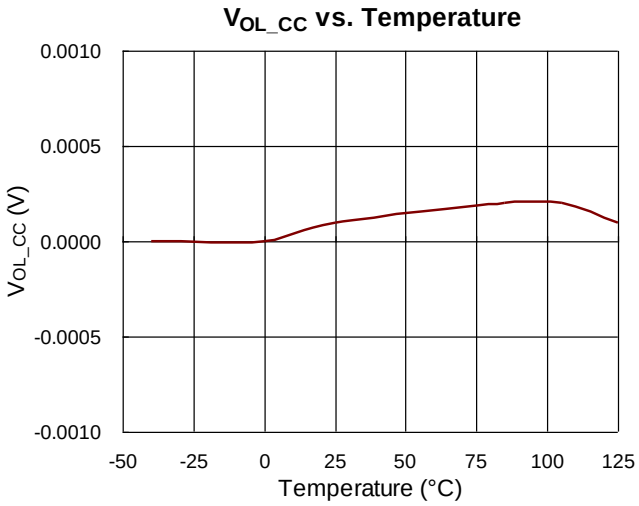


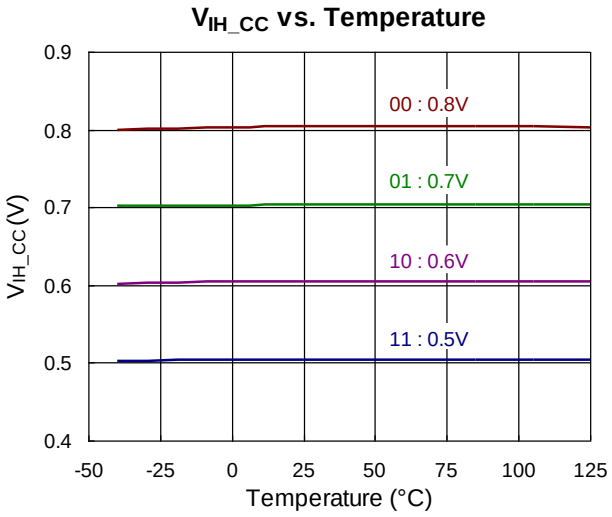
V_{OL_DPDM} vs. Temperature

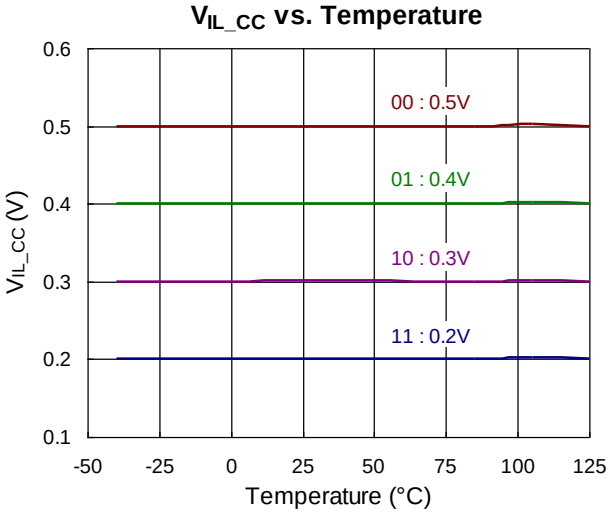


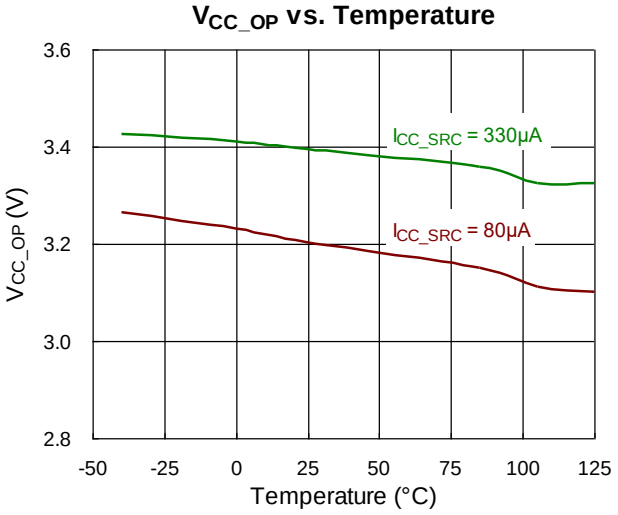




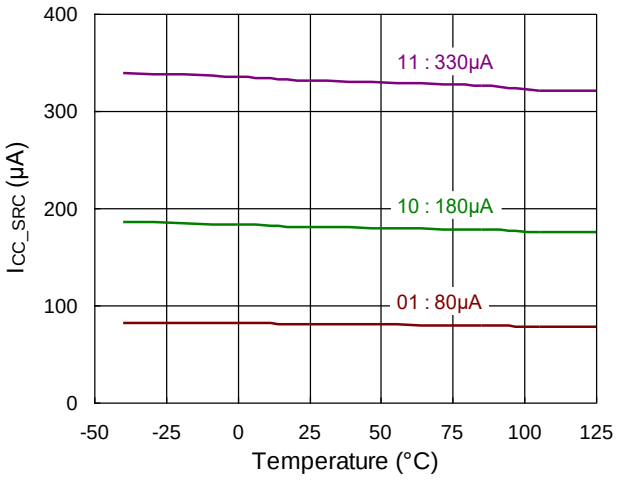




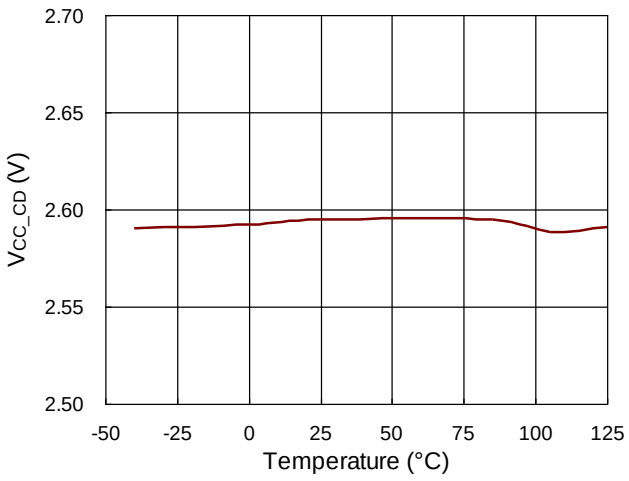




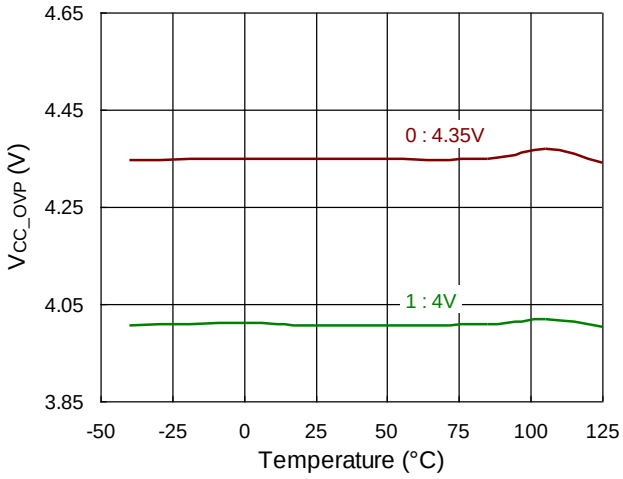
I_{CC_SRC} vs. Temperature



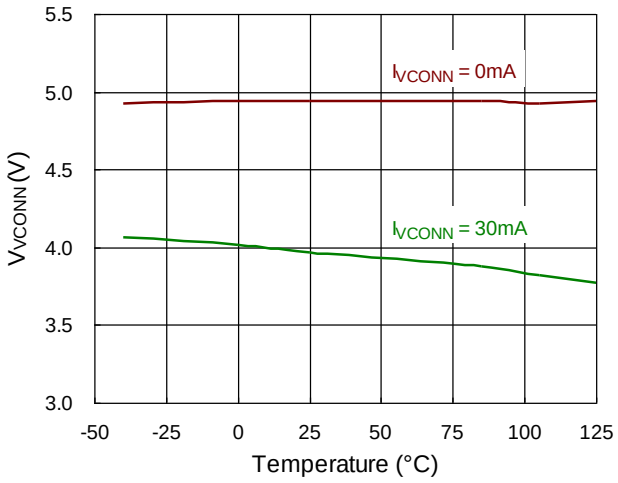
V_{CC_CD} vs. Temperature



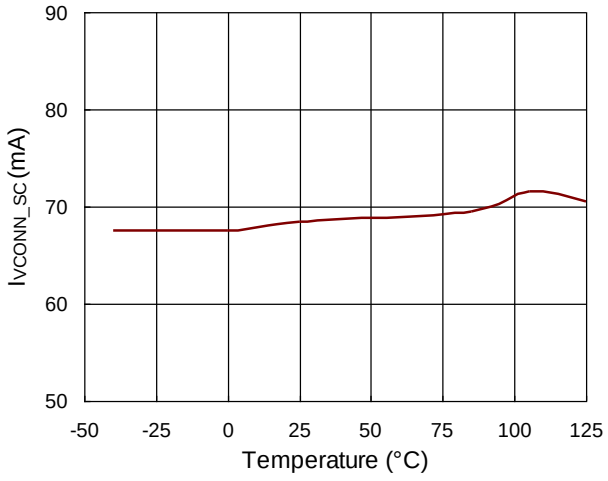
V_{CC_OVP} vs. Temperature



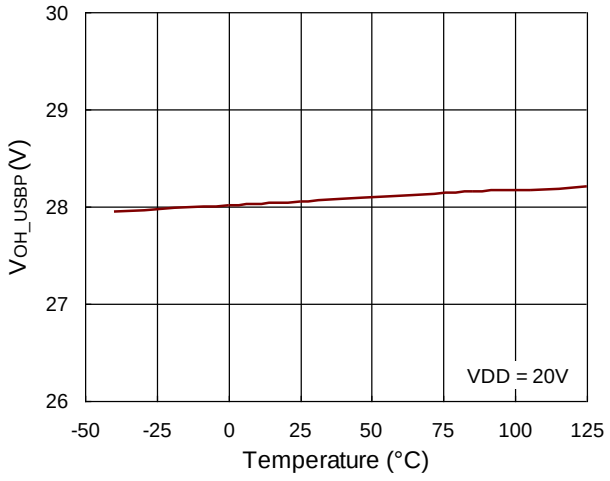
V_{VCONN} vs. Temperature

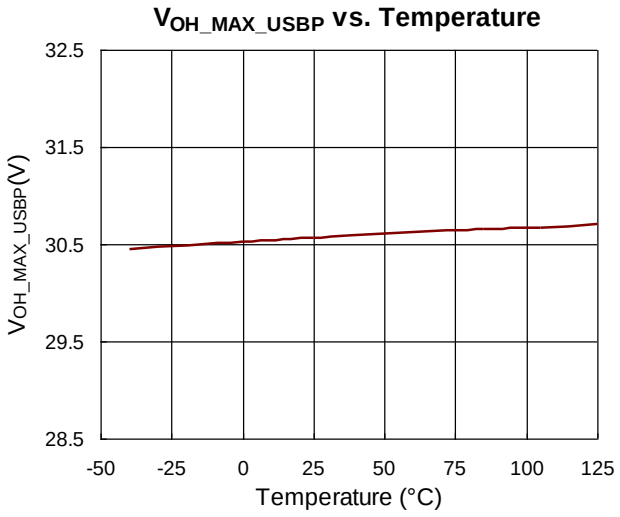


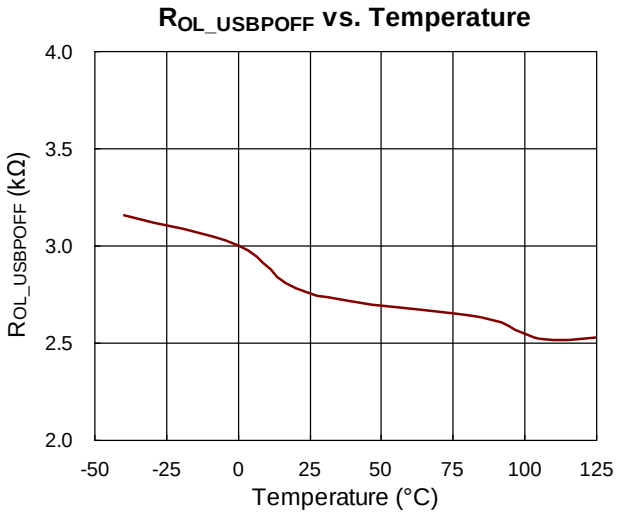
I_{VCONN_SC} vs. Temperature

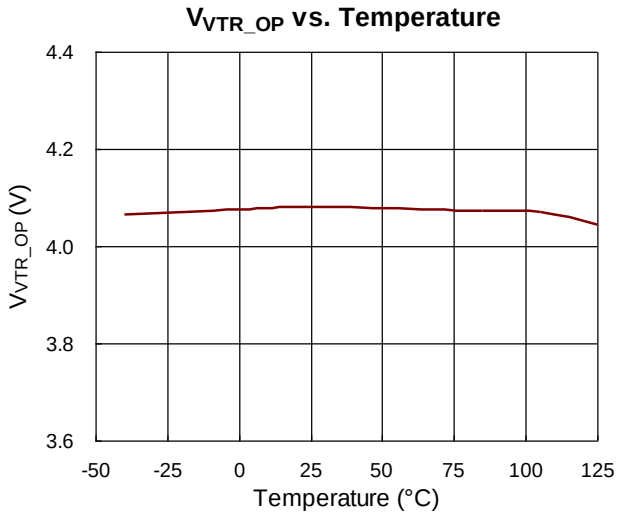


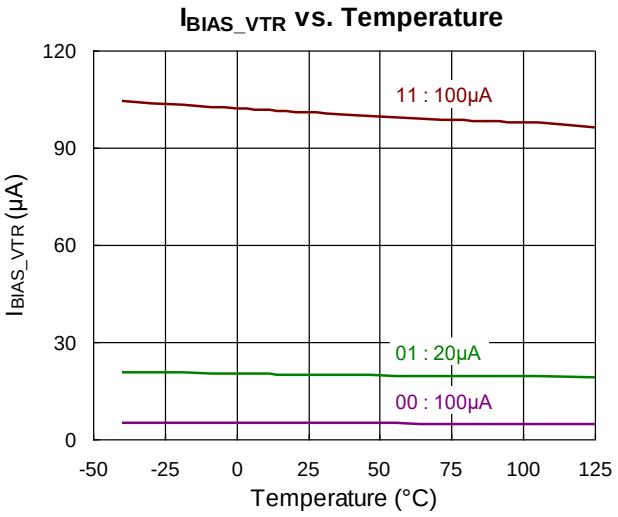
V_{OH_USBP} vs. Temperature











15 Operation

The RT7202KLC is a highly integrated programmable USB multi-protocol controller, providing various functions and comprehensive protections for the sink and source charging port.

15.1 Power Structure

The internal V5 and V2 regulated voltages, biased by VDD, of the RT7202KLC are used to supply the internal circuit and the internal microprocessor (MCU), respectively.

15.2 Current Sense Amplifier

To minimize the power loss of the current sense resistor, a low input offset amplifier with a voltage gain of 20 or 40 is used. When the 5mΩ (typical) R_{CS} is used with a voltage gain of 40, the resolution of the output current is around 5mA.

15.3 External Temperature Sensing

As shown in Figure 1, the RT7202KLC provides the RT pin as a register-programmable current source to bias a remote thermal sensor, such as a thermistor (NTC). If the RT voltage is below the over-temperature protection (OTP) threshold and the condition sustains for a programmed delay time, the OTP will be triggered.

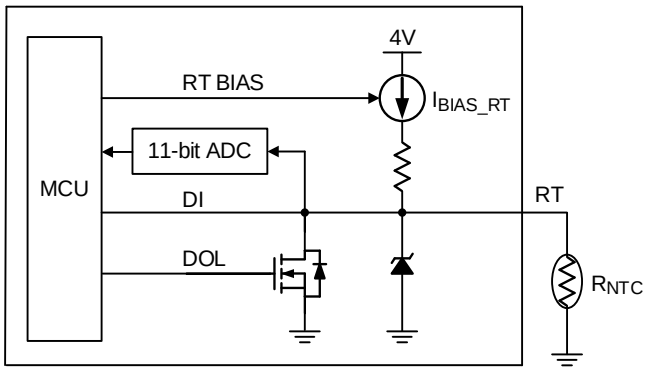


Figure 1. External Temperature Sensing

15.4 Open-Drain Driver of the VBUS Pin

Figure 2 shows the VBUS pin with the open-drain drivers. The internal bleeder circuit at VBUS pin is used to discharge the VBUS capacitor to Vsafe0V while cable is detached from a device. The VBUS pin voltage can be detected by ADC to achieve VBUS drop protection.

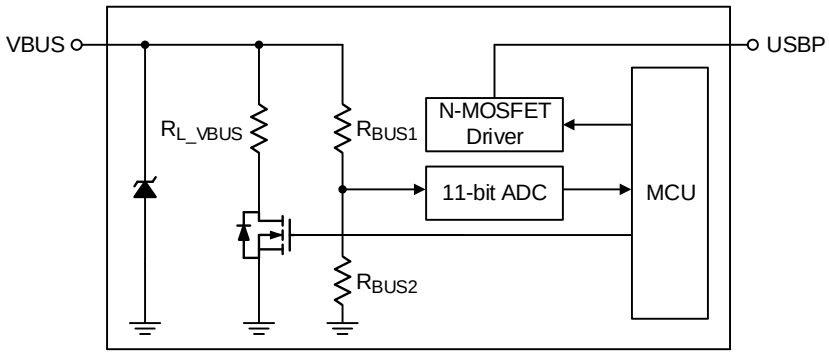


Figure 2. Open-Drain Driver of the VBUS Pin

15.5 Blocking N-MOSFET Control

The RT7202KLC provides a charge-pump driver for controlling an external blocking N-MOSFET, as shown in Figure 3. The blocking N-MOSFET can be quickly turned off in any fault condition. Once communication is established with a UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector is detected, the N-MOSFET will be turned on. If a VOUT overvoltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged. When VOUT is shorted to GND, the N-MOSFET will be turned off automatically and the output power will be limited.

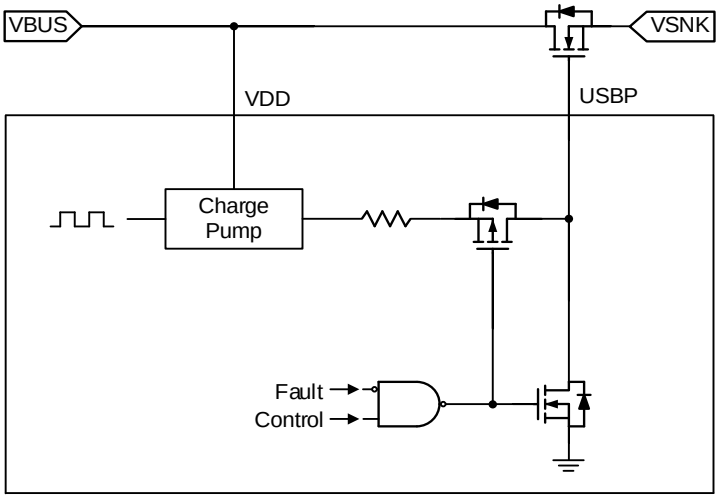


Figure 3. Blocking N-MOSFET Control

15.6 I²C Communication

The RT7202KLC provides slave I²C communication by connecting GPIO2 (SDA) and GPIO3 (SCL) to other MCU-based controllers that contain Master I²C. To identify the address, the RT7202KLC can be configured with programmable options by implementing a resistor from GPIO1 to GND.

16 Application Information

(Note 8)

16.1 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to- ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-24L 4x4 package, the thermal resistance, θ_{JA}, is 39.6°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (39.6°C/W) = 2.52W for a WQFN-24L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 4 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

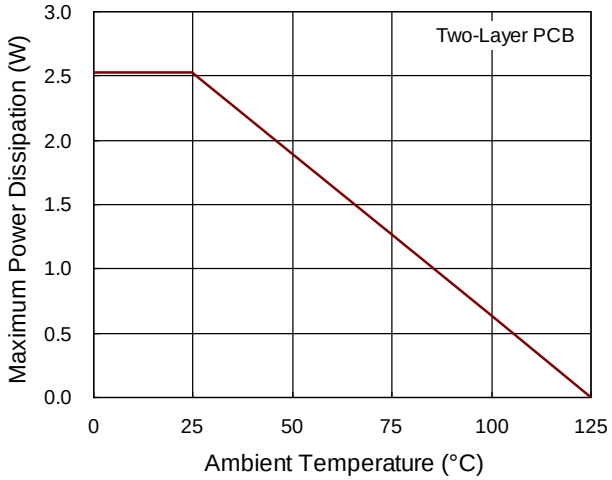
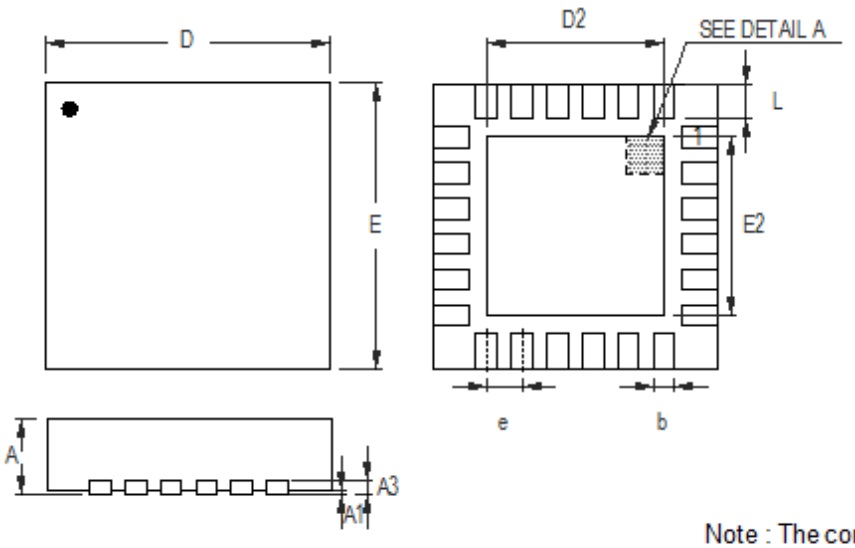
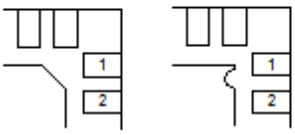


Figure 4. Derating Curve of Maximum Power Dissipation

Note 8. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

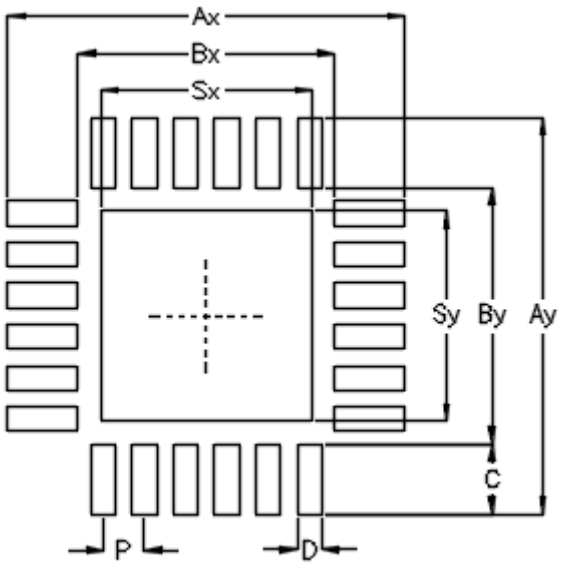
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.180	0.300	0.007	0.012
D		3.950	4.050	0.156	0.159
D2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
E		3.950	4.050	0.156	0.159
E2	Option 1	2.400	2.500	0.094	0.098
	Option 2	2.650	2.750	0.104	0.108
e		0.500		0.020	
L		0.350	0.450	0.014	0.018

W-Type 24L QFN 4x4 Package

Note 9. The package of the RT7202KLC uses Option 2.

18 Footprint Information

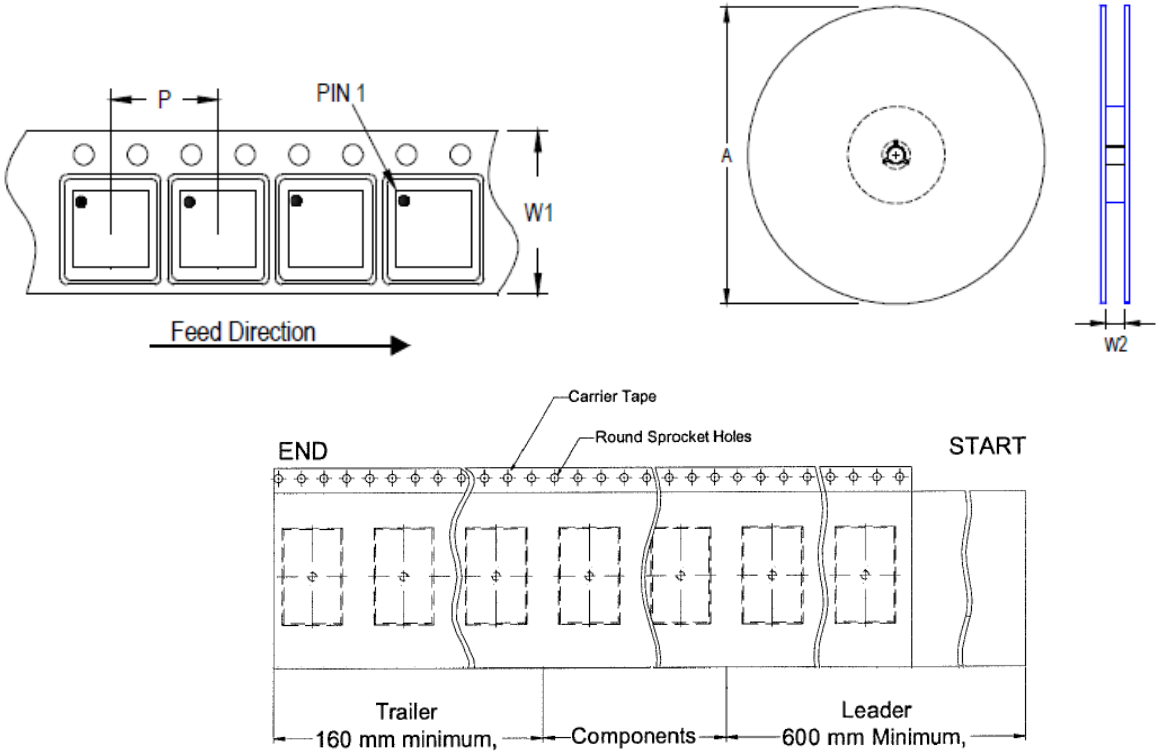


Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-24	Option1	24	0.50	4.80	4.80	3.10	3.10	0.85	0.30	2.55	2.55	±0.05
	Option2									2.60	2.60	

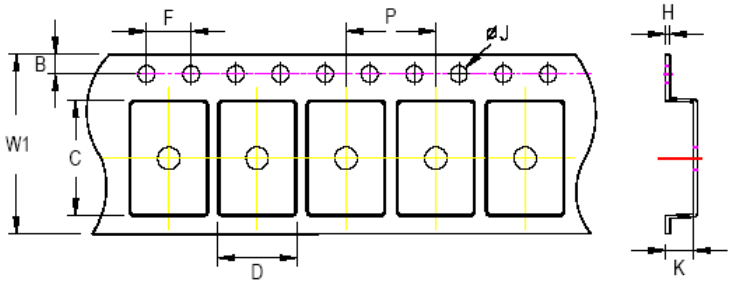
Note 10. The package of the RT7202KLC uses Option2.

19 Packing Information

19.1 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
00	2025/1/20	Final	*Packing Information on page 23, 24* - Updated packing information