Highly Integrated USB PD Type-C Controller for SMPS

1 General Description

The RT7202K is a simple yet flexible multipurpose of USB PD controller. By programming, it can operate as either a source or a sink.

When used as a source, it can be utilized in an off-line AC-DC converter, as it integrates a shunt regulator, constant voltage (CV) and constant current (CC) control loop with a programmable reference voltage to meet the Programmable Power Supply (PPS) specification. When combined with an external buck or buck-boost controller, it can constitute a DC-DC converter, such as a car charger, and also meet the PPS specification. When used as a sink, it is simple, low cost, yet flexible enough to request required power from a source. If using the RT7202KJ/KT/KS for a sink design, it has an I^2C interface and two GPIOs for flexible use and can be easily controlled by another MCU acting as the master.

The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 105°C.

2 Ordering Information

RT7202K□□□-□

- **Programmed Firmware Code AABBX**
  - AA: Application Code
  - BB: Model Code
  - X: Customer Approved Version Code
- **Package Type**(1)
  - QW: WQFN-16L 4x4 (W-Type) (RT7202KD/KJ/KT/KS)
  - S: SOP-10 (RT7202KE/KF/KH/KP)
- **Lead Plating System**
  - G: Richtek Green Policy Compliant(2)
- **RT7202K Version**
  - (Refer to Version Table)

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

3 Features

- **Protocol Support**
  - **USB PD 2.0 and 3.0 (PPS)**
- **Highly Integrated**
  - **Embedded MCU with a Mask-ROM of 24kB, an OTP-ROM of 8kB (RT7202KD/KE/KF) or 16kB (RT7202KH/KJ/KP/KT/KS), and an SRAM of 2kB**
  - **Embedded BMC Transceiver**
  - **Wide VDD Operation Range: 3V to 22V**
  - **Built-In Shunt Regulator for Constant-Voltage and Constant-Current Regulations**
  - **Built-In 10-bit Analog-to-Digital Converter (ADC)**
  - **Programmable Cable Compensation**
  - **The BLD Pin for Output Capacitor Quick Discharge (RT7202KD/KJ/KS)**
  - **The VDD Pin for Output Capacitor Quick Discharge (RT7202KE/KF/KH/KP/KT)**
  - **The USBP Pin for External Blocking N-MOSFET Direct Drive**
  - **Power-Saving Mode in Standby Mode**
- **Protection**
  - **Adaptive Overvoltage Protection**
  - **Adaptive Undervoltage Protection**
  - **Firmware-Programmable Overcurrent Protection**

4 Applications

- USB PD Type-C Chargers/Adapters for Smart Phones, NBs, Tablets and All Other Electronics
- USB PD Extension Cores with Offline AC-DC Converters

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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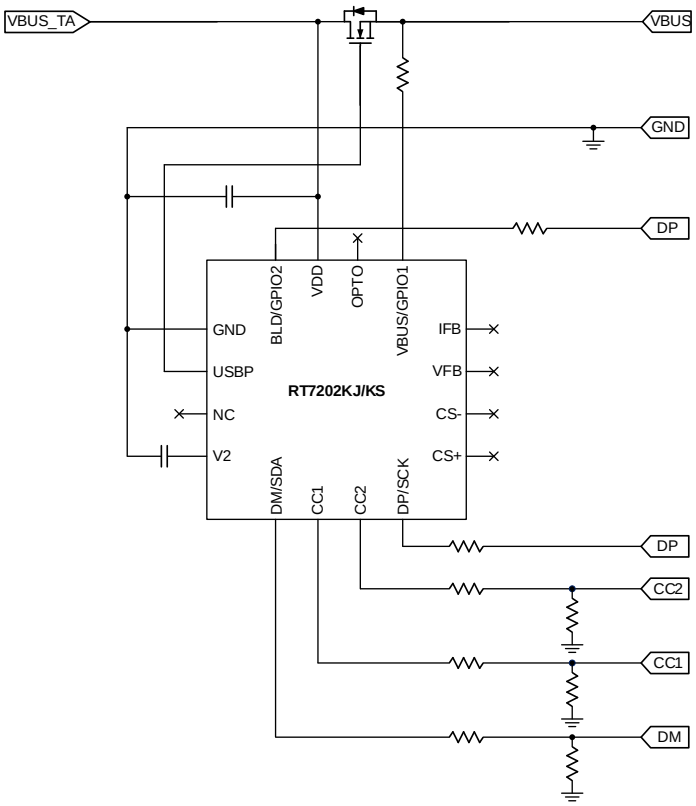
6 RT7202K Version Table

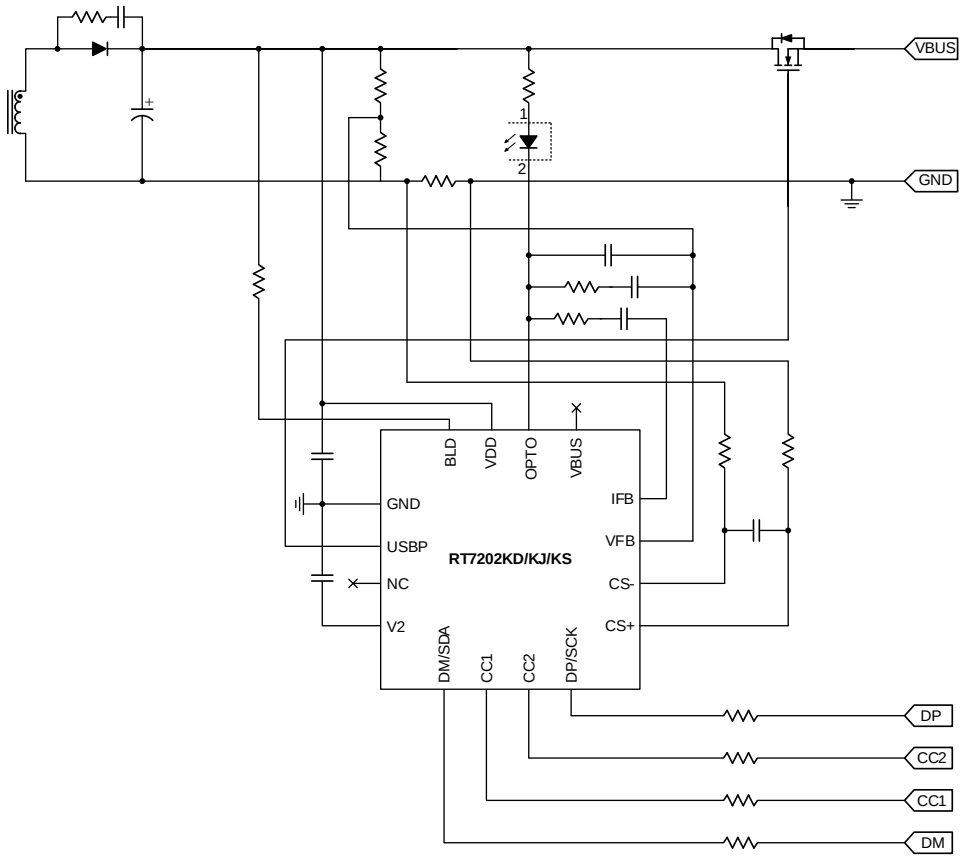
Version	RT7202KD	RT7202KE	RT7202KF	RT7202KH	RT7202KJ	RT7202KP	RT7202KT	RT7202KS
Output Voltage Supported	3V to 22V	3V to 22V	3V to 22V	3V to 22V	3V to 22V	3V to 22V	3V to 22V	3V to 22V
V_{OUT} Scaling Factor R_{FB2} / (R_{FB1} + R_{FB2})	1/10	1/10	1/10	1/10	1/10	1/10	1/10	1/10
DP/DM Pin	O	X	DM only	X	O	DM only	O	O
Blocking MOSFET Driver	N-MOSFET	N-MOSFET	N-MOSFET	N-MOSFET	N-MOSFET	N-MOSFET	N-MOSFET	N-MOSFET
IFB Pin	O	O	X	X	O	X	O	O
VBUS Pin	O	X	X	X	O	X	O	O
BLD Pin	O	X	X	X	O	X	X	O
Built-in FB Resistors	X	X	X	O	X	X	O	X
OTP ROM	8kB	8kB	8kB	16kB	16kB	16kB	16kB	16kB
Maximum Constant Discharge Current	120mA (BLD Pin)	120mA (VDD Pin)	120mA (VDD Pin)	120mA (VDD Pin)	120mA (BLD Pin)	120mA (VDD Pin)	180mA (VDD Pin)	180mA (BLD Pin)

7 Simplified Application Circuit

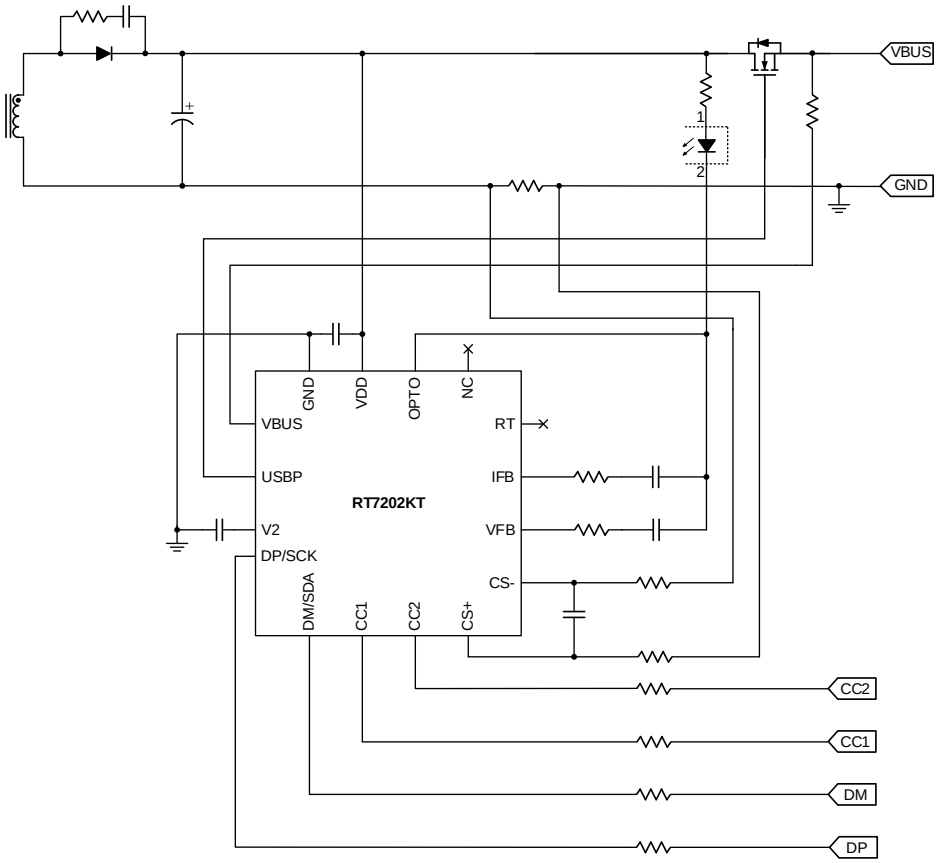
7.1 The RT7202KJ/KS Simplified Application Circuit for Sink Side



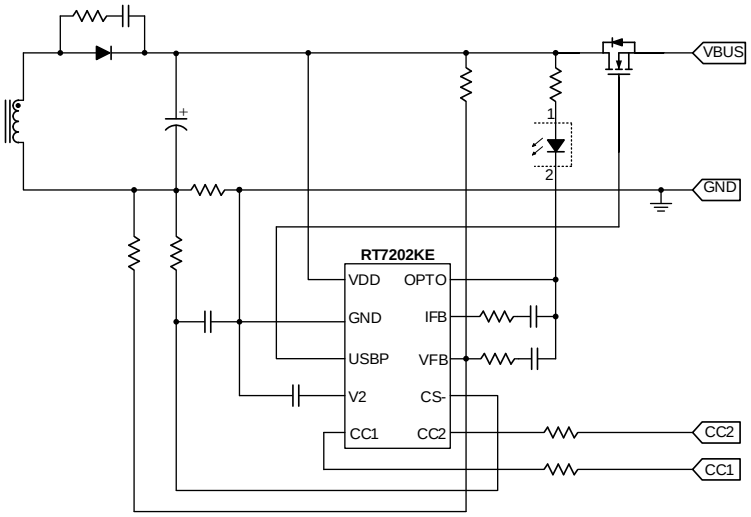
7.2 The RT7202KD/KJ/KS Simplified Application Circuit for Source Side



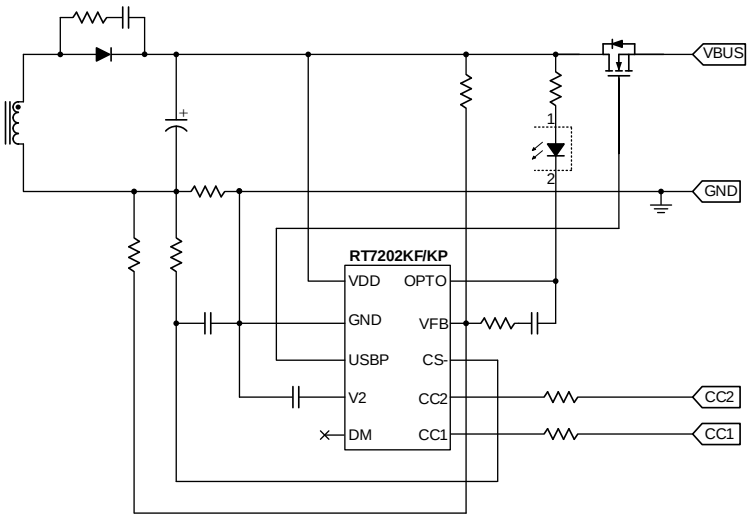
7.3 The RT7202KT Simplified Application Circuit for Source Side



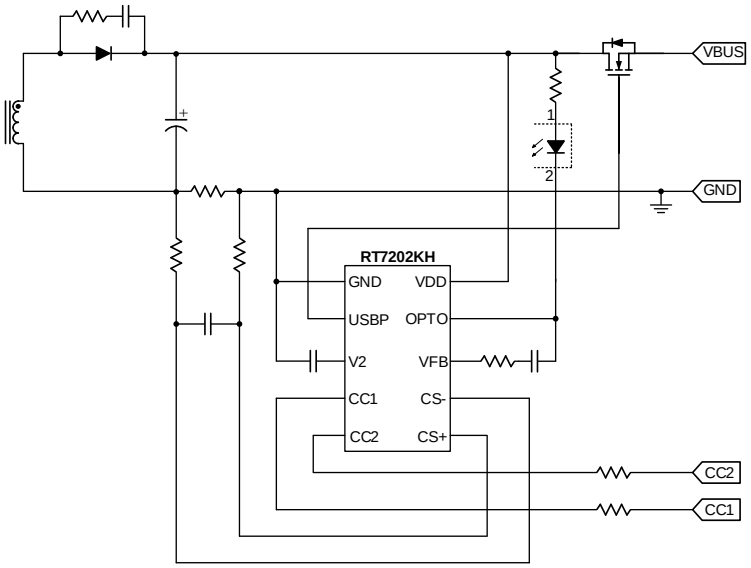
7.4 The RT7202KE Simplified Application Circuit for Source Side



7.5 The RT7202KF/KP Simplified Application Circuit for Source Side

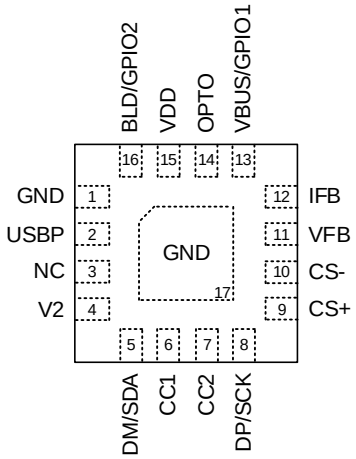


7.6 The RT7202KH Simplified Application Circuit for Source Side

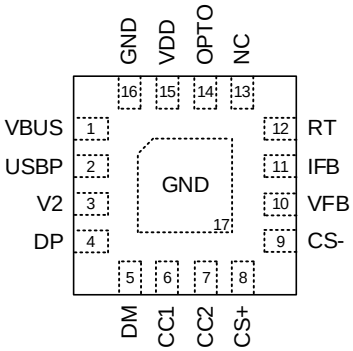


8 Pin Configuration

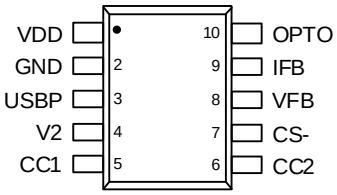
(TOP VIEW)



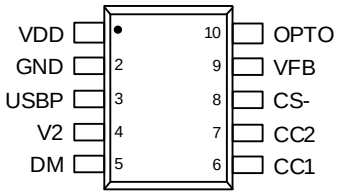
WQFN-16L 4x4 (RT7202KD/KJ/KS)



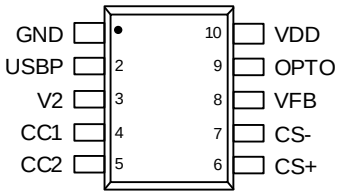
WQFN-16L 4x4 (RT7202KT)



SOP-10 (RT7202KE)



SOP-10 (RT7202KF/KP)



SOP-10 (RT7202KH)

9 Functional Pin Description

9.1 For the RT7202KD/KJ/KS

Pin No.	Pin Name	Type	Pin Function
1, 17 (Exposed Pad)	GND	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2	USBP	D IO	Control signal of the blocking N-MOSFET.
3	NC	--	No internal connection.
4	V2	PWR	Regulated DC bias to supply power to the MCU.
5	DM/SDA	A/D IO	USB DM channel. Can be configured as ADC input.
6	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
7	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
8	DP/SCK	A/D IO	USB DP channel. Can be configured as ADC input.
9	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
10	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
11	VFB	AI	Feedback input for the constant-voltage loop.
12	IFB	AI	Feedback input for the constant-current loop.
13	VBUS/GPIO1	A IO	Over-voltage fault indication output, used to pull low an optocoupler. Can be configured as ADC input.
14	OPTO	AO	Current sink output for optocoupler connection. Can be configured as ADC input.
15	VDD	PWR	Supply input voltage.
16	BLD/GPIO2	D IO	Bleeder connection node to provide another path to discharge the output capacitor.

9.2 For the RT7202KE

Pin No.	Pin Name	Type	Pin Function
1	VDD	PWR	Supply input voltage.
2	GND	GND	Ground.
3	USBP	D IO	Control signal of the blocking N-MOSFET.
4	V2	PWR	Regulated DC bias to supply power to the MCU.
5	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
6	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
7	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
8	VFB	AI	Feedback input for the constant-voltage loop.

Pin No.	Pin Name	Type	Pin Function
9	IFB	AI	Feedback input for the constant-current loop.
10	OPTO	AO	Current sink output for optocoupler connection. Can be configured as ADC input.

9.3 For the RT7202KF/KP

Pin No.	Pin Name	Type	Pin Function
1	VDD	PWR	Supply input voltage.
2	GND	GND	Ground.
3	USBP	D IO	Control signal of the blocking N-MOSFET.
4	V2	PWR	Regulated DC bias to supply power to the MCU.
5	DM	A/D IO	USB DM channel. Can be configured as ADC input.
6	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
7	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
8	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
9	VFB	AI	Feedback input for the constant-voltage loop.
10	OPTO	AO	Current sink output for optocoupler connection. Can be configured as ADC input.

9.4 For the RT7202KH

Pin No.	Pin Name	Type	Pin Function
1	GND	GND	Ground.
2	USBP	D IO	Control signal of the blocking N-MOSFET.
3	V2	PWR	Regulated DC bias to supply power to the MCU.
4	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
5	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
6	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
7	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
8	VFB	AI	Feedback input for the constant-voltage loop.
9	OPTO	AO	Current sink output for optocoupler connection. Can be configured as ADC input.
10	VDD	PWR	Supply input voltage.

9.5 For the RT7202KT

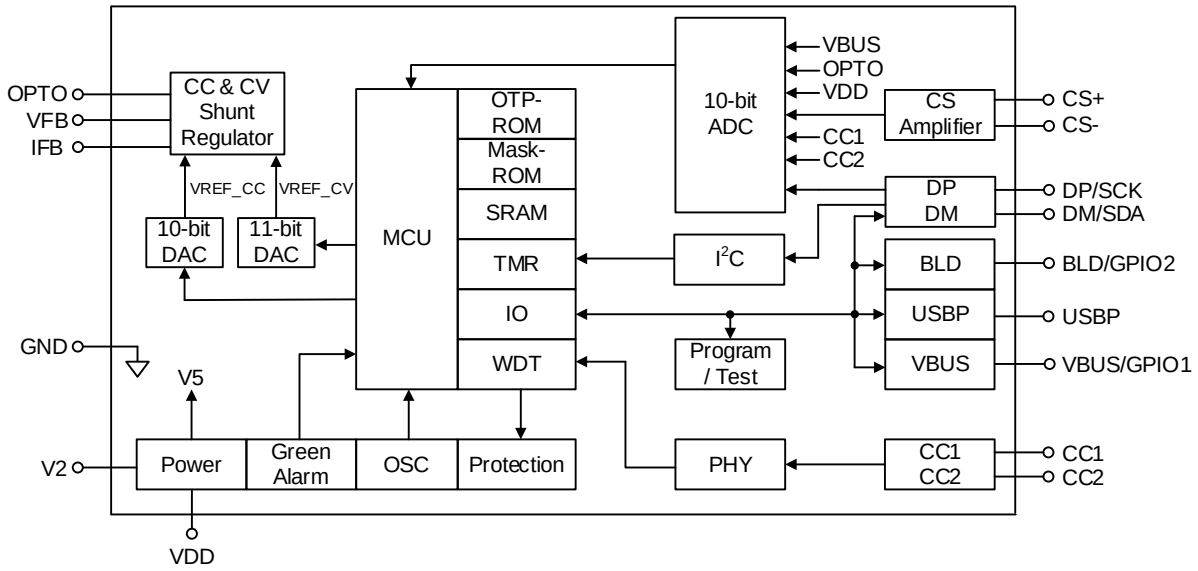
Pin No.	Pin Name	Type	Pin Function
1	VBUS	D I	To provide the path to discharge the VBUS capacitor or thermal sensor connection node for over-temperature protection.
2	USBP	D IO	Control signal of the blocking N-MOSFET.
3	V2	PWR	Regulated DC bias to supply power to the MCU.
4	DP	A/D IO	USB DM channel. Can be configured as ADC input and I^2C-SCL.
5	DM	A/D IO	USB DM channel. Can be configured as ADC input and I^2C-SDA.
6	CC1	A/D IO	Type-C connector Configuration Channel (CC) 1. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
7	CC2	A/D IO	Type-C connector Configuration Channel (CC) 2. It is used to detect a cable plug event and determine the cable orientation. Can be configured as ADC input.
8	CS+	AI	Positive input of a current-sense amplifier for output current sensing.
9	CS-	AI	Negative input of a current-sense amplifier for output current sensing.
10	VFB	AI	Feedback input for the constant-voltage loop.
11	IFB	AI	Feedback input for the constant-current loop.
12	RT	A/D IO	Remote thermal sensor connection node for over-temperature protection. Can be configured as ADC input.
13	NC	--	No internal connection.
14	OPTO	AO	Current sink output for optocoupler connection. Can be configured as ADC input.
15	VDD	PWR	Supply input voltage.
16, 17 (Exposed Pad)	GND	GND	Bleeder connection node to provide another path to discharge the output capacitor.

9.6 IO Type Definition

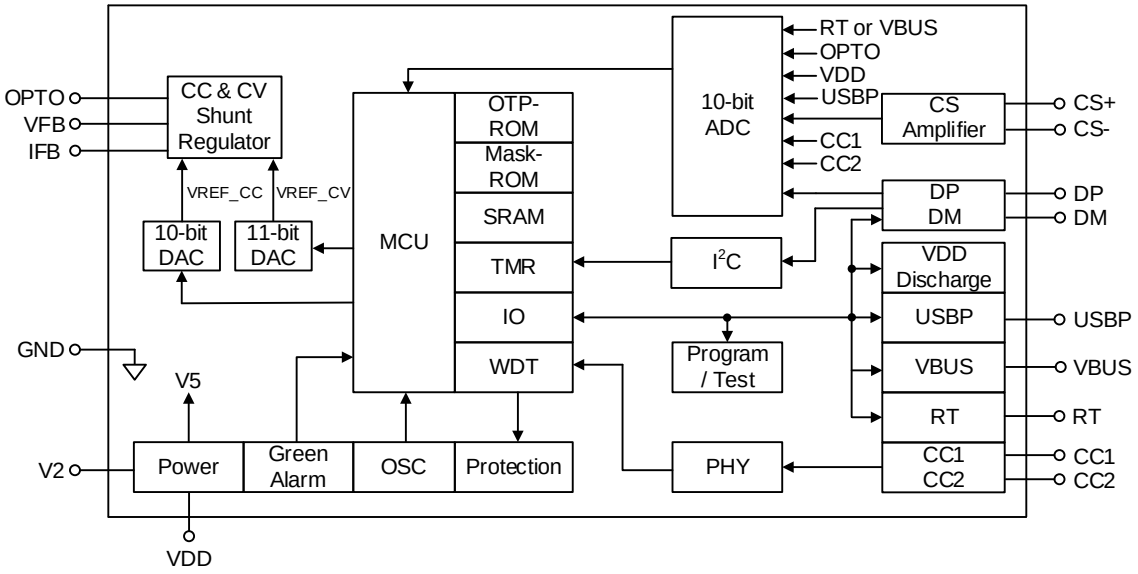
- PWR: Power Pin
- GND: Ground Pin
- AI: Analog Input Pin
- AO: Analog Output Pin
- A IO: Analog Input/Output Pin
- D I: Digital Input Pin
- D IO: Digital Input/Output Pin
- A/D IO: Analog/Digital Input/Output Pin

10 Functional Block Diagram

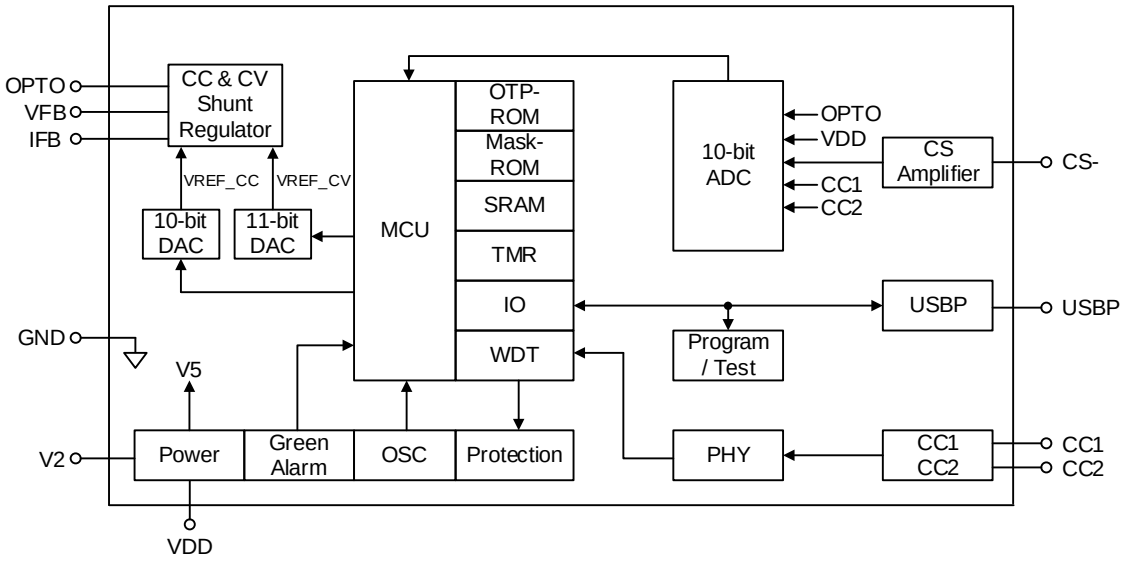
10.1 For the RT7202KD/KJ/KS



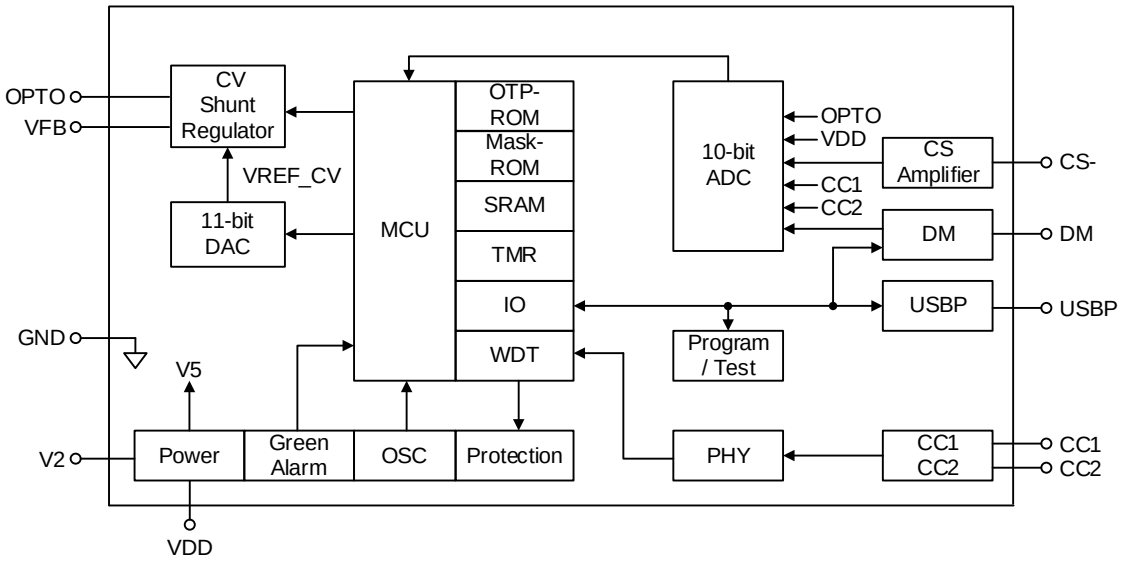
10.2 For the RT7202KT



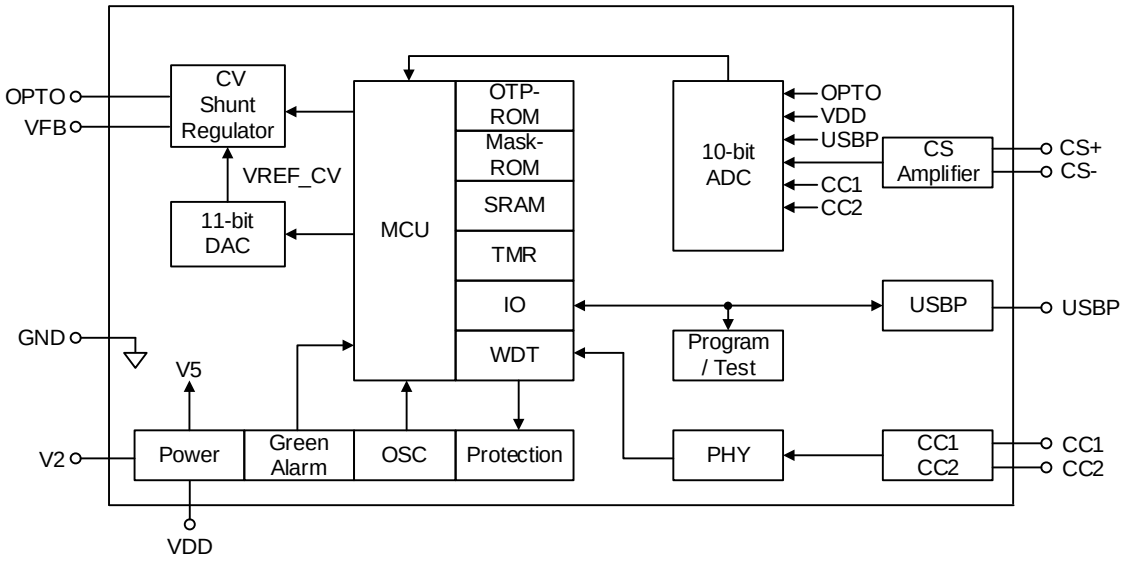
10.3 For the RT7202KE



10.4 For the RT7202KF/KP



10.5 For the RT7202KH



11 Absolute Maximum Ratings

(Note 2)

- USBP to GND ---------- –0.3V to 32V
- VDD, OPTO, BLD/GPIO2, RT, VBUS/GPIO1 to GND ---------- –0.3V to 28V
- CC1, CC2 to GND ---------- –0.3V to 22V
- VFB, IFB, DP, DM, CS+, CS- to GND ---------- –0.3V to 7V
- V2 to GND ---------- –0.3V to 2.5V
- Power Dissipation, P_D @ T_A = 25°C

  WQFN-16L 4x4 ---------- 0.39W

  SOP-10 ---------- 0.51W
- Package Thermal Resistance (Note 3)

  WQFN-16L 4x4, θ_{JA} ---------- 256.4°C/W

  WQFN-16L 4x4, θ_{JC} ---------- 7°C/W

  SOP-10, θ_{JA} ---------- 194.2°C/W

  SOP-10, θ_{JC} ---------- 36.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity single-layer test board on a JEDEC 51-3 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VDD ---------- 3V to 22V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 105°C

Note 5. The device is not guaranteed to function outside its operating conditions.

13 Electrical Characteristics

(T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
VDD Section							
VDD Turn-On Threshold Voltage	V_{VDD_ON}			2.9	3.05	3.2	V
VDD Turn-Off Threshold Voltage	V_{VDD_OFF}			2.7	2.75	2.8	V
VDD Turn-On/-Off Hysteresis	V_{VDD_HYS}			0.2	0.3	0.4	V
VDD Start-Up Current	I_{DD_START}	V_{DD} = 2.6V		100	200	300	µA
VDD Operating Current	I_{DD_OP}			4	6	8	mA
VDD Sleep-Mode Current	I_{DD_SLEEP}	In sleep mode		400	550	750	µA
VDD Overvoltage Protection Threshold Voltage	V_{VDD_OVP}			23	24	25	V
VDD Overvoltage Protection Deglitch Time	t_{D_VDDOVP}	(Note 6)		25	50	90	µs
		(For RT7202KT) (Note 6)		15	30	45	
Register-Programmable Overvoltage Protection Threshold	V_{VOUT_OVP}	Ratio of V_{REF_CV}		109.25	115	120.75	%
				114	120	126	
				118.75	125	131.25	
				Disable			**%**
		Ratio of V_{REF_CV} (For RT7202KT)		105.45	111	116.55	
				109.25	115	120.75	
				114	120	126	
				118.75	125	131.25	
				Disable			
Register- Programmable VDD Undervoltage Wake-Up Threshold	$V_{DD\_UV\_WK}$		0	85.5	90	94.5	%
			1	80.75	85	89.25	
VDD Undervoltage Protection Deglitch Time	$t_{D\_VDD\_UV}$	(Note 6)		--	50	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Register-Programmable VDD Discharge Current	I_{DD_DISCH}	(For RT7202KE/KF/KH/KP)	15	30	45	mA
			40	60	80	
			63	90	117	
			84	120	156	
		(For RT7202KT)	15	30	45	
			40	60	80	
			63	90	117	
			84	120	156	
			105	150	195	
			126	180	234	
MCU Operating Frequency	f_{OSC_MCU}	V_{DD} = 5V	20.5	21.6	22.7	MHz
Internal Bias						
V2	V_{BIAS_V2}	3V < V_{DD} < 25V	1.71	1.80	1.89	V
V2 Output Short-Circuit Current	I_{V2_SC}		30	50	70	mA
Regulator Section						
Internal Resistor between VFB and VDD	R_{FB1}	(For RT7202KH/KT)	144	180	216	kΩ
Internal Low-Side VFB Resistor	R_{FB2}	(For RT7202KH/KT)	16	20	24	kΩ
V_{OUT} Scaling Factor	K_{VOUT}	(R_{FB1} + R_{FB2}) / R_{FB2} (For RT7202KH/KT)	9.9	10	10.1	--
Default Reference Voltage for Standby CV Regulators	$V_{ST\_REF\_CV}$		0.485	0.5	0.515	V
Minimum DAC Output Voltage for CV Regulators	$V_{DAC\_MIN\_CV}$	11-bit D/A conversion	0.147	0.15	0.153	V
Maximum DAC Output Voltage for CV Regulators	$V_{DAC\_MAX\_CV}$	11-bit D/A conversion	2.178	2.2	2.222	V
Maximum DAC Output Voltage for CC Regulators	$V_{DAC\_MAX\_CC}$	10-bit Digital-to-Analog converter	1.485	1.5	1.515	V
Maximum ADC Sense Voltage	V_{ADC_MAX}	10-bit A/D conversion	2.178	2.2	2.222	V
Ratio of Change in Reference Input Voltage to Change in OPTO Voltage	$\frac{\Delta V_{REF}}{\Delta V_{OPTO}}$	ΔV_{OPTO} = 25V to V_{REF} (Note 6)	–2.4	–1.2	–0.1	mV/V
Reference Input Current	I_{REF}	(Note 6)	0.01	0.1	1	μA
Off-State OPTO Current	I_{OPTO_OFF}	OPTO is open (Note 6)	0.1	230	500	nA
Dynamic Impedance	$\lvert Z_{OPTO} \rvert$	V_{OPTO} = V_{REF}, I_{OPTO} = 1mA, at 1kHz (Note 6)	0.1	0.22	0.5	Ω
OPTO Turn-On Impedance	R_{ON_OPTO}	I_{OPTO_SINK} = 10mA (Note 6)	30	70	150	Ω
Maximum OPTO Sinking Current	I_{OPTO_MAX}		2	--	20	mA

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Internal Resistor between OPTO and VDD	R_{OPTO_VDD}			40.8	51	61.2	kΩ
Internal Resistor between OPTO and GND	R_{OPTO_GND}			50	60	70	kΩ
Internal Sinking Current Source	I_{SINK_OPTO}	During VDD UVLO, I_{SINK_OPTO} will be shorted.		20	25	30	μA
VBUS Section (For RT7202KD/KJ/KT/KS)							
Maximum VBUS Sinking Current	I_{VBUS_MAX}			2	--	20	mA
Pull-Low Impedance	R_{L_VBUS}	I_{VBUS_SINK} = 10mA (Note 6)		40	70	150	Ω
Open-Loop Voltage	V_{VBUS_OP}	V_{DD} = 5V (register selection)		3.2	3.6	4	V
Register-Programmable Internal Bias Current	I_{BIAS_VBUS}	Register selection	0	Open-Drain			μA
			1	90	100	110	
RT Section (For RT7202KT)							
Open-Loop Voltage	V_{RT_OP}	V_{DD} = 5V		3.2	3.6	4	V
Register-Programmable Internal Bias Current	I_{BIAS_RT}		0	Open-Drain			μA
			1	90	100	110	
BLD Section (For RT7202KD/KJ/KS)							
Maximum BLD Sinking Current	I_{BLD_MAX}	In 300ms		0.23	--	0.32	A
Pull-Low Impedance	R_{L_BLD}	(Note 6)		20	30	40	Ω
Register-Programmable BLD Discharge Current	I_{BLD_DISCH}	(For RT7202KD/KJ)		15	30	45	mA
				40	60	80	
				63	90	117	
				84	120	156	
		(For RT7202KS)		15	30	45	
				40	60	80	
				63	90	117	
				84	120	156	
				105	150	195	
				126	180	234	
Current Sense Amplifier							
Register-Programmable Current-Sense Voltage Gain	K_{CS}		0	19.8	20	20.2	V/V
			1	39.6	40	40.4	
Current-Sense Amplifier Output Offset Voltage	V_{OFFSET_CS}			0.36	0.4	0.44	V
Unit Gain Bandwidth		(Note 6)		1000	--	5000	kHz
Output Current		(Note 6)		0.07	0.1	0.13	mA

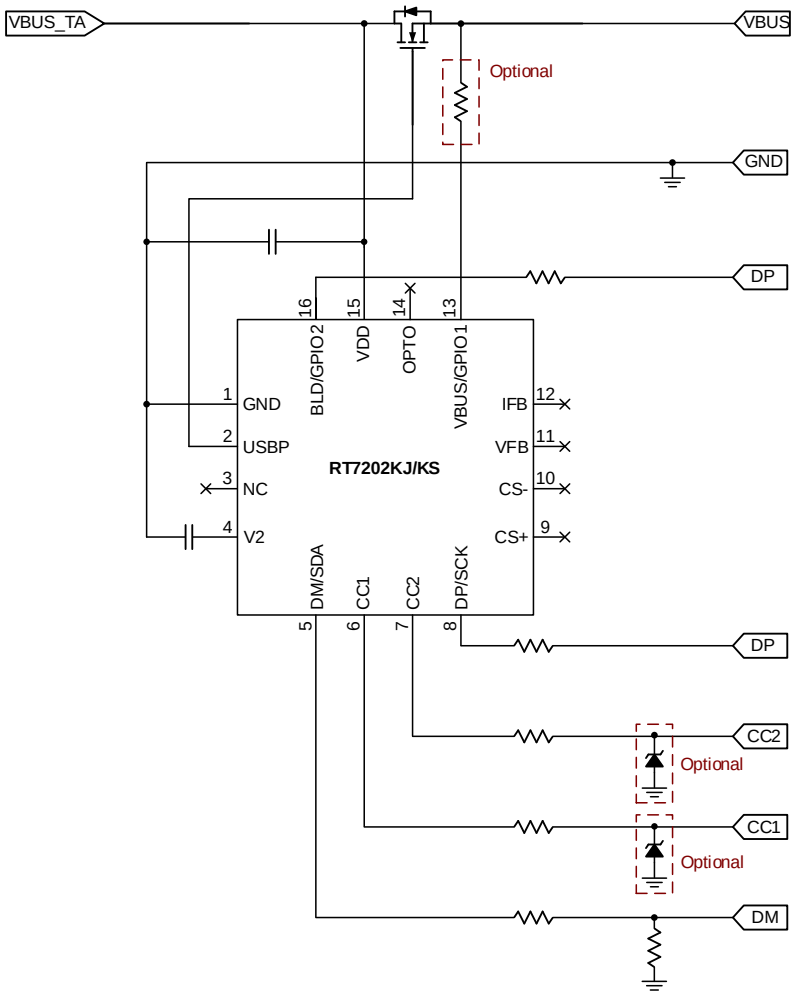
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
DP and DM Section (For RT7202KD/KF/KJ/KP/KS)							
Pull-High Resistor	R_{H_DPDM}			5	10	15	kΩ
Pull-Low Resistor	R_{L_DPDM}			15	20	25	kΩ
Register-Programmable Output High Voltage	V_{OH_OD}	V_{DD} = 5V, R_{Load} = 15kΩ	00	Open-Drain			V
	$V_{OH\_3.3V}$		01	2.97	3.3	3.63	
	$V_{OH\_1.8V}$		10	1.62	1.8	1.98	
	$V_{OH\_4.2V}$		11	3.78	4.2	4.62	
Output Low Voltage	V_{OL_OD}	R_{Load} = 15kΩ		0.01	--	0.2	V
	$V_{OL\_3.3V}$						
	$V_{OL\_1.8V}$						
	$V_{OL\_4.2V}$						
Register-Programmable Input High Trip Voltage	V_{IH_DPDM}		00	0.7	0.8	0.9	V
			01	1.3	1.4	1.5	
			10	1.8	1.9	2.0	
			11	2.0	2.1	2.2	
Register-Programmable Input Low Trip Voltage	V_{IL_DPDM}		00	0.5	0.6	0.7	V
			01	1.0	1.1	1.2	
			10	1.7	1.8	1.9	
			11	1.8	1.9	2.0	
DPDM Switch On-Resistance	R_{ON_DPDM}			20	30	40	Ω
Register-Programmable Internal Bias Current	I_{BIAS_DPDM}		0	Disable			µA
			1	90	100	110	
I^2C Section							
SCL Clock Rate	f_{SCL}	(Note 6)		--	--	100	kHz
Hold Time for a Repeated START Condition	$t_{HD;STA}$	(Note 6)		4	--	--	µs
Low Period of the SCL Clock	t_{LOW}	(Note 6)		4.7	--	--	µs
High Period of the SCL Clock	t_{HIGH}	(Note 6)		4	--	--	µs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	(Note 6)		4.7	--	--	µs
Data Hold Time	$t_{HD;DAT}$	(Note 6)		0	--	--	µs
Data Set-Up Time	$t_{SU;DAT}$	(Note 6)		0.25	--	--	µs
Set-Up Time for STOP Condition	$t_{SU;STO}$	(Note 6)		4	--	--	µs
Bus Free Time between a STOP and a START Condition	t_{BUF}	(Note 6)		3	--	--	µs
Rising Time of Both SDA/SCL Signals	t_R	(Note 6)		--	--	1	µs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Falling Time of Both SDA/SCL Signals	t_F	(Note 6)		--	--	0.3	μs
CC1 and CC2 Section							
Output High Voltage	V_{OH_CC}			1.05	1.125	1.2	V
Output Low Voltage	V_{OL_CC}			0	0.0375	0.075	V
Register-Programmable Input High Trip Voltage	V_{IH_CC}		00	0.7	0.8	0.9	V
			01	0.6	0.7	0.8	
			10	0.5	0.6	0.7	
			11	0.4	0.5	0.6	
		(For RT7202KS)	00	0.4	0.5	0.6	
			01	0.5	0.6	0.7	
			10	0.2	0.3	0.4	
			11	0.7	0.8	0.9	
Register-Programmable Input Low Trip Voltage	V_{IL_CC}		00	0.4	0.5	0.6	V
			01	0.3	0.4	0.5	
			10	0.2	0.3	0.4	
			11	0.1	0.2	0.3	
		(For RT7202KS)	00	0.2	0.3	0.4	
			01	0.3	0.4	0.5	
			10	0.1	0.2	0.3	
			11	0.6	0.7	0.8	
Rising Time	t_{R_CC}	C_{Load} = 470pF		300	--	700	ns
Falling Time	t_{F_CC}	C_{Load} = 470pF		300	--	700	ns
Register-Programmable Sourcing Current	I_{CC_SRC}		00	High Impedance			μA
			01	72	80	88	
			10	166	180	194	
			11	304	330	356	
USBP Section							
Output High Voltage	V_{OH_USBP}			VDD + 6.5	VDD + 8	VDD + 9.5	V
Maximum Output High Voltage	V_{MAX_USBP}			26.5	28	29.5	V
Register-Programmable Rising Time	t_{R_USBP}	C_{Load} = 4nF, V_{DD} = 5V, from 20% to 80%	00	200	300	400	μs
			01	480	600	720	
			10	980	1200	1440	
			11	1920	2400	2880	
Output Low Voltage	V_{OL_USBP}	V_{DD} = 3V, I_{USBP} = 100μA before start-up		0.1	0.5	1	V
Falling Time	t_{F_USBP}	C_{Load} = 4nF, V_{DD} = 5V, from 90% to 10%		0.4	1	2	μs

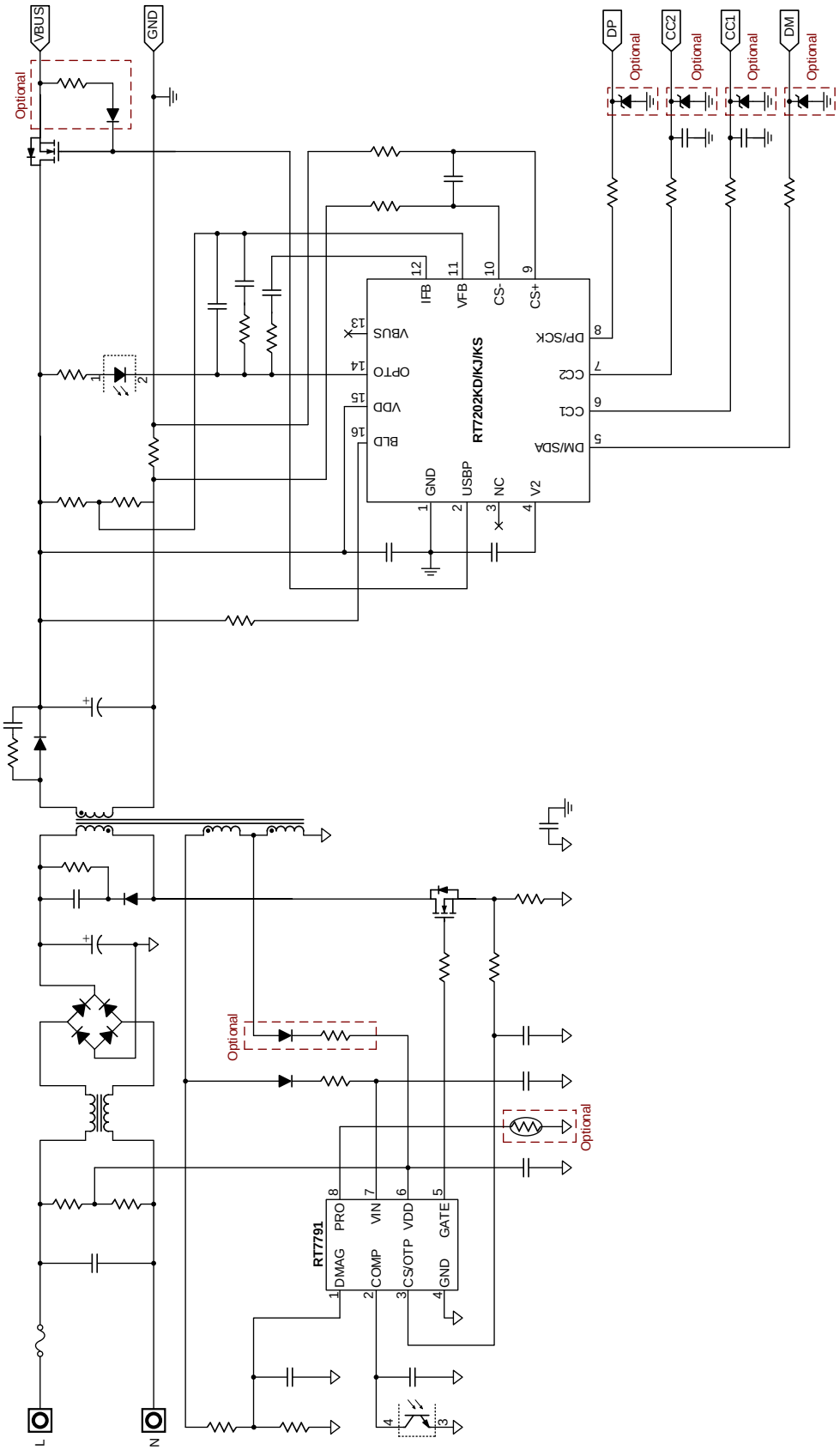
Note 6. Guaranteed by design.

14 Typical Application Circuit

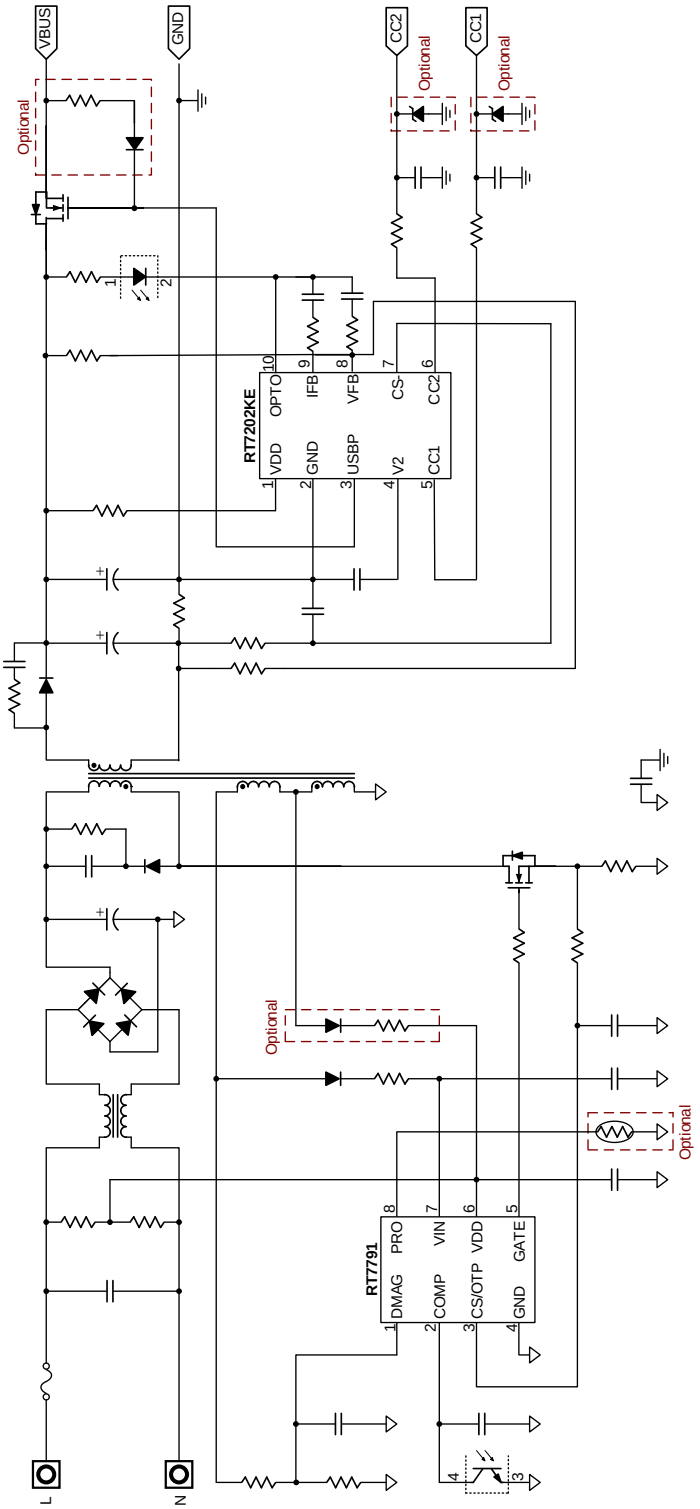
14.1 The RT7202KJ/KS Typical Application Circuit for Sink Side



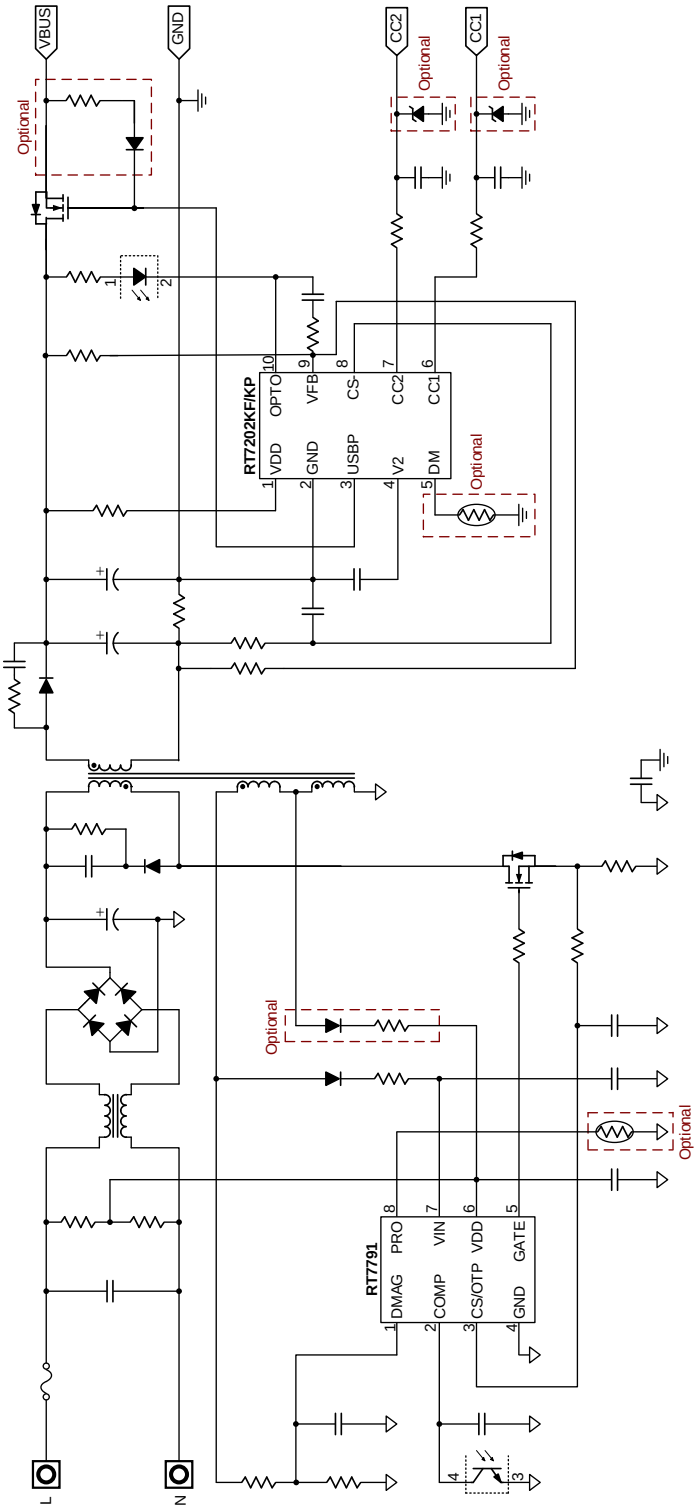
14.2 The RT7202KD/KJ/KS Typical Application Circuit for Source Side



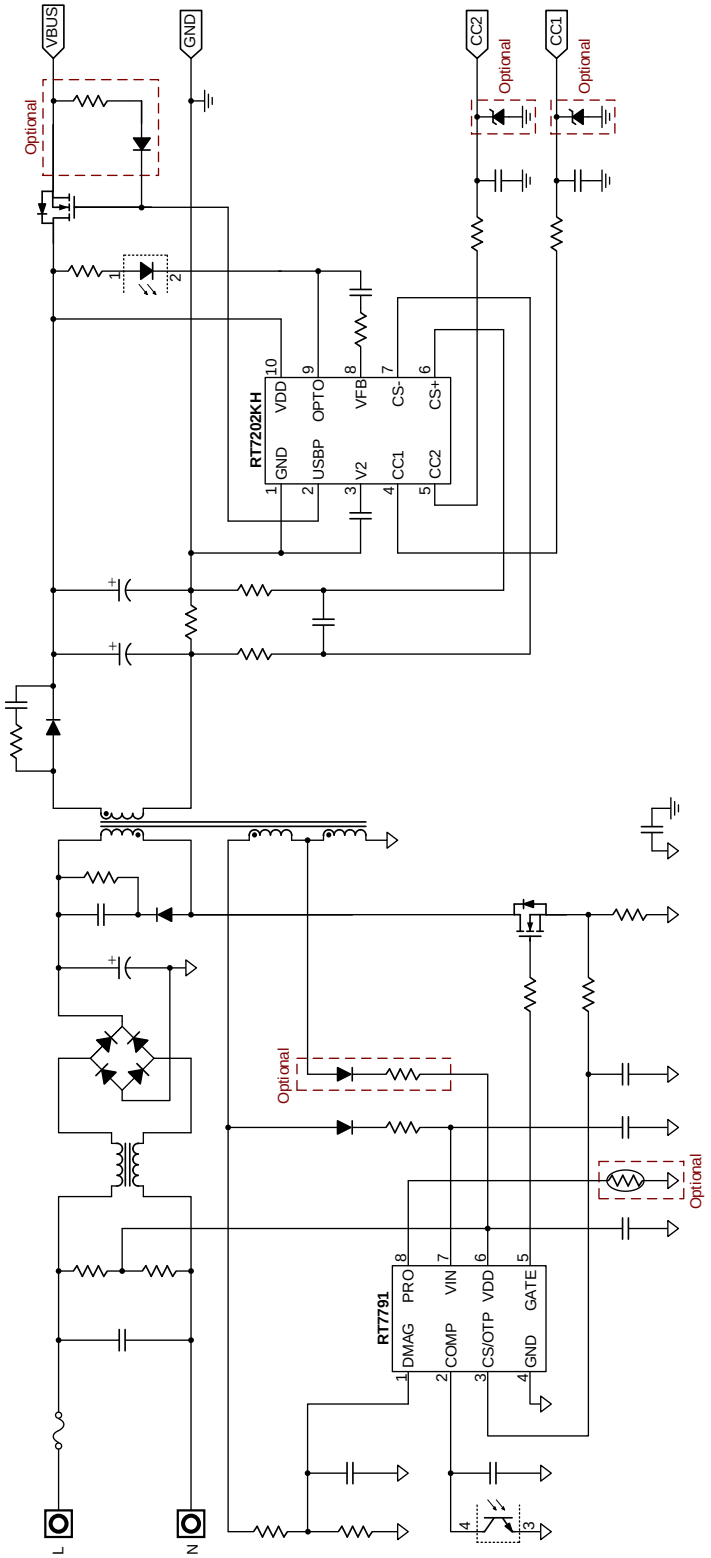
14.3 The RT7202KE Typical Application Circuit for Source Side



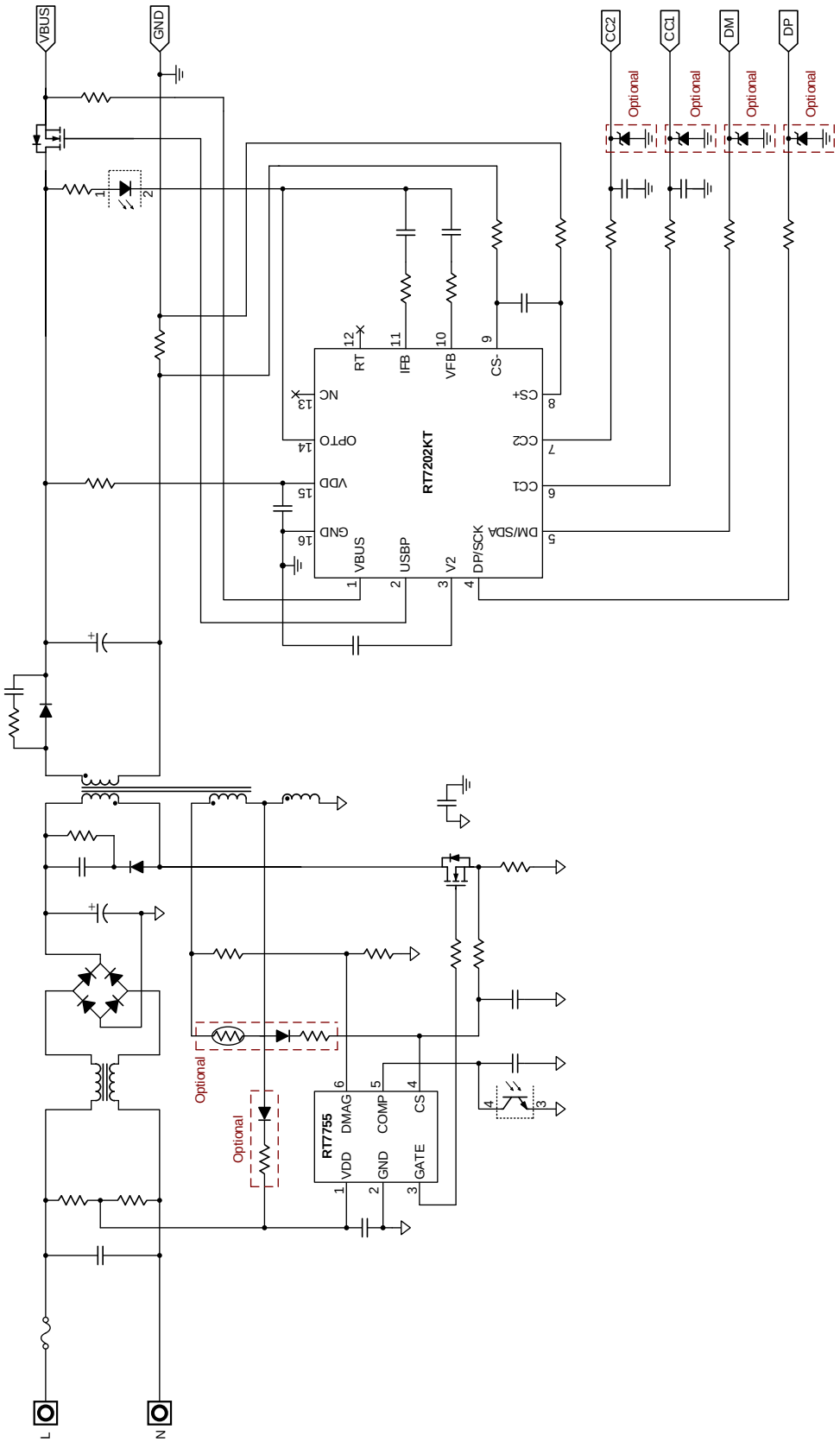
14.4 The RT7202KF/KP Typical Application Circuit for Source Side



14.5 The RT7202KH Typical Application Circuit for Source Side

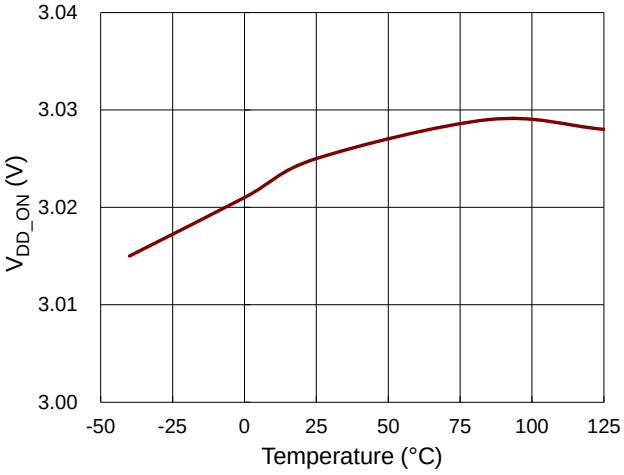


14.6 The RT7202KT Typical Application Circuit for Source Side

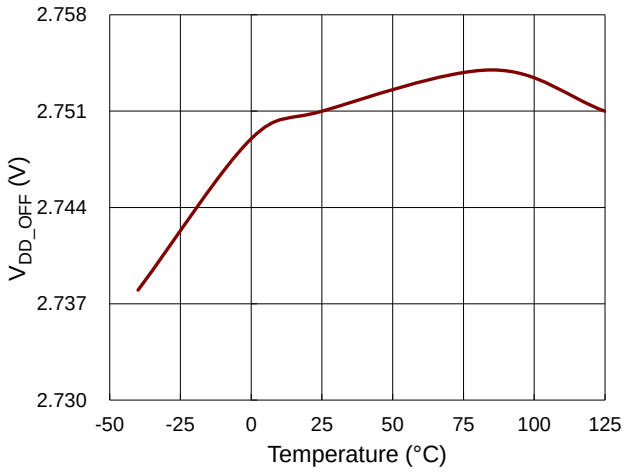


15 Typical Operating Characteristics

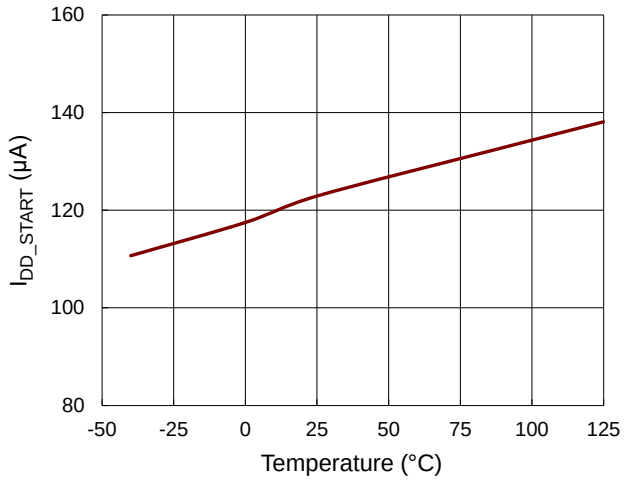
V_{DD_ON} vs. Temperature



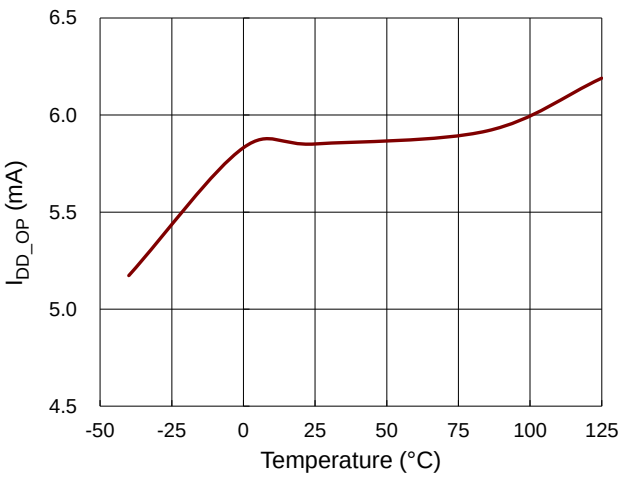
V_{DD_OFF} vs. Temperature



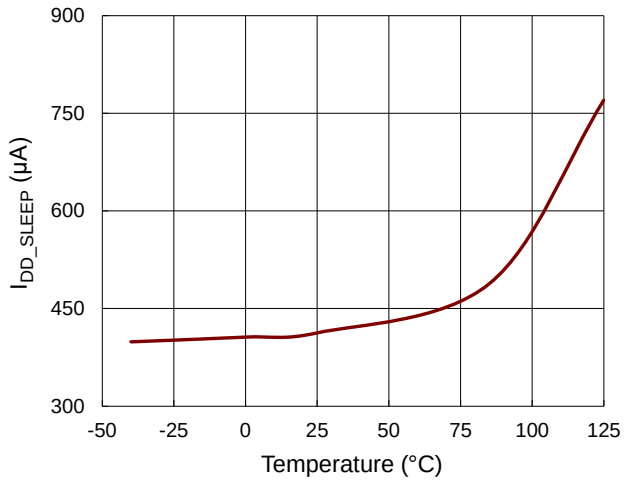
I_{DD_START} vs. Temperature



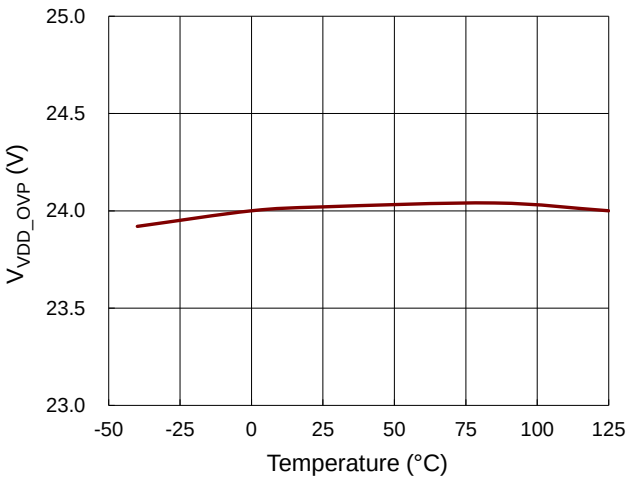
I_{DD_OP} vs. Temperature

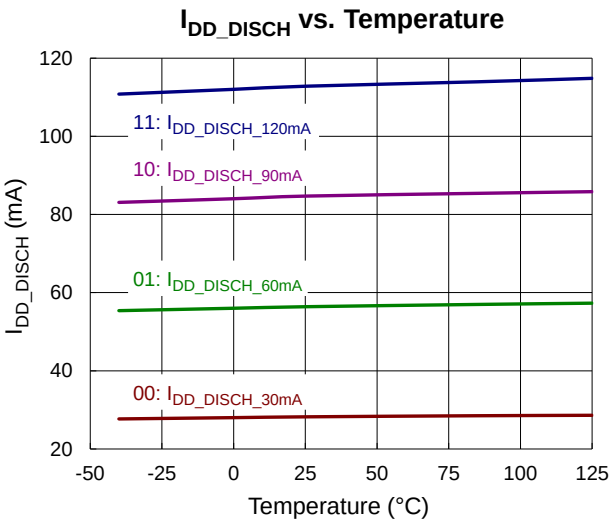


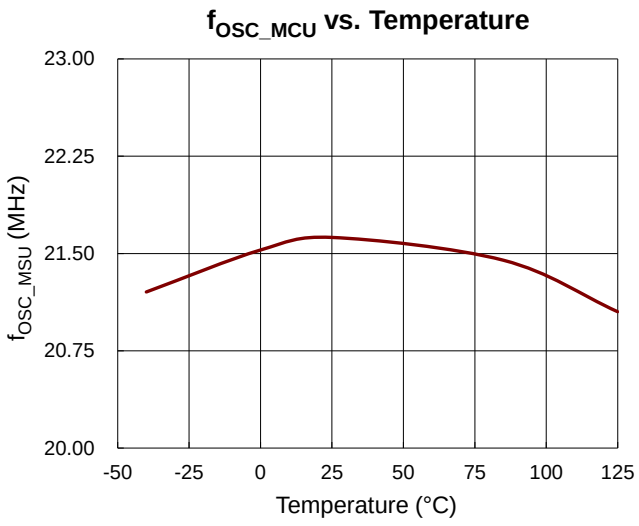
I_{DD_SLEEP} vs. Temperature

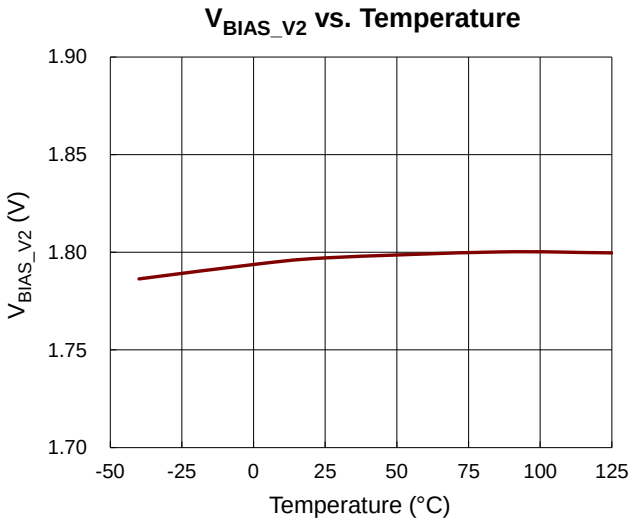


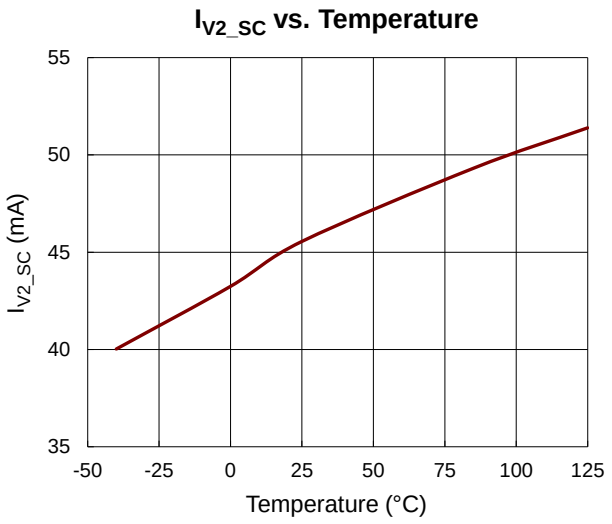
V_{VDD_OVP} vs. Temperature

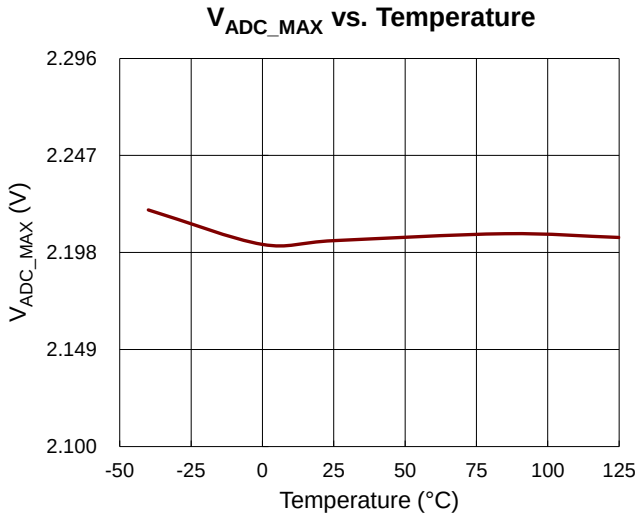


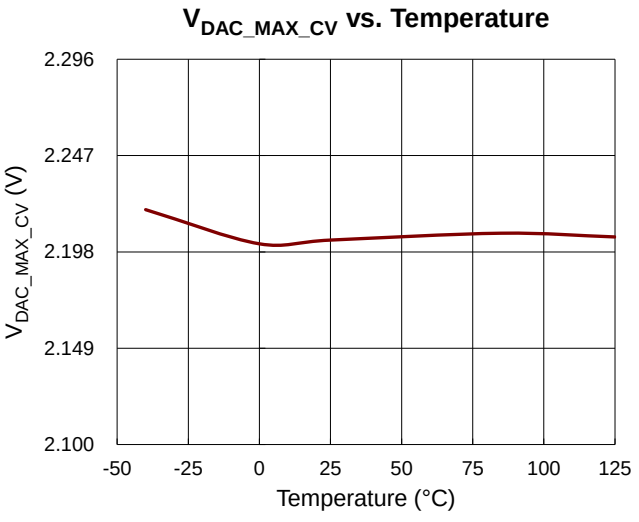




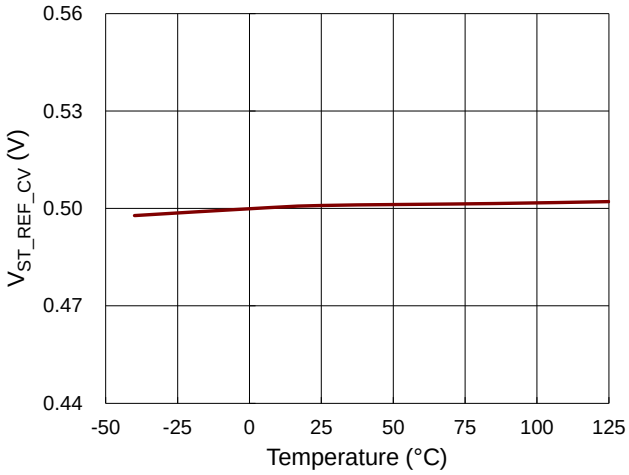




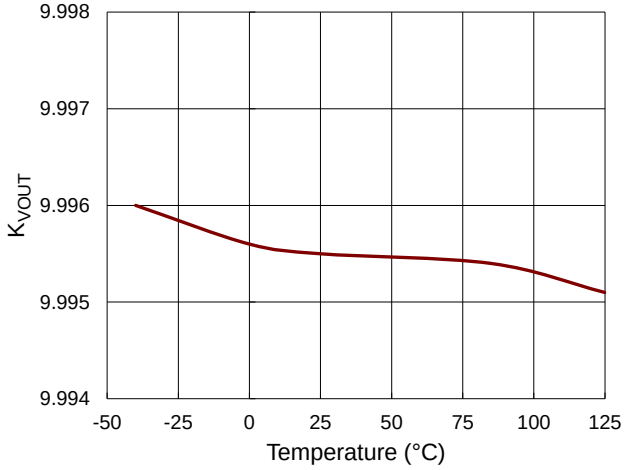




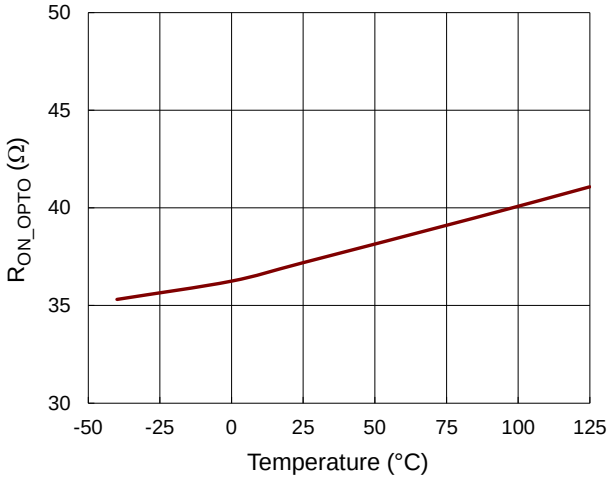
$V_{ST\_REF\_CV}$ vs. Temperature



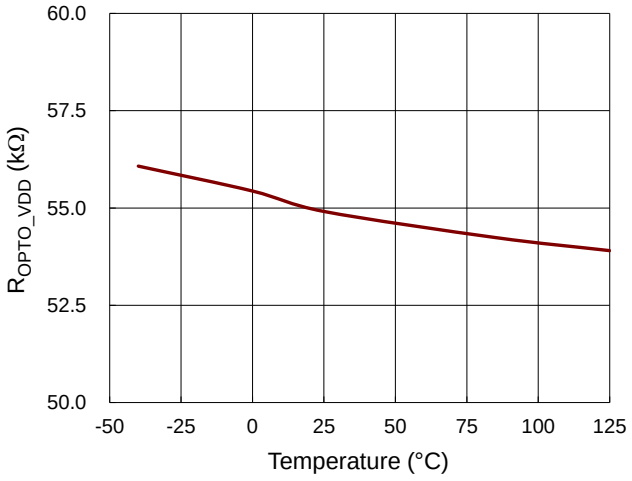
K_{VOUT} vs. Temperature



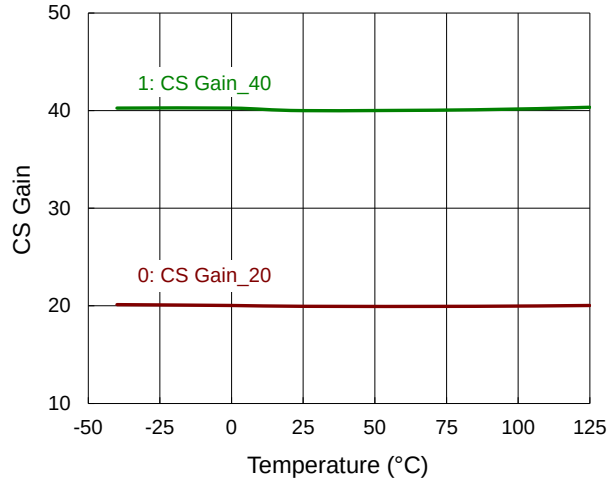
R_{ON_OPTO} vs. Temperature



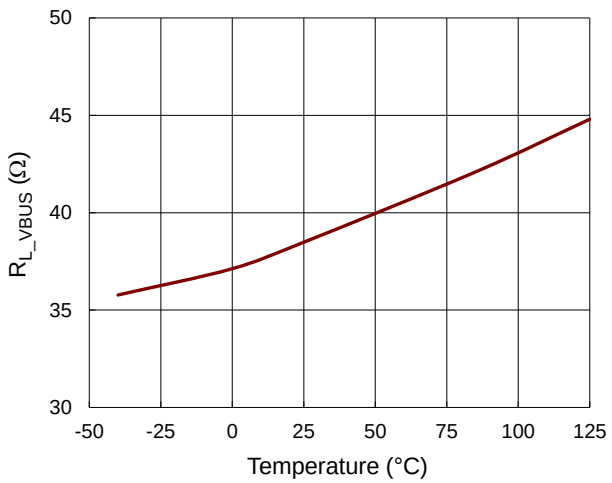
R_{OPTO_VDD} vs. Temperature



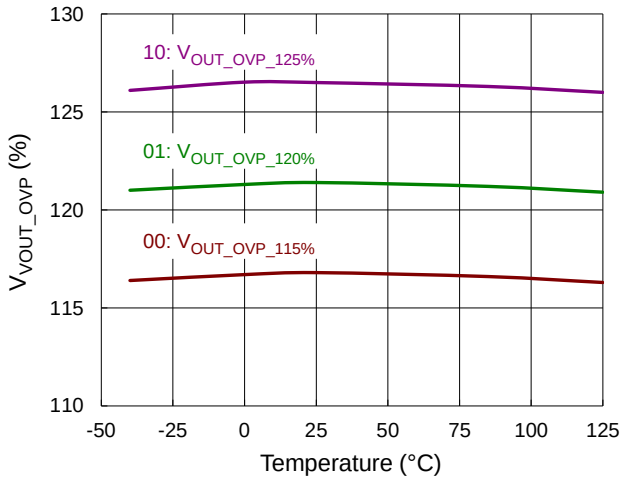
CS Gain vs. Temperature



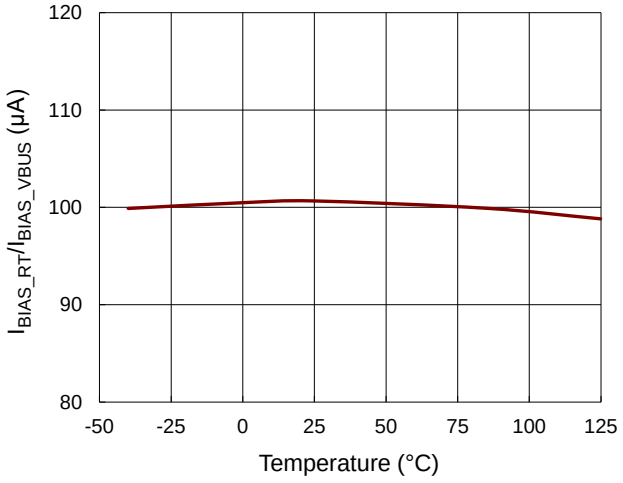
R_{L_VBUS} vs. Temperature



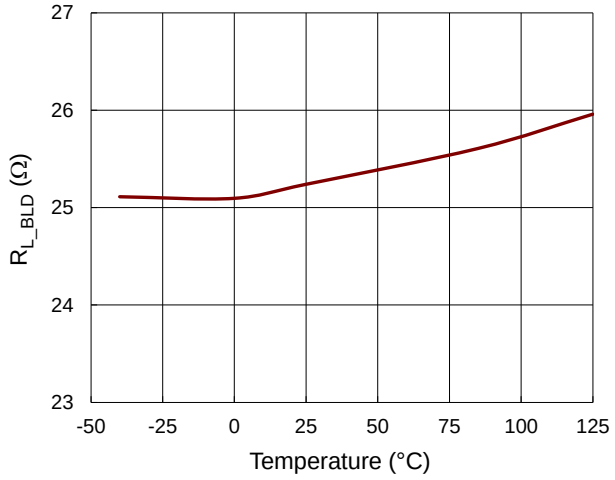
V_{VOUT_OVP} vs. Temperature



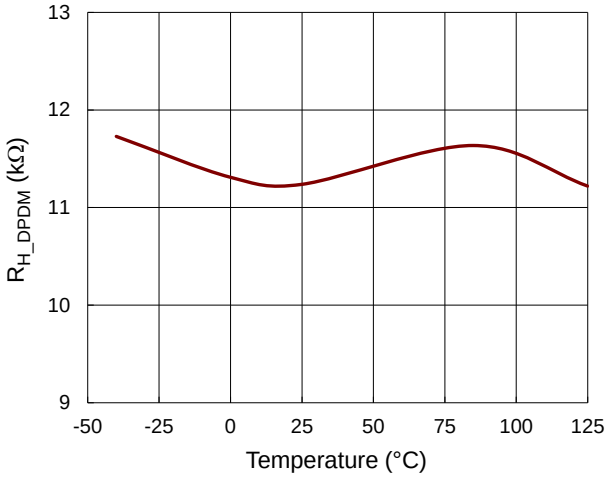
$I_{BIAS\_RT}/I_{BIAS\_VBUS}$ vs. Temperature



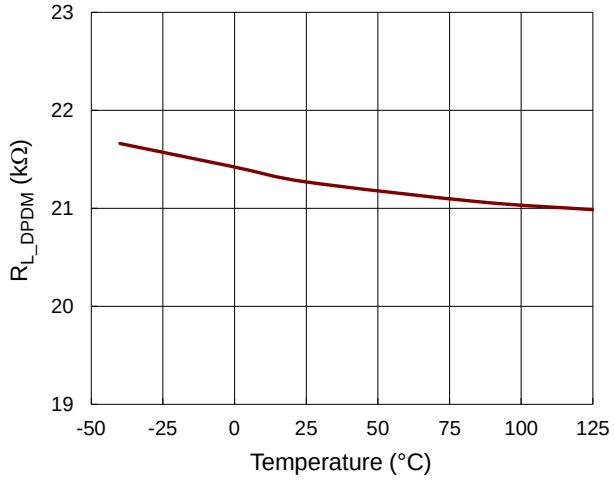
R_{L_BLD} vs. Temperature



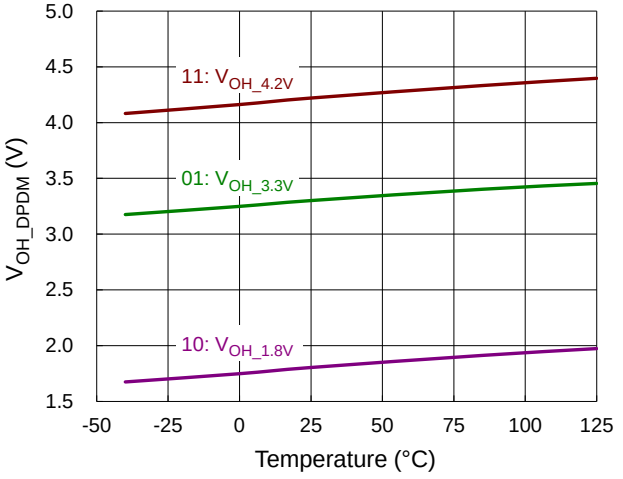
R_{H_DPDM} vs. Temperature

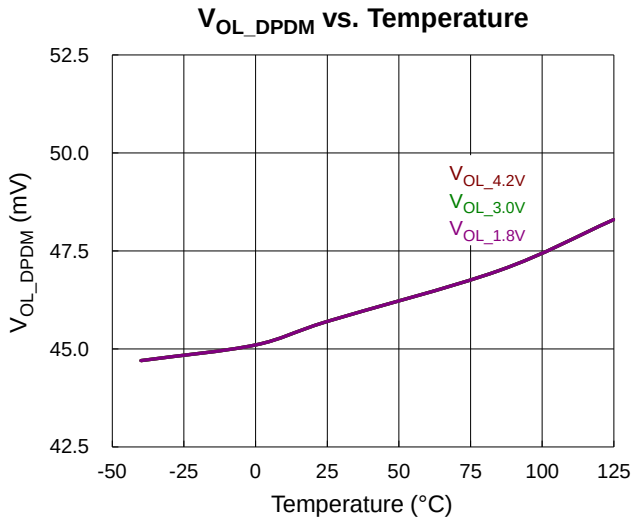


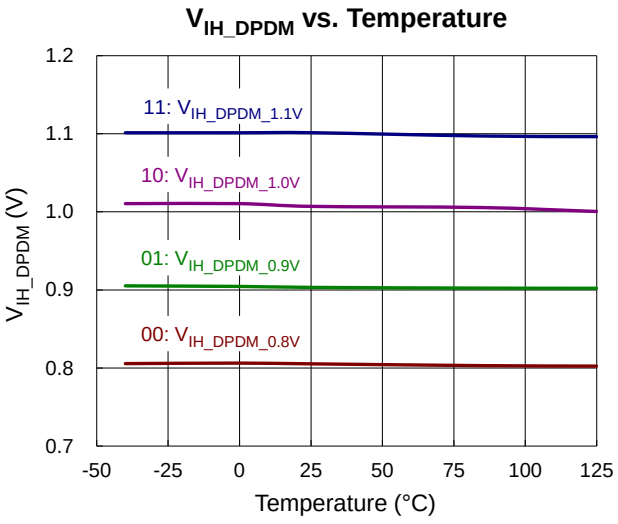
R_{L_DPDM} vs. Temperature

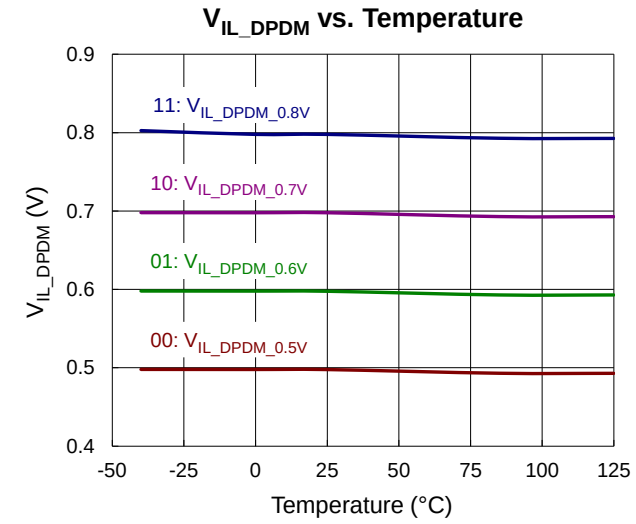


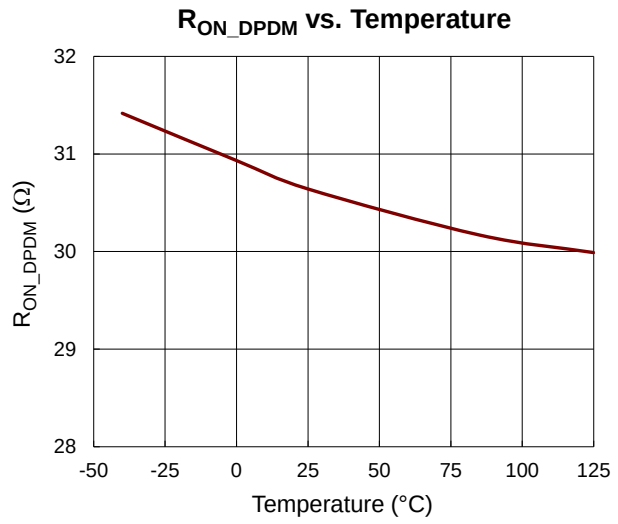
V_{OH_DPDM} vs. Temperature

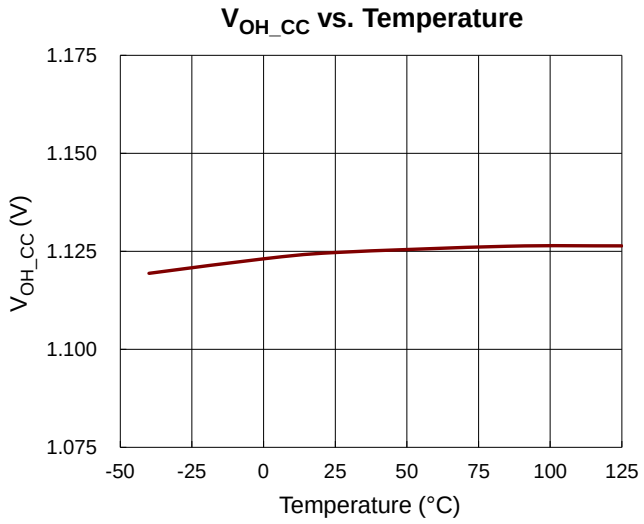


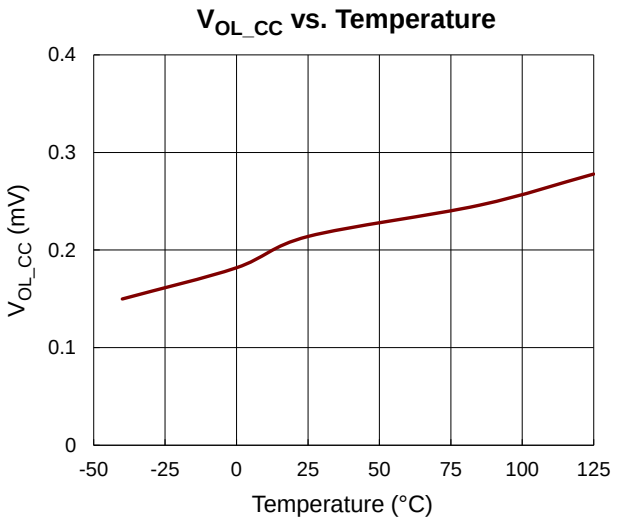


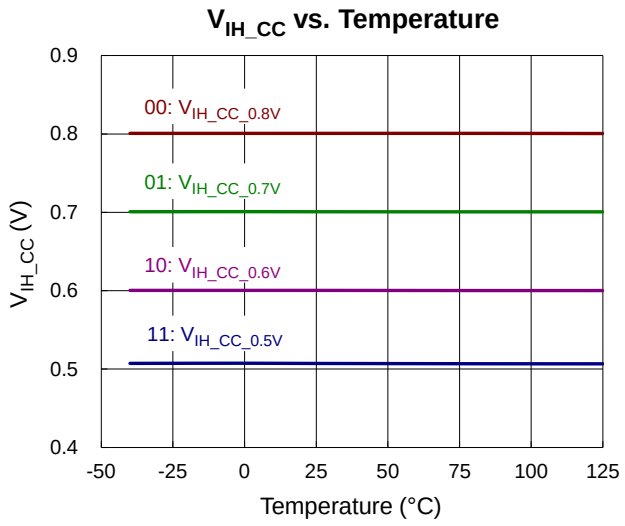


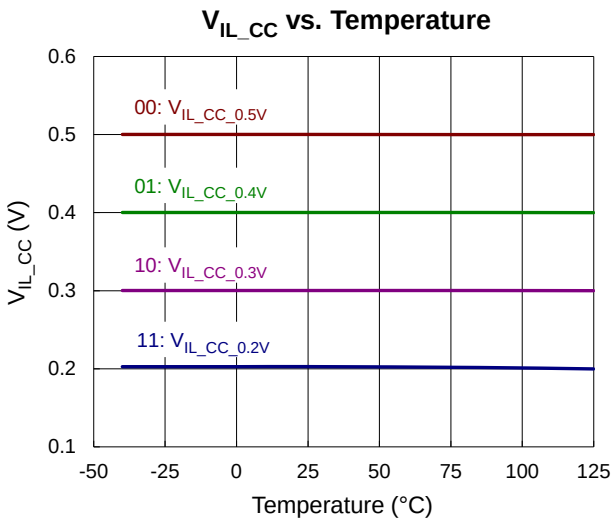


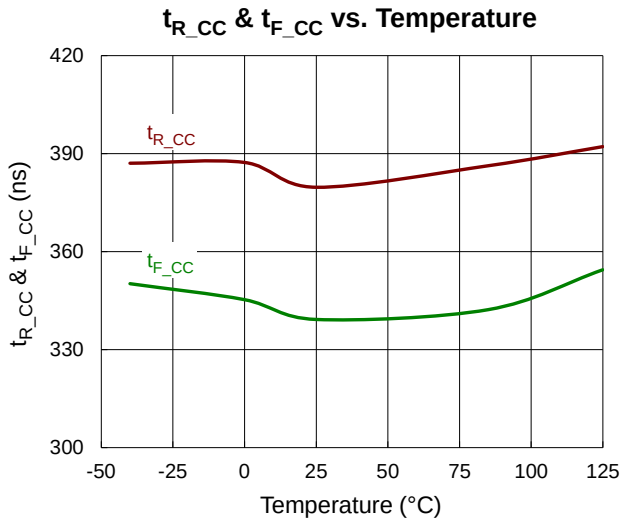


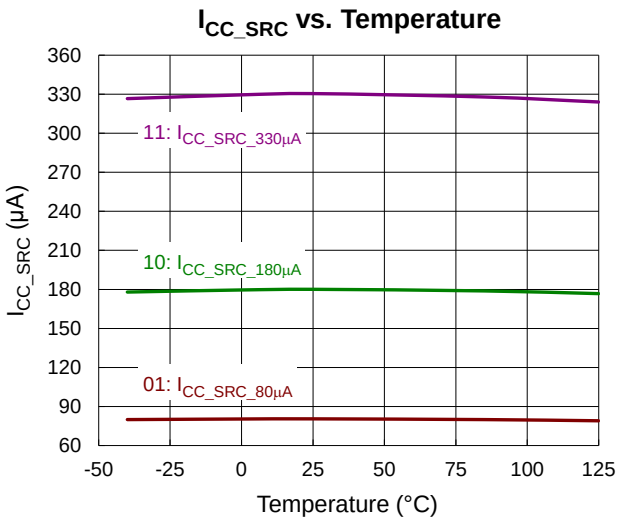


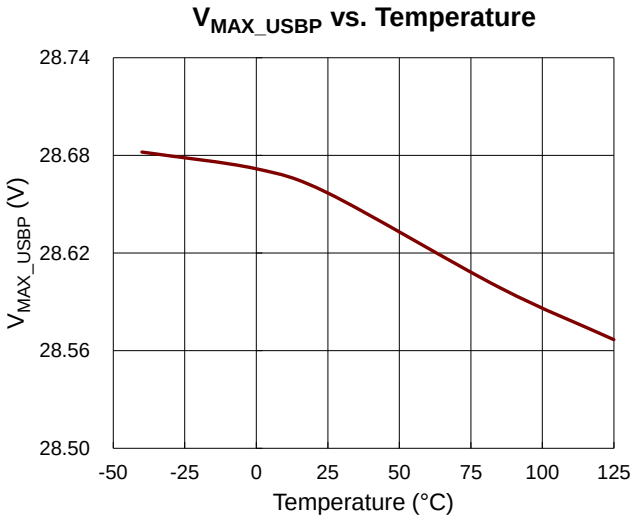


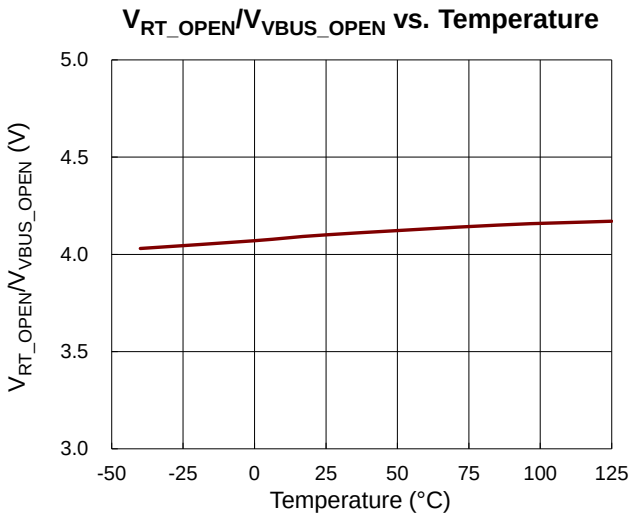












16 Operation

The RT7202K is a highly integrated secondary-side USB PD Type-C controller, offering various functions and protections for off-line AC-DC converters.

16.1 Power Structure

Biased by the VDD pin, the RT7202K provides two regulated DC output voltages, V_5 and V_2, to supply internal circuitry and an internal microprocessor (MCU). A bypass capacitor at the V2 pin is required to improve the stability of the internal LDO and to minimize regulated ripple voltages.

16.2 Constant-Voltage (CV) Regulators

A constant-voltage (CV) regulator is connected to OPTO, an open-drain output pin. The operation of the feedback loop is similar to that of the traditional TL431 shunt regulator, except that the V_{OPTO} operating range is wider, from 0.3V to 25V, enabling easy design of converters with a wider output range. The OPTO pin will be in high-impedance state if the VDD voltage is still below the UVLO threshold V_{VDD_ON}, ensuring a smooth power-on sequence. The reference voltage, V_{REF_CV}, for the voltage feedback loop is the analog output voltage from the embedded DAC, with its digital counterpart from the MCU. The analog output range of the 11-bit DAC is from V_{DAC_MIN} = 0.15V to V_{DAC_MAX} (2.2V typical), providing an output voltage resolution as small as 10mV to achieve high-precision CV regulation.

16.3 Constant-Current (CC) Regulators

The constant-current (CC) regulator is also connected to the OPTO pin. The analog current loop output range of the 10-bit DAC is from 0 to V_{DAC_MAX} (1.5V typical).

16.4 Current-Sense Amplifier

To minimize power loss of the current sense resistor in the converter, the RT7202K includes an amplifier with virtually zero input offset voltage and with a register-programmable voltage gain of 20 or 40. The sensed output current signal is amplified by the current-sense amplifier, shown as “Io_signal” in Figure 1. This amplified signal is then sent to the MCU via an ADC for analog-to-digital conversion, updating the output current status in the MCU. Based on the output current status and the firmware-programmable overcurrent threshold, overcurrent protection can be activated.

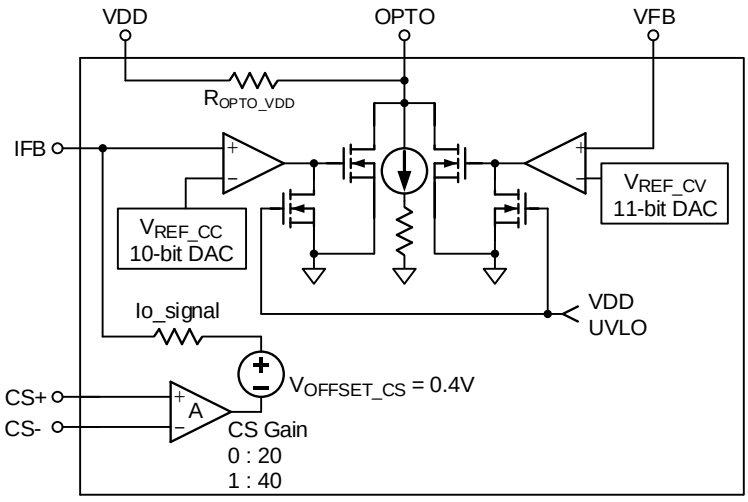


Figure 1. CV/CC Loop Block Diagram

16.5 Interface of DP and DM

The DP and DM pin, connected to the MCU via an ADC, can be reprogrammed for other purposes since they can be used as analog/digital inputs/outputs, as shown in Figure 2.

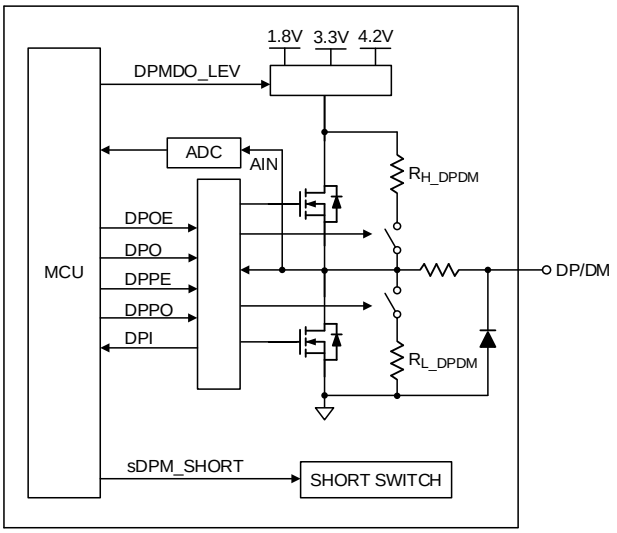


Figure 2. Interface of DP/DM

16.6 Interface of CC1 and CC2

The CC1 and CC2 pins are used for compliance with USB PD Type-C specification. When configured as a Downstream Facing Port (DFP), three current capabilities of 80μA, 180μA, and 330μA, provided by each of the CC pins, will be advertised to an Upstream Facing Port (UFP) as default USB current, 1.5A, and 3.0A, respectively, as shown in Figure 3.

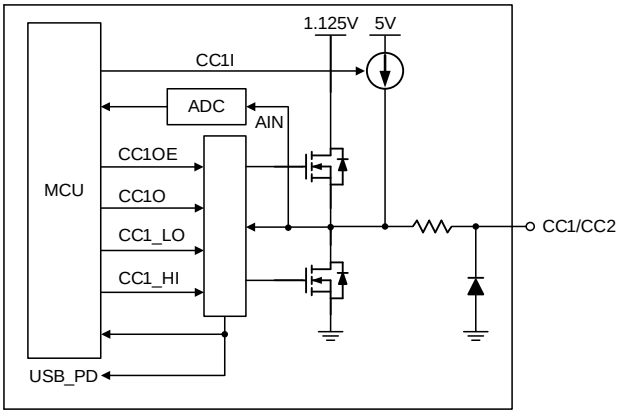


Figure 3. Interface of CC1 and CC2

16.7 Open-Drain Drivers for the BLD and VBUS Pins

The BLD and VBUS pins, with their specific functions, are driven by open-drain drivers, as shown in Figure 4 and explained below.

The BLD pin is used as a bleeder to help discharge the output capacitor to V_{safe5V} upon the detachment of a connected device, or to a lower desired output voltage level upon a UFP request, such as from 12V to 5V. A resistor is connected between the VOUT and the BLD pin and a power resistor can be used for better power dissipation capability.

The VBUS pin is used as a bleeder to help discharge the VBUS capacitor to V_{safe0V} upon the detachment of a connected device and provide real-time VBUS voltage detection by ADC.

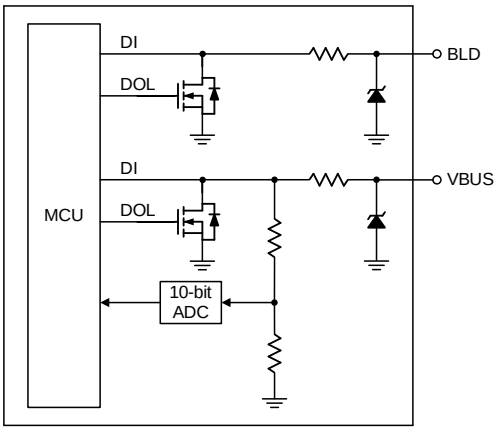


Figure 4. Interface of the BLD and VBUS Pins

17 Application Information

(Note 7)

17.1 Constant-Voltage (CV) Loop

As shown in Figure 5, the RT7202K integrates an error amplifier (EA) to regulate the output voltage. The output voltage is determined by the following equation:

$V_{DD} = K_{VOUT} \times V_{REF\_CV}$

where $K_{VOUT} = (R_{FB1} + R_{FB2}) / R_{FB2} = 10$ (typical)

Therefore, the VOUT is determined by V_{REF_CV}, the analog output from the DAC, and its digital counterpart, which is controlled by the MCU, as shown in Functional Block Diagram.

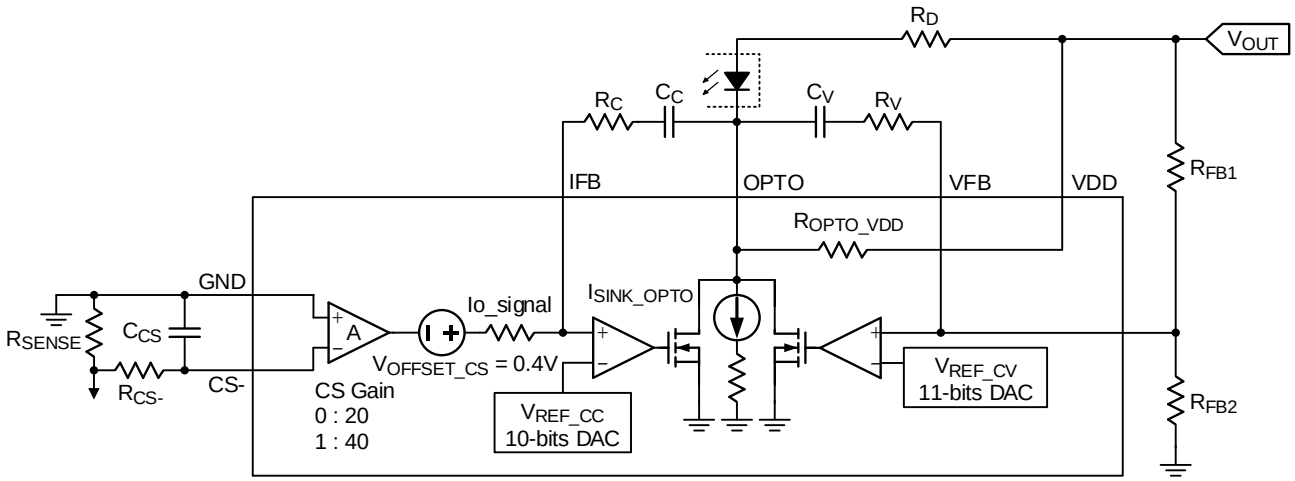


Figure 5. CV Loop and Current-Sense Amplifier

The OPTO driver sinks current through an optocoupler and an external resistor R_D from the output voltage. The optocoupler isolates the secondary side from the primary side and also provides the feedback compensation signal for the primary side. Note that for better linearity of the loop compensation range, R_D should be designed to cover operation at the minimum output voltage.

$$\frac{V_{OUT\_MIN} - V_F - 0.3V}{R_D} \times CTR \geq I_{COMP\_MAX}$$

CTR: Current transfer ratio of the optocoupler

V_F: Forward voltage of the optocoupler

0.3V: The minimum OPTO voltage for the OPTO driver to sink 2mA.

I_{COMP_MAX}: The maximum COMP sourcing current of a traditional PWM controller on the primary side. It is a current sourced from an internal bias through a built-in pull-high resistor connected the COMP pin in the PWM controller.

17.2 Constant-Current (CC) Loop and Current-Sense Amplifier

The RT7202K integrates a virtually zero input-offset-voltage current-sense amplifier. The voltage gain of 20 or 40 can be set by the internal register. The amplified output current sense signal, sent to an ADC for A/D conversion, is monitored and processed by the MCU, and is also sent to the CC loop. The reference voltage of the CC loop is determined by V_{REF_CC} (from the DAC), which is programmed according to the chargers' requirements. Both the constant-voltage and constant-current compensation loops are connected together at the OPTO pin.

17.3 External Cable Compensation Circuit

The RT7202K provides option for external CV resistors in order to conduct linear cable compensation. The cable compensation can be implemented by the compensation resister R_{SENSE} of the application circuit. The compensation voltage is determined as:

$V_{COMPENSATION} = I_{OUT} \times R_{SENSE} \times (R_{FB1} / R_{FB2})$

17.4 Power-Up Sequence

Figure 6 shows the timing diagram for the power-up sequence. When start-up, the default output is set to 5V. Once a Type-C cable is connected, the UFP delivers voltage and current settings to the RT7202K, enabling the MCU to decode these settings and program reference voltages, V_{REF_CV} for the CV, which are the analog outputs converted by the DAC. If the Type-C cable is detached, or the output current is lower than the power-saving mode threshold, typically programmed as 200mA, the RT7202K will enter power-saving mode. In this mode, the RT7202K operates at an ultra-low operating current, thereby saving total input power. If the output current increases and exceeds the power-saving mode threshold, or any input/output signal is toggled, the RT7202K will exit power-saving mode.

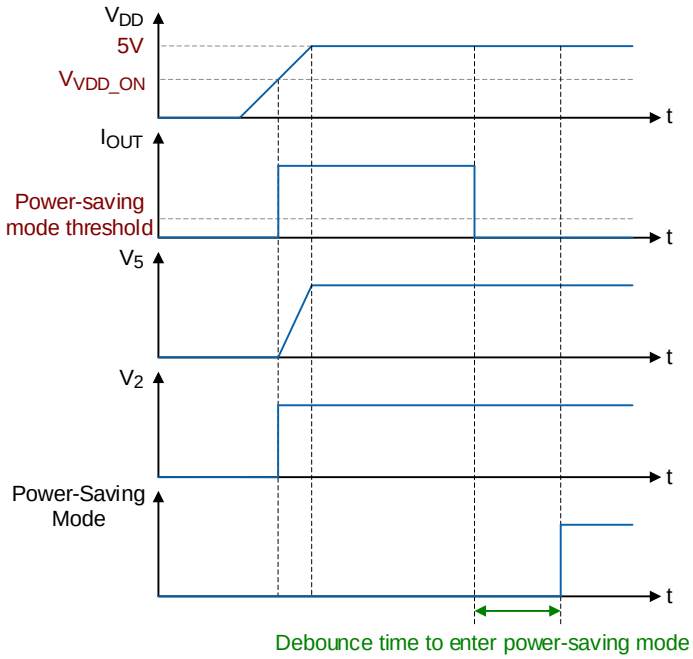
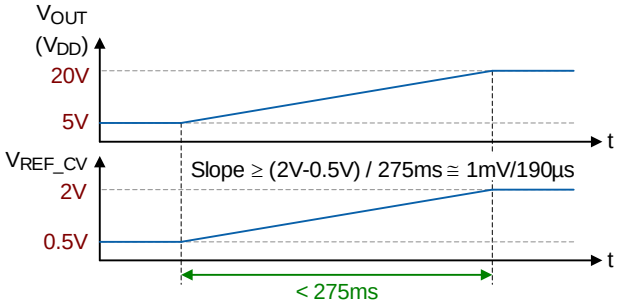


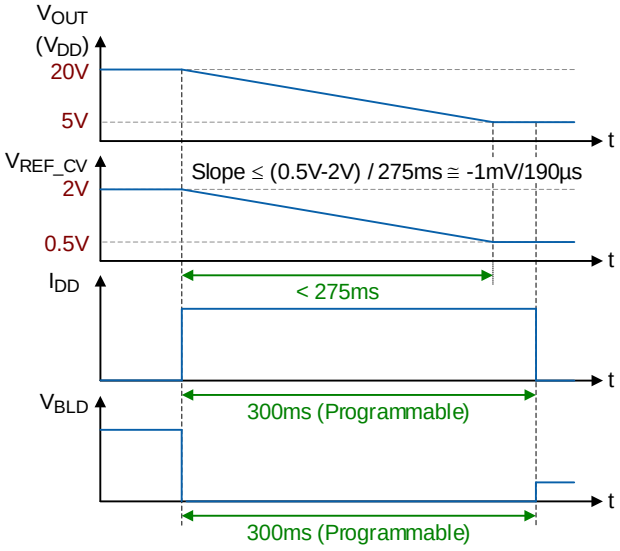
Figure 6. The Output Sequence during Start-Up

17.5 Output Voltage Rises and Falls

When the protocol is detected, the reference voltage V_{REF_CV} can be set by the request of the UFP. Both the rise time and fall time of output voltages should be less than 275ms in accordance with the USB PD Specification, as shown in Figure 7.



(a) Output Voltage Rising



(b) Output Voltage Falling

Figure 7. Output Voltage Transient Waveforms

During the time of V_{OUT} falling, as shown in Figure 7(b), the RT7202K will provide an extra discharging path for the output capacitor so that V_{OUT} can be settled in a shorter duration. The discharge path, whether from the VDD pin or the BLD pin, depends on RT7202K's version.

The RT7202K provides control for the discharge current from the VDD pin. The discharge current can be programmed by the register according to the VDD voltage level, as shown in Figure 8.

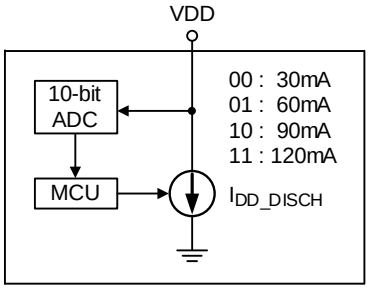


Figure 8. Discharge Current Control from the VDD Pin

The RT7202KD/KJ/KS provides an open-drain driver at the BLD pin as an active dummy load switch to discharge the output capacitor, as shown in Figure 9. The turn-on timing can be programmed. The designed R_{DUMMY} can be calculated using the following formula:

C_{OUT} x (R_{DUMMY} + R_{L_BLD}) x 2 < 275ms

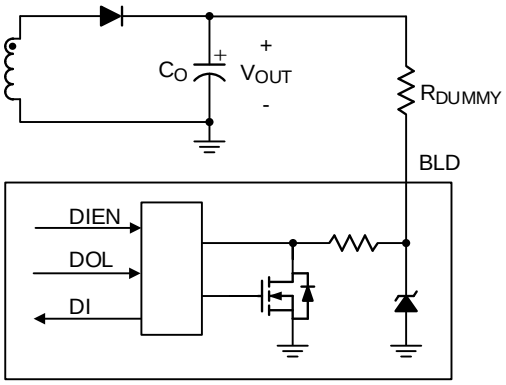


Figure 9. Application Circuit of an Active Dummy Load

17.6 Blocking MOSFET Control (USBP)

The RT7202K provides a push-pull driver for controlling an external blocking N-MOSFET. The push-pull driver can not only control the N-MOSFET for smooth turn-on to avoid V_{OUT} drops in capacitive load conditions but also provide quickly turn-off in fault conditions.

Once communication is set up with an UFP, or a 5.1kΩ resistor at the CC1/CC2 pin of a Type-C connector of the UFP is detected, the N-MOSFET will be turned on. If a V_{OUT} overvoltage condition occurs, the blocking N-MOSFET will be turned off to prevent the UFP from being damaged by the V_{OUT} overvoltage condition. If V_{OUT} is shorted to GND, the N-MOSFET will also be turned off automatically to limit the output power.

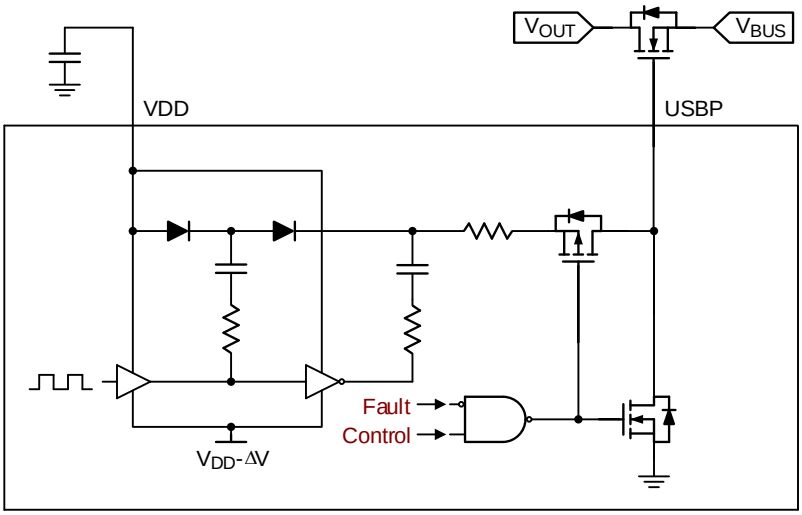
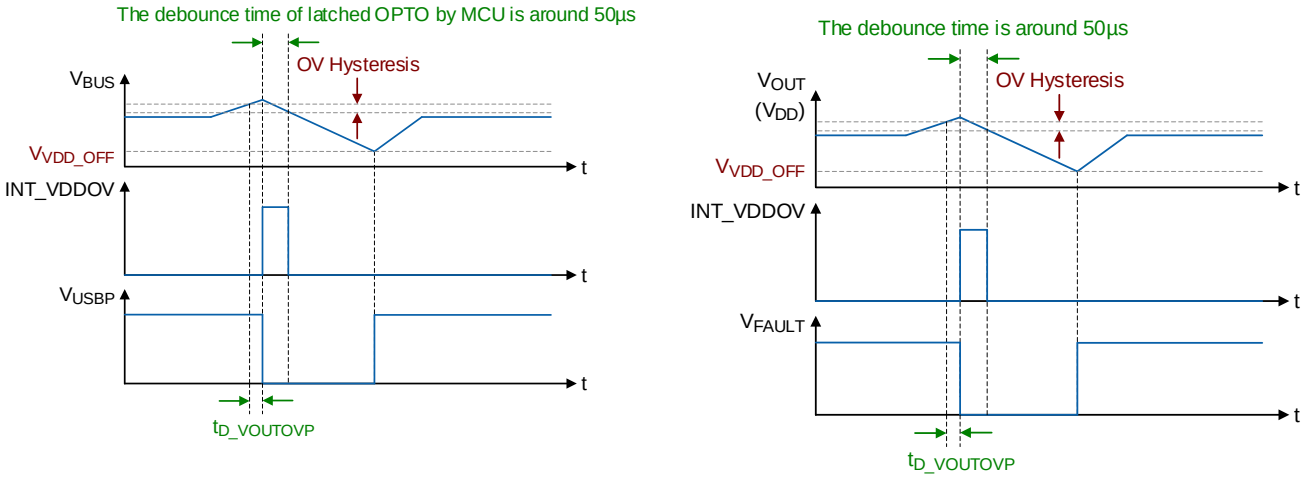


Figure 10. Blocking N-MOSFET Control

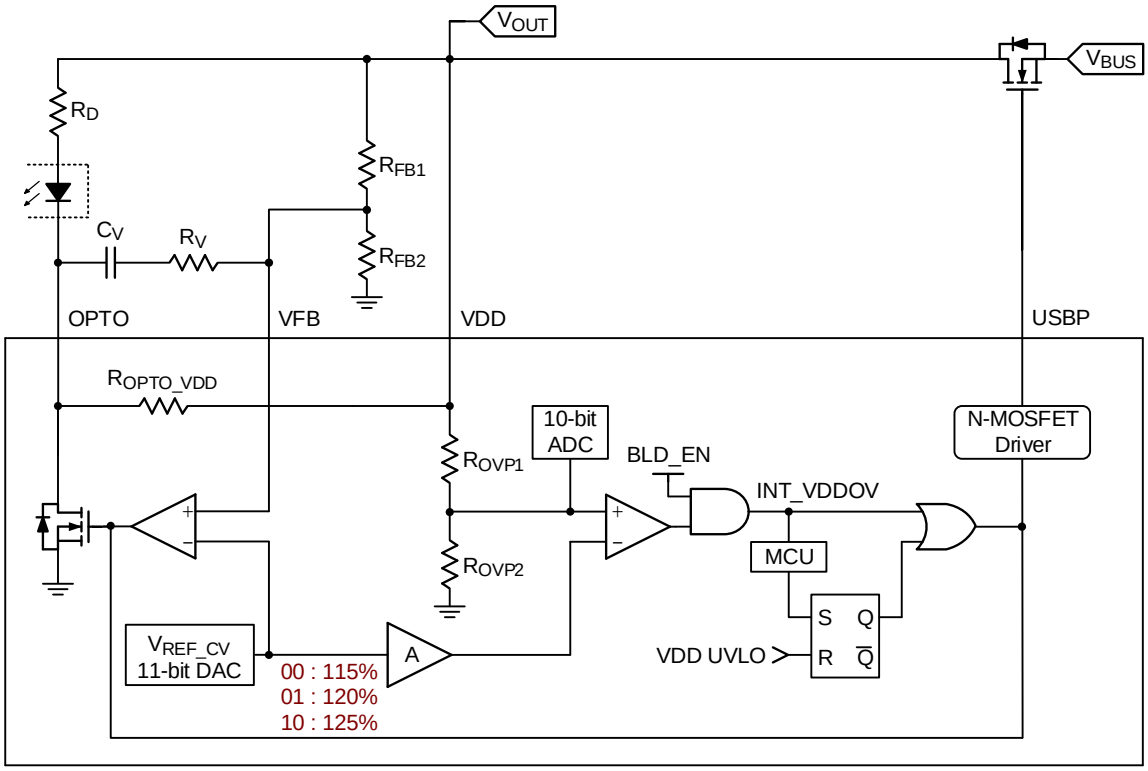
17.7 Output Overvoltage Protection

As shown in the Figure 11 and Figure 12, the RT7202K provides a fast turn-off blocking N-MOSFET as a backup V_{OUT} overvoltage protection, in case the optocoupler of the feedback loop malfunctions due to aging. If the internal voltage related to VDD is higher than the programmable threshold V_{VOUT_OVP}, the USBP pin will be pulled low. The USBP pin voltage will be latched low until the VDD voltage drops below the VDD turn-off threshold V_{VDD_OFF}.

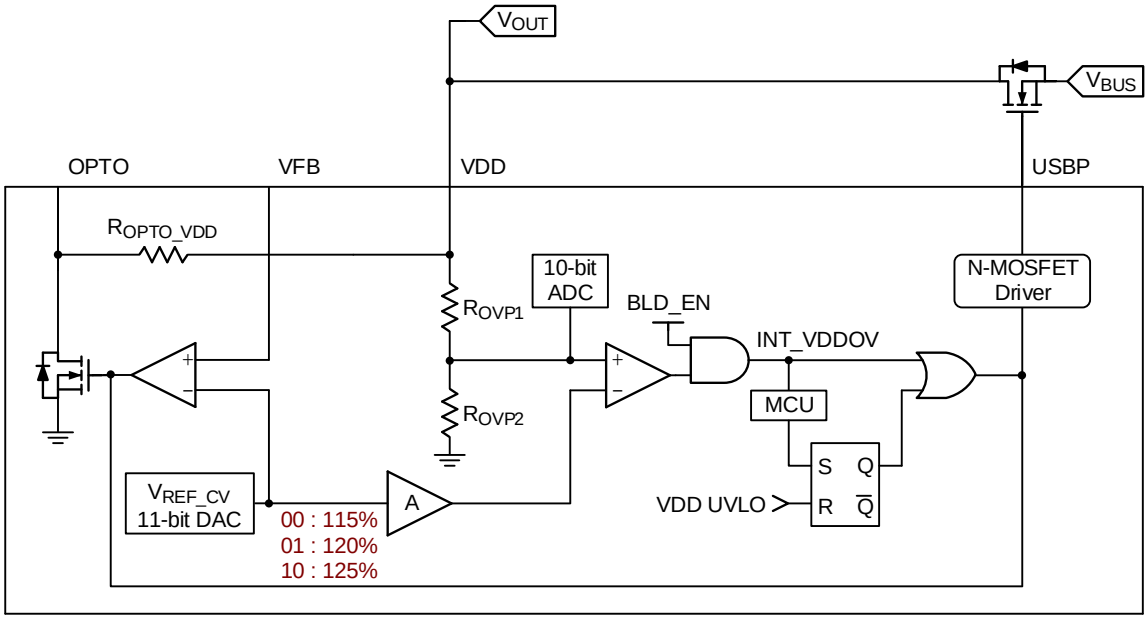


(a) For Source Application (b) For Sink Application

Figure 11. Timing Sequence of the OVP Pin Function



(a) For Source Application



(b) For Sink Application

Figure 12. OVP Functional Diagram

17.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to -ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-16L 4x4 package, the thermal resistance, θ_{JA}, is 256.4°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. For a SOP-10 package, the thermal resistance, θ_{JA}, is 194.2°C/W on a standard JEDEC 51-3 low effective-thermal-conductivity single-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (256.4°C/W) = 0.39W for a WQFN-16L 4x4 package.

$P_{D(MAX)}$ = (125°C - 25°C) / (194.2°C/W) = 0.51W for a SOP-10 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 13 allow the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

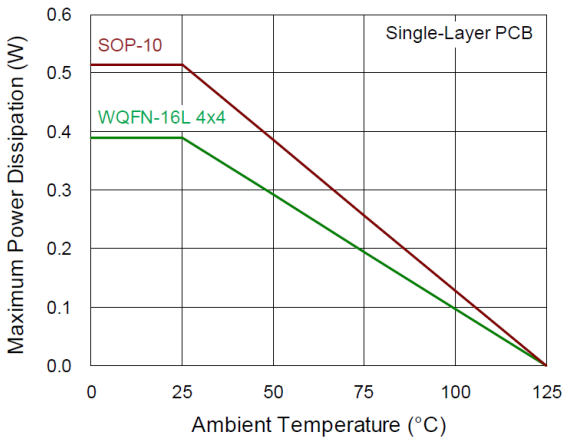
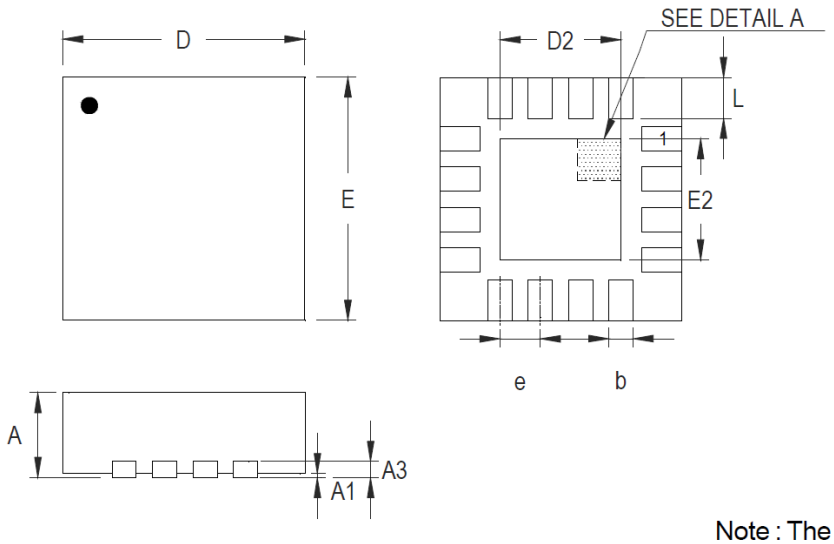


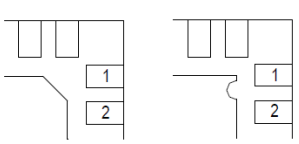
Figure 13. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

18 Outline Dimension

18.1 WQFN-16L 4x4





DETAIL A

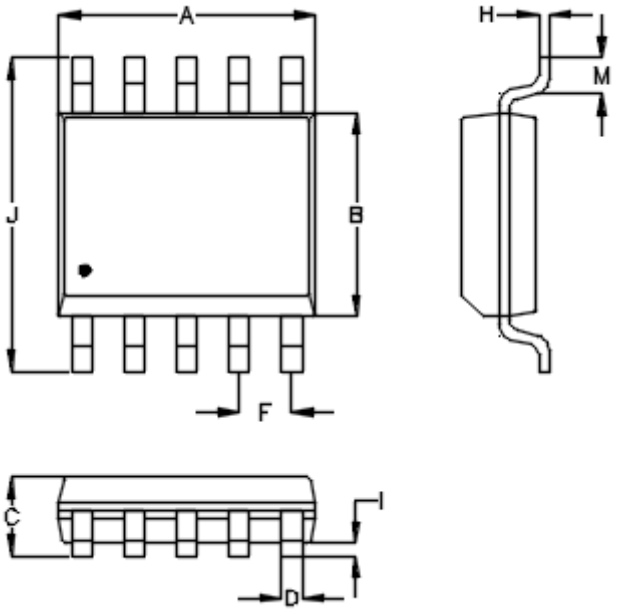
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.250	0.380	0.010	0.015
D	3.950	4.050	0.156	0.159
D2	2.000	2.450	0.079	0.096
E	3.950	4.050	0.156	0.159
E2	2.000	2.450	0.079	0.096
e	0.650		0.026	
L	0.500	0.600	0.020	0.024

W-Type 16L QFN 4x4 Package

18.2 SOP-10

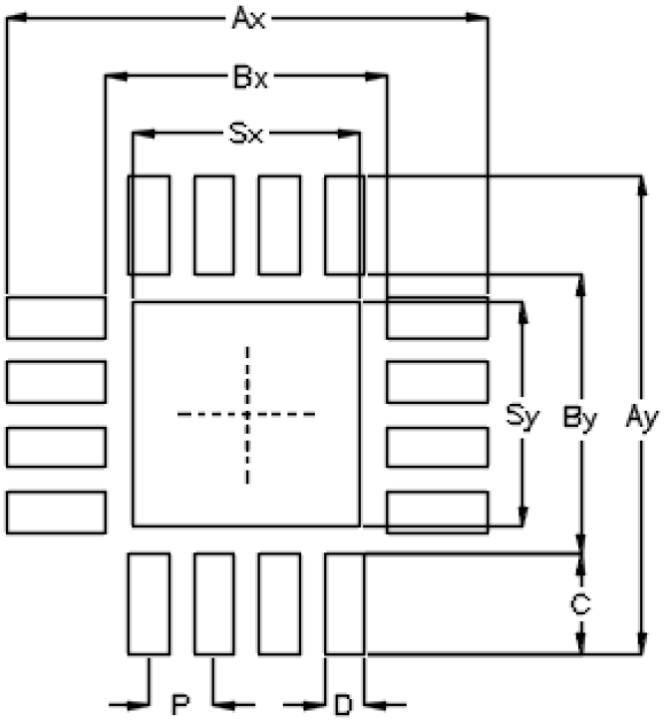


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.800	5.000	0.189	0.197
B	3.800	4.000	0.150	0.157
C	1.300	1.750	0.051	0.069
D	0.300	0.500	0.012	0.020
F	1.000		0.039	
H	0.100	0.250	0.004	0.010
I	0.050	0.250	0.002	0.010
J	5.800	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

10-Lead SOP Plastic Package

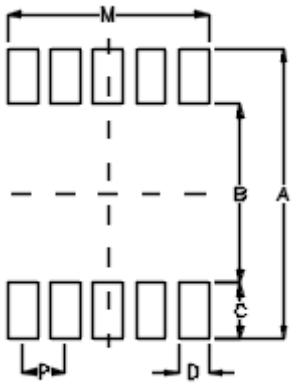
19 Footprint Information

19.1 WQFN-16L 4x4



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN4*4-16	16	0.65	4.80	4.80	2.80	2.80	1.00	0.40	2.25	2.25	±0.05

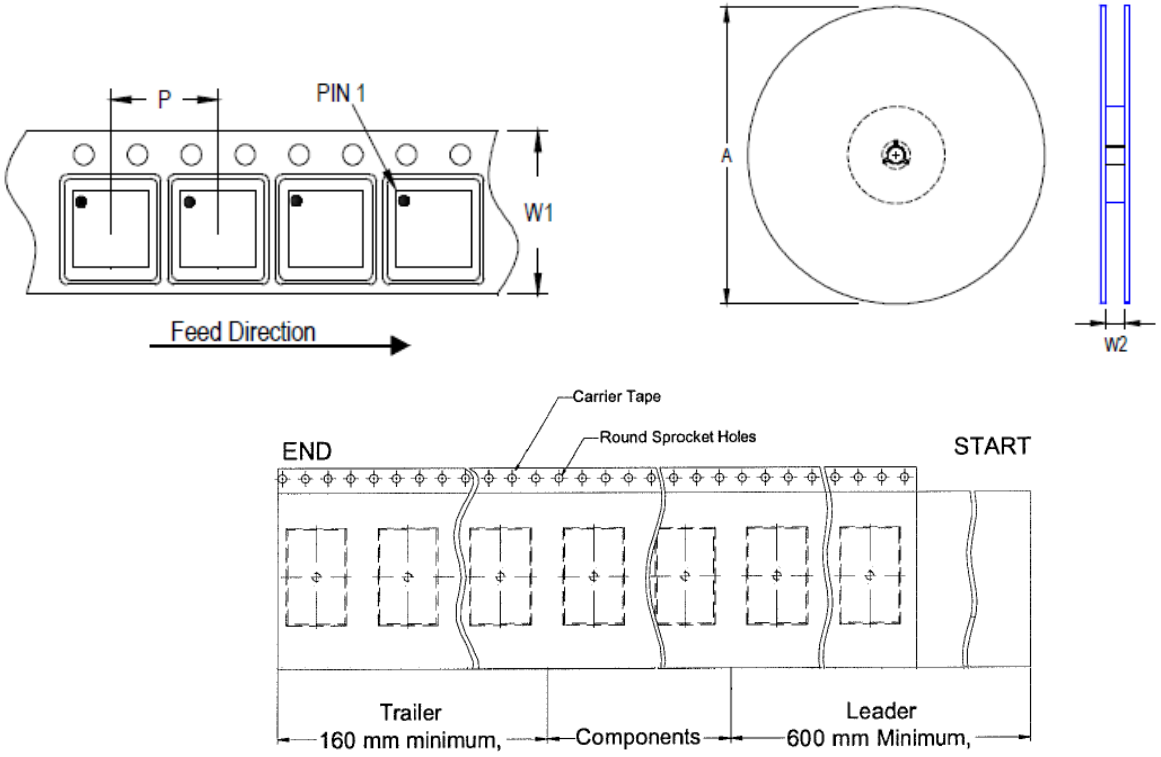
19.2 SOP-10



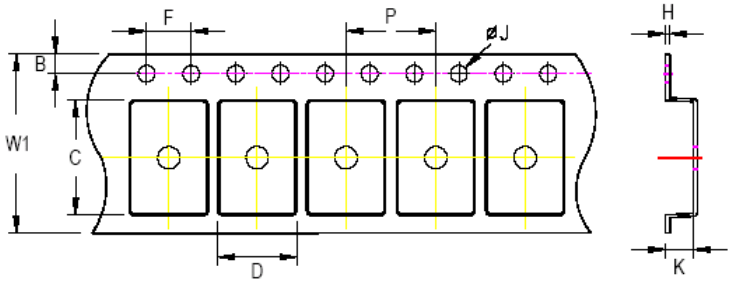
Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P	A	B	C	D	M	
SOP-10	10	1.00	6.80	4.20	1.30	0.70	4.70	±0.10

20 Packing Information

20.1 QFN&DFN 4x4 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4

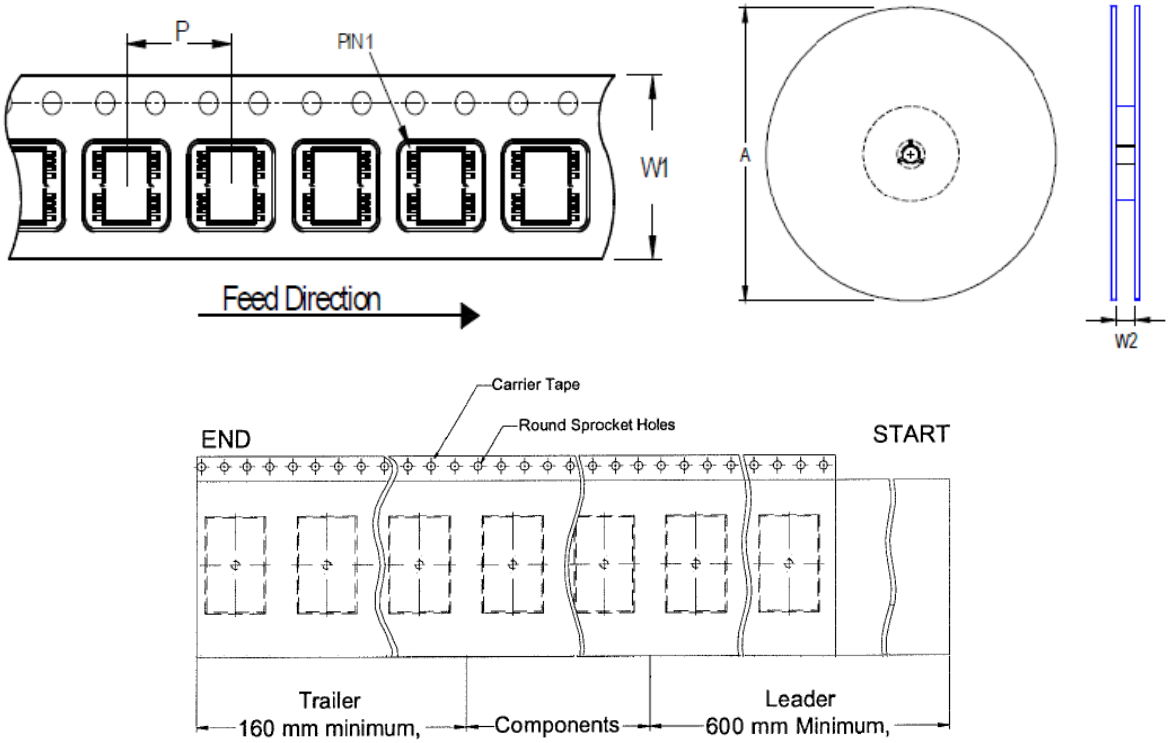


C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

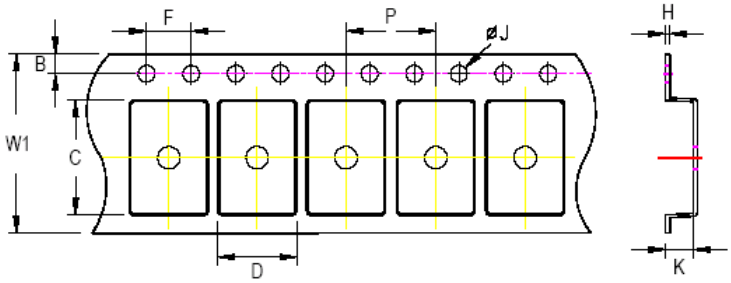
- For 12mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.2 SOP-10 Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
SOP-10	12	8	330	13	3,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 1.0mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

20.3 QFN&DFN 4x4 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.4 SOP-10 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 13”	4	 1 reel per inner box **Box G**
2	 HIC & Desiccant (2 Unit) inside	5	 6 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Units
SOP-10	13”	3,500	Box G	1	3,500	Carton A	6	21,000

20.5 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Tel: (8863)5526789

21 Datasheet Revision History

Version	Date	Description	Item
12	2023/8/25	Modify	Features on P1 Ordering Information on P1 Functional Pin Description on P10 Functional Block Diagram on P14 Electrical Characteristics on P17, 18, 19 Typical Operating Characteristics on P31, 33 Application Information on P34
13	2024/6/18	Modify (Added RT7202KS)	General Description on P1 Features on P1 Ordering Information on P1 RT7202K Version Table on P3 Simplified Application Circuit on P3, 4, 6 Pin Configuration on P7 Functional Pin Description on P8, 9, 10 Functional Block Diagram on P11, 13 Electrical Characteristics on P15 to 19 Typical Application Circuit on P20, 21, 25 Operation on P32, 33 Application Information on P36, 38 Packing Information on P46 to 50
14	2024/9/9	Modify	*General Description on page 1* - Removed the RT7202KD *RT7202K Version Table on page 3* - Modified Maximum Constant Discharge Current *Simplified Application Circuit on page 3* - Removed the RT7202KD for Section 7.1 - Modified the CC Pin Circuit *Electrical Characteristics on page 16, 17, 18* - Added I^2C Section and BLD Discharge Current - Modified VDD Discharge Current *Typical Application Circuit on page 20* - Removed the RT7202KD for Section 14.1 *Operation on page 32, 33* - Modified the title of Section 16.3 and 16.5 *Application Information on page 36, 39, 40, 41* - Modified the title of Section 17.3 - Added Sink OVP Diagram - Updated declaration