RICHTEK®

RT7082A2M

Three-Phase PMSM/BLDC Motor Controller with Pre-Driver

1 General Description

The RT7082A2M is an application-specific IC designed for PMSM/BLDC motor applications. This two-in-one ASIC integrates several functional circuits, including a 3-phase motor controller, a 3-phase gate driver, three bootstrap diodes, a 5V LDO, and an LDO for gate driver supply.

The RT7082A2M embeds the ARM 32-bit Cortex-M0 core with peripheral circuits to perform sensorless Field Oriented Control (FOC). In addition, this ASIC provides several system-level peripheral functions, including filters at the ADC input, a communication interface, a thermal sensor, adjustment of sourcing current for the gate driver, adjustment of supply voltage for the gate driver, short circuit protection (SCP), and locked-rotor protection, to reduce component count, PCB size, and system cost.

Moreover, the RT7082A2M drives external N-Channel MOSFETs in a three half-bridge configuration with built-in bootstrap circuitry up to 30V.

The RT7082A2M is available in a VQFN-32L 4x4 package. The recommended junction temperature range is −40°C to 125°C, and the ambient temperature range is −40°C to 105°C.

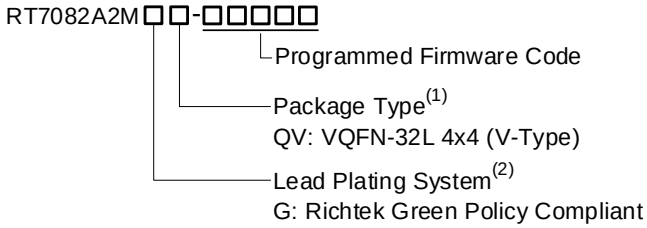
2 Applications

- Pedestal Fan
- Ventilation Fan
- Water Pump
- Vacuum Cleaner
- Server Fan

3 Features

- **Integrates 3-Phase PMSM/BLDC Controller, Gate Driver, Bootstrap Diodes, 5V LDO, and Gate Driver LDO**
- **Input Voltage Range: 6.5V to 30V**
- **Sensorless, Sine-Wave Field Oriented Control (FOC)**
- **Integrates Filters at ADC Input**
- **Protections: SCP, UVLO, Locked-Rotor, and Thermal Detection**
- **PMSM/BLDC Motor Controller**
  - **ARM 32-bit Cortex-M0 CPU, Frequency up to 60MHz**
  - **Memories Size: 16kB MTP, Internal ROM with Embedded Motor Control Library and 4kB SRAM**
  - **Power Management: Deep Sleep**
  - **Communication Interface: I^2C and UART**
  - **Configurable ADC Gain: x1, x4, and x8**
  - **6-Channel 12-Bit ADC**
    - **AD0 to AD3 for Differential Mode Current Sense**
    - **AD6 to AD9 for System Application**
  - **1-Channel Voltage Type 8-bit DAC**
- **Gate Driver**
  - **Floating Channel Designed for Bootstrap Operation**
  - **Programmable Supply Voltage**
  - **Programmable Sourcing Current**
  - **Sourcing/Sinking Current: 300mA/800mA**
  - **Built-In UVLO Functions for All Channels**
  - **Matched Propagation Delays for All Channels**
- **VQFN-32L 4x4 Package**

4 Ordering Information



Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

5 Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

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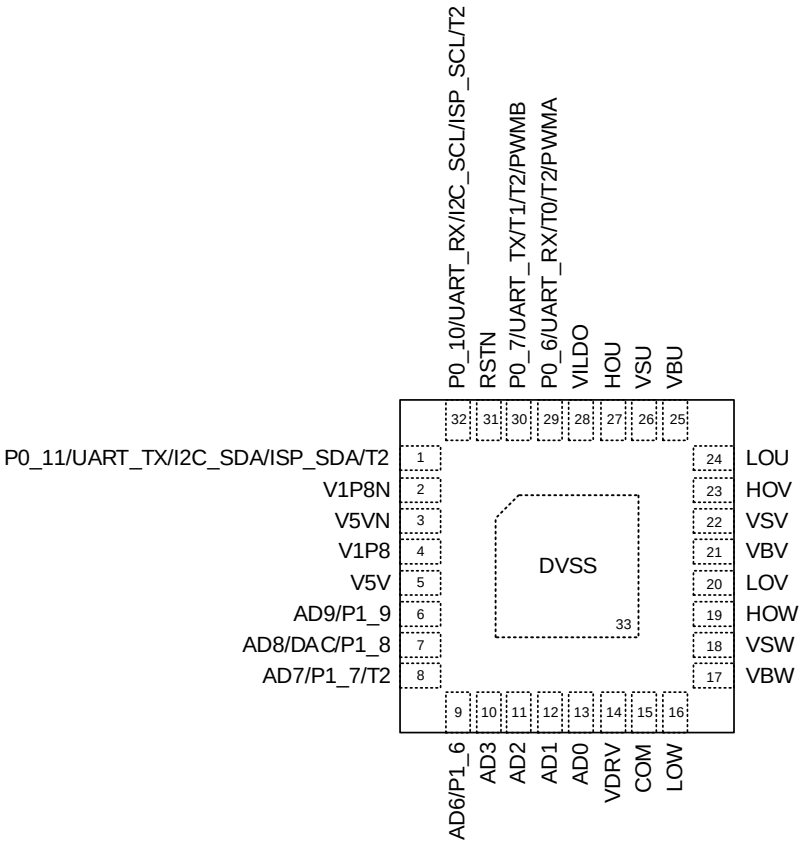
6 Pin Configuration

(TOP VIEW)



VQFN-32L 4x4

7 Functional Pin Description

Pin No.	Pin Name	Type	Pin Function
1	P0_11	DI/DO	Pin 11 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	I2C_SDA	DI/DO	I^2C data pin.
	ISP_SDA	DI/DO	In system programming data pin.
	T2	DI	T2 external enable or external clock input pin.
2	V1P8N	GND	Digital ground.
3	V5VN	GND	Analog ground.
4	V1P8	P	1.8V power pin.
5	V5V	P	5V power pin.
6	AD9	AI	ADC channel 9 input pin.
	P1_9	DI/DO	Pin 9 of GPIO port 1.

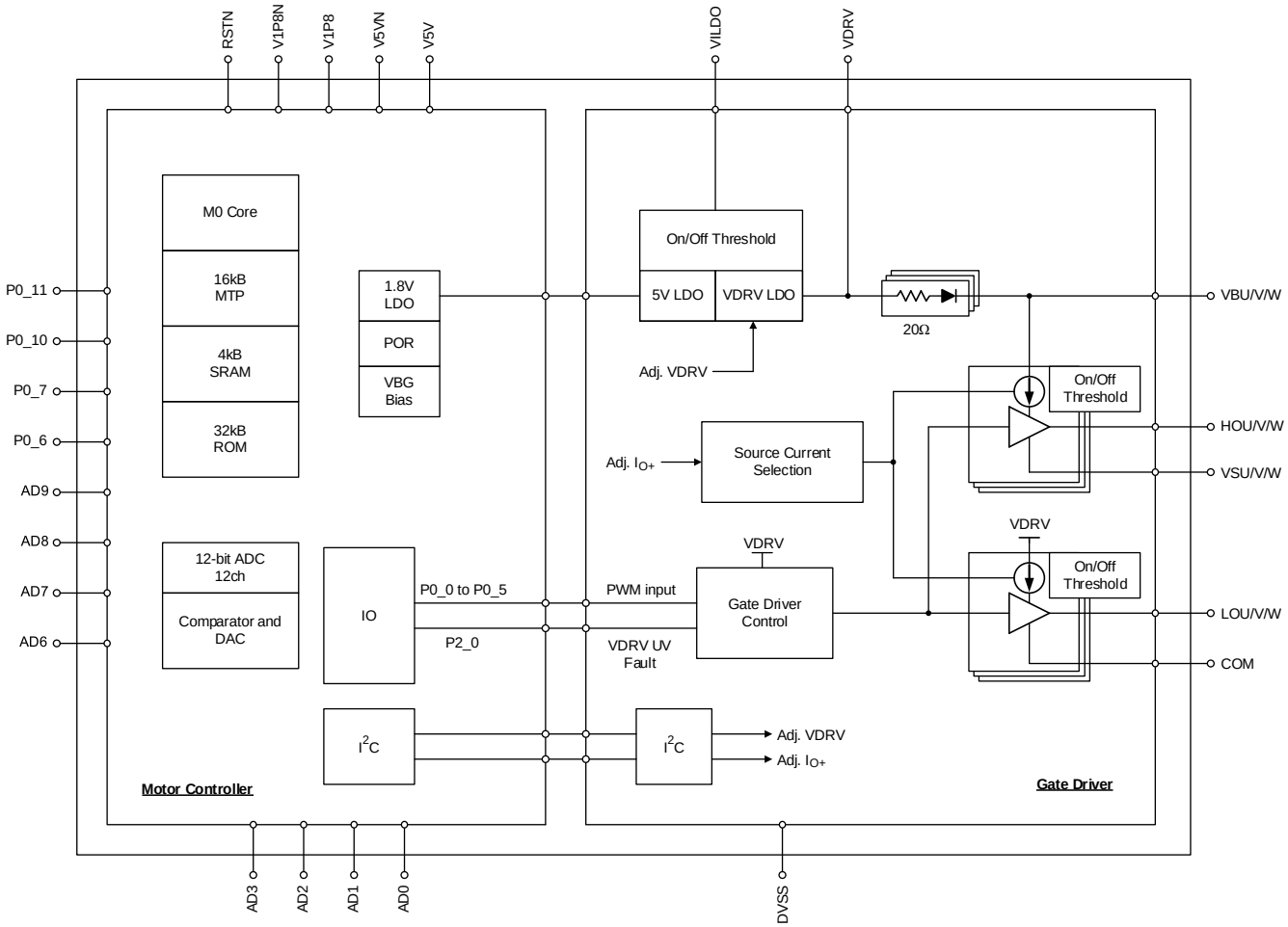
Pin No.	Pin Name	Type	Pin Function
7	AD8	AI	ADC channel 8 input pin.
	DAC	AO	Voltage type DAC output pin.
	P1_8	DI/DO	Pin 8 of GPIO port 1.
8	AD7	AI	ADC channel 7 input pin.
	P1_7	DI/DO	Pin 7 of GPIO port 1.
	T2	DI	T2 external enable or external clock input pin.
9	AD6	AI	ADC channel 6 input pin.
	P1_6	DI/DO	Pin 6 of GPIO port 1.
10	AD3	AI	ADC channel 3 for differential negative input pin only.
11	AD2	AI	ADC channel 2 for differential positive input pin only.
12	AD1	AI	ADC channel 1 for differential negative input pin only.
13	AD0	AI	ADC channel 0 for differential positive input pin only.
14	VDRV	P	High/Low-side driver supply voltage.
15	COM	GND	Gate driver ground.
16	LOW	VO	Low-side gate output of Phase W.
17	VBW	VI	High-side floating supply voltage of Phase W.
18	VSW	VI	High-side floating supply offset voltage of Phase W.
19	HOW	VO	High-side gate output of Phase W.
20	LOV	VO	Low-side gate output of Phase V.
21	VBV	VI	High-side floating supply voltage of Phase V.
22	VSV	VI	High-side floating supply offset voltage of Phase V.
23	HOV	VO	High-side gate output of Phase V.
24	LOU	VO	Low-side gate output of Phase U.
25	VBU	VI	High-side floating supply voltage of Phase U.
26	VSU	VI	High-side floating supply offset voltage of Phase U.
27	HOU	VO	High-side gate output of Phase U.
28	VILDO	P	LDO supply voltage.
29	P0_6	DI/DO	Pin 6 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	T0	DI	T0 external enable or external clock input pin.
	T2	DI	T2 external enable or external clock input pin.
	PWMA	DO	Programmable PWMA output pin.
30	P0_7	DI/DO	Pin 7 of GPIO port 0.
	UART_TX	DO	UART transmitting pin.
	T1	DI	T1 external enable or external clock input pin.
	T2	DI	T2 external enable or external clock input pin.
	PWMB	DO	Programmable PWMB output pin.
31	RSTN	DI	Low active reset pin.

Pin No.	Pin Name	Type	Pin Function
32	P0_10	DI/DO	Pin 10 of GPIO port 0.
	UART_RX	DI	UART receiving pin.
	I2C_SCL	DI/DO	I^2C clock pin.
	ISP_SCL	DI	In system programming clock pin.
	T2	DI	T2 external enable or external clock input pin.
33 (Exposed Pad)	DVSS	GND	Digital ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

7.1 IO Type Definition

DI: Digital Input Pin
DO: Digital Output Pin
AI: Analog Input Pin
AO: Analog Output Pin
P: Power Pin
VI: Voltage Input Pin
VO: Voltage Output Pin

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- LDO Supply Voltage, VILDO ---------- –0.3V to 40V
- Driver Supply Voltage, VDRV ---------- –0.3V to 15V
- Controller Supply Voltage, V5V ---------- –0.3V to 6.5V
- Controller Supply Voltage, V1P8 ---------- –0.3V to 2.5V
- VSU, VSV, VSW to COM ---------- –2V to 40V
- VSU, VSV, VSW to COM (Transient, 2μs) ---------- –5V to 40V
- VBU, VBV, VBW to COM ---------- –0.3V to 40V
- HOU, HOV, HOW to COM ---------- –0.3V to 40V
- LOU, LOV, LOW to COM ---------- –0.3V to 15V
- VSU, VSV, VSW dv/dt ---------- ±5V/ns
- Voltage of I/O Pin (P0_6, P0_7, P0_10, and P0_11) ---------- –0.3V to 6.5V
- Analog Input Voltage (AD0 to AD3 and AD6 to AD9) ---------- –0.3V to 6.5V
- Voltage of I/O Pin, RSTN ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  VQFN-32L 4x4 ---------- 3.59W
- Package Thermal Resistance (Note 3)

  VQFN-32L 4x4, θ_{JA} ---------- 27.8°C/W

  VQFN-48L 4x4, θ_{JC} ---------- 4.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

10 Recommended Operating Conditions

(Note 5)

- LDO Supply Voltage, VILDO ---------- 6.5V to 30V
- Driver Supply Voltage, VDRV ---------- 6V to 12V
- Controller Supply Voltage, V5V ---------- 4.5V to 5.5V
- VSU, VSV, VSW to COM ---------- –2V to 30V
- VSU, VSV, VSW to COM (Transient, 2μs) ---------- –3V to 30V
- VBU, VBV, VBW to COM ---------- 0V to 36V

- Digital I/O Pin (P0_6, P0_7, P0_10 and P0_11) ---------- 0V to 5V
- Analog Input Voltage (AD0 to AD3 and AD6 to AD9) ---------- 0V to 5V
- Voltage of I/O Pin, RSTN ---------- 0V to 5V
- LDO Capacitor on V5V ---------- 1μF
- LDO Capacitor on V1P8 ---------- 1μF
- Minimum Time Period of RSTN, t_{RSTN} ---------- 100μs
- Ambient Temperature Range ---------- –40°C to 105°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

11 Electrical Characteristics

(V_{V5V} = 5V, V_{VILDO} = 24V, V_{VDRV} = 7V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Section						
System Frequency	f_{SCLK}		58.8	60	61.2	MHz
Slow Clock for Sleep Mode	f_{LCLK}		77.6	80	82.4	kHz
LDO Section						
VILDO Turn-On Threshold	V_{VILDO_THON}		5	5.5	6	V
VILDO Turn-Off Threshold	V_{VILDO_THOFF}		4.5	5	5.5	V
VILDO Threshold Hysteresis	V_{VILDO_HYS}		--	0.5	--	V
V5V LDO Output Voltage	V_{V5V}		4.85	5	5.15	V
V5V Current at Operation Mode	I_{V5V_OPER}		--	20	--	mA
V5V Current at Deep Sleep Mode	I_{V5V_DSLP}		--	1.3	--	mA
V5V LDO Current Limit	I_{V5V_OC}	V_{VILDO} = 6.5V, V_{V5V} = 4.5V	70	--	--	mA
VDRV LDO Output Voltage	V_{VDRV}	As default	--	6	--	V
VDRV LDO Current Limit	I_{VDRV_OC}	V_{VILDO} = 6.5V, V_{VDRV} = 5V	20	--	--	mA
V1P8 LDO Turn-On Threshold	$V_{V1P8\_LDO\_THON}$		3.9	4.1	4.3	V
V1P8 LDO Turn-Off Threshold	$V_{V1P8\_LDO\_THOFF}$		3.4	3.6	3.8	V
V1P8 LDO Hysteresis	V_{V1P8_HYS}		--	0.5	--	V
V1P8 LDO Output Voltage	V_{V1P8}	C_{V1P8} = 1μF, I_{LOAD} = 40mA	1.62	1.8	1.98	V
V5V Undervoltage for Interrupt Flag	V_{V5V_UV}		4.1	4.3	4.5	V
V1P8 Undervoltage for Interrupt Flag	V_{1p8_UV}		--	1.5	--	V

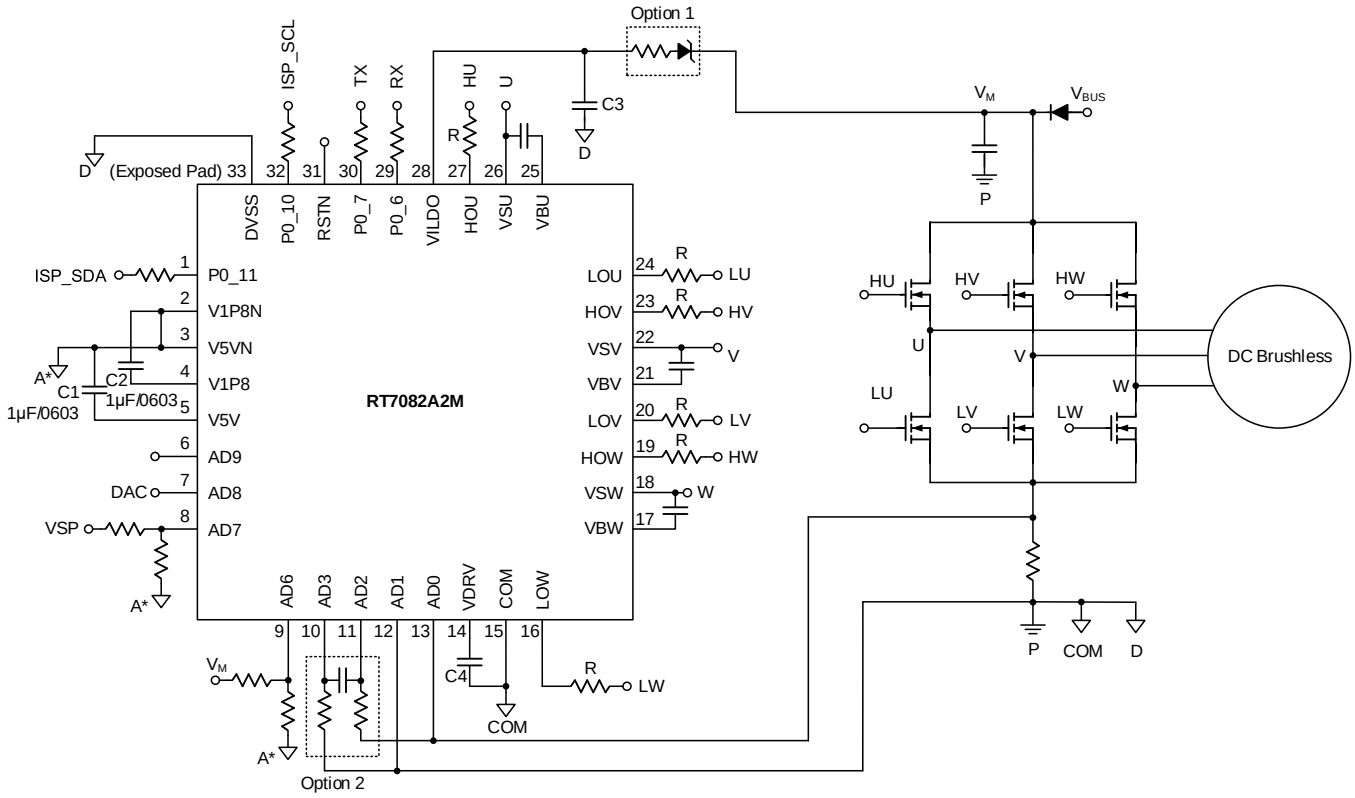
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Section (0V to 3V, 12-bit, Single End Mode, Gain = 1) (Note 6)						
Minimum Conversion Voltage	V_{I_MIN}	Code 000h	--	0	--	V
Maximum Conversion Voltage	V_{I_MAX}	Code FFFh	--	3	--	V
ADC Offset	V_{OFFSET}		–20	--	20	LSB
SCDAC Section (0V to 1.2V, 8-bit for Short Current) (Note 6)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	1.2	--	V
DAC Offset	V_{OFFSET}		–4	--	4	LSB
VDAC Section (0V to 3V, 8-bit for General Purposed Comparator) (Note 6)						
Minimum Conversion Voltage	V_{O_MIN}	Code 00h	--	0	--	V
Maximum Conversion Voltage	V_{O_MAX}	Code FFh	--	3	--	V
DAC Offset	V_{OFFSET}		–4	--	4	LSB
Output Resistance of DAC	R_O		--	5	--	kΩ
Current Limit Comparator (Short Circuit)						
Input Voltage Range of Comparator	V_{I_COMP}		0	--	1.2	V
Comparator Offset	V_{OFFSET}		–15	0	15	mV
General Purposed Comparator (Level Comparator)						
Input Voltage Range of Comparator	V_{I_COMP}		0.5	--	3	V
Comparator Offset	V_{OFFSET}		–20	0	20	mV
IO of P0_6 Section						
Input High Voltage	V_{IH}		2.2	2.6	3	V
Input Low Voltage	V_{IL}		1.1	1.6	2	V
Hysteresis	V_H		--	1	--	V
Pull-Up Resistor	R_{UP}		--	80	--	kΩ
Pull-Down Resistor	R_{DOWN}		--	40	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	5	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	10	--	mA
IO of P0_7, P0_10, and P0_11 Section						
Input High Voltage	V_{IH}		2.2	2.6	3	V
Input Low Voltage	V_{IL}		1.1	1.6	2	V
Hysteresis	V_H		--	1	--	V
Pull-Up Resistor	R_{UP}		--	40	--	kΩ
Pull-Down Resistor	R_{DOWN}		--	80	--	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	5	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	10	--	mA
IO of P1_6 to P1_9 Section						
Input High Voltage	V_{IH}		2.2	2.6	3	V
Input Low Voltage	V_{IL}		1.1	1.6	2	V
Hysteresis	V_H		--	1	--	V
Pull-Up Resistor	R_{UP}	Only P1_6/P1_7	--	80	--	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V5V	--	5	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V5V	--	10	--	mA
IO of RSTN						
Input High Voltage	V_{IH}		1.6	2	2.4	V
Input Low Voltage	V_{IL}		0.8	1	1.2	V
Hysteresis	V_H		0.6	1	1.4	V
Pull-Up Resistor	R_{UP}		20	40	60	kΩ
Debounce Time of RSTN High Voltage	t_{RSTN_H}		0.4	0.8	1.6	ms
Debounce Time of RSTN Low Voltage	t_{RSTN_L}		50	100	200	µs
IO of AD6 to AD9						
Time Constant of Input RC Filter at AD_FLT = 1	$t_{AD6-9FLT=1}$	Set register AD_FLT = 1, AD_FLT_ORD = 0	--	6	--	µs
Time Constant of Input RC Filter at AD_FLT = 0	$t_{AD6-9FLT=0}$	Set register AD_FLT = 0, AD_FLT_ORD = 0	--	1	--	µs
Bias Current at AD8 to AD9	I_{AD8-9_BIAS}		95	100	105	µA
I^2C Interface ($t_{SYS} = 1 / f_{SCLK}$)						
I^2C Clock Cycle Time	t_{SCL}		t_{SYS} x 80	--	--	ns
I^2C Start Bit Setup Time	t_{START}		--	t_{SCL} / 2	--	ns
I^2C Stop Bit Setup Time	t_{STOP}		--	t_{SCL} / 2	--	ns
I^2C Data Setup Time	t_{SETUP}		--	t_{SYS}	--	ns
I^2C Data Hold Time	t_{HOLD}		--	t_{SYS}	--	ns
Programmable VDRV of Gate Driver						
Minimum Driver Output Voltage	V_{VDRV_MIN}		5.7	6	6.3	V
Maximum Driver Output Voltage	V_{VDRV_MAX}		11.4	12	12.6	V
Driver Voltage Adjustment Step	V_{VDRV_Step}		--	0.5	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Side and Low-Side Driver Section						
High-Side Driver Turn-On Threshold	V_{HS_THON}		2.9	3.2	3.5	V
High-Side Driver Turn-Off Threshold	V_{HS_THOFF}		2.7	3	3.3	V
High-Side Threshold Hysteresis	V_{HS_HYS}		--	0.2	--	V
Low-Side Driver Turn-On Threshold	V_{LS_THON}		4	4.25	4.5	V
Low-Side Driver Turn-Off Threshold	V_{LS_THOFF}		3.85	4.05	4.25	V
Low-Side Threshold Hysteresis	V_{LS_HYS}		--	0.2	--	V
VDRV Operating Current	I_{VDRV_OP}	PWM = 20kHz (C_{OUT} = 1nF)	--	1.3	--	mA
VDRV Quiescent Current	I_{VDRV_Q}	LOU/V/W and HOU/V/W output low	--	--	1500	μA
VBS Quiescent Current for All Channels	I_{BSX_Q}	HOU/V/W output low	--	--	600	μA
Bootstrap Diode Forward Voltage	V_{D_BOOT}	Id = 5mA	--	0.8	--	V
		Id = 0.1A	--	2.9	--	
Resistance for Current Limitation	R_{LMT}	(Note 6)	--	20	--	Ω
The Different between Input Voltage and Output Voltage	V_{OH}	IO = 5mA, $V_{VBU/V/W}$ - $V_{HOU/V/W}$, V_{VDRV} - $V_{LOU/V/W}$ (Note 6)	--	50	--	mV
	V_{OL}	IO = –5mA, $V_{HOU/V/W}$ - $V_{VSU/V/W}$, $V_{LOU/V/W}$ - V_{COM} (Note 6)	--	20	--	
HOU/V/W and LOU/V/W Sourcing Current	I_{O+}	PWM input is high, $V_{VBSU/V/W}$ = V_{VDRV} = 7V, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = 2V (Note 6)	--	300	--	mA
HOU/V/W and LOU/V/W Sinking Current	I_{O-}	PWM input is low, $V_{HOU/V/W}$ = $V_{LOU/V/W}$ = 5V (Note 6)	--	800	--	mA
Turn-on Rise Time	t_R	V_{DRV} = 6V, C_{OUT} = 1nF (Note 6)	--	120	--	ns
Turn-off Fall Time	t_F	V_{DRV} = 6V, C_{OUT} = 1nF (Note 6)	--	60	--	ns
Turn-On Propagation Delay	t_{ON}	V_{DRV} = 6V	10	--	100	ns
Turn-Off Propagation Delay	t_{OFF}	V_{DRV} = 6V	10	--	100	ns
Delay Matching	MT	V_{DRV} = 6V, $V_{VSU/V/W}$ = 6V	--	--	50	ns
		V_{DRV} = 6V, $V_{VSU/V/W}$ = 30V	--	--	50	

Note 6. This parameter is guaranteed by design.

12 Typical Application Circuit



Note:
1. If C1 and C2 cannot be placed close to the IC, an additional 0.1µF capacitor should be placed close to the IC.
2. C3 should be placed as close as possible to the IC and DVSS (D).
3. C4 should be placed as close as possible to the IC and COM.
4. The resistor (R) can be between 3.3Ω and 10Ω for ESD protection.
5. A* is a separate loop, do not connect it to DVSS (D) and PGND (P).
6. Option 1 is to reduce power consumption of IC.
7. Option 2 is for power control demand.

13 Application Information

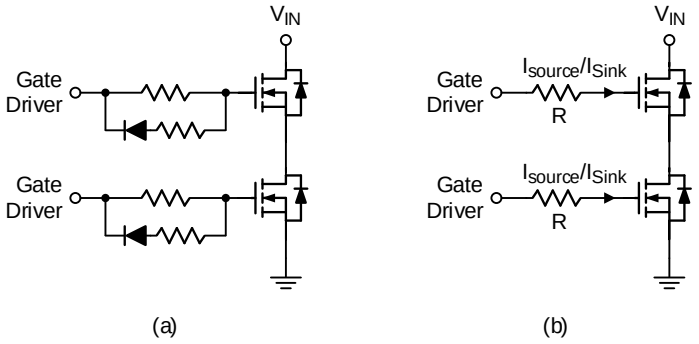
(Note 7)

13.1 Adjustable Gate Drive Voltage

In this application, the RT7082A2M supports programmable gate drive voltage. The voltage is set from 6V to 12V in increments of 0.5V per level through RICHTEK's GUI for BLDC.

13.2 Adjustable Gate Drive Source Current

Typically, gate drive current is controlled by the external gate resistors and diodes to fine-tune the switching speed of the MOSFET as shown in Figure 1(a). The RT7082A2M provides a function to adjust the gate drive source current without adding external components to the circuit, as shown in Figure 1(b). This feature can adjust the slew rate of the MOSFET, allowing the switching loss and EMI performance to be fine-tuned. The function can be enabled through RICHTEK's GUI for BLDC, allowing the gate drive current I_{source} can be adjusted from 20mA to 200mA. Additionally, disabling this function will fix I_{source} at 300mA..



Note: The resistance (R) can be 3.3Ω to 10Ω.

Figure 1. Gate Driver Output Circuit

13.3 Gate Driver Pre-Charge State

The pre-charge state provides a high current to drive the MOSFETs for approximately 40ns. This results in a quick gate voltage charge speed, further reducing the freewheeling time.

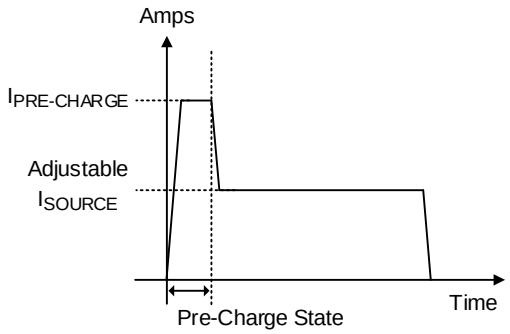


Figure 2. Gate Driver Turn-On Sequence

13.4 Negative Voltage of V_{phase}

When the high-side MOSFET turns off, a high di/dt current commutation is generated from the low-side MOSFET to the load during the switching transient. The fast transition slew rate, combined with parasitic inductance, induces a negative voltage spike that can be estimated with the equation $V_L = L \cdot di/dt$. The inductance $L = L_1 + L_2$ represents the parasitic inductance of the PCB trace and the wire bonding of the MOSFET.

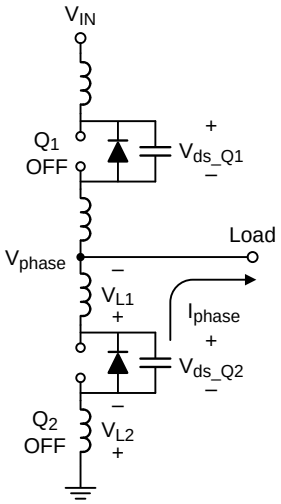


Figure 3. Negative V_{phase} Voltage Spike during Low-Side MOSFET Conducts Transition

According to the equation, higher parasitic inductance can contribute to a larger negative voltage at the V_{phase} point. To reduce the negative V_{phase} voltage, it is recommended to minimize the trace of the power loop and the distance between components. However, if the negative V_{phase} spike remains excessive, a further step can be taken as shown in Figure 4. A resistance between 3.3Ω and 10Ω is recommended for R_{ext}, which is placed between the VS pin and the switching node V_{phase}.

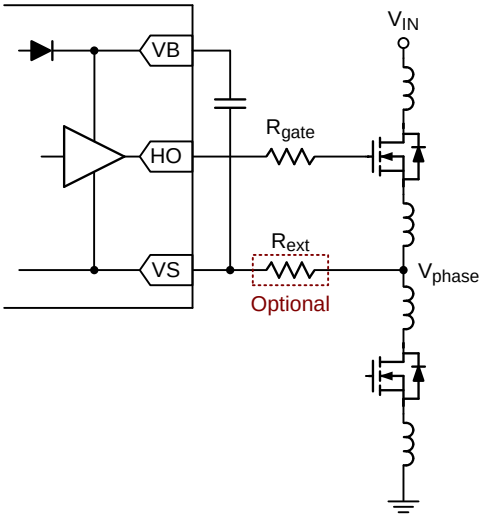


Figure 4. External Resistor between VS and V_{phase}

13.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to -ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-32L 4x4 package, the thermal resistance, θ_{JA}, is 27.8°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (27.8°C/W) = 3.59W for a VQFN-32L 4x4 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 5 allows the designer to estimate the effect of rising ambient temperature on the maximum power dissipation.

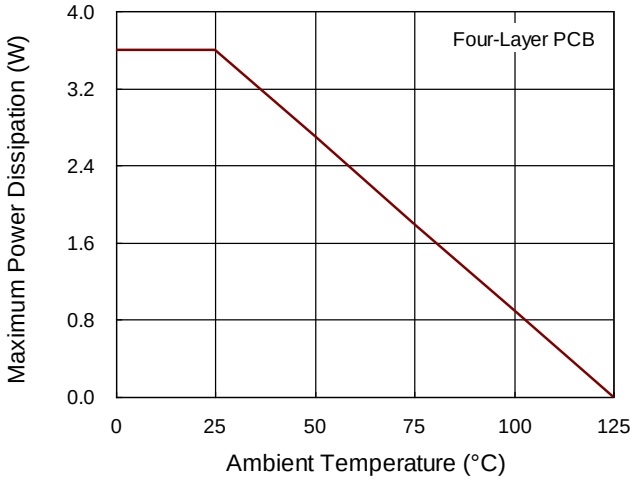
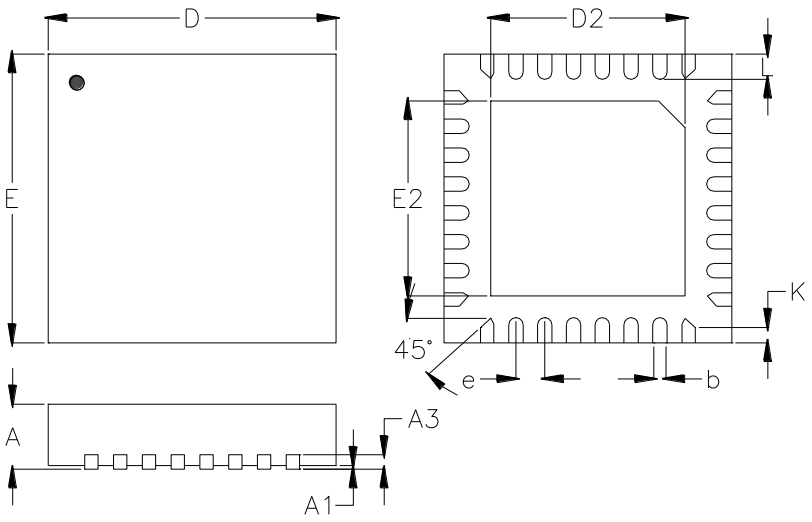
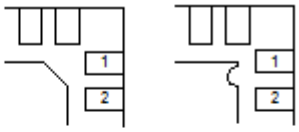


Figure 5. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

14 Outline Dimension





DETAIL A

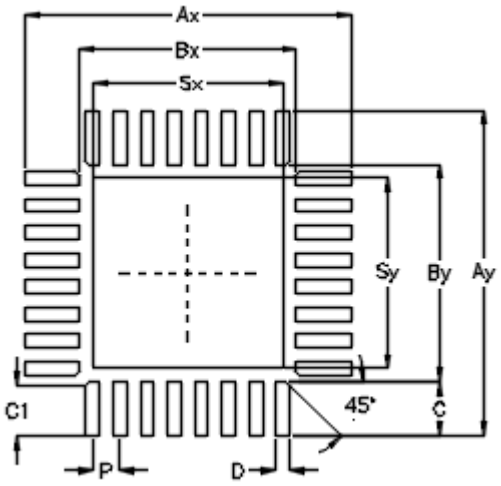
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	3.950	4.050	0.156	0.159
D2	2.650	2.750	0.104	0.108
E	3.950	4.050	0.156	0.159
E2	2.650	2.750	0.104	0.108
e	0.400		0.016	
L	0.300	0.400	0.012	0.016
K	0.200		0.008	

V-Type 32L QFN 4x4 Package

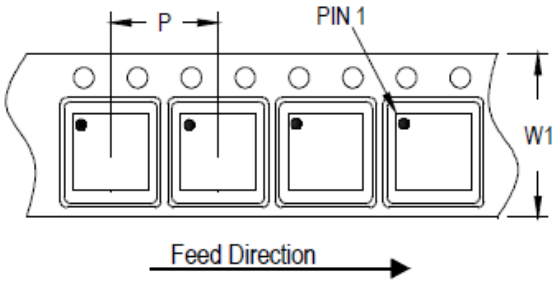
15 Footprint Information

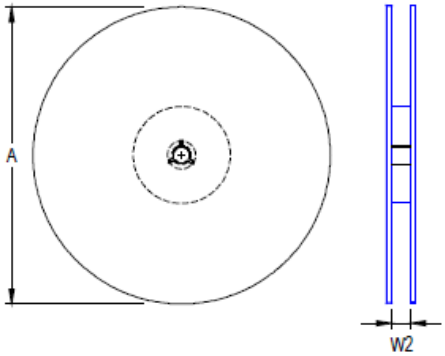


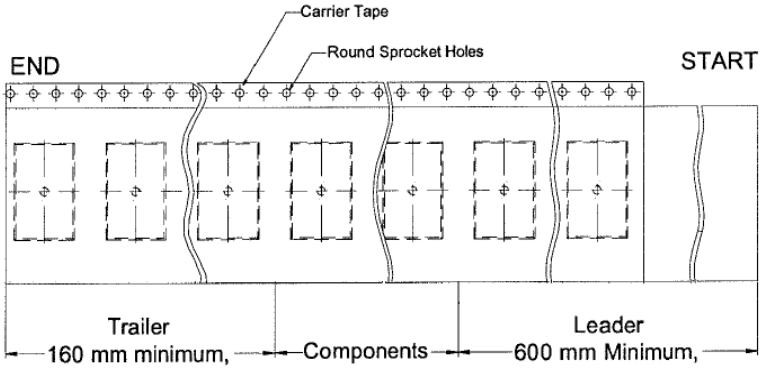
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C*32	C1*8	D	Sx	Sy	
V/W/U/XQFN4*4-32	32	0.40	4.80	4.80	3.20	3.20	0.80	0.75	0.20	2.80	2.80	±0.05

16 Packing Information

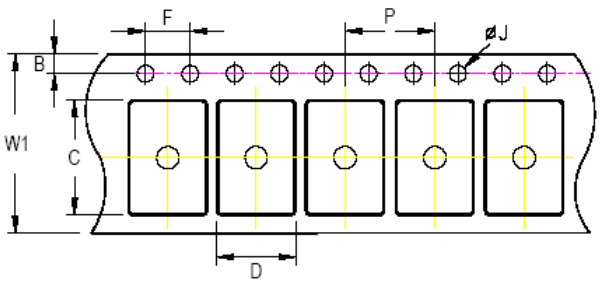
16.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 4x4	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

16.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
QFN/DFN 4x4	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

16.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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17 Datasheet Revision History

Version	Date	Description	Item
00	2024/6/7	Final	