RT6338

23V, 8A Synchronous Buck Converter with 3.3V/5V LDO

1 General Description

The RT6338 family is high efficiency synchronous buck converters with pseudo constant switching frequency 500kHz and delivers up to 8A output current. The RT6338A/B/F and RT6338AH/BH/FH operate from 4.5V to 23V input voltage. The output voltage of the RT6338A/AH/F/FH is programmed between 0.6V to 5.5V and RT6338B/BH is fixed to 3.3V output voltage. The input voltage of RT6338C/CH ranges from 5.2V to 23V and the output voltage of RT6338C/CH is fixed to 5.1V.

The RT6338 adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultra-fast transient response and further reduces the external component count. In steady states, the ACOT® operates at nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

By setting the voltage of the EN/MODE pin, the RT6338 operates either in diode emulation mode (DEM) or ultrasonic mode (USM) at light load. The USM maintains operation frequency above 25kHz, which eliminates the acoustic noise. In the DEM, the RT6338 provides the best light-load efficiency and improves the acoustic noise with spread spectrum function.

The RT6338 provides a PG indicator for easy system sequence control. Full protection features are also integrated in the device, including the cycle-by-cycle current limit, OVP, UVP, input UVLO, and OTP.

All above functions are integrated in a UQFN-23L 3x3 (FC) package. The recommended junction temperature is –40°C to 125°C.

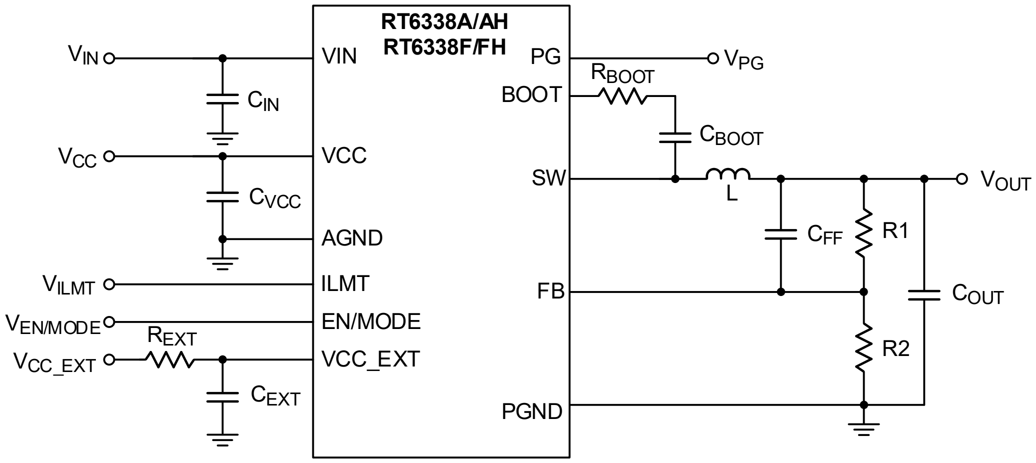
2 Applications

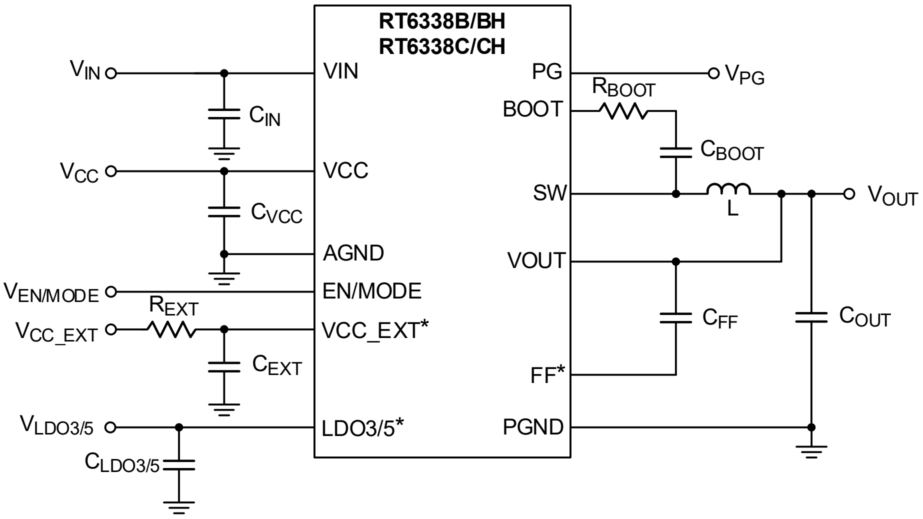
- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

3 Features

- **Input Voltage Range:**
  - **RT6338A/B/F and RT6338AH/BH/FH: 4.5V to 23V**
  - **RT6338C/CH: 5.2V to 23V**
- **Output Voltage:**
  - **RT6338A/AH/F/FH: 0.6V to 5.5V**
  - **RT6338B/BH: 3.3V**
  - **RT6338C/CH: 5.1V**
- **8A Continuous Output Current**
- **Stable with POSCAP and MLCC Capacitor**
- **Fast Transient Response**
- **Diode Emulation Mode (DEM) for Power Saving**
- **Ultrasonic Mode (USM) for Avoiding Acoustic Noise**
- **Pseudo Constant Switching Frequency 500kHz in CCM**
- **Internal Power MOSFET Switch 26mΩ (High-Side) and 14mΩ (Low-Side)**
- **Up to 98% Duty for 2S Battery Application (RT6338B/BH/C/CH)**
- **LDO**
  - **RT6338B/BH: 3.3V/100mA**
  - **RT6338C/CH: 5V/100mA**
- **Overcurrent Limit:**
  - **RT6338A/AH/F/FH: Adjustable (10A, 12A or 14A)**
  - **RT6338B/BH/C/CH: 12A**
- **Output Undervoltage/Overvoltage Protection (UVP/OVP)**
  - **RT6338A/B/C: Latched Mode UVP/OVP**
  - **RT6338AH/BH/CH: Hiccup Mode UVP and Non-Latched Mode OVP**
- **Input Undervoltage-Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**
  - **RT6338A/B/C: Latched Mode OTP**
  - **RT6338AH/BH/CH: Non-Latched Mode OTP**

4 Simplified Application Circuit





Pin Name	RT6338B/BH	RT6338C/CH
LDO3/5* (Pin 23)	✓ (LDO3)	✓ (LDO5)
VCC_EXT* (Pin 21)	✓	N/A
FF* (Pin 21)	N/A	✓

5 Ordering Information

RT6338 □□□

Package Type(1)
QUF: UQFN-23L 3x3 (FC) (U-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

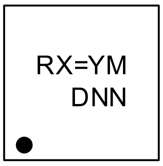
Output Voltage & Protection Option & Operation Mode
A: Adjustable & Latched Mode(3), USM/DEM
B: 3.3V & Latched Mode(3), USM/DEM
C: 5.1V & Latched Mode(3), USM/DEM
F: Adjustable & Latched Mode(3), FCCM/DEM
AH: Adjustable & Hiccup Mode(4), USM/DEM
BH: 3.3V & Hiccup Mode(4), USM/DEM
CH 5.1V& Hiccup Mode(4)), USM/DEM
FH: Adjustable & Hiccup Mode(4), FCCM/DEM

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.
- Marked with (3) indicated: Latched mode for UVP, OVP, and OTP.
- Marked with (4) indicated: Hiccup mode for UVP & Non-latched mode for OVP and OTP.

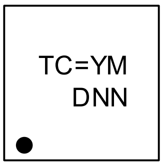
6 Marking Information

RT6338AGQUF



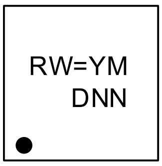
RX= : Product Code
YMDNN : Date Code

RT6338AHGQUF



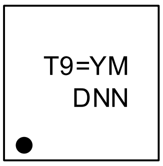
TC= : Product Code
YMDNN : Date Code

RT6338BGQUF



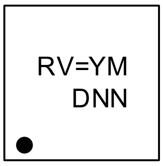
RW= : Product Code
YMDNN : Date Code

RT6338BHGQUF



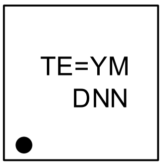
T9= : Product Code
YMDNN : Date Code

RT6338CGQUF



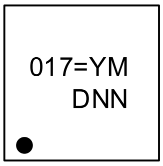
RV= : Product Code
YMDNN : Date Code

RT6338CHGQUF



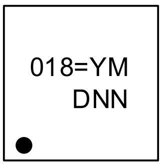
TE= : Product Code
YMDNN : Date Code

RT6338FGQUF



017= : Product Code
YMDNN : Date Code

RT6338FHGQUF

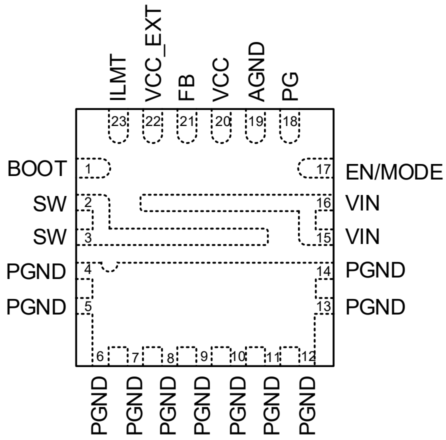


018= : Product Code
YMDNN : Date Code

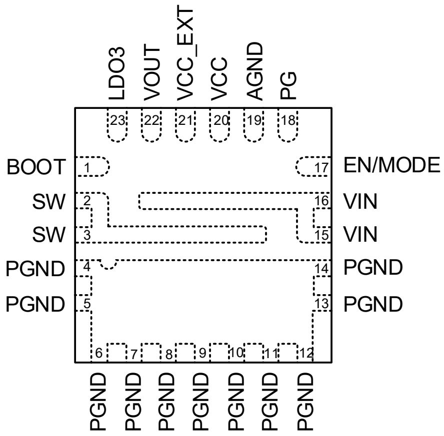
Table of Contents

7 Pin Configuration

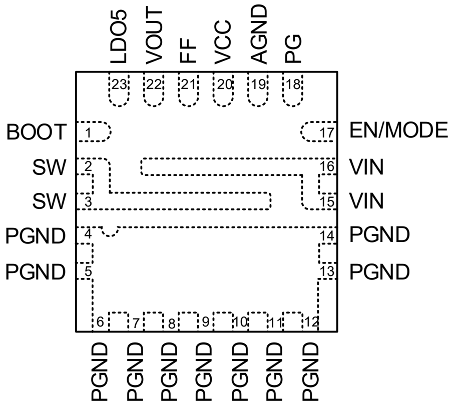
(TOP VIEW)



RT6338A/AH
RT6338F/FH



RT6338B/BH



RT6338C/CH

UQFN-23L 3x3 (FC)

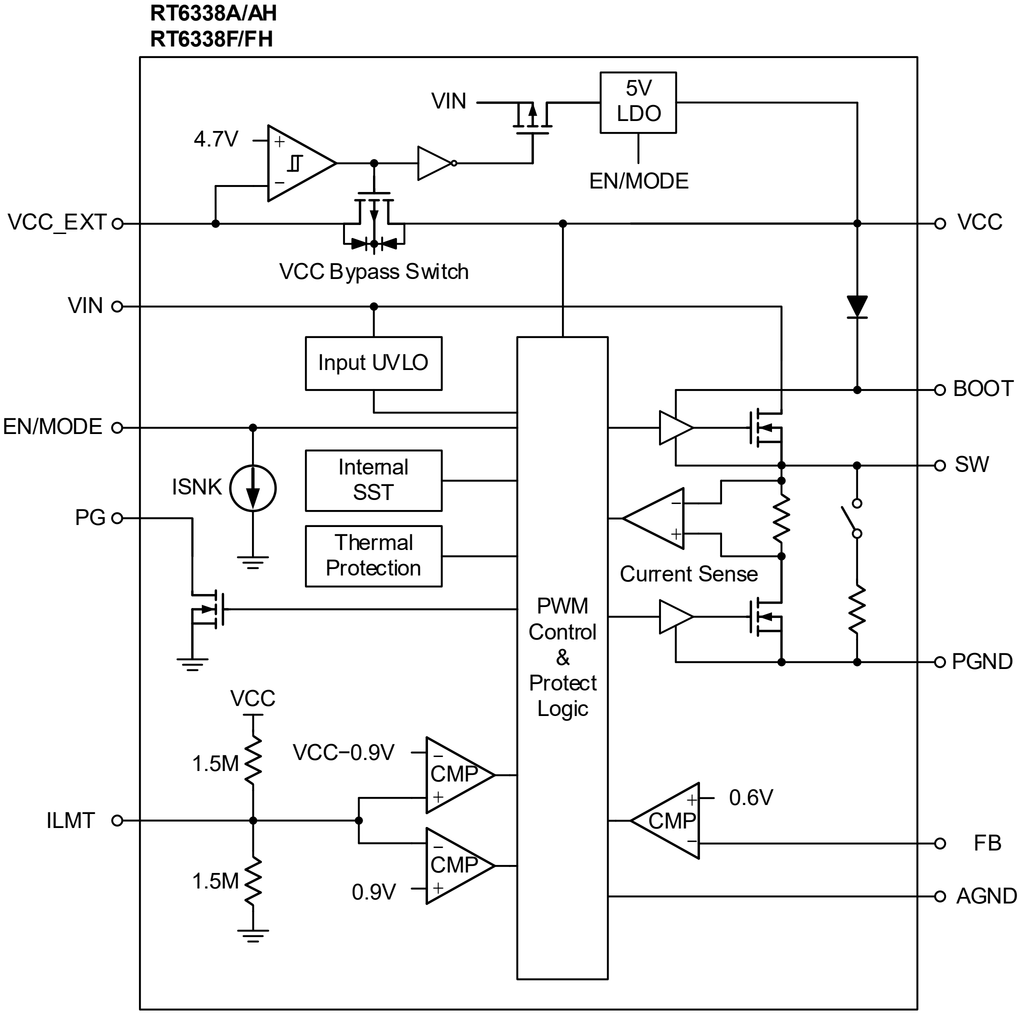
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high-side gate driver. Connect a high quality and low ESR ceramic capacitor (minimum C = 0.1μF/0603) from the BOOT pin to the SW pin through a short and low inductance paths. During the period of low-side MOSFET turn-on, the bootstrap capacitor is charged by the BOOT pin to store required energy for the high-side gate driver. A bootstrap resistor (0603 size, ≤ 10Ω) in series with the bootstrap capacitor is strongly recommended for reducing the voltage spike at the SW node.
2, 3	SW	Switch node of the buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. SW is also used for the internal ramp generation, on-time generation and current detection. Connect this pin to output inductor and keep the sensitive trace and signals away.
4 to 14	PGND	Ground return from low-side power MOSFET and its driver. Directly soldering to a large PCB PGND plane and connecting thermal vias under the PGND pin are required to minimize the parasitic impedance and thermal resistance.
15, 16	VIN	Input voltage pin. The VIN pin is used to supply the internal bias voltage, VCC and LDO. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805x2 + 0.1μF/0603x1) as close as possible from the VIN pin to the PGND pin is necessary.

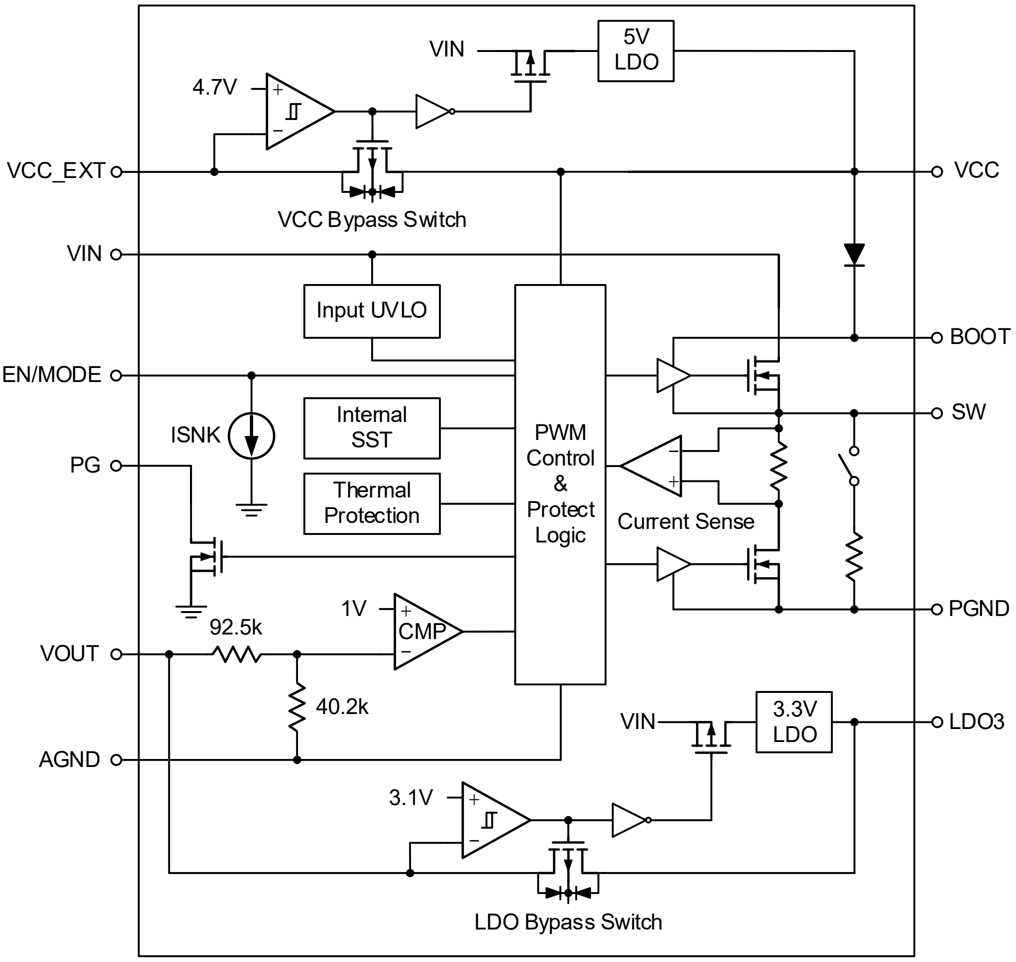
Pin No.	Pin Name	Pin Function
17	EN/MODE (RT6338A/B/C/AH/BH/CH)	Enable and operation mode control input. In order to ensure the IC logic status of turn-on/off, the low logic time length of EN/MODE control signal must be larger than 0.5μs. DO NOT leave this pin floating. The RT6338 supports either in diode emulation mode (DEM) and ultrasonic mode (USM) at light load (Table 3) through setting the voltage of the EN/MODE pin. Regarding the EN/MODE control logic of the RT6338, refer to Table 4.
	EN/MODE (RT6338F/FH)	Enable and operation mode control input. In order to ensure the IC logic status of turn-on/off, the low logic time length of EN/MODE control signal must be larger than 0.5μs. DO NOT leave this pin floating. The RT6338 supports either in diode emulation mode (DEM) and Continuous Conduction Mode (FCCM) at light load (Table 3, Table 4, and Table 5) through setting the voltage of the EN/MODE pin. Regarding the EN/MODE control logic of the RT6338, refer to Table 4.
18	PG	Power-good indicator is an open-drain output. This pin is pulled low as UVP, OVP, OTP, EN/MODE low or output voltage is not regulated (such as before soft-start). An external pull-up resistor to VCC or other external rail is required, and the recommended pull-up resistor ranges from 10kΩ to 100kΩ. Do not pull the PG voltage higher than 6V.
19	AGND	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
20	VCC	Internal LDO output. Used as supply to internal control circuits. DO NOT connect to any external loads. Connect a high-quality capacitor (C = 1μF/0603) from this pin to AGND. When the voltage on VCC_EXT (RT6338A/AH/B/BH) or VOUT (RT6338C/CH) pin is higher than "VCC bypass switch turn-on voltage", the VCC will be internally switchover to VCC_EXT (or VOUT) to reduce power consumption (refer to Figure 4 and Figure 5).
21	FB (RT6338A/AH/F/FH)	Feedback voltage input. A resistor divider from V_{OUT} to FB sets the desired V_{OUT} level. V_{OUT} is regulated by FB tracking internal reference voltage 0.6V. Further, FB is used to detect output voltage status for OVP, UVP, or PG. If the FB voltage is below 60% of the internal reference 0.6V, the UVP is triggered. If the FB voltage is greater than 120% of the internal reference 0.6V, the OVP is triggered. After soft-start is completed, if the FB voltage is greater than 90% of the internal reference 0.6V, PG is pulled high. Conversely, if the FB voltage is below 74% of the internal reference 0.6V, PG is pulled low.
	VCC_EXT (RT6338B/BH)	External voltage input for VCC. If an external 5V supply voltage is applied to the VCC_EXT pin, VCC will be internally switched over to the VCC_EXT pin and the internal LDO of VCC will be disabled for further reducing the power consumption. In order to avoid any noise disturbance including switching noise, an external 5V supply voltage must be stable and constant. Hence, a RC filter (R = 1.1Ω/0603 and C = 4.7μF/0603) is required between an external 5V supply voltage and the VCC_EXT pin. It should be placed as close as possible to the VCC_EXT pin. Leave the VCC_EXT pin floating if this pin is not used.

Pin No.	Pin Name	Pin Function
	FF (RT6338C/CH)	Output feedforward pin. The FF pin is connected between internal divider resistors. A proper feedforward capacitor connecting from the VOUT pin to the FF pin can enhance the transient performance. Furthermore, the FF pin is used to detect the output voltage status for OVP, UVP, or PG. If the FF voltage is below 60% of the internal reference 1V, the UVP is triggered. If the FF voltage is greater than 120% of the internal reference 1V, the OVP is triggered. After soft-start is completed, if the FF voltage is greater than 90% of the internal reference 1V, PG is pulled high. Conversely, if the FF voltage is below 77% of the internal reference 1V, PG is pulled low.
22	VCC_EXT (RT6338A/AH/F/FH)	External voltage input for VCC. If an external 5V supply voltage is applied to the VCC_EXT pin, VCC will be internally switchover to the VCC_EXT pin and the internal LDO of VCC will be disabled for further reducing the power consumption. In order to avoid any noise disturbance including switching noise, an external 5V supply voltage must be stable and constant. Hence, a RC filter (R = 1.1Ω/0603 and C = 4.7μF/0603) is required between an external 5V supply voltage and the VCC_EXT pin. It should be placed as close as possible to the VCC_EXT pin. Leave the VCC_EXT pin floating if this pin is not used.
	VOUT (RT6338B/BH)	Output voltage sense pin. Connect to the output of buck converter. LDO3 (3.3V) will be internally switched over to the VOUT pin when the LDO bypass switch is turned on. Furthermore, the VOUT pin is used to detect the output voltage status for OVP, UVP or PG. If the output voltage is below 60% of the fixed output voltage 3.3V, the UVP is triggered. If the output voltage is greater than 120% of the fixed output voltage 3.3V, the OVP is triggered. After soft-start is completed, if the output voltage is greater than 90% of the fixed output voltage 3.3V, PG is pulled high. Conversely, if the output voltage is below 77% of the fixed output voltage 3.3V, PG is pulled low.
	VOUT (RT6338C/CH)	Output voltage sense pin. Connect to the output of the buck converter. LDO5 (5V) and VCC will be internally switched over to the VOUT pin when the VCC and LDO bypass switches are turned on.
23	ILMT (RT6338A/AH)	Valley current limit setting pin. 10A: Connect the ILMT pin to PGND. 12A: Leave the ILMT pin floating/open. 14A: Connect the ILMT pin to 5V.
	ILMT (RT6338F/FH)	Valley current limit setting pin. 5A: Connect the ILMT pin to PGND. 7A: Leave the ILMT pin floating/open. 9A: Connect the ILMT pin to 5V.
	LDO3 (RT6338B/BH)	Internal 3.3V LDO output. Bypass a capacitor (10μF/0603) to PGND. This pin is capable of sourcing 100mA. When the input voltage exceeds the UVLO rising threshold, the internal 3.3V LDO is enabled. Besides, LDO3 switches over to the VOUT pin after the soft-start period is finished.
	LDO5 (RT6338C/CH)	Internal 5V LDO output. Bypass a capacitor (10μF/0603) to PGND. This pin is capable of sourcing 100mA. When the input voltage exceeds the UVLO rising threshold, the internal 5V LDO is enabled. Besides, LDO5 switches over to the VOUT pin after the soft-start period is finished.

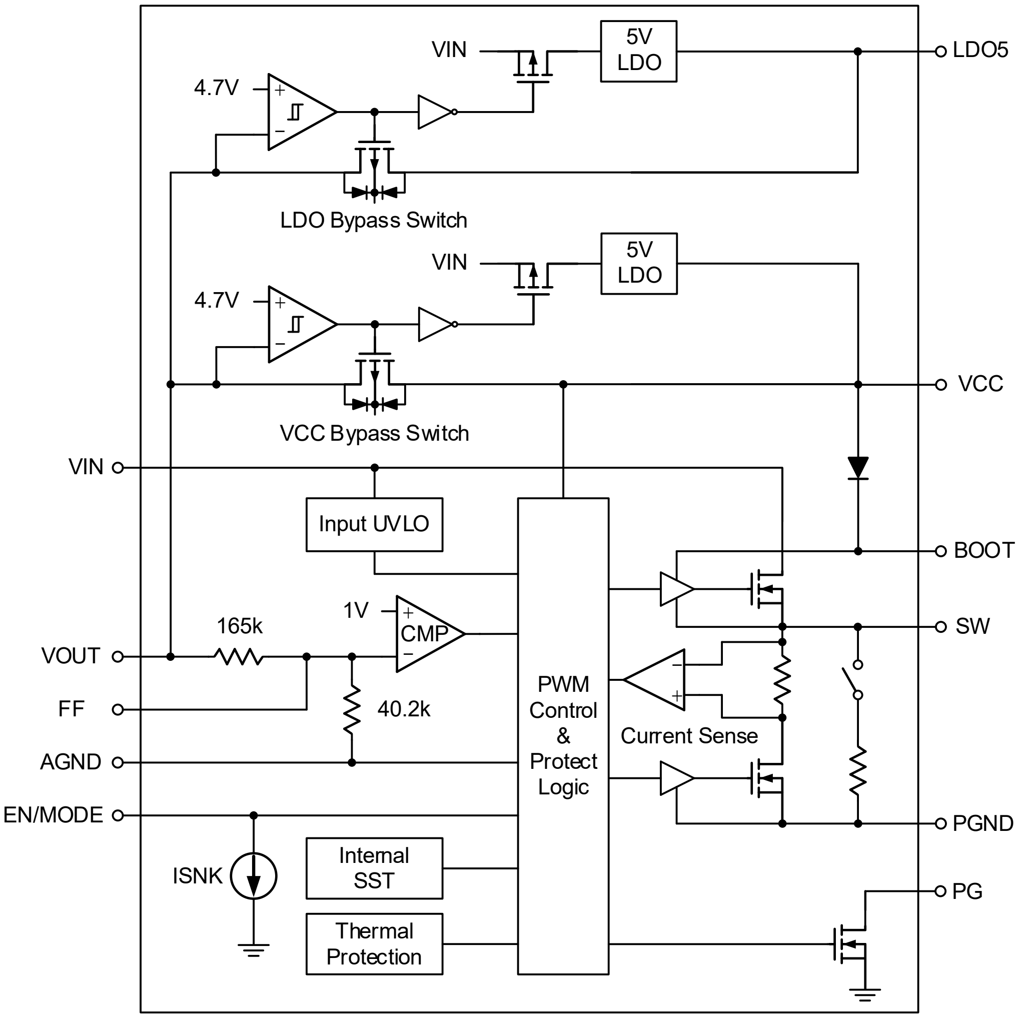
9 Functional Block Diagram



RT6338B/BH


5V LDO
VIN
4.7V
VCC_EXT
VCC
VCC Bypass Switch
VIN
Input UVLO
BOOT
EN/MODE
SW
ISNK
Internal SST
PWM Control & Protect Logic
PG
Thermal Protection
Current Sense
PGND
1V
CMP
92.5k
VOUT
40.2k
VIN
3.3V LDO
LDO3
AGND
3.1V
LDO Bypass Switch

RT6338C/CH


VIN
5V
LDO
LDO5
4.7V
+
−
LDO Bypass Switch
VIN
5V
LDO
4.7V
+
−
VCC
VCC Bypass Switch
VIN
Input UVLO
BOOT
1V
+
CMP
−
SW
165k
VOUT
FF
40.2k
PWM
Control
&
Protect
Logic
−
+
Current Sense
AGND
PGND
EN/MODE
ISNK
Internal
SST
Thermal
Protection
PG

10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, V_{IN} -- –0.3V to 28V
- Enable/Mode Pin Voltage, $V_{EN/MODE}$ -- –0.3V to 28V
- VCC Pin Voltage, V_{CC} -- –0.3V to 6.5V
- VOUT Pin Voltage, V_{OUT} (RT6338B/BH) -- –0.3V to 4.5V
- VOUT Pin Voltage, V_{OUT} (RT6338C/CH) -- –0.3V to 6.5V
- Switch Voltage, V_{SW} -- –0.3V to (V_{IN} + 0.3V)
  <10ns -- –10V to 38V
  <5ns -- –14V to 38V
- Boot Voltage, V_{BS} -- (V_{SW}–0.3V) to (V_{SW} + 6V)
- Other I/O Pin Voltages -- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) -- 260°C
- Junction Temperature -- 150°C
- Storage Temperature Range -- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- ESD Susceptibility
  HBM (Human Body Model) -- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage (RT6338A/AH/B/BH/F/FH) -- 4.5V to 23V
- Supply Input Voltage (RT6338C/CH) -- 5.2V to 23V
- Junction Temperature Range -- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		UQFN-23L 3x3 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	40.8	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	6.8	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	4.2	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	30.6	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	0.14	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board (Richtek EVB) which is in size of 140mm x 90mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 12V. The typical values are referenced to T_A = T_J = 25°C. Both minimum and maximum values are referenced to T_A = T_J from −10°C to 105°C. Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Voltage Range	V_{IN}	RT6338A/AH/B/BH/F/FH	4.5	--	23	V
		RT6338C/CH	5.2	--	23	
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	RT6338A/AH/F/FH: $V_{EN/MODE}$ = 0V	--	5	--	μA
		RT6338B/C and RT6338BH/CH: $V_{EN/MODE}$ = 0V	--	40	--	μA
Supply Current (Quiescent)	I_Q	RT6338A/AH/F/FH: $V_{EN/MODE}$ = 5V (diode emulation mode), V_{OUT} = V_{SET} x 105%, not switching	70	85	105	μA
		RT6338B/BH: $V_{EN/MODE}$ = 5V (diode emulation mode), V_{OUT} = V_{SET} x 105%, not switching RT6338C/CH: $V_{EN/MODE}$ = 5V (diode emulation mode), V_{FF} = 1 x 105%, not switching	75	95	130	μA
UVLO						
UVLO Rising Threshold	V_{UVLO_Rising}	RT6338A/AH/B/BH/F/FH	3.8	4.1	4.4	V
		RT6338C/CH	4.1	4.4	4.7	
UVLO Hysteresis	V_{HYS}		--	0.3	--	V

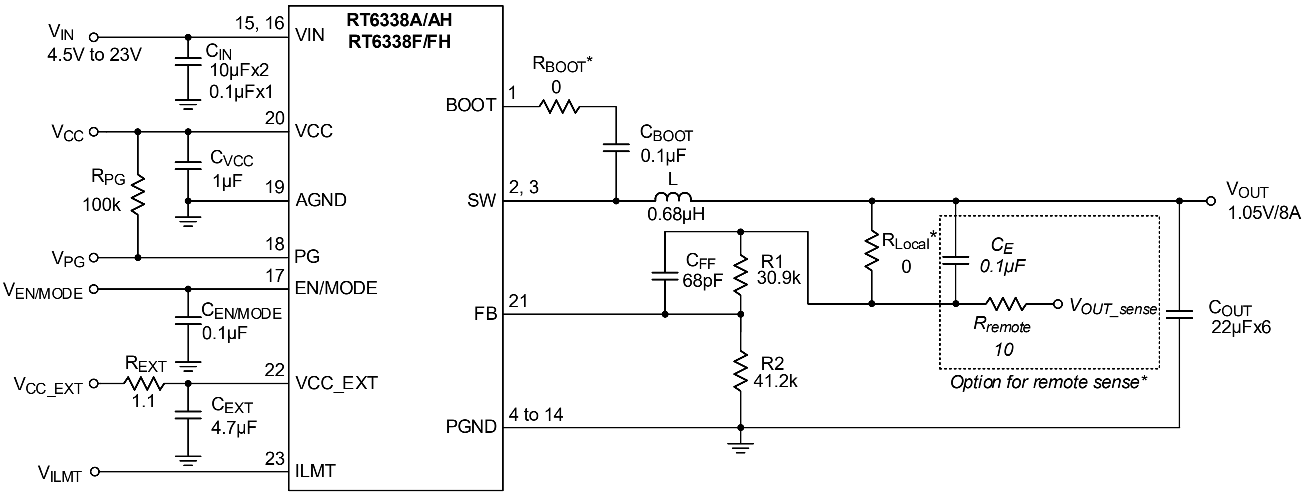
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Enable/Mode Logic Threshold and Timing						
EN/MODE Input High Voltage	$V_{EN/MODE\_H}$		400	635	880	mV
EN/MODE Input Low Voltage	$V_{EN/MODE\_L}$		230	500	800	mV
EN/MODE Input Current	$I_{EN/MODE}$	$V_{EN/MODE}$ = 0.1V	0	2	4	μA
Ultrasonic Mode	$V_{EN/MODE}$	RT6338A/AH/B/BH/C/CH	0.88	--	1.7	V
Diode Emulation Mode	$V_{EN/MODE}$		2.3	--	--	V
Force Continuous Conduction Mode	$V_{EN/MODE}$	RT6338F/FH	0.88	--	1.7	V
Output Voltage						
Output Voltage Set Point	V_{OUT}	RT6338B/BH; $T_A = T_J = 25°C$, CCM	3.267	3.3	3.333	V
		RT6338C/CH; $T_A = T_J = 25°C$, CCM	5.049	5.1	5.151	
VCC Regulator Voltage	V_{CC}		--	5	--	V
Feedback Reference						
Feedback Reference Voltage	V_{REF}	RT6338A/AH: $T_A = T_J = 25°C$, CCM	0.594	0.6	0.606	V
Feedback Input Current	I_{FB}	RT6338A/AH: V_{FB} = 4V	–100	--	100	nA
On-Resistance						
High-Side MOSFET On-Resistance	$R_{DS(ON)\_H}$	$T_A = T_J = 25°C$	--	26	--	mΩ
Low-Side MOSFET On-Resistance	$R_{DS(ON)\_L}$	$T_A = T_J = 25°C$	--	14	--	mΩ
Discharge MOSFET On-Resistance	R_{DISCHG}	$T_A = T_J = 25°C$, $V_{EN/MODE}$ = 0V. From SW to PGND	30	50	100	Ω
Current Limit						
Low-Side MOSFET Valley Current Limit	I_{LIM_VY}	RT6338A/AH/F/FH: $T_A = T_J = 25°C$; ILMT = 0V	8	10	12	A
		ILMT = Open	10	12	15	
		ILMT = 5V	11	14	17	
		RT6338B/C and RT6338BH/CH: $T_A = T_J = 25°C$	10	12	15	A
ILMT Rising Threshold	V_{ILMTH}	RT6338A/AH/F/FH	V_{CC} –0.9	--	V_{CC}	V
ILMT Falling Threshold	V_{ILMTL}	RT6338A/AH/F/FH	--	--	0.9	V
Negative over Current Limit		RT6338F/FH: $T_A = T_J = 25°C$	--	–4.5	--	A
Oscillator Frequency						
Oscillator Frequency	f_{OSC}		400	500	600	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	55	--	ns

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Minimum Off-Time	t_{OFF_MIN}	RT6338A/AH/F/FH		--	260	--	ns
		RT6338B/C and RT6338BH/CH		--	200	--	
Ultrasonic Mode							
Operation Period	t_{USM}			20	30	40	μs
Soft-Start							
Soft-Start Time	t_{SS}	RT6338A/AH/F/FH	$T_A = T_J = 25°C$, from EN/MODE high to PG high	1.8	2.4	2.9	ms
		RT6338B/C and RT6338BH/CH		1.5	2.1	2.6	
Output Rising Time	t_R	RT6338A/AH/F/FH	$T_A = T_J = 25°C$, from 10% to 90% V_{OUT}	--	0.5	0.75	ms
		RT6338B/C and RT6338BH/CH		--	0.7	1.05	ms
Output Overvoltage Protection							
Output Overvoltage Threshold		RT6338A/AH/C/CH/F/FH: V_{FB}/V_{FF} rising		114	120	126	%
		RT6338B/BH: V_{OUT} rising					
Output Overvoltage Hysteresis		RT6338AH/FH		--	8	--	%
		RT6338BH/CH		--	5	--	
Output Overvoltage Deglitch Time				--	11	--	μs
Output Undervoltage Protection							
Output Undervoltage Falling Threshold		RT6338A/AH/C/CH/F/FH: V_{FB}/V_{FF} falling		54	60	64	%
		RT6338B/BH: V_{OUT} falling					
Output Undervoltage Rising Threshold		RT6338A/AH/C/CH/F/FH: V_{FB}/V_{FF} rising		--	72	--	%
		RT6338B/BH: V_{OUT} rising					
Output Undervoltage Deglitch Time		RT6338A/AH/C/CH/F/FH: force V_{FB}/V_{FF} below UVP falling threshold until SW stop switching.		--	11	--	μs
		RT6338B/BH: force V_{OUT} below UVP falling threshold until SW stop switching.					
UV Blank Time		RT6338A/AH/F/FH	From EN/MODE high	1.8	2.4	2.9	ms
		RT6338B/C and RT6338BH/CH		1.5	2.1	2.6	
Power Good							
Power-Good Threshold		RT6338A/AH/C/CH/F/FH: V_{FB}/V_{FF} rising		87	90	93	%
		RT6338B/BH: V_{OUT} rising					
Power-Good Hysteresis		RT6338A/AH/F/FH: $T_A = T_J = 25°C$		--	16	--	%
		RT6338B/C and RT6338BH/CH: $T_A = T_J = 25°C$		--	13	--	

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Power-Good Low Deglitch Time				--	11	--	μs
LDO Regulator							
LDO Output Voltage	V_{LDO3}	RT6338B/BH	$T_A = T_J = 25°C$, $V_{EN/MODE} = 0V$, no bypass	3.25	3.3	3.35	V
	V_{LDO5}	RT6338C/CH		4.925	5	5.075	
LDO Dropout Voltage	V_{DROP}	$I_{LDO} = 20mA$, $V_{EN/MODE} = 0V$, no bypass. (Note 7)		--	200	--	mV
LDO Output Current Limit	I_{LIM_LDO}			120	200	300	mA
LDO Bypass Switch							
LDO Bypass Switch On-Resistance	R_{BYP_LDO}	RT6338B/BH	$T_A = T_J = 25°C$	--	3	--	Ω
		RT6338C/CH		--	1.2	--	
LDO Bypass Switch Turn-On Voltage	$V_{BYP\_LDO\_ON}$	RT6338B/BH		2.9	3.1	3.3	V
		RT6338C/CH		4.55	4.7	4.85	
Bypass Switch Switchover Hysteresis		RT6338B/C and RT6338BH/CH		0.1	0.2	0.3	V
VCC Bypass Switch							
VCC Bypass Switch On-Resistance	V_{BYP_VCC}	$T_A = T_J = 25°C$		--	4.75	--	Ω
VCC Bypass Switch Turn-On Voltage	$V_{BYP\_VCC\_ON}$			4.55	4.7	4.85	V
VCC Bypass Switch Switchover Hysteresis				0.1	0.2	0.3	V
Over-Temperature Protection							
Over-Temperature Protection Threshold	T_{OTP}			--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	RT6338AH/BH/CH/FH		--	20	--	°C

Note 7. Guaranteed by design.

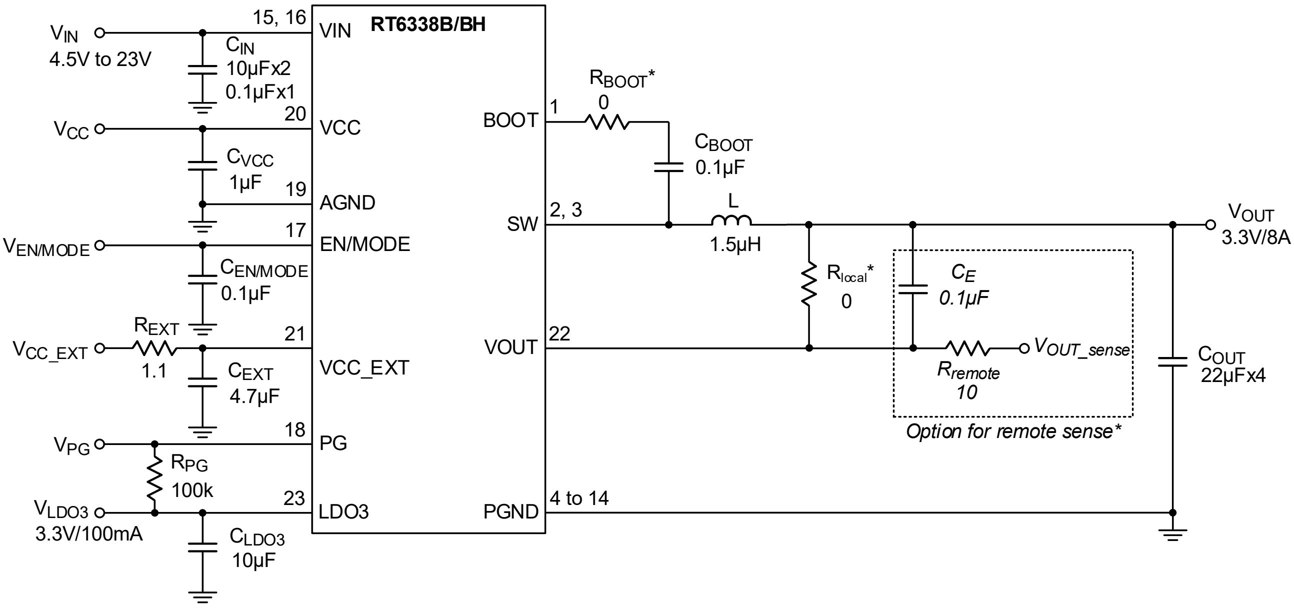
15 Typical Application Circuit



*Option for remote sense** : C_E and R_{Remote} are employed to minimize the effects of parasitic components on the VOUT power trace. If this option is used, loop stability can be further enhanced.

R_{Local}* : If the remote sense is to be used, R_{local} must be removed.

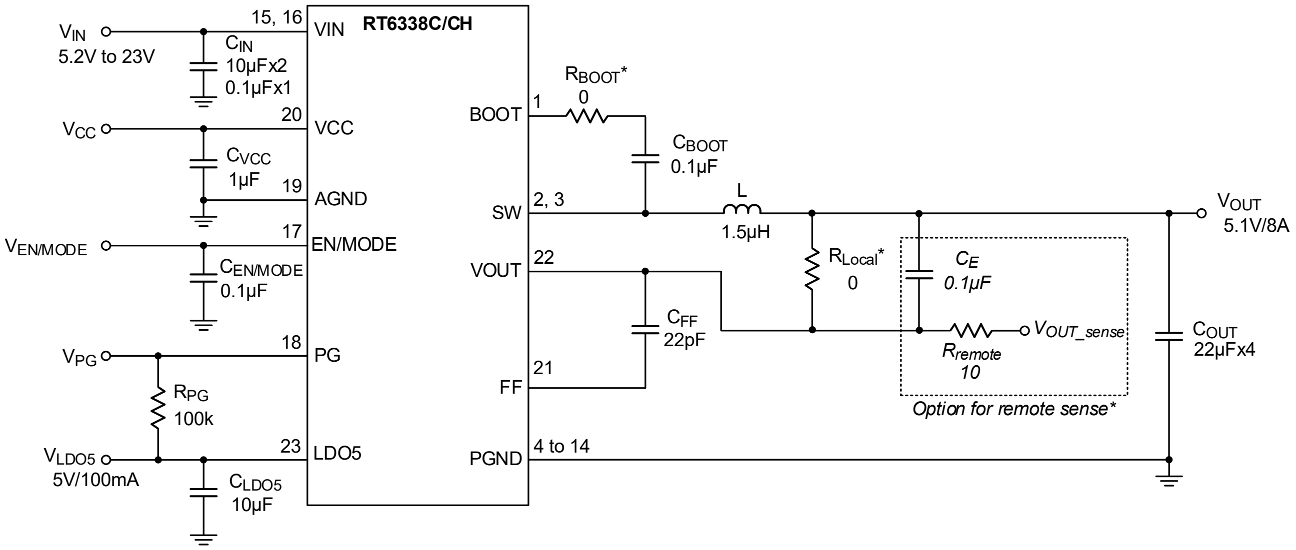
R_{BOOT}* : R_{BOOT} is reserved for option. R_{BOOT} must be less than 10Ω.



*Option for remote sense** : C_E and R_{Remote} are employed to minimize the effects of parasitic components on the VOUT power trace. If this option is used, loop stability can be further enhanced.

R_{Local}* : If the remote sense is to be used, R_{local} must be removed.

R_{BOOT}* : R_{BOOT} is reserved for option. R_{BOOT} must be less than 10Ω.



*Option for remote sense** : C_E and R_{Remote} are employed to minimize the effects of parasitic components on the VOUT power trace. If this option is used, loop stability can be further enhanced.

R_{Local}* : If the remote sense is to be used, R_{local} must be removed.

R_{BOOT}* : R_{BOOT} is reserved for option. R_{BOOT} must be less than 10Ω.

Table 1. Suggested Typical Component Selections for the Application-Part I

Part Number	V_{OUT}	R1	R2	C_{FF}	L[(2), (3)]	C_{LDO}	R_{EXT}	C_{EXT}
RT6338A/AH/F/FH	1.05V	30.9kΩ	41.2kΩ	68pF/50V/0603	0.68µH	NA	1.1Ω/0603	4.7µF/6.3V/0603
	1.8V	80.6kΩ	40.2kΩ	39pF/50V/0603				
	3.3V	182kΩ	40.2kΩ	33pF/50V/0603	1.5µH			
	5.1V	301kΩ	40.2kΩ	22pF/50V/0603				
RT6338B/BH	3.3V	NA	NA	NA		10µF/6.3V/0603		
RT6338C/CH	5.1V			22pF/50V/0603		10µF/6.3V/0603	NA	NA

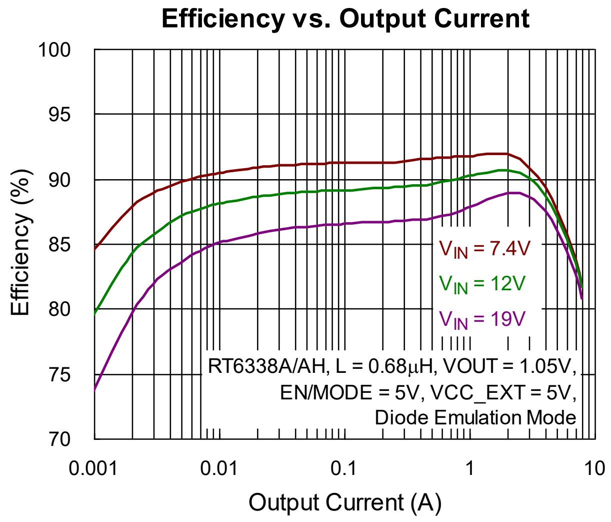
Table 2. Suggested Typical Component Selections for the Application-Part II

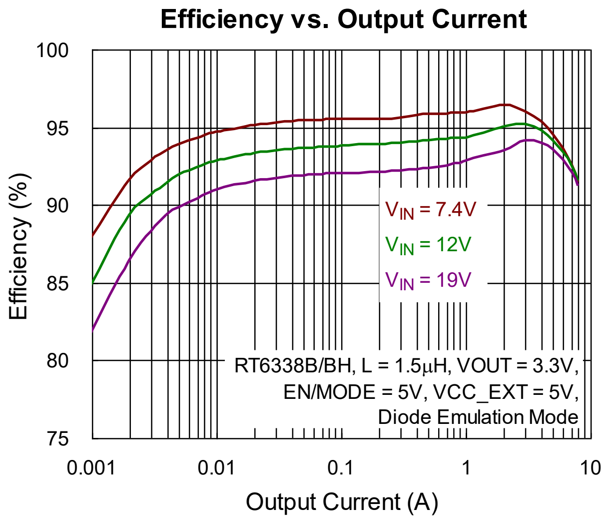
Part Number	V_{OUT}	C_{IN}	C_{OUT}	R_{BOOT}	C_{BOOT}	C_{VCC}	$C_{EN/MODE}$	C_E	R_{Remote}	R_{Local}
RT6338A/AH/F/FH	1.05V	10µF/35V/0805x2 0.1µF/50V/0603x1	22µF/6.3V /0805x6	0Ω/0603	0.1µF/50V /0603	1µF/6.3V /0603	0.1µF/50V /0603	0.1µF/50V/ 0603	10Ω/ 0603	0Ω/ 0603
	1.8V									
	3.3V									
	5.1V									
RT6338B/BH	3.3V		22µF/6.3V /0805x4							
RT6338C/CH	5.1V									

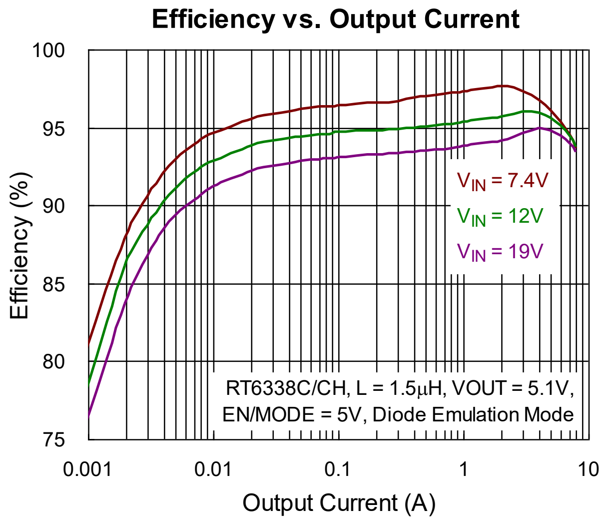
Note 8.

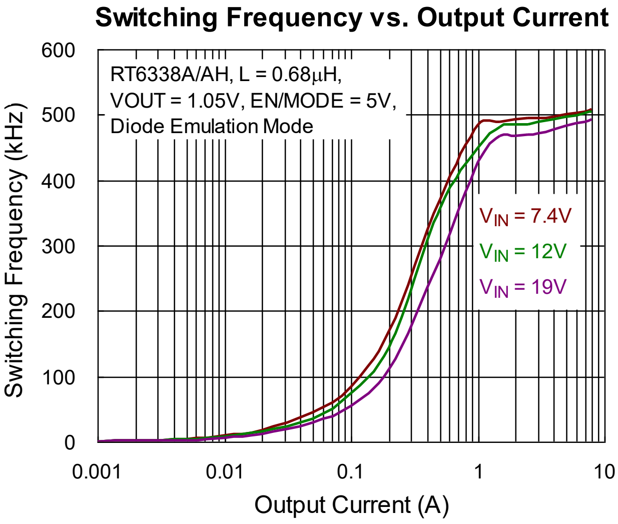
1. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.
2. PEUE063T-R68MS: Size(mm) = 7.3 x 6.8 x 3, L = 0.68µH, DCR = 4.3mΩ, I_{SAT} = 18.5A
3. PEUE063T-1R5MS: Size(mm) = 6.95 x 6.6 x 2.8, L = 1.5µH, DCR = 7.7mΩ, I_{SAT} = 14.8A

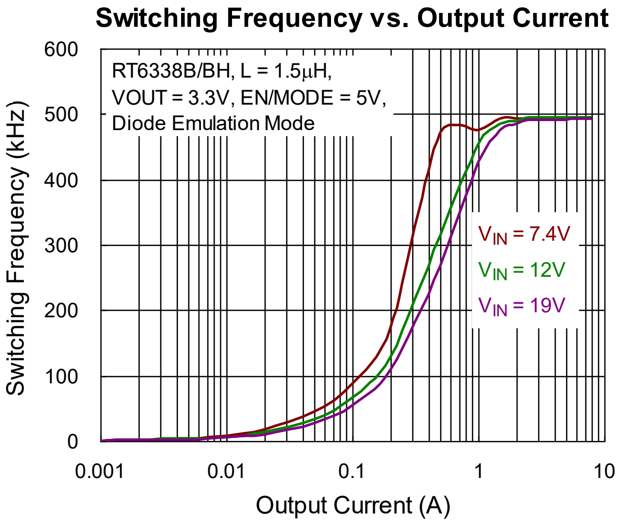
16 Typical Operating Characteristics

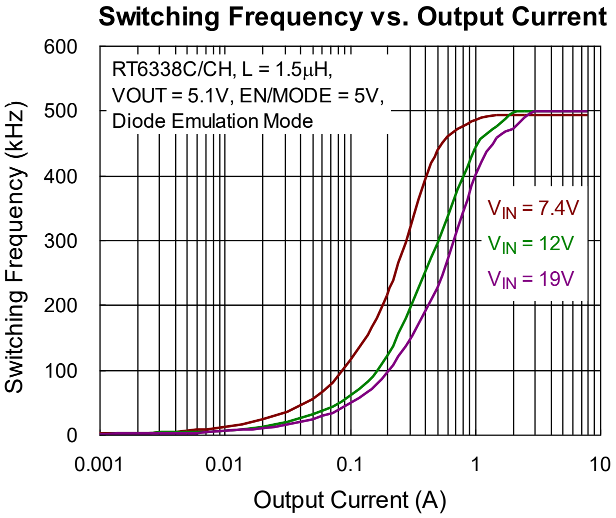




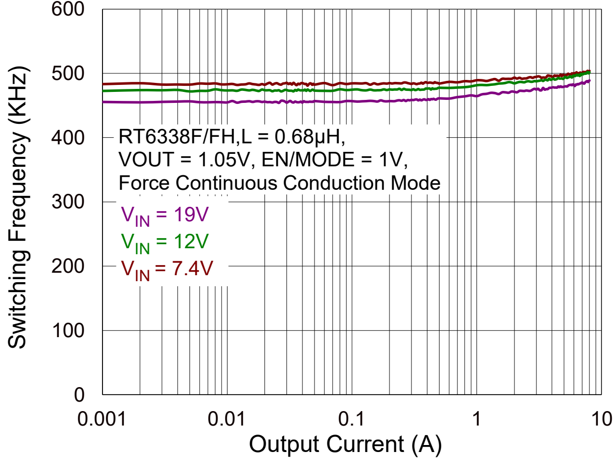




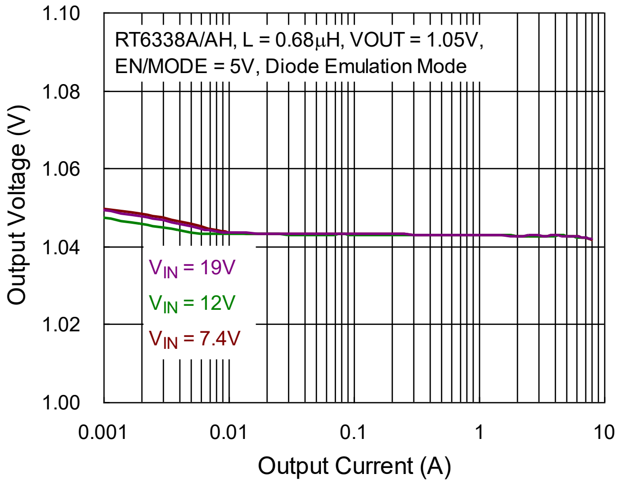




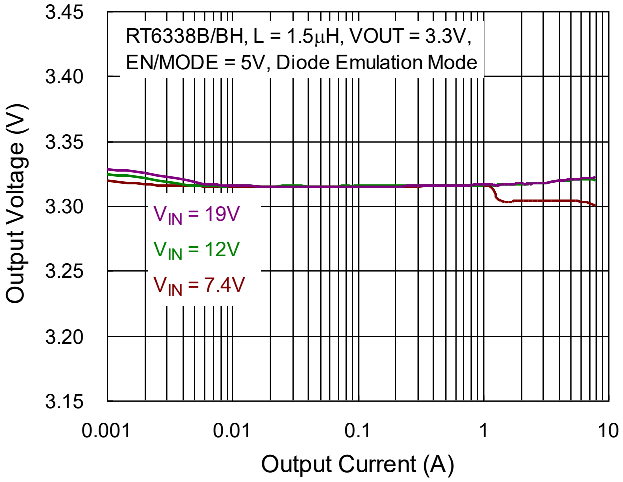
Switching Frequency vs. Output Current



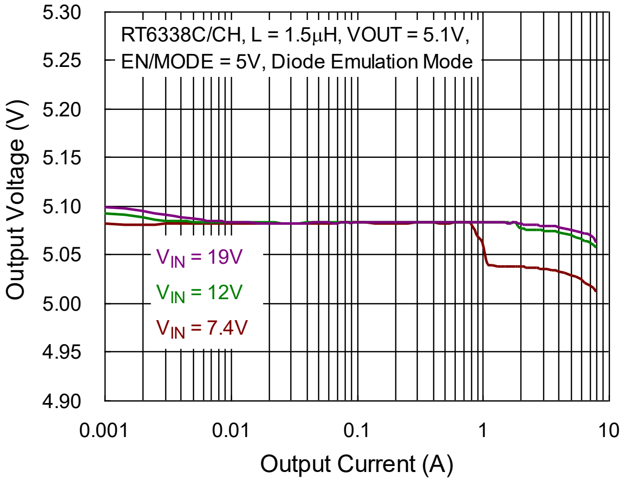
Output Voltage vs. Output Current



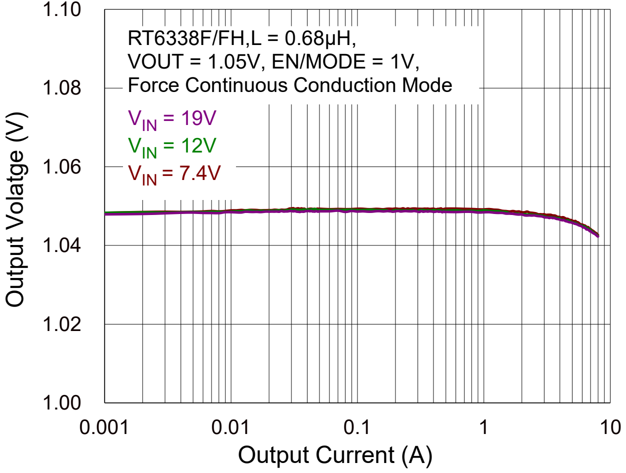
Output Voltage vs. Output Current



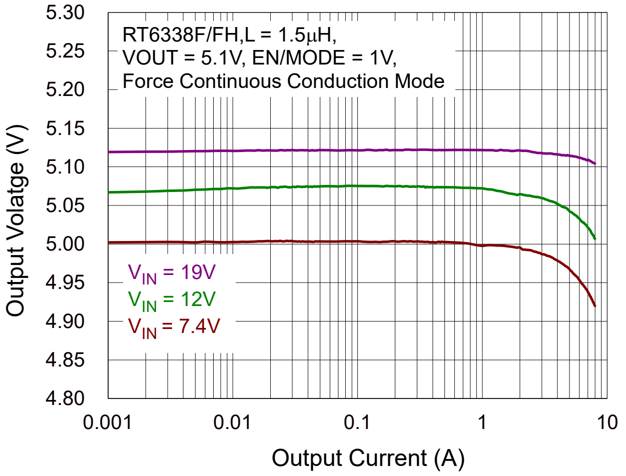
Output Voltage vs. Output Current

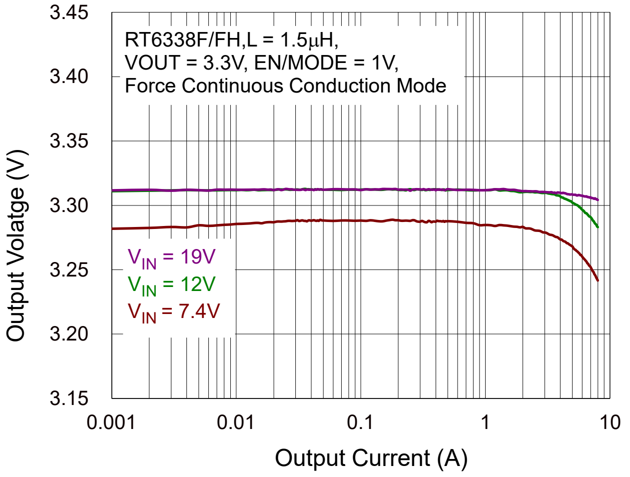


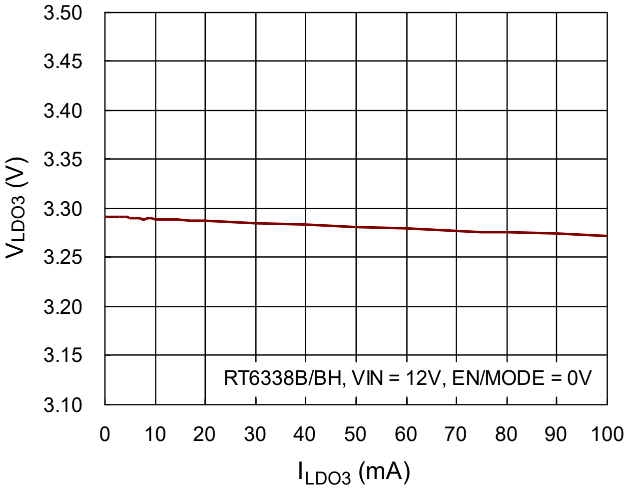
Output Voltage vs. Output Current

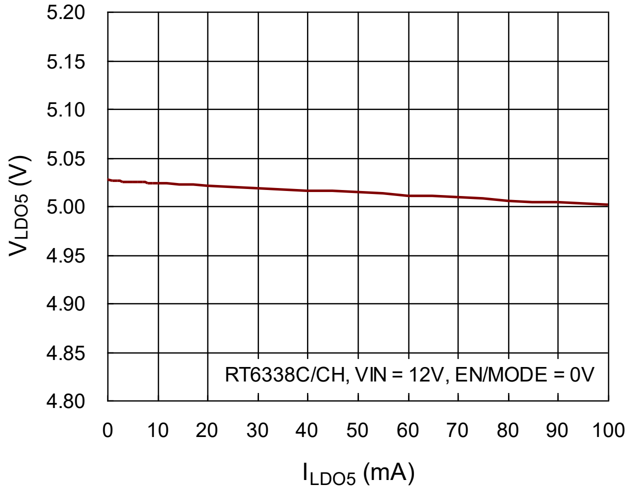


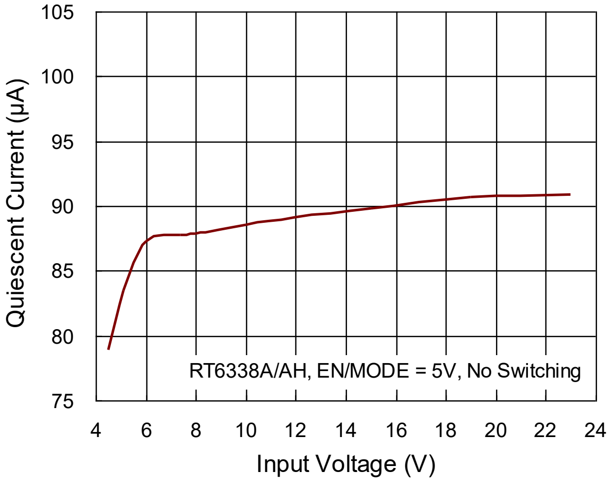
Output Voltage vs. Output Current

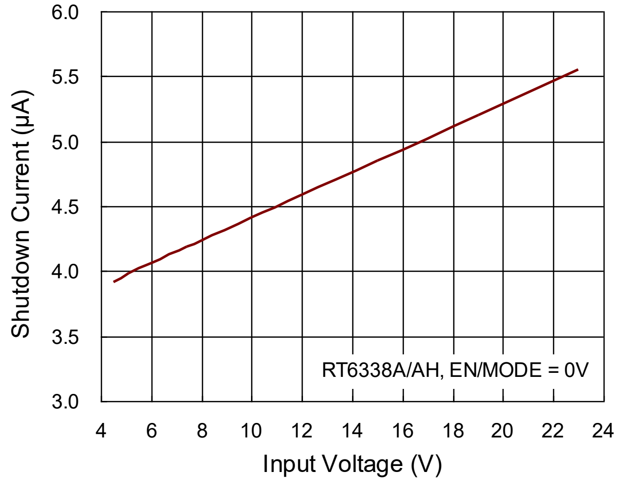


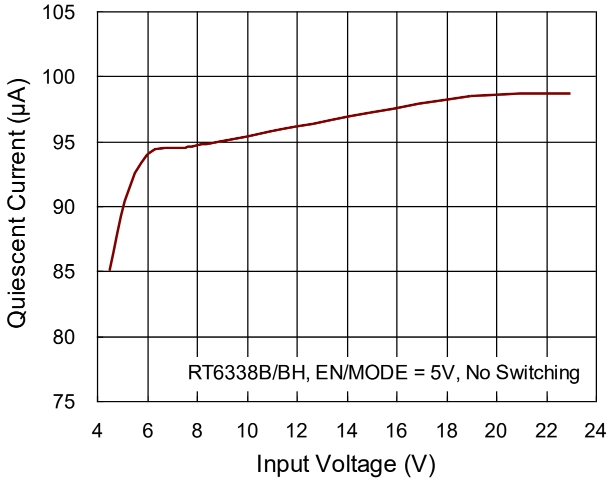

Output Voltage vs. Output Current


V_{LDO3} vs. I_{LDO3}

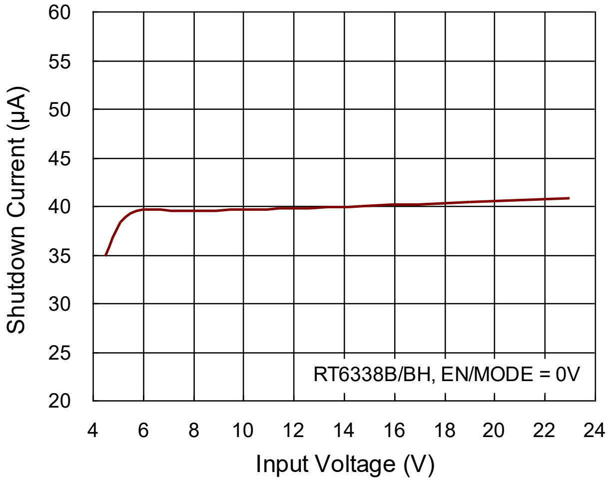

V_{LDO5} vs. I_{LDO5}


Quiescent Current vs. Input Voltage

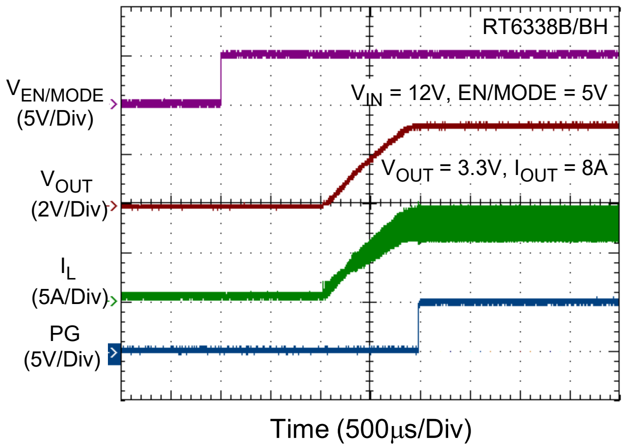

Shutdown Current vs. Input Voltage


Quiescent Current vs. Input Voltage

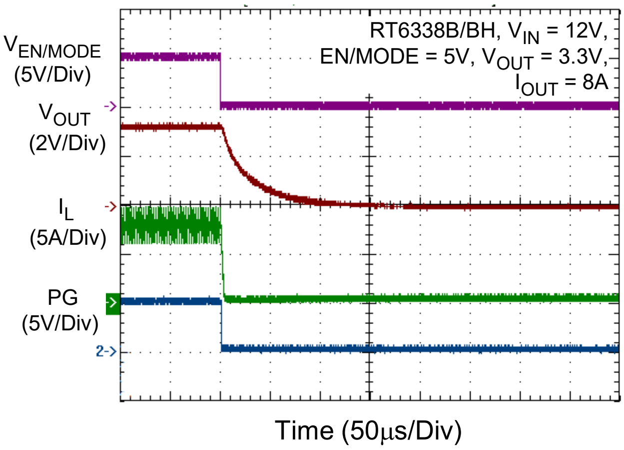
Shutdown Current vs. Input Voltage



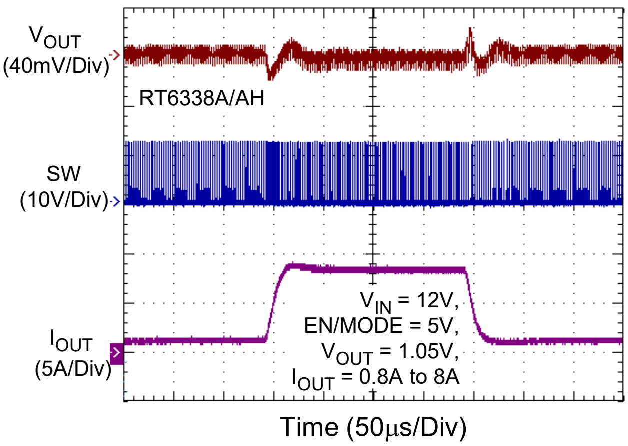
Power On from EN/MODE



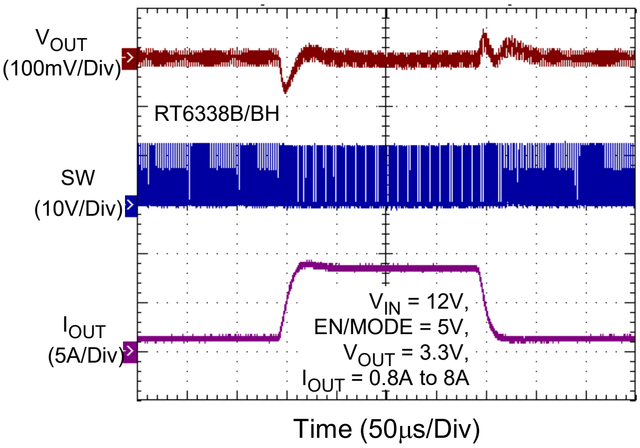
Power Off from EN/MODE



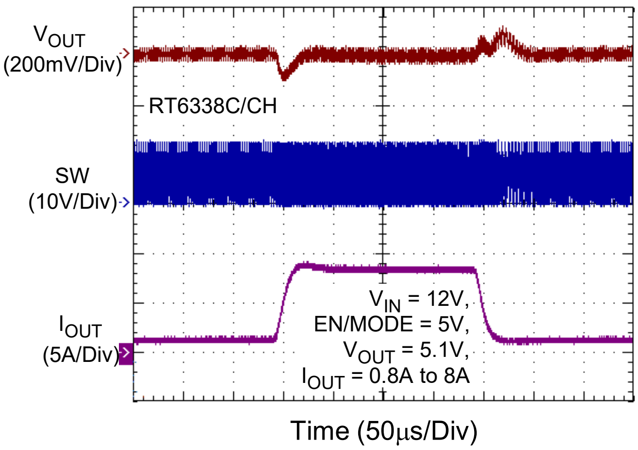
Load Transient Response



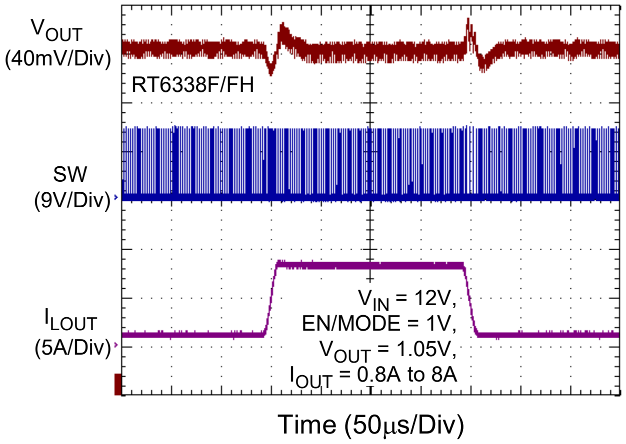
Load Transient Response



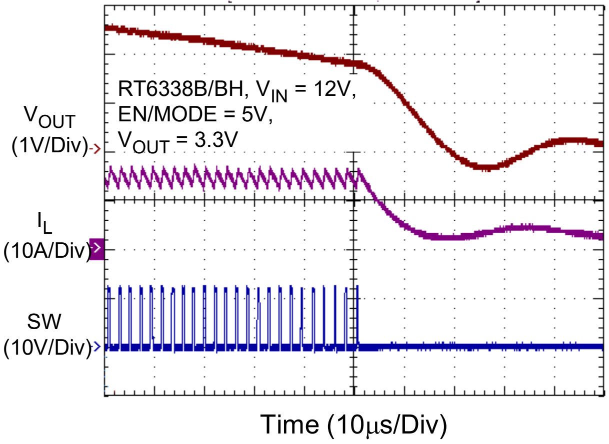
Load Transient Response



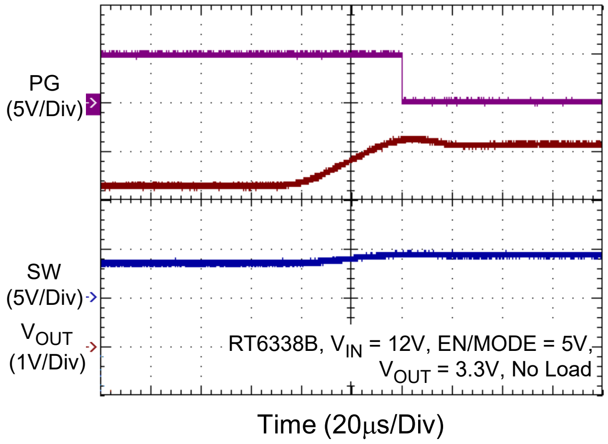
Load Transient Response



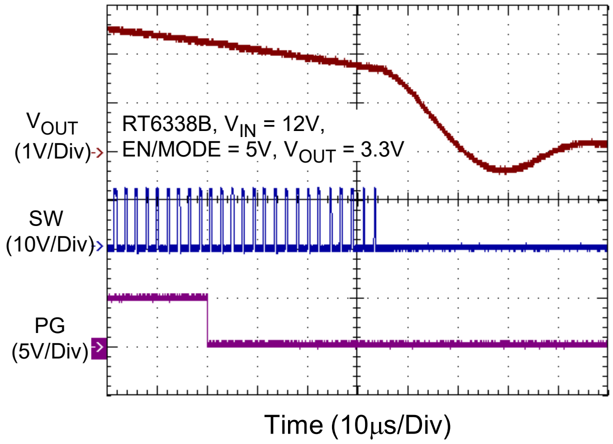
Over Current Limit



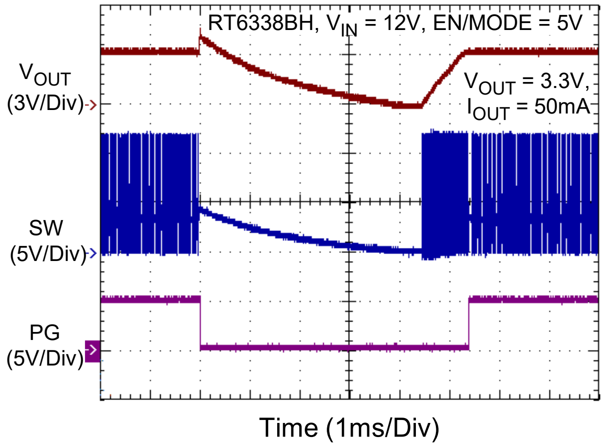
VOUT OVP with Latched Mode



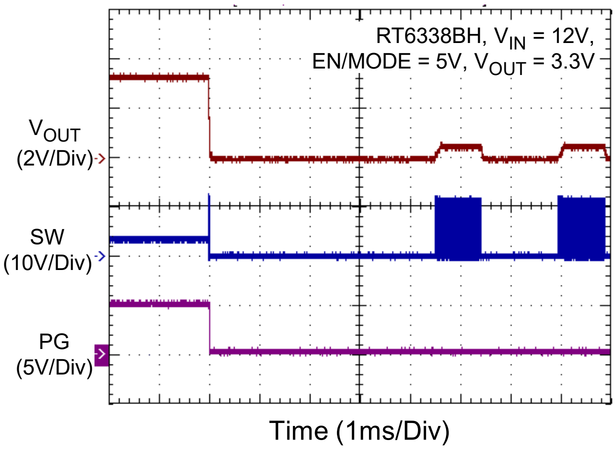
VOUT UVP with Latched Mode



VOUT OVP with Non-Latched Mode



VOUT UVP with Hiccup Mode



17 Operation

The RT6338 is a high efficiency synchronous buck converter with integrated MOSFETs. The RT6338 utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture providing vary fast transient response. The ultra-fast ACOT® control enables the use of small output capacitance and optimizes the component size without additional compensation network.

During normal operation, the high-side MOSFET turns on with a fixed one-shot on-time timer after the beginning of each clock cycle. The inductor current linearly increases when the high-side MOSFET turns on and the low-side MOSFET turns off. Similarly, the inductor current linearly decreases when the high-side MOSFET turns off and the low-side MOSFET turns on. The voltage ripple on the output has similar shape to the inductor current due to the output capacitor ESR.

The feedback voltage ripple comparing with an internal reference is caught by feedback resistor network. When a fixed minimum off-time timer is timeout and the inductor valley current is below the valley current-limit threshold, the fixed one-shot one-time timer is triggered if the feedback voltage falls below the feedback reference voltage. Therefore, the output voltage is regulated.

17.1 ACOT® Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. The internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Conventional COT control implements the on-time timer proportional to V_{OUT} and inversely proportional to V_{IN} to achieve pseudo-fixed frequency with wide VIN range. A fixed on-time timer of conventional COT control has no compensation for the voltage drop of the MOSFETs and inductor during higher load condition.

In order to compensate the voltage drop of MOSFETs and inductor without influencing the fast transient behavior of the COT topology, a frequency locked loop system with slowly adjusting on-time timer is further added to the ACOT® control.

17.2 Average Output Voltage Control Loop

In continuous conduction mode, conventional COT control has DC offset between $V_{FB\ (average)}$ and V_{REF}, as shown in Figure 1. In order to cancel the DC offset, the RT6338 provides an average output voltage control loop to adjust the comparator input V_{REF}. Hence, the $V_{FB\ (average)}$ always follows the designed value. The control loop efficiently improves the load and line regulation without affecting the transient performance.

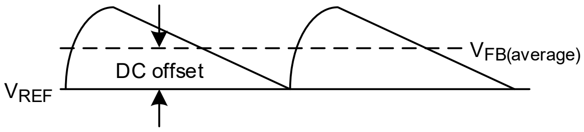


Figure 1. Conventional COT Control Loop Operation

17.3 High Voltage Conversion Ratio Function

In conventional COT control, the maximum duty cycle is limited by the minimum off-time. The RT6338B/BH/C/CH provides a feature for increasing the on-time function (up to 15μs) to extend the maximum duty cycle of 2S battery applications.

17.4 Diode Emulation Mode (DEM)

Diode emulation mode is selected by the EN/MODE voltage level. The device enters diode emulation mode when the EN/MODE voltage is greater than 2.3V. In diode emulation mode, the RT6338 automatically and smoothly reduces switching frequency at light-load conditions. As the output current decreases from heavy load to light load, the inductor current is naturally reduced. Once the valley point of inductor current touches to zero during decreasing output current, the behavior is boundary mode between continuous conduction and discontinuous conduction mode. In order to emulate the behavior of free-wheeling diode, the device only allows partial negative current to flow from drain to source of the low-side MOSFET when inductor free-wheeling current becomes negative.

During decreasing output current, the discharge time of the output capacitor is gradually longer. When the voltage on the output capacitor is lower than the reference of regulating voltage, the next one-shot on-time timer is activated. On the contrary, when the output current increases from light load to heavy load and the inductor current finally reaches to the continuous conduction, the switching frequency smoothly increases to preset value. The boundary load condition between continuous conduction and discontinuous conduction mode is shown in Figure 2 and is calculated as follows:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times t_{ON}$$

where I_{LOAD} is the output loading current and t_{ON} is the on-time

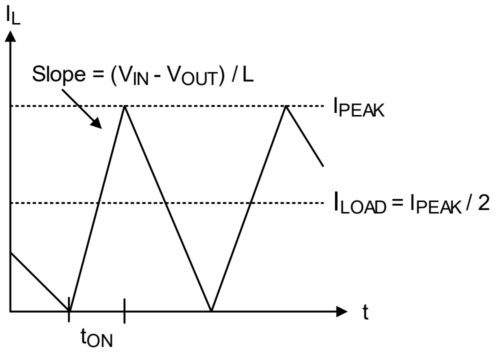


Figure 2. Boundary Condition of CCM/DEM

As mentioned above, diode emulation mode features natural high efficiency in the light-load conditions. In DEM operation (assuming that the coil resistance remains fixed), low inductor value has high efficiency and high output voltage ripple. However, high inductor value features low efficiency and less output voltage ripple. The drawback of using high inductor value includes larger physical size and lower load transient response (especially at low input voltage level).

17.5 Ultrasonic Mode (USM)

The RT6338 activates a unique type of diode emulation mode with a minimum switching frequency of 25kHz, called ultrasonic mode. The acoustic frequency is avoided in ultrasonic mode. Ultrasonic mode is selected by the EN/MODE voltage level. If the EN/MODE voltage ranges from 0.88V to 1.7V, the device operates in ultrasonic mode.

When the internal 25kHz oscillator is triggered, the one-shot on-time timer is activated for turning on the high-side MOSFET. Once the one-shot on-time timer is completed, the low-side MOSFET is turned on with off-time timer. After the one-shot on-time timer and off-time timer are finished, the device keeps both high-side and low-side MOSFET off and waits for next trigger.

In order to regulate output voltage with 25kHz minimum switching frequency, the one-shot on-time timer and off-time timer are adjusted based on load condition. In no-load condition, the shorter one-shot on-time timer and longer off-time timer are applied as initial value. In this manner, the inductor current decreases to negative value during the off-time state. When the output current slowly increases from no load, the valley point of inductor current is increased by reducing the width of off-time timer until the inductor valley point reaches from negative value to zero. In previous load condition, if the output current is further increased, the width of on-time timer is gradually increased from shorter value to normal value before the switching frequency is higher than 25kHz. Once the switching frequency is higher than 25kHz with increasing output current, the behavior of device is changed from ultrasonic mode to diode emulation mode.

For better load transient performance in USM mode, it is recommended to ensure that the minimum load current is greater than 100mA during load transient testing.

17.6 Force Continuous Conduction Mode

The RT6338F/FH is designed to operate in forced PWM mode (FCCM mode) for applications requiring the exclusion of switching harmonics from the signal band. While FCCM mode compromises light load efficiency, it provides benefits for low output voltage ripple, precise output voltage regulation, swift transient response, and a stable switching frequency.

17.7 On-Time Reduction Function for DEM

In normal diode emulation mode, the output voltage ripple of converter is proportional to on-time and inversely proportional to load current. In order to have smaller voltage ripple in light-load applications, the RT6338 provides a smart reduction on-time function. The smart reduction on-time function naturally decreases on-time when load current is decreasing. Therefore, the output voltage ripple is reduced.

17.8 Spread Spectrum Function for DEM

In order to reduce the acoustic noise in diode emulation mode, the RT6338 provides spread spectrum function with randomly adjusted on-time. The random variation value is ±7% of normal on-time value. Once the load condition enters to CCM, the device disables the spread spectrum function because the switching frequency is much higher than acoustic frequency.

17.9 EN/MODE Sink Current

The RT6338 does not allow an uncertain voltage on the EN/MODE pin, which may cause the logic errors or abnormal device behavior . In order to prevent the EN/MODE pin from floating, the RT6338 builds the EN/MODE input current for eliminating floating voltage on the EN/MODE pin. The characteristic of EN/MODE input current vs EN/MODE input voltage is shown in Figure 3.

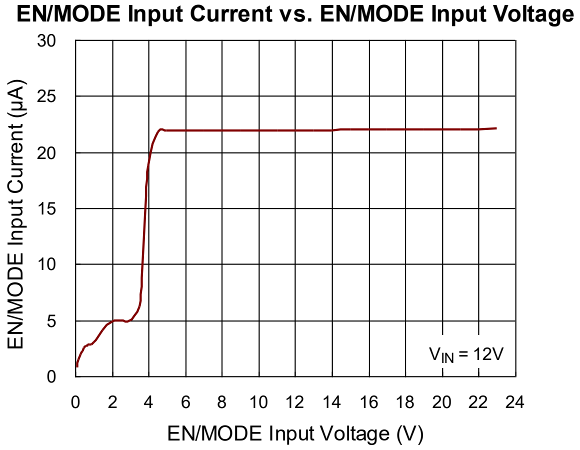


Figure 3. Characteristics of EN/MODE Input Current

17.10 Soft-Start

The RT6338 provides an internal soft-start to prevent large input inrush current and output voltage overshoot. If the EN/MODE voltage and input voltage exceed their rising thresholds, the soft-start function is activated. The V_{FB} starts to track the internal reference voltage ranging from zero to the target.

17.11 Valley Current-Limit Setting

The RT6338A/AH/F/FH provides valley current-limit setting pin to adjust current-limit level. When both "VIN rises to its UVLO rising threshold" and "EN/MODE is activated" are satisfied and kept for 600μs, the RT6338 determines and locks the current-limit level according to the voltage on the ILMT pin. In addition to the previously described timing behavior, any change of the valley current-limit status is invalid. The valley current-limit setting level is selected as follows:

RT6338A/AH:

- 10A: Connect ILMT pin to PGND.
- 12A: Leave ILMT pin floating/open.
- 14A: Connect ILMT pin to 5V.

RT6338F/FH:

- 5A: Connect ILMT pin to PGND.
- 7A: Leave ILMT pin floating/open.
- 9A: Connect ILMT pin to 5V.

17.12 Valley Current Limit

The RT6338 features a cycle-by-cycle valley current limit for avoiding the large output current and overheat. The device cycle-by-cycle compares the valley current of the inductor with the valley current-limit threshold. The output current is limited to the sum of the valley current and a half of the ripple current when the inductor valley current reaches the valley current-limit threshold.

After the device completes the minimum off-time and keeps ON state of the low-side MOSFET, the inductor valley current level is monitored by measuring the low-side MOSFET voltage between the SW pin and the PGND pin during the ON state of the low-side MOSFET. During the ON state of the low-side MOSFET, the measured low-side MOSFET voltage is proportional to the low-side MOSFET current. In order to improve the accuracy of the measured current, the temperature compensation circuit is built internally.

In order to prevent the device from overcurrent, if the measured low-side MOSFET current is higher than the valley current-limit threshold, the device remains ON state of the low-side MOSFET and the one-shot on-time timer is inhibited until its current linearly decreases lower than the valley current-limit threshold. Once the low-side MOSFET current is below valley current-limit threshold, the next one-shot on-time timer is permitted to generate. The circuit of the cycle-by-cycle valley current limit works in every switching cycle.

17.13 Peak Current Limit

The RT6338 with a cycle-by-cycle peak current limit prevents the device from inductor saturation or any possibility of damage caused by too much output inrush current. The device cycle-by-cycle compares the peak current of the inductor with the peak current-limit threshold.

After the device finishes the minimum on-time timer and remains ON state of high-side MOSFET, the inductor peak current level is monitored by sensing the high-side MOSFET voltage between the VIN pin and the SW pin during the ON state of the high-side MOSFET. During the ON state of the high-side MOSFET, the measured high-side MOSFET voltage is proportional to the high-side MOSFET current.

In order to prevent the device from inductor saturation or any risk of damage, if the measured high-side MOSFET current is higher than the peak current-limit threshold, the on-time timer is terminated immediately to limit the inductor current and the inductor current is decreased by turning on the low-side MOSFET. Once the low-side MOSFET current is below the valley current-limit threshold, the next one-shot on-time timer is permitted to generate. The circuit of the cycle-by-cycle peak current limit works in every switching cycle.

17.14 Output Undervoltage Protection (UVP)

The output undervoltage protection of the RT6338 includes latched mode and hiccup mode. If the inductor current is higher than the current-limit threshold (valley/peak current-limit threshold) during heavy-load condition, the output voltage tends to drop because the load demand exceeds that the converter can support.

When the load demand is larger than the current ability of the converter, the V_{FB} (RT6338A/AH/F/FH)/V_{OUT} (RT6338B/BH)/V_{FF} (RT6338C/CH) starts to drop. Once the V_{FB}/V_{OUT}/V_{FF} drops below 60% (typical) of the reference/target voltage and the time length of this state is larger than the time width 11μs (typical), the latched/hiccup mode UVP is triggered. The different behaviors for latched/hiccup mode UVP are as follows:

- The RT6338A/B/C/F provides output undervoltage protection (UVP) with latched mode. Once UVP is triggered, the IC stops PWM switching and enters latched mode. If the UVP event is released, users should re-toggle the EN/MODE pin or power recycle the VIN supply to re-power on the device.
- The RT6338AH/BH/CH/FH provides output undervoltage protection (UVP) with hiccup mode. Once UVP is triggered, the IC takes a determined period for initiating an auto-recovery soft-start sequence. If the UVP event is released, the output voltage is regulated to the target reference.

17.15 Output Overvoltage Protection (OVP)

The output overvoltage protection of the RT6338 includes latched mode and non-latched mode. If the V_{FB}/V_{OUT}/V_{FF} rises above typical 120% of the reference/target voltage and the time length of this state is larger than the time width 11μs (typical), the latched/non-latched mode OVP is triggered. The different behaviors of latched/non-latched mode OVP are as follows:

- The RT6338A/B/C/F provides output overvoltage protection (OVP) with latched mode. Once OVP is triggered, the IC stops PWM switching and enters latched mode. If the OVP event is released, users should re-toggle the

EN/MODE pin or power recycle VIN supply to re-power on the device.

- The RT6338AH/BH/CH/FH provides output overvoltage protection (OVP) with non-latched mode. Once OVP is triggered, the IC stops PWM switching and enters non-latched mode. If the OVP condition is released and the output voltage is lower than the regulation level, the device returns to regulate output voltage.

17.16 Over-Temperature Protection (OTP)

The over-temperature protection of the RT6338 includes latched mode and non-latched mode. The OTP circuitry prevents the device from overheating due to excessive power dissipation. If the junction temperature of the device exceeds typical 150°C, the latched/non-latched mode OTP is triggered to stop the temperature rising. The different behaviors of latched/non-latched mode OTP are as follows:

- The RT6338A/B/C/F provides over-temperature protection (OTP) with latched mode. Once OTP is triggered, the IC stops PWM switching and enters latched mode. If the OTP event is released, users should re-toggle the EN/MODE pin or power recycle VIN supply to re-power on the device.
- The RT6338AH/BH/CH/FH provides over-temperature protection (OTP) with non-latched mode. Once OTP is triggered, the IC stops PWM switching and enters non-latched mode. If the junction temperature of device drops below typical 130°C, the device enables the soft-start function to build the output voltage.

17.17 Input Undervoltage-Lockout (UVLO)

The RT6338 provides an Undervoltage Lockout (UVLO) function that monitors the input voltage. In order to protect the device from operating at insufficient input voltage, the UVLO function inhibits switching when the input voltage drops below the UVLO falling threshold. The IC resumes switching when the input voltage exceeds the UVLO rising threshold.

17.18 Enable Control and Mode Selection

The EN/MODE pin integrates both enable control and mode selection. If the EN/MODE voltage is less than 0.23V, the RT6338 is turned off (shutdown). If the EN/MODE voltage ranges from 0.88V to 1.7V, the RT6338 is turned on and the operation mode is USM or FCCM. Similarly, if the EN/MODE voltage is larger than 2.3V, the RT6338 is turned on and the operation mode is DEM. For the EN/MODE control logic and operation mode selection, refer to Table 3, Table 4, and Table 5.

Table 3. RT6338A/AH/B/BH/C/CH Operation Mode Selection

EN/MODE Voltage	Operation Mode
< 0.23V	Shutdown
0.88V to 1.7V	USM
≥ 2.3V	DEM

Table 4. RT6338F/FH Operation Mode Selection

EN/MODE Voltage	Operation Mode
< 0.23V	Shutdown
0.88V to 1.7V	FCCM
≥ 2.3V	DEM

Table 5. RT6338 Power Logic

Note: 0 = Logic low, 1 = Logic high, X = Don't care, ON = Active, OFF = Inactive, N/A = Not applicable

Part Number	Input*		Output			
	EN/MODE*	**VCC_EXT***	**VCC Bypass Switch**	**VCC**	**LDO**	**VOUT**
RT6338A/AH/F/FH	0	X	OFF	OFF	N/A	OFF
	1	0	OFF	ON	N/A	ON
	1	1	ON	ON	N/A	ON
RT6338B/BH	0	X	OFF	ON	ON	OFF
	1	0	OFF	ON	ON	ON
	1	1	ON	ON	ON	ON
RT6338C/CH	0	N/A	N/A	ON	ON	OFF
	1	N/A	N/A	ON	ON	ON

Input*: VIN is ready in the whole power logic table.
EN/MODE*: Logic = 1 means $V_{EN/MODE} > 0.88V$. Logic = 0 means $V_{EN/MODE} < 0.23V$
VCC_EXT*: Logic = 1 means VCC_EXT > 4.85V. Logic = 0 means VCC_EXT < 4.25V.

17.19 Internal Output Voltage Discharge

The RT6338 has an output voltage discharge function by using an internal MOSFET 50Ω (typical), which is connected from the SW pin to the PGND pin. The output voltage discharge function is enabled if any of the following events is triggered:

- Input undervoltage-lockout (UVLO)
- Output undervoltage or overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- The EN/MODE pin is pulled low

17.20 Internal Vcc Regulator (VCC)

The internal V_{CC} regulator is a linear regulator. The V_{CC} regulator steps down the input voltage to typical 5V to supply both the internal circuitry and gate drivers. DO NOT connect to any external loads. Connect a capacitor (C = 1μF/0603) from the VCC pin to the AGND pin. The RT6338A/AH/F/FH enables V_{CC} regulator after V_{IN} rises higher than the UVLO rising threshold and the EN/MODE voltage is larger than the EN/MODE input high voltage. The RT6338B/BH or RT6338C/CH enables V_{CC} regulator after V_{IN} rises higher than the UVLO rising threshold. The power logic of V_{CC} is shown in Table 4.

For lower power consumption, VCC switches over to the following pins as the specified condition (refer to Figure 4 and Figure 5) are satisfied:

- RT6338A/AH/F/FH: VCC_EXT pin
- RT6338B/BH: VCC_EXT pin
- RT6338C/CH: VOUT pin

17.21 Low Dropout Regulator (LDO)

Both RT6338B/BH and RT6338C/CH have 3.3V LDO and 5V LDO, respectively. The output current capability of these two LDOs are 100mA. The output current limit of these two LDOs are 200mA. Once the input voltage exceeds the UVLO rising threshold, the LDO is enabled.

In order to reduce power consumption, the LDO output is switched to the VOUT pin through the LDO bypass switch when all of the following events are satisfied:

- Soft-start is completed
- The VOUT pin voltage is higher than the LDO bypass switch turn-on voltage
  - The LDO bypass switch turn-on voltage of the RT6338B/BH is 3.1V
  - The LDO bypass switch turn-on voltage of the RT6338C/CH is 4.7V

The LDO bypass switch is turned off when any of the following specified events is triggered:

- Input undervoltage-lockout (UVLO)
- Output undervoltage or overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- The EN/MODE pin is pulled low
- Soft-start is not completed
- The VOUT pin voltage is lower than the LDO bypass switch turn-off voltage (LDO bypass switch turn-on voltage minus LDO bypass switch hysteresis voltage)
  - The LDO bypass switch turn-off voltage of the RT6338B/BH is 2.9V
  - The LDO bypass switch turn-off voltage of the RT6338C/CH is 4.5V

17.22 External Voltage Input for V_{CC} (VCC_EXT)

The RT6338A/AH/B/BH/F/FH features the VCC_EXT pin. In order to reduce the power consumption, the internal V_{CC} regulator is switched over to the VCC_EXT through the VCC bypass switch if the VCC_EXT pin is connected to an external voltage larger than 4.7V (typical). Once the voltage of the VCC_EXT pin is lower than 4.5V (typical), the VCC bypass switch is disconnected. The power logic of VCC_EXT is shown in Table 4.

17.23 Power Good (PG)

The PG pin is an open-drain output. An external pull-up resistor to VCC or other external rail is required, and the recommended pull-up resistor ranges from 10k to 100k. Do not pull the PG voltage higher than 6V. In order to prevent unwanted PG glitches during load transient or dynamic V_{OUT} change, the RT6338 provides PG low deglitch time with typical 11μs.

The PG pin is pulled low when any of the following specified events is triggered:

- Input undervoltage-lockout (UVLO)
- Output undervoltage or overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- The EN/MODE pin is pulled low
- Soft-start is not completed
- The FB/FF/VOUT pin voltage is lower than the PG falling threshold (PG rising threshold minus PG hysteresis voltage) of the target voltage

17.24 Power Sequence

The power sequence of the RT6338 includes the VIN pin power on/off and the EN/MODE pin power on/off. The detailed sequence information is shown in Figure 4 to Figure 12.

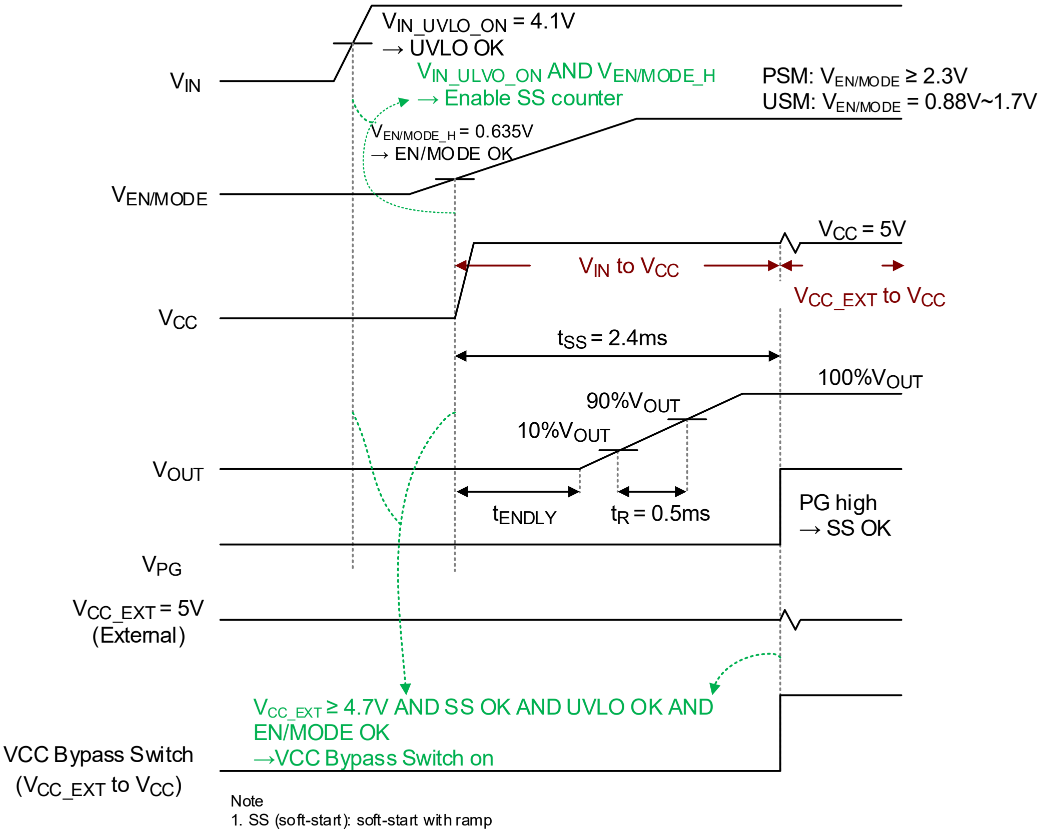
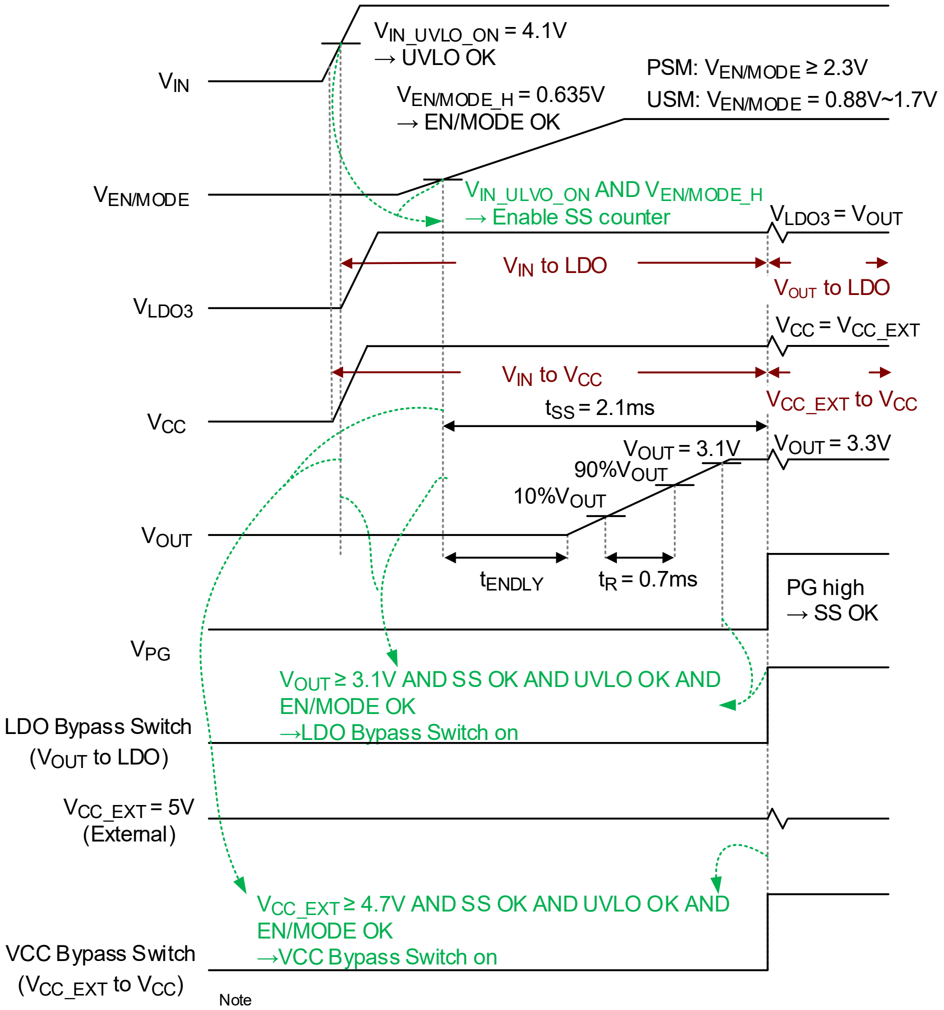
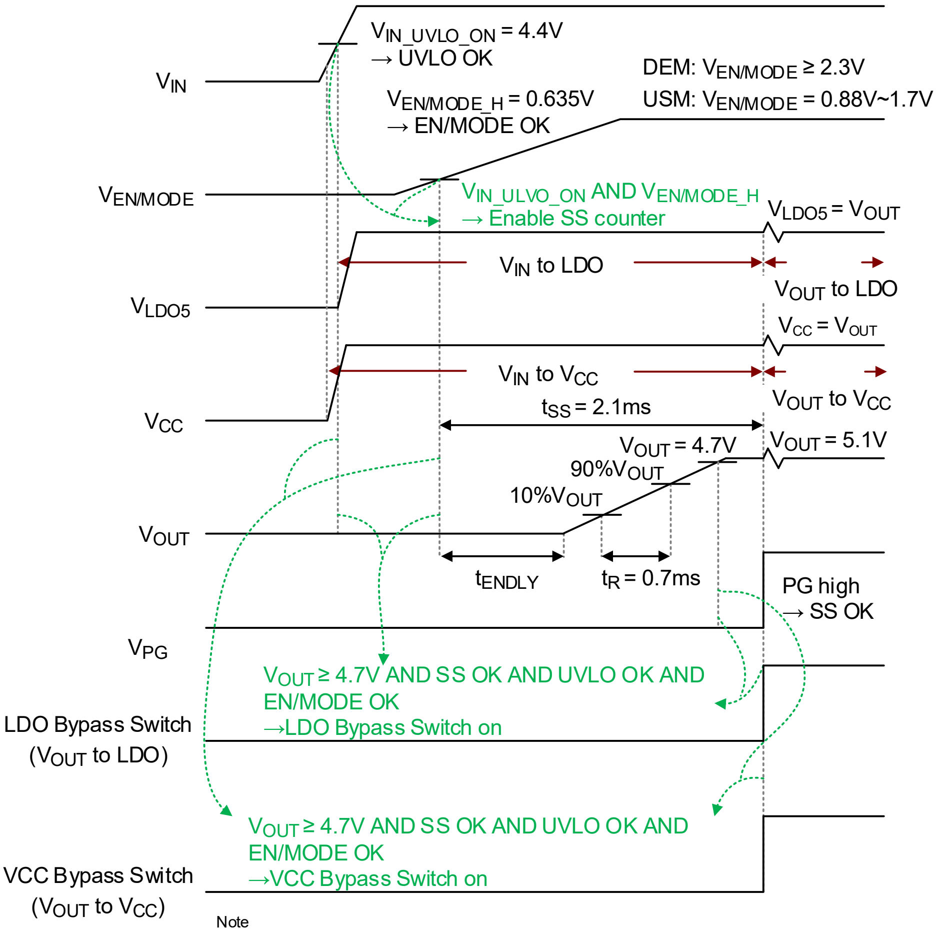


Figure 4. The RT6338A/AH/F/FH VIN and EN/MODE Pin Power On



Note
1. SS (soft-start): soft-start with ramp

Figure 5. The RT6338B/BH VIN and EN/MODE Pin Power On



Note
1. SS (soft-start): soft-start with ramp

Figure 6. The RT6338C/CH VIN and EN/MODE Pin Power On

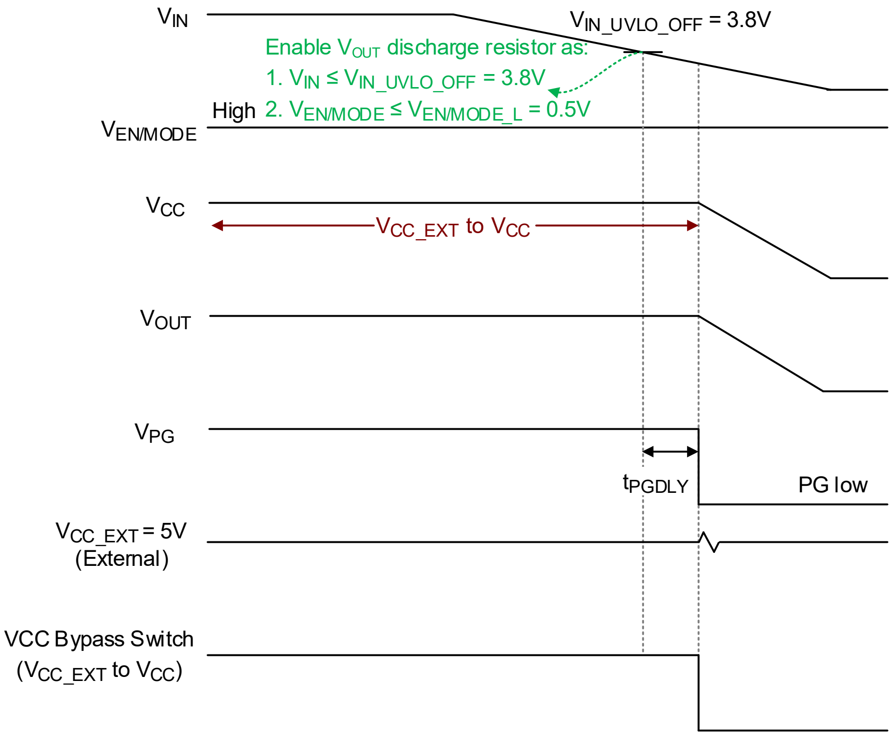


Figure 7. The RT6338A/AH/F/FH VIN Pin Power Off

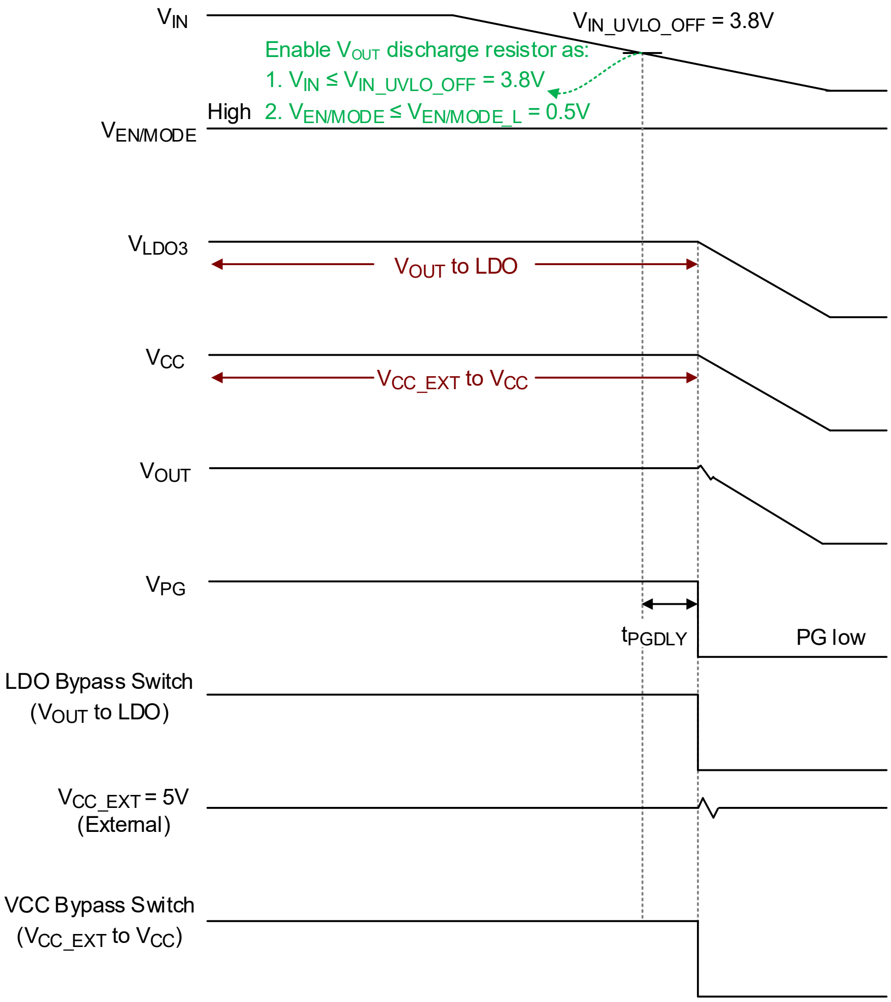


Figure 8. The RT6338B/BH VIN Pin Power Off

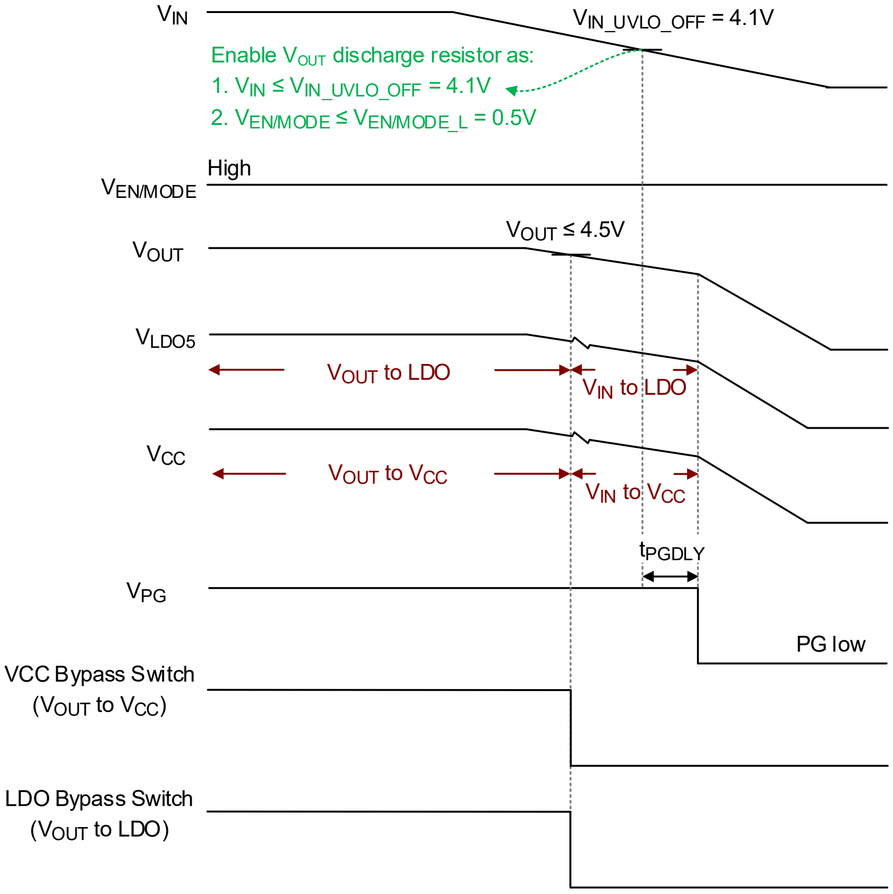


Figure 9. The RT6338C/CH VIN Pin Power Off

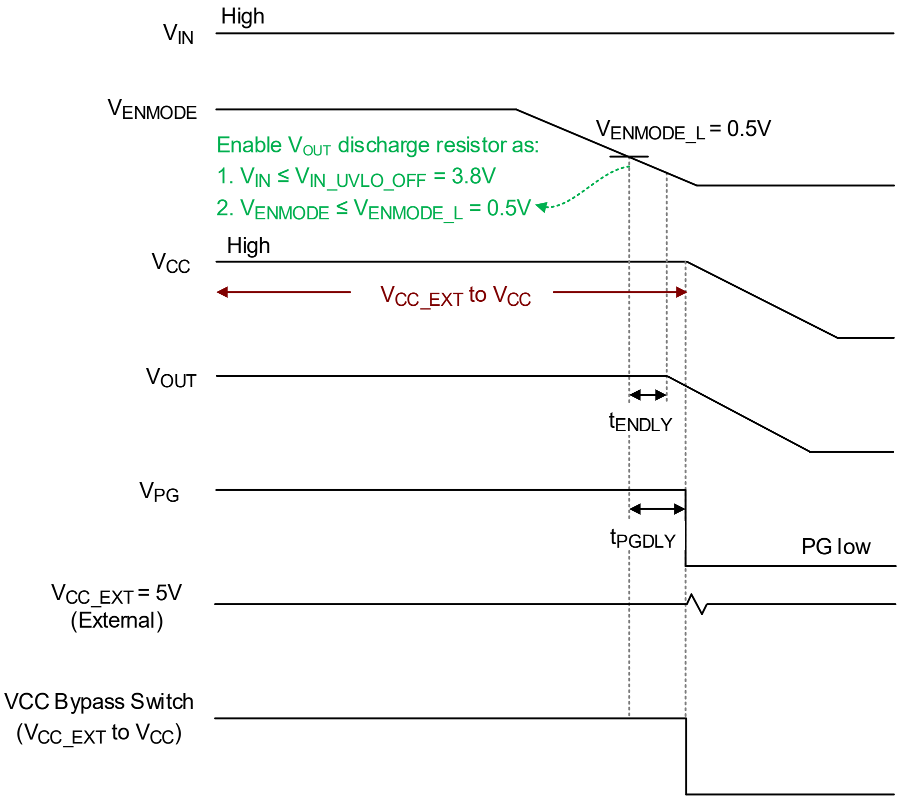


Figure 10. The RT6338A/AH/F/FH EN/MODE Pin Power Off

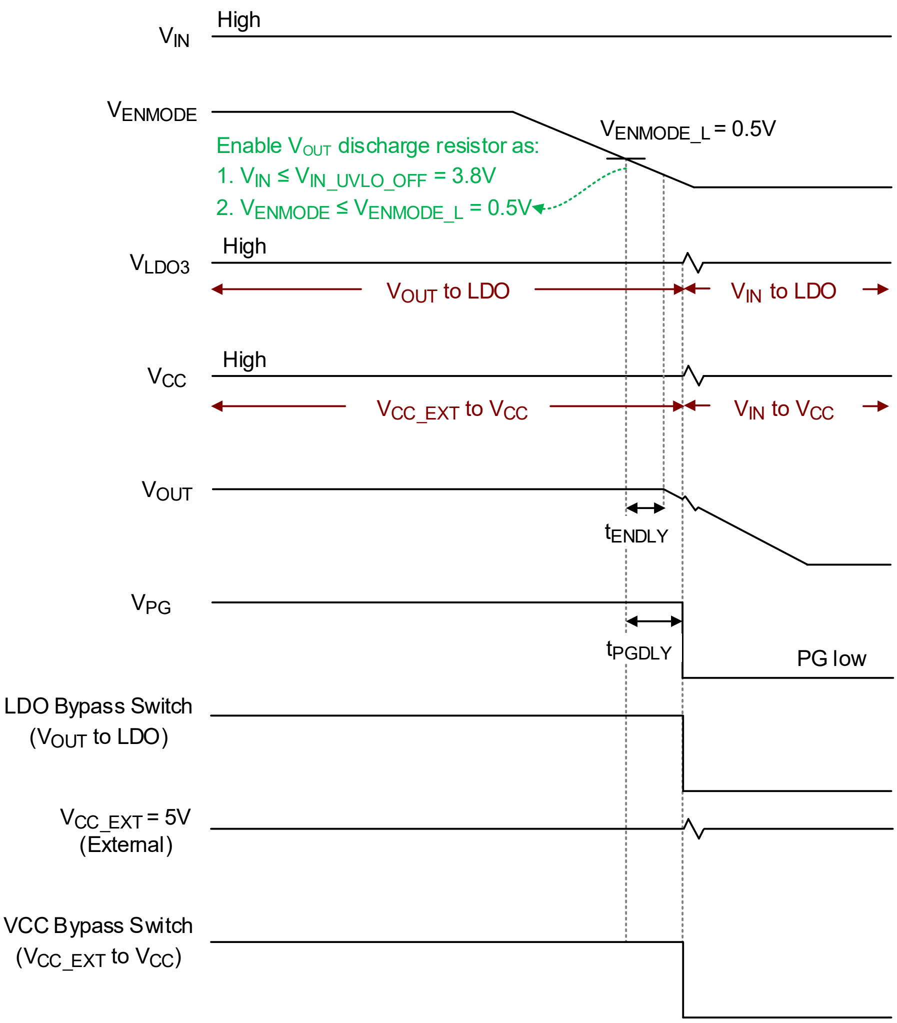


Figure 11. The RT6338B/BH EN/MODE Pin Power Off

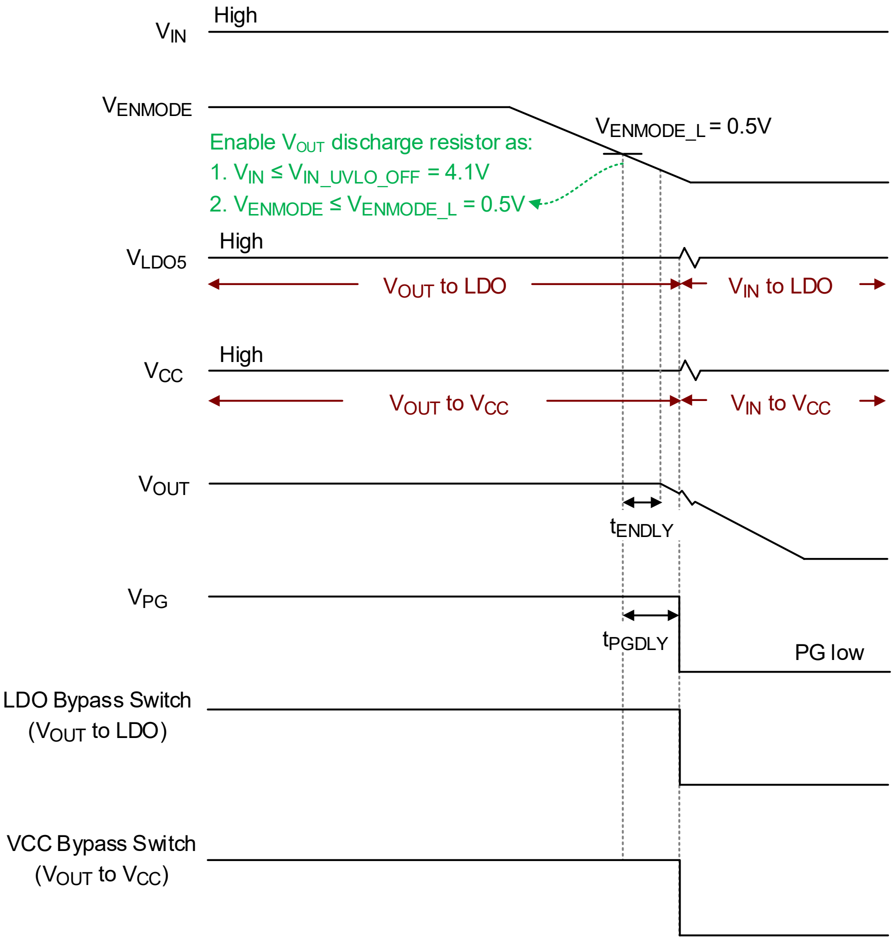


Figure 12. The RT6338C/CH EN/MODE Pin Power Off

18 Application Information

(Note 9)

A general RT6338 application circuit is shown in the Typical Application Circuit section. The external component selection is primarily driven by the load requirements. In this section, key external components such as the inductor L, the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} are introduced.

18.1 Output Voltage Adjust

The RT6338C/CH is internally built with feedback resistors for setting the V_{OUT} voltage to 5.1V. The FF pin is located between feedback R1 resistor (165kΩ) and feedback R2 resistor (40.2kΩ). In application, to slightly decrease the output voltage, an additional resistor (R3) can be added between the VOUT pin and the FF pin. To slightly increase the output voltage, the additional resistor (R4) can be added between the FF pin and GND. Refer to the following equation and Figure 13.

$$V_{OUT\_Valley} = \left(1 + \frac{R1//R3}{R2//R4}\right) \times V_{REF},$$

where R1 = 165kΩ, R2 = 40.2kΩ, V_{REFF} = 1V

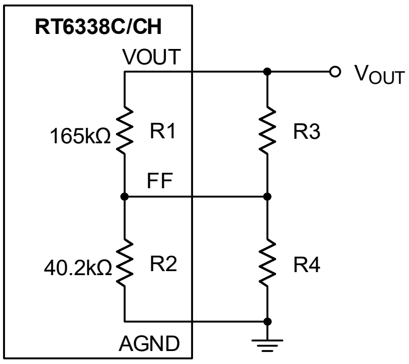


Figure 13. RT6338C/CH Slightly Adjusts V_{OUT} with the FF Pin

18.2 Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the larger ripple current increases the AC losses in the inductor. To enhance efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load current of boundary between DEM and CCM.

In the applications, the RT6338 may encounter the events of power-on inrush current (capacitive load or heavy load) and output overloading. The RT6338 provides the peak and valley current-limit protection to prevent the device from damages. Moreover, to make the current-limit protection effective, a saturation current rating of the inductor must be greater than the valley current limit of the RT6338.

18.3 Input Capacitor Selection

Input capacitance (C_{IN}) is needed to filter the pulsating current at the drain of the high-side MOSFET. The large ripple voltage on the VIN pin must be minimized by C_{IN}. The peak-to-peak voltage ripple on the input capacitor is estimated as below:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times R_{ESR}$$

Where R_{ESR} is the equivalent series resistance of C_{IN} and

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple caused by ESR can be ignored, and the minimum input capacitance is estimated as below:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D \times (1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where ΔV_{IN_MAX} = 200mV for typical application ($V_{IN} > 7V$)

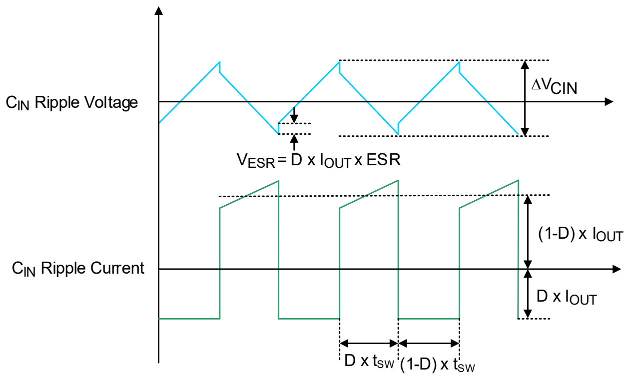


Figure 14. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have very low ESR and must be rated to handle the worst-case RMS input current:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worst $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. Therefore, the de-rating of capacitor is worse in actual application. Selecting capacitors with a higher temperature rating is required for less de-rating.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality factor (underdamped) tank circuit. If the RT6338 circuit is plugged into a live supply, the input voltage can ring up to twice of its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitors of 0.1μF should be placed close to the VIN pin. The capacitor should be 0402 or 0603 in size.

18.4 Output Capacitor Selection

The selection of C_{OUT} should satisfy the voltage ripple and transient loads, and ensure control loop stability. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, expressed as below:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}.

The output ripple is highest at the maximum input voltage, since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding the transient loads, the V_{SAG} and V_{SOAR} requirements should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which is calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage is determined by:

$$\Delta V_{OUT\_SAG} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times \left(V_{IN} \times D_{MAX} - V_{OUT}\right)}$$

When the load is removed, the amount of overshoot due to stored inductor energy is calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

18.5 Internal V_{CC} Regulator (VCC)

Good bypassing at the VCC pin is necessary to supply the high transient currents required by the MOSFET gate drivers. Place a low ESR MLCC capacitor (C = 1μF/0603) as close as possible to the VCC and AGND pins. Applications with high input voltage and high switching frequency will increase the die temperature because of the higher power dissipation across the LDO. Do not connect the VCC pin to provide power to other devices or loads.

18.6 External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1μF/0603 low ESR ceramic capacitor and ≤ 10Ω resistor between the BOOT and SW pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side MOSFET. The internal gate driver is optimized to turn on the high-side MOSFET fast enough for low power loss and good efficiency, but also slowly enough to reduce EMI. The most of EMI occurs since V_{SW} rises rapidly when the high-side MOSFET is turned on fast. In some cases, slightly increasing the R_{BOOT} reduces EMI and SW pin spikes directly, but the switching loss of the high-side MOSFET and die/case temperature are also increased.

18.7 Output Voltage Programming

For the RT6338A/AH/F/FH, an external resistive divider sets the output voltage according to the following equation:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{REF}$$

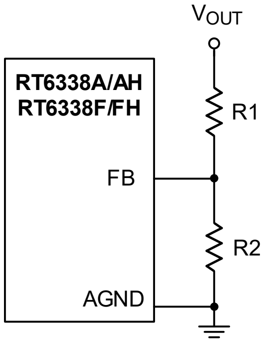


Figure 15. Output Voltage Setting

The recommended R2 is set to around 40kΩ. For a given R2, the resistance of R1 is calculated as below:

$$R1 = \frac{R2 \times \left(V_{OUT} - V_{REF}\right)}{V_{REF}}$$

1% resistors are recommended to maintain output voltage accuracy. Besides, the resistor divider generates a small load on the output, which influences the light-load efficiency. The total resistance of the FB resistor divider should be as large as possible when good light-load efficiency is desired.

Place resistors R1 and R2 very close to the FB pin to minimize PCB trace length and noise. Great care should be taken to route the FB trace away from noise sources, such as the inductor or the SW trace. For better transient and stability performance, it is recommended to add C_{FF}.

18.8 Feedforward Capacitor CFF Design

To save time for compensator design and to reduce the layout area through external components, the components of compensator are integrated in the IC. However, this integrated compensator might not be suitable for every load transient specification. Hence, to make the RT6338 more adaptable, the feedforward capacitor CFF is used in the feedback loop to improve transient response, as shown in Figure 16 and Figure 17. Figure 18 shows the comparison result of bode plot with different feedback loop conditions. As shown in Figure 18, adding a CFF to the feedback network increases both gain and phase in the mid-frequency, which not only extends the bandwidth but also boosts the phase margin. Moreover, there is also a high-frequency pole to eliminate high-frequency noise. Consequently, those features of the feedforward feedback network allow the RT6338 to have faster response to different load transients.

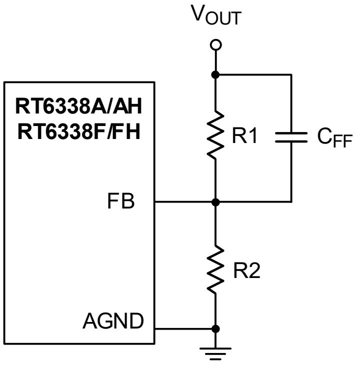


Figure 16. RT6338A/AH Feedback Loop with Feedforward Capacitor

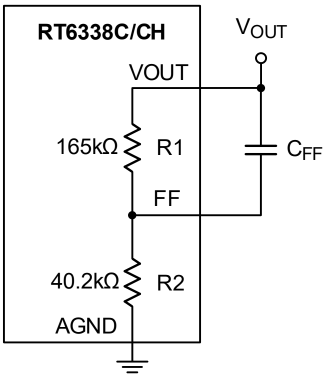


Figure 17. RT6338C/CH Feedback Loop with Feedforward Capacitor

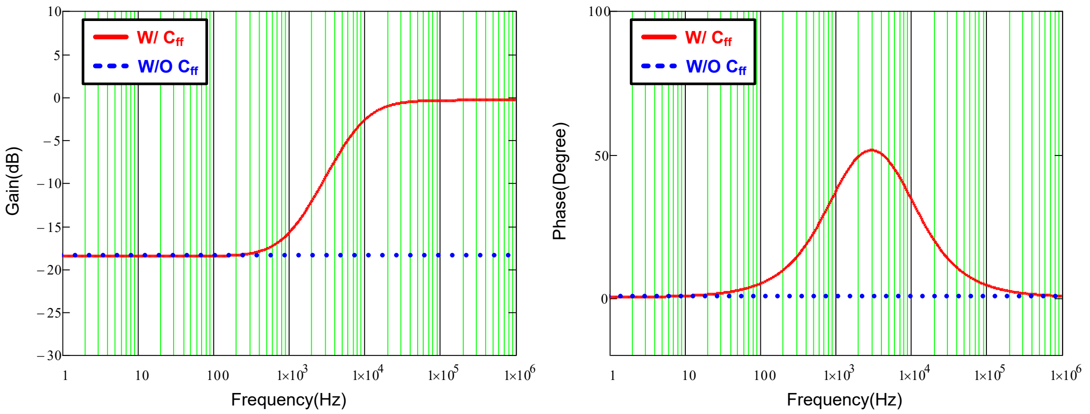


Figure 18. Bode Plot with Different Feedback Loop Conditions

The transfer function of the feedforward network is expressed in equation (1) and the positions of zero and pole are calculated in equation (2) and equation (3).

$$\frac{V_{FB}(s)}{V_{OUT}(s)} = \frac{1}{1+\frac{R1}{R2}} \times \frac{1+\frac{s}{\frac{1}{R1 \times C_{FF}}}}{1+\frac{s}{\frac{1}{(R1//R2) \times C_{FF}}}} \quad (1)$$

$$f_P = \frac{1}{2\pi \times R1//R2 \times C_{FF}} \quad (2)$$

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (3)$$

According to Figure 18, the maximum phase boost that occurs between zero and pole frequencies is defined as maximum phase boost frequency, as expressed in equation (4). Hence, in order to achieve the maximum phase boost by adding C_{FF} in the RT6338, the system's original bandwidth has to be located at maximum phase boost frequency.

$$f_{ph\_max} = \sqrt{f_P \times f_Z} \quad (4)$$

For putting zero at the correct frequency to implement maximum phase boost, the first thing is to determine system's bandwidth. A simple way to measure bandwidth of the RT6338 is through load transient analysis. By using a converter without feedforward network to observe the voltage deviation frequency during load step, the bandwidth of the converter is obtained since the crossover frequency is related to the voltage deviation frequency approximately, as shown in Figure 19.

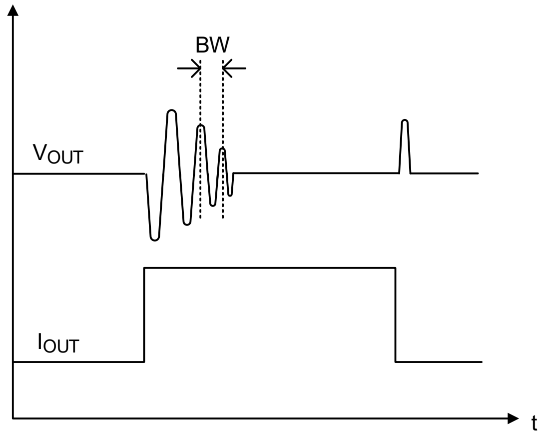


Figure 19. A Simple Way to Get the Bandwidth

Based on the above concept, the equation of bandwidth with feedforward C_{FF} is derived, as expressed in equation (5).

$$BW = \sqrt{\frac{1}{2\pi \times R1 \times C_{FF}} \times \frac{1}{2\pi \times C_{FF}}\left(\frac{1}{R1}+\frac{1}{R2}\right)} \quad (5)$$

For optimizing transient response, the C_{FF} is obtained from equation (5), as shown in equation (6).

$$C_{FF} = \frac{1}{2\pi \times BW} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1}+\frac{1}{R2}\right)} \quad (6)$$

After defining the C_{FF}, the load regulation should also be checked, because the feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage exceeds the specified range due to the calculated C_{FF}, the value of the feedforward capacitor C_{FF} should be reduced.

18.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a UQFN-23L 3x3 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, 30.6°C/W is measured in the natural convection at T_A = 25°C on a four-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C)/(30.6°C/W) = 3.27W for a UQFN-23L 3x3 (FC) package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curve in Figure 20 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

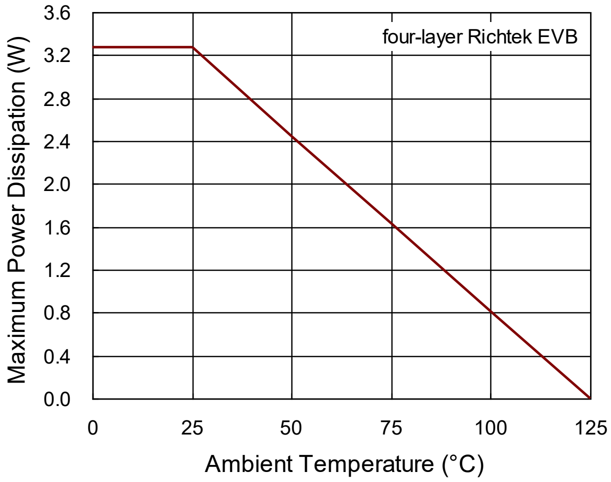


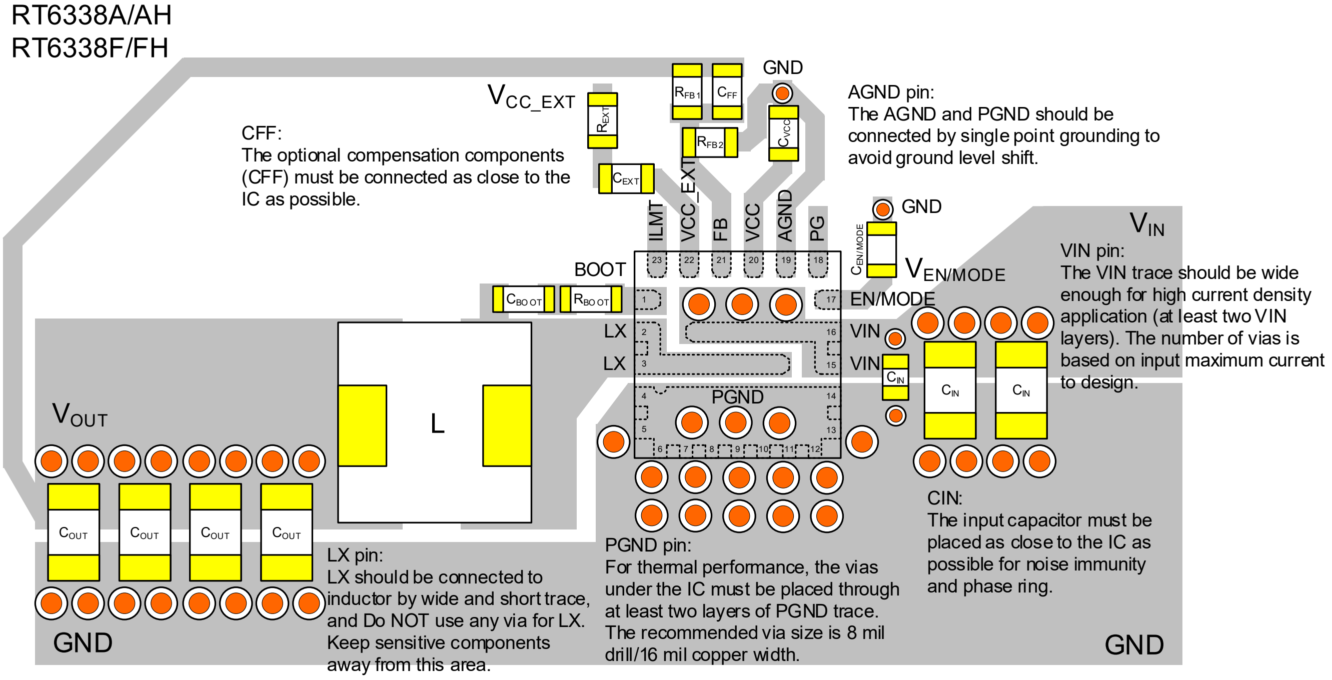
Figure 20. Derating Curve of Maximum Power Dissipation

18.10 Layout Considerations

Printed circuit board (PCB) layout design for switch-mode power supply IC is critical and important. Improper PCB layout brings lots of problems in the power supply, such as poor output voltage regulation, switching jitter, bad thermal performance, excessive radiated noise and reduced component reliability. To avoid those issues, designers must understand the current trace and signal flow in the switching power supply. The following are design considerations of PCB layout for switching power supply.

- To suppress phase ringing and extra power losses that affect device reliability, the input capacitor should be placed close to the VIN pin to reduce the influence of parasitic inductor.
- For thermal stress and power consumption considerations, the current paths of V_{IN} and V_{OUT} should be as short and wide as possible to decrease the trace impedance.
- Since the SW node voltage swings from V_{IN} to 0V with very fast rising and falling times, switching power supplies can suffer quite serious EMI issues. To eliminate EMI problems, the inductor must be put as close as possible to the IC to narrow the SW node area. Besides, the SW node should be arranged in the same plate to reduce coupling noise path caused by parasitic capacitance.
- For system stability and coupling noise elimination, the sensitive components and signals, such as control signals and feedback loop, should be kept away from the SW node.
- To enhance noise immunity on the VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to the IC.
- The feedback signal path from V_{OUT} to the IC should be wide and kept away from high switching paths.
- The trace width and numbers of vias should be designed based on application current. Make sure the switching power supply has great thermal performance and good efficiency.

Examples of PCB layout guides are shown in Figure 21 to Figure 23 for reference.



CFF:
The optional compensation components (CFF) must be connected as close to the IC as possible.

AGND pin:
The AGND and PGND should be connected by single point grounding to avoid ground level shift.

VIN pin:
The VIN trace should be wide enough for high current density application (at least two VIN layers). The number of vias is based on input maximum current to design.

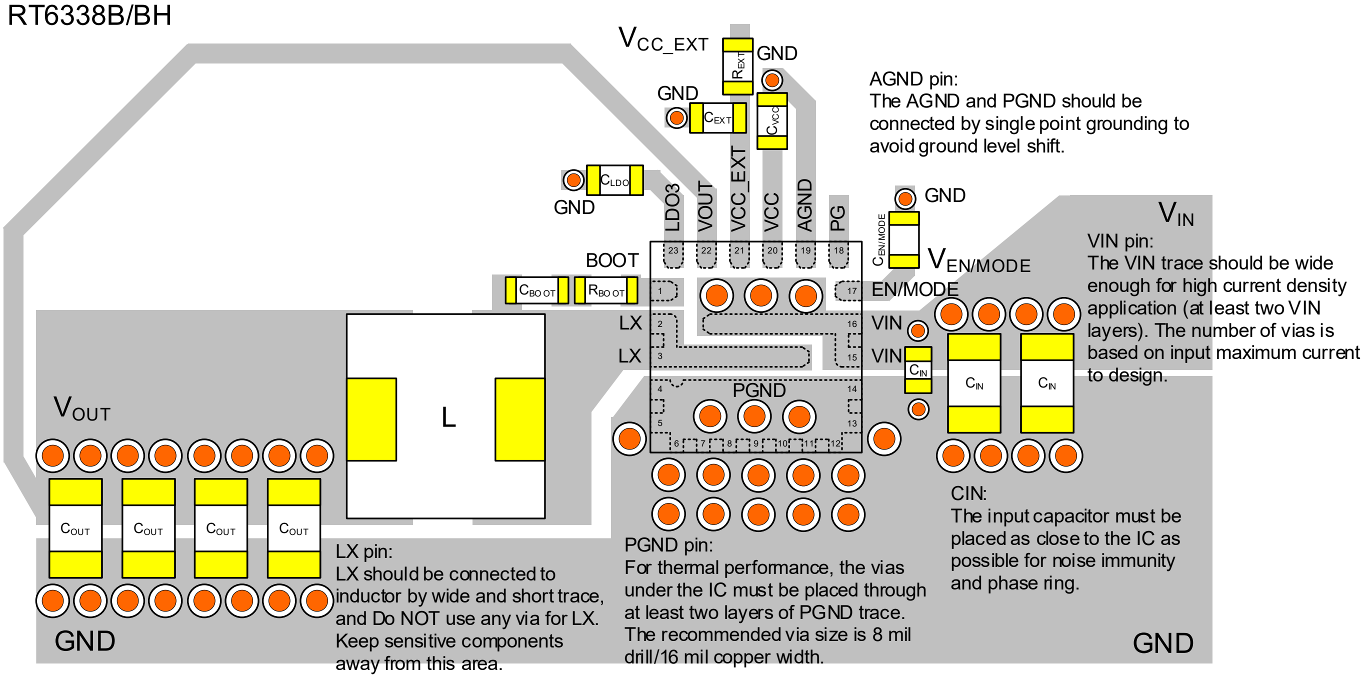
LX pin:
LX should be connected to inductor by wide and short trace, and Do NOT use any via for LX. Keep sensitive components away from this area.

PGND pin:
For thermal performance, the vias under the IC must be placed through at least two layers of PGND trace. The recommended via size is 8 mil drill/16 mil copper width.

CIN:
The input capacitor must be placed as close to the IC as possible for noise immunity and phase ring.

Figure 21. RT6338A/AH/F/FH Layout Guide

RT6338B/BH



AGND pin:
The AGND and PGND should be connected by single point grounding to avoid ground level shift.

VIN pin:
The VIN trace should be wide enough for high current density application (at least two VIN layers). The number of vias is based on input maximum current to design.

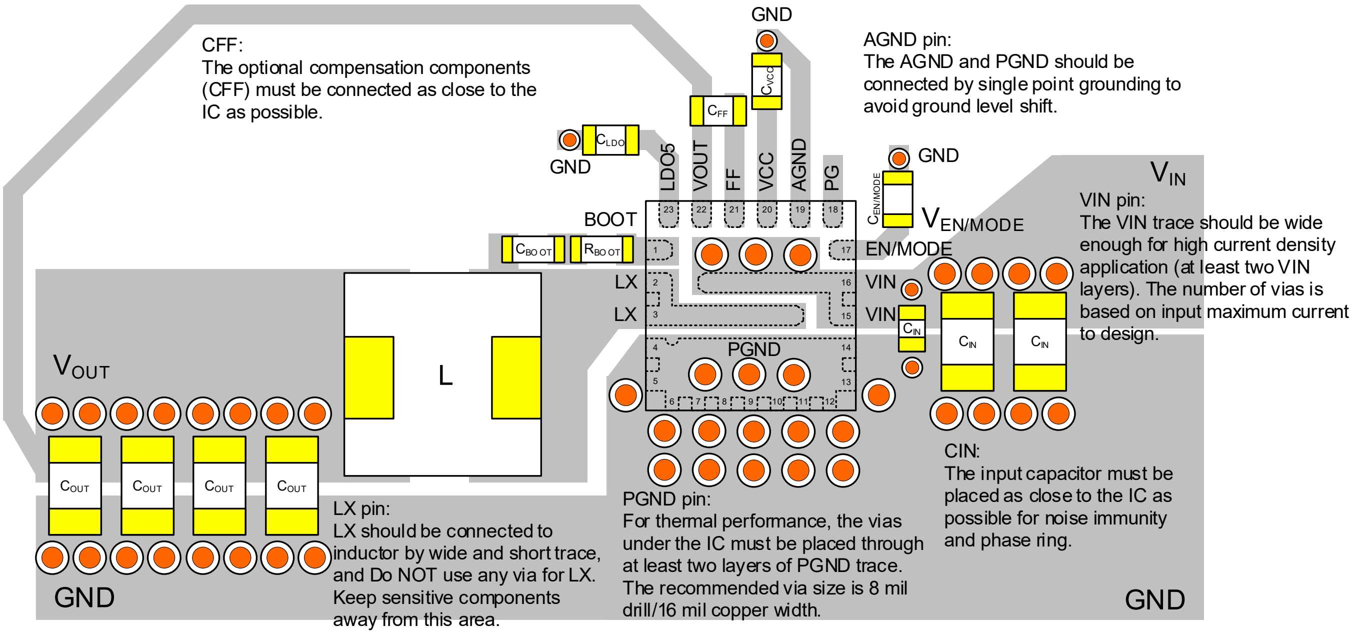
LX pin:
LX should be connected to inductor by wide and short trace, and Do NOT use any via for LX. Keep sensitive components away from this area.

PGND pin:
For thermal performance, the vias under the IC must be placed through at least two layers of PGND trace. The recommended via size is 8 mil drill/16 mil copper width.

CIN:
The input capacitor must be placed as close to the IC as possible for noise immunity and phase ring.

Figure 22. RT6338B/BH Layout Guide

RT6338C/CH



CFF:
The optional compensation components (CFF) must be connected as close to the IC as possible.

AGND pin:
The AGND and PGND should be connected by single point grounding to avoid ground level shift.

VIN pin:
The VIN trace should be wide enough for high current density application (at least two VIN layers). The number of vias is based on input maximum current to design.

LX pin:
LX should be connected to inductor by wide and short trace, and Do NOT use any via for LX. Keep sensitive components away from this area.

PGND pin:
For thermal performance, the vias under the IC must be placed through at least two layers of PGND trace. The recommended via size is 8 mil drill/16 mil copper width.

CIN:
The input capacitor must be placed as close to the IC as possible for noise immunity and phase ring.

Figure 23. RT6338C/CH Layout Guide

18.11 Thermal Performance

A well-designed PCB has optimized thermal performance and efficiency. Under the ambient temperature 25°C, and using the specified BOM list (refer to Table 1 and Table 2) and the Richtek evaluation board , the thermal images of the RT6338 are shown in Figure 24 to Figure 26.

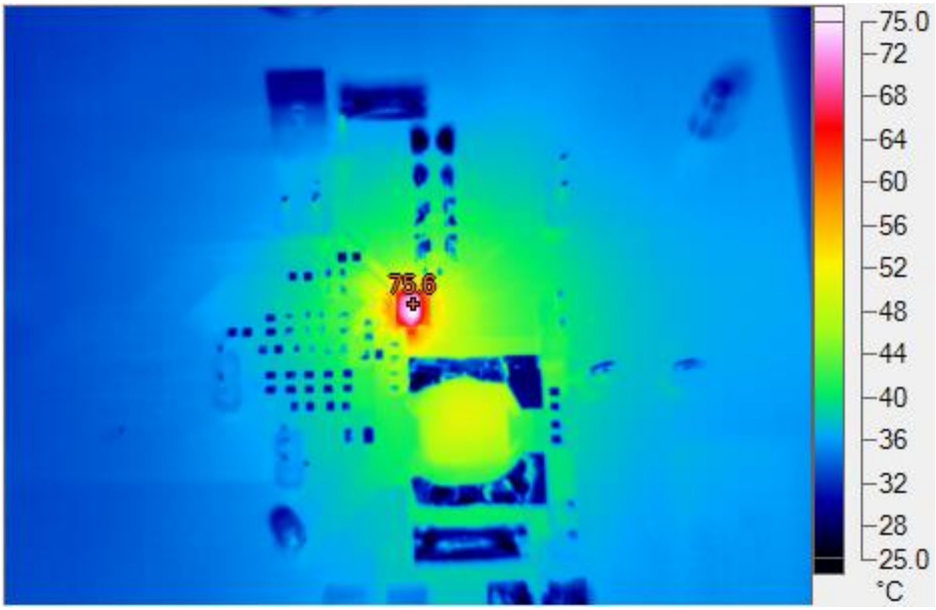


Figure 24. Thermal image of RT6338A/AH with V_{OUT} = 1.05V, V_{IN} = 19V, I_{OUT} = 8A and V_{CC_EXT} = 5V

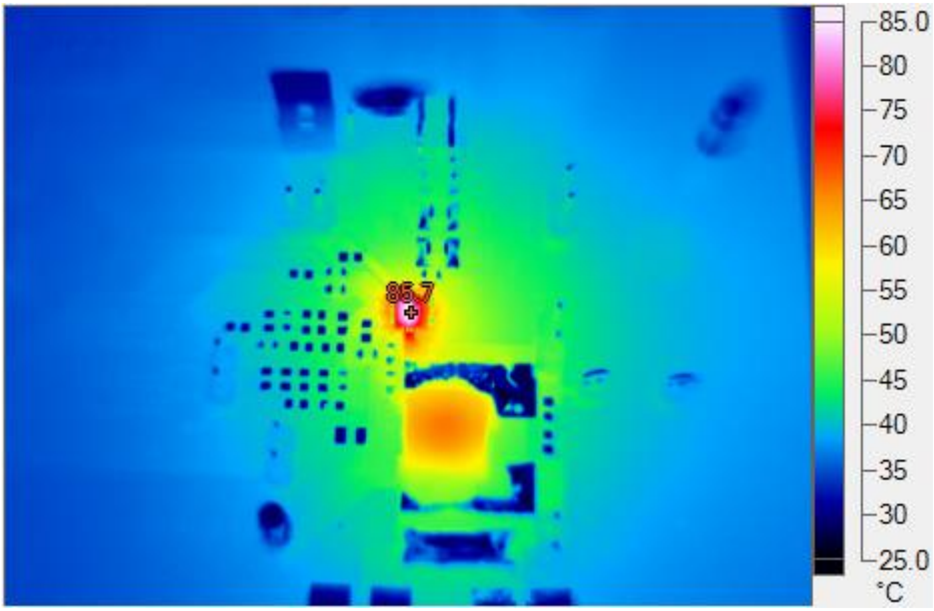


Figure 25. Thermal image of RT6338B/BH with V_{OUT} = 3.3V, V_{IN} = 19V, I_{OUT} = 8A and V_{CC_EXT} = 5V

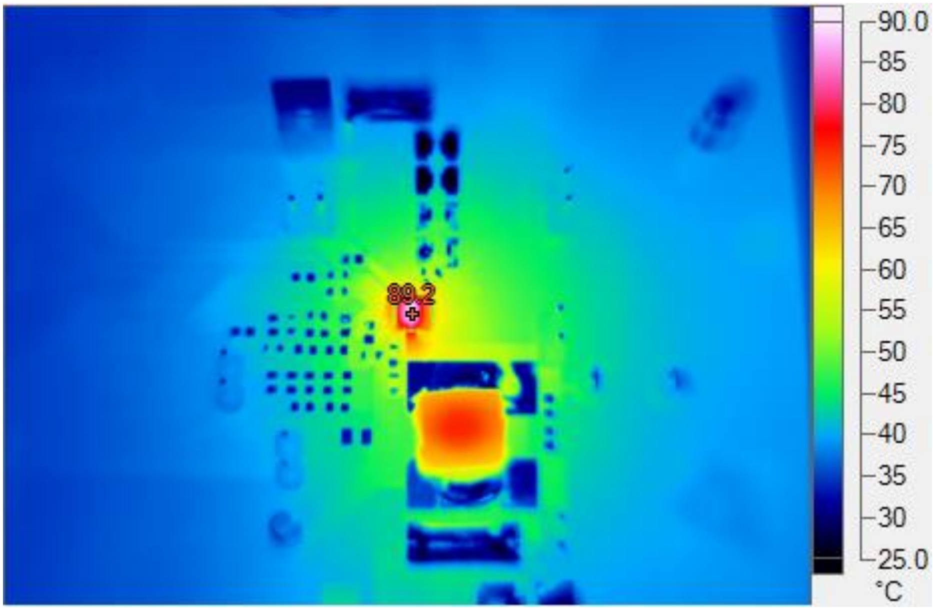
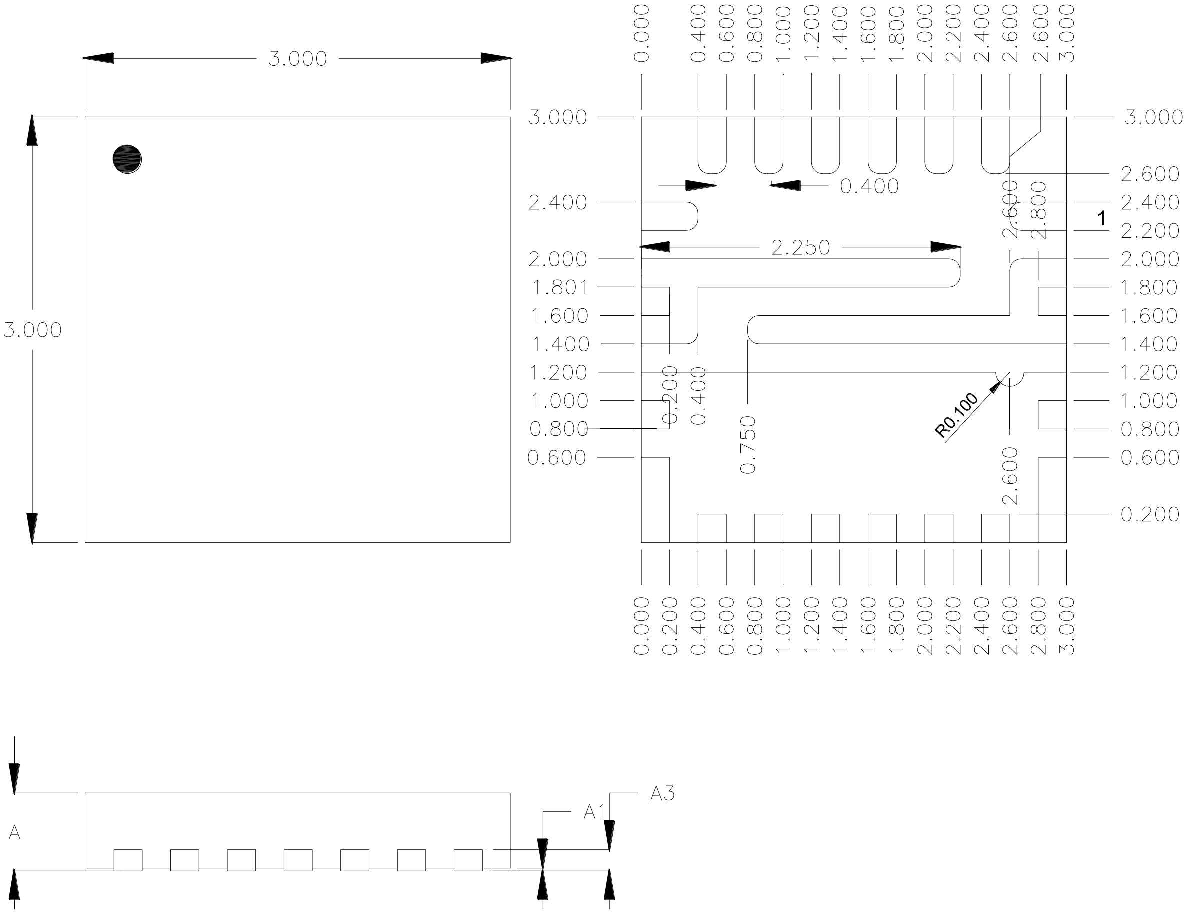


Figure 26. Thermal image of RT6338C/CH with V_{OUT} = 5.1V, V_{IN}=19V, I_{OUT} = 8A

Note 9. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

19 Outline Dimension

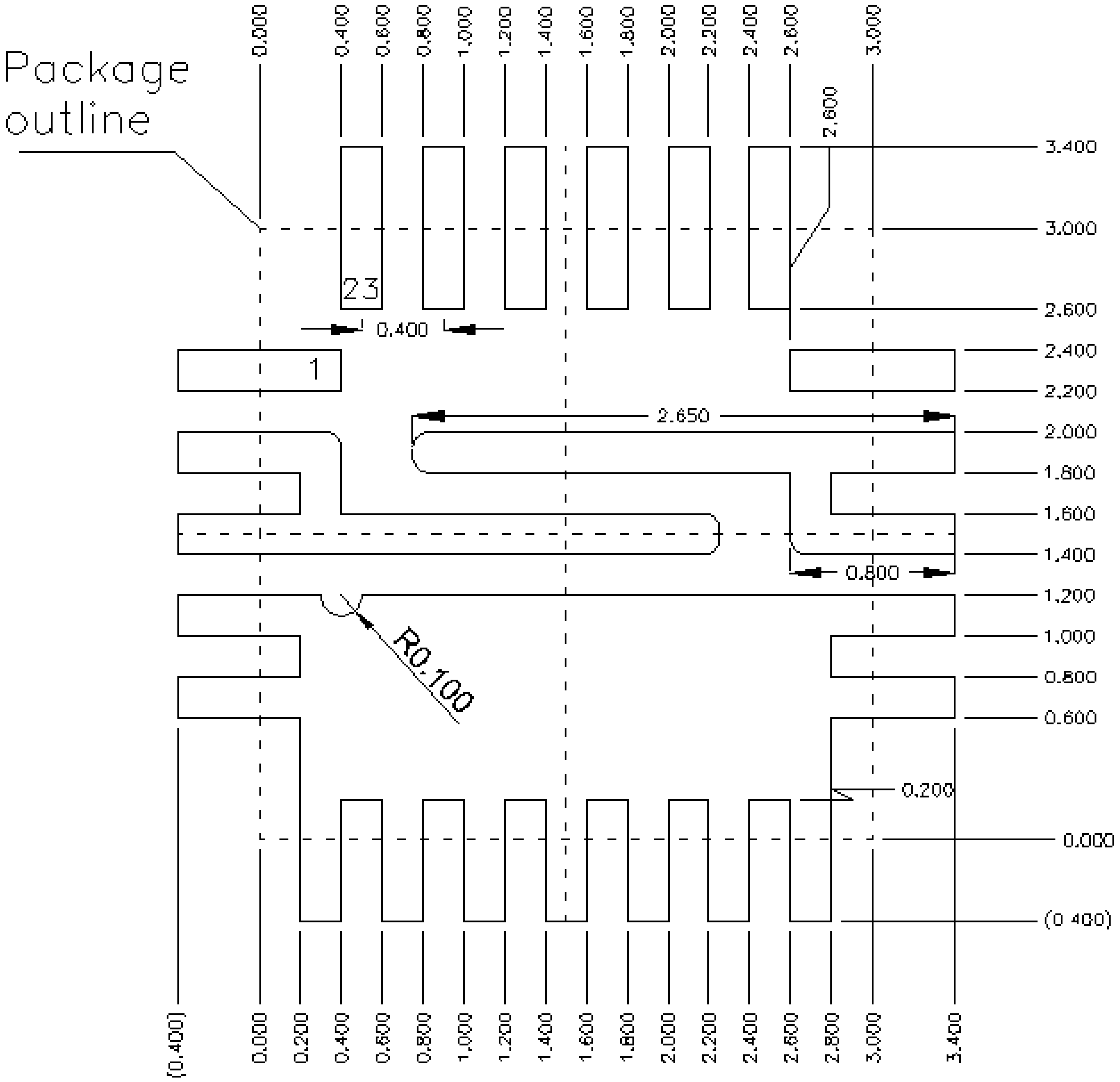


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008

Tolerance
±0.050

U-Type 23L QFN 3x3 (FC) Package

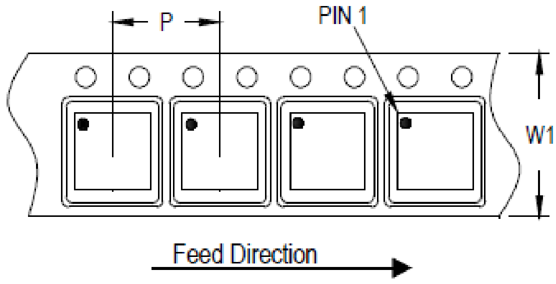
20 Footprint Information

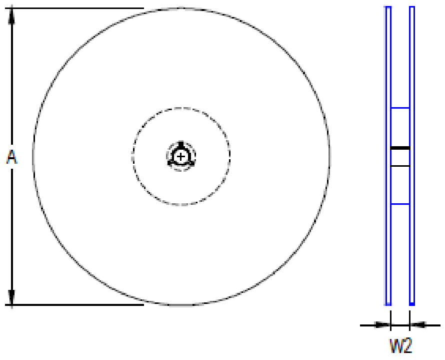


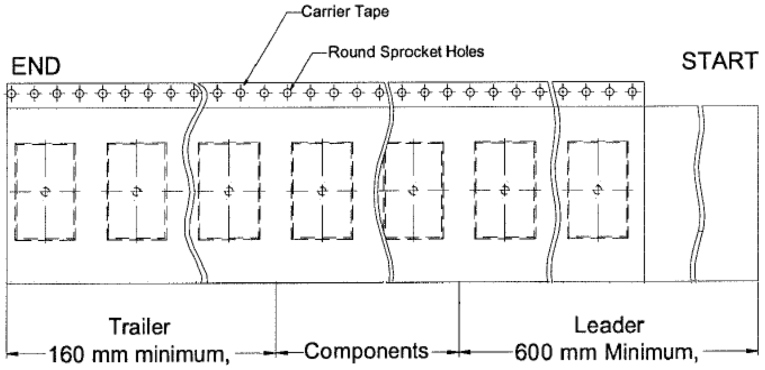
Package	Number of Pin	Tolerance
V/W/U/XQFN3x3-23(FC)	23	±0.05

21 Packing Information

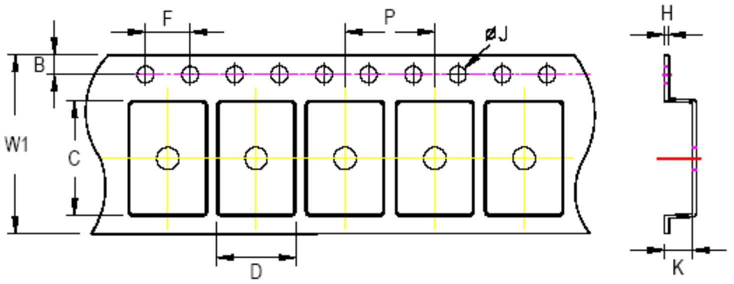
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(U) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.9mm	0.6mm

21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(U) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation
14F, No. 8, Taiyuan 1st St., Zhubei City,
Hsinchu County 302082, Taiwan (R.O.C.)
Tel: 886-3-5526-789

22 Datasheet Revision History

Version	Date	Description
03	2023/2/10	Operation Absolute Maximum Ratings Electrical Characteristics Application Information
04	2023/8/14	Ordering Information Operation
05	2024/4/11	General Description Outline Dimension Packing Information
06	2026/1/29	Changed the names PGOOD to PG Changed the names LX to SW Changed the Step-Down to Buck Add RT6338F/FH Marking Information Typical Operating Characteristics Packing Information - Added Tape Size “K”