10A, 23V Synchronous Step-Down Converter with 3.3V LDO

General Description

The RT6310E/EH family are high efficiency synchronous step-down DC-DC converters with pseudo constant switching frequency 500kHz and deliver up to 10A output current. The RT6310E/EH operate from 4.5V to 23V input voltage. The output voltage of RT6310E/EH is fixed to 3.36V output voltage.

The RT6310E/EH adopts Advanced Constant On-Time (ACOT®) control architecture that provides ultra-fast transient response and further reduces the external component count. In steady states, the ACOT® operates at nearly constant switching frequency over line, load and output voltage ranges and makes the EMI filter design easier.

By setting the voltage of the EN/MODE pin, RT6310E/EH operates either in diode emulation mode (DEM) or ultrasonic mode (USM) at light load. The USM maintains operation frequency above 25kHz, which eliminates the acoustic noise. In the DEM, RT6310E/EH provides the best light-load efficiency and improves the acoustic noise with spread spectrum function.

RT6310E/EH provides PGOOD indicator for easy system sequence control. Full protection features are also integrated in the device, including the cycle-by-cycle current limit, OVP, UVP, input UVLO and OTP.

All above functions are integrated in a UQFN-23L 3x3 (FC) package.

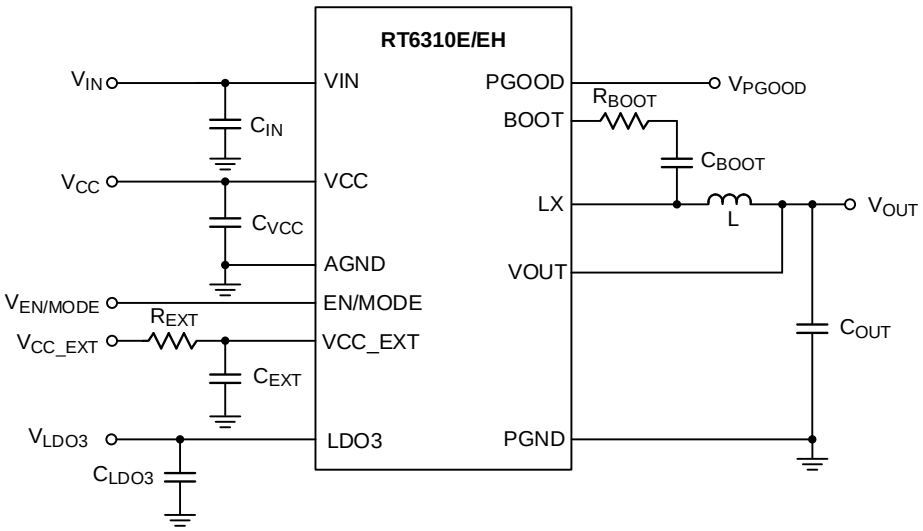
Features

- **Input Voltage Range**
  - **RT6310E/EH: 4.5V to 23V**
- **Output Voltage**
  - **RT6310E/EH: 3.36V**
- **10A Continuous Output Current**
- **Stable with POSCAP and MLCC Capacitor**
- **Fast Transient Response**
- **Diode Emulation Mode (DEM) for Power Saving**
- **Ultrasonic Mode (USM) for Avoiding Acoustic Noise**
- **Pseudo Constant Switching Frequency 500kHz in CCM**
- **Internal Power MOSFET Switch 17mΩ (high-side) and 7.5mΩ (low-side)**
- **LDO**
  - **RT6310E/EH: 3.3V/100mA**
- **Overcurrent Limit**
  - **RT6310E/EH: 15A**
- **Output Under-/Overvoltage Protection (UVP/OVP)**
  - **RT6310E: Latched Mode UVP/OVP**
  - **RT6310EH: Hiccup Mode UVP and Non-Latched Mode OVP**
- **Input Undervoltage-Lockout (UVLO)**
- **Over-Temperature Protection (OTP)**
  - **RT6310E: Latched Mode OTP**
  - **RT6310EH: Non-Latched Mode OTP**

Applications

- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

Simplified Application Circuit



Ordering Information

RT6310 □□□

- Package Type
  QUF : UQFN-23L 3x3 (FC) (U-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Output Voltage & Protection Option
  E : 3.36V & Latched Mode(1)
  EH : 3.36V & Hiccup Mode(2)

Note:

Richtek products are:

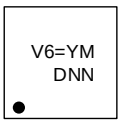
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

(1): Latched mode for UVP, OVP and OTP

(2): Hiccup mode for UVP & Non-latched mode for OVP and OTP

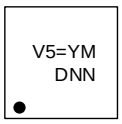
Marking Information

RT6310EGQUF



V6=: Product Code
YMDNN : Date Code

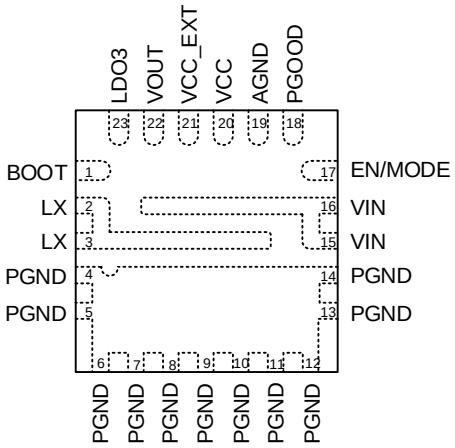
RT6310EHGQUF



V5=: Product Code
YMDNN : Date Code

Pin Configuration

(TOP VIEW)



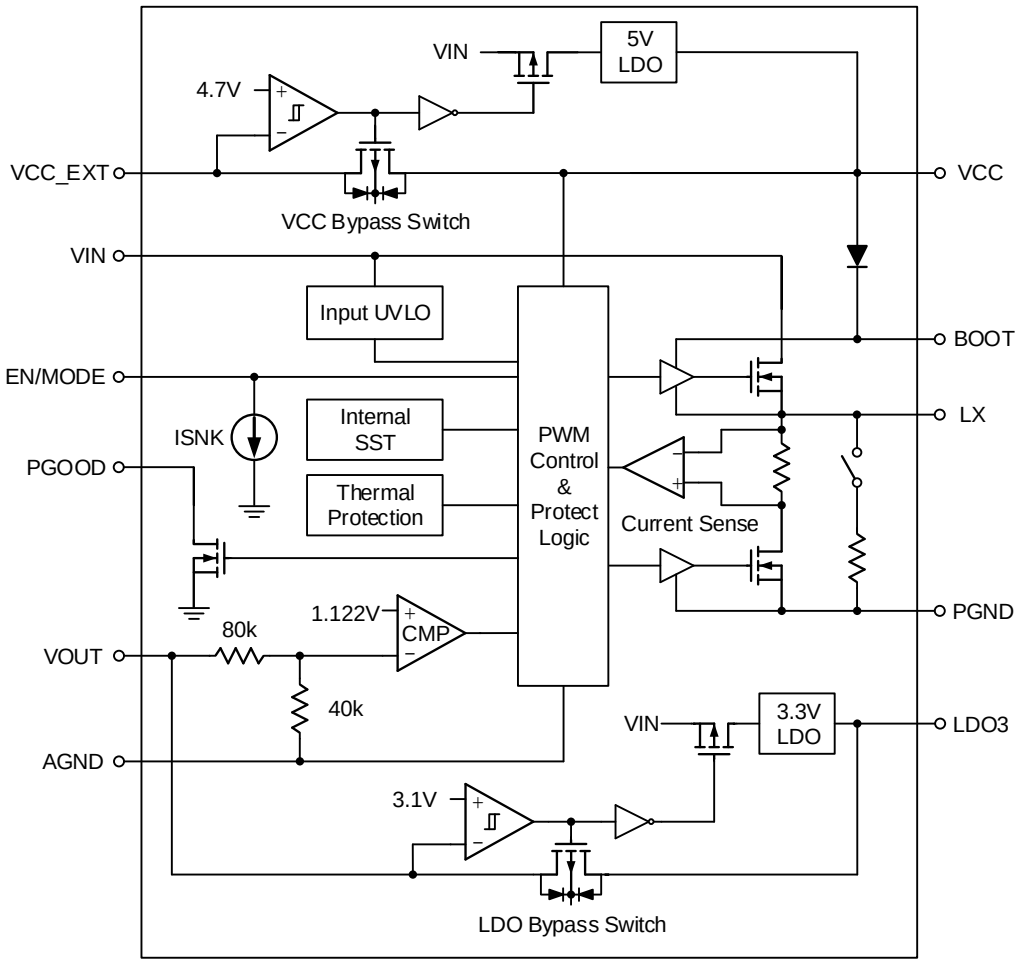
UQFN-23L 3x3 (FC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high-side gate driver. Connect a high quality and low ESR ceramic capacitor (minimum C = 0.1μF/0603) from BOOT pin to LX pin through a short and low inductance paths. During the period of low-side MOSFET turn-on, the bootstrap capacitor is charged by BOOT pin to store required energy for high-side gate driver. A bootstrap resistor (0603 size, ≤ 10Ω) in series with the bootstrap capacitor is strongly recommended for reducing the voltage spike at LX node.
2, 3	LX	Switch node of the buck converter is internally connected to the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET. LX is also used for the internal ramp generation, on-time generation and current detection. Connect this pin to output inductor and keep the sensitive trace and signals away.
4 to 14	PGND	Ground return from low-side power MOSFET and its driver. Directly soldering to a large PCB PGND plane and connecting thermal vias under PGND pin are required to minimize the parasitic impedance and thermal resistance.
15, 16	VIN	Input voltage pin. VIN pin is used to supply the internal bias voltage, VCC and LDO. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for the input trace. Connecting the ceramic capacitor (C = 10μF/0805x2 + 0.1μF/0603x1) as close as possible from VIN pin to PGND pin is necessary.
17	EN/MODE	Enable and operation mode control input. In order to ensure the IC logic status of turn-on/off, the low logic time length of EN/MODE control signal must be larger than 0.5μs. DO NOT leave this pin floating. RT6310E/EH supports either in diode emulation mode (DEM) or ultrasonic mode (USM) at light load (Table 1) through setting the voltage of the EN/MODE pin. Regarding the EN/MODE control logic of RT6310E/EH, please refer to Table 2.
18	PGOOD	Power good indicator is an open-drain output. This pin is pulled low as UVP, OVP, OTP, EN/MODE low or output voltage is not regulated (such as before soft-start). An external pull-up resistor to VCC or other external rail is required, and the recommended pull-up resistor ranges from 10kΩ to 100kΩ. Do not pull the PGOOD voltage higher than 6V.
19	AGND	Ground of internal analog circuitry. AGND must be connected to the PGND plane through a single point.
20	VCC	Internal LDO output. Used as supply to internal control circuits. DO NOT connect to any external loads. Connect a high-quality capacitor (C = 1μF/0603) from this pin to AGND. When the voltage on VCC_EXT pin is higher than "VCC bypass switch turn-on voltage", the VCC will be internally switchover to VCC_EXT (or VOUT) to reduce power consumption (refer to Figure 4).
21	VCC_EXT	External voltage input for VCC. If an external 5V supply voltage is applied to VCC_EXT pin, VCC will be internally switchover to VCC_EXT pin and the internal LDO of VCC will be disabled for further reducing the power consumption. Notice, in order to avoid any noise disturbance including switching noise, an external 5V supply voltage must be stable and constant. Hence, a RC filter (R = 1.1Ω/0603 and C = 4.7μF/0603) is required between an external 5V supply voltage and the VCC_EXT pin. It should be placed as close as possible to the VCC_EXT pin. Leave the VCC_EXT pin floating if this pin is not used.
22	VOUT	Output voltage sense pin. Connect to the output of buck converter. LDO3 (3.3V) will be internally switchover to VOUT pin when the LDO bypass switch is turned on. Furthermore, VOUT pin is used to detect output voltage status for OVP, UVP or PGOOD. If output voltage is below 60% of fixed output voltage 3.36V, the UVP is triggered. If output voltage is greater than 120% of fixed output voltage 3.36V, the OVP is triggered. After soft-start is completed, if output voltage is greater than 90% of fixed output voltage 3.36V, PGOOD is pulled high. Conversely, if output voltage is below 77% of fixed output voltage 3.36V, PGOOD is pulled low.

Pin No.	Pin Name	Pin Function
23	LDO3	Internal 3.3V LDO output. Bypass a capacitor (10μF/0603) to PGND. This pin is capable of sourcing 100mA. When input voltage exceeds the UVLO rising threshold, the internal 3.3V LDO is enabled. Besides, LDO3 switchovers to VOUT pin after soft-start period is finished.

Functional Block Diagram



Operation

The RT6310E/EH is a high efficiency synchronous step-down converter with integrated MOSFETs. The RT6310E/EH utilizes the proprietary Advanced Constant On-Time (ACOT®) control architecture providing vary fast transient response. The ultra-fast ACOT® control enables the use of small output capacitance and optimizes the component size without additional compensation network.

During normal operation, the high-side MOSFET turns on with a fixed one-shot on-time timer after the beginning of each clock cycle. The inductor current linearly increases when high-side MOSFET turns on and low-side MOSFET turns off. Similarly, the inductor current linearly decreases when high-side MOSFET turns off and low-side MOSFET turns on. The voltage ripple on the output has similar shape to the inductor current due to the output capacitor ESR.

The feedback voltage ripple comparing with an internal reference is caught by feedback resistor network. When a fixed minimum off-time timer is timeout and the inductor valley current is below the valley current-limit threshold, the fixed one-shot one-time timer is triggered if the feedback voltage falls below the feedback reference voltage. Therefore, the output voltage is regulated through the previously mentioned principle.

ACOT® Control Architecture

In order to achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. The internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

Conventional COT control implements the on-time timer proportional to V_{OUT} and inversely proportional to V_{IN} to achieve pseudo-fixed frequency with wide VIN range. A fixed on-time timer of conventional COT control has no compensation for the voltage drop of the MOSFETs and inductor during higher load condition.

In order to compensate the voltage drop of MOSFETs and inductor without influencing the fast transient behavior of the COT topology, a frequency locked loop system with slowly adjusting on-time timer is further added to the ACOT® control.

Average Output Voltage Control Loop

In continuous conduction mode, conventional COT control has DC offset between $V_{FB(average)}$ and V_{REF} as shown in Figure 1. In order to cancel the DC offset, the RT6310E/EH provides an average output voltage control loop to adjust the comparator input V_{REF}. Hence, the $V_{FB(average)}$ always follows the designed value. The control loop efficiently improves the load and line regulation without affecting the transient performance.

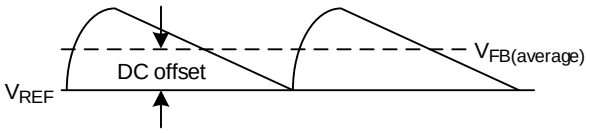


Figure 1. Conventional COT Control Loop Operation

High Voltage Conversion Ratio Function

In conventional COT control, the maximum duty cycle is limited by the minimum off-time. RT6310E/EH provides a feature of increasing the on-time function (up to 15μs) to extend the maximum duty cycle of 2S battery applications.

Diode Emulation Mode (DEM)

Diode emulation mode is selected by the EN/MODE voltage level. The device enters diode emulation mode when EN/MODE voltage is greater than 2.3V. In diode emulation mode, the RT6310E/EH automatically and smoothly reduces switching frequency at light-load conditions. As the output current decreases from heavy load to light load, the inductor current is naturally reduced. Once the valley point of inductor current touches to zero during decreasing output current, the behavior is boundary mode between continuous conduction and discontinuous conduction mode. In order to emulate the behavior of free-wheeling diode, the device only allows partial negative current flow from drain to source of the low-side MOSFET when inductor free-wheeling current becomes negative.

During decreasing output current, the discharge time of the output capacitor is gradually longer. When the

voltage on output capacitor is lower than the reference of regulating voltage, the next one-shot on-time timer is activated. On the contrary, when the output current increases from light load to heavy load and inductor current finally reaches to the continuous conduction, the switching frequency smoothly increases to preset value. The boundary load condition between continuous conduction and discontinuous conduction mode is shown in Figure 2 and is calculated as follows:

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times t_{ON}$$

where I_{LOAD} is the output loading current and t_{ON} is the on-time

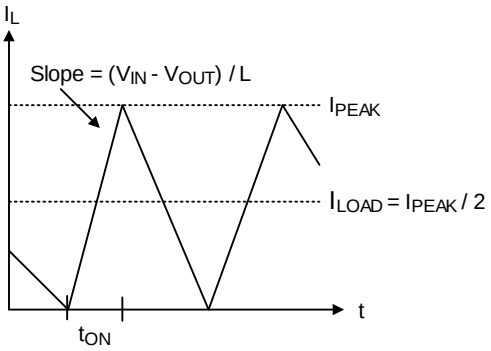


Figure 2. Boundary Condition of CCM/DEM

As mentioned above, diode emulation mode features natural high efficiency in the light-load conditions. In DEM operation (assuming that the coil resistance remains fixed), low inductor value has high efficiency and high output voltage ripple. However, high inductor value features low efficiency and less output voltage ripple. The drawback of using high inductor value includes larger physical size and lower load transient response (especially at low input voltage level).

Ultrasonic Mode (USM)

The RT6310E/EH activates a unique type of diode emulation mode with a minimum switching frequency of 25kHz, called ultrasonic mode. The acoustic frequency is avoided in ultrasonic mode. Ultrasonic mode is selected by the EN/MODE voltage level. If EN/MODE voltage ranges from 0.88V to 1.7V, the device operates in ultrasonic mode.

When the internal 25kHz oscillator is triggered, the one-shot on-time timer is activated for turning on high-side MOSFET. Once the one-shot on-time timer is completed, the low-side MOSFET is turned on with off-time timer. After the one-shot on-time timer and off-time timer are finished, the device keeps both high-side and low-side MOSFET off and waits for next trigger.

In order to regulate output voltage with 25kHz minimum switching frequency, the one-shot on-time timer and off-time timer are adjusted based on load condition. In no-load condition, the shorter one-shot on-time timer and longer off-time timer are applied as initial value. In this manner, the inductor current decreases to negative value during the off-time state. When the output current slowly increases from no load, the valley point of inductor current is increased by reducing the width of off-time timer until the inductor valley point reaches from negative value to zero. In previous load condition, if the output current is further increased, the width of on-time timer is gradually increased from shorter value to normal value before the switching frequency is higher than 25kHz. Once the switching frequency is higher than 25kHz with increasing output current, the behavior of device is changed from ultrasonic mode to diode emulation mode.

On-Time Reduction Function for DEM

In normal diode emulation mode, the output voltage ripple of converter is proportional to on-time and inversely proportional to load current. In order to have smaller voltage ripple in light-load applications, the RT6310E/EH provides a smart reduction on-time function. The smart reduction on-time function naturally decreases on-time when load current is decreasing. Therefore, the output voltage ripple is reduced.

Spread Spectrum Function for DEM

In order to reduce the acoustic noise in diode emulation mode, RT6310E/EH provides spread spectrum function with randomly adjusted on-time. The random variation value is ±7% of normal on-time value. Once the load condition enters to CCM, the device disables the spread spectrum function because switching frequency is much higher than acoustic frequency.

EN/MODE Sink Current

The RT6310E/EH does not allow uncertain voltage on EN/MODE pin, which may cause the logic or behavior error on device. In order to prevent the EN/MODE pin from floating, the RT6310E/EH builds the EN/MODE input current for eliminating floating voltage on EN/MODE pin. The characteristic of EN/MODE input current vs EN/MODE input voltage is shown in Figure 3.

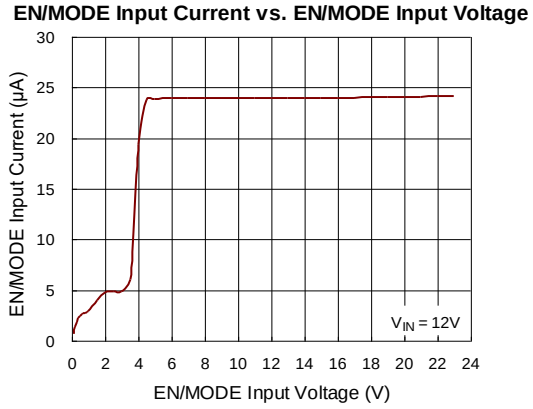


Figure 3. Characteristics of EN/MODE Input Current

Soft-Start

The RT6310E/EH provides an internal soft-start to prevent large input inrush current and output voltage overshoot. If EN/MODE voltage and input voltage exceed their rising thresholds, the soft-start function is activated. The V_{FB} starts to track the internal reference voltage ranging from zero to the target.

Valley Current Limit

The RT6310E/EH features a cycle-by-cycle valley current limit for avoiding the large output current and overheat. The device cycle-by-cycle compares the valley current of the inductor with the valley current-limit threshold. The output current is limited to the sum of the valley current and a half of ripple current when valley current of inductor reaches valley current-limit threshold.

After the device completes the minimum off-time and keeps ON state of low-side MOSFET, the inductor valley current level is monitored by measuring the low-side MOSFET voltage between the LX pin and PGND pin during the ON state of low-side MOSFET. During the ON state of low-side MOSFET, the measured low-side MOSFET voltage is proportional to the low-side MOSFET current. In order to improve the accuracy of measured current, the temperature compensation circuit is built internally.

In order to prevent the device from overcurrent, if the measured low-side MOSFET current is higher than valley current-limit threshold, the device remains ON state of the low-side MOSFET and the one-shot on-time timer is inhibited until its current linearly decreases lower than valley current-limit threshold. Once the low-side MOSFET current is below valley current-limit threshold, the next one-shot on-time timer is permitted to generate. The circuit of the cycle-by-cycle valley current limit works in every switching cycle.

Peak Current Limit

The RT6310E/EH with a cycle-by-cycle peak current limit prevents the device from inductor saturation or any possibility of damage caused by too much output inrush current. The device cycle-by-cycle compares the peak current of the inductor with the peak current-limit threshold.

After the device finishes the minimum on-time timer and remains ON state of high-side MOSFET, the inductor peak current level is monitored by sensing the high-side MOSFET voltage between the VIN pin and LX pin during the ON state of high-side MOSFET. During the ON state of high-side MOSFET, the measured high-side MOSFET voltage is proportional to the high-side MOSFET current.

In order to prevent the device from inductor saturation or any risk of damage, if the measured high-side MOSFET current is higher than peak current-limit threshold, the on-time timer is terminated immediately to limit the inductor current and the inductor current is decreased by turning on the low-side MOSFET. Once the low-side MOSFET current is below valley current-limit threshold, the next one-shot on-time timer is permitted to generate. The circuit of the cycle-by-cycle peak current limit works in every switching cycle.

Output Undervoltage Protection (UVP)

The output undervoltage protection of RT6310E/EH includes latched and hiccup mode. If the inductor current is higher than current-limit threshold (valley/peak current-limit threshold) during heavy-load

condition, the output voltage tends to drop because the load demand exceeds that the converter can support.

When the load demand is larger than the current ability of converter, the V_{OUT} (RT6310E/EH) starts to drop. Once the V_{OUT} drops below typical 60% of target voltage and the time length of this state is larger than the time width 11μs (typical), the latched/hiccup mode UVP is triggered. The different behaviors for latched/hiccup mode UVP is as follows:

- The RT6310E provides output undervoltage protection (UVP) with latched mode. Once UVP is triggered, the IC stops PWM switching and enter latched mode. If UVP event is released, users should re-toggle the EN/MODE pin or power recycle VIN supply to re-power on the device.
- The RT6310EH provides output undervoltage protection (UVP) with hiccup mode. Once UVP is triggered, the IC takes a determined period for initiating auto-recovery soft-start sequence. If UVP event is released, the output voltage is regulated to target reference.

Output Overvoltage Protection (OVP)

The output overvoltage protection of RT6310E/EH includes latched and non-latched mode. If the V_{OUT} rises above typical 120% of target voltage and the time length of this state is larger than the time width 12μs (typical), the latched/non-latched mode OVP is triggered. The different behaviors of latched/non-latched mode OVP is as follows:

- The RT6310E provides output overvoltage protection (OVP) with latched mode. Once OVP is triggered, the IC stops PWM switching and enter latched mode. If OVP event is released, users should re-toggle the EN/MODE pin or power recycle VIN supply to re-power on the device.
- The RT6310EH provides output overvoltage protection (OVP) with non-latched mode. Once OVP is triggered, the IC stops PWM switching and enter non-latched mode. If the OVP condition is released and the output voltage is lower than regulation level, the device returns to regulate output voltage.

Over-Temperature Protection (OTP)

The over-temperature protection of RT6310E/EH includes latched and non-latched mode. OTP circuitry prevents device from overheating due to excessive power dissipation. If the junction temperature of device exceeds typical 150°C, the OTP is triggered to stop the temperature rising. The behaviors of latched and non-latched mode OTP is as follows:

- The RT6310E provides over-temperature protection (OTP) with latched mode. Once OTP is triggered, the IC stops PWM switching and enter latched mode. If OTP event is released, users should re-toggle the EN/MODE pin or power recycle VIN supply to re-power on the device.
- The RT6310EH provides over-temperature protection (OTP) with non-latched mode. Once OTP is triggered, the IC stops PWM switching and enter non-latched mode. If the junction temperature of device drops below typical 130°C , the device enables the soft-start function to build the output voltage.

Input Undervoltage-Lockout (UVLO)

The RT6310E/EH provides an Undervoltage-Lockout (UVLO) function that monitors the input voltage. In order to protect the device from operating at insufficient input voltage, the UVLO function inhibits switching when input voltage drops below the UVLO falling threshold. The IC resumes switching when input voltage exceeds the UVLO rising threshold.

Enable Control and Mode Selection

The EN/MODE pin integrates both enable control and mode selection (USM/DEM) for RT6310E/EH. If EN/MODE voltage is less than 0.23V, the RT6310E/EH is turned off (shutdown). If EN/MODE voltage ranges from 0.88V to 1.7V, the RT6310E/EH is turned on and the operation mode is USM. Moreover, if EN/MODE voltage is larger than 2.3V, the RT6310E/EH is turned on and the operation mode is DEM. For the EN/MODE control logic and operation mode selection, please refer to Table 1 and Table 2.

Table 1. RT6310E/EH Operation Mode Selection

Part Number	EN/MODE Voltage	Operation Mode
RT6310E/EH	< 0.23V	Shutdown
RT6310E/EH	0.88V ~ 1.7V	USM
RT6310E/EH	≥ 2.3V	DEM

Table 2. RT6310E/EH Power Logic

Notice: 0 = Logic low, 1 = Logic high, X = Don't care, ON = Active, OFF = Inactive, N/A = Not applicable						
Part Number	Input*		Output			
	EN/MODE*	VCC_EXT*	VCC Bypass Switch	VCC	LDO	VOUT
RT6310E/EH	0	X	OFF	ON	ON	OFF
	1	0	OFF	ON	ON	ON
	1	1	ON	ON	ON	ON

Input*: VIN is ready in the whole power logic table.
EN/MODE*: Logic = 1 means $V_{EN/MODE}$ > 0.88V. Logic = 0 means $V_{EN/MODE}$ < 0.23V
VCC_EXT*: Logic = 1 means VCC_EXT > 4.9V. Logic = 0 means VCC_EXT < 4.2V.

Internal Output Voltage Discharge

The RT6310E/EH has an output voltage discharge function by using an internal MOSFET 50Ω (typical), which is connected from the LX pin to PGND pin. The output voltage discharge function is enabled if any of the following events is triggered:

- Input undervoltage-lockout (UVLO)
- Output under/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- EN/MODE pin is pulled low

Internal V_{CC} Regulator (VCC)

The internal V_{CC} regulator is a linear regulator. The V_{CC} regulator steps down input voltage to typical 5V in order to supply both internal circuitry and gate drivers. DO NOT connect to any external loads. Connect a capacitor (C = 1μF/0603) from VCC pin to AGND pin. RT6310E/EH enables V_{CC} regulator after V_{IN} rises higher than UVLO rising threshold. The power logic of V_{CC} is shown in Table 2.

Low Dropout Regulator (LDO)

RT6310E/EH have 3.3V LDO, respectively. The output current capability of these two LDOs are 100mA. The output current limit of these two LDOs are 200mA. Once the input voltage exceeds the UVLO rising threshold, the LDO is enabled.

In order to reduce the power consumption, LDO switchovers to VOUT pin through the LDO bypass switch when the following events are all satisfied:

- Soft-start is completed
- VOUT pin voltage is higher than LDO bypass switch turn-on voltage
  - LDO bypass switch turn-on voltage of RT6310E/EH is 3.1V

The LDO bypass switch is turned off when any of the following specified events is triggered:

- Input undervoltage-lockout (UVLO)
- Output under/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- EN/MODE pin is pulled low
- Soft-start is not completed
- The VOUT pin voltage is lower than LDO bypass switch turn-off voltage (LDO bypass switch turn-on voltage minus LDO bypass switch hysteresis voltage)
  - LDO bypass switch turn-off voltage of RT6310E/EH is 2.9V

External Voltage Input for V_{CC} (VCC_EXT)

The RT6310E/EH have VCC_EXT pin. In order to reduce the power consumption, the internal V_{CC} regulator switchovers to VCC_EXT through the VCC bypass switch if VCC_EXT pin is connected to an external voltage larger than typical 4.7V. Once the voltage of VCC_EXT pin is lower than typical 4.5V, the VCC bypass switch is disconnected. The power logic of VCC_EXT is shown in Table 2.

Power Good (PGOOD)

The PGOOD pin is an open-drain output. An external pull-up resistor to VCC or other external rail is required, and the recommended pull-up resistor ranges from 10k to 100k. Do not pull the PGOOD voltage higher than 6V. In order to prevent unwanted PGOOD glitches during load transient or dynamic V_{OUT} change, the RT6310E/EH provides PGOOD low deglitch time with typical 20μs.

The PGOOD pin is pulled low when any of the following specified events is triggered:

- Input undervoltage-lockout (UVLO)
- Output under/overvoltage protection (UVP/OVP)
- Over-temperature protection (OTP)
- EN/MODE pin is pulled low
- Soft-start is not completed
- The VOUT pin voltage is lower than PGOOD falling threshold (PGOOD rising threshold minus PGOOD hysteresis voltage) of the target voltage

Power Sequence

The power sequence of RT6310E/EH includes VIN pin power on/off and EN/MODE pin power on/off. The detailed sequence information is shown in Figure 4 to Figure 6.

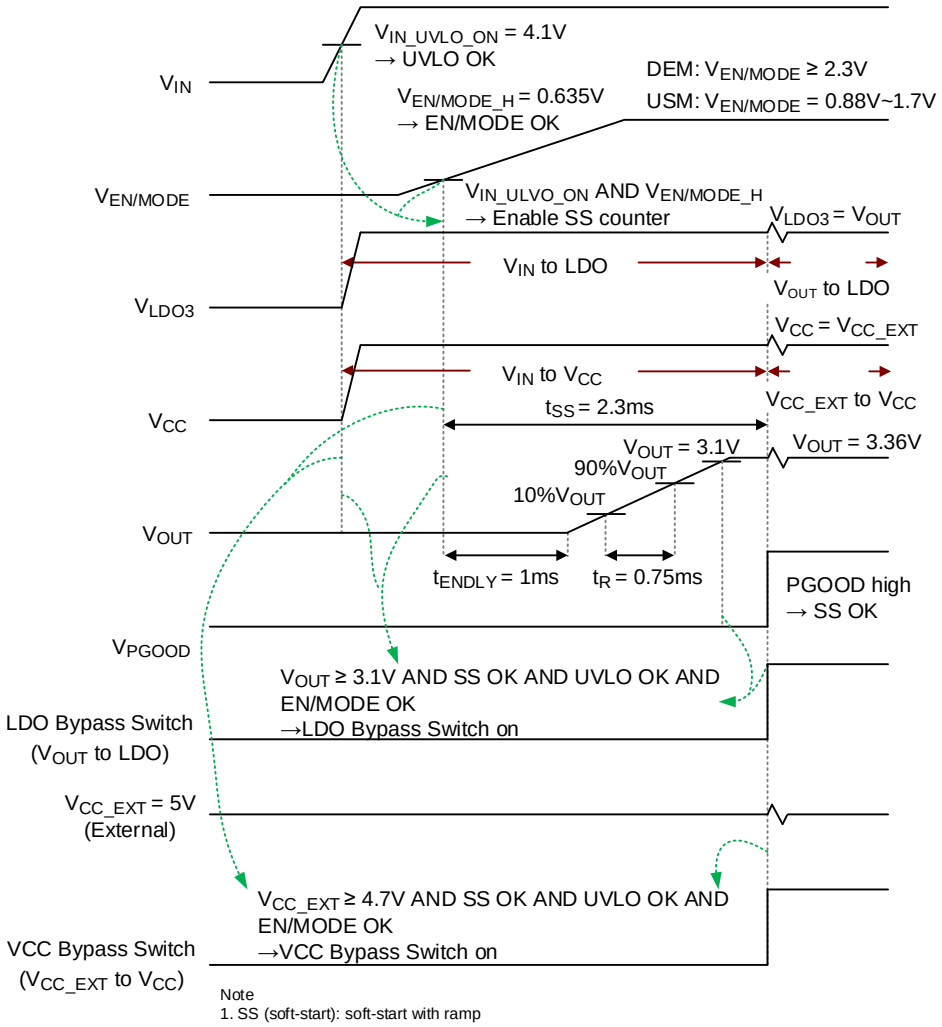


Figure 4. Power-on sequence of RT6310E/EH: Ramping Up VIN Followed by VEN/MODE

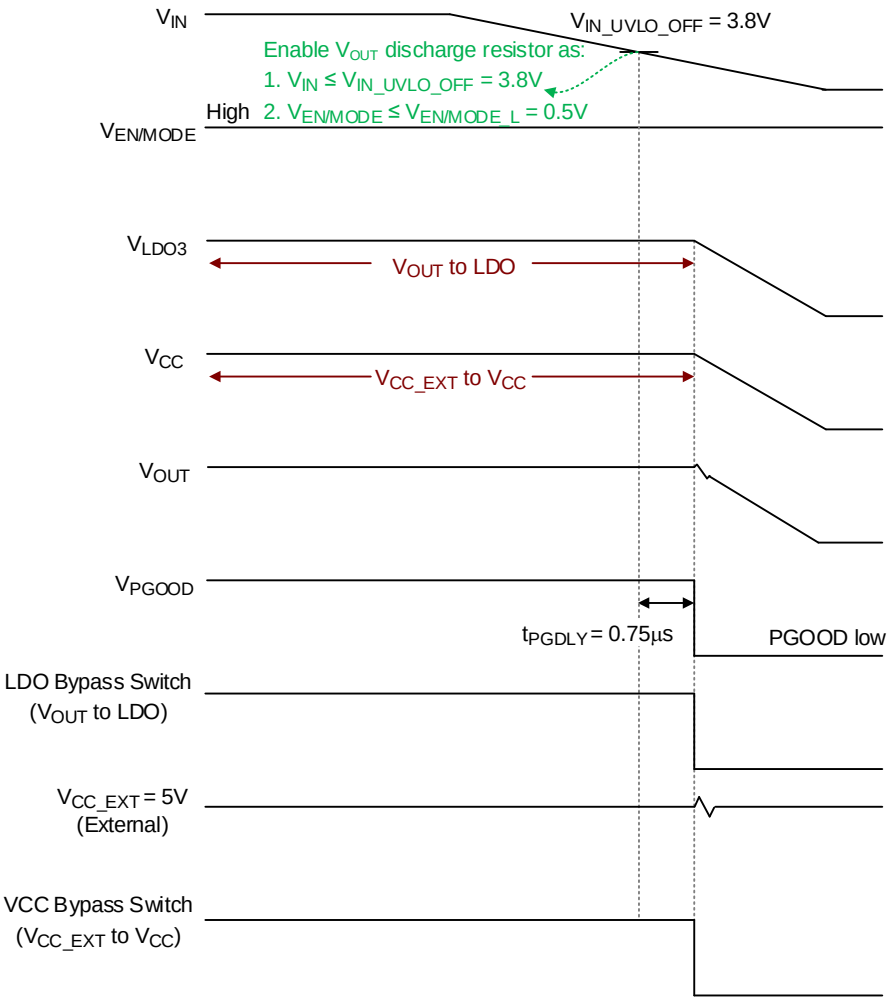


Figure 5. Power-off sequence of RT6310E/EH: Ramping Down V_{IN}

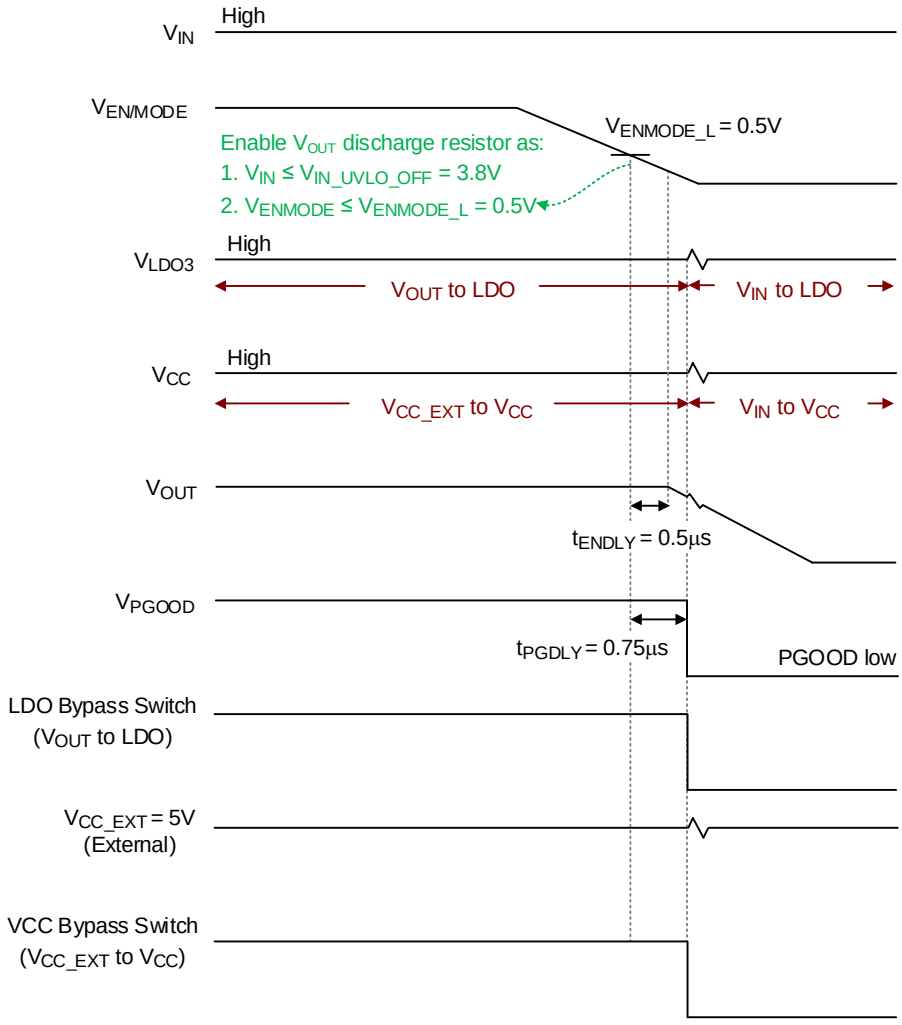


Figure 6. Power-off sequence of RT6310E/EH: Ramping Down $V_{EN/MODE}$

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 28V
- Enable/Mode Pin Voltage, $V_{EN/MODE}$ ---------- –0.3V to 28V
- VCC Pin Voltage, V_{CC} ---------- –0.3V to 6.5V
- VOUT Pin Voltage, V_{OUT} ---------- –0.3V to 4.5V
- Switch Voltage, V_{LX} ---------- –0.3V to (V_{IN} + 0.3V)
  <10ns ---------- –10V to 38V
  <5ns ---------- –14V to 38V
- Boot Voltage, V_{BS} ---------- (V_{LX}–0.3V) to (V_{LX} + 6V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings

- ESD Susceptibility (Note 2)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 4.5V to 23V
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		UQFN-23L 3x3 (FC)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	34.3	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	5.2	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	30.1	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	0.08	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.6	°C/W

Electrical Characteristics

(V_{IN} = 12V. The typical values are referenced to T_A = T_J = 25°C. Both minimum and maximum values are referenced to T_A = T_J from −10°C to 105°C. Unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
Input Voltage Range	V_{IN}	RT6310E/EH	4.5	--	23	V
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	RT6310E/EH: $V_{EN/MODE}$ = 0V	--	45	--	μA
Supply Current (Quiescent)	I_Q	RT6310E/EH: $V_{EN/MODE}$ = 5V (diode emulation mode), V_{OUT} = V_{SET} x 105%, not switching	75	95	130	μA
UVLO						
UVLO Rising Threshold	V_{UVLO_Rising}	RT6310E/EH	3.8	4.1	4.4	V
UVLO Hysteresis	V_{HYS}		--	0.3	--	V
Enable/Mode Logic Threshold and Timing						
EN/MODE Input High Voltage	$V_{EN/MODE\_H}$		400	635	880	mV
EN/MODE Input Low Voltage	$V_{EN/MODE\_L}$		230	500	800	mV
EN/MODE Input Current	$I_{EN/MODE}$	$V_{EN/MODE}$ = 0.1V	0	2	4	μA
Ultrasonic Mode	$V_{EN/MODE}$		0.88	--	1.7	V
Diode Emulation Mode	$V_{EN/MODE}$		2.3	--	--	V
Output Voltage						
Output Voltage Set Point	V_{OUT}	RT6310E/EH, T_A = T_J = 25°C, CCM	3.326	3.36	3.394	V
VCC Regulator Voltage	V_{CC}		--	5	--	V
On-Resistance						
High-Side MOSFET On-Resistance	$R_{DS(ON)\_H}$	T_A = T_J = 25°C	--	17	--	mΩ
Low-Side MOSFET On-Resistance	$R_{DS(ON)\_L}$	T_A = T_J = 25°C	--	7.5	--	mΩ
Discharge MOSFET On-Resistance	R_{DISCHG}	T_A = T_J = 25°C, $V_{EN/MODE}$ = 0V. From LX to PGND	30	50	100	Ω
Current Limit						
Low-Side MOSFET Valley Current Limit	I_{LIM_VY}	RT6310E/EH T_A = T_J = 25°C	12	15	18	A
Oscillator Frequency						
Oscillator Frequency	f_{OSC}		400	500	600	kHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}		--	50	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	200	--	ns

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Ultrasonic Mode							
Operation Period	t_{USM}			20	30	40	μs
Soft-Start							
Soft-Start Time	t_{SS}	RT6310E/EH	T_A = T_J = 25°C, from EN/MODE high to PGOOD high	1.7	2.3	2.9	ms
Output Rising Time	t_R	RT6310E/EH	T_A = T_J = 25°C, from 10% to 90% V_{OUT}	--	0.75	1.22	ms
Output Overvoltage Protection							
Output Overvoltage Threshold		RT6310E/EH: V_{OUT} rising		114	120	126	%
Output Overvoltage Deglitch Time				--	12	--	μs
Output Overvoltage Hysteresis		RT6310EH		--	8	--	%
Output Undervoltage Protection							
Output Undervoltage Falling Threshold		RT6310E/EH: V_{OUT} falling		55	60	65	%
Output Undervoltage Rising Threshold		RT6310E/EH: V_{OUT} rising		--	72	--	%
Output Undervoltage Deglitch Time		RT6310E/EH: force V_{OUT} below UVP falling threshold until LX stop switching.		--	11	--	μs
UV Blank Time		RT6310E/EH	From EN/MODE high	1.7	2.3	2.9	ms
Power Good							
Power Good Threshold		RT6310E/EH: V_{OUT} rising		87	90	93	%
Power Good Hysteresis		RT6310EH	T_A = T_J = 25°C	--	10.9	--	%
Power Good Low Deglitch Time				--	20	--	μs
LDO Regulator							
LDO Output Voltage	V_{LDO3}	RT6310E/EH	T_A = T_J = 25°C, $V_{EN/MODE}$ = 0V, no bypass	3.25	3.3	3.35	V
LDO Dropout Voltage	V_{DROP}	ILDO = 20mA, $V_{EN/MODE}$ = 0V, no bypass. (Note 6)		--	200	--	mV
LDO Output Current Limit	I_{LIM_LDO}			120	200	300	mA
LDO Bypass Switch							
LDO Bypass Switch On-Resistance	R_{BYP_LDO}	RT6310E/EH	T_A = T_J = 25°C	--	2.6	--	Ω
LDO Bypass Switch Turn-on Voltage	$V_{BYP\_LDO\_ON}$	RT6310E/EH		2.9	3.1	3.3	V
Bypass Switch Switchover Hysteresis		RT6310E/EH		0.1	0.2	0.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Bypass Switch						
VCC Bypass Switch On-Resistance	R_{BYP_VCC}	$T_A = T_J = 25°C$	--	4.4	--	Ω
VCC Bypass Switch Turn-on Voltage	$V_{BYP\_VCC\_ON}$		4.5	4.7	4.9	V
VCC Bypass Switch Switchover Hysteresis			0.1	0.2	0.3	V
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	T_{SD_HYS}	RT6310EH	--	20	--	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precautions are recommended.

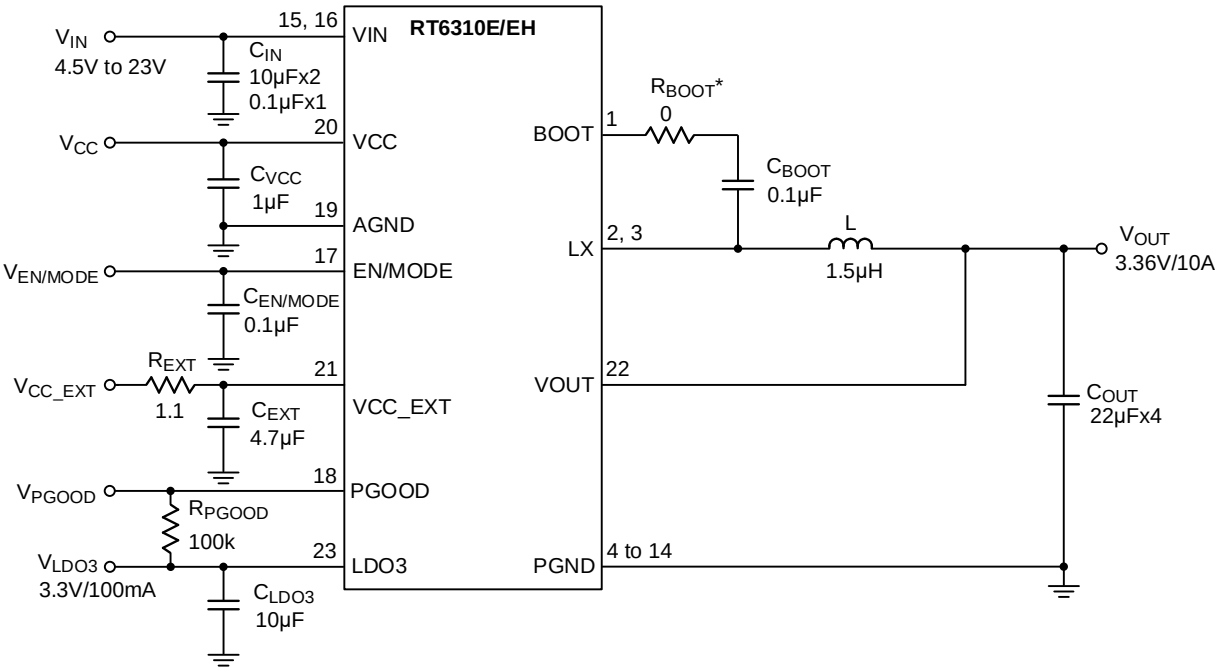
Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board (Richtek EVB) which is in size of 140mm x 90mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Note 6. Guaranteed by design.

Typical Application Circuit



R_{BOOT}* : R_{BOOT} is reserved for option. R_{BOOT} must be less than 10Ω.

Table 3. Suggested Typical Component Selections for the Application-Part I

Part Number	V_{OUT}	R1	R2	C_{FF}	L (2)	C_{LDO}	R_{EXT}	C_{EXT}
RT6310E/EH	3.36V	NA	NA	NA	1.5μH	10μF/6.3V/0603	1.1Ω/0603	4.7μF/6.3V/0603

Table 4. Suggested Typical Component Selections for the Application-Part II

Part Number	VOUT	CIN	COUT	RBOOT	CBOOT	CVCC	CEN/MODE
RT6310E/EH	3.36V	10μF/35V/0805x2 0.1μF/50V/0603x1	22μF/6.3V/0805x4	0Ω/0603	0.1μF/50V/0603	1μF/6.3V/0603	0.1μF/50V/0603

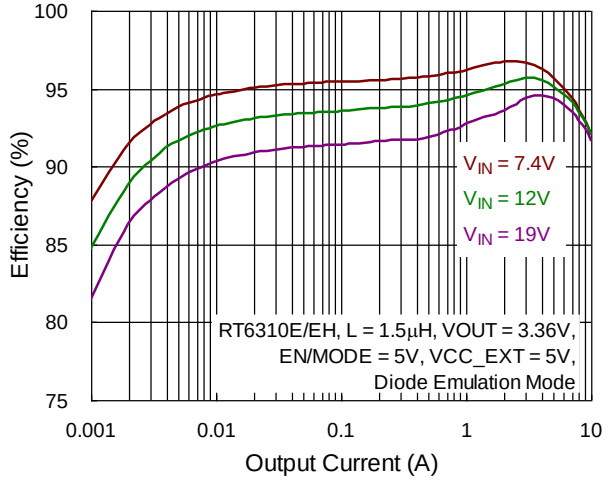
Note:

(1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

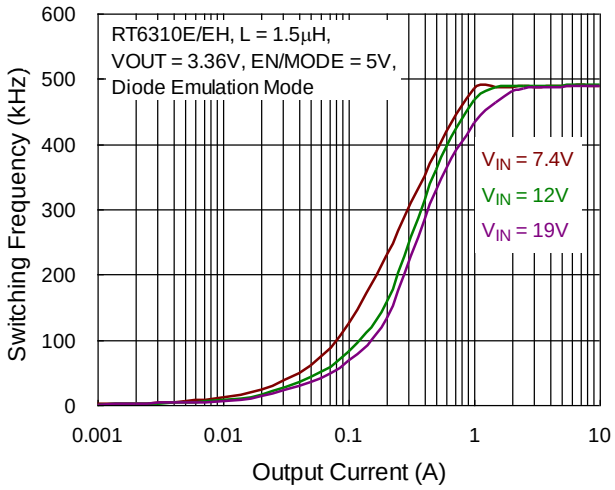
(2) PEUE063T-1R5MS: Size(mm) = 6.95 x 6.6 x 2.8, L = 1.5μH, DCR = 7.7mΩ, I_{SAT} = 14.8A

Typical Operating Characteristics

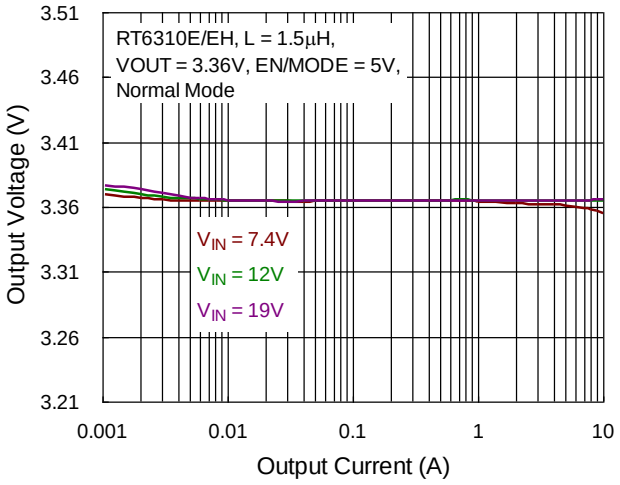
Efficiency vs. Output Current



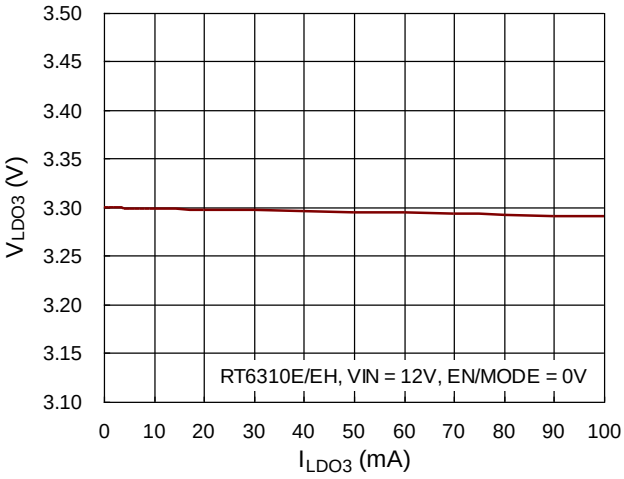
Switching Frequency vs. Output Current



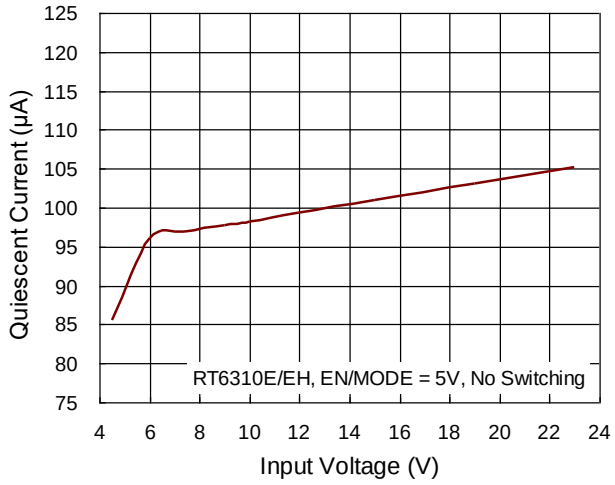
Output Voltage vs. Output Current



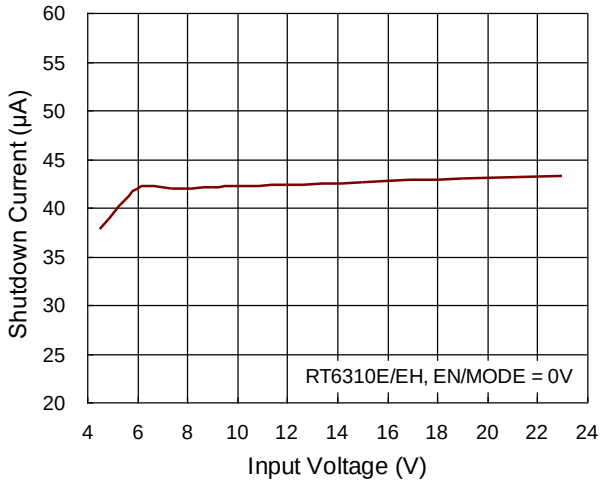
V_{LDO3} vs. I_{LDO3}



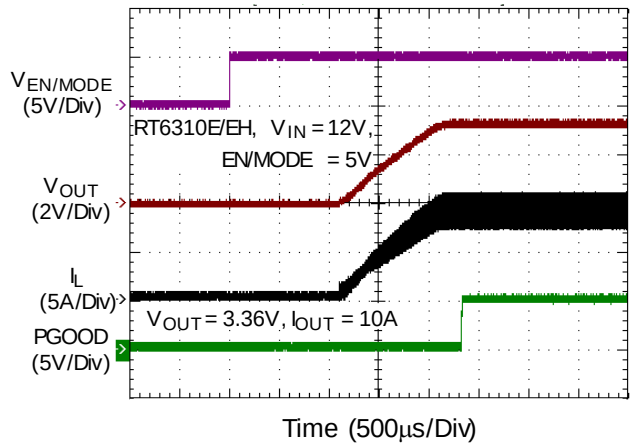
Quiescent Current vs. Input Voltage



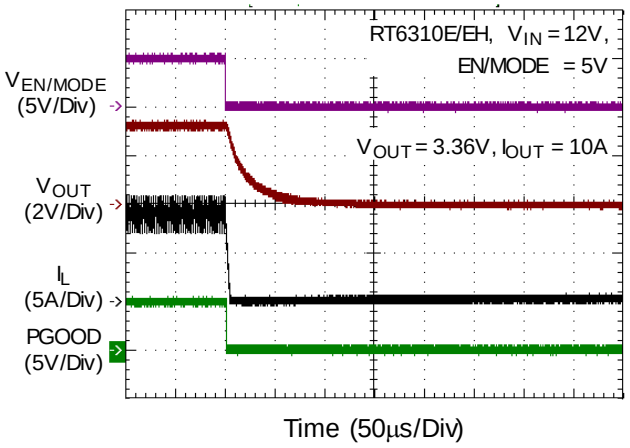
Shutdown Current vs. Input Voltage



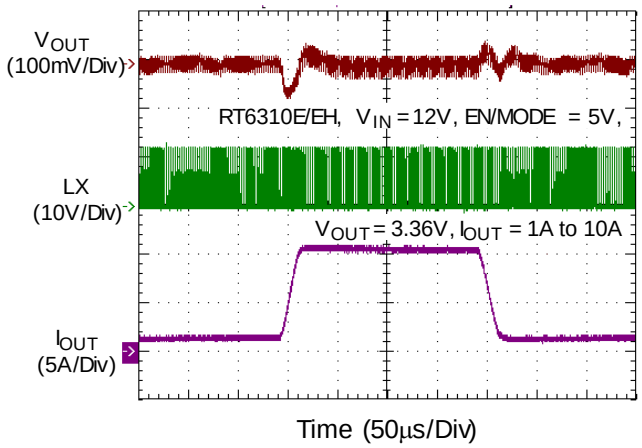
Power On from EN/MODE



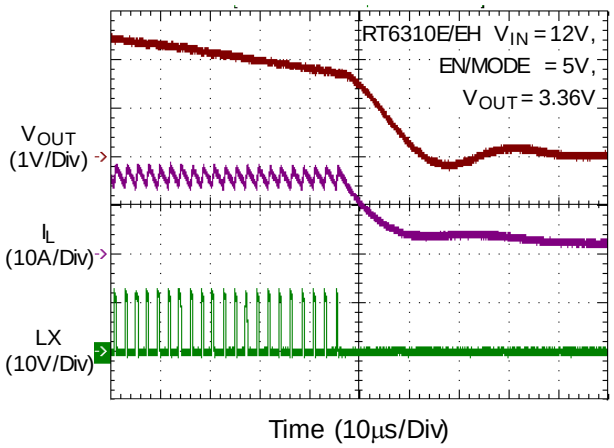
Power Off from EN/MODE



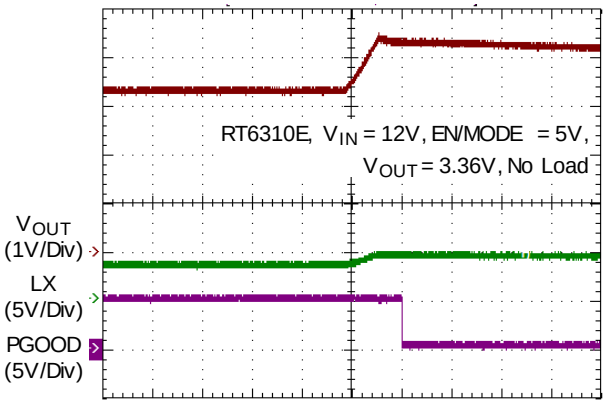
Load Transient Response



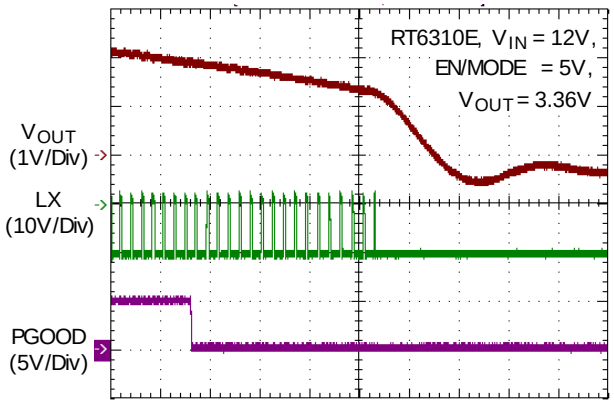
Over Current Limit



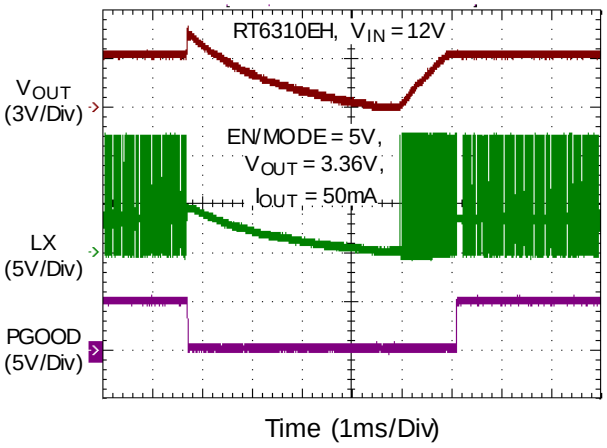
VOUT OVP with Latched Mode



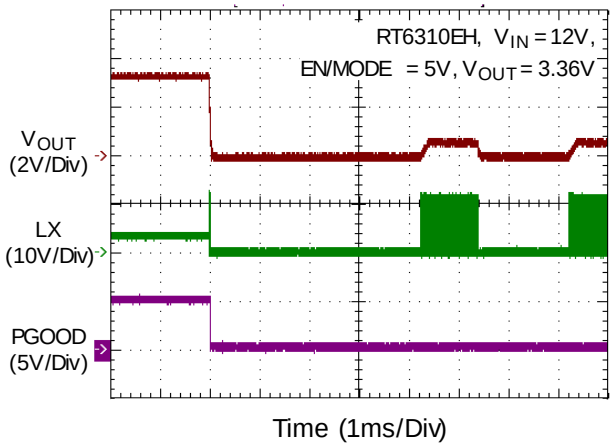
VOUT UVP with Latched Mode



VOUT OVP with Non-Latched Mode



VOUT UVP with Hiccup Mode



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

A general RT6310E/EH application circuit is shown in Typical Application Circuit section. External component selection is largely driven by the load requirement. In this section, the key external components such as the inductor L, the input capacitor C_{IN}, the output capacitor C_{OUT}, the internal regulator capacitor C_{VCC}, and the bootstrap capacitor C_{BOOT} are introduced.

Inductor Selection

The inductor selection makes trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is a 30% peak-to-peak ripple current ΔI_L to the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Larger inductance values result in lower output ripple voltage and higher efficiency, but a slightly degraded transient response. Lower inductance values allow for smaller case size, but the larger ripple current increases the AC losses in the inductor. To enhance the efficiency, choose a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The inductor value determines not only the ripple current but also the load current of boundary between DEM and CCM.

In the applications, the RT6310E/EH may encounter the events of power on inrush current (capacitive load or heavy load) and output overloading. The RT6310E/EH provides the peak and valley current-limit protections to prevent the device from damages. Moreover, to make the current-limit protection effective, a saturation current rating of the inductor must be greater than the valley current limit of the RT6310E/EH.

Input Capacitor Selection

Input capacitance (C_{IN}) is needed to filter the pulsating current at the drain of the high-side MOSFET. The large ripple voltage on VIN pin must be minimized by C_{IN}. The peak-to-peak voltage ripple on input capacitor is estimated as equation below:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times R_{ESR}$$

Where R_{ESR} is the equivalent series resistance of C_{IN} and

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple caused by ESR can be ignored, and the minimum input capacitance is estimated as equation below:

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D \times (1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

Where ΔV_{IN_MAX} = 200mV for typical application (V_{IN} > 7V)

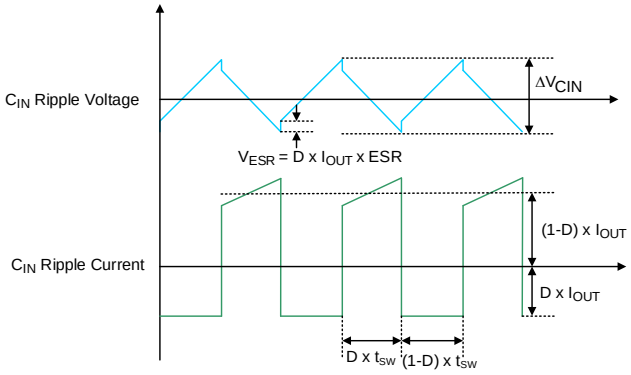


Figure 7. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of:

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. Therefore, the de-rating of capacitor is worse in actual application. Selecting higher temperature rating of capacitor is required for less de-rating.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications due to its small, robust and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality factor (under damped) tank circuit. If the RT6310E/EH circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pin, with a low inductance connection to the PGND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitors of 0.1μF should be placed close to the VIN pin. The capacitor should be 0402 or 0603 in size.

Output Capacitor Selection

The selection of C_{OUT} should satisfy the voltage ripple, the transient loads and to ensure that control loop is stable. Loop stability can be checked by viewing the load transient response. The peak-to-peak output ripple, ΔV_{OUT}, is characterized by two components, ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, are expressed as below:

$$\Delta V_{OUT} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Where the ΔI_L is the peak-to-peak inductor ripple current and R_{ESR} is the equivalent series resistance of C_{OUT}.

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Regarding to the transient loads, the V_{SAG} and V_{SOAR} requirement should be taken into consideration for choosing the output capacitance value. The amount of output sag is a function of the maximum duty factor, which is calculated from the on-time and minimum off-time.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The worst-case output sag voltage is determined by:

$$\Delta V_{OUT\_SAG} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

When the load is removed, the amount of overshoot due to stored inductor energy is calculated as:

$$\Delta V_{OUT\_SOAR} = \frac{L \times I^2_{L\_PEAK}}{2 \times C_{OUT} \times V_{OUT}}$$

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. Be careful to consider the voltage coefficient of ceramic capacitors when choosing the value and case size. Most ceramic capacitors lose 50% or more of their rated value when used near their rated voltage.

Internal V_{CC} Regulator (VCC)

Good bypassing at VCC pin is necessary to supply the high transient currents required by the MOSFET gate drivers. Place a low ESR MLCC capacitor (C = 1μF/0603) as close as possible to VCC pin and AGND pin. Applications with high input voltage and high switching frequency will increase die temperature

because of the higher power dissipation across the LDO. Do not connect VCC pin to provide power to other devices or loads.

External Bootstrap Capacitor and Resistor (C_{BOOT} and R_{BOOT})

Connect a 0.1μF/0603 low ESR ceramic capacitor and ≤ 10Ω resistor between BOOT pin and LX pin. This bootstrap capacitor provides the gate driver supply voltage for the high-side MOSFET. The internal gate driver is optimized to turn the high-side MOSFET on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. The most of EMI occurs since V_{LX} rises rapidly when the high-side MOSFET is turned on fast. In some cases, slightly increasing the R_{BOOT} reduces EMI and LX pin spike directly, but the switching loss of high-side MOSFET and die/case temperature are also increased.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a UQFN-23L 3x3 (FC) package, the thermal resistance, $\theta_{JA(EVB)}$, 30.1°C/W is measured in the natural convection at T_A = 25°C on a four-layer Richtek evaluation board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C − 25°C)/(30.1°C/W) = 3.32W for a UQFN-23L 3x3 (FC) package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The de-rating curves in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

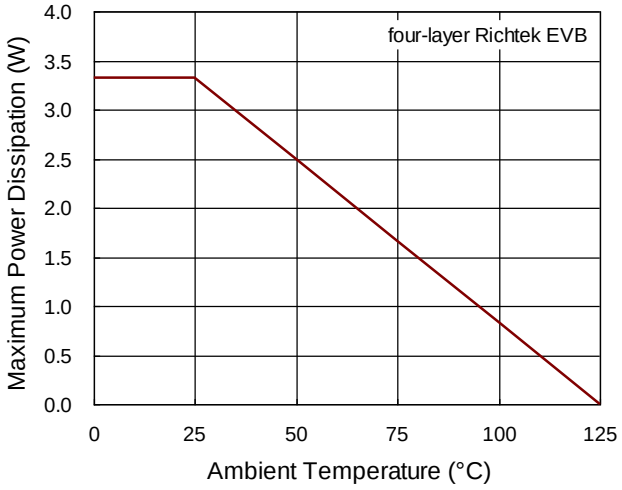


Figure 8. De-rating Curve of Maximum Power Dissipation

Layout Considerations

Printed circuit board (PCB) layout design for switch-mode power supply IC is critical and important. Improper PCB layout brings lots of problems on power supply, such as poor output voltage regulation, switching jitter, bad thermal performance, excessively radiate noise and reducing component reliability. To avoid those issues, designers have to understand current trace and signal flow in the switching power supply. The following are design considerations of PCB layout for switching power supply.

- For suppressing phase ring and extra power losses that affect device reliability, the input capacitor has to be placed close to VIN pin to reduce the influence of parasitic inductor.
- For thermal stress and power consumption considerations, the current paths of V_{IN} and V_{OUT} has to be as short and wide as possible to decrease the trace impedance.
- Since the LX node voltage swings from V_{IN} to 0V with very fast rising and falling times, switching power supply suffers quite serious EMI issues. To eliminate

EMI problems, the inductor must be put as close as possible to IC to narrow the LX node area. Besides, the LX node should be arranged in the same plate to reduce coupling noise path caused by parasitic capacitance.

- For system stability and coupling noise elimination, the sensitive components and signals, such as control signal and feedback loop, should be kept away from LX node.
- For enhancing noise immunity on VCC pin, the decoupling capacitor must be connected from VCC to AGND, and the capacitor should be placed close to IC.
- The feedback signal path from V_{OUT} to IC should be wide and kept away from high switching path.
- The trace width and numbers of via should be designed based on application current. Make sure the switching power supply has great thermal performance and good efficiency.

An example of PCB layout guides are shown in Figure 9 for reference.

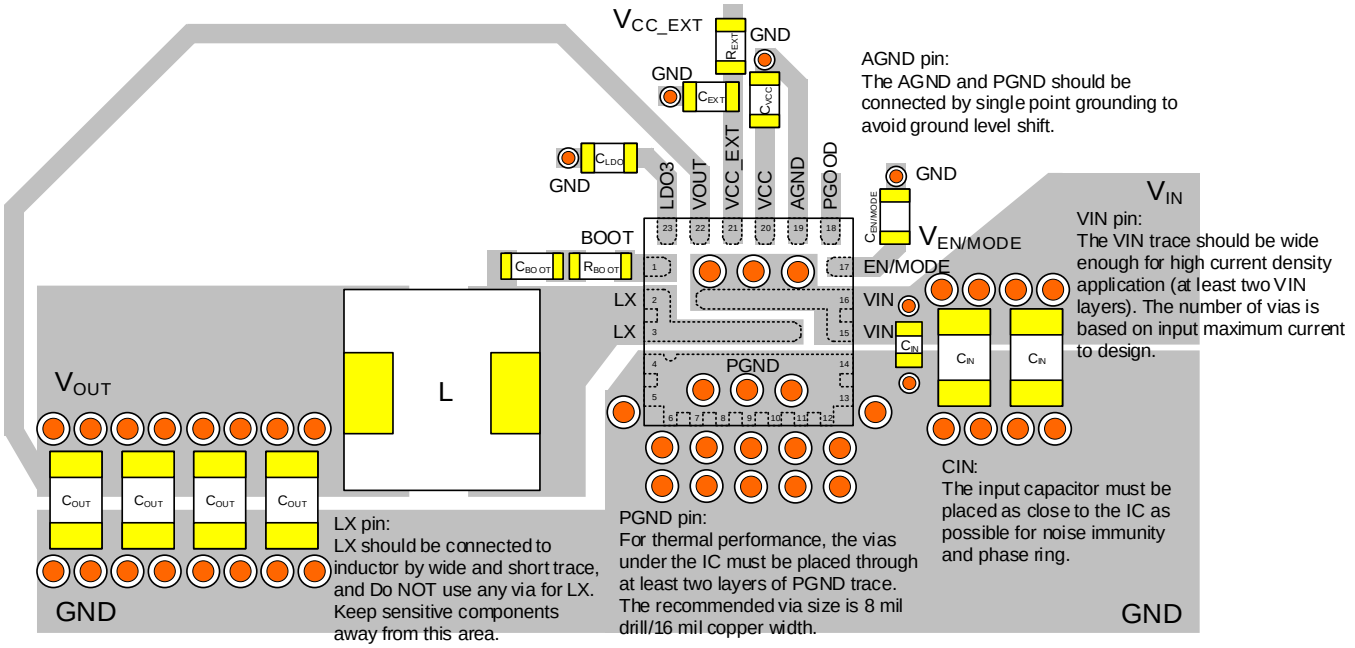


Figure 9. RT6310E/EH Layout Guide

Thermal Performance

A good PCB design has the optimized thermal performance and efficiency. Under the ambient temperature 25°C, and specified BOM list (refer to Table 3 and Table 4) and Richtek evaluation board, the thermal images of RT6310E/EH are shown in Figure 10.

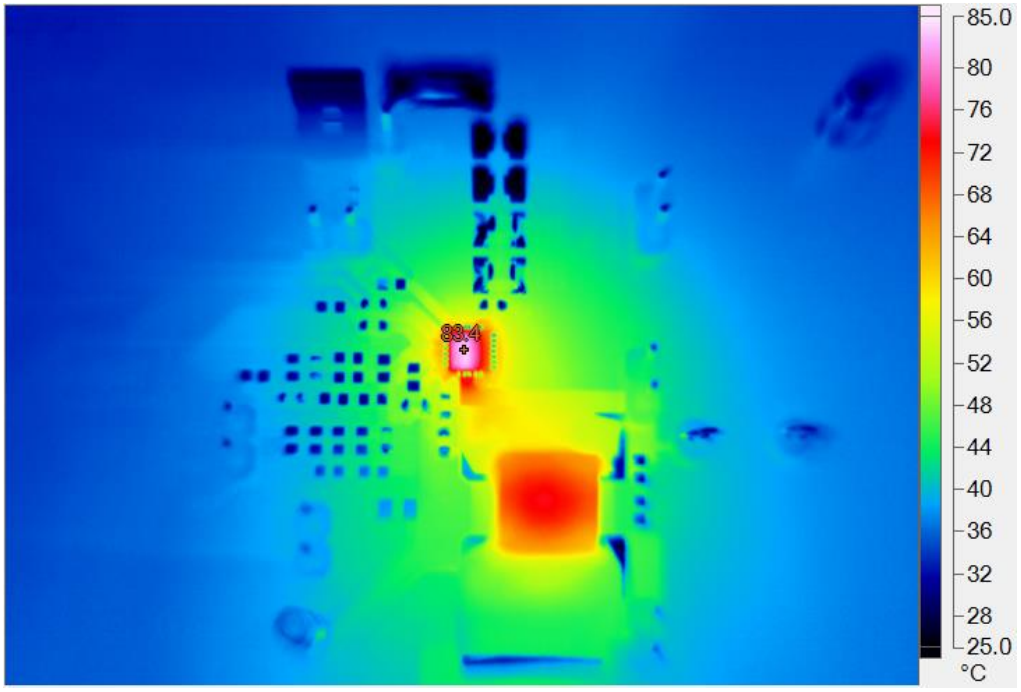
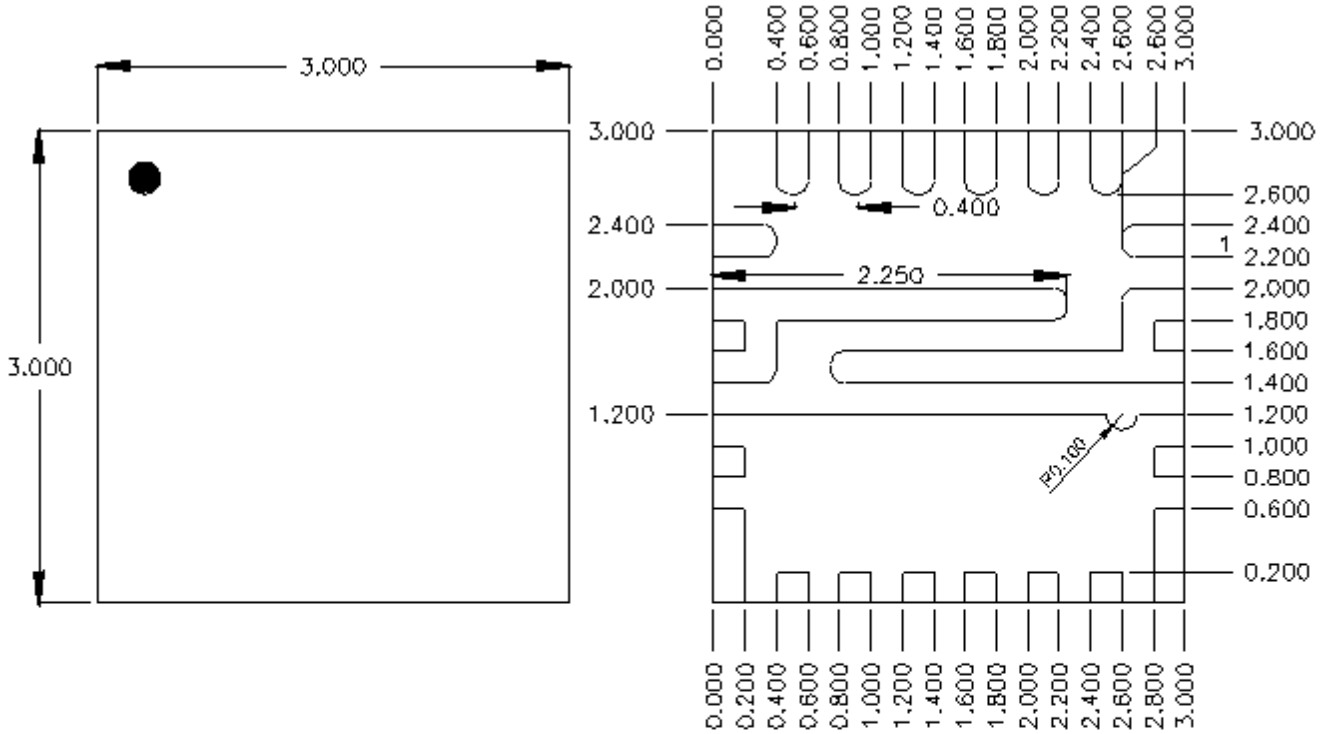
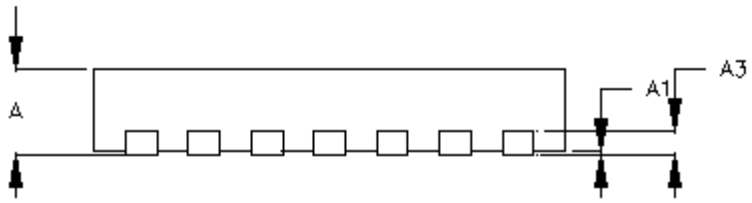


Figure 10. Thermal image of RT6310E/EH with V_{OUT} = 3.36V, V_{IN} = 19V, I_{OUT} = 10A and V_{CC_EXT} = 5V

Outline Dimension



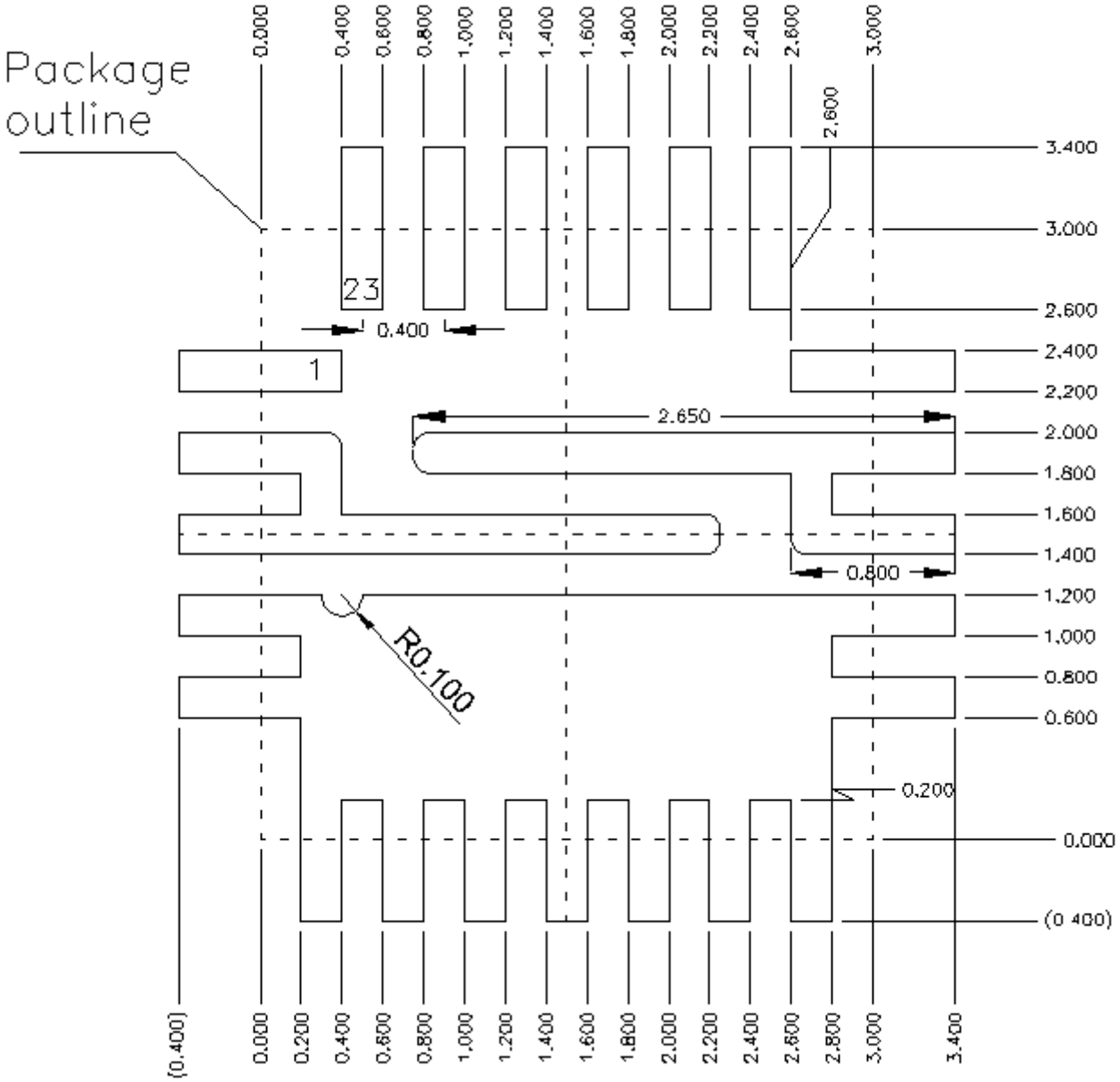


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008

Tolerance
±0.050

U-Type 23L QFN 3x3 (FC) Package

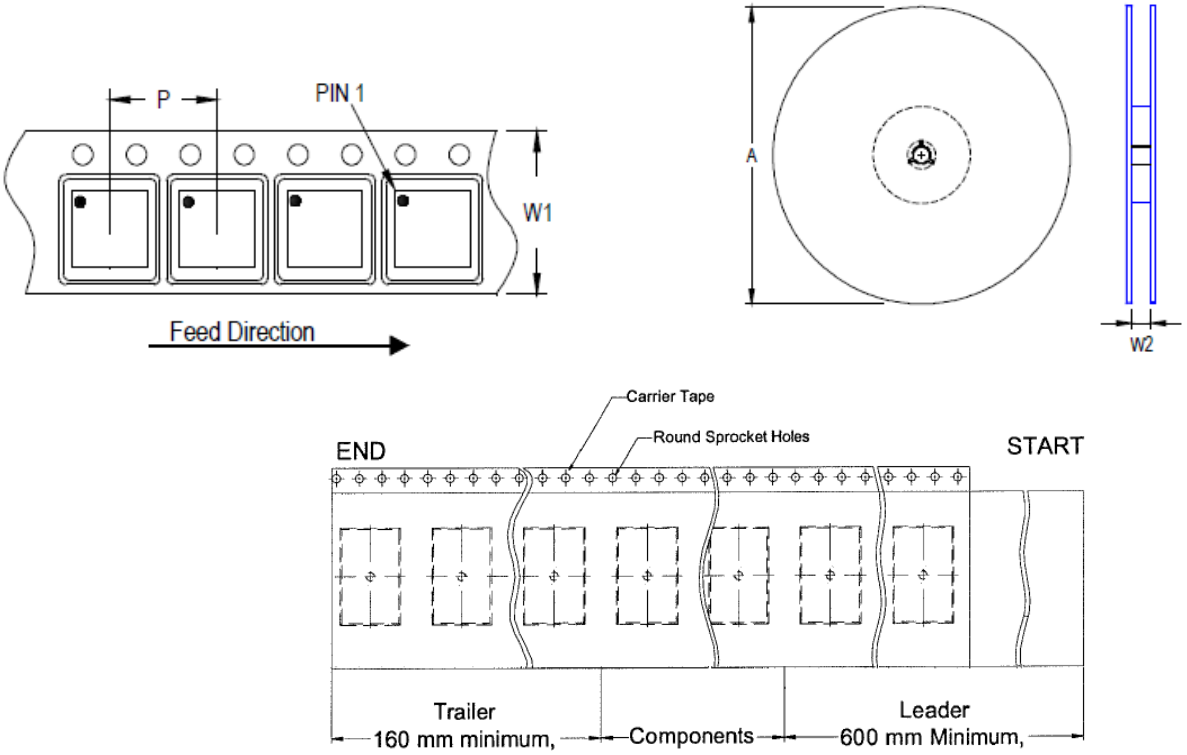
Footprint Information



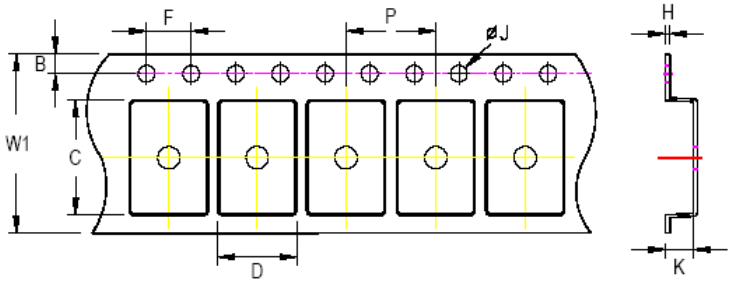
Package	Number of Pin	Tolerance
V/W/U/XQFN3x3-23(FC)	23	±0.05

Packing Information

Tape and Reel Data



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm

Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box				Carton			
	Size	Units	Item	Size(cm)	Reels	Units	Item	Size(cm)	Boxes	Unit
QFN & DFN 3x3	7”	1,500	Box A	18.3*18.3*8.0	3	4,500	Carton A	38.3*27.2*38.3	12	54,000
			Box E	18.6*18.6*3.5	1	1,500	For Combined or Partial Reel.			

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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Datasheet Revision History

Version	Date	Description	Item
00	2023/4/21	Final	