RICHTEK®

RT6250A/RT6250B

18V, 10A, 500kHz ACOT® Synchronous Buck Converter

1 General Description

The RT6250A/RT6250B is a simple, easy-to-use, 10A synchronous Buck converter with an input supply voltage range of 4.5V to 18V. The device builds in an accurate 0.6V reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in a UQFN-12HL 3x3 package. The RT6250A/RT6250B adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate at nearly constant switching frequency over the line, load, and output voltage range. The RT6250A/RT6250B operates in automatic PSM that maintains high efficiency during light load operation. The RT6250A/RT6250B operates in Forced PWM that helps meet tight voltage regulation accuracy requirements. The RT6250A/RT6250B senses both MOSFETs current for a robust overcurrent protection. It features cycle-by-cycle current-limit protection and prevent the device from the catastrophic damage in output short circuit, overcurrent or inductor saturation. A built-in soft-start function prevents inrush current during start-up. The device also includes input undervoltage-lockout, output undervoltage protection, overvoltage protection, and over-temperature protection to provide safe and smooth operation in all operating conditions. The RT6250A/RT6250B is offered in a UQFN-12HL 3x3 (FC) package. The recommended junction temperature range is –40°C to 125°C, and the ambient temperature range is –40°C to 85°C.

2 Features

- **10A Converter with Built-In 20mΩ/10mΩ Low $R_{DS(ON)}$ Power MOSFETs**
- **Input Supply Voltage Range: 4.5V to 18V**
- **Output Voltage Range: 0.6V to 6V**
- **Advanced Constant On-Time (ACOT®) Control**
  - **Ultrafast Transient Response**
  - **No Needs for External Compensations**
  - **Optimized for Low-ESR Ceramic Output Capacitors**
- **0.6V ±1% High-Accuracy Feedback Reference Voltage**
- **Optional for Operation Modes:**
  - **Power Saving Mode (PSM) (RT6250A)**
  - **Forced PWM Mode (RT6250B)**
- **Fixed Switching Frequency: 500kHz**
- **Built-In Internally Fixed Soft-Start (Typical 0.4ms)**
- **Input Undervoltage-Lockout (UVLO)**
- **Output Undervoltage Protection (UVP) with Hiccup Mode**
- **Output Overvoltage Protection (OVP) with Auto-Recovery Mode**
- **Ultrasonic Mode (USM)**
- **Available In UQFN-12HL 3x3 (FC) (U-Type) Package**

3 Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs
- Networking Communication

4 Ordering Information

RT6250A/B □□□

Package Type(1)
QUF : UQFN-12HL 3x3 (FC) (U-Type)

Lead Plating System
G: Richtek Green Policy Compliant(2)

UVP Option
H : Hiccup

Operation Mode
A : PSM/PWM
B : Force-PWM

Note 1.

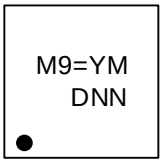
- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

5 Marking Information

RT6250AHGQUF

MA= : Product Code
YMDNN : Date Code

RT6250BHGQUF



M9= : Product Code
YMDNN : Date Code

6 Simplified Application Circuit

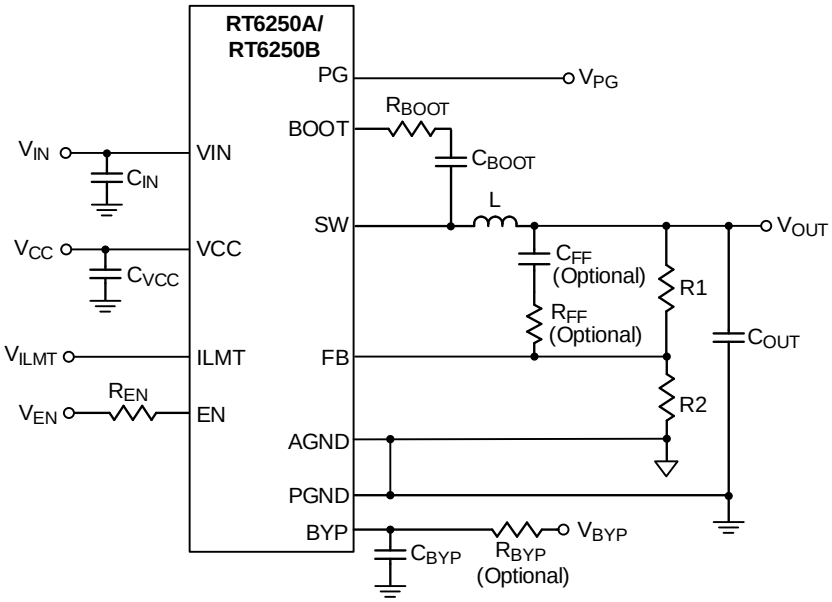
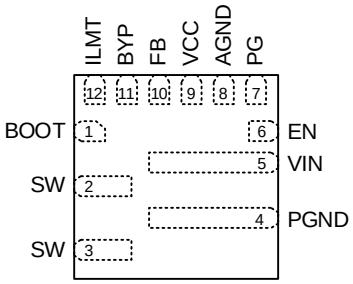


Table of Contents

7 Pin Configuration

(TOP VIEW)

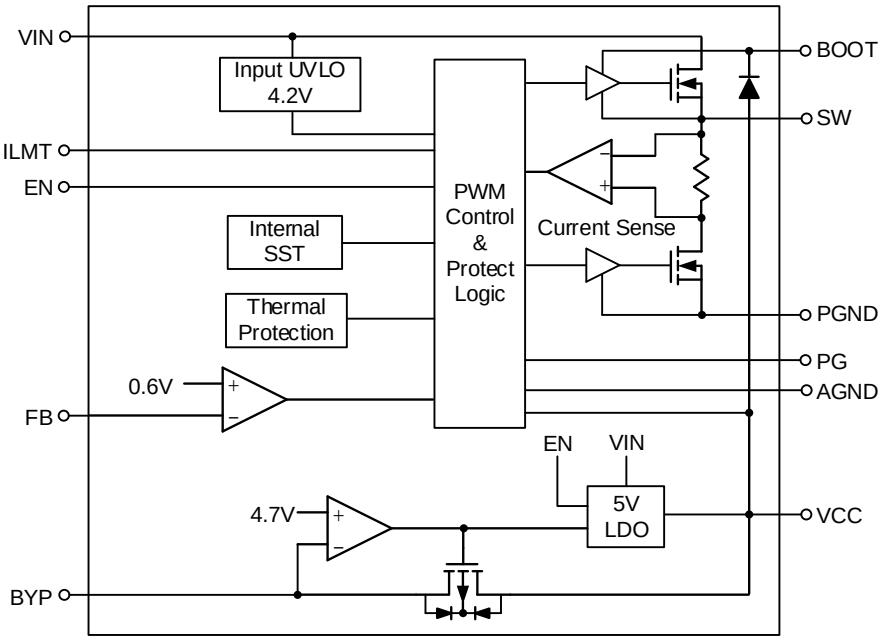


UQFN-12HL 3x3

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Boot-strap pin. Supply the high-side gate driver. Decouple this pin to the SW pin with a 0.1μF ceramic capacitor.
2, 3	SW	Inductor pin. Connect this pin to the switching node of inductor.
4	PGND	Power ground.
5	VIN	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
6	EN	Enable control. Pull this pin high to turn on the buck converter. Do not leave this pin floating. The EN pin will also be used to set the USM mode, when the EN pin voltage is between 2.3V and 18V, it will enter USM mode, if the EN pin voltage is between 0.8V and 1.7V, then it is normal mode.
7	PG	Power-good indicator. Open drain output when the output voltage is within 90% to 120% of the regulation point.
8	AGND	Analog ground. Connect AGND to a clean inner GND point with a separate trace.
9	VCC	5V linear regulator output for the internal control circuit. A capacitor (typically 1μF) should be connected to PGND. Do not connect to an external Load.
10	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
11	BYP	Bypass input for the internal LDO. BYP is externally connected to the output of the switching regulator. When the BYP voltage rises above the bypass switch turn-on threshold, the LDO regulator shuts down and the VCC pin is connected to the BYP pin through an internal switch. If the BYP pin is not used, it should be connected to ground.
12	ILMT	Current limit setting pin. The current limit is set to 8A, 10A, or 12A when this pin is pulled low, floating, or pulled high, respectively.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- Supply Voltage, VIN ---------- –0.3V to 20V
- Enable Pin Voltage, EN ---------- –0.3V to 20V
- FB Pin Voltage, FB ---------- –0.3V to 4.5V
- Switch Voltage, SW ----------–0.3V to (V_{IN} + 0.3V)
  <30ns ---------- –5V to 21V
- Boot Voltage, VBS ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  UQFN-12HL 3x3 (FC)---------- 2.9W
- Package Thermal Resistance (Note 3)
  UQFN-12HL 3x3 (FC), θ_{JA} ---------- 34.3°C/W
  UQFN-12HL 3x3 (FC), Ψ_{JC} ---------- 0.21°C/W
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Junction Temperature---------- 150°C
- Storage Temperature Range---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Richtek Evaluation Board. Ψ_{JC} is measured at the top of the package.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- Supply Input Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range---------- –40°C to 125°C
- Ambient Temperature Range---------- –40°C to 85°C

Note 5. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5	--	18	V
Supply Current						
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0	--	5	10	μA
Supply Current (Quiescent)	I_Q	I_{OUT} = 0, V_{FB} = V_{REF} x 105%	--	130	--	μA
Logic Threshold						
EN Input Voltage Falling Threshold	V_{EN_F}		0.4	0.54	0.68	V
EN Input Voltage Rising Threshold	V_{EN_R}		0.45	0.625	0.8	V
Ultrasonic Mode	V_{EN}		2.3	--	--	V
Normal Mode	V_{EN_NOR}		--	--	1.7	V
Output Voltage						
VCC Regulator Voltage	V_{CC}		--	5	--	V
Feedback Voltage						
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
Feedback Current	I_{FB}	V_{FB} = 4V	–50	--	50	nA
On Resistance						
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$		--	20	--	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$		--	10	--	mΩ
Discharge FET Ron	R_{DISCHG}		--	50	--	Ω
Current Limit						
Bottom FET Current Limit	I_{LIM}	I_{LMT} = ”0”	8	--	--	A
		I_{LMT} = Floating	10	--	--	
		I_{LMT} = ”1”	12	--	--	
ILMT Rising Threshold	V_{ILMTH}		VCC – 0.8	--	VCC	V
ILMT Falling Threshold	V_{ILMTL}		--	--	0.8	V
Oscillator Frequency						
Oscillator Frequency	f_{OSC}		--	0.5	--	MHz
On-Time Timer Control						
Minimum On-Time	t_{ON_MIN}	V_{IN} = $V_{IN(MAX)}$	--	50	--	ns
Minimum Off-Time	t_{OFF_MIN}		--	400	--	ns
Ultrasonic Mode						
Operation Period	t_{USM}		20	30	40	μs
Soft-Start						
Power Good Enable Delay Time		From EN high to PG high	1.3	1.65	2	ms
Soft-Start Time	t_{SS}	From 10% to 90% VOUT	--	0.4	--	ms

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVLO						
Input UVLO Threshold	V_{UVLO}	Wake up	--	--	4.4	V
UVLO Hysteresis	V_{UVLO_HYS}		--	0.3	--	V
Output Overvoltage Protection						
Output Overvoltage Threshold		V_{OUT} rising	115	120	125	%
Output Overvoltage Hysteresis			--	3	--	%
Output Overvoltage Delay Time			--	20	--	μs
Output Undervoltage Protection						
Output Undervoltage Threshold		V_{FB} falling	--	60	--	%
Output Undervoltage Delay Time		FB forced below UV threshold	--	20	--	μs
UV Blank Time		From EN high	--	1.65	--	ms
Power-Good Indicator						
Power-Good Threshold		V_{OUT} rising (Good)	88	90	92	%
Power-Good Hysteresis			--	15	--	%
Power-Good Delay Time			--	10	--	μs
Bypass Switch						
Bypass Switch RON	R_{BYP}		--	3	--	Ω
Bypass Switch Turn-On Voltage	V_{BYP_ON}		--	4.7	--	V
Bypass Switch Switchover Hysteresis			--	0.2	--	V
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	15	--	°C

14 Typical Application Circuit

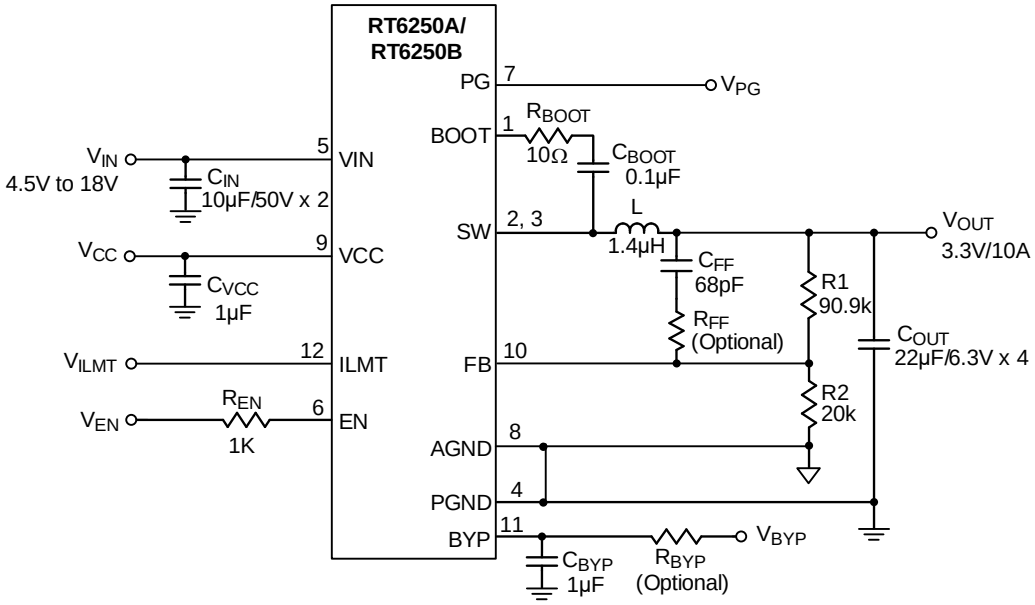


Table 1. Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)	C_{FF} (pF)
1	13.3	20	0.68	22x4/0805/6.3V	82
1.2	20	20	0.68	22x4/0805/6.3V	82
1.8	40.2	20	1	22x4/0805/6.3V	82
2	46.6	20	1.5	22x4/0805/6.3V	82
3.3	90.9	20	1.5	22x4/0805/6.3V	68
5	147	20	2.2	22x4/0805/6.3V	68

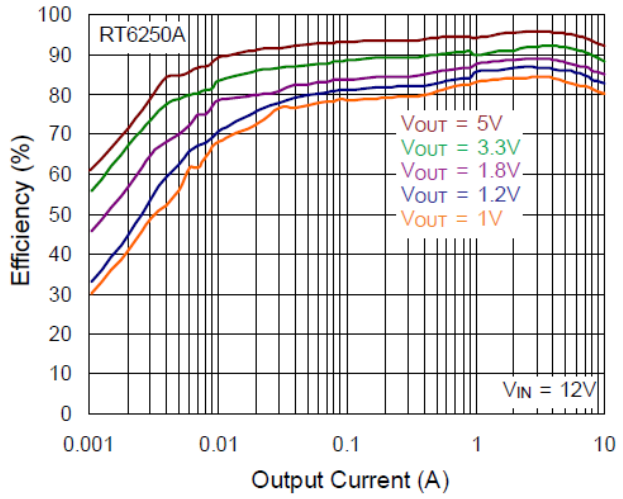
Table 2. USM Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)	C_{FF} (pF)
1	13.3	20	1	22x4/0805/6.3V	100
1.2	20	20	1	22x4/0805/6.3V	100
1.8	40.2	20	1	22x4/0805/6.3V	100
2	46.6	20	2.2	22x4/0805/6.3V	100
3.3	90.9	20	2.2	22x4/0805/6.3V	100
5	147	20	2.2	22x4/0805/6.3V	100

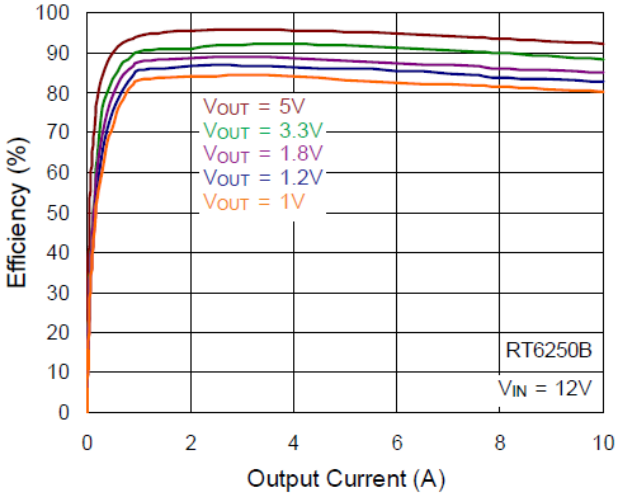
Note 6. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

15 Typical Operating Characteristics

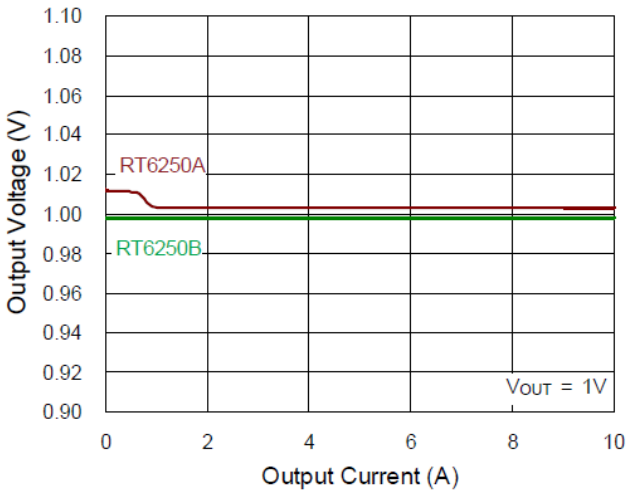
Efficiency vs. Output Current



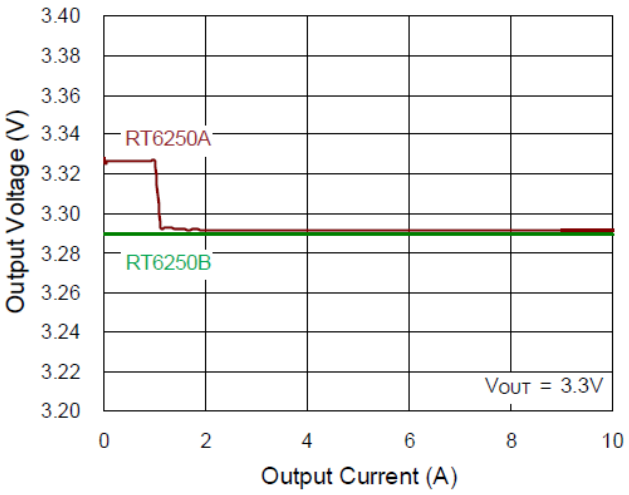
Efficiency vs. Output Current



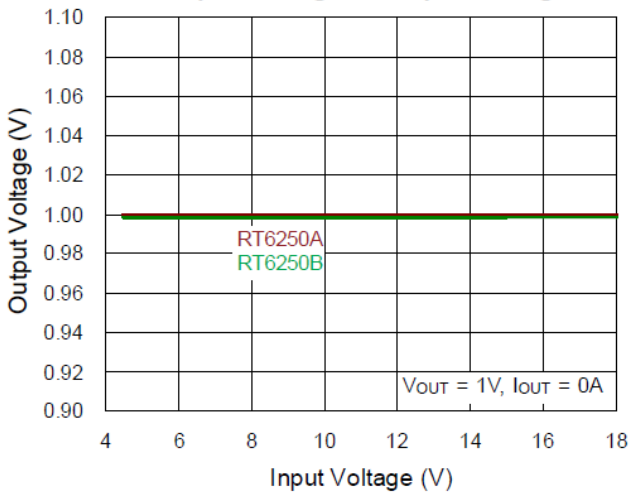
Output Voltage vs. Output Current



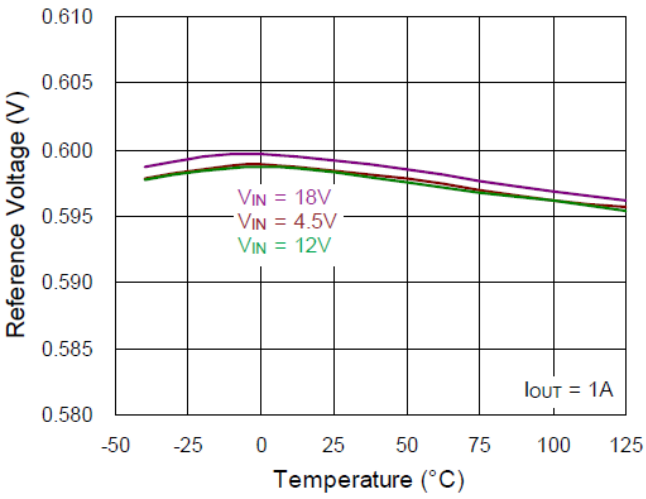
Output Voltage vs. Output Current



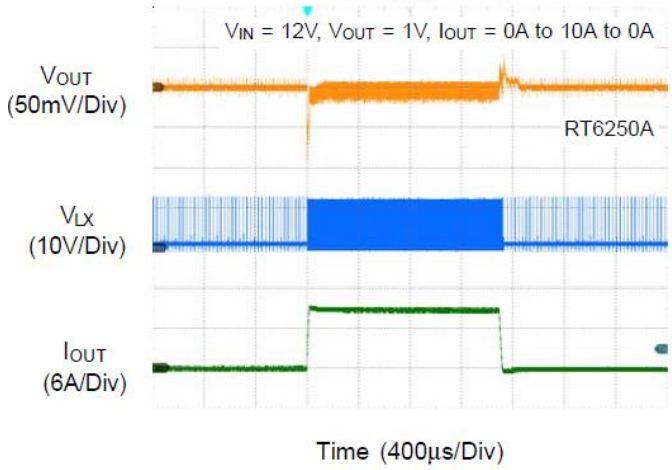
Output Voltage vs. Input Voltage



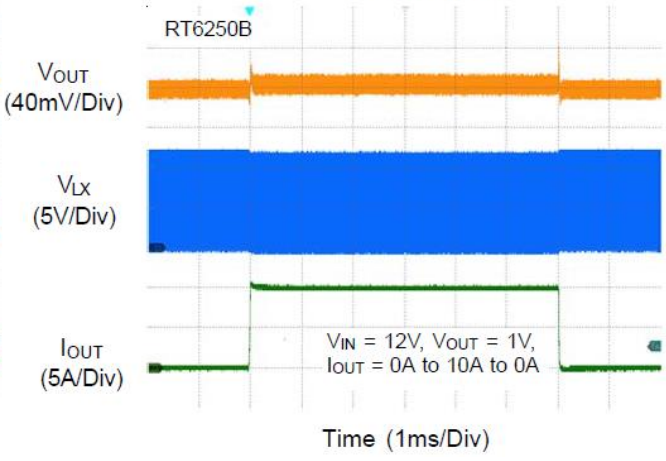
Reference Voltage vs. Temperature



Load Transient



Load Transient



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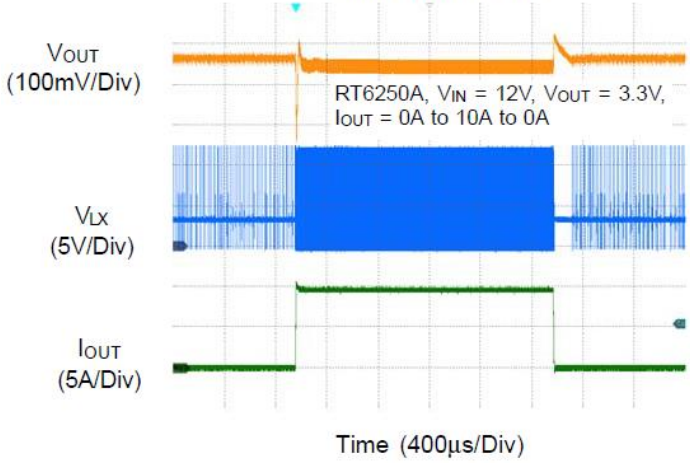
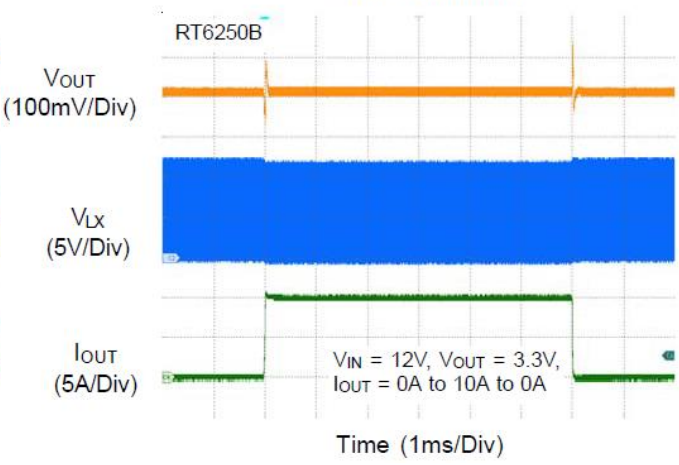


Load Transient



16 Operations

The RT6250A/RT6250B is a high-efficiency, synchronous buck converter that can deliver up to 10A output current from a 4.5V to 18V input supply. The RT6250A/RT6250B adopts the ACOT® control mode, which can reduce the output capacitance, provide ultrafast transient responses, and allow for minimal component sizes without any additional external compensation network.

16.1 Input Undervoltage-Lockout

In addition to the EN pin, the RT6250A/RT6250B also provides enable control through the VIN pin. It features an undervoltage-lockout (UVLO) function that monitors the internal linear regulator (VCC). If V_{EN} rises above V_{ENH} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It ensures that the internal regulator is ready, preventing operation with not-fully-enhanced internal MOSFET switches. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume switching.

16.2 Soft-Start

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RT6250A/RT6250B provides an internal soft-start feature for inrush control. During the start-up sequence, the internal capacitor is charged by an internal current source ISS to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up. The typical soft-start time is 0.4ms.

16.3 Current-Limit Protection

The RT6250A/RT6250B current limit is (8A, 10A, 12A) it is a cycle-by-cycle “valley” type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. If the output voltage drops below the output undervoltage protection level, the RT6250A/RT6250B will stop switching to avoid excessive heat.

16.4 Output Overvoltage Protection (OVP) and Undervoltage Protection (UVP)

The RT6250A/RT6250B includes output undervoltage protection (UVP) against overload or short-circuited conditions by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection trip threshold (typically 60% of the internal reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

16.5 Power-Good Indicator

The PG pin is an open-drain output and is connected to an external pull-up resistor. It is controlled by a comparator, which the feedback signal V_{FB} is fed to. If V_{FB} is above 90% of the internal reference voltage, the PG pin will be in high impedance and V_{PG} will be held high. Otherwise, the PG output will be pulled low.

16.6 Over-Temperature Protection

The RT6250A/RT6250B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds an over-temperature protection threshold T_{OTP}. Once the junction temperature cools down by an over-temperature protection hysteresis (ΔT_{OTP}), the IC will resume normal operation with a complete soft-start.

17 Application Information

(Note 7)

The RT6250A/RT6250B is high-performance 10A buck regulators with internal power switches and synchronous rectifiers. It features an Advanced Constant On-Time (ACOT®) control architecture that provides stable operation for ceramic output capacitors without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 18V. The output voltage is adjustable from 0.6V to 6V.

The proprietary ACOT® control scheme improves conventional constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, the response to transients is nearly instantaneous and the inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

17.1 ACOT® Control Architecture

The conventional CFCOT (constant frequency constant on-time) control, which makes the on-time proportional to VOUT and inversely proportional to VIN is not sufficient to achieve good constant-frequency behavior. This is because voltage drops across the MOSFET switches and the inductor cause sensing mismatches when sensing input and output voltage from the SW pin. When the load changes, the voltage drops across the MOSFET switches and the inductor cause a switching frequency variation with load current. One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT® uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range. To achieve good stability with low-ESR ceramic capacitors, ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

17.2 ACOT® One-Shot Operation

The RT6250A/RT6250B control algorithm is simple to understand. The feedback voltage, combined with the virtual inductor current ramp, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered if the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time period, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (400ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

17.3 Diode Emulation Mode (DEM)

In diode emulation mode, the RT6250A/RT6250B automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. As the output current decreases from a heavy load condition, the inductor current is also reduced, and eventually comes to the point that its current valley touches zero, which is the boundary between continuous conduction and discontinuous conduction modes. To emulate the behavior of diodes, the low-side MOSFET allows only partial negative current to flow when the inductor freewheeling current becomes negative. As the load current further decreases, it takes longer to discharge the output capacitor to the level that requires the next “ON” cycle. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the

inductor current reaches the continuous conduction. The transition load point to the light load operation is shown in Figure 1 and can be calculated as follows:

$$I_{LOAD} = \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the on-time.

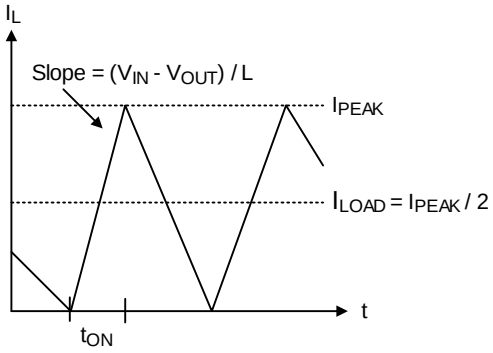


Figure 1. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when a light load causes diode emulation operation. This is normal and results in high efficiency. Trade-offs in DEM noise versus light load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency versus load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load transient response (especially at low input voltage levels).

At the boundary condition between discontinuous switching and continuous switching, the on-time is immediately increased to add “hysteresis” to discourage the IC from discontinuous switching back to continuous switching unless the load increases substantially. The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for the designed switching frequency, encouraging the circuit to remain in continuous conduction, and preventing repetitive mode transitions between continuous switching and discontinuous switching.

17.4 Ultrasonic Mode (USM)

The RT6250A/RT6250B activates a unique type of diode emulation mode with a minimum switching period of 30μs (typical), called ultrasonic mode. This mode eliminates audio-frequency modulation that will otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low-side switch gate driver signal is “OR”ed with an internal oscillator (>33kHz). Once the internal oscillator is triggered, the controller will turn on UGATE and give it a shorter on-time. When the on-time expires, LGATE turns on until the inductor current goes to zero crossing threshold and keep both high-side and low-side MOSFETs off to wait for the next trigger. Because the shorter on-time causes a smaller pulse of the inductor current, the controller can keep the output voltage and switching frequency simultaneously. The on-time decrease has a limitation and the output voltage will be lifted under the light load conditions. The controller will turn on LGATE first to pull down the output voltage. When the output voltage is pulled down to the balance point of the output load current, the controller will proceed with the short on-time sequence as described above. Ultrasonic mode is selected by the EN voltage level. When EN is above 2.3V, it enters ultrasonic mode. If EN is in the range of 0.8V to 1.7V, it enters normal mode. If using the ultrasonic mode, The Richtek-provided BOM must be used.

17.5 On-Time Reduction Function for DEM

In normal diode emulation mode, the output voltage ripple of the converter is proportional to the on-time and inversely proportional to the load current. To have smaller voltage ripple in light load applications, the RT6250A/RT6250B provides a smart reduction on-time function, which will follow decreased load current to decrease on-time naturally, therefore the output voltage ripple can be reduced effectively.

17.6 Linear Regulators (VCC)

The RT6250A/RT6250B also includes a 5V linear regulator (VCC). The VCC regulator steps down the input voltage to supply both internal circuitry and gate drivers. Do not connect the VCC pin to external loads.

17.7 Bypass Function for VCC

When PG is pulled high and the BYP pin voltage of the RT6250A/RT6250B is above 4.7V, an internal 3Ω P-MOSFET switch connects VCC to the BYP pin while the VCC linear regulator is simultaneously turned off. Since the VCC is power source for internal logic devices and gate drivers, it is recommended to place an RC filter on the BYP pin to enhance power quality for the IC internal power when the bypass function is enabled. If the BYP pin is not used, it should be connected to ground.

17.8 Current Limit

The RT6250A/RT6250B current limit is adjustable (8A,10A,12A) by the ILMT pin and it is a cycle-by-cycle “valley” type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between source and drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the current limit, the on-time one-shot is inhibited until the inductor current ramps down below the current limit. Thus, only when the inductor current is well below the current limit, another on-time is permitted. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output undervoltage protection level (see Output Overvoltage Protection and Undervoltage Protection), the IC will stop switching to avoid excessive heat.

17.9 Output Overvoltage Protection and Undervoltage Protection

The RT6250A/RT6250B includes output overvoltage protection (OVP). If the output voltage rises above the regulation level, the high-side switch naturally remains off and the synchronous rectifier will turn on until the inductor current reaches zero or the next on-time one-shot is triggered. If the output voltage exceeds the OVP threshold for longer than 20μs (typical), the IC's OVP is triggered. The RT6250A/RT6250B also includes output undervoltage protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 20μs (typical), the IC's UVP is triggered. The RT6250A/RT6250B uses auto-recovery mode in OVP and Hiccup Mode in UVP. When the UVP function is triggered remains for a period, the RT6250A/RT6250B will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during the soft-start period. If the OVP function is triggered, the IC will stops switching. When the OVP condition is removed, the converter will resume operation.

17.10 Input Undervoltage-Lockout

In addition to the enable function, the RT6250A/RT6250B provides an Undervoltage-Lockout (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when the input voltage drops below the UVLO-falling threshold. The IC resumes switching when the input voltage exceeds the UVLO-rising threshold.

17.11 Enable and Disable

The RT6250A/RT6250B's EN is used to control the converter. The enable voltage (EN) has a logic-low level of 0.4V. When VEN is below this level, the IC enters shutdown mode. When VEN exceeds its logic-high level of 0.8V, the converter is fully operational.

17.12 Soft-Start

The RT6250A/RT6250B provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the IC is enabled. During soft-start, it clamps the ramping of the internal reference voltage, which is compared with the FB signal. The typical soft-start duration is 0.4ms. A unique PWM duty limit control, designed specifically for FB floating, prevents output overvoltage during the soft-start period.

17.13 Power-Good Output (PG)

The power-good output is an open-drain output that requires a pull-up resistor. When the output voltage is 15% (typical) below its set voltage, PG will be pulled low. It is held low until the output voltage returns to 90% of its set voltage. During soft-start, PG is actively held low and is only allowed to be pulled high after the soft-start is over and the output reaches 90% of its set voltage. There is a 10μs delay built into the PG circuitry to prevent false transitions.

17.14 External Bootstrap Capacitor (C_{BOOT})

Connect a 0.1μF low ESR ceramic capacitor between the BOOT pin and the SW pin. This bootstrap capacitor provides the gate driver supply voltage for the high side N-channel MOSFET switch.

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. In some cases, it is desirable to reduce EMI further at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small ($10\Omega \le R_{BOOT} \le 30\Omega$) resistor between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{SW}'s rise, improving EMI performance and enhancing of the internal MOSFET switch.

17.15 Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation:

$$V_{OUT,VALLEY} = \left(1+\frac{R1}{R2}\right)\times 0.6V$$

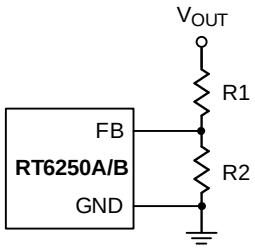


Figure 2. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows:

$$R1 = \frac{R2 \times (V_{OUT} - 0.6V)}{0.6V}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

17.16 Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required. Transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$), and estimating ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and}$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output undervoltage shutdown feature makes this unnecessary for most applications. For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses, some type of ferrite core is usually best, and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

17.17 Input Capacitor Selection

High-quality ceramic input decoupling capacitor, such as X5R or X7R, with values greater than 20μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and more temperature stability. Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design. The input capacitor is used to supply the input RMS current, which can be calculated using the following equation:

$$I_{RMS} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left[\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}^2 + \frac{\Delta I_L^2}{12} \right]}$$

The next step is to select a proper capacitor for RMS current rating. One good design uses more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation:

$$\Delta V_{IN} = \frac{I_{OUT} \times V_{IN}}{C_{IN} \times f_{SW} \times V_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The typical operating circuit is recommended to use two 10μF low ESR ceramic capacitors on the input.

17.18 Output Capacitor Selection

The IC is optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps). Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$
$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$
$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick, and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's switching frequency.

However, some modern digital loads can exhibit nearly instantaneous load changes, and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increases compensations for the voltage losses. Calculate the output voltage SAG as:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive SOAR is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Most applications never experience instantaneous full load steps, and the IC's high switching frequency and fast transient response can easily control voltage regulation at all times. Therefore, sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, it should calculate soar and sag to make sure that overvoltage protection and undervoltage protection will not be triggered.

17.19 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a UQFN-12HL 3x3 (FC) package, the thermal resistance, θ_{JA}, is 34.3°C/W on a standard JEDEC 51-7 high effective-thermal conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (125°C – 25°C) / (34.3°C /W) = 2.9W for a UQFN-12HL 3x3 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

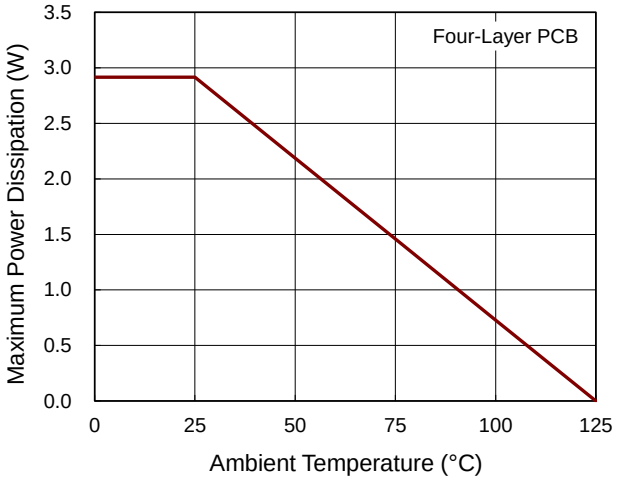


Figure 3. Derating Curve of Maximum Power Dissipation

17.20 Layout Considerations

Proper Layout is very important in high-frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

Certain points must be considered before starting a layout using the IC.

- Make traces of the high current paths as short and wide as possible.
- Place the input capacitor as close as possible to the device pins (VIN and GND).
- The SW node encounters high-frequency voltage swings, so it should be kept in a small area. Keep sensitive components away from the SW node to prevent stray coupling as possible.
- The GND pin should be connected to a strong ground plane for heat sinking and noise protection.
- Avoid using vias in the power path connections that have switched currents (from C_{IN} to GND and C_{IN} to V_{IN}) and the switching node (SW).

An example of a PCB layout guide is shown in Figure 4 for reference.

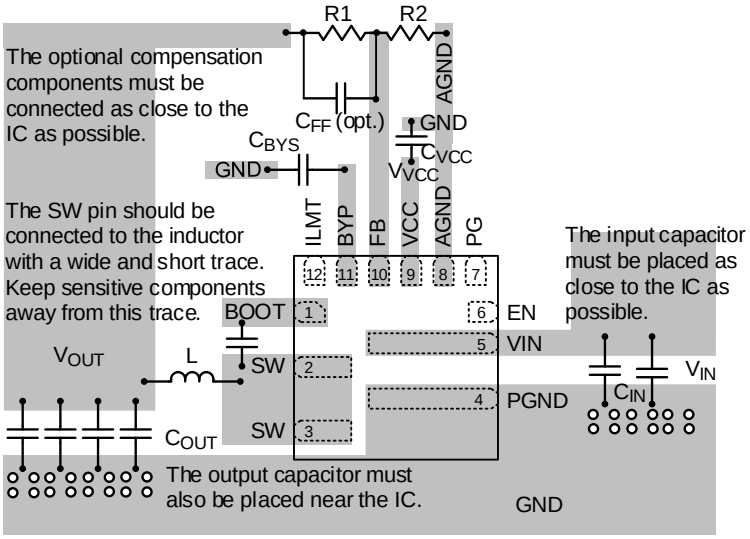
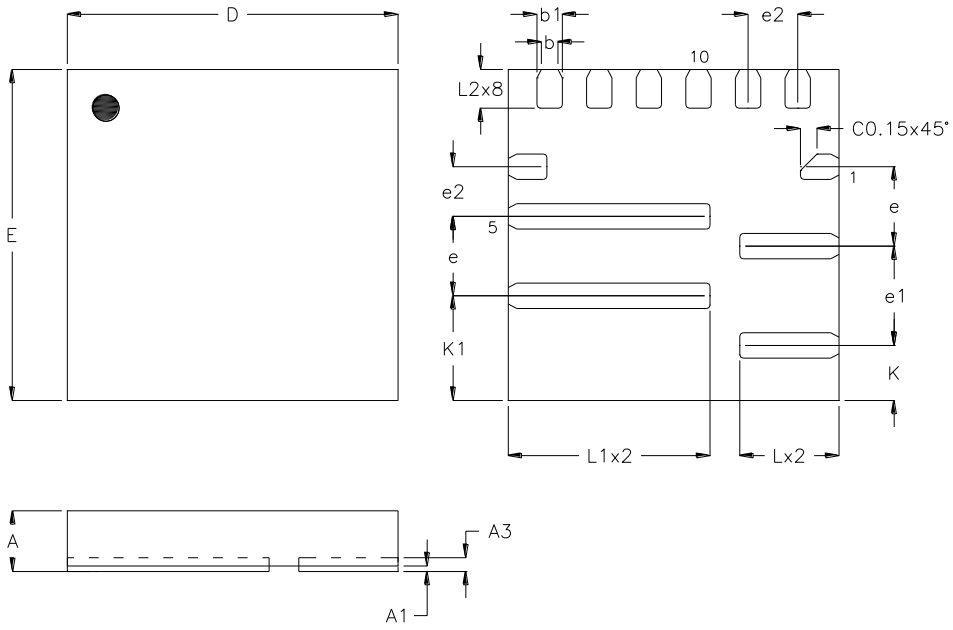


Figure 4. PCB Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

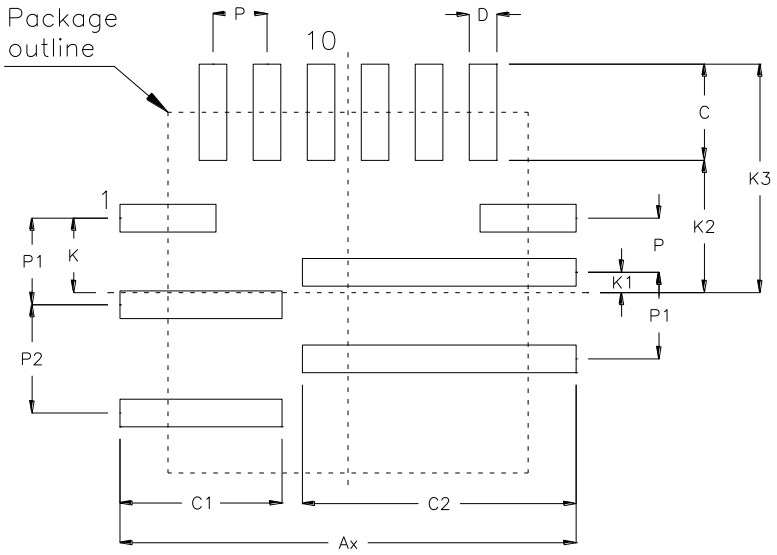
18 Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.100	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
b	0.100	0.200	0.004	0.008
b1	0.180	0.280	0.007	0.011
L	0.800	1.000	0.031	0.039
L1	1.730	1.930	0.068	0.076
L2	0.250	0.450	0.010	0.018
e	0.720		0.028	
e1	0.900		0.035	
e2	0.450		0.018	
K	0.500		0.020	
K1	0.950		0.037	

U-Type 12HL QFN 3x3 (FC) Package

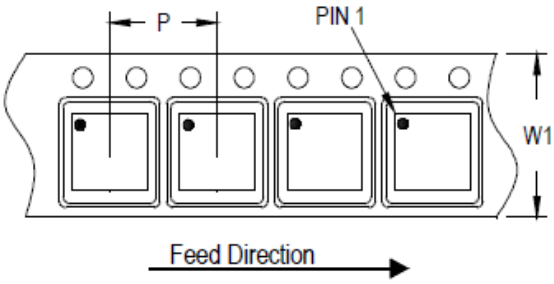
19 Footprint Information

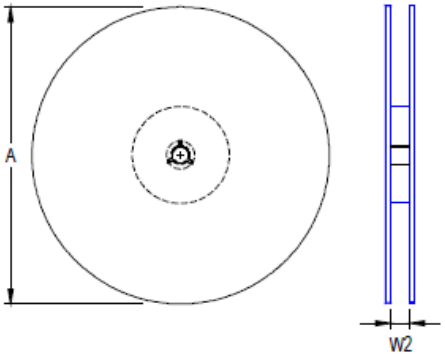


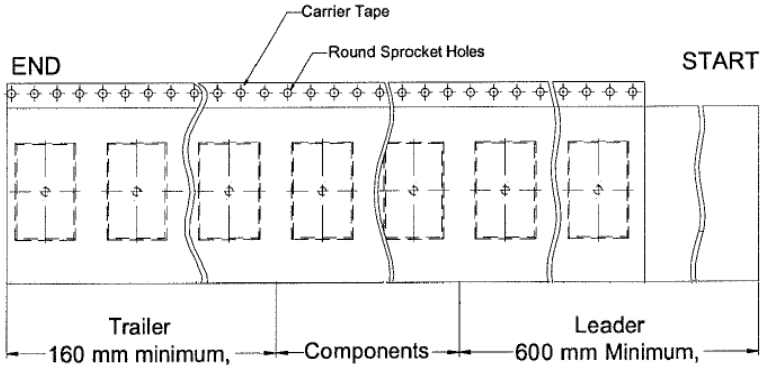
Package	Number of Pin	Footprint Dimension (mm)												Tolerance
		P	P1	P2	Ax	C*8	C1*2	C2*2	D*12	K	K1	K2	K3	
UQFN3*3-12H(FC)	12	0.450	0.720	0.900	3.800	0.800	1.350	2.280	0.230	0.619	0.169	1.100	1.900	±0.050

20 Packing Information

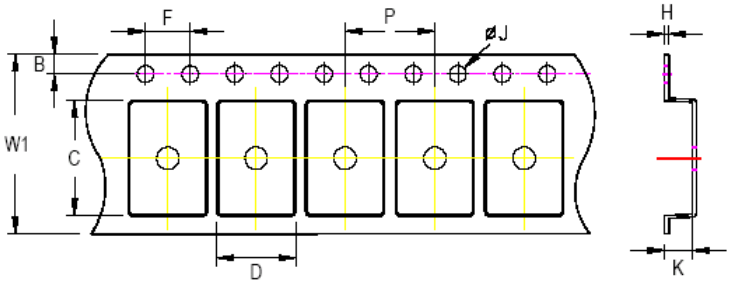
20.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(U) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 12mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.7mm	0.9mm	0.6mm

20.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(U) QFN & DFN 3x3	7”	1,500	Box A	3	4,500	Carton A	12	54,000
			Box E	1	1,500	For Combined or Partial Reel.		

20.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789

21 Datasheet Revision History

Version	Date	Description	Item
03	2025/5/19	Modify	*Changed the names LX to SW, PGOOD to PG* *Changed the names Step-Down to Buck* *General Description on page 1* *Features on page 1* *Ordering Information on page 2* *Electrical Characteristics on page 7, 8* *Application Information on page 14* *Packing Information on page 24 to 26* - Added packing information