RICHTEK®

RT5797A

3A, 1MHz, 6V CMCOT Synchronous Step-Down Converter

1 General Description

The RT5797A is a high efficiency synchronous step-down converter. Its input voltage range is from 2.7V to 6V, and it provides an adjustable regulated output voltage from 0.6V to 3.4V while delivering up to 3A of output current.

The device integrates synchronous low on-resistance power switches, which enhance efficiency and eliminate the need for an external Schottky diode. Its Current Mode Constant-On-time (CMCOT) operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors. The RT5797A is available in the WDFN-8L 2x2 and WDFN-8SL 2x2 packages.

The recommended junction temperature range is –40°C to 125°C, while the ambient temperature range is –40°C to 85°C.

2 Applications

- STB, Cable Modem, xDSL Platforms
- LCD TV Power Supply, Metering Platforms
- General Purpose Point of Load (POL)

3 Features

- **Efficiency Up to 95%**
- **R_{DSON} 100mΩ High-Side / 70mΩ Low-Side**
- **V_{IN} Range: 2.7V to 6V**
- **V_{REF} is 0.6V with ±1% Accuracy at 25°C**
- **CMCOT Control Loop Design for Best Transient Response, Robust Loop Stability with Low-ESR (MLCC) C_{OUT}**
- **Soft-Start Time: 1.2ms**
- **Power Saving in Light Load**

4 Ordering Information

RT5797A □□□

Package Type(1)
QW: WDFN-8L 2x2 (W-Type)
QWA: WDFN-8SL 2x2 (W-Type)
(Exposed Pad-Option 2)

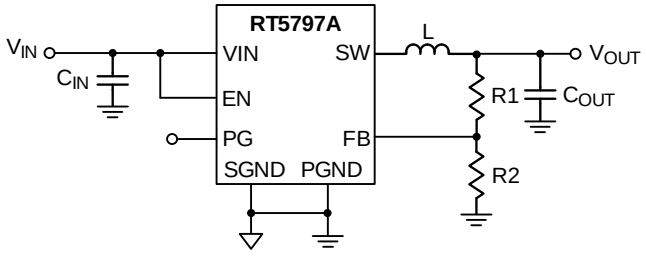
Lead Plating System
G: Richtek Green Policy Compliant (2)

UVP Option
H: Hiccup
L: Latched-Off
(For WDFN-8SL 2x2 (W-Type) Only)

Note 1.

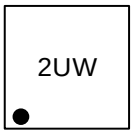
- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

5 Simplified Application Circuit



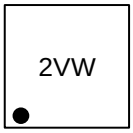
6 Marking Information

RT5797ALGQW



2U: Product Code
W: Date Code

RT5797AHGQW



2V: Product Code
W: Date Code

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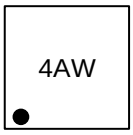

4A: Product Code
W: Date Code

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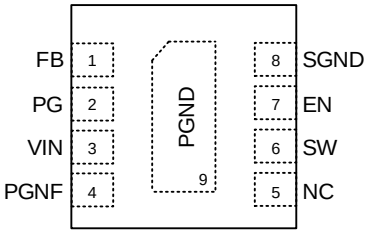
7 Pin Configuration

(TOP VIEW)

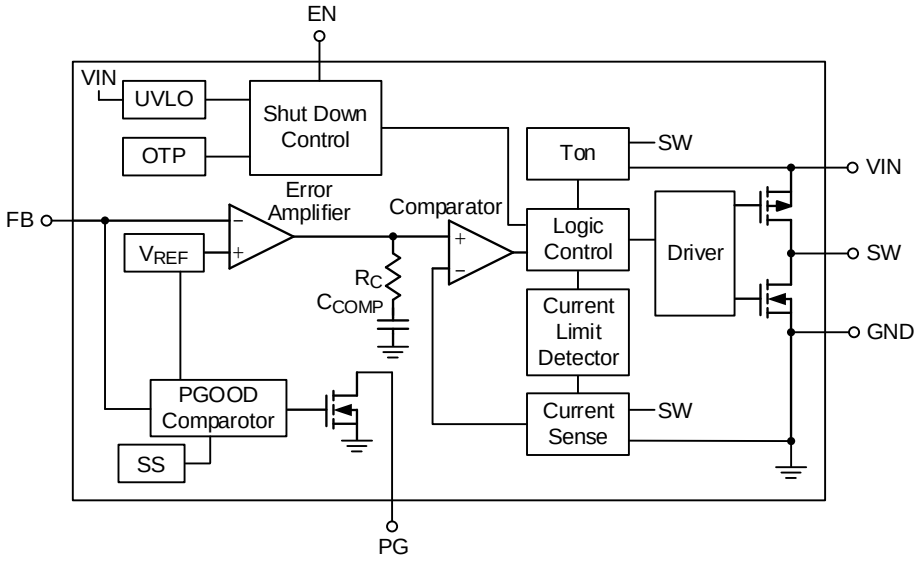


WDFN-8L 2x2/WDFN-8SL 2x2

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
WDFN-8L 2x2 WDFN-8SL 2x2		
1	FB	Feedback voltage input. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
2	PG	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. The PG is pulled high when the FB voltage exceeds 90% of the output voltage; otherwise, it is low.
3	VIN	Supply voltage input. The RT5797A operates from a 2.7V to 6V input.
4, 9 (Exposed Pad)	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
5	NC	No internal connection.
6	SW	Switch node.
7	EN	Enable control input.
8	SGND	Signal GND.

9 Functional Block Diagram



10 Absolute Maximum Ratings

(Note 2)

- VIN Supply Input Voltage ---------- –0.3V to 6.5V
- VIN to SW ---------- –0.3V to 6.5V
- VIN to SW (t ≤ 10ns) ---------- –4.5V to 9V
- Switch Voltage, SW ---------- –0.3V to 6.5V

  SW (t ≤ 10ns) ---------- –4.5V to 9V
- Others Pins ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C

  WDFN-8L 2x2 ---------- 2.19W

  WDFN-8SL 2x2 ---------- 2.19W
- Package Thermal Resistance (Note 3)

  WDFN-8L 2x2, θ_{JA} ---------- 45.5°C/W

  WDFN-8SL 2x2, θ_{JA} ---------- 45.6°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- –40°C to 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)

  HBM (Human Body Model) ---------- 2kV

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 3. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 4. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 5)

- VIN Supply Input Voltage ---------- 2.7V to 6V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Note 5. The device is not guaranteed to function outside its operating conditions.

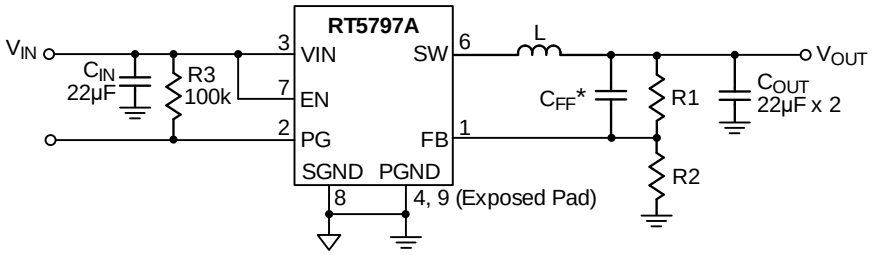
12 Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Supply Input Voltage	V_{IN}		2.7	--	6	V
Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Pin Current	I_{FB}	V_{FB} = 0.6V	--	--	0.1	μA
Quiescent Current (Switching Current)	I_{Q_SW}	Active, V_{FB} = 0.63V, not switching	--	22	36	μA
Shutdown Current	I_{SHDN}	Shutdown	--	--	1	μA
Switching Leakage Current			--	--	1	μA
Switching Frequency	f_{SW}		0.8	1	1.2	MHz
On-Resistance of Low-Side MOSFET	R_{DSON_L}	I_{SW} = 0.3A	--	70	85	mΩ
On-Resistance of High-Side MOSFET	R_{DSON_H}	I_{SW} = 0.3A	--	100	125	mΩ
Positive Inductor Valley Current Limit	I_{LIM_VALLEY}		3.03	3.7	4.6	A
Undervoltage Lockout Rising Threshold	V_{UVLO_R}	VDD rising	--	2.25	2.5	V
Undervoltage Lockout Falling Threshold	V_{UVLO_F}	VDD falling	--	2	--	V
Over-Temperature Protection Threshold	V_{OVP}		--	150	--	°C
EN Input Voltage Rising Threshold	V_{EN_R}	EN rising	0.7	0.85	1.05	V
EN Input Voltage Falling Threshold	V_{EN_F}	EN falling	0.5	0.75	0.95	V
Power-Good Voltage Rising Threshold	V_{PGOOD_R}	Rising	85	90	95	%
Power-Good Voltage Falling Threshold	V_{PGOOD_F}	Falling	80	85	90	%
PG Open-Drain Impedance (PG = Low)			--	--	20	Ω
Soft-Start Time	t_{SS}		0.5	1.2	2	ms
Minimum Off-Time	t_{OFF_MIN}		70	120	180	ns
Maximum Duty Cycle	D_{MAX}	(Note 6)	70	--	--	%
Discharge Resistor	R_{DISCHG}		1.2	1.8	2.4	kΩ
Output Overvoltage Rising Threshold	V_{OVP_R}	Rising	115	120	125	%

Note 6. Guaranteed by design.

13 Typical Application Circuit



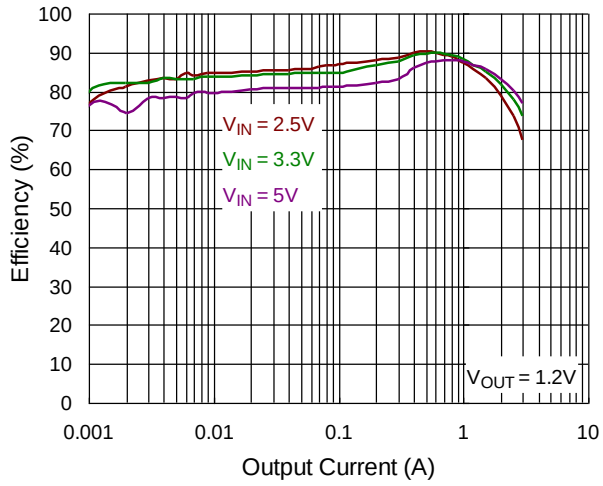
*C_{FF}: Optional for performance fine-tuning.

Table 1. Suggested Component Values

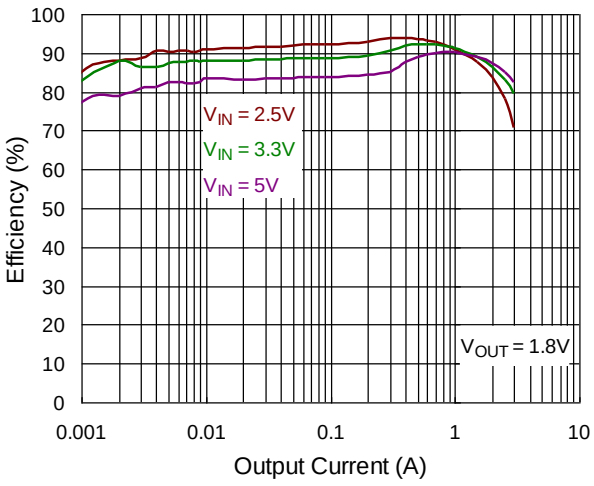
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{IN} (µF)	L (µH)	C_{OUT} (µF)
3.3	90	20	22	1.5	22 x2
1.8	100	50	22	1.5	22 x2
1.5	100	66.6	22	1.5	22 x2
1.2	100	100	22	1.5	22 x2
1.05	100	133	22	1.5	22 x2
1	100	148	22	1.5	22 x2

14 Typical Operating Characteristics

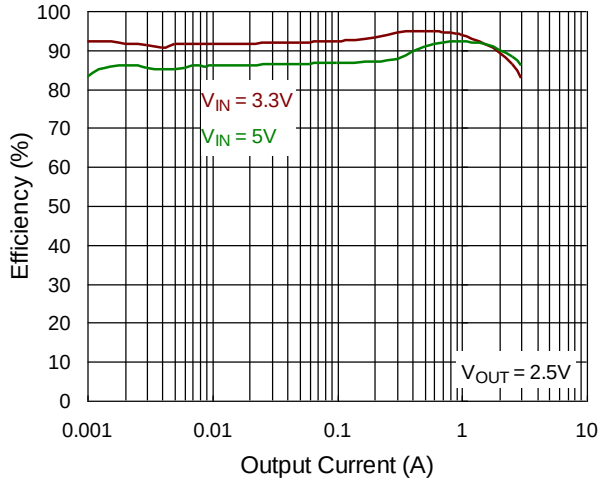
Efficiency vs. Output Current



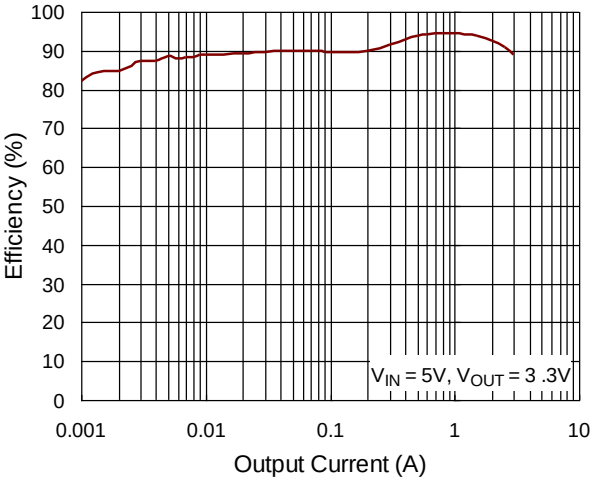
Efficiency vs. Output Current



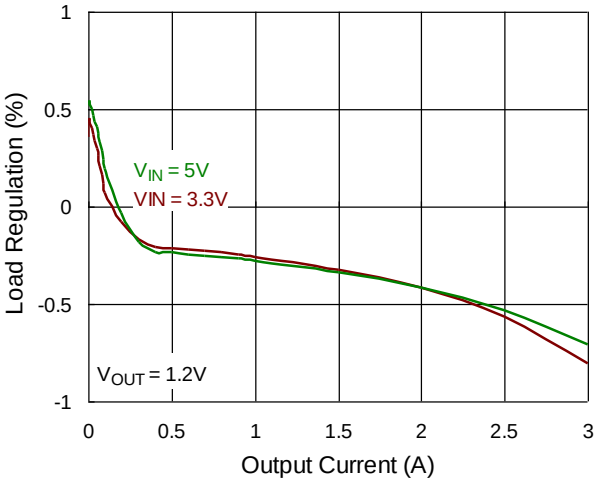
Efficiency vs. Output Current



Efficiency vs. Output Current



Load Regulation



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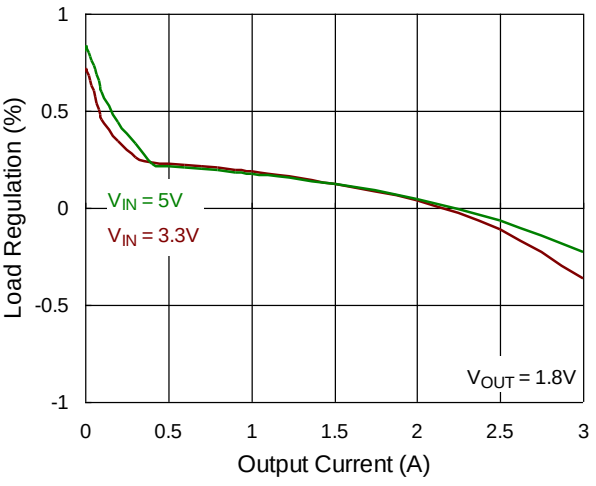

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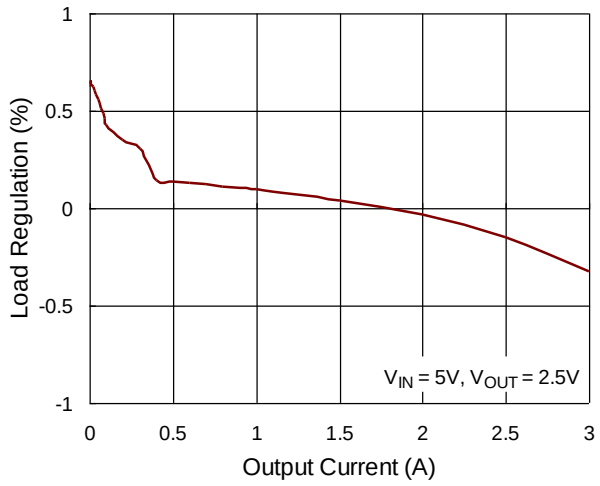
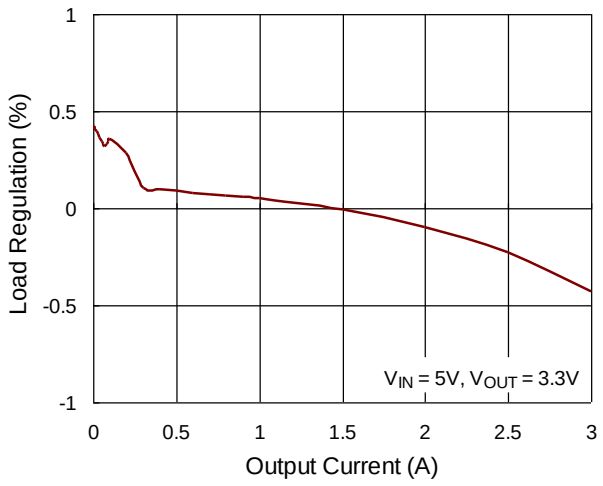
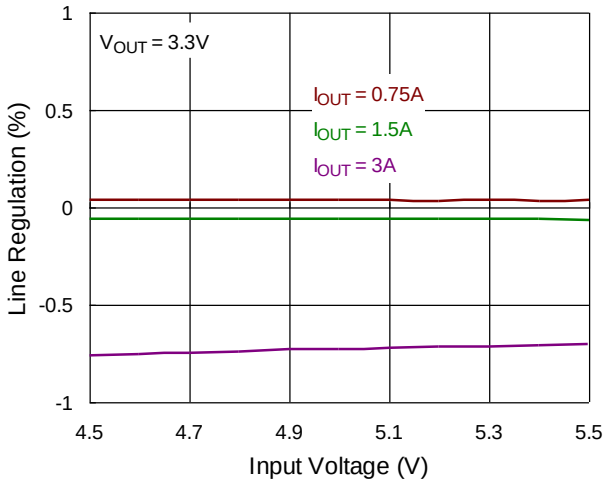


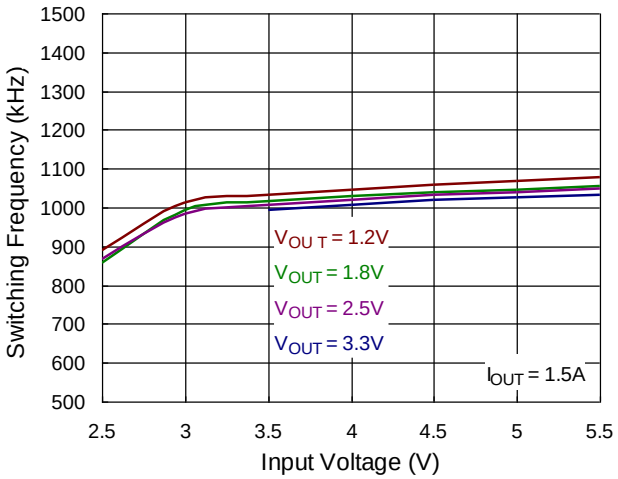
Load Regulation



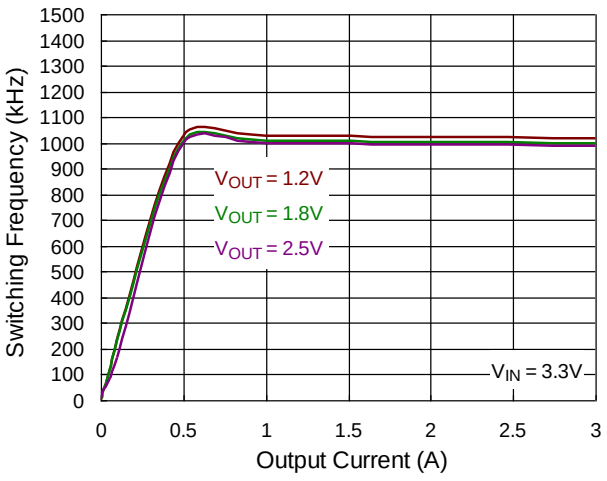
Line Regulation



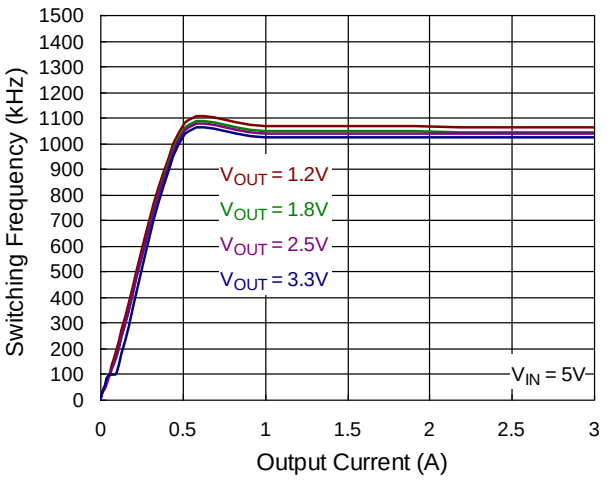
Switching Frequency vs. Input Voltage



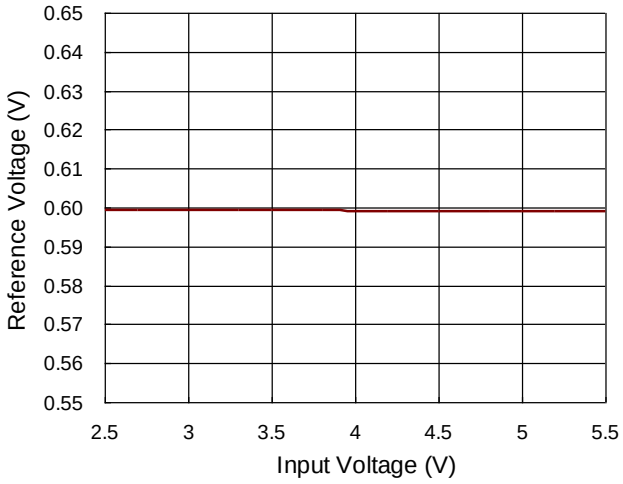
Switching Frequency vs. Output Current



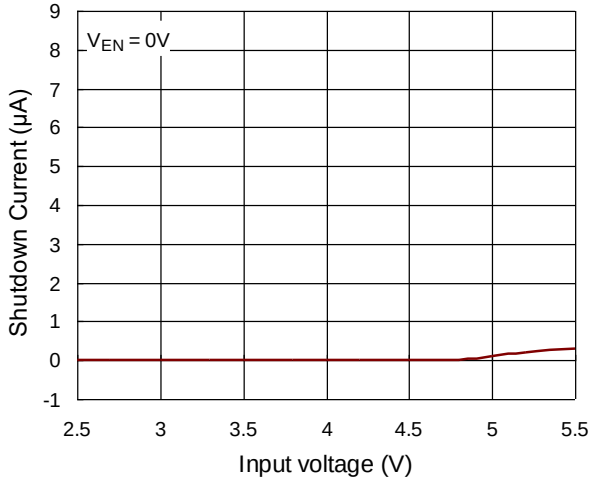
Switching Frequency vs. Output Current



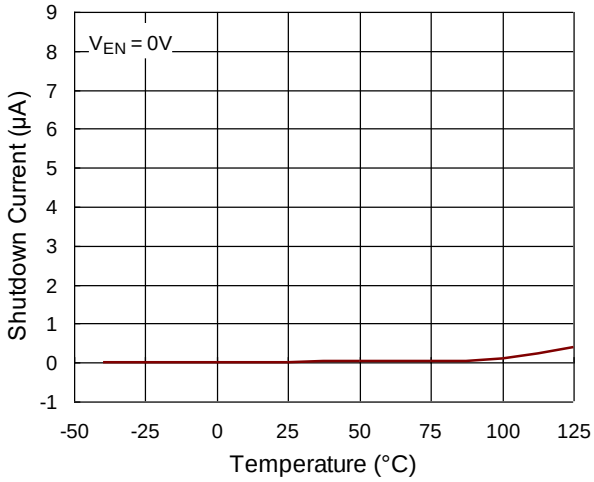
Reference Voltage vs. Input Voltage



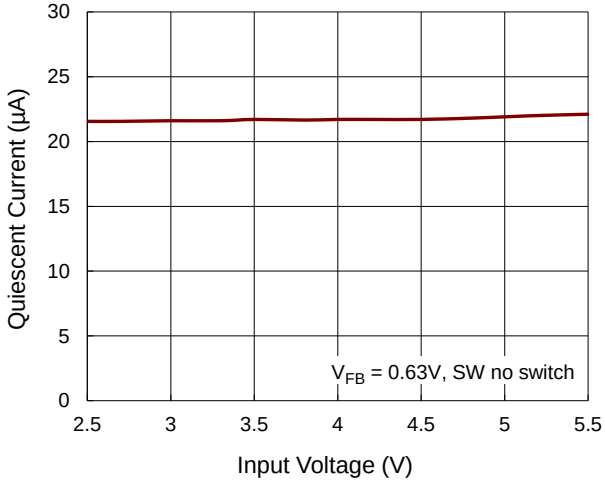
Shutdown Current vs. Input Voltage



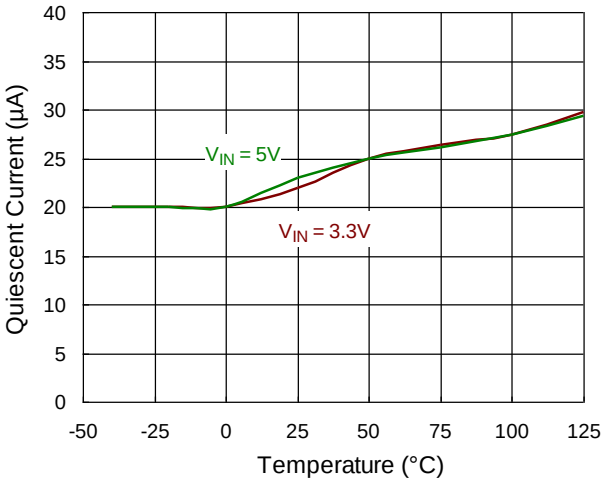
Shutdown Currrent vs. Temperature



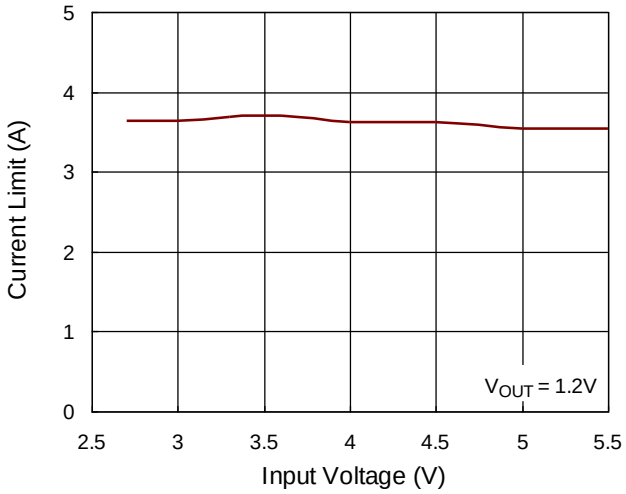
Quiescent Current vs. Input Voltage



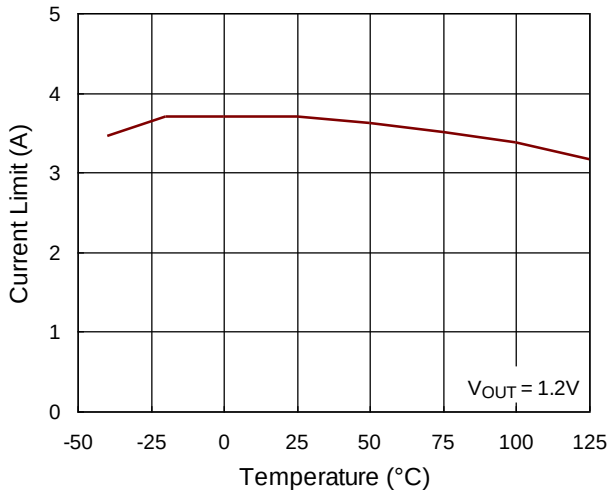
Quiescent Current vs. Temperature



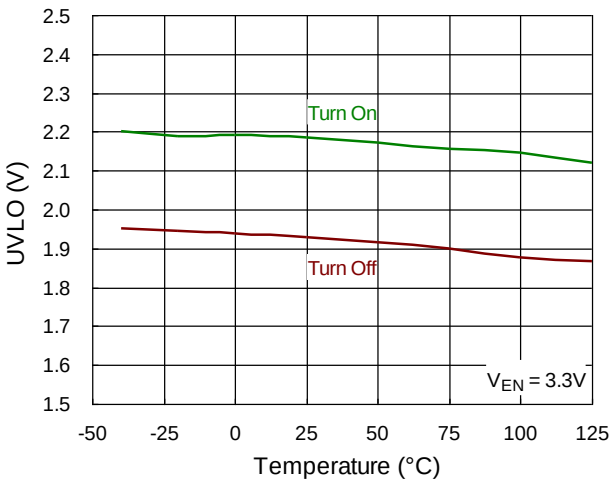
Current Limit vs. Input Voltage



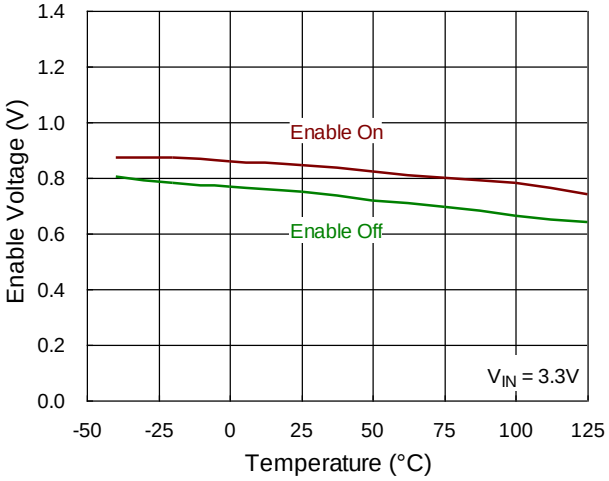
Current Limit vs. Temperature



UVLO vs. Temperature



Enable Voltage vs. Temperature



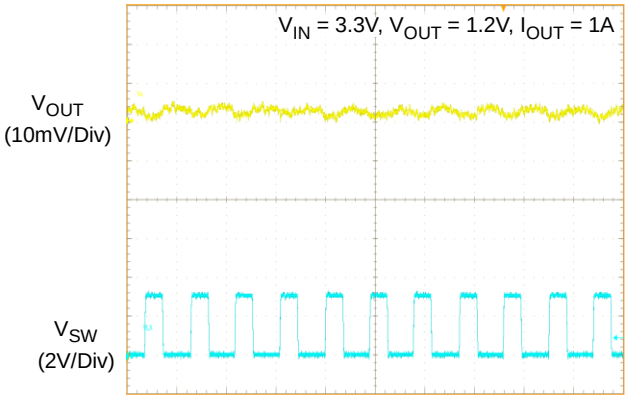
Load Transient Response

Time (100μs/Div)

Load Transient Response

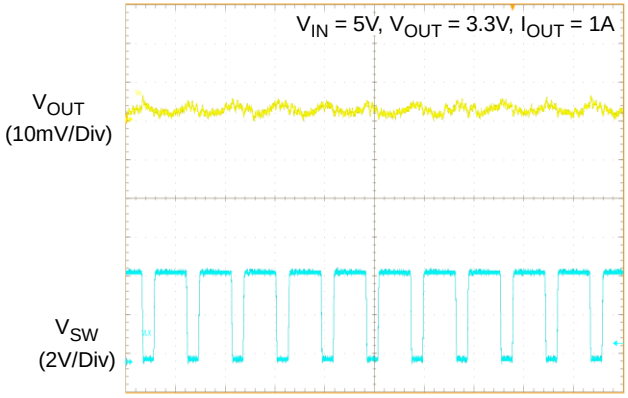
Time (100μs/Div)

Voltage Ripple

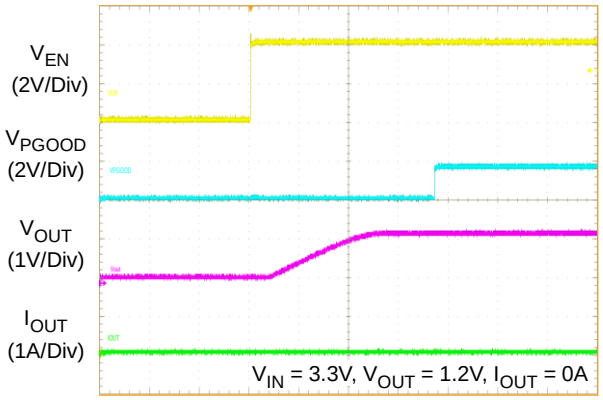


Time (1μs/Div)

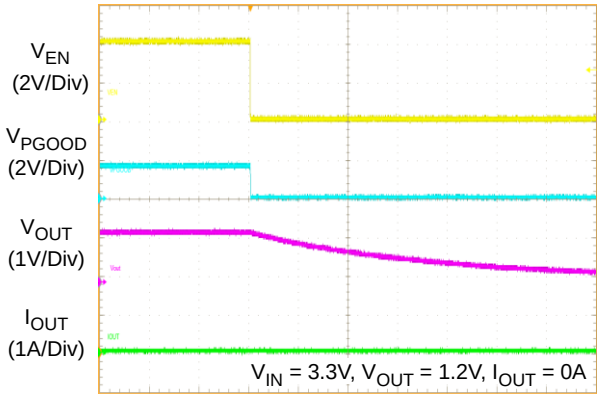
Voltage Ripple



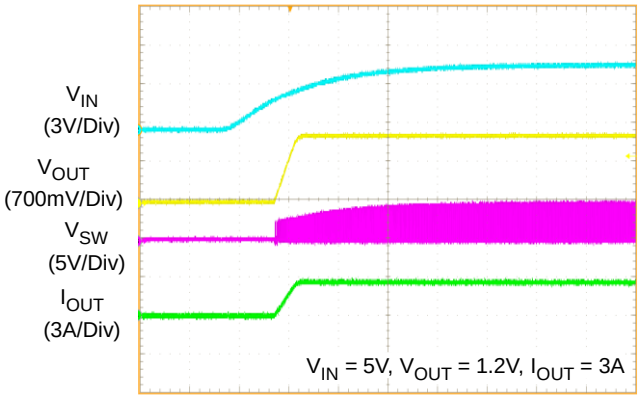
Power On from EN



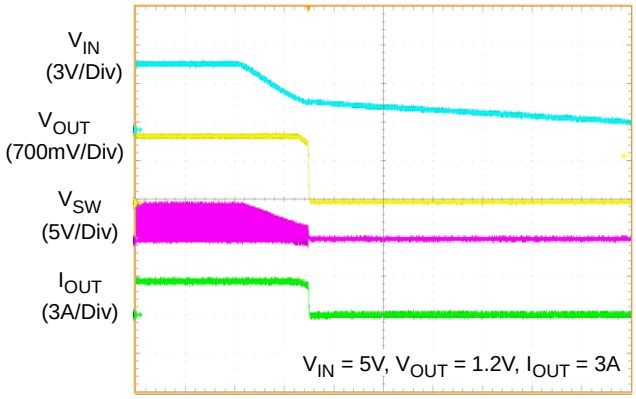
Power Off from EN



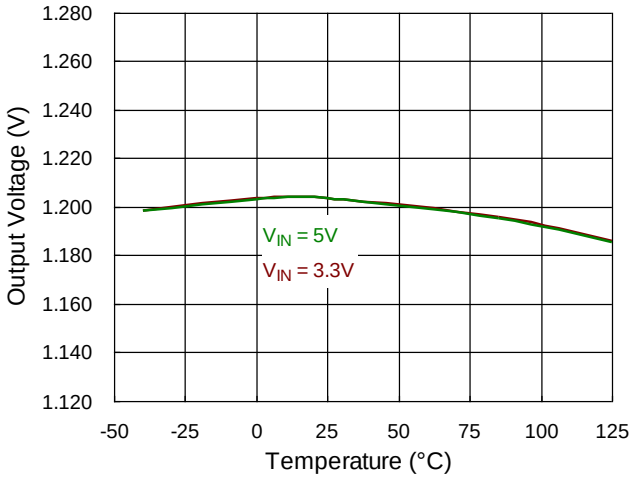
Power On from VIN



Power Off from VIN



Output Voltage vs. Temperature



15 Operation

The RT5797A is a synchronous low voltage step-down converter designed to accommodate an input voltage range from 2.7V to 6V, with the capability to deliver an output current of up to 3A. The RT5797A utilizes a constant on-time, current mode architecture. In normal operation, the high-side P-MOSFET is turned on when the switch controller is set by the comparator and is turned off when the Ton comparator resets the switch controller. The low-side MOSFET peak current is measured by internal RSENSE.

The error amplifier (EA) dynamically adjusts the COMP voltage by comparing the feedback signal (V_{FB}), which is derived from the output voltage, against the internal 0.6V reference voltage. An increase in load current results in a decrease in the feedback voltage compared to the reference, prompting the COMP voltage to increase. This adjustment allows for higher inductor current to match the increased load demand, ensuring stable output voltage under varying load conditions.

15.1 UV Comparator

If the feedback voltage (V_{FB}) is lower than threshold voltage 0.2V, the UV comparator's output will go high and the switch controller will turn off the high-side MOSFET. The RT5797A implements the undervoltage differently depending on the model: the RT5797AH is designed to enter Hiccup mode, while the RT5797AL will engage Latch mode upon detection of an undervoltage condition.

15.2 Soft-Start (SS)

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 1.2ms.

15.3 PGOOD Comparator

When the feedback voltage (V_{FB}) is higher than the threshold voltage 0.54V and the internal soft-start function has completed, the PGOOD open-drain output will go to high impedance. The internal PGOOD MOSFET has a typical resistance of 20Ω. The delay time of the PGOOD signal is defined as the duration from when EN goes high to the completion of the internal soft-start function, which is about 2ms (Typical).

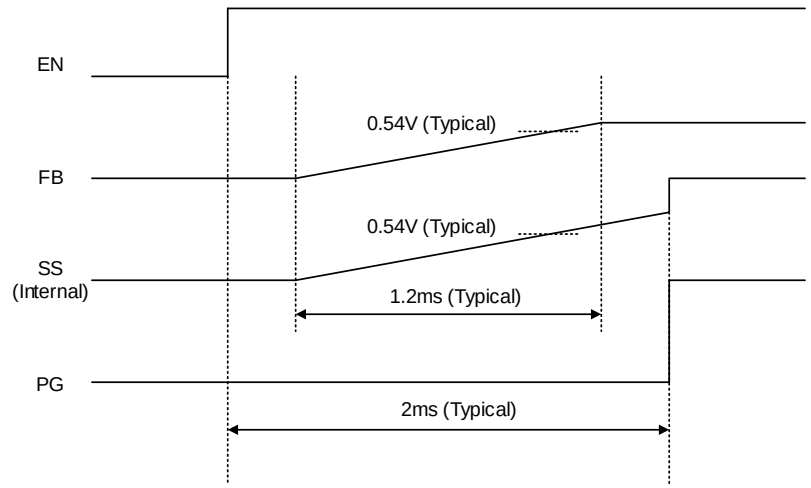


Figure 1. PGOOD Comparator

15.4 Enable Comparator

A logic-high enables the converter; a logic-low forces the IC into shutdown mode.

15.5 Overcurrent Protection (OCP)

The RT5797A features overcurrent protection that monitor the valley current of the low-side MOSFET inductor. If the sensed valley inductor current exceeds the current-limit threshold of 3.7A typical), the OCP will be triggered. Once triggered, the OCP maintains the overcurrent threshold level, which in turn may engage the undervoltage (UV) protection mechanism.

15.6 Over-Temperature Protection (OTP)

The device features an internal over-temperature protection function that activates when the junction temperature exceeds 150°C. The over-temperature protection forces the device to stop switching when the junction temperature exceeds the over-temperature protection threshold. Once the die temperature falls below the threshold by a hysteresis margin of 20°C, the device will initiate the power-up sequence.

15.7 Maximum Duty Cycle

The maximum duty cycle (70%, minimum) can be calculated by minimum off-time (180ns, maximum), dead time (60ns, maximum) and switching frequency (1.2MHz, maximum).

$D_{MAX} = 1 - (t_{OFF\_MIN} + t_D) \times f_{SW}$

Where t_{OFF_MIN} is minimum off-time, t_D is dead time, and f_{SW} is switching frequency.

If the input voltage and the output voltage are close, the RT5797A operates at a high duty cycle. Once the operational duty cycle is larger than the maximum duty cycle (70%, minimum), the RT5797A keeps minimum off-time (180ns, maximum) and dead time (60ns, maximum), then the output voltage starts to drop. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

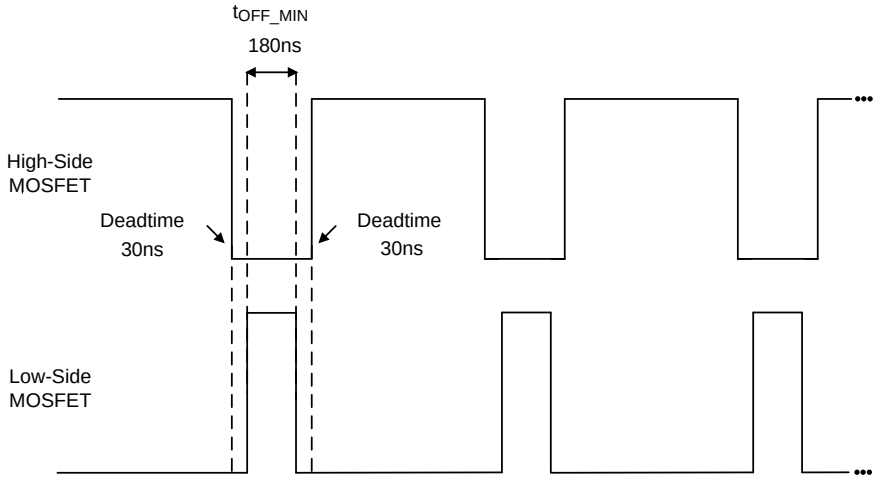


Figure 2. Maximum Duty Cycle

16 Application Information

(Note 7)

The RT5797A is a single-phase step-down converter. It provides a single feedback loop constant on-time, current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz) oscillator and internal compensation are integrated to minimize external component count. It also includes protection features such as overcurrent, undervoltage and over-temperature protection.

16.1 Output Voltage Setting

Connect a resistive voltage divider at the FB between V_{OUT} and GND to adjust the output voltage. The output voltage is set according to the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} is the feedback reference voltage 0.6V (typical).

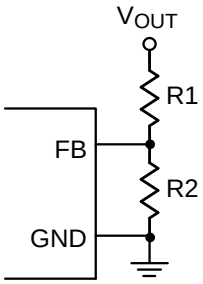


Figure 3. Setting V_{OUT} with a Voltage Divider

16.2 Chip Enable and Disable

The EN pin allows for power sequencing between the controller bias voltage and another voltage rail. The RT5797A remains in shutdown if the EN pin is lower than 400mV. When the EN pin exceeds the V_{EN} trip point, the RT5797A initiates a new initialization and soft-start cycle.

The enable-disable falling time slew rate should be larger than 1mV/μs.

16.3 Internal Soft-Start

The RT5797A features an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During the soft-start, the internal soft-start capacitor is charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing PWM pulse width to increase slowly and in turn reduce the input surge current. The internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V.

16.4 Overvoltage Protection (OVP)

The RT5797AL features an overvoltage protection function that activates when the output voltage exceeds 120% of the set output voltage, causing the IC to enter latch-off mode.

16.5 UVLO Protection

The RT5797A features an input Undervoltage Lockout protection (UVLO). When the input voltage exceeds the UVLO rising threshold voltage (2.25V typical), the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device will stop switching. The UVLO rising and falling threshold voltage has a hysteresis to prevent noise-caused reset.

16.6 Input Capacitor Selection

High-quality ceramic input decoupling capacitors, such as X5R or X7R, with values greater than 22μF are recommended for the input capacitor. The X5R and X7R ceramic capacitors are usually selected for power regulator capacitors because the dielectric material has less capacitance variation and offers more temperature stability.

Voltage rating and current rating are the key parameters when selecting an input capacitor. Generally, selecting an input capacitor with voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation:

$$I_{IN\_RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for RMS current rating. A good design is to use multiple capacitors with low equivalent series resistance (ESR) in parallel to form a capacitor bank.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be approximately calculated using the following equation:

$$\Delta V_{IN} = \frac{I_{OUT(MAX)}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

16.7 Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the Buck converter topology. In steady-state condition, the ripple current flowing into/out of the capacitor generates a ripple voltage. The output voltage ripple (V_{P-P}) can be calculated by the following equation:

$$V_{P\_P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

When load transient occurs, the output capacitor supplies the load current before the controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage undershoot (V_{SAG}) can be calculated by the following equation:

$$V_{SAG} = \Delta I_{LOAD} \times ESR$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that influences on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, the ESL contributes to part of the voltage sag. Using a capacitor with low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using a single capacitor for the same total ESR.

16.8 Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown below:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times LIR \times I_{LOAD(MAX)} \times V_{IN}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \times I_{LOAD(MAX)}\right)$$

The calculation above serves as a general reference. To further improve transient response, the output inductor can be further reduced. This relation should be considered along with the selection of the output capacitor.

The inductor saturation current rating should be higher than IC's current limit.

16.9 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-8L 2x2 package, the thermal resistance, θ_{JA}, is 45.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a WDFN-8SL 2x2 package, the thermal resistance, θ_{JA}, is 45.6°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C – 25°C) / (45.5°C/W) = 2.19W for a WDFN-8L 2x2 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (45.6°C/W) = 2.19W for a WDFN-8SL 2x2 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

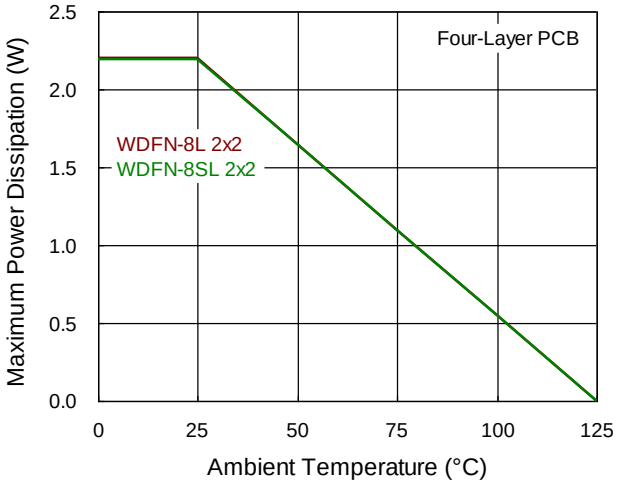


Figure 4. Derating Curve of Maximum Power Dissipation

16.10 Layout Considerations

For best performance of the RT5797A, the following layout guidelines must be strictly followed.

- The input capacitor must be placed as close to the IC as possible.
- SW should be connected to the inductor by wide and short trace. Keep sensitive components away from this trace.
- Keep every trace connected to pins as wide as possible for improving thermal dissipation.
- The feedback components must be connected as close to the device as possible. Keep sensitive components away.
- Vias can help to reduce power trace and improve thermal dissipation.

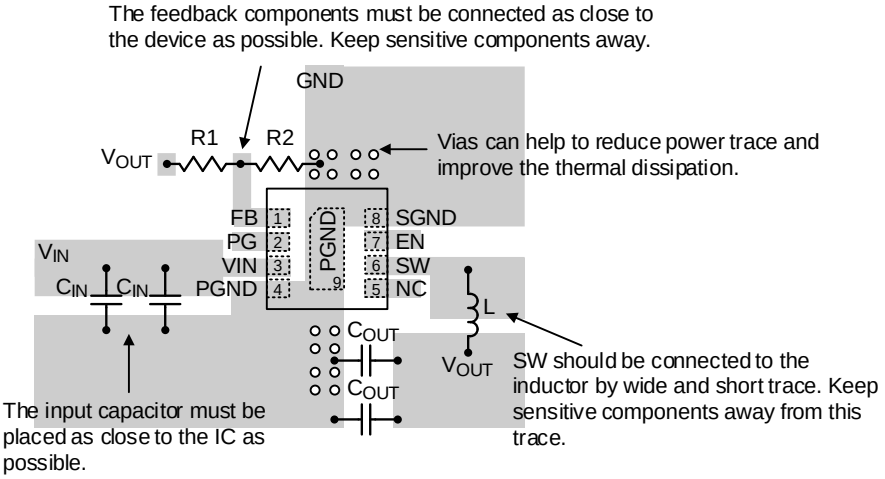
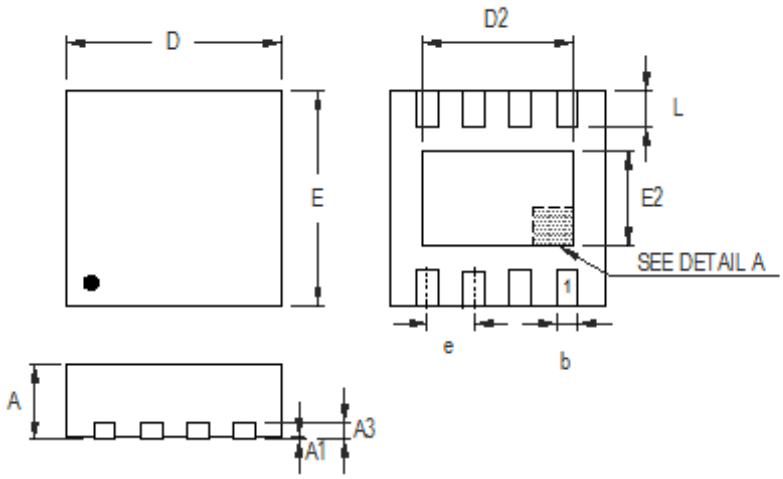
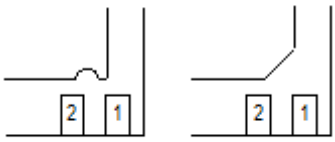


Figure 5. PCB Layout Guide

Note 7. The information provided in this section is for reference only. The customer is solely responsible for designing, validating, and testing any applications incorporating Richtek's product(s). The customer is also responsible for applicable standards and any safety, security, or other requirements.

17 Outline Dimension





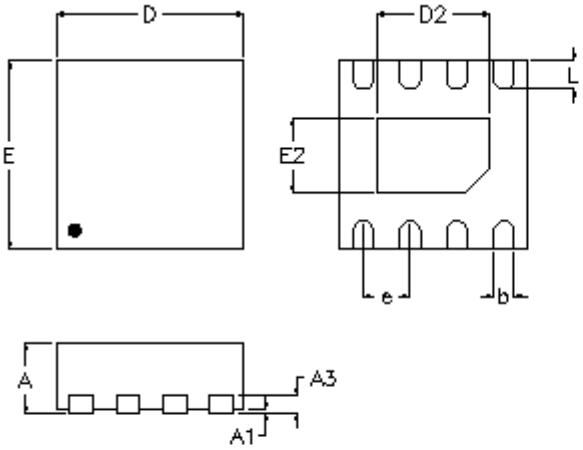
DETAIL A

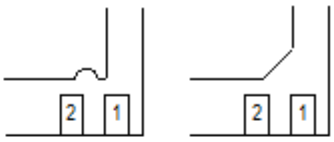
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package





DETAIL A

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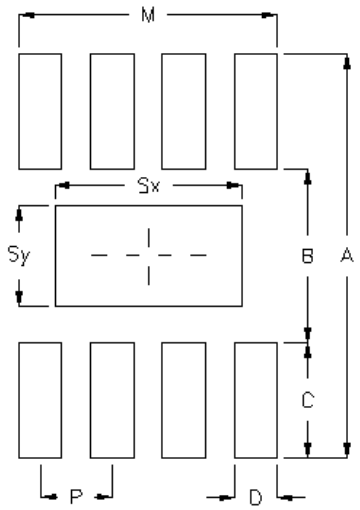
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

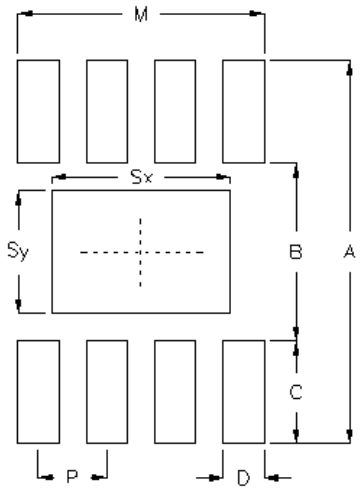
W-Type 8SL DFN 2x2 Package

Note 8. The package of the RT5797A uses Option2.

18 Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8	8	0.50	2.80	1.20	0.80	0.30	1.30	0.70	1.80	±0.05

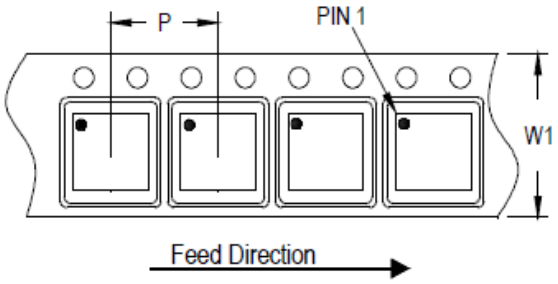


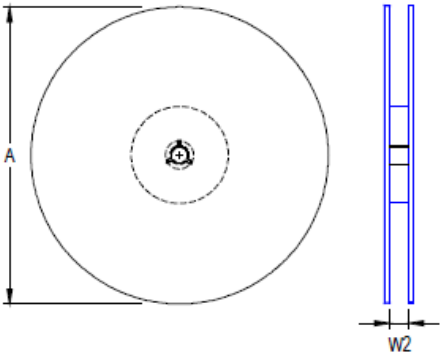
Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8S	Option1	8	0.50	2.80	1.30	0.75	0.30	1.30	0.90	1.80	±0.05
	Option2							1.60	0.90		

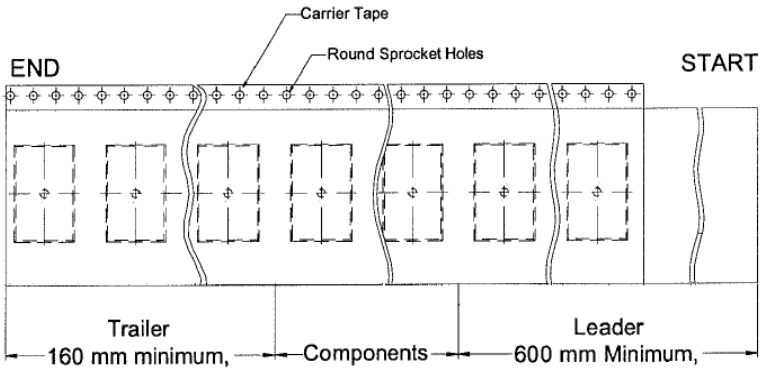
Note 9. The package of the RT5797A uses Option2.

19 Packing Information

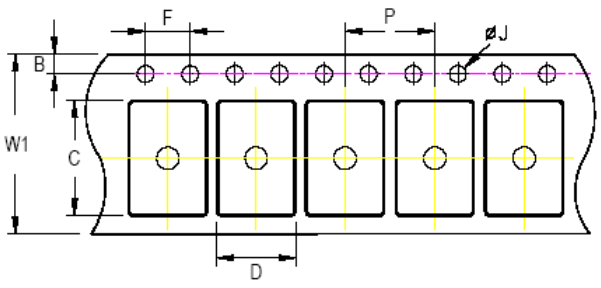
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	2,500	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	2,500	Box A	3	7,500	Carton A	12	90,000
			Box E	1	2,500	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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20 Datasheet Revision History

Version	Date	Description	Item
12	2023/12/28	Modify	General Description on P1 Ordering Information on P1 Operation on P3 Application Information on P13 Outline Dimension on P17 Footprint Information on P18, 19 Packing Information on P20, 21, 22
13	2024/10/14	Modify	*Changed the name of pin 6 to SW.* *Ordering Information on page 1* - Added note *Electrical Characteristics on page 6* - Updated the parameter and symbol *Application Information on page 19* - Added declaration *Packing Information on page 24* - Updated Tape and Reel Data