RICHTEK®

RT5753

3A, 1.2MHz, 6V Synchronous Step-Down Converter

1 General Description

The RT5753 is a simple, easy-to-use, 3A synchronous step-down converter with an input supply voltage range from 2.5V to 6V. The device builds in an accurate 0.6V reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in WDFN-8L 2x2 and WDFN-8SL 2x2 packages.

The RT5753 adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate at nearly constant switching frequency over the line, load, and output voltage range. The RT5753A/C/E/F operates in automatic PSM that maintains high efficiency during light load operation. The RT5753B/D operates in Forced PWM that helps to meet tight voltage regulation accuracy requirements.

The RT5753 senses the current in both MOSFETs for robust overcurrent protection. The device features cycle-by-cycle current-limit protection, which prevents the device from catastrophic damage in the event of an output short circuit, overcurrent, or inductor saturation. A built-in soft-start function prevents inrush current during start-up. The device also includes input undervoltage-lockout, output undervoltage protection, overvoltage protection (RT5753AL/BL/CL/DL/EL/FL), and over-temperature protection to provide safe and smooth operation in all operating conditions. The recommended junction temperature range is –40°C to 125°C.

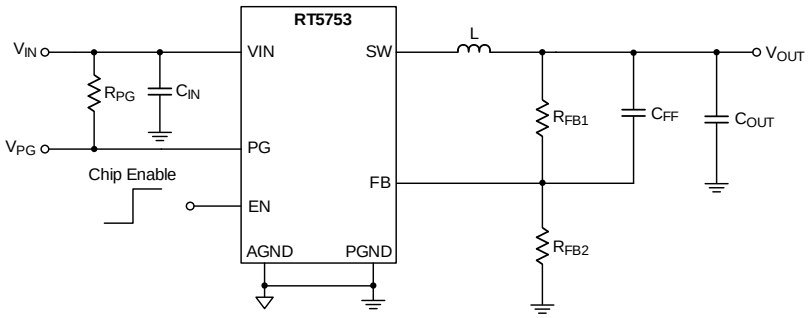
2 Features

- **Input Voltage Range from 2.5V to 6V**
- **Integrated 100mΩ and 70mΩ MOSFETs**
- **100% Duty Cycle for Lowest Dropout**
- **Internal Reference Voltage with 1% Accuracy**
- **1.2MHz Typical Switching Frequency**
- **Power Saving Mode for Light Loads (RT5753A/C/E/F)**
- **Advanced Constant On-Time (ACOT®) Control**
- **Internal Soft-Start (1.5ms/750μs)**
- **Enable Control Input**
- **Power-Good Indicator**
- **Both MOSFETs Overcurrent Protection**
- **Negative Overcurrent Protection (RT5753B/D)**
- **Input Undervoltage-Lockout Protection**
- **Output Undervoltage Protection**
- **Over-Temperature Protection**

3 Applications

- Mobile Phones and Handheld Devices
- Set-Top Boxes and xDSL Platforms
- WLAN ASIC Power/Storage (SSD and HDD)
- General Purpose for POL LV Buck Converters

4 Simplified Application Circuit



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5 Ordering Information

RT5753 □□□□

Package Type(1)

QW: WDFN-8L 2x2 (W-Type)

QWA: WDFN-8SL 2x2 (W-Type)
(Exposed Pad-Option 2)

Lead Plating System

G: Richtek Green Policy Compliant(2)

UVP Option

H: Hiccup (For A, B, C, D only)

L: Latched-Off

PWM Operation Mode

A: SS TIME = 1.5m(typical) & Automatic PSM & R_{DISCHG} = 100Ω

B: SS TIME = 1.5m(typical) & Forced PWM & R_{DISCHG} = 100Ω

C: SS TIME = 750μs(typical) & Automatic PSM & R_{DISCHG} = 100Ω

D: SS TIME = 750μs(typical) & Forced PWM & R_{DISCHG} = 100Ω

E: SS TIME = 1.5m(typical) & Automatic PSM & R_{DISCHG} = 50Ω

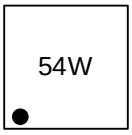
F: SS TIME = 750μs(typical) & Automatic PSM & R_{DISCHG} = 50Ω

Note 1.

- Marked with (1) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (2) indicated: Richtek products are Richtek Green Policy compliant.

6 Marking Information

RT5753AHGQW



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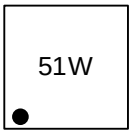

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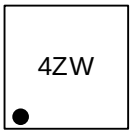

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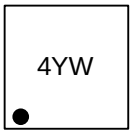

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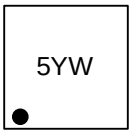

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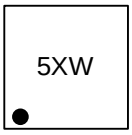

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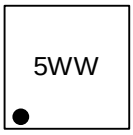

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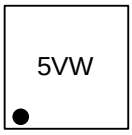

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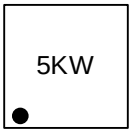

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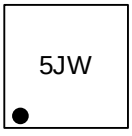

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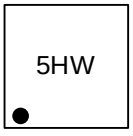

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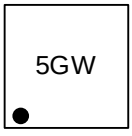

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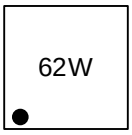

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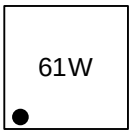

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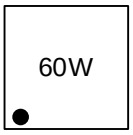

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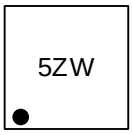

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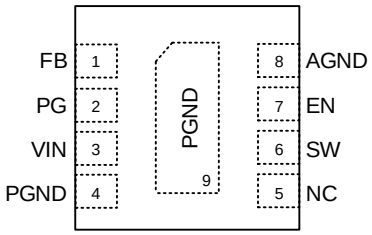
7 Pin Configuration

(TOP VIEW)



WDFN-8L 2x2/WDFN-8SL 2x2

8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Output voltage sense. Sense the output voltage at the FB pin through a resistive divider. The feedback reference voltage is typically 0.6V.
2	PG	Open-drain power-good indicator output. Once started up, PG will be pulled low to ground if any internal protection is triggered.
3	VIN	Power input. The input voltage range is from 2.5V to 6V. Connect a suitable input capacitor between this pin and PGND pins, usually one 22μF or higher than 22μF ceramic capacitor is recommended.
4, 9 (Exposed Pad)	PGND	Power ground. The exposed pad is internally unconnected and must be soldered to a large PCB cooper area and connected to PGND for maximum power dissipation.
5	NC	No internal connection. Keep this pin floating.
6	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor.
7	EN	Enable control input. Connect this pin to a logic high to enable the device and connect this pin to ground to disable the device.
8	AGND	Analog ground.

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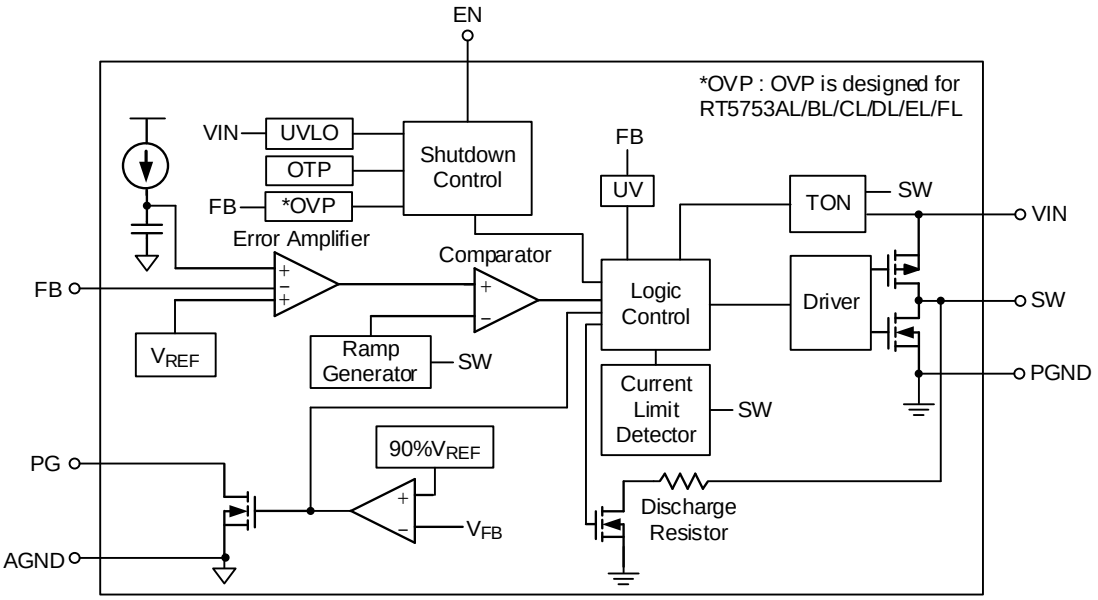
9 Functional Block Diagram



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10 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage ---------- –0.3V to 6.5V
- VIN to SW ---------- –0.3V to 6.5V
- VIN to SW (t ≤ 10ns) ---------- –2.5V to 9V
- Switch Voltage, SW ---------- –0.3V to 6.5V

  SW (t ≤ 10ns) ---------- –2.5V to 9V
- Other Pins ---------- –0.3V to 6.5V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

11 ESD Ratings

(Note 3)

- HBM (Human Body Model) ---------- 2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

12 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage ---------- 2.5V to 6V
- Output Voltage ---------- 0.6V to V_{IN}
- Junction Temperature Range ---------- –40°C to 125°C

Note 4. The device is not guaranteed to function outside its operating conditions.

13 Thermal Information

(Note 5 and Note 6)

Thermal Parameter		WDFN-8L 2x2	WDFN-8SL 2x2	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	49.5	48.2	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	167.1	158.5	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	5.8	5.5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	49.7	49.7	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	5.01	5.01	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.5	30.5	°C/W

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Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6.$\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board with dimensions of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

14 Electrical Characteristics

(V_{IN} = 3.6V. T_J = T_A = −40°C to 125°C. Typical value is tested at T_A = 25°C. The limit over-temperature is guaranteed by characterization, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Voltage	V_{IN}		2.5	--	6	V
Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising	2.15	2.3	2.45	V
Undervoltage-Lockout Threshold Hysteresis	ΔV_{UVLO}		--	300	--	mV
Shutdown Current	I_{SHDN}	V_{EN} = 0V, T_A = 25°C	--	--	2	μA
		V_{EN} = 0V	--	--	15	
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 0.7V, not switching	--	23	35	μA
Soft-Start						
Soft-Start Time	t_{SS}	0%V_{OUT} to 95%V_{OUT}, RT5753A/B/E	1	1.5	2.4	ms
		0%V_{OUT} to 95%V_{OUT}, RT5753C/D/F	0.5	0.75	1.2	
Enable Voltage						
EN Input Voltage Rising threshold	V_{EN_R}		0.8	--	1.2	V
EN Input Voltage Falling threshold	V_{EN_F}		0.4	--	0.85	V
Enable Pull-Low Current	I_{EN_PL}		--	1.5	--	μA
Feedback Voltage						
Feedback Voltage	V_{FB}		0.594	0.6	0.606	V
Feedback Input Current	I_{FB}	V_{FB} = 0.6V, T_A = 25°C	--	0.1	0.4	μA
Internal MOSFET						
On-Resistance of High-Side MOSFET	R_{DSON_H}		--	100	120	mΩ
On-Resistance of Low-Side MOSFET	R_{DSON_L}		--	70	85	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1.5μH, T_A = 25°C	3.6	4.14	4.8	A
Low-Side Switch Current Limit	I_{LIM_L}		3	3.45	3.9	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency						
Switching Frequency	f_{SW}		1	1.2	1.44	MHz
On-Time Timer Control						
Minimum Off-Time	t_{OFF_MIN}		--	90	--	ns
Output Voltage Protection						
Output Undervoltage Threshold (RT5753AH/BH/CH/DH: Hiccup Mode) (RT5753AL/BL/CL/DL/EL/FL: Latch-Off Mode)	V_{UVP}		--	40	--	%
Output Overvoltage Threshold (RT5753AL/BL/CL/DL/EL/FL: Latch-Off Mode, Deglitch Time = 2μs)	V_{OVP}	V_{FB} rising	110	120	130	%
Over-Temperature Protection						
Over-Temperature Protection Threshold	T_{OTP}		--	150	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	
Power Good						
Power-Good High Threshold	V_{TH_PGLH}	V_{FB} rising, PG goes high	83	90	--	%
Power-Good Falling Threshold	V_{TH_PGHL}	V_{FB} falling, PG goes low	78	85	--	%
Power-Good Sink Current Capability		I_{PG} sinks 5mA	--	--	0.4	V
Output Discharge Resistor						
Output Discharge Switch On-Resistor (RT5753A/B/C/D)	R_{DISCHG}	V_{EN} = 0V (Protection)	--	100	--	Ω
Output Discharge Switch On-Resistor (RT5753E/F)			--	52	--	Ω

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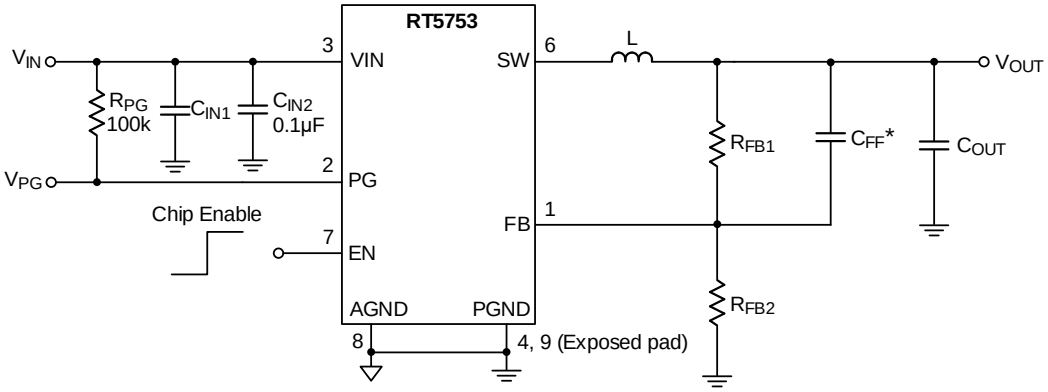
15 Typical Application Circuit



C_{FF}*: Optional for performance fine-tune

Table 1. Suggested Component Values

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{IN1} (µF)	L (µH)	C_{OUT} (µF)	C_{FF} (pF)
3.3	100	22.1	22	1	44 to 66	--
1.8	100	50	22	1	44 to 66	--
1.5	100	66.6	22	1	44 to 66	--
1.2	100	100	22	1	44 to 66	22
1.05	100	133	22	1	44 to 66	22
1	100	148	22	1	44 to 66	22

Table 2. Recommended External Components

Component	Description	Vendor P/N
C_{IN}	22µF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (MURATA)
C_{OUT}	22µF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (MURATA)
L	1µH	DFE322512F-1R0M (MURATA)

Note 7. C_{OUT} and C_{IN}: Considering the effective capacitance, which is de-rated based on the biased voltage level and size, the C_{OUT} and C_{IN} components need to satisfy the effective capacitance as specified for the recommended external components.

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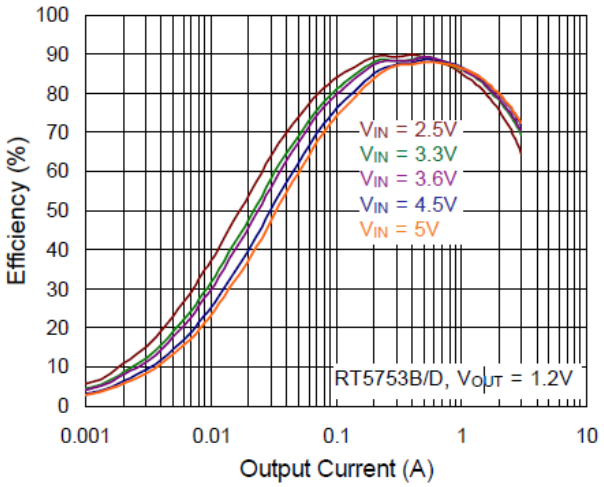
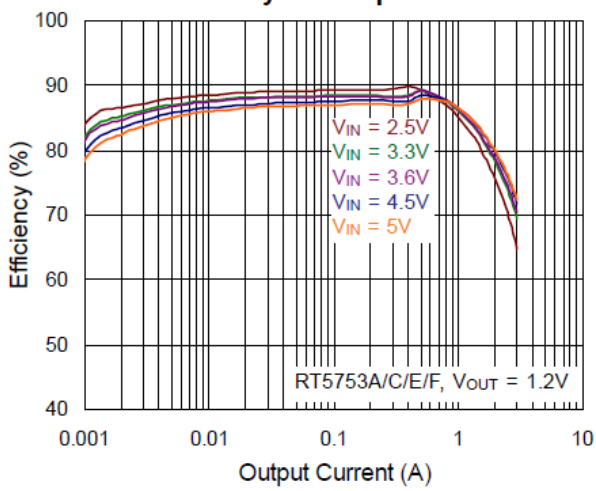
16 Typical Operating Characteristics

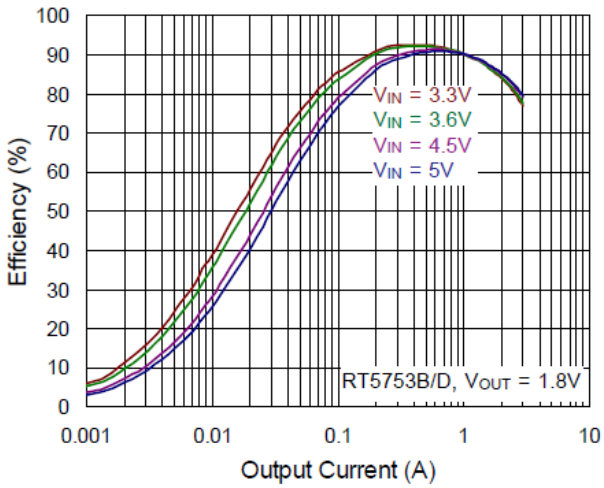
Efficiency vs. Output Current



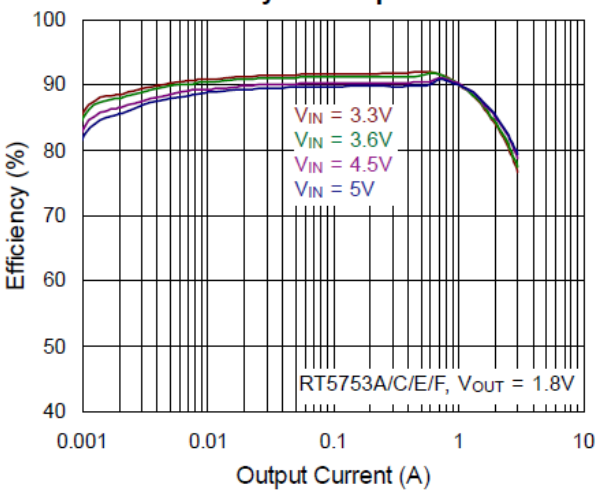
Efficiency vs. Output Current



Efficiency vs. Output Current



Efficiency vs. Output Current



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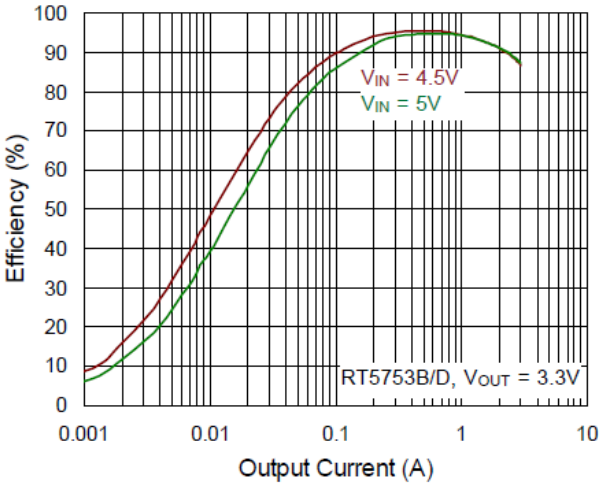

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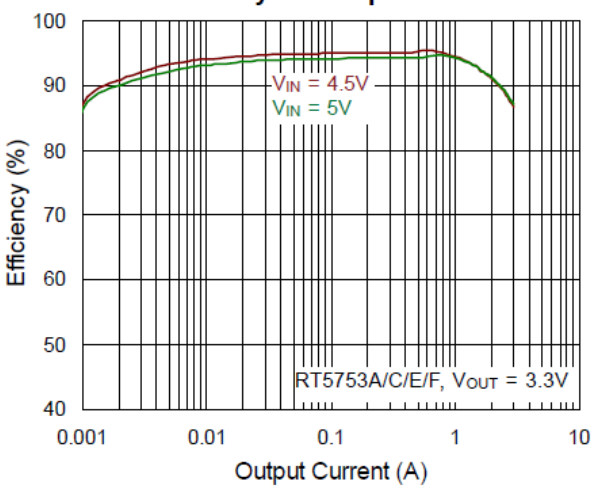

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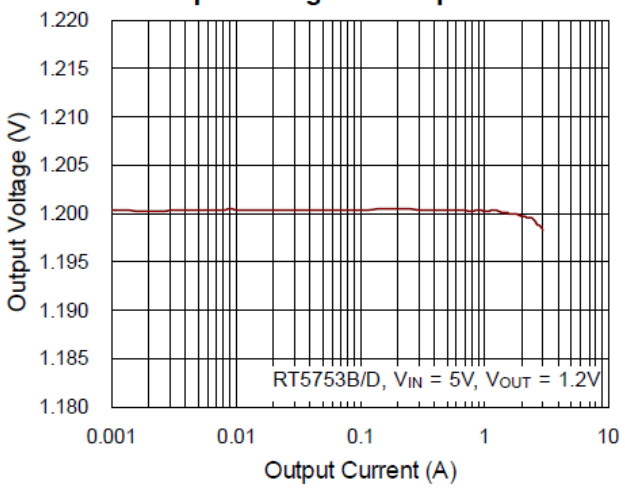
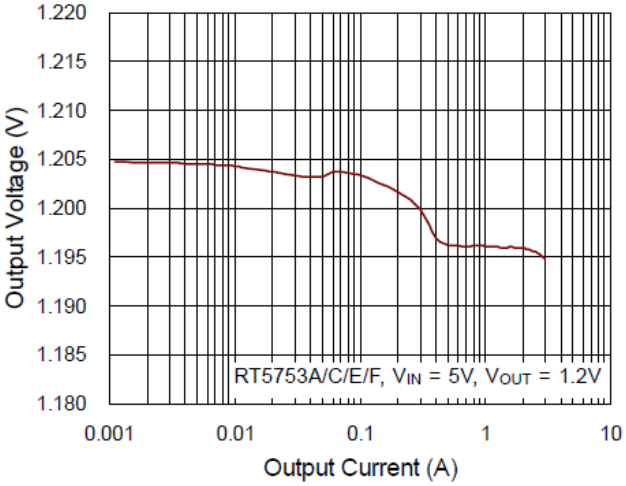
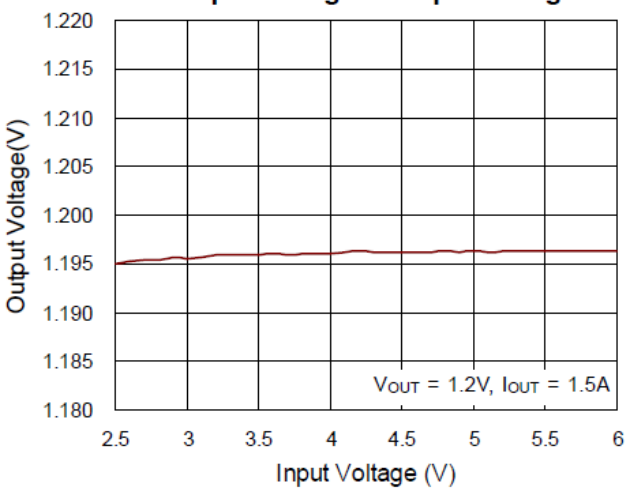
Output Voltage vs. Output Current



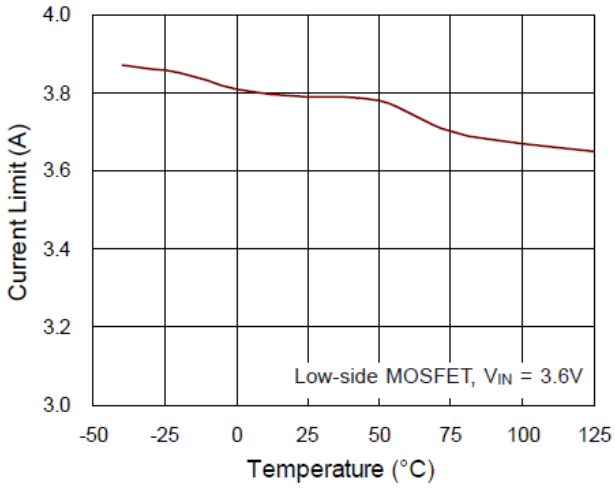
Output Voltage vs. Output Current



Output Voltage vs. Input Voltage



Current Limit vs. Temperature



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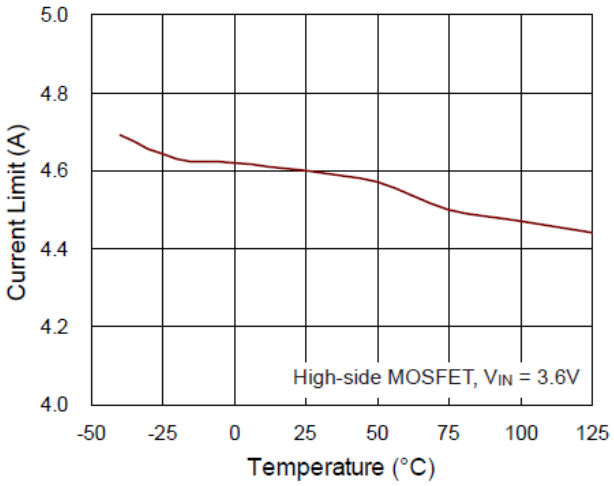
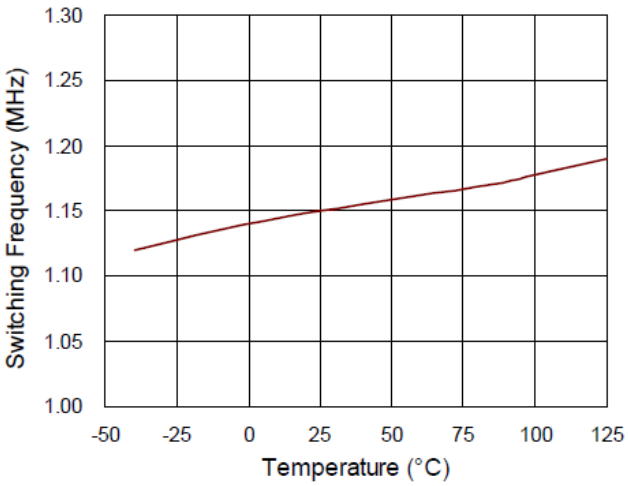


Switching Frequency vs. Temperature



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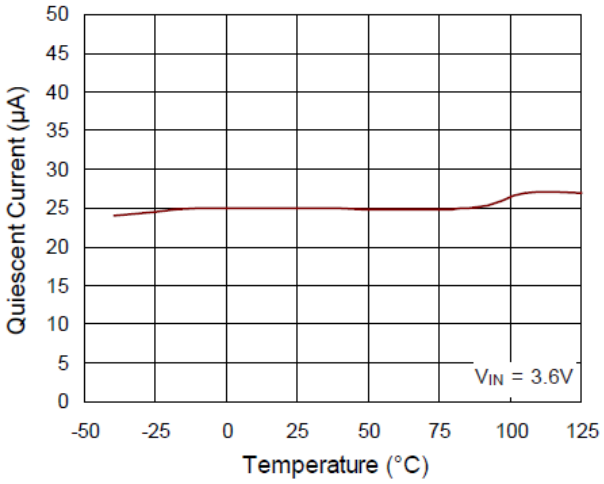
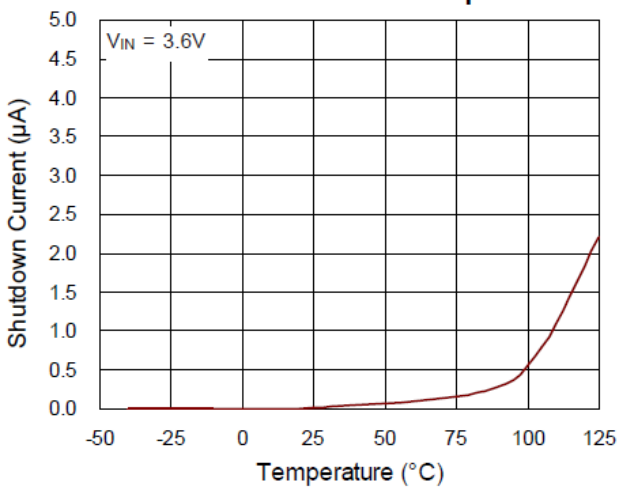
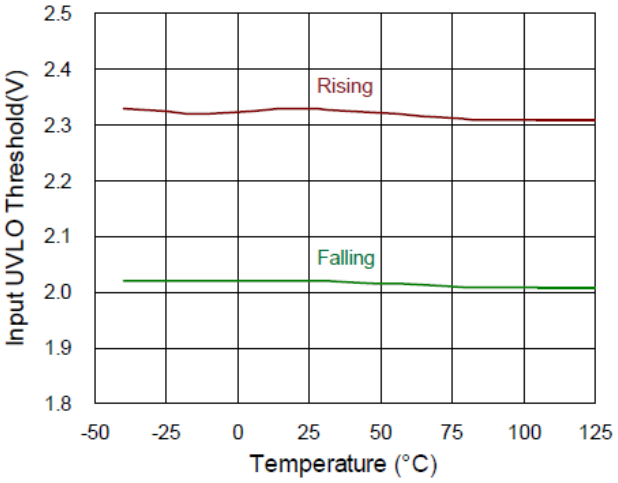
Quiescent Current vs. Temperature



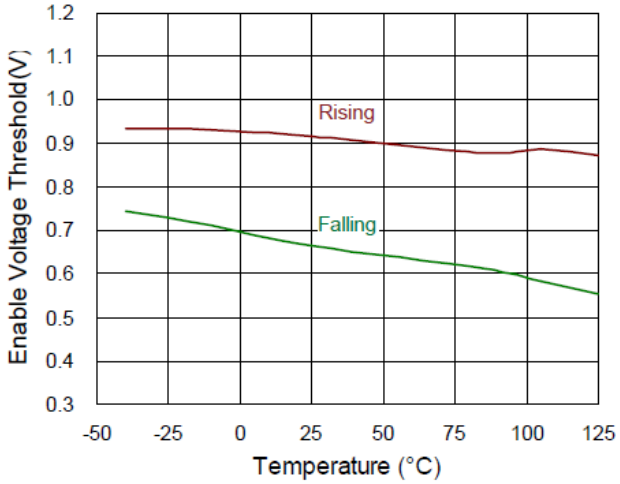
Shutdown Current vs. Temperature



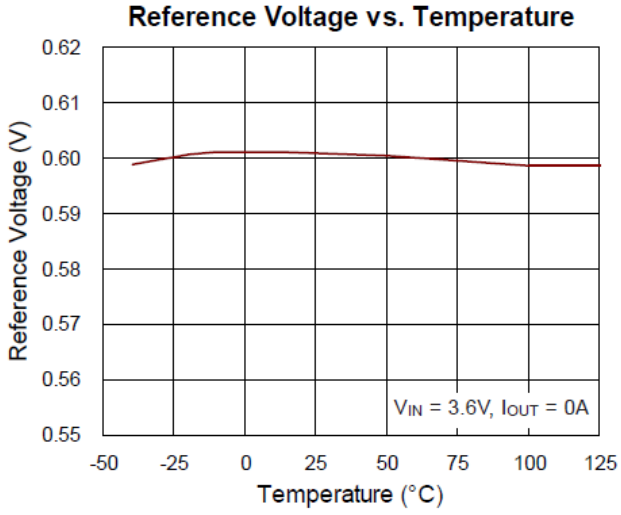
Input UVLO Threshold vs. Temperature



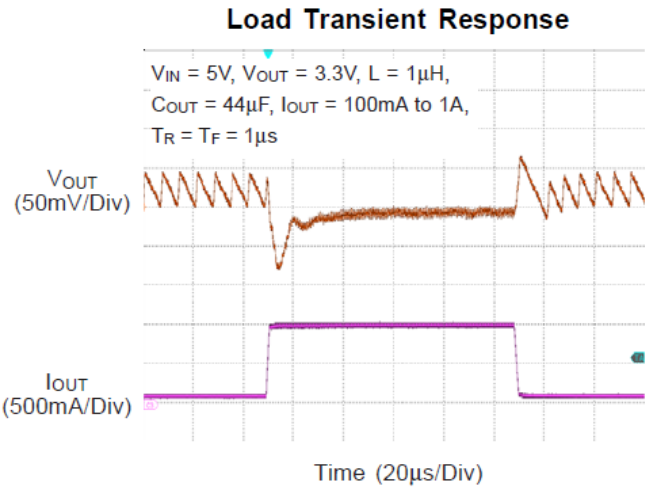
Enable Voltage Threshold vs. Temperature



Reference Voltage vs. Temperature



Load Transient Response



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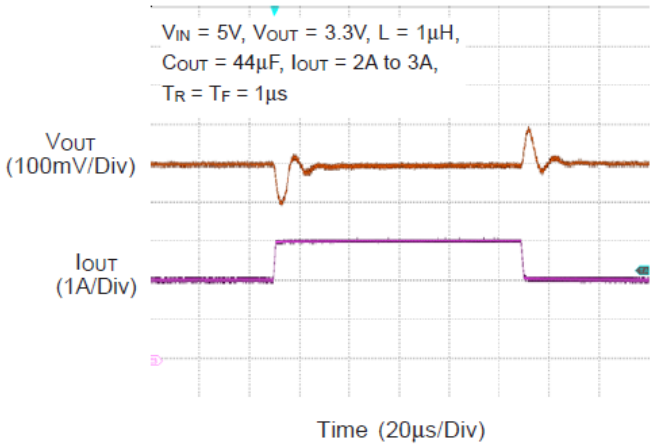
Load Transient Response



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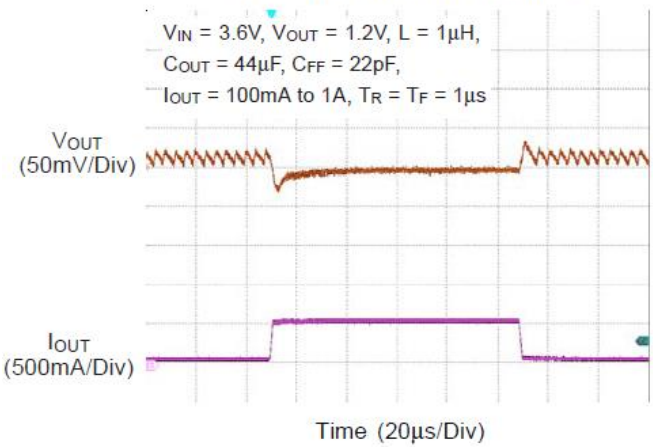

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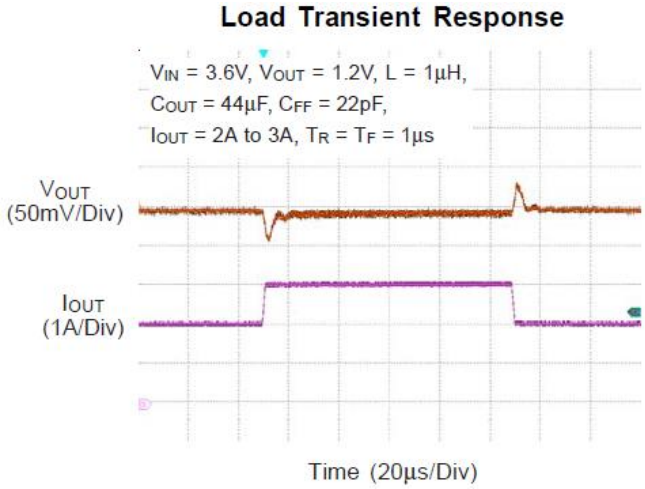
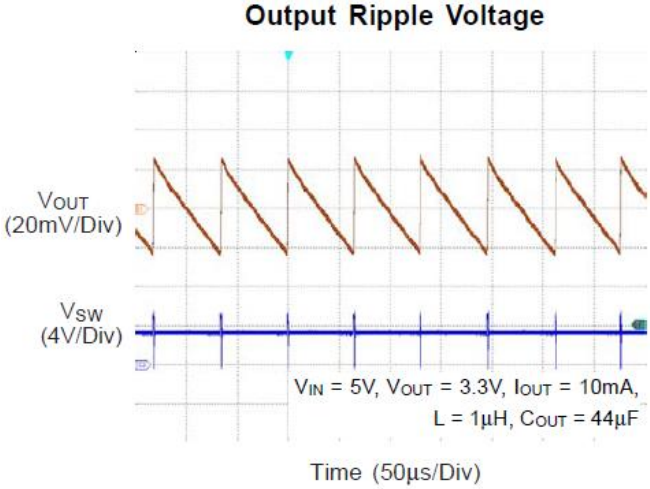


Output Ripple Voltage



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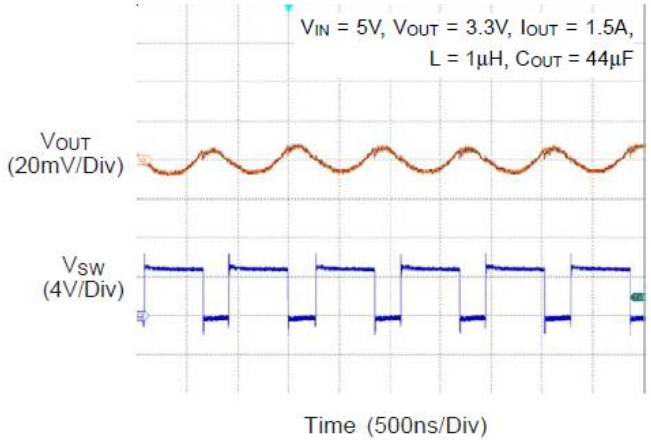

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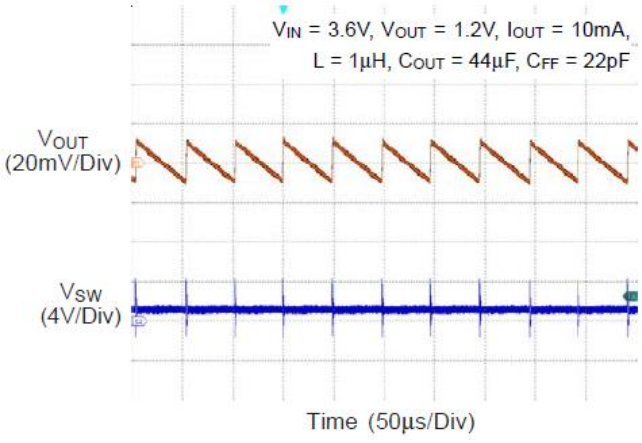

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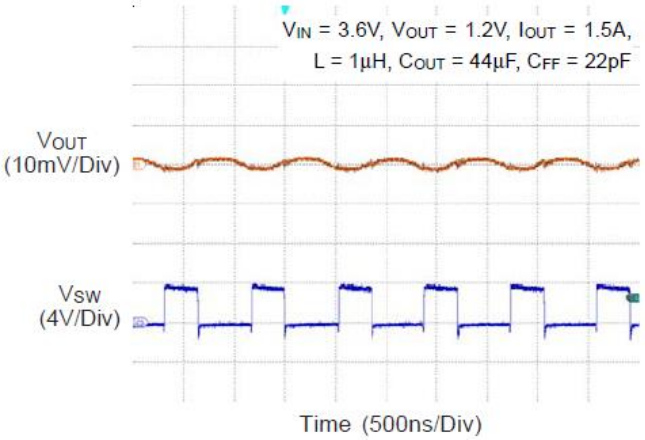
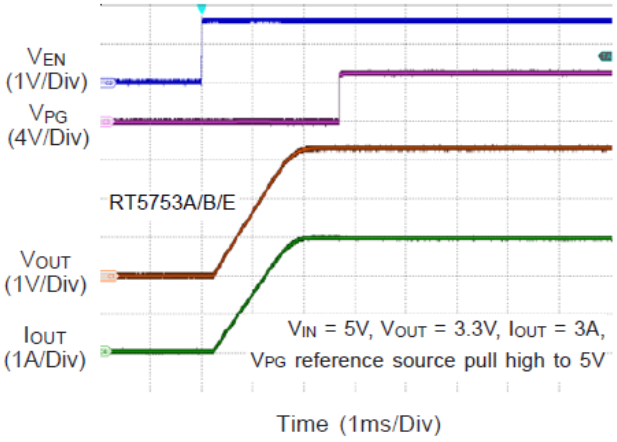
Output Ripple Voltage



Power On from EN



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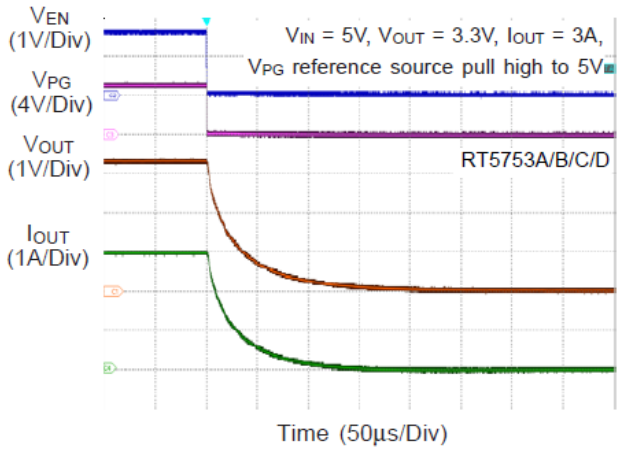
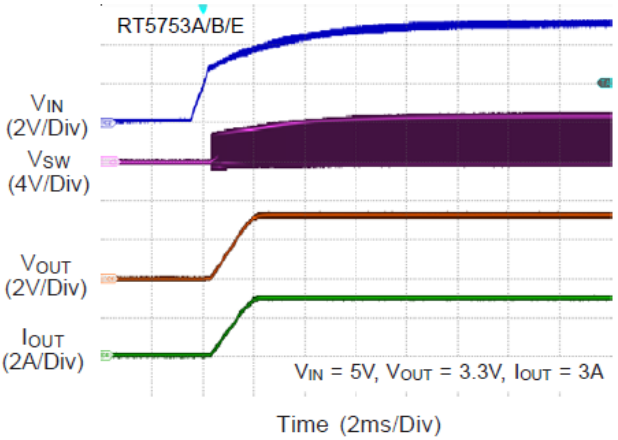


Power On from VIN



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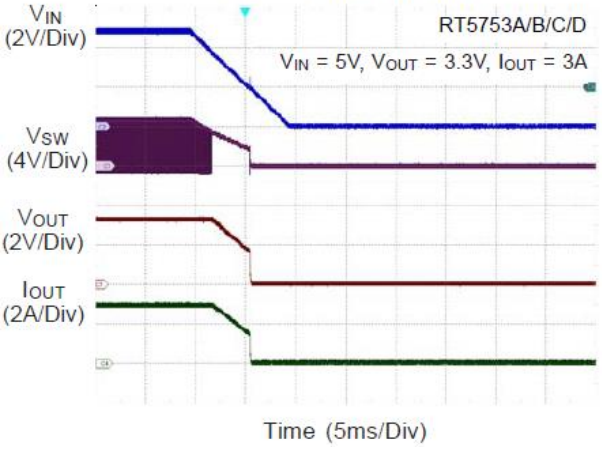
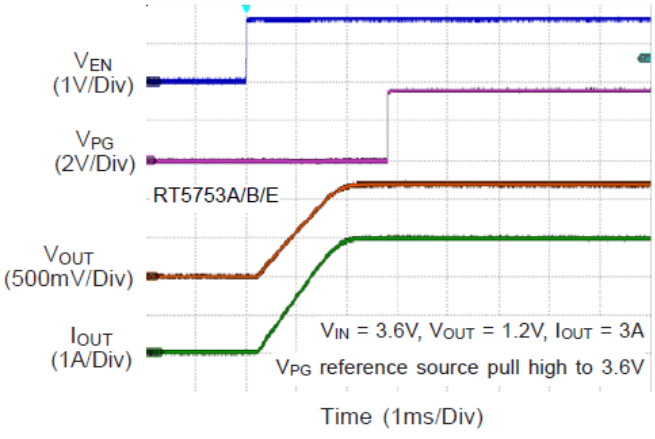


Power On from EN



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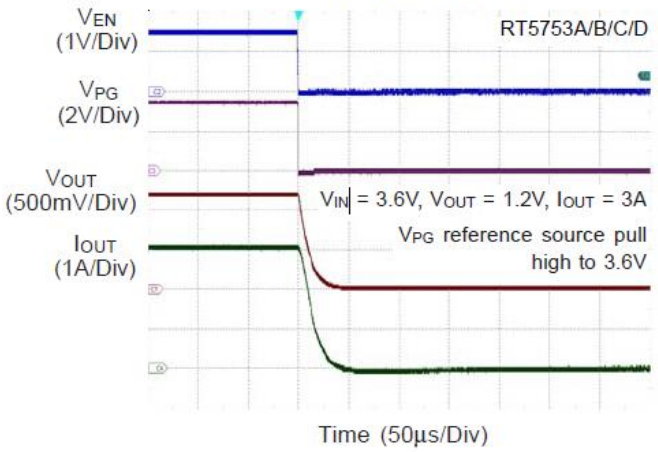
Power Off from EN



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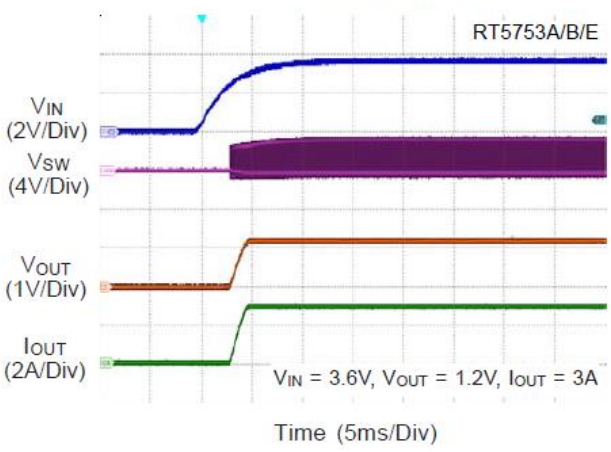

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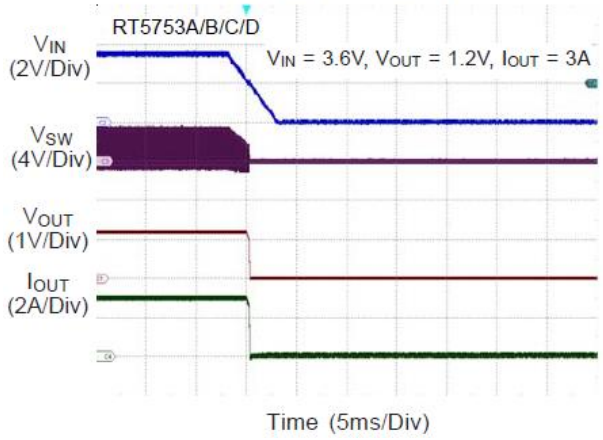

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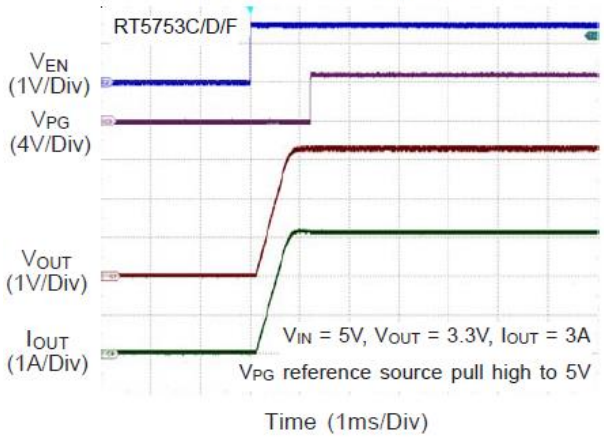

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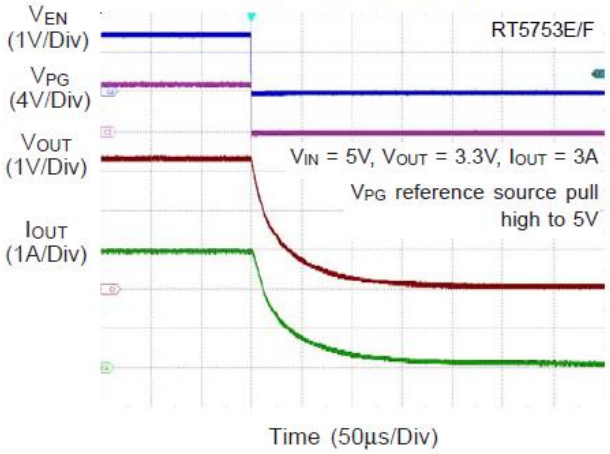
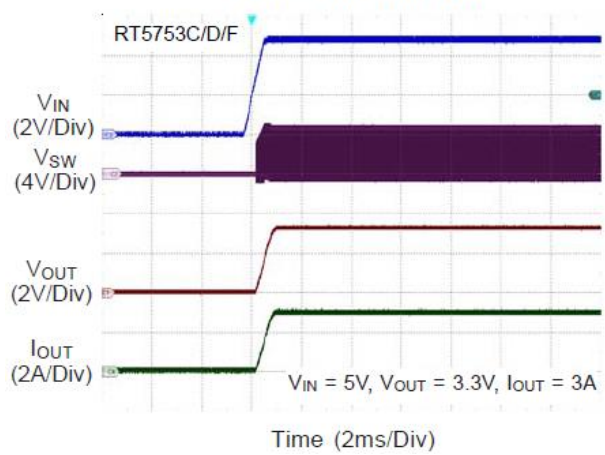


Power On from VIN



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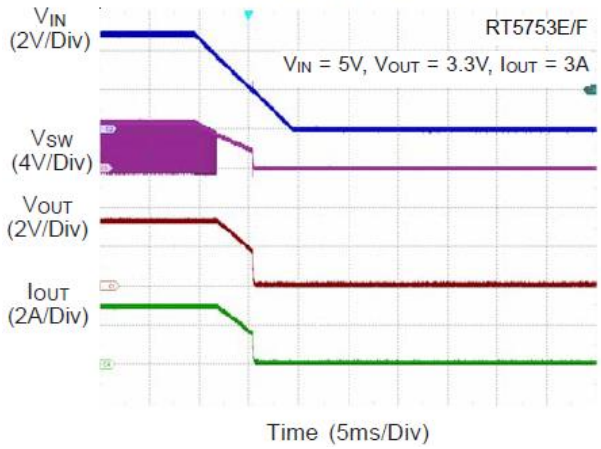
Power Off from VIN



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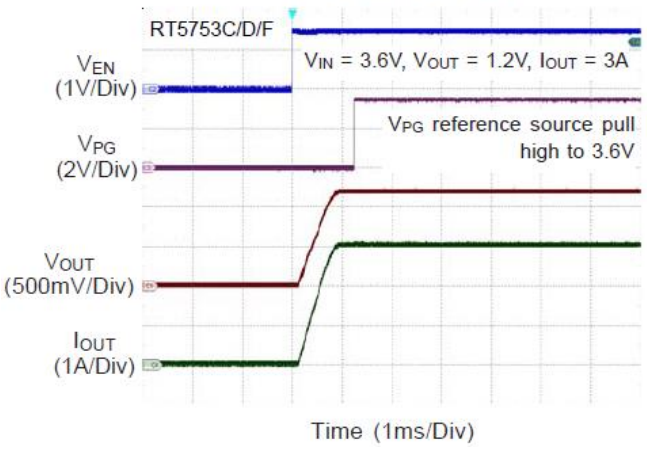

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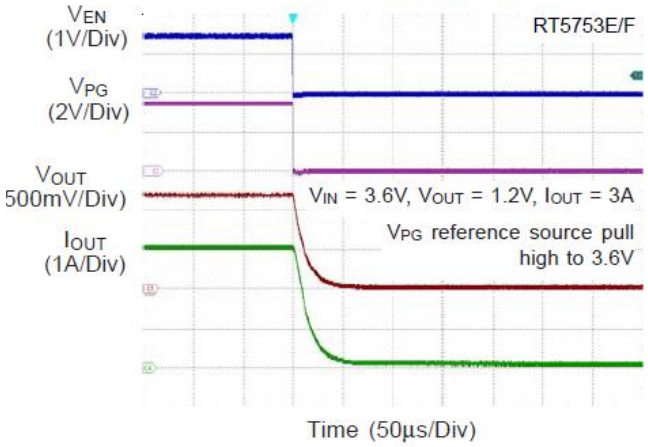
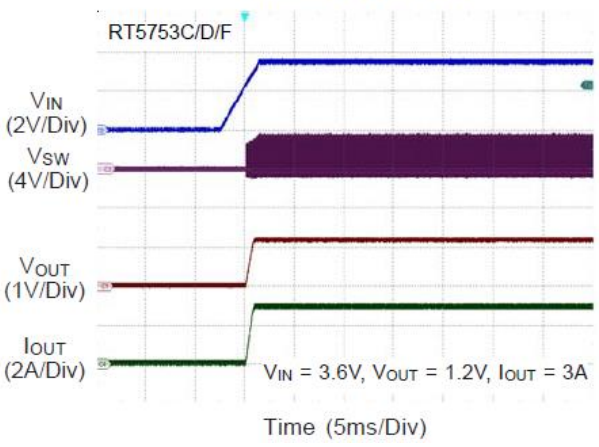
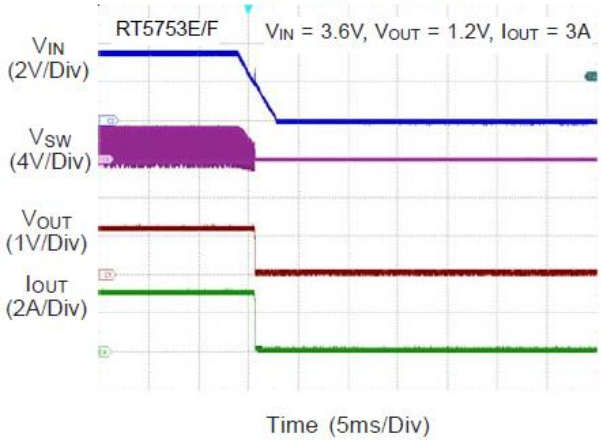


Power On from VIN



Power Off from VIN



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17 Operation

The RT5753 is a high-efficiency, synchronous step-down converter that delivers up to 3A output current from a 2.5V to 6V input supply.

17.1 Advanced Constant On-Time Control and PWM Operation

The RT5753 adopts ACOT® control for its ultrafast transient response, low external component count, and stability with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (90ns, typical) has timed out, and the inductor current is below the current-limit threshold, the internal on-time one-shot circuitry is triggered, and the high-side switch is turned on. Since the minimum off-time is short, the device exhibits an ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to the input voltage and directly proportional to the output voltage to achieve a pseudo fixed frequency over the input voltage range. After the on-time one-shot timer expires, the high-side switch is turned off and the low-side switch is turned on until the on-time one-shot is triggered again. In the steady state, the error amplifier compares the feedback voltage V_{FB} and an internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new pre-determined fixed on-time will be triggered by the on-time one-shot generator.

17.2 Power Saving Mode

The RT5753A/C/E/F automatically enters power saving mode (PSM) at light loads to maintain high efficiency. As the load current decreases and eventually the inductor current ripple valley touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes, the low-side switch is turned off when the zero inductor current is detected. As the load current further decreases, it takes longer to discharge the output capacitor to the level that requires the next on-time. The switching frequency decreases and is proportional to the load current to maintain high efficiency at light loads.

17.3 Enable Control

The RT5753 provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below the falling threshold (V_{EN_F}) of the enable input (EN), the converter will disable the output voltage, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above the VIN undervoltage-lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (15μA or below). If the EN voltage rises above the rising threshold voltage (V_{EN_R}) while the V_{IN} voltage is higher than the UVLO threshold, the device will be turned on, that is, switching is enabled and the soft-start sequence is initiated.

17.4 Soft-Start Function

The RT5753 provides an internal soft-start (SS) feature to control inrush current. At power-up, the internal capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching, and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth startup from a pre-biased output. The output voltage starts to rise in 220μs/130μs (typical) from EN rising, and the soft-start ramp-up time (0% V_{OUT} to 95% V_{OUT}) is 1.5ms/750μs (typical).

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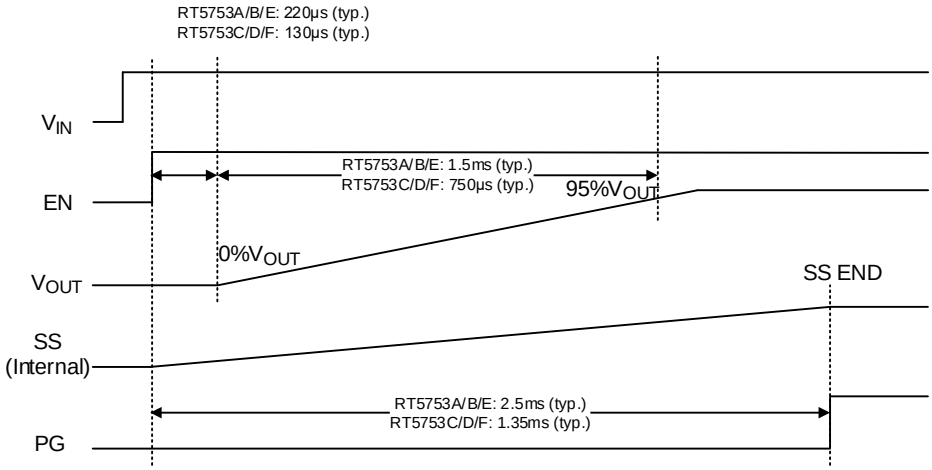

Figure 1. Start-Up Sequence

17.5 Maximum Duty Cycle Operation

The RT5753 is designed to operate in dropout at a high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than the minimum off-time, the RT5753 starts to enable the skip off-time function and keeps the high-side MOSFET switch on continuously. The RT5753 implements the skip off-time function to achieve a high duty cycle approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application when the input voltage momentarily falls to the normal output voltage requirement. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

17.6 Power-Good Indication

The RT5753 features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of the comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Connect the PG pin to VIN or an external voltage source below 6V through a pull-up resistor. When the VIN voltage rises above V_{UVLO}, the power-good function is activated. After soft-start is finished, the PG pin is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high. When V_{FB} falls short of the power-good low threshold (V_{TH_PGHL}) (typically 85% of the reference voltage), the PG pin will be pulled low. Once started up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device will pull the PG pin low. The power-good indication profile is shown below:

Table 3. PG Pin Status

Conditions		PG Pin
Enable	$V_{EN} > V_{EN_H}$, $V_{FB} > V_{TH_PGLH}$	High Impedance
	$V_{EN} > V_{EN_H}$, $V_{FB} < V_{TH_PGHL}$	Low
Shutdown	$V_{EN} < V_{EN_L}$	Low
OTP	$T_J > T_{SD}$	Low

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17.7 Input Undervoltage-Lockout

In addition to the EN pin, the RT5753 also provides enable control through the VIN pin. If V_{EN} rises above V_{EN_R} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. This ensures that the internal regulator is ready, preventing operation with not-fully-enhanced internal MOSFET switches. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume normal operation with a complete soft-start.

17.8 Current-Limit Protection

The RT5753 features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs, preventing the device from catastrophic damage in an output short circuit, overcurrent, or inductor saturation. The high-side MOSFET current-limit protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch current limit (I_{LIM_H}) after a certain delay when the high-side switch is turned on each cycle. If a current-limit condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current from exceeding the high-side current limit. The low-side MOSFET current-limit protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch current limit threshold (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit threshold (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output undervoltage protection threshold, the IC will stop switching to avoid excessive heat.

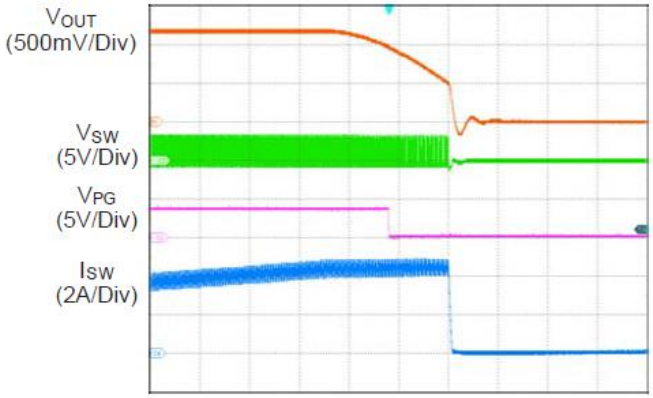

Figure 2. Current-Limit Protection

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17.9 Output Active Discharge

When the RT5753 is disabled by the EN pin, UVLO, or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (100Ω /50Ω) connected to ground. This function prevents the reverse current flow from the output capacitors to the input capacitors once the input voltage collapses. It does not need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

17.10 Output Undervoltage Protection

The RT5753 includes output undervoltage protection (UVP) against overload or short-circuit conditions by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection threshold (typically 40% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RT5753 will enter output undervoltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF} (5ms/2.5ms, typical), and then attempt to recover automatically for t_{HICCUP_ON} 1ms/0.5ms, typical). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, this auto-recovery cycle will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short-circuit condition is removed. A short-circuit protection and recovery profile is shown below.

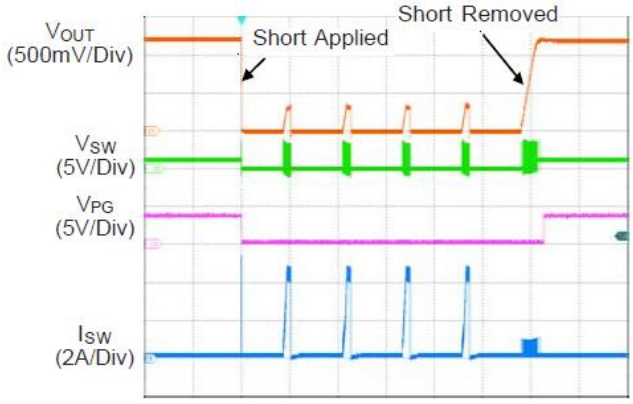

Figure 3. Short-Circuit Protection and Recovery

17.11 Output Overvoltage Protection

The RT5753AL/BL/CL/DL/EL/FL includes an output overvoltage protection (OVP) circuit to limit output voltage and minimize output voltage overshoot. If the V_{FB} goes above 120% of the reference voltage, the high-side MOSFET will be forced off to limit the output voltage, and then the IC will enter latch-off mode.

17.12 Over-Temperature Protection

The RT5753 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds an over-temperature protection threshold (T_{OTP}). Once the junction temperature cools down by an over-temperature protection hysteresis (ΔT_{OPT_HYS}), the IC will resume normal operation with a complete soft-start. Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

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17.13 Negative Overcurrent Limit

The RT5753B/D is the part that is forced to operate in PWM and allows negative current operation. In the case of PWM operation, high negative current may be generated if an external power source is unexpectedly tied to the output terminal. To mitigate this risk, the internal circuit monitors negative current in each on-time interval of the low-side MOSFET and compares it with the NOC threshold. Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET is turned on to discharge the energy of the output inductor. This behavior keeps the valley of negative current at the NOC threshold to protect the low-side MOSFET. However, the negative current cannot be limited at the NOC threshold once the minimum off-time is reached.

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18 Application Information

(Note 8)

The output stage of a synchronous buck converter, consisting of an inductor and a capacitor, stores and delivers energy to the load. They form a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

18.1 Inductor Selection

The inductor selection involves trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR). A good compromise between size and loss is to choose the peak-to-peak ripple current to be equal to 20% to 50% of the IC's rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L_PEAK} = I_{OUT_MAX} + \frac{1}{2}\Delta I_L$$

$I_{L(PEAK)}$ should not exceed the minimum value of the IC's upper current limit level. Besides, the current flowing through the inductor is the inductor ripple current plus the output current. During power-up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

For the selected inductor, the inductor's saturation and thermal rating should meet or exceed the ripple current (ΔI_L). For a more conservative approach, the rating for inductor saturation current must be equal to or greater than the switch current limit of the device rather than the inductor peak current.

For EMI-sensitive applications, choosing a shielding type inductor is preferred.

18.2 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The waveform of C_{IN} ripple voltage and ripple current are shown in Figure 4. The peak-to-peak voltage ripple on the input capacitor can be estimated using the equation below:

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

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For ceramic capacitors, the equivalent series resistance (ESR) is very low, so the ripple caused by ESR can be ignored, and the minimum input capacitance can be estimated using the following equation:

$$C_{IN_MIN} = I_{OUT_MAX} \times \frac{D(1-D)}{\Delta V_{CIN_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} is the maximum input ripple voltage.

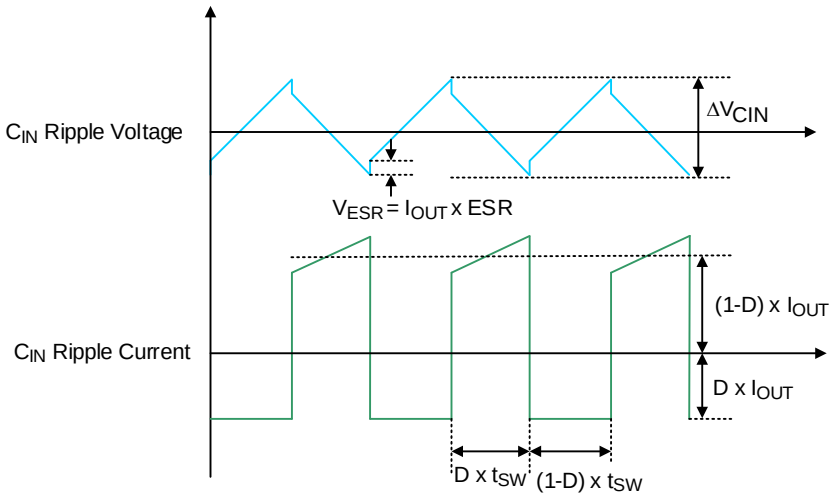

Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current:

$$I_{RMS} \cong I_{OUT_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worst-case $I_{RMS} \approx I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further de-rate the capacitor or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height, and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of their small size, robustness, and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high-quality (under-damped) tank circuit. If the RT5753 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitor of 0.1μF should be placed close to the VIN and GND pins. This capacitor should be 0402 or 0603 in size.

18.3 Output Capacitor Selection

The RT5753 is optimized for ceramic output capacitors, and the best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient

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response requirements for sag (undershoot on load apply) and soar (overshoot on load release).

18.4 Output Voltage Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance C_{OUT} and its equivalent series resistance R_{ESR} must be taken into consideration. The output peak-to-peak ripple voltage V_{RIPPLE}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple $V_{RIPPLE(ESR)}$ and capacitive ripple $V_{RIPPLE(C)}$, and can be expressed as follows:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both components need to be considered due to the extremely low ESR and relatively small capacitance.

18.5 Output Transient Undershoot and Overshoot

In addition to the voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick, and output transients are usually small. The following paragraph details how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot are influenced by two main factors: the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formula to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$V_{ESR_STEP} = \Delta I_{OUT} \times R_{ESR}$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as follows:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect this since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as follows:

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

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Because some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR step up or down should be taken into consideration.

18.6 Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB, as shown in Figure 5. The output voltage is set according to the following equation:

$V_{OUT} = 0.6V \times (1 + R_{FB1}/R_{FB2})$

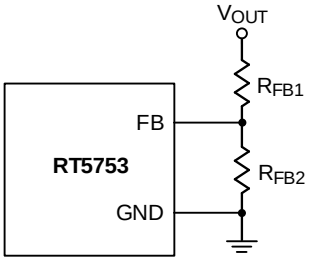

Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with 1% or better tolerance.

18.7 EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 6, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 7. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device from being enabled when VIN is smaller than the VOUT target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage-lockout threshold, as shown in Figure 8.

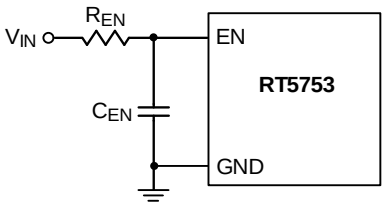

Figure 6. Enable Timing Control

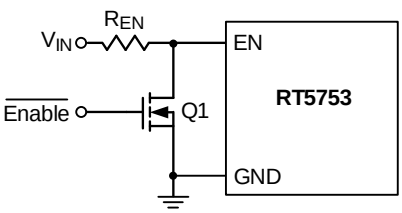

Figure 7. Logic Control for the EN Pin

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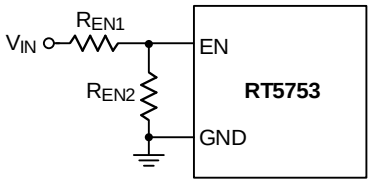

Figure 8. Resistive Divider for Undervoltage-Lockout Threshold Setting

18.8 Power-Good Output

The PG pin is an open-drain power-good indication output and should be connected to an external voltage source through a pull-up resistor. The external voltage source can be an external voltage supply below 6V, V_{CC}, or the output of the RT5753 if the output voltage is regulated under 6V. It is recommended to connect a 100kΩ resistor between the external voltage source and the PG pin.

18.9 Feedforward Capacitor (C_{FF})

The RT5753 is optimized for low duty-cycle applications, and its control loop is stable with low ESR ceramic output capacitors. This optimization makes it easier for the circuit to achieve stability with reasonable output capacitors. However, it also narrows the optimization of transient responses of the converter. In higher duty-cycle applications (higher output voltages or lower input voltages), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Because of the large internal ripple in this condition, the response may become too slow and may show an under-damped response. This can cause some ringing in the output and is especially visible in higher output voltage applications where the duty cycle is high. The feedback network attenuation is large, adding to the delay. As shown in Figure 9, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

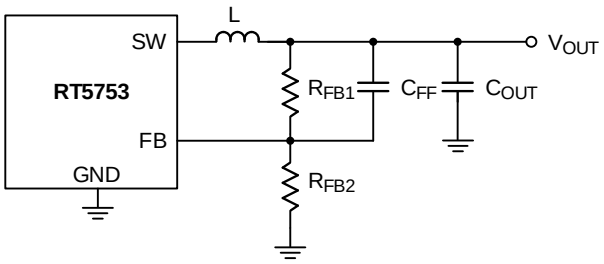

Figure 9. Feedback Loop with Feedforward Capacitor

Loop stability can be checked by viewing the load transient response. A load step with a speed that exceeds the converter bandwidth must be applied. For ACOT®, loop bandwidth can be range from100 to 200kHz, so a load step with a 500ns maximum rise time (di/dt≈2A/μs) ensures that the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current-limit threshold. A load transient from 30% to 60% of the maximum load is reasonable, as shown in Figure 10.

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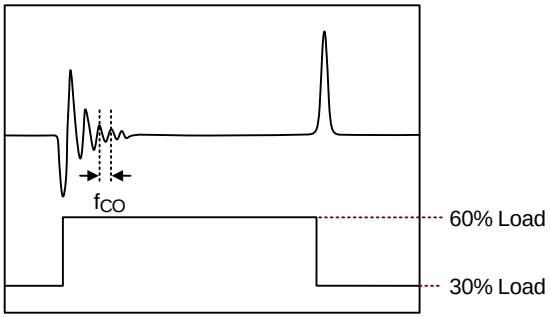

Figure 10. Example of Measuring the Converter f_{CO} by Fast Load Transient

C_{FF} can be calculated based on the following equation:

$$C_{FF} = \frac{1}{2\pi \times f_{co}} \times \sqrt{\frac{1}{R_{FB1}} \times \left(\frac{1}{R_{FB1}} + \frac{1}{R_{FB2}} \right)}$$

Note that after defining the C_{FF}, you should also check the load regulation because the feedforward capacitor might inject an offset voltage into V_{OUT}, causing V_{OUT} inaccuracy. If the output voltage is out of specification due to the calculated C_{FF}, decrease the value of the feedforward capacitor C_{FF}.

Figure 11 shows the transient performance with and without the feedforward capacitor.

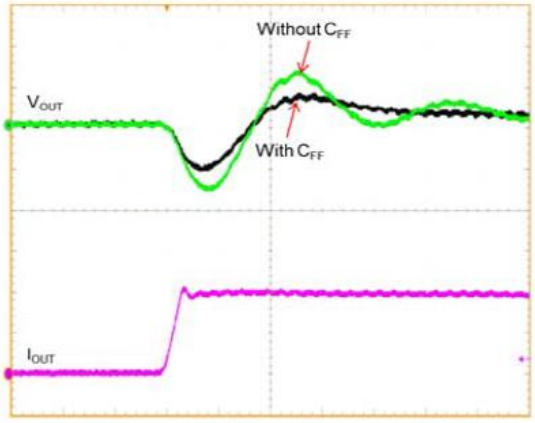

Figure 11. Load Transient Response with and without Feedforward Capactior

18.10 Thermal Considerations

In many applications, the RT5753 does not generate much heat due to its high efficiency and the low thermal resistance of its WDFN-8L 2x2 and WDFN-8SL 2x2 packages. However, in applications where the RT5753 operates at a high ambient temperature, high input voltage, or high switching frequency, the generated heat may exceed the maximum junction temperature of the part. The junction temperature should never exceed the absolute maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 150°C, the RT5753 stops switching the power MOSFETs until the temperature cools down by 20°C.

The maximum power dissipation can be calculated by the following formula:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA(EFFECTIVE)}$

Where $T_{J(MAX)}$ is the maximum junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient temperature, and $\theta_{JA(EFFECTIVE)}$ is the system-level junction-to-ambient thermal resistance. It can be estimated from thermal modeling or

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measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply setting $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RT5753 is used in applications where V_{IN} = 5V, I_{OUT} = 3A, f_{SW} = 1.2MHz, V_{OUT} = 1.2V. The efficiency at 1.2V and 3A is 74.2% by using WE-74437324010 (1μH, 22mΩ DCR) as the inductor and measured at room temperature. The core loss, 16.5mΩ, can be obtained from its website in this case. In this case, the power dissipation of the RT5753 is

$$P_{D,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^2 \times DCR + P_{CORE}\right) = 1.03W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 59.64°C/W by using the RT5753 evaluation board with a 4-layer PCB, all layers with 1 oz. Cu, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

T_J = 1.03W x 59.64°C/W + 25°C = 86.4°C

18.11 Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path comprising the input capacitor, high-side MOSFET, inductor, and output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and PGND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT5753.
- The SW node has a high-frequency voltage swing and should be kept to a small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect the feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, design a wide and thick plane for the PGND pin or add a lot of vias to the GND plane.
- AGND and PGND should be connected with a via at only one point to reduce circulating currents.
- An example of a PCB layout guide is shown in Figure 12.

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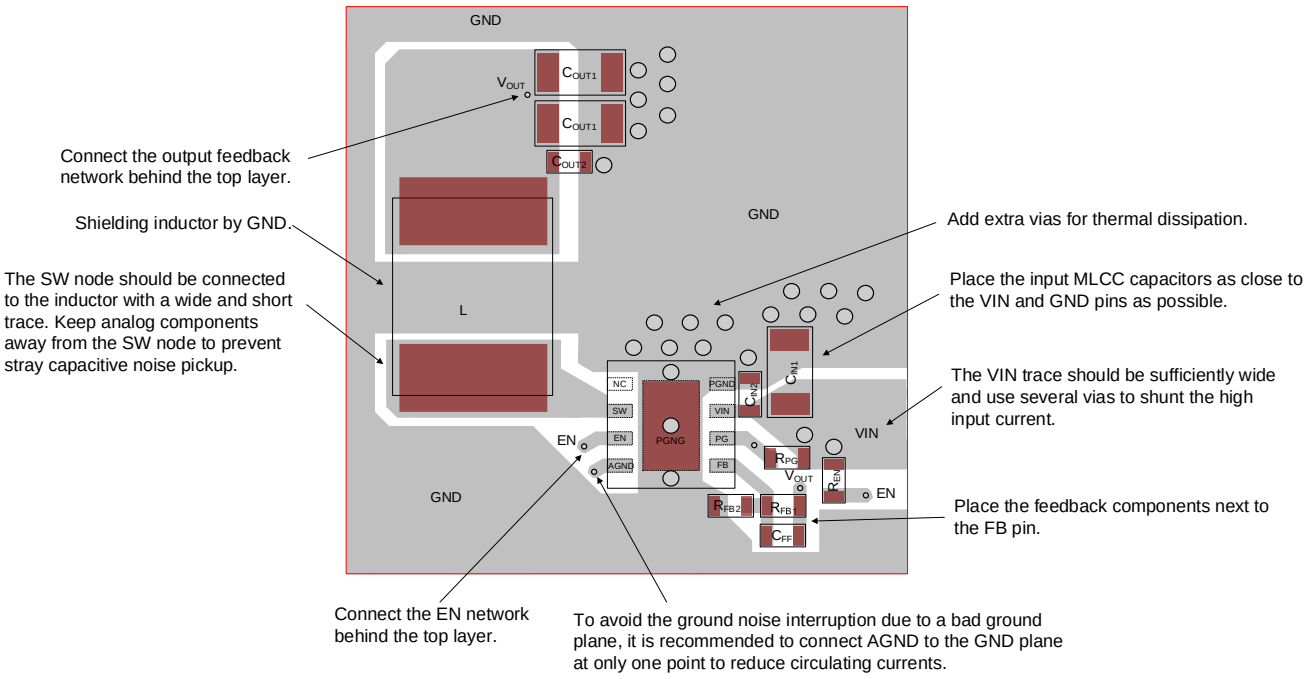

Figure 12. Layout Guide

Note 8. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

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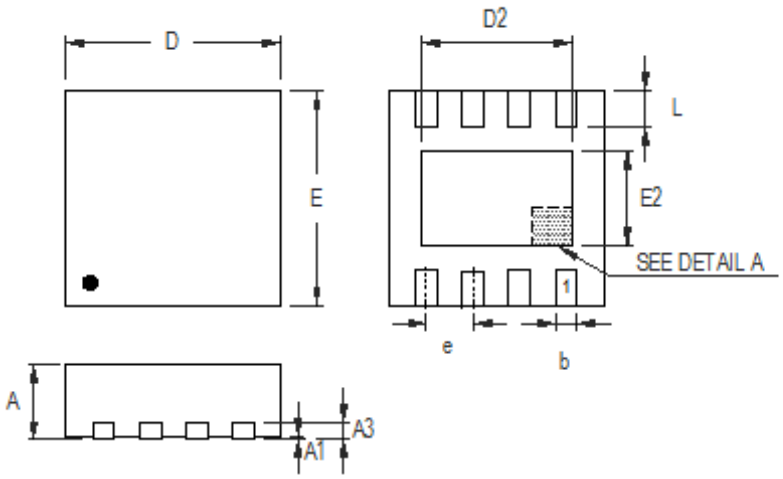
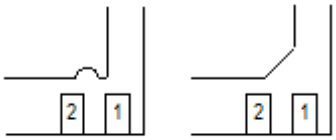
19 Outline Dimension

19.1 WDFN-8L 2x2





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

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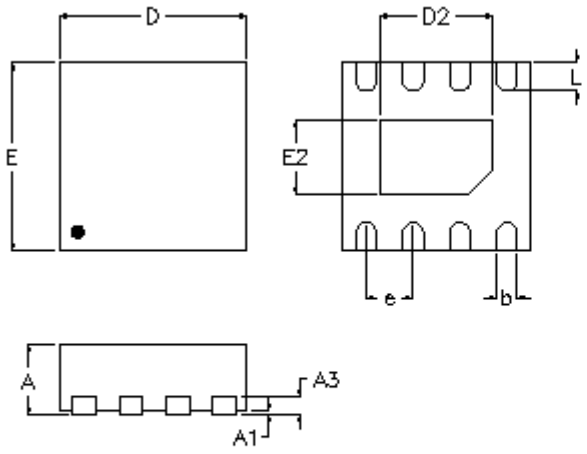
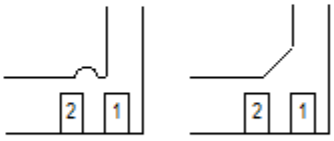
19.2 WDFN-8SL 2x2





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

W-Type 8SL DFN 2x2 Package

Note 9. The package of the RT5753 uses Option2.

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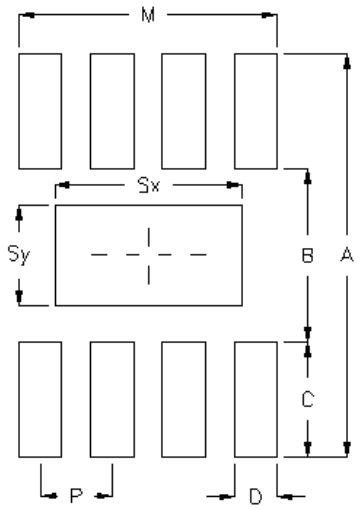
20 Footprint Information

20.1 WDFN-8L 2x2



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8	8	0.50	2.80	1.20	0.80	0.30	1.30	0.70	1.80	±0.05

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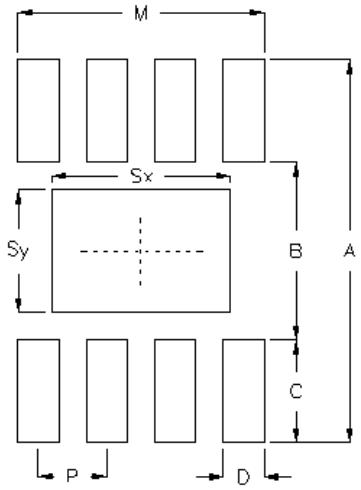
20.2 WDFN-8SL 2x2



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8S	Option1	8	0.50	2.80	1.30	0.75	0.30	1.30	0.90	1.80	±0.05
	Option2							1.60	0.90		

Note 10. The package of the RT5753 uses Option2.

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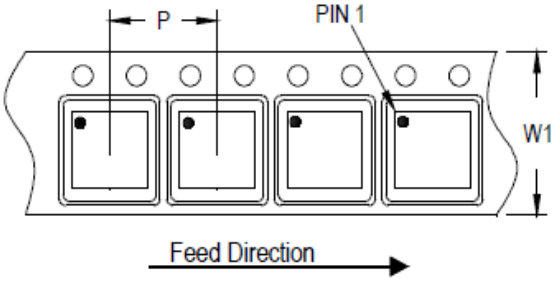
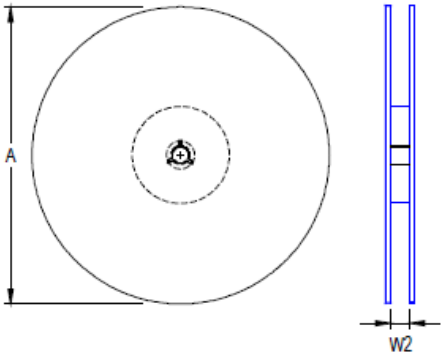
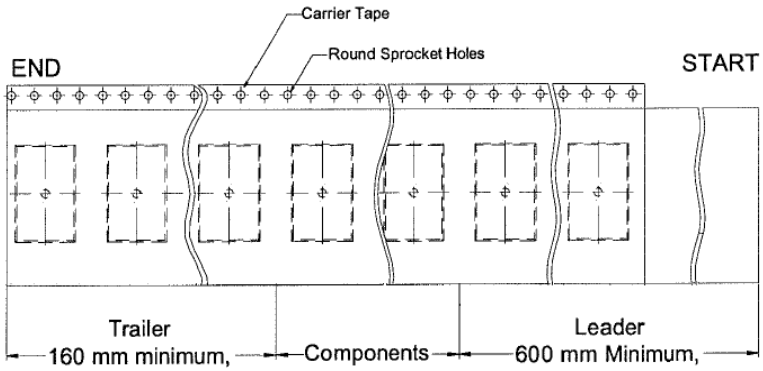
21 Packing Information

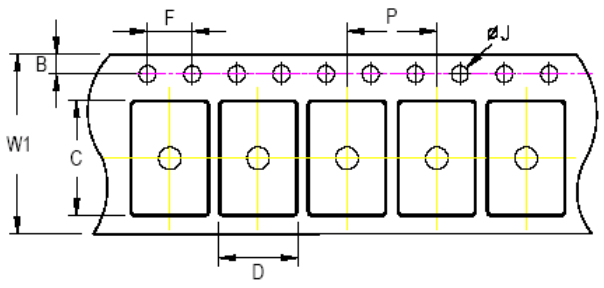
21.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 2x2	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

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21.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	Reel 7”	4	3 reels per inner box **Box A**
2	HIC & Desiccant (1 Unit) inside	5	12 inner boxes per outer box
3	Caution label is on backside of Al bag	6	Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 2x2	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

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21.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

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22 Datasheet Revision History

Version	Date	Description	Item
04	2023/1/10	Modify	*Add RT5753EL, RT5753FL* *General Description on page 1* *Features on page 1* *Simplified Application Circuit on page 1* *Ordering Information on page 2* *Marking Information on page 4* *Functional Block Diagram on page 5* *Operation on page 6, 7, 8, 9* *Electrical Characteristics on page 11, 12* *Typical Application Circuit on page 13* *Typical Operating Characteristics on page 14* *Application Information on page 21*
06	2023/11/7	Modify	*Electrical Characteristics on page 11* *Typical Application Circuit on page 17*
06	2024/10/30	Modify	*General Description on page 1* Features *on page 1* *Ordering Information on page 2* *Electrical Characteristics on page 7, 8* *Operation on page 17 to 21* *Application Information on page 22 to 28* *Packing Information on page 34 to 36* - Added packing information

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