3A, 1.2MHz, 6V Synchronous Step-Down Converter In WDFN-8L 2x2

General Description

The RT5753 is a simple, easy-to-use, 3A synchronous step-down DC-DC converter with an input supply voltage range from 2.5V to 6V. The device builds in an accurate 0.6V reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in WDFN-8L 2x2 and WDFN-8SL 2x2 packages.

The RT5753 adopts Advanced Constant On-Time (ACOT®) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT5753A/C/E/F operates in automatic PSM that maintains high efficiency during light load operation. The RT5753B/D operates in Forced PWM that helps to meet tight voltage regulation accuracy requirements.

The RT5753 senses both FETs current for a robust overcurrent protection. The device features cycle-by-cycle current limit protection which prevents the device from the catastrophic damage in output short circuit, over current or inductor saturation. A built-in soft-start function prevents inrush current during start-up. The device also includes input undervoltage lockout, output undervoltage protection, overvoltage protection (RT5753AL/BL/CL/DL/EL/FL) and over-temperature protection to provide safe and smooth operation in all operating conditions.

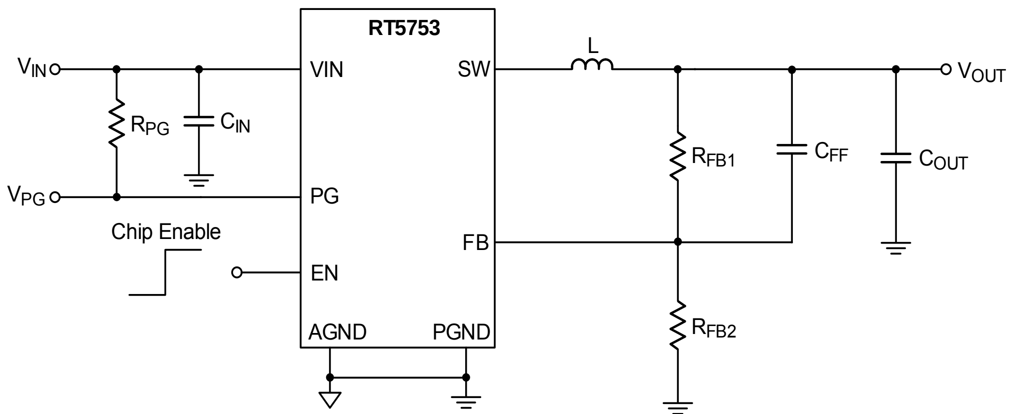
Features

- **Input Voltage Range from 2.5V to 6V**
- **Integrated 100mΩ and 70mΩ FETs**
- **100% Duty Cycle for Lowest Dropout**
- **Internal Reference Voltage with 1% Accuracy 1.2MHz Typical Switching Frequency**
- **Power Saving Mode for Light Loads (RT5753A/C/E/F)**
- **Advanced Constant On-Time (ACOT®) Control**
- **Internal Soft-Start (1.5ms/750μs)**
- **Enable Control Input**
- **Power Good Indicator**
- **Both FETs Overcurrent Protection**
- **Negative Overcurrent Protection (RT5753B/D)**
- **Input Undervoltage Lockout Protection**
- **Output Undervoltage Protection**
- **Over-Temperature Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Mobile Phones and Handheld Devices
- STB, Cable Modem, and xDSL Platforms
- WLAN ASIC Power / Storage (SSD and HDD)
- General Purpose for POL LV Buck Converters

Simplified Application Circuit



Ordering Information

RT5753□□□□

- Package Type
  - QW : WDFN-8L 2x2 (W-Type)
  - QWA : WDFN-8SL 2x2 (W-Type) (Exposed Pad-Option 2)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- UVP Option
  - H : Hiccup (For A, B, C, D only)
  - L : Latched-Off
- PWM Operation Mode
  - A : SS TIME = 1.5m(typ.) & Automatic PSM & Rdischg = 100ohm
  - B : SS TIME = 1.5m(typ.) & Forced PWM & Rdischg = 100ohm
  - C : SS TIME = 750μs(typ.) & Automatic PSM & Rdischg = 100ohm
  - D : SS TIME = 750μs(typ.) & Forced PWM & Rdischg = 100ohm
  - E : SS TIME = 1.5m(typ.) & Automatic PSM & Rdischg = 50ohm
  - F : SS TIME = 750μs(typ.) & Automatic PSM & Rdischg = 50ohm

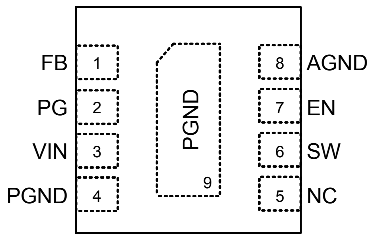
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



WDFN-8L 2x2/WDFN-8SL 2x2

Marking Information

RT5753AHGQW

54W

54 : Product Code
W : Date Code

RT5753AHGQWA

5KW

5K : Product Code
W : Date Code

RT5753ALGQW

51W

51 : Product Code
W : Date Code

RT5753ALGQWA

5JW

5J : Product Code
W : Date Code

RT5753BHGQW

4ZW

4Z : Product Code
W : Date Code

RT5753BHGQWA

5HW

5H : Product Code
W : Date Code

RT5753BLGQW

4YW

4Y : Product Code
W : Date Code

RT5753BLGQWA

5GW

5G : Product Code
W : Date Code

RT5753CHGQW

5YW

5Y : Product Code
W : Date Code

RT5753CHGQWA

62W

62 : Product Code
W : Date Code

RT5753CLGQW

5XW

5X : Product Code
W : Date Code

RT5753CLGQWA

61W

61 : Product Code
W : Date Code

RT5753DHGQW

5WW

5W : Product Code
W : Date Code

RT5753DHGQWA

60W

60 : Product Code
W : Date Code

RT5753DLGQW

5VW

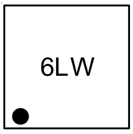
5V : Product Code
W : Date Code

RT5753DLGQWA

5ZW

5Z : Product Code
W : Date Code

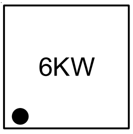
RT5753FLGQW



6L : Product Code

W : Date Code

RT5753FLGQWA



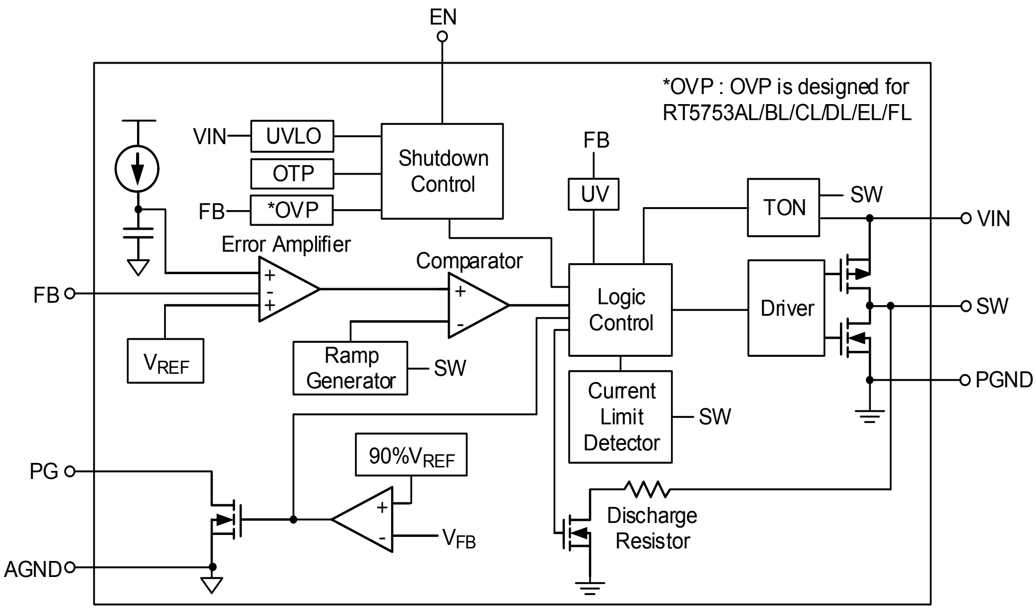
6K : Product Code

W : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	FB	Output voltage sense. Sense the output voltage at the FB pin through a resistive divider. The feedback reference voltage is 0.6V typically.
2	PG	Open-drain power-good indicator output. Once being started-up, PG will be pulled low to ground if any internal protection is triggered.
3	VIN	Power input. The input voltage range is from 2.5V to 6V. Connect a suitable input capacitor between this pin and PGND pins, usually one 22μF or higher than 22μF ceramic capacitors is recommended.
4, 9 (Exposed Pad)	PGND	Power ground. The exposed pad is internally unconnected which must be soldered to a large PCB cooper area and connected to PGND for maximum power dissipation.
5	NC	No internal connection. Keep this pin floating.
6	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor.
7	EN	Enable control input. Connect this pin to logic high enables the device and connect this pin to ground disables the device.
8	AGND	Analog ground.

Functional Block Diagram



Operation

The RT5753 is a high-efficiency, synchronous step-down DC-DC converter that delivers up to 3A output current from a 2.5V to 6V input supply.

Advanced Constant On-Time Control and PWM Operation

The RT5753 adopts ACOT® control for its ultrafast transient response, low external component counts and stable with low ESR MLCC output capacitors. When the feedback voltage falls below the feedback reference voltage, the minimum off-time one-shot (90ns, typ.) has timed out and the inductor current is below the current limit threshold, then the internal on-time one-shot circuitry is triggered and the high-side switch is turned on. Since the minimum off-time is short, the device exhibits ultrafast transient response and enables the use of smaller output capacitance.

The on-time is inversely proportional to input voltage and directly proportional to output voltage to achieve pseudo-fixed frequency over the input voltage range. After the on-time one-shot timer is expired, the high-side switch is turned off and the low-side switch is turned on until the on-time one-shot is triggered again. In the steady state, the error amplifier compares the feedback voltage V_{FB} and an internal reference voltage. If the virtual inductor current ramp voltage is lower than the output of the error amplifier, a new pre-determined fixed on-time will be triggered by the on-time one-shot generator.

Power Saving Mode

The RT5753A/C/E/F automatically enters power saving mode (PSM) at light load to maintain high efficiency. As the load current decreases and eventually the inductor current ripple valley touches the zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side switch is turned off when the zero inductor current is detected. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level that requires the next on-time. The switching frequency decreases and is proportional to the load current to maintain high efficiency at light load.

Enable Control

The RT5753 provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage (V_{EN_L}) of the enable input (EN), the converter will disable output voltage, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above VIN undervoltage lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (15μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{EN_H}) while the VIN voltage is higher than UVLO threshold, the device will be turned on, that is, switching being enabled and soft-start sequence being initiated.

Soft-Start (SS)

The RT5753 provides an internal soft-start feature for inrush control. At power up, the internal capacitor is charged by an internal current source to generate a soft-start ramp voltage as a reference voltage to the PWM comparator. The device will initiate switching and the output voltage will smoothly ramp up to its targeted regulation voltage only after this ramp voltage is greater than the feedback voltage V_{FB} to ensure the converters have a smooth start-up from pre-biased output. The output voltage starts to rise in 220μs/130μs (Typ.) from EN rising, and the soft-start ramp-up time (0%V_{OUT} to 95%V_{OUT}) is 1.5ms/750μs (Typ.).

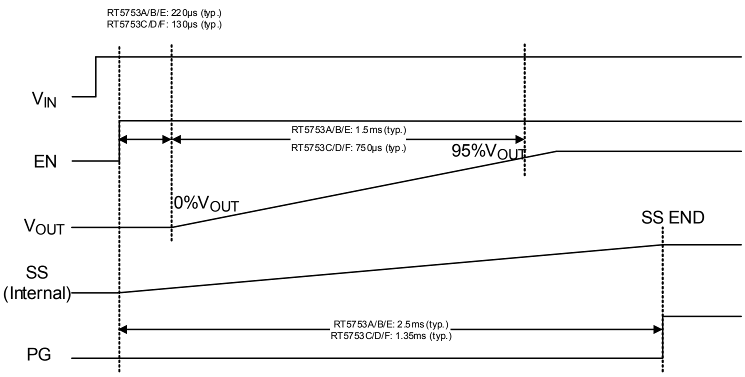


Figure 1. Start-Up Sequence

Maximum Duty Cycle Operation

The RT5753 is designed to operate in dropout at the high duty cycle approaching 100%. If the operational duty cycle is large and the required off-time becomes smaller than minimum off-time, the RT5753 starts to enable skip off-time function and keeps high-side MOSFET switch on continuously. The RT5753 implements skip off-time function to achieve high duty approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application for input voltage momentarily falls down to the normal output voltage requirement. The input voltage at which the devices enter dropout changes depending on the input voltage, output voltage, switching frequency, load current, and the efficiency of the design.

Power Good Indication

The RT5753 features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to VIN or an external voltage below 6V. When VIN voltage rises above V_{UVLO}, the power-good function is activated. After soft-start is finished, the PG pin is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} rises above a power-good high threshold (V_{TH_PGLH}) (typically 90% of the reference voltage), the PG pin will be in high impedance and V_{PG} will be held high. When V_{FB} falls short of power-good low threshold (V_{TH_PGHL}) (typically 85% of the reference voltage), the PG pin will be pulled low. Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull-down device will pull the PG pin low. The power good indication profile is shown below.

Table 1. PG Pin Status

Conditions		PG Pin
Enable	$V_{EN} > V_{EN\_H}$, $V_{FB} > V_{TH\_PGLH}$	High Impedance
	$V_{EN} > V_{EN\_H}$, $V_{FB} < V_{TH\_PGHL}$	Low
Shutdown	$V_{EN} < V_{EN\_L}$	Low
OTP	$T_J > T_{SD}$	Low

Input Undervoltage Lockout

In addition to the EN pin, the RT5753 also provides enable control through the VIN pin. If V_{EN} rises above V_{ENH} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not-fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage VIN goes below the UVLO falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if VIN rises above the UVLO rising threshold (V_{UVLO}), the device will resume normal operation with a complete soft-start.

The Overcurrent Protection

The RT5753 features cycle-by-cycle current-limit protection on both the high-side and low-side MOSFETs and the protection prevents the device from the catastrophic damage in output short circuit, over current or inductor saturation.

The high-side MOSFET overcurrent protection is achieved by an internal current comparator that monitors the current in the high-side MOSFET during each on-time. The switch current is compared with the high-side switch peak-current limit (I_{LIM_H}) after a certain amount of delay when the high-side switch being turned on each cycle. If an overcurrent condition occurs, the converter will immediately turn off the high-side switch and turn on the low-side switch to prevent the inductor current from exceeding the high-side current limit.

The low-side MOSFET overcurrent protection is achieved by measuring the inductor current through the synchronous rectifier (low-side switch) during the low-side on-time. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. If the output load current exceeds the available inductor current (clamped by the low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output undervoltage protection threshold, the IC will stop switching to avoid excessive heat.

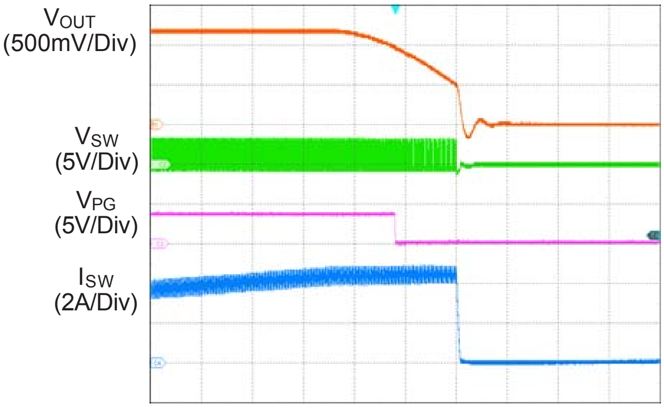


Figure 2. Overcurrent Protection

typ.), and then attempt to recover automatically for t_{HICCUP_ON} (1ms/0.5ms, typ.). Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed. A short-circuit protection and recovery profile is shown below.

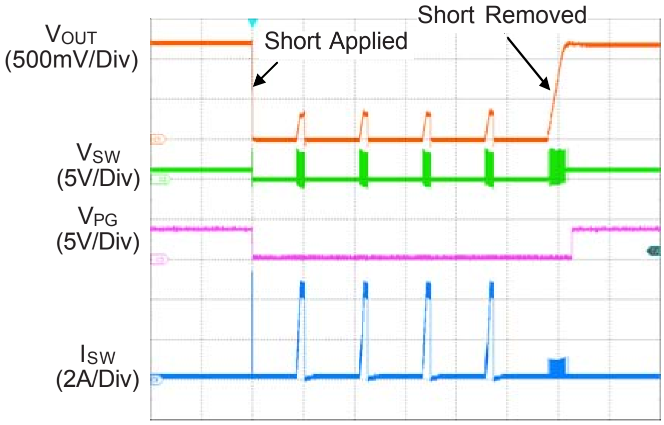


Figure 3. Short-Circuit Protection and Recovery

Output Active Discharge

When the RT5753 is disabled by EN pin, UVLO or OTP, the device discharges the output capacitors (via SW pins) through an internal discharge resistor (100Ω/50Ω) connected to ground. This function prevents the reverse current flow from the output capacitors to the input capacitors once the input voltage collapses. It doesn't need to rely on another active discharge circuit for discharging output capacitors. This function will be turned off when the fault condition is removed.

Output Undervoltage Protection

The RT5753 includes output undervoltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the undervoltage protection threshold (typically 40% of the internal feedback reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches. The RT5753 will enter output undervoltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF} (5ms/2.5ms,

Output Overvoltage Protection

The RT5753AL/BL/CL/DL/EL/FL includes an output overvoltage protection (OVP) circuit to limit output voltage and minimize output voltage overshoot. If the V_{FB} goes above the 120% of the reference voltage, the high-side MOSFET will be forced off to limit the output voltage then the IC will be into Latch-off mode.

Thermal Shutdown

The RT5753 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold (T_{SD}). Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Note that the over-temperature protection is intended to protect the device during momentary overload conditions. The protection is activated outside of the absolute maximum range of operation as a secondary fail-safe and therefore should not be relied upon operationally. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Negative Overcurrent Limit

The RT5753B/D is the part which is forced to PWM and allows negative current operation. In case of PWM operation, high negative current may be generated as an external power source which is tied to output terminal unexpectedly. As the risk described above, the internal circuit monitors negative current in each on-time interval of low-side MOSFET and compares it with NOC threshold. Once the negative current exceeds the NOC threshold, the low-side MOSFET is turned off immediately, and then the high-side MOSFET will be turned on to discharge the energy of output inductor. This behavior can keep the valley of negative current at NOC threshold to protect low-side MOSFET. However, the negative current can't be limited at NOC threshold anymore since minimum off-time is reached.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- –0.3V to 6.5V
- VIN to SW ---------- –0.3V to 6.5V
- VIN to SW ($t \leq 10ns$) ---------- –2.5V to 9V
- Switch Voltage, SW ---------- –0.3V to 6.5V
  SW ($t \leq 10ns$) ---------- –2.5V to 9V
- Other Pins ---------- –0.3V to 6.5V
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C

ESD Ratings (Note 2)

- ESD Susceptibility
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 2.5V to 6V
- Output Voltage ---------- 0.6V to V_{IN}
- Junction Temperature Range ---------- –40°C to 125°C

Thermal Information (Note 4 and Note 5)

Thermal Parameter		WDFN-8L 2x2	WDFN-8SL 2x2	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	49.5	48.2	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	167.1	158.5	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	5.8	5.5	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	49.7	49.7	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	5.01	5.01	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	30.5	30.5	°C/W

Electrical Characteristics

(V_{IN} = 3.6V. T_J = T_A = –40°C to 125°C. Typical value is tested at T_A = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		2.5	--	6	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising	2.15	2.3	2.45	V
Undervoltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	300	--	mV
Supply Current (Shutdown)	I_{SHDN}	V_{EN} = 0V	--	--	15	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.7V, not switching	--	23	35	
Soft-Start						
Soft-Start Time	t_{SS}	0%V_{OUT} to 95%V_{OUT}, RT5753A/B/E	1	1.5	2.4	ms
		0%V_{OUT} to 95%V_{OUT}, RT5753C/D/F	0.5	0.75	1.2	
Enable Voltage						
Enable Voltage Threshold	V_{EN_H}	EN high-level input voltage	0.8	--	1.2	V
	V_{EN_L}	EN low-level input voltage	0.4	--	0.85	
Enable Pull-Low Current	I_{EN_PL}		--	1.5	--	μA
Feedback Voltage						
Feedback Threshold Voltage	V_{FB}		0.594	0.6	0.606	V
Feedback Input Current	I_{FB}	V_{FB} = 0.6V, T_A = 25°C	--	0.1	0.4	μA
Internal MOSFET						
High-Side On-Resistance	$R_{DS(ON)\_H}$		--	100	120	mΩ
Low-Side On-Resistance	$R_{DS(ON)\_L}$		--	70	85	
Current Limit						
High-Side Switch Current Limit	I_{LIM_H}	V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1μH, T_A = 25°C	3.6	4.14	4.8	A
Low-Side Switch Valley Current Limit	I_{LIM_L}		3	3.45	3.9	
Switching Frequency						
Switching Frequency	f_{SW}		1	1.2	1.44	MHz
On-Time Timer Control						
Minimum Off-Time	t_{OFF_MIN}		--	90	--	ns
Output Voltage Protection						
Output Undervoltage Threshold (RT5753AH/BH/CH/DH : Hiccup) (RT5753AL/BL/CL/DL/EL/FL : Latch-Off)	V_{UVP}		--	40	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Overvoltage Threshold (RT5753AL/BL/CL/DL/EL/FL: Latch-Off, Deglitch Time = 2μs)	V_{OVP}	V_{FB} rising	110	120	130	%
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
Power Good						
Power Good High Threshold	V_{TH_PGLH}	V_{FB} rising, PG goes high	83	90	--	%
Power Good Falling Threshold	V_{TH_PGHL}	V_{FB} falling, PG goes low	78	85	--	%
Power Good Sink Current Capability		I_{PG} sinks 5mA	--	--	0.4	V
Output Discharge Resistor						
Output Discharge Switch On-Resistor (RT5753A/B/C/D)	R_{DISCHG}	V_{EN} = 0V (Protection)	--	100	--	Ω
Output Discharge Switch On-Resistor (RT5753E/F)	R_{DISCHG}	V_{EN} = 0V (Protection)	--	50	--	Ω

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

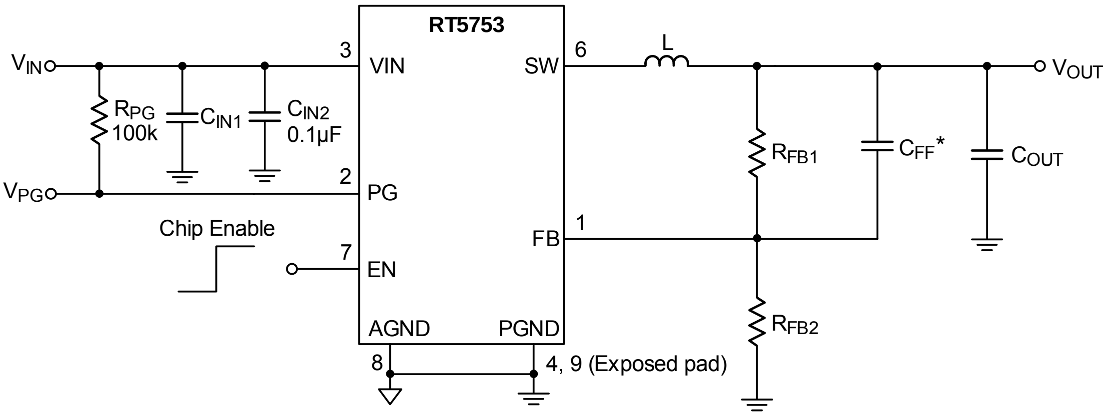
Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 5. $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and Ψ_{JB} are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

Typical Application Circuit



C_{FF}*: Optional for performance fine-tune

Table 2. Suggested Component Values

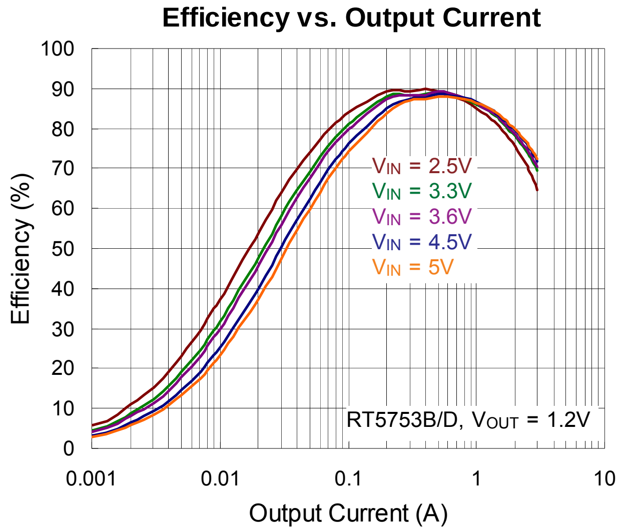
V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	C_{IN1} (μF)	L (μH)	C_{OUT} (μF)	C_{FF} (pF)
3.3	100	22.1	22	1	44 to 66	--
1.8	100	50	22	1	44 to 66	--
1.5	100	66.6	22	1	44 to 66	--
1.2	100	100	22	1	44 to 66	22
1.05	100	133	22	1	44 to 66	22
1	100	148	22	1	44 to 66	22

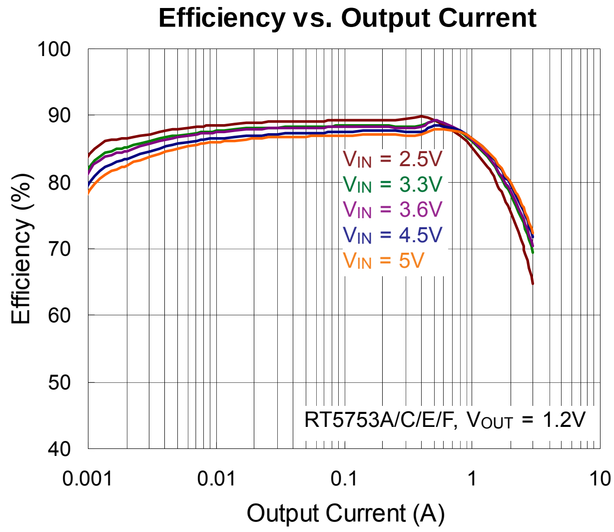
Table 3. Recommended External Components

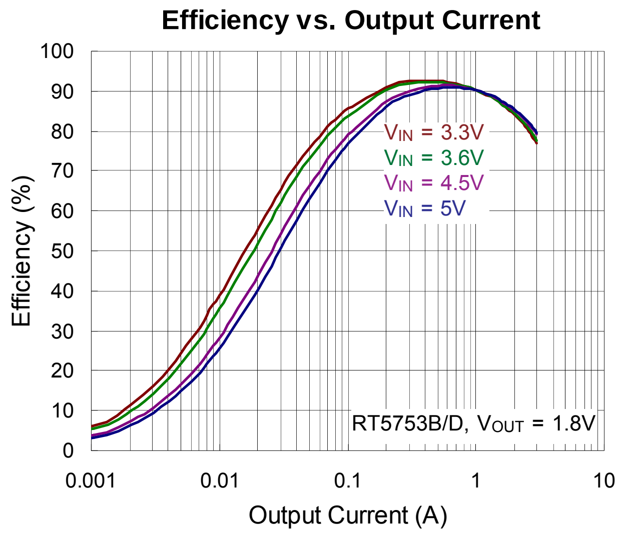
Component	Description	Vendor P/N
C_{IN}	22μF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (MURATA)
C_{OUT}	22μF, 6.3V, X5R, 0603	GRM188R60J226MEA0D (MURATA)
L	1μH	DFE322512F-1R0M (MURATA)

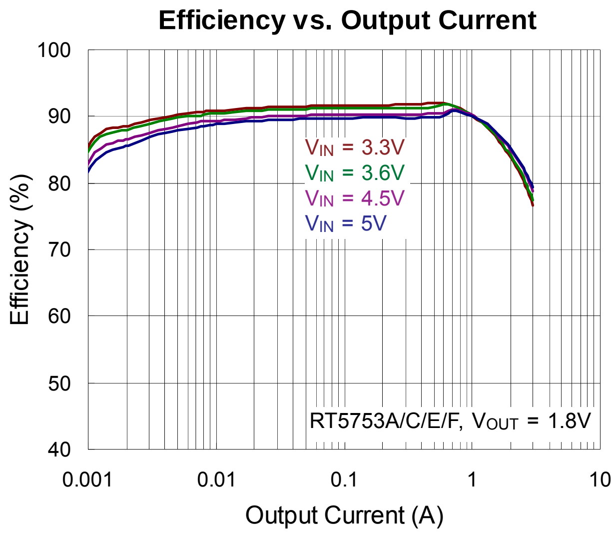
C_{OUT} and C_{IN} : Considering the effective capacitance de-rated with biased voltage level and size, the C_{OUT} and C_{IN} components need to satisfy the effective capacitance which corresponding to recommended external components.

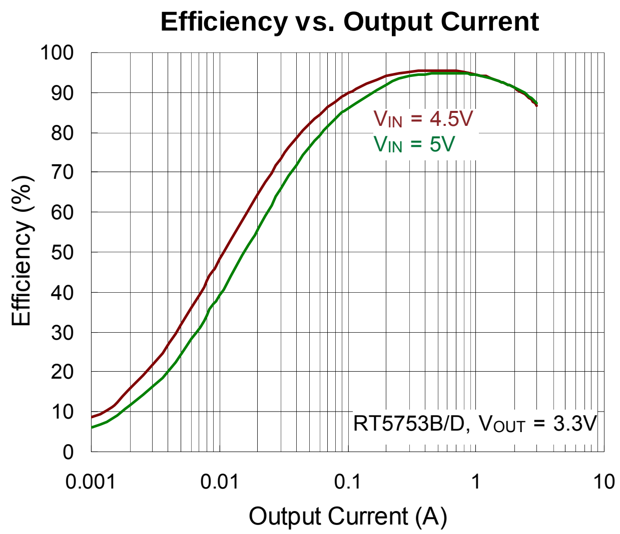
Typical Operating Characteristics

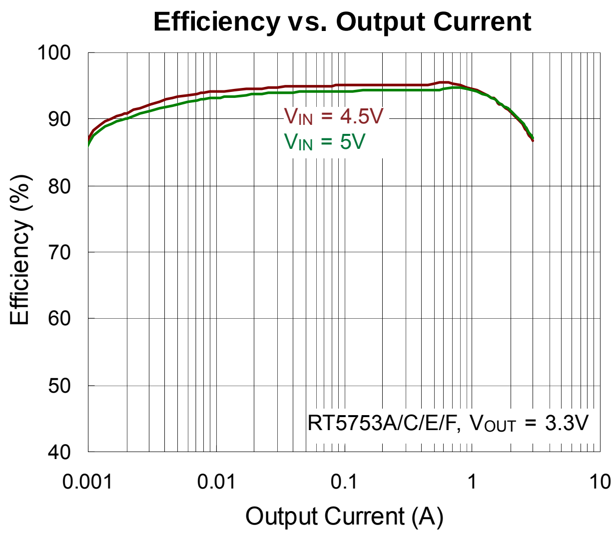


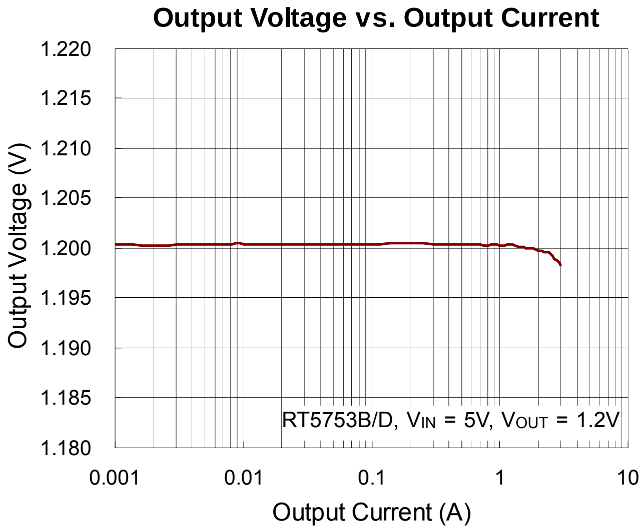


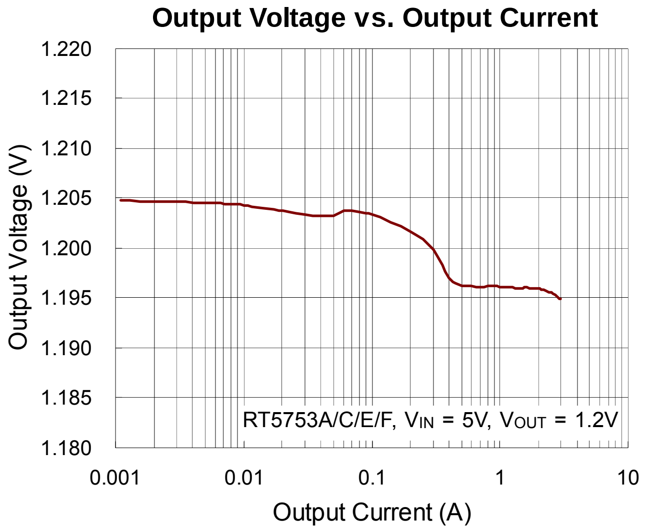


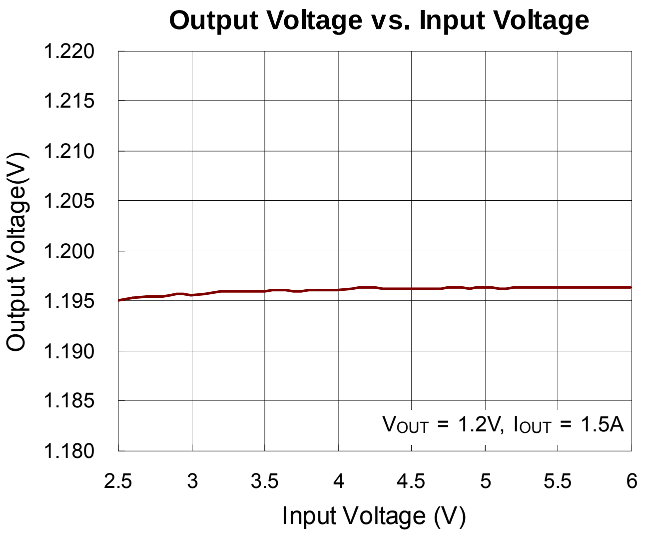


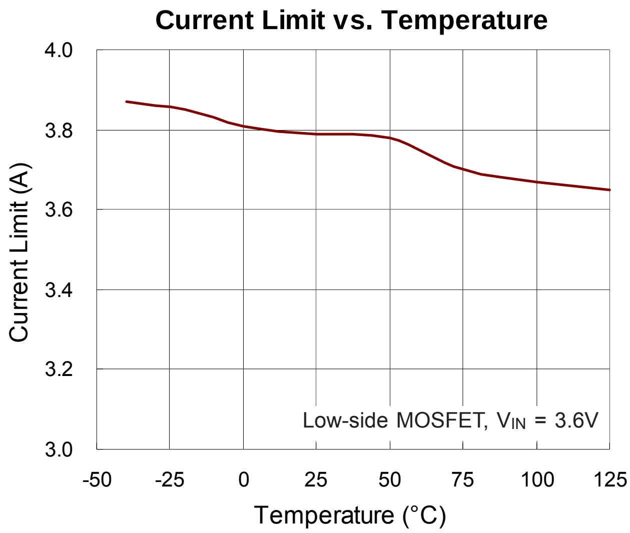


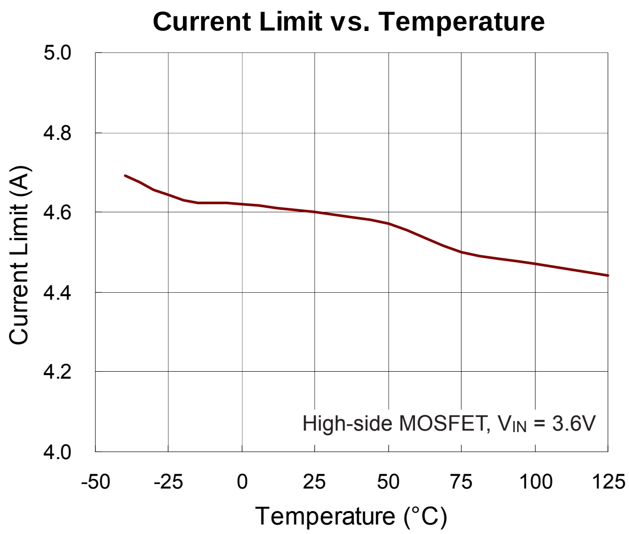


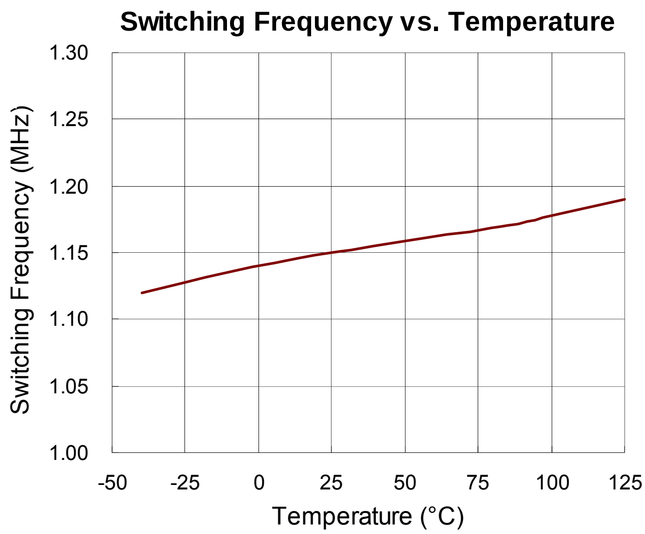

Output Voltage vs. Output Current
Output Voltage (V)
1.220
1.215
1.210
1.205
1.200
1.195
1.190
1.185
1.180
0.001
0.01
0.1
1
10
Output Current (A)
RT5753B/D, VIN = 5V, VOUT = 1.2V


Output Voltage vs. Output Current
Output Voltage (V)
1.220
1.215
1.210
1.205
1.200
1.195
1.190
1.185
1.180
0.001
0.01
0.1
1
10
Output Current (A)
RT5753A/C/E/F, VIN = 5V, VOUT = 1.2V

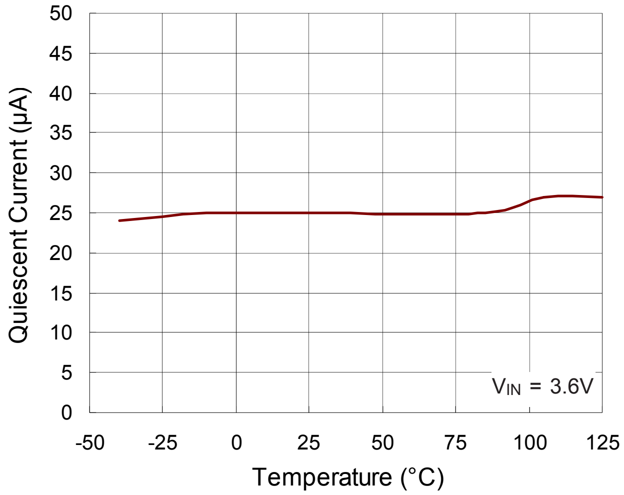

Output Voltage vs. Input Voltage
Output Voltage(V)
1.220
1.215
1.210
1.205
1.200
1.195
1.190
1.185
1.180
2.5
3
3.5
4
4.5
5
5.5
6
Input Voltage (V)
VOUT = 1.2V, IOUT = 1.5A


Current Limit vs. Temperature
Current Limit (A)
4.0
3.8
3.6
3.4
3.2
3.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
Low-side MOSFET, VIN = 3.6V

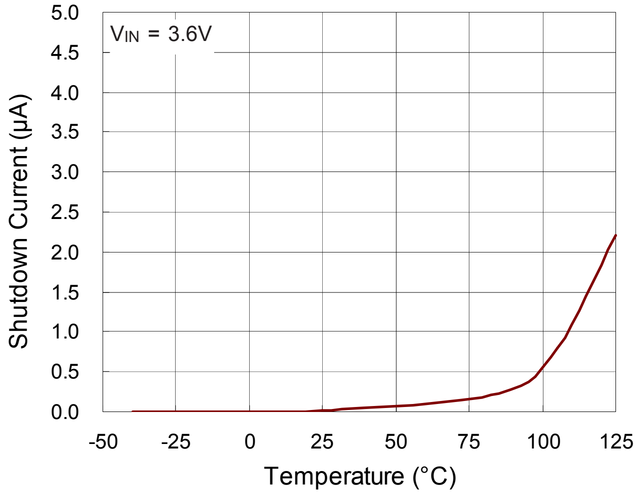

Current Limit vs. Temperature
Current Limit (A)
5.0
4.8
4.6
4.4
4.2
4.0
-50
-25
0
25
50
75
100
125
Temperature (°C)
High-side MOSFET, VIN = 3.6V


Switching Frequency vs. Temperature
Switching Frequency (MHz)
1.30
1.25
1.20
1.15
1.10
1.05
1.00
-50
-25
0
25
50
75
100
125
Temperature (°C)

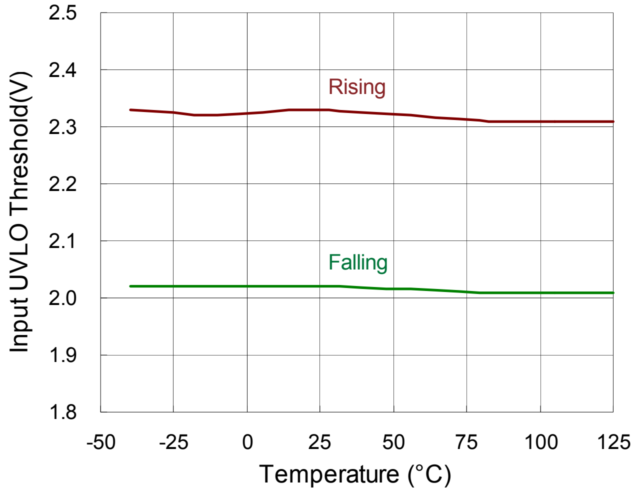
Quiescent Current vs. Temperature



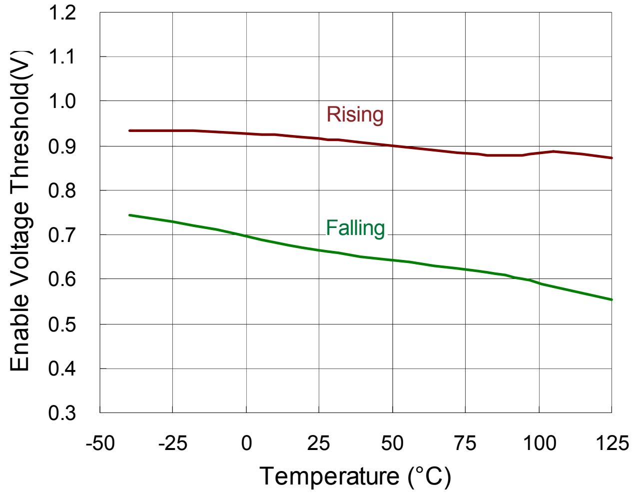
Shutdown Current vs. Temperature



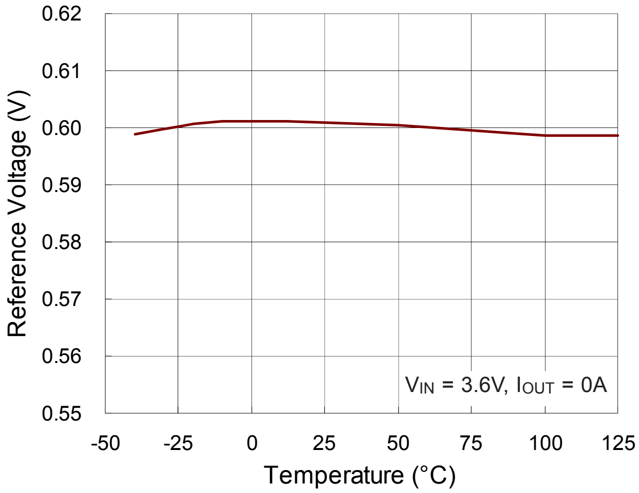
Input UVLO Threshold vs. Temperature



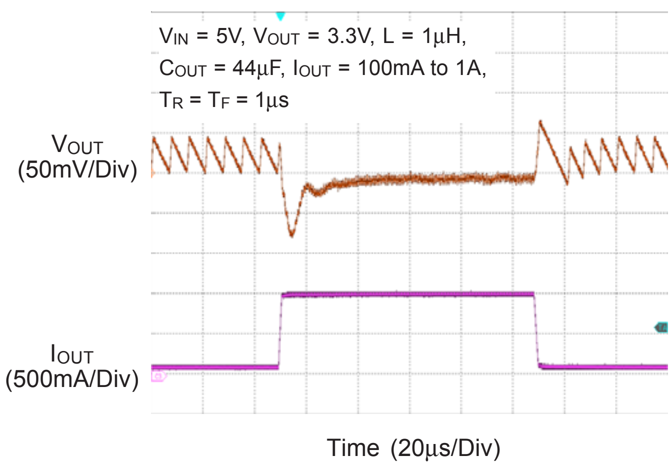
Enable Voltage Threshold vs. Temperature



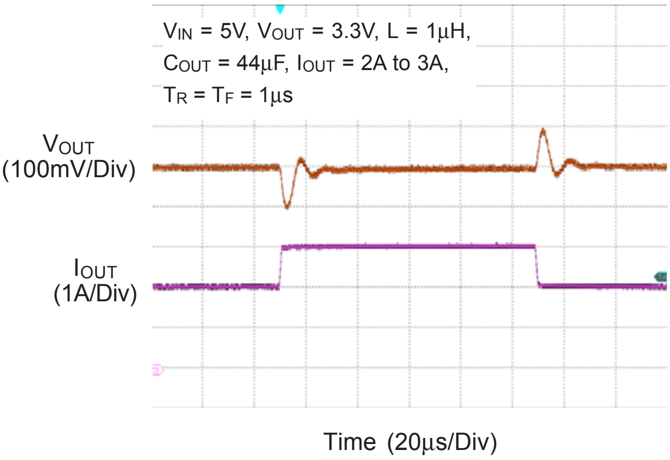
Reference Voltage vs. Temperature



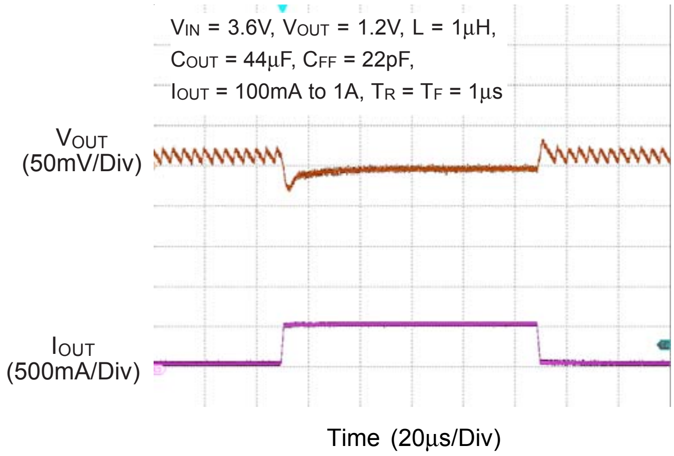
Load Transient Response



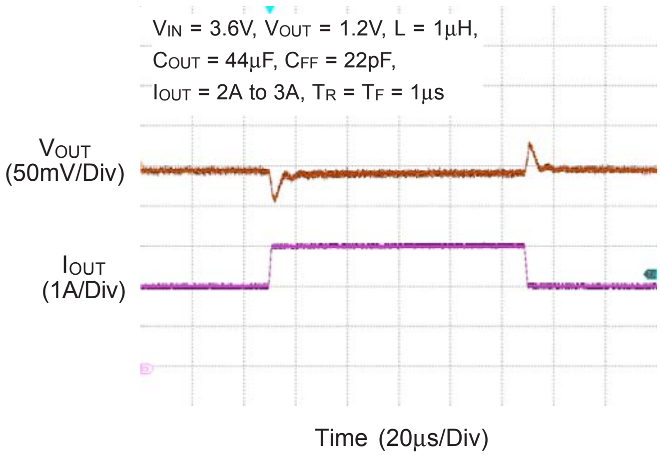
Load Transient Response



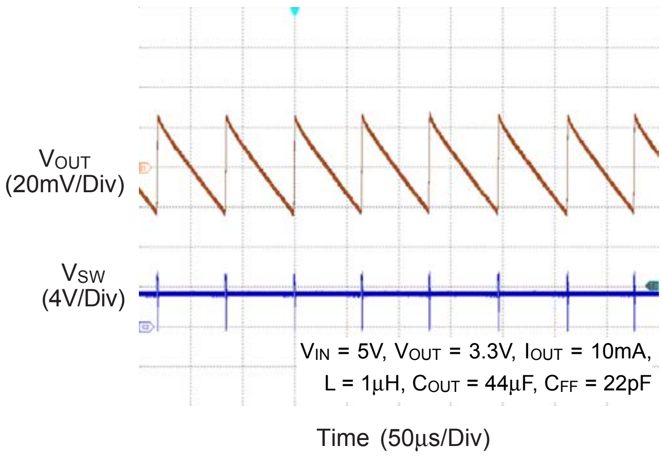
Load Transient Response



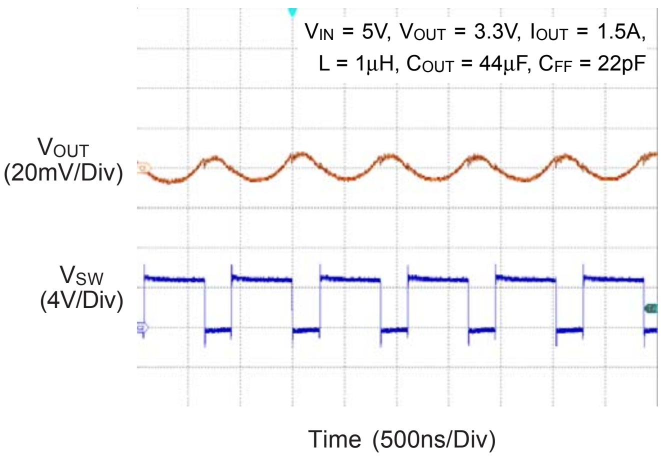
Load Transient Response



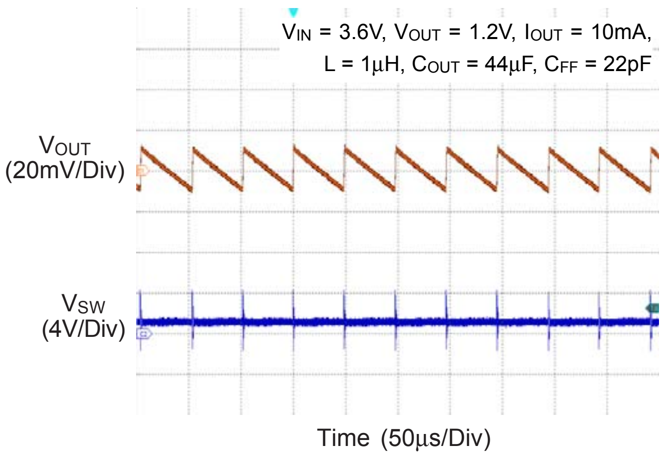
Output Ripple Voltage



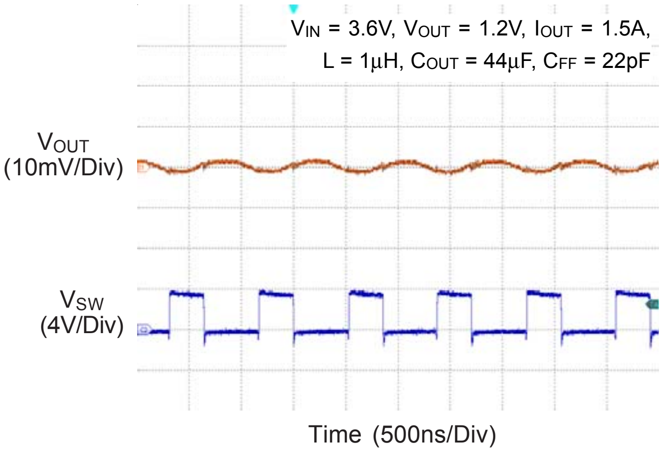
Output Ripple Voltage



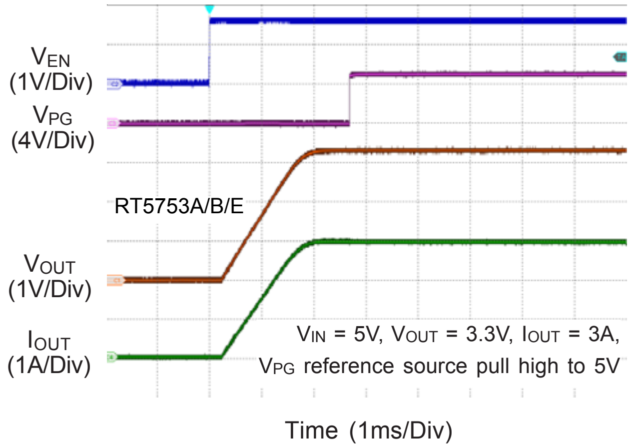
Output Ripple Voltage



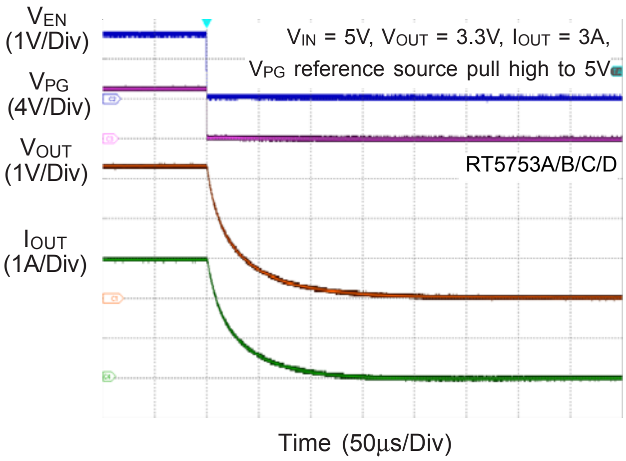
Output Ripple Voltage



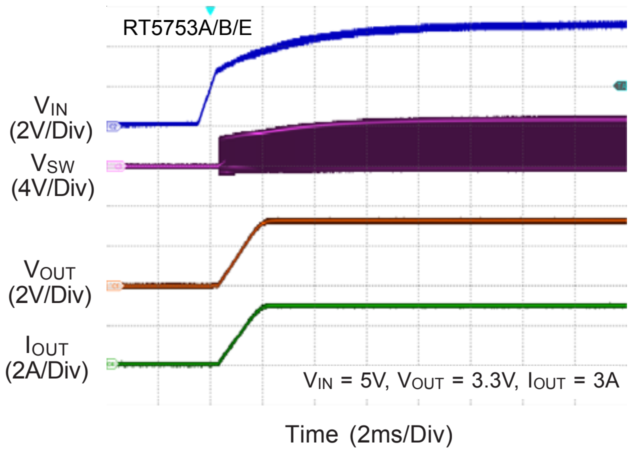
Power On from EN



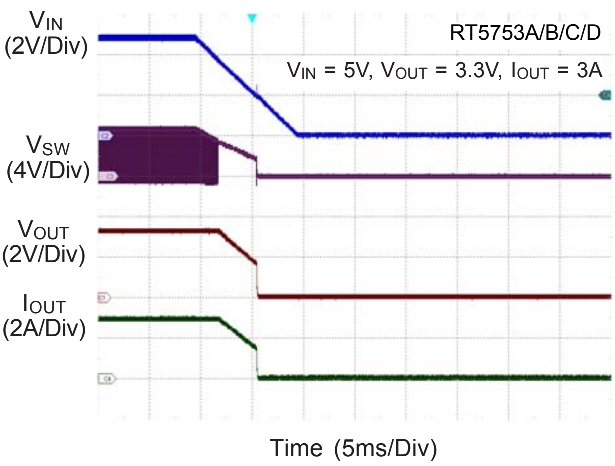
Power Off from EN



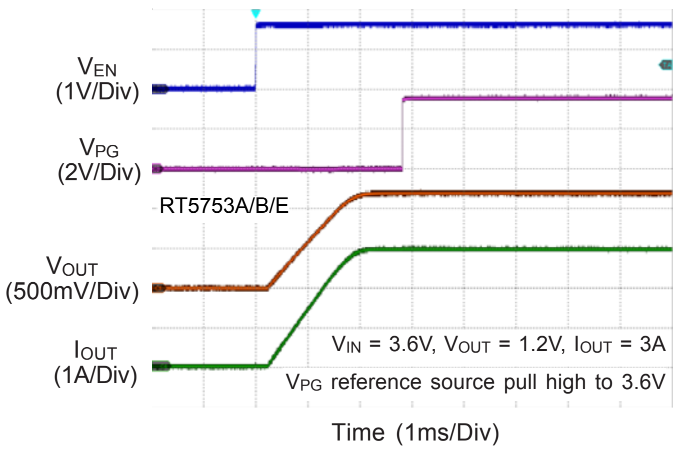
Power On from VIN



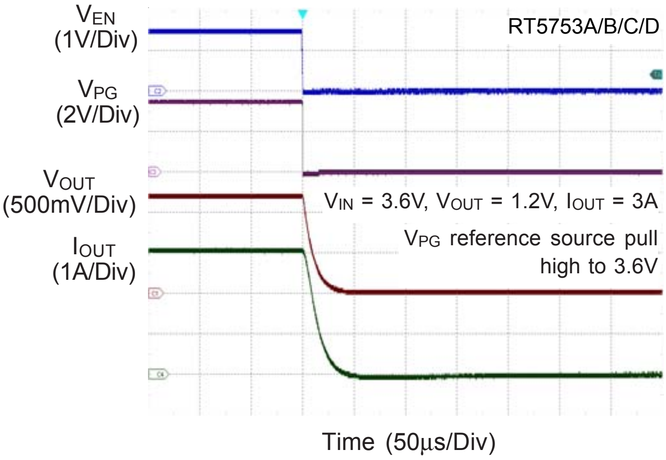
Power Off from VIN



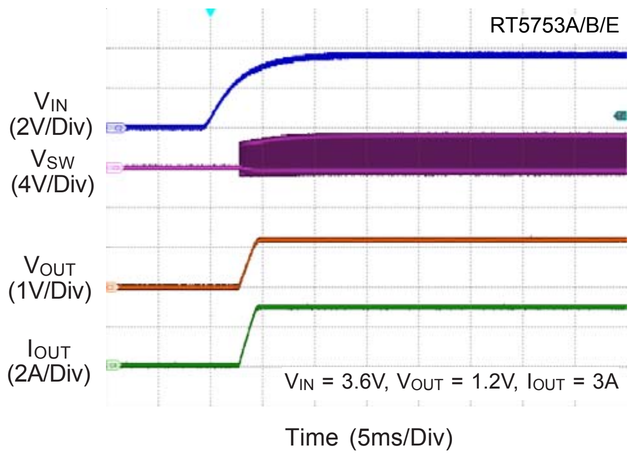
Power On from EN



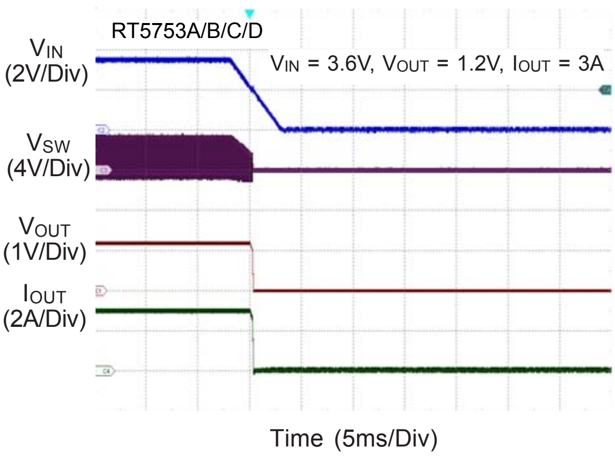
Power Off from EN



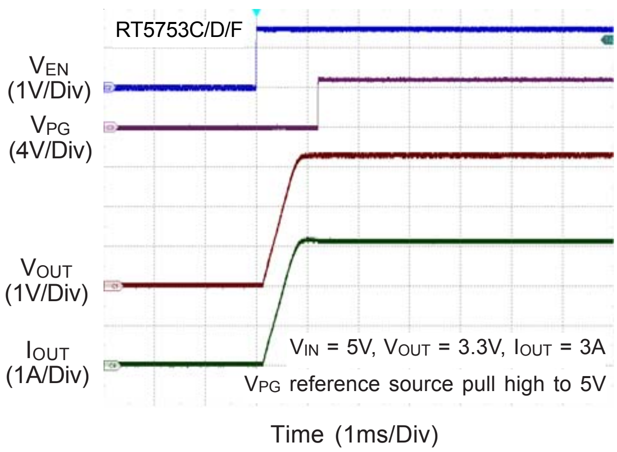
Power On from VIN



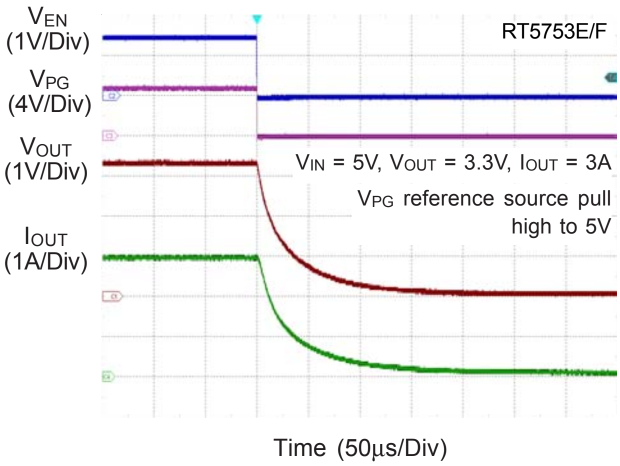
Power Off from VIN



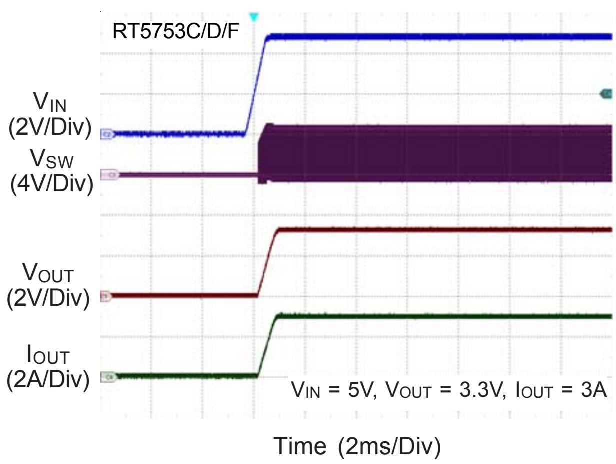
Power On from EN



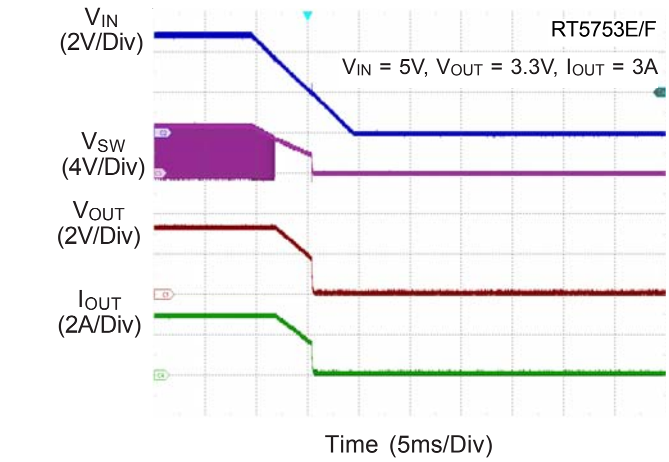
Power Off from EN



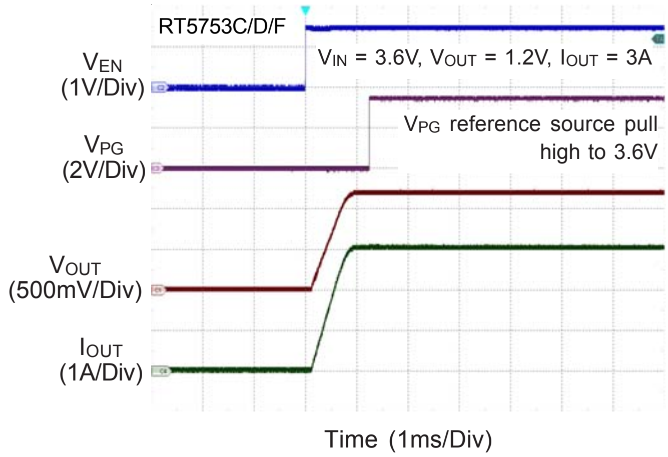
Power On from VIN



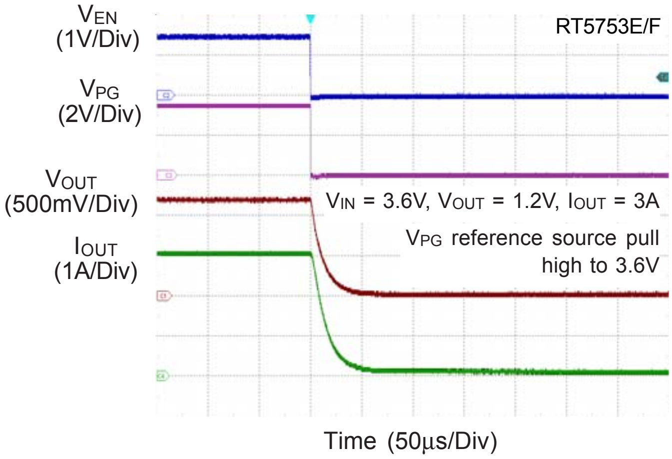
Power Off from VIN



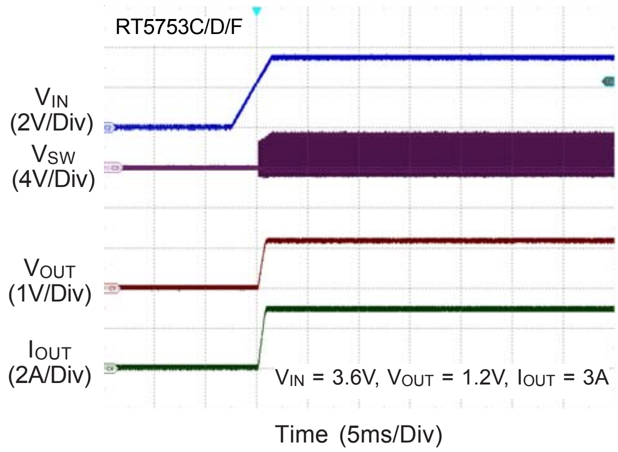
Power On from EN



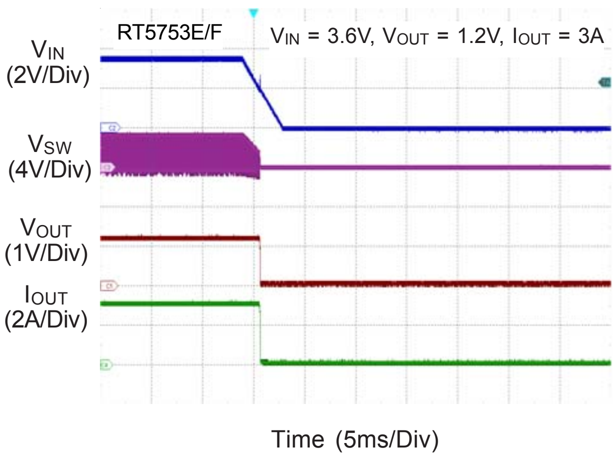
Power Off from EN



Power On from VIN



Power Off from VIN



Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and to ensure the functional suitability of their components and systems.

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Generally, three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (DCR).

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 50% of the IC rated current. The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value as follows :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2} \Delta I_L$$

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level. Besides, the current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

For the selected inductor, the inductor's saturation and thermal rating should meet or greater than the ripple current (ΔI_L). For more conservative, the rating for inductor saturation current must be equal to or greater than switch current limit of the device rather than the inductor peak current.

For EMI sensitive application, choosing shielding type inductor is preferred.

Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The waveform of C_{IN} ripple voltage and ripple current are shown in Figure 4. The peak-to-peak voltage ripple on input capacitor can be estimated as equation below :

$$\Delta V_{CIN} = D \times I_{OUT} \times \frac{1-D}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR$$

where

$$D = \frac{V_{OUT}}{V_{IN} \times \eta}$$

For ceramic capacitors, the equivalent series resistance (ESR) is very low, the ripple which is caused by ESR can be ignored, and the minimum input capacitance can be estimated as equation below :

$$C_{IN\_MIN} = I_{OUT\_MAX} \times \frac{D(1-D)}{\Delta V_{CIN\_MAX} \times f_{SW}}$$

where ΔV_{CIN_MAX} is maximum input ripple voltage.

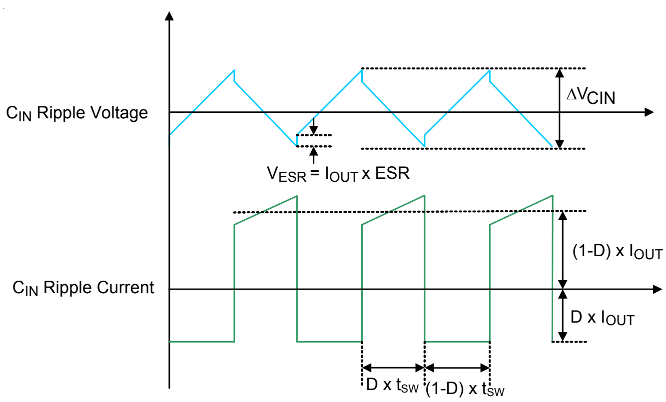


Figure 4. C_{IN} Ripple Voltage and Ripple Current

In addition, the input capacitor needs to have a very low ESR and must be rated to handle the worst-case RMS input current of :

$$I_{RMS} \cong I_{OUT\_MAX} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

It is common to use the worse $I_{RMS} \cong I_{OUT}/2$ at $V_{IN} = 2V_{OUT}$ for design. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size, height and thermal requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Ceramic capacitors are ideal for switching regulator applications because of its small size, robustness and very low ESR. However, care must be taken when these capacitors are used at the input. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the RT5753 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided by placing the low ESR ceramic input capacitor in parallel with a bulk capacitor with higher ESR to damp the voltage ringing.

The input capacitor should be placed as close as possible to the VIN pins, with a low inductance connection to the GND of the IC. In addition to a larger bulk capacitor, a small ceramic capacitors of 0.1μF should be placed close to the VIN and GND pin. This capacitor should be 0402 or 0603 in size.

Output Capacitor Selection

The RT5753 are optimized for ceramic output capacitors and best performance will be obtained by using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on load apply) and soar (overshoot on load release).

Output Ripple

The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage V_{RIPPLE}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple $V_{RIPPLE(ESR)}$ and capacitive ripple $V_{RIPPLE(C)}$, and can be expressed as below :

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT® transient response is very quick and output transients are usually small. The following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formula to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor :

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT® control scheme will ramp the current using on-times spaced apart with minimum off-times, which is as fast as allowed. Calculate the approximate on-time (neglecting parasites) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{OUT}\right)}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Because some modern digital loads can exhibit nearly instantaneous load changes, the amplitude of the ESR step up or down should be taken into consideration.

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB, as shown in Figure 5. The output voltage is set according to the following equation :

$V_{OUT} = 0.6V \times (1 + R_{FB1} / R_{FB2})$

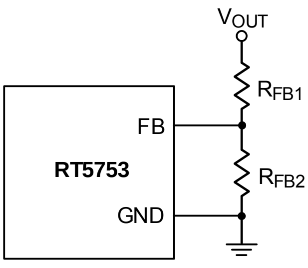


Figure 5. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. For output voltage accuracy, use divider resistors with 1% or better tolerance.

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin can be connected to the input supply V_{IN} directly. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 6, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 7. In this case, a pull-up resistor, R_{EN}, is connected between VIN and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when VIN is smaller than the VOUT target level or some other desired voltage level, a resistive divider (R_{EN1} and R_{EN2}) can be used to externally set the input undervoltage lockout threshold, as shown in Figure 8.

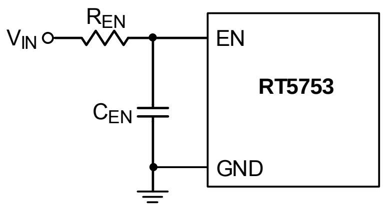


Figure 6. Enable Timing Control

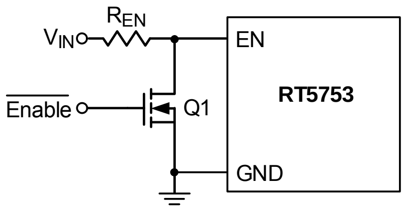


Figure 7. Logic Control for the EN Pin

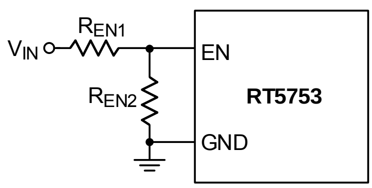


Figure 8. Resistive Divider for Undervoltage Lockout Threshold Setting

Power-Good Output

The PG pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor.

The external voltage source can be an external voltage supply below 6V, V_{CC} or the output of the RT5753 if the output voltage is regulated under 6V. It is recommended to connect a 100kΩ between external voltage source to PG pin.

Feedforward Capacitor (C_{FF})

The RT5753 is optimized for low duty-cycle applications, and the control loop is stable with low ESR ceramic output capacitors. This optimization makes circuit easily to achieve stability with reasonable output capacitors, but it also narrows the optimization of transient responses of the converter. In higher duty-cycle applications (higher output voltages or lower input voltage), the internal ripple signal will increase in amplitude. Before the ACOT® control loop can react to an output voltage fluctuation, the voltage change on the feedback signal must exceed the internal ripple amplitude. Because of the large internal ripple in this condition, the response may become too slow and may show an under-damped response. This can cause some ringing in the output and is especially visible at higher output voltage applications where duty-cycle is high. The feedback network attenuation is large, adding to the delay. As shown in Figure 9, adding a feedforward capacitor (C_{FF}) across the upper feedback resistor is recommended. This increases the damping of the control system.

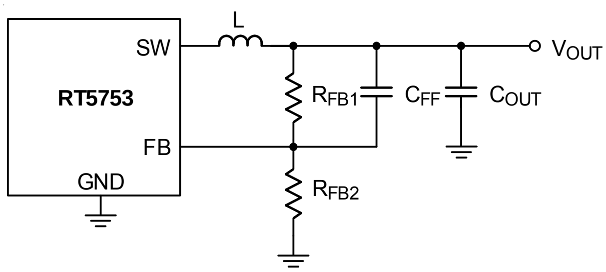


Figure 9. Feedback Loop with Feedforward Capacitor

Loop stability can be checked by viewing the load transient response. A load step with a speed that exceeds the converter bandwidth must be applied. For ACOT®, loop bandwidth can be in the order of 100 to 200kHz, so a load step with 500ns maximum rise time (di/dt ≈ 2A/μs) ensures the excitation frequency is sufficient. It is important that the converter operates in PWM mode, outside the light load efficiency range, and below any current limit threshold. A load transient from 30% to 60% of maximum load is reasonable which is shown in Figure 10.

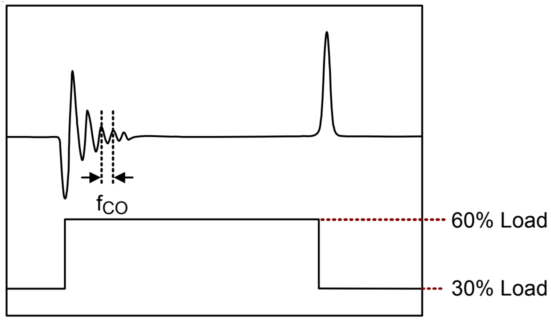


Figure 10. Example of Measuring the Converter f_{CO} by Fast Load Transient

C_{FF} can be calculated base on below equation :

$$C_{FF} = \frac{1}{2\pi \times f_{CO}} \times \sqrt{\frac{1}{R_{FB1}} \times \left(\frac{1}{R_{FB1}} + \frac{1}{R_{FB2}}\right)}$$

Note that, after defining the C_{FF}, please also check the load regulation because the feedforward capacitor might inject an offset voltage into V_{OUT} to cause V_{OUT} inaccuracy. If the output voltage is over specification caused by calculated C_{FF}, please decrease the value of feedforward capacitor C_{FF}.

Figure 11. shows the transient performance with and without feedforward capacitor.

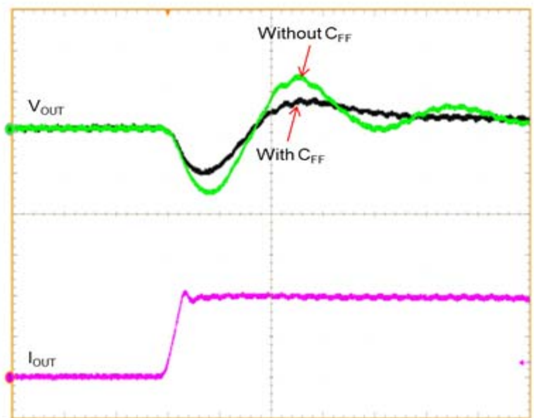


Figure 11. Load Transient Response with and without Feedforward Capactior

Thermal Considerations

In many applications, the RT5753 does not generate much heat due to its high efficiency and low thermal resistance of its WDFN-8L 2x2 and WDFN-8SL 2x2 packages. However, in applications which the RT5753 runs at a high ambient temperature and high input voltage or high switching frequency, the generated heat may exceed the maximum junction temperature of the part. The junction temperature should never exceed the absolute maximum junction temperature of the part.

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. If the junction temperature reaches approximately 150°C, the RT5753 stops switching the power MOSFETs until the temperature cools down by 20°C.

The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA(EFFECTIVE)}$

where $T_{J(MAX)}$ is the maximum junction temperature of the die. For recommended operating condition specifications, the maximum junction temperature is 150°C. T_A is the ambient temperature, and $\theta_{JA(EFFECTIVE)}$ is the system-level junction to ambient thermal resistance. It can be estimated from thermal modeling or measurements in the system.

The thermal resistance of the device strongly depends on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground. The addition of backside copper with thermal vias, stiffeners, and other enhancements can also help reduce thermal resistance.

Experiments in the Richtek thermal lab show that simply set $\theta_{JA(EFFECTIVE)}$ as 110% to 120% of the θ_{JA} is reasonable to obtain the allowed $P_{D(MAX)}$.

As an example, consider the case when the RT5753 is used in applications where V_{IN} = 5V, I_{OUT} = 3A, f_{SW} = 1.2MHz, V_{OUT} = 1.2V. The efficiency at 1.2V, 3A is 74.2% by using WE-74437324010 (1μH, 22mΩ DCR) as the inductor and measured at room temperature. The core loss, 16.5mW, can be obtained from its website in this case. In this case, the power dissipation of the RT5753 is

$$P_{D,\,RT} = \frac{1-\eta}{\eta} \times P_{OUT} - \left(I_O^{\,2} \times DCR + P_{CORE}\right) = 1.03W$$

Considering the $\theta_{JA(EFFECTIVE)}$ is 59.64°C/W by using the RT5753 evaluation board with 4 layers PCB, all layers with 1 oz. Cu, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately :

T_J = 1.03W x 59.64°C/W + 25°C = 86.4°C

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the device.

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path comprising of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible. This practice is essential for high efficiency.
- Place the input MLCC capacitors as close to the VIN and PGND pins as possible. The major MLCC capacitors should be placed on the same layer as the RT5753.
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Place the feedback components next to the FB pin.
- For better thermal performance, design a wide and thick plane for PGND pin or add a lot of vias to GND plane.
- AGND and PGND are connected with a via and at only one point to reduce circulating currents.

An example of PCB layout guide is shown from Figure 12.

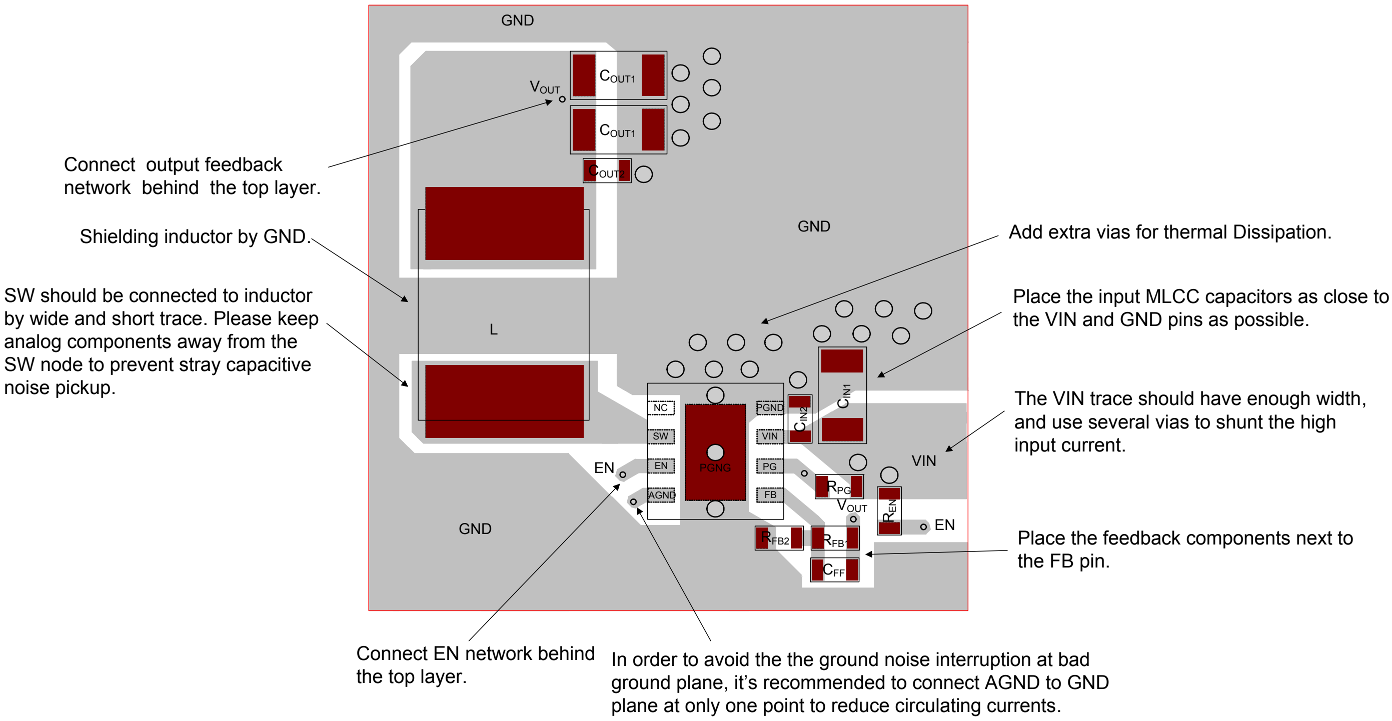
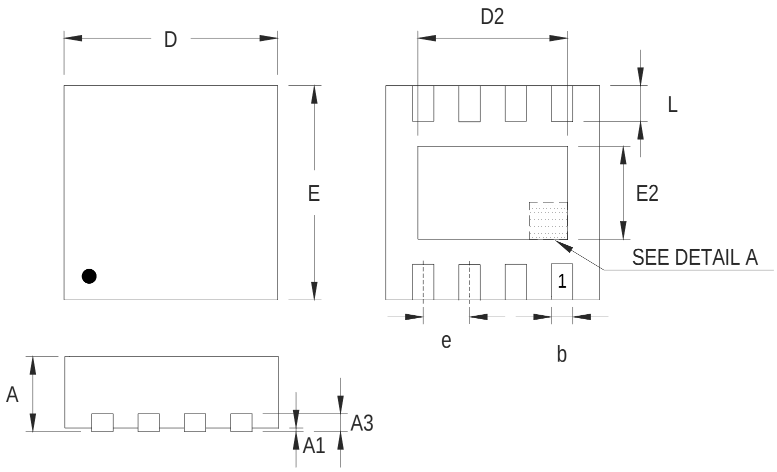
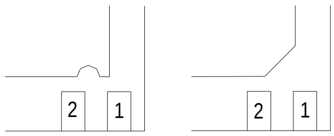


Figure 12. Layout Guide

Outline Dimension





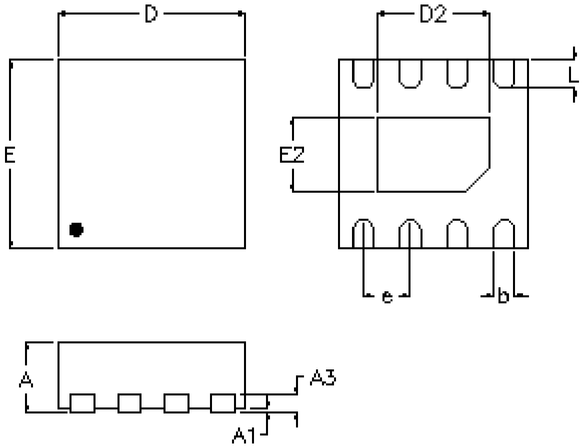
DETAIL A

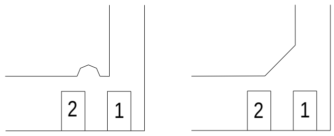
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package





DETAIL A

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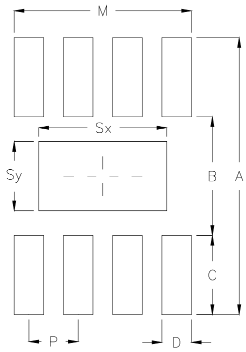
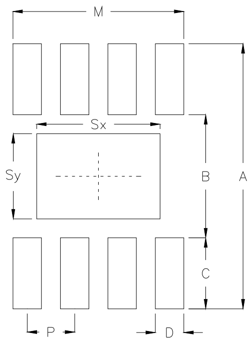
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.200	0.300	0.008	0.012
D		1.900	2.100	0.075	0.083
D2	Option1	1.150	1.250	0.045	0.049
	Option2	1.550	1.650	0.061	0.065
E		1.900	2.100	0.075	0.083
E2	Option1	0.750	0.850	0.030	0.033
	Option2	0.850	0.950	0.033	0.037
e		0.500		0.020	
L		0.250	0.350	0.010	0.014

W-Type 8SL DFN 2x2 Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8	8	0.50	2.80	1.20	0.80	0.30	1.30	0.70	1.80	±0.05



Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
V/W/U/XDFN2*2-8S	Option1	8	0.50	2.80	1.30	0.75	0.30	1.30	0.90	1.80	±0.05
	Option2							1.60	0.90		

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Datasheet Revision History

Version	Date	Description	Item
04	2023/1/10	Modify	Add RT5753EL, RT5753FL General Description on P1 Features on P1 Simplified Application Circuit on P1 Ordering Information on P2 Marking Information on P4 Functional Block Diagram on P5 Operation on P6, 7, 8, 9 Electrical Characteristics on P11, 12 Typical Application Circuit on P13 Typical Operating Characteristics on p14 Application Information on P21